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Performance Analysis of CMOS, PTL and GDI Based Braun Multiplier for Signal Processing Applications

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***Abstract*—Power, speed and area are key design constraints in signal processing for computing applications as well as for handy electronic gadgets. Multiplier plays a significant role in energy efficient signal processing applications in digital systems. Product of large bit numbers occurs efficiently through binary multiplication. A low power and high speed Gate Diffusion Input (GDI) based Braun multiplier with improved row and column bypassing scheme is presented in this paper. From the simulated results, it is observed that, the GDI based Braun multiplier achieves energy savings more than 4% and up to 99% with CMOS and other methods and in the same way EDP savings more than 15% and up to 30% with CMOS and other methods by means of column and row bypassing techniques. From the layout, it is also analyzed that, GDI Braun multiplier is area efficient over CMOS and its other counter parts at the penalty of 9% more area in comparison with pass transistor logic (PTL) based column and row bypassing techniques.**

Keywords—CMOS, PTL, GDI, Braun Multiplier, Area, Energy, EDP

I. INTRODUCTION

Multiplication is the process of adding the number to itself repeatedly for specific number of times. Hence, obtained result is known as a product. Many multiplication techniques exist in nature, but the efficient and the fastest one makes the work easier. Binary multipliers [1] are the fastest and there exist only 0 and 1. Numbers with large bits are multiplied through binary multiplication. Binary multiplication is the process of converting the input of a multiplier into binary value and then processing them bitwise. Recent digital systems include a parallel multiplication entity to carry out high speed mathematical operations. Parallel array [2] multipliers are employed to attain high speed and low power consumption. Generally Braun's multiplier is most widely used parallel array multiplier. The Braun's multiplier consists of1 ripple carry adder and (n-1) carry save adders [3] in his basic form and alternatively it is also named as carry save array multiplier. The principle operation of carry save adder is same as full adder. The most significant characteristics of CMOS logic style is low static power consumption [4] and high noise immunity. The major drawback of CMOS logic circuits, it uses extra transistors, which increases area and delay. A well-liked and broadly used substitute to CMOS logic is PTL, which minimize the transistor count needed to realize logic functions [5-6].The main drawback of PTL logic is, lower speed and condensed voltage swing. The GDI [7] is an alternative design technique which enhances the logic swing and decrease static power dissipation. One such method is GDI logic style based multiplication. By employing GDI technique, more than a few logic functions can be implemented by means of fewer transistors. To design a fast and low-power circuits, GDI technique is appropriate choice for designers with less number of transistors and improved performance.

II. CONVENTIONAL CMOS BRAUN MULTIPLIER

Multipliers play a vital role in today's arithmetic applications. With tremendous development in technology, many researchers are focusing on, to design efficient multipliers and making them suitable for VLSI implementation [8]. The simplest parallel multiplier is the Braun array multiplier [9], [16] which is shown in figure 1. Here, all the partial products are evaluated in parallel and then composed through a series of carry save adders which have developed based on voltage level shifting to ensure power consumption [10-15].

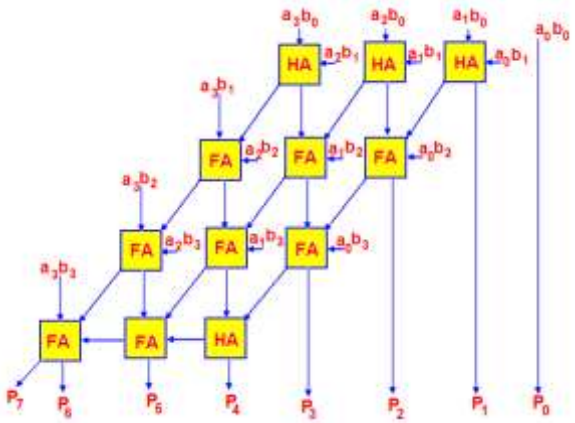

Fig. 1. Schematic diagram of Braun Multiplier

The execution time is restricted by the deepness of the carry save array, and propagation. The Braun multiplier removes the extra correction circuitry and also the number of adders needed is less.

III. SIMULATION OF MULTIPLIERS

A. CMOS Braun Multiplier

The schematic depicted in figure 2 is a C-CMOS Braun multiplier with input and output pins. Figure 3 shows the pre layout timing diagram after the simulation for C- CMOS

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Braun multiplier at 65 nm technology. For all the inputs the supply voltage of 1voltwere given and the layout after the post layout simulations of the CMOS Braun multiplier depicted in figure 4.The multiplier consists of new adder architecture which is also responsible for reducing the power consumption. Reduction in power consumption is obtained by disabling the supply voltage of non-functional blocks when the operands of the multiplicands are zero.

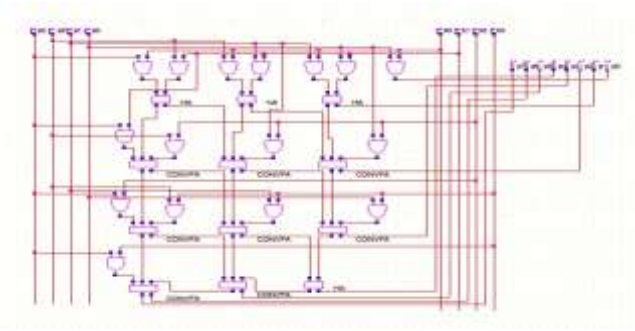

Fig. 2. CMOS Braun Multiplier logic

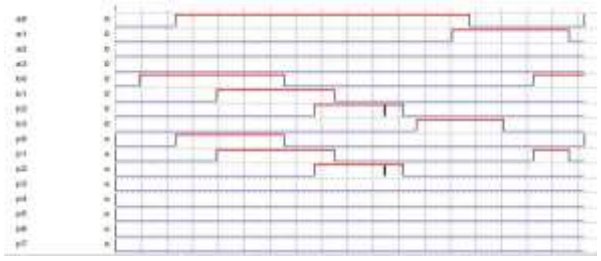

Fig. 3. CMOS Braun multiplier–pre layout timing diagram

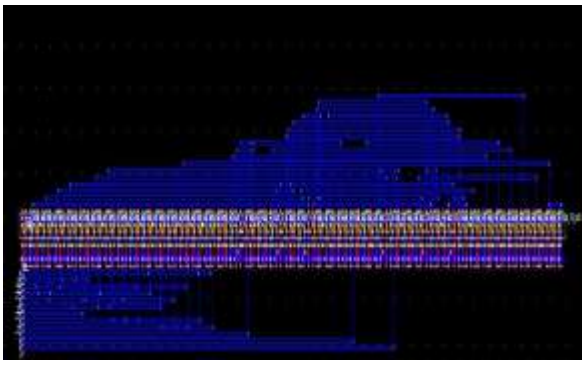

Fig. 4. CMOS Braun multiplier–Layout diagram

B. PTL Braun Multiplier

The schematic of column by passing Braun multiplier with PTL logic is shown in figure 5 with input and output pins. Thepre layout timing diagram after the simulation for the Braun multiplier with PTL logic at 65 nm technologyis shown in figure 6. The simulation has been carried out at a supply voltage of 1 voltsand the layout after the post layout simulations of the PTL logic with column by passing Braun multiplier depicted in figure 7.

C. GDI Braun Multiplier

Gate Diffusion Input logic is a bit advanced cell over CMOS technology. Leakage of Gate which is a drawback of CMOS technology has been reduced by this architecture which is shown in below figure 8.

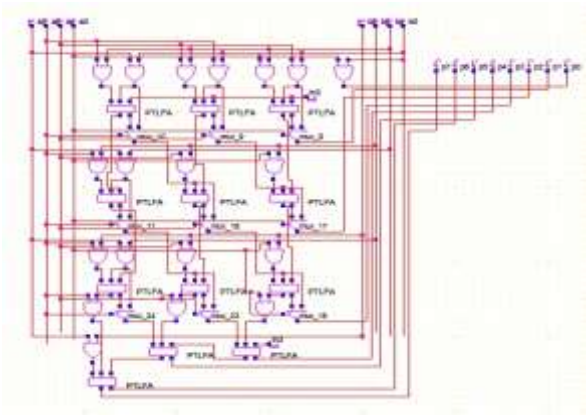

Fig. 5. PTL Braun Multiplier logic–Column by passing

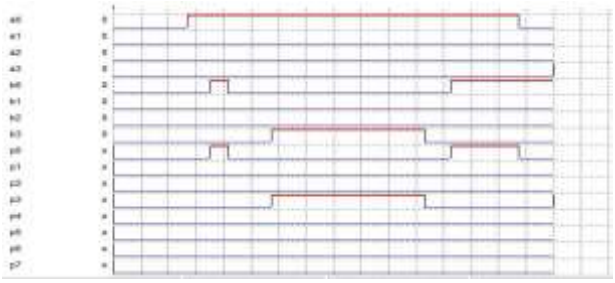

Fig. 6. PTL logic –Column by passing -pre layout timing diagram

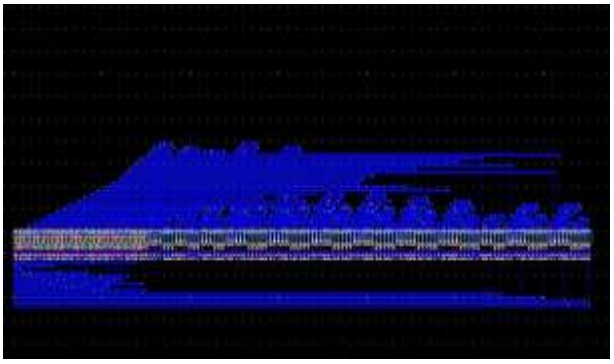

Fig. 7. PTL logic - Layout diagram–Column by passing

Due to the arrangements of terminals G, P and N, the number of logics functions, that can be implemented with this circuit are increased.

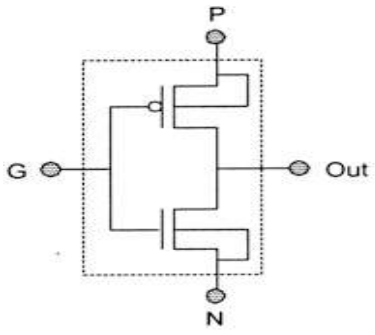

Fig. 8. Basic GDI cell

This reduces the hardware utilization with extra bits of logic. The functional truth table of GDI cell is shown in Table 1.This multiplier reduces the hardware which is required for a specific circuit, and basically used for 16 bit multiplication.

This technique is used to increase the speed of the digital circuits with minimal propagation delay.

TABLE I. GDI CELL BASED DIFFERENT LOGIC FUNCTIONS

P	N	G	Output	Function
B	'1'	A	A+B	OR
'0'	B	A	A.B	AND
B	C	A	A(bar)B+AC	MUX
'1'	'0'	A	A(bar)	NOT
'1'	B (bar)	A	(A+B)(bar)	NOR
B (bar)	'0'	A	(A.B)(bar)	NAND
B	B (bar)	A	A(bar)B+A.B(bar)	EXOR
B (bar)	B	A	A.B+A.B(bar)	EXNOR

Two's complement is the technique of converting 1's into 0's and 0's into 1's. A generator which is used for this process is known as two's complement generator. A multiplicand is given as an input to the two's complement generator. All the bits of two's complement generator are replaced with their complement bits and obtained result is returned to the multiplier. As GDI multiplier is a binary multiplier all thedigits involved in the multiplication are converted into binary system. Consider the following example to understand the process of two's complement generator. If value of n=1010, which is a binary value of decimal 10, then its two's complement includes 0110 which is the binary value of decimal 6. In this way two's complement generator works.

The schematic of row by passing Braun multiplier with GDI logic is shown in figure 9 with input and output pins. The pre layout timing diagram after the simulation for the Braun multiplier with PTL logic at 65 nm technologyis shown in figure 10. The simulation has been carried out at a supply voltage of 1 volts and the layout after the post layout simulations of the PTL logic with row by passing Braun multiplier depicted in figure 11.

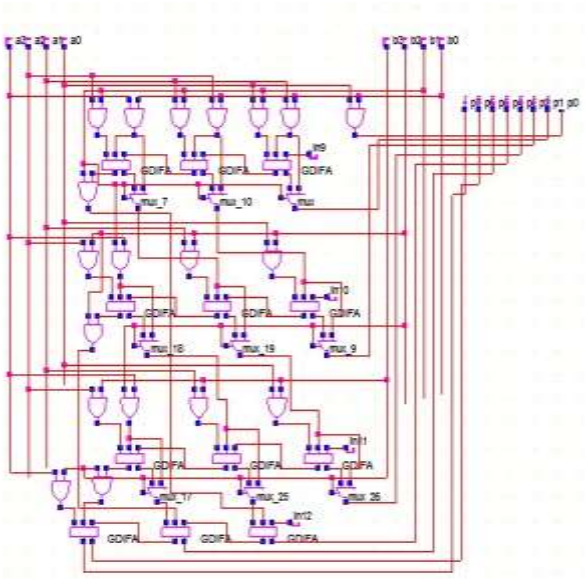

Fig. 9. GDI Braun Multiplier –Technique–Row by passing

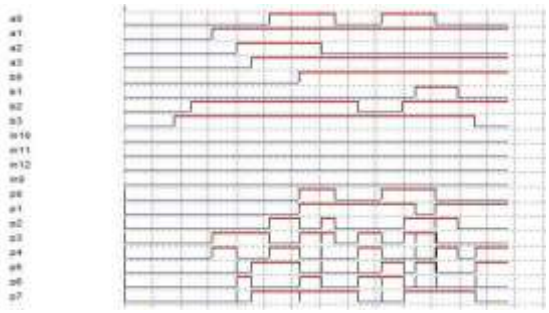

Fig. 10. GDI logic - Row by passing-pre layout timing diagram

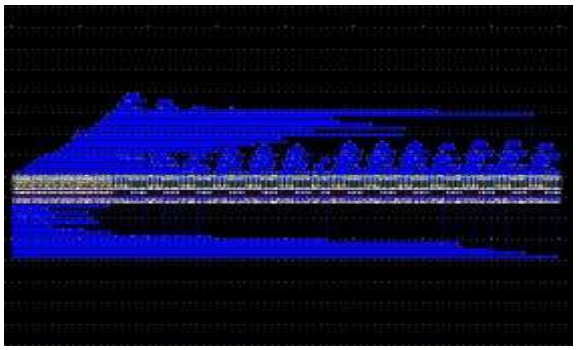

Fig. 11. GDI logic –Layout diagram– Row by passing

IV. RESULTS AND DISCUSSION

The performances of different multiplier circuits are simulated and the results were compared with C-CMOS, PTL and GDI cell based circuits as well as row and column bypassing designs. All the simulations were performed using DSCH 3.1 tool at 65nm technology with a supply voltage of 1V. The performance metrics like delay, Area, Power, PDP, EDP of CMOS, PTL and GDI Braun multipliers by various techniques are shown in Table II, III and IV respectively.

TABLE II. PERFORMANCE METRICS OF CMOS BRAUN MULTIPLIER

Multiplier	Delay (ns)	Power (µw)	PDP (fJ)	EDP (yJs)
BRAUN CMOS	0.488	11.28	5.5	2.684
ROW BYPASSING	0.549	43.79	24.04	13.197
COLUMN BYPASSING	0.504	16.820	8.47	4.268

TABLE III. PERFORMANCE METRICS OF PTL BRAUN MULTIPLIER

Multiplier	Delay (ns)	Power (µw)	PDP (fJ)	EDP (yJs)
BRAUN PTL	0.137	1.80	0.2466	0.033
ROW BYPASSING	0.162	2.26	0.3661	0.059
COLUMN BYPASSING	0.155	15.95	2.4722	0.383

TABLE IV. PERFORMANCE METRICS OF GDI BRAUN MULTIPLIER

Multiplier	Delay (ns)	Power (µw)	PDP (fJ)	EDP (yJs)
BRAUN GDI	0.140	1.459	0.204	0.028
ROW BYPASSING	0.141	2.471	0.348	0.049
COLUMN BYPASSING	0.129	16.138	2.08	0.268

From the Tables II, III and IV it is observed that the GDI cell based Braun multiplier scheme achieves more than 96% and 17% savings in energy consumption as well as98% and 15% savings in EDP when compared to CMOS and PTL based multipliers respectively. Similarly, the GDI cell based Braun multiplier with column bypassing scheme achieves more than 75% and 15% savings in energy consumption as well as 93% and 30% savings in EDP when compared to CMOS and PTL based multipliers with column bypassing respectively. Finally, the GDI cell based Braun multiplier with row bypassing scheme achieves more than 98% and 4% savings in energy consumption as well as99% and 16% savings in EDP when compared to CMOS and PTL based multipliers with row bypassing respectively. The area of CMOS, PTL and GDI Braun multipliers by various techniques are depicted in figure 12. It could be observed that the area of the GDI is for better than other multiplier techniques.

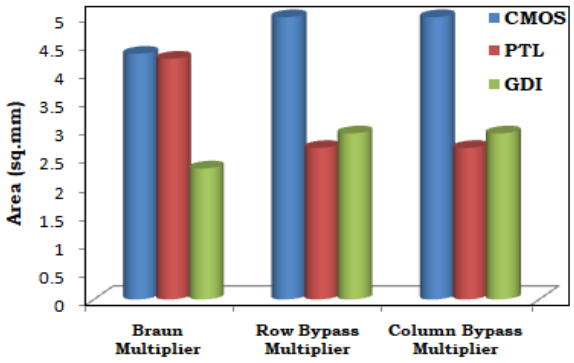

Fig. 12. Area of CMOS, PTL and GDI Braun multipliers

CONCLUSION

In this paper, a Braun multiplier with conventional and with row and column bypassing scheme is designed for computing applications in signal processing to maximize the energy efficiency. The circuit simulations have been carried out with a supply voltage of 1 volt at65nm technology. The performances of Braun multiplier for C – CMOS, PTL and GDI logic styles via conventional and by multiplying with the row and column by passing were evaluated and it is observed that GDI with column by passing reduces the delay in the circuit. From the simulations of various multipliers, it is observed that, the GDI cell based Braun multiplier is energy and EDP efficient over other counter parts. The GDI Braun multiplier is area efficient over CMOS and its other methods at the penalty of 9% more area in comparison with PTL based column and row bypassing techniques.

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