A New Planar InGaAs–InAlAs Avalanche Photodiode

B. F. Levine, R. N. Sacks, J. Ko, M. Jazwiecki, J. A. Valdmanis, D. Gunther, and J. H. Meier

***Abstract*—We discuss a new simple InGaAs–InAlAs avalanche photodiode (APD) with a planar buried multiplication region. Some of the advantages compared to standard APDs are as follows: 1) The thickness of the avalanche and the charge control regions are accurately controlled by molecular beam epitaxy growth in contrast to the standard diffusion process; 2) InAlAs is the multiplication material (avalanching faster electrons) instead of InP (avalanching slower holes); 3) InAlAs avalanche gain has a lower noise figure than that for InP; 4) a guard ring is not required; 5) fabrication is as simple as that for a p-i-n detector; 6) the APD has high wafer uniformity, and high reproducibility; 7) the InAlAs breakdown voltage is lower than InP, and its variation with temperature is three times lower than that for InP; 8) excellent aging and reliability including Telcordia GR-468 qualification for die and modules; 9) high gain-bandwidth product as high as 150 GHz; and 10) high long-range (LR-2) bit-error-rate 10^{-12} receiver sensitivity of -29.0 dBm at 10 Gb/s, -28.1 at 10.7Gb/s, and -27.1 dBm at 12.5 Gb/s.**

***Index Terms*—Avalanche photodiode (APD), molecular beam epitaxy (MBE), optical receivers, photodetectors.**

I. Introduction, Structure, and Fabrication

STANDARD planar InP avalanche photodiodes (APDs) [1], [2], use diffusion and/or implantation to create the high field p-n junction. This is a critical process requiring exceptional accuracy and control of the dose and diffusion depth since this step determines the length of the high field avalanche region, the magnitude of the high electric field in the avalanche region, and the value of the sheet charge needed to reduce the field in the absorption region. In addition, the high surface fields created by this p-n junction require guard rings [1]–[3] that increase the parasitic capacitance and further increase the difficulty of fabrication and lower the yield.

The backside illuminated high bandwidth APD structure[1] shown in Fig. 1 avoids these disadvantages. The structure, grown using molecular beam epitaxy (MBE), on an InP substrate is as follows: an n+Si-doped contact layer of InAlAs, a thin [4] not intentionally doped (n.i.d.) 1300-A InAlAs multiplication layer, an InAlAs charge control layer, a graded bandgap layer of InAlAs–InGaAs, a n.i.d. InGaAs absorption layer, another graded bandgap layer, a n.i.d. InAlAs passivation layer, an InGaAs p^+ stop etch layer, an InAlAs p^+ contact layer, and a thin p^+ InGaAs contact layer.

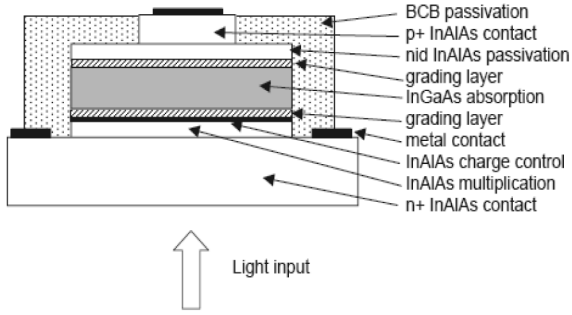

Fig. 1. Schematic illustration of the planar APD structure.

The noncritical, simple wet etched processing is highly reproducible, and is in fact, essentially the same as for a p-i-n detector since no guard ring is necessary. A 33-μm p^+ contact which defines the active area, is etched down to the stop etch, then the outer 50-μm diameter is etched, and the n- and p- metals deposited. This design in which all the layers are accurately grown using MBE, is much simpler to process than a recently reported structure [5], having some of the advantages of our APD, but which relies on Zn diffusion.

II. Principle of Operation

A guard ring is not needed since the electric field at the surface is small due to the high field multiplication region being buried below the charge control layer. Furthermore, due to this arrangement, the field distribution across the avalanche region is a maximum in the center and smoothly decreases at the edge, as indicated by the simulations in Fig. 2. In addition, the low bandgap InGaAs absorption layer is fully passivated, since it is buried below the high bandgap InAlAs passivation layer, and due to both the charge control and the p^+ contact geometry, the electric field is low in the center (increasing slightly under the edge of the p^+ contact), and nearly zero at the edges of the 50-μm n^+ contact. Thus, the electric field in the InGaAs is completely buried inside the semiconductor. Finally, it is worth noting that the initial high 2.2-pF capacitance at low bias (Fig. 3), due to the large junction area between the p^+ charge control layer (which extends to the n^+ contact edge) and the small separation from the n^+ contact, disappears above the 9-V punch through voltage due to the depletion of the absorption layer, to be replaced by the low 0.11-pF capacitance determined by the small p^+ contact diameter and its large separation from the n^+ contact. Thus, although the p^+ charge control layer extends across the entire APD, it does not affect the capacitance or bandwidth at the operating bias.

Manuscript received March 31, 2006; revised June 22, 2006.

B. F. Levine, R. N. Sacks, M. Jazwiecki, J. A. Valdmanis, D. Gunther, and J. H. Meier are with Picometrix LLC, Ann Arbor, MI 48104 USA (e-mail: blevine@picometrix.com).

J. Ko was with Picometrix LLC, Ann Arbor, MI 48104 USA. He is now with Fish and Richardson P.C., San Diego, CA 92130 USA.

Digital Object Identifier 10.1109/LPT.2006.881684

[1]This work is based on our patent applications: Provisional applications 60/353,530 and 60/353,765 filed February 1, 2002; U.S. patent application "Planar avalanche photodiode" 2005/0156192 A1 and PCT/US03/03323 filed February 3, 2003, and U.S. patent application "Planar avalanche photodiode" 2004/0251483 A1 and PCT/US04/13584 filed April 30, 2004. All four of these later patents claim the benefit of the February 1, 2002 filing date. (These applications disclose both the etched and the diffused contact designs.)

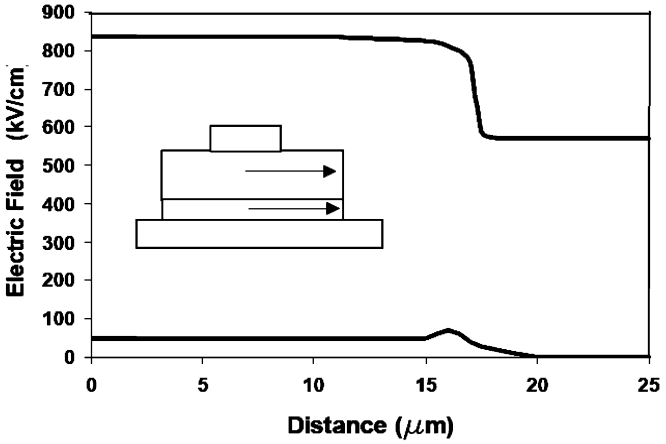

Fig. 2. Electric field versus radial distance from the center in the absorption layer (bottom trace) and the avalanche layer (top trace).

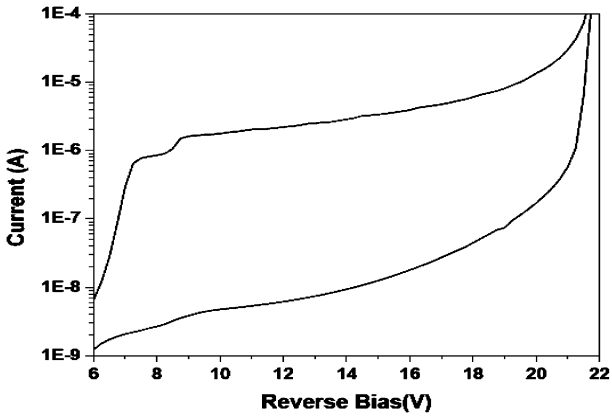

Fig. 4. Photocurrent versus bias measured at 1550 nm with 1 μW. Note the sharp increase in photocurrent at the 9-V punch through voltage, and the initial increase at 7.5 V as the charge control layer is depleted.

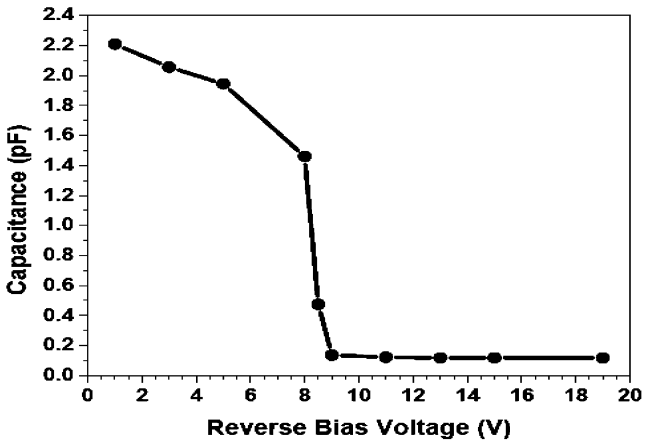

Fig. 3. Capacitance versus bias showing the dramatic drop at the 9-V punch through voltage.

III. Measurements

The 1-μW photocurrent and dark current curves measured at 1550 nm are shown in Fig. 4. The responsivity at a gain of unity is 0.8 A/W at 1550 nm and 0.85 A/W at 1310 nm (determined by absolute source calibration), and the gain at the 9-V punch through voltage is $M = 2$. Note that due to the thin accurately grown MBE avalanche layer, $M = 10$ only requires 19 V, with a dark current of typically 100 nA. A gain of $M = 20$ only requires 20.3 V, $M = 40$ only 21.1 V, and gains of over 100 have been measured. In addition, due to the excellent MBE thickness and doping uniformity, over 95% of the avalanche breakdown voltages are within ± 0.1 V across a 3-in wafer (all APDs from the three aging wafers discussed below have $V_b = 21.5 \pm 0.4$ V). Furthermore, 95% of the dark currents across the wafer are within $\pm 15\%$ of the mean. The temperature dependence of the breakdown voltage (defined as the voltage at 100 μA of dark current) was measured to be only 0.015 V/°C, which is over three times better than that for InP-based APDs.

The die gain bandwidth product was measured to be 130 GHz at -20-dBm input power and 150 GHz at -10 dBm, and highly uniform with less than a 5% variation across the wafer. "Small form factor" modules were built and tested for bandwidth and sensitivity using production APD die and a commercially available GaAs pHEMT transimpedance amplifier. World record high receiver sensitivities at 1550 nm, with an optimum gain of $M = 15$, were achieved for a bit-error-rate (BER) 10^{-12}, an extinction ratio of 12, and a standard $2^{31} - 1$ pseudorandom bit pattern: -29.0 dBm at 10 Gb/s, -28.1 dBm at 10.7 Gb/s and -27.1 dBm at 12.5 Gb/s. Thus, long-range LR-2 sensitivities are achieved even at the high bit rate of 12.5 Gb/s that is required for some error correction codes. Due to the low temperature dependence of the InAlAs breakdown voltage, the BER was essentially unchanged from 25 °C to 75 °C only requiring a shift in the optimum bias of 0.8 V.

IV. Aging and Reliability

A 5000-h APD aging and reliability study [6] has been completed in compliance with Telcordia GR-468. A total of 176 die from three different wafers were randomly selected and aged at a dark current of 100 μA at five different temperatures ($T = 150$ °C, 175 °C, 190 °C, 210 °C, and 230 °C). Devices were measured weekly and were considered failed if the room-temperature dark current exceeded 500 nA at the operating voltage of 19 V. Using a standard Weibull statistical failure mode analysis, which takes into account the exact number of failures, the precise times of these failures and the temperatures at which they occurred, one can determine the three important aging parameters, namely the activation energy E_a, the Weibull shape parameter β, and the lifetime $L(T) \sim \exp(E_a/T)$ as a function of temperature. The value of the shape parameter β determines whether the failures are due to infant mortality $\beta < 1$, random failures $\beta = 1$, or wear out failures $\beta > 1$, while the activation energy E_a determines how the observed failures at the aging temperatures extrapolate back to the operating temperature.

A detailed statistical analysis has determined that the failures were due to wear out (the Weibull statistical failure shape parameter $\beta = 1.48$), with a wear out failure activation energy $E_a = 1.46$ eV. Note that the activation energy is, as expected, closely equal to the InAlAs bandgap $E_g = 1.47$ eV. This is due to the high field in the thin InAlAs multiplication region being close to the field required for tunneling through the InAlAs band gap. That is, the failure mechanism is a result of aging related

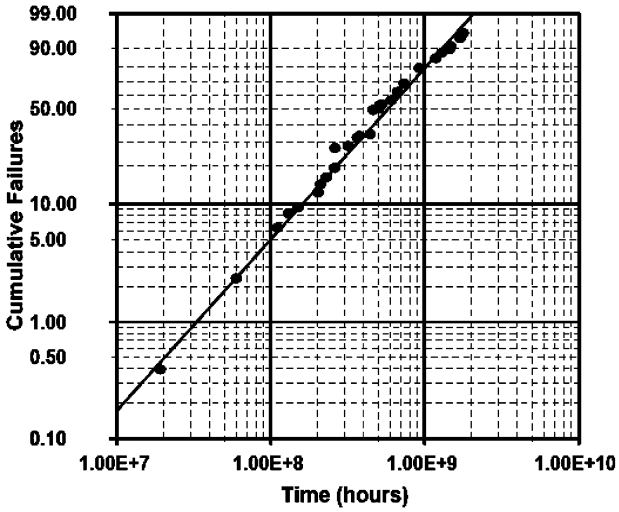

Fig. 5. Plot of cumulative failures (%) versus time for 176 APDs from three different wafers aged at five different temperatures, referred to an operating temperature of 70 °C. The lifetime determined from the 63% failure level is 7.4×10^8 h at 70 °C.

charge accumulation in the passivation layer that changes the field distribution thereby allowing tunneling to dominate the current flow. Using this data, the lifetimes have been determined to be extremely long: 7.4×10^8 h (85 000 years) at 70 °C, 42 000 years at 75 °C, 21 000 years at 80 °C, and 11 000 years at 85 °C. These are the highest reliability and longest lifetime APDs ever developed. Furthermore, the fact that all the data fall closely on a straight line (see Fig. 5) proves the consistency of the statistical method and the accuracy of the determination of the failure parameters.

A small portion of the data is shown in Fig. 6 for 50 die from two different wafers aged at 150 °C for 5000 h. (The dark current from the other wafer falls between these extremes.) Note that the increase in dark current is very small ∼100 nA at 19 V, and that even the worst APDs only have a dark current <400 nA after 5000 h of aging. Furthermore, even after aging for 5000 h at 150 C, the shift in breakdown voltage was <0.1 V. The shift in breakdown voltage for all nonfailed die, during the 5000 h of aging is <0.3 V for all temperatures, and thus negligible. These exceptionally long lifetimes far exceed the Telcordia requirements, with negligible wear our failures of much less than one FIT (failures in 109 device hours) over 25 years at all temperatures even up to 85 °C. These extremely long lifetimes and low failure rates clearly demonstrate the robustness of the planar APD design and the high quality of the processing.

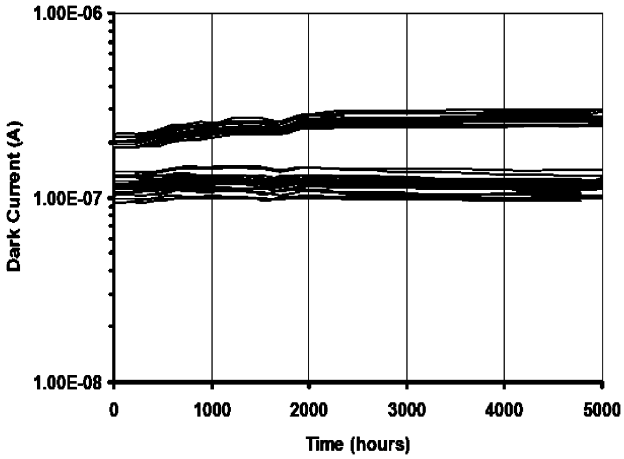

Fig. 6. Room-temperature dark current (at 19 V) versus aging time at 150 °C and 100-μA bias for 50 die from two different wafers.

V. Conclusion

We have developed a new, planar, APD design based on MBE-grown InAlAs material that has dramatically improved performance, and process uniformity. These new structures enable higher sensitivity, lower operating voltages, less temperature dependence, and higher gain-bandwidth than InP APDs. The result is a Telcordia qualified receiver that can reliably achieve LR-2 long-range performance even at 12.5 Gb/s, with high consistency from module to module.

References

[1] M. A. Itzler, C. S. Wang, S. McCoy, N. Codd, and N. Komba, "Planar bulk InP avalanche photodiode design for 2.5 and 10 Gb/s applications," in *Proc. 24th ECOC*, Madrid, Spain, Sep. 20–24, 1998, vol. 1, pp. 59–60, Paper MoB03.

[2] L. E. Tarof, J. Yu, R. Bruce, D. G. Knight, T. Baird, and B. Oosterbrink, "High frequency performance of separate absorption grading charge and multiplication InP/InGaAs avalanche photodiodes," *IEEE Photon. Technol. Lett.*, vol. 5, no. 6, pp. 672–674, Jun. 1993.

[3] I. Watanabe, T. Nakata, M. Tsuji, K. Makita, and K. Taguchi, "High reliability and low dark current 10 Gb/s planar superlattice avalanche photodiodes," *IEEE Photon. Technol. Lett.*, vol. 9, no. 12, pp. 1619–1621, Dec. 1997.

[4] J. C. Campbell, S. Demiguel, F. Ma, A. Beck, X. Guo, S. Wang, X. Zheng, X. Li, J. D. Beck, M. A. Kinch, A. Huntington, L. A. Coldren, J. Decobert, and N. Tscherptner, "Recent advances in avalanche photodiodes," *IEEE J. Sel. Topics Quantum Electron.*, vol. 10, no. 4, pp. 777–787, Jul./Aug. 2004.

[5] E. Yagyu, E. Ishimura, M. Nakaji, T. Aoyagi, and Y. Tokuda, "Simple planar structure for high performance AlInAs avalanche photodiodes," *IEEE Photon. Technol. Lett.*, vol. 18, no. 1, pp. 76–78, Jan. 1, 2006.

[6] R. R. Sutherland, C. P. Skrimshire, and M. J. Robertson, "A reliability methodology applied to very high reliability planar InGaAs/InP PIN photodetectors," *Br. Telecom. Technol. J.*, vol. 7, pp. 69–77, Jan. 1989.