Vertical InGaAs Biristor for Sub-1 V Operation

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***Abstract*— A vertical bi-stable resistor (biristor) composed of $In_{0.53}Ga_{0.47}As$ was demonstrated for sub-1 V operation. An inherent small bandgap and a scaled base length of 150 nm led to the remarkable reduction in latch-up voltage compared to Si(Ge)-based conventional biristors. The epitaxially grown n-p-n structure allowed an abrupt p-n junction, which was also very important to reduce the latch-up voltage. Furthermore, the physical mechanism of carrier transport in the InGaAs biristor was explored with TCAD simulations.**

***Index Terms*— 3-D integration, abrupt junction artificial neural network, epitaxial growth, impact ionization, InGaAs, vertical biristor.**

I. Introduction

ALTHOUGH the capacitor-less one-transistor dynamic random-access memory (1T-DRAM) has shown great potential of being able to replace conventional DRAM with a higher packing density beyond $4F^2$, its three-terminal structure suffers from inherent gate reliability issues, such as hot carrier injection. [1], [2] To mitigate these issues, the bistable-resistor abbreviated as "biristor", has been developed. A biristor is an open-based two-channel bipolar junction transistor with a collector-base-emitter structure with a doping profile of either n^+-p-n^+ or p^+-n-p^+. Biristors have shown promising characteristics with enhanced endurance and reliability for post-DRAM technology applications thanks to their gate-less operation. [3]–[6]

Compared to 1T-DRAM, another attractive aspect of biristors is their potential for further cell size reduction thanks to their gate-less structure. In principle, when a biristor is formed vertically, the packing density can be reduced to be as small as $1F^2$ [7]. Moreover, its fabrication can be even simpler in comparison to conventional 3-terminal 1T-DRAM.

Previous studies have also suggested the usability of biristors as neuronic devices in neuromorphic systems using the leaky integrate-and-fire function [8]. Therefore, a vertically stacked neuron structure is a very promising candidate for 3-D integrated artificial neural networks [9] with the advantages of improved gate reliability and high packing density with simple fabrication.

Despite these advantages, previously demonstrated biristors have shown quite high operating voltages. To achieve impact ionization in the open-base region, a biristor requires a minimum collector voltage (V_C), known as the latch-up voltage (V_{LU}). Previously reported numerical simulation studies have suggested strategies to reduce V_{LU}, such as bandgap engineering by using Si_xGe_{1-x}, [10] or optimization of the biristor structure [11]. However, the demonstrated biristors have shown a limited reduction of V_{LU} and still have high operating voltages [4]–[7]. The main reasons for high V_{LU} in experimental results are the fabrication difficulties in forming an abrupt p-n junction and the inherent limits of the physical properties of Si-based material systems. Ion implantation, which is most commonly used to form a p-n junction, limits fabrication freedom due to the diffusion of dopants during activation. This not only limits the abruptness of the p-n junction for the emitter-base-collector profile but also makes it difficult to scale down the base length (L_B). Epitaxially grown III-V compounds have shown promising 1T-DRAM characteristics thanks to their lower band-gap and the abrupt p-n junction with a narrowed L_B with epitaxially grown S/D [12]. Moreover, a gate-free nature can mitigate reliability issues. A vertical structure can increase packing density and allow hybrid 3-D integration of other memory or neuronic devices [9].

In this study, a vertical InGaAs biristor was experimentally demonstrated with V_{LU} of sub-1 V, which is the lowest V_{LU} ever reported. This feature is attributed to its inherent small bandgap offset and abrupt p-n junction with a reduced L_B by epitaxial growth. Numerical simulations supported the measured data with physical mechanism.

II. Device Fabrication

The vertical III-V biristor was experimentally fabricated on epitaxially grown an $InGa_{0.53}As_{0.47}$ (InGaAs) wafer. A schematic illustration of the InGaAs vertical biristor structure is shown in Fig. 1. An InGaAs layer was epitaxially grown on bulk InP, where the collector and emitter were formed with *in-situ* n^+ doping by tellurium (Te) with a doping concentration of 10^{19} cm^{-3}, a layer thickness of 200 nm. The L_B was controlled during epitaxial growth. Afterwards, the patterning

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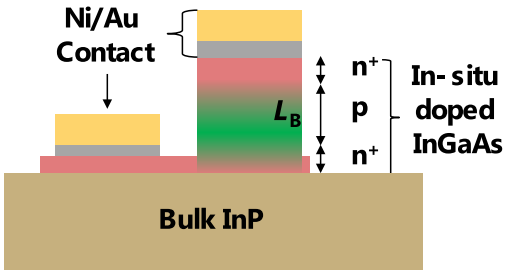

Fig. 1. Schematic illustration of vertical InGaAs biristor on bulk InP.

processes were carried out. First, 70-nm-thick Au (top) and 30-nm-thick Ni (bottom) were sequentially deposited as a collector contact with a size of $80 \times 80\ \mu m^2$. Next, the vertical biristor was etched by an H_3PO_4-based solution. In that step, the patterned Ni/Au served as a hard mask. Here, one concern would be the metal-assisted chemical (MAC) etching, but there was no such reaction because there was no direct noble metal contact for InGaAs. Then, another set of Ni/Au layers were deposited as an emitter contact. Note that the highest process temperature was lower than 200 °C, which can be a very important figure-of-merit for subsequent 3D integration.

As shown in Fig. 2(a), transmission electron microscopy (TEM) was used to investigate the epitaxial structure of the vertical biristor. The cross-sectional TEM image shows a clear InGaAs layer on the InP substrate without any visible defects. Good crystal quality was confirmed by the electron diffraction image in the inset of Fig. 2(a). Secondary ion mass spectroscopy (SIMS) was also conducted to analyze its doping profile, as shown in Fig. 2(b). The SIMS profile shows that an abrupt p-n junction had formed with Te with an L_B of 400 nm.

III. Results and Discussion

The measured current-voltage (I-V) characteristic of the fabricated InGaAs vertical biristor with a nominal L_B of 400 nm is shown in Fig. 3(a). When the collector voltage (V_C) approached the latch-up voltage (V_{LU}), latch-up to abruptly increase the collector current (I_C) was enabled by impact ionization. After the latch-up, the biristor was turned on. It should be noted that the InGaAs biristor showed a V_{LU} of 1.5 V. This is remarkably lower than the V_{LU} of approximately 4 V of a conventional Si biristor. By reversed sweeping, it showed a latch-down voltage (V_{LD}) of 1.25 V. Thus, a latch window ($V_{LU} - V_{LD}$) of 0.25 V was achieved by the InGaAs biristor.

To investigate the physical mechanism, numerical simulations were performed with the aid of a Silvaco Atlas tool. The set of physical models used in the simulation is based on previous work [10]. It includes an energy balance model for carrier transport, low and high electric field mobility models, a carrier temperature-dependent mobility model, a Shockley-Read-Hall (SRH) recombination model, a trap-assisted tunneling (TAT) model, a Toyabe impact ionization model, and band-to-band tunneling (BTBT) models (local and nonlocal). Trap energy and saturation velocity for the SRH model, effective tunneling mass, and relaxation lifetimes, were used as fitting parameters. The I-V characteristics were simulated by using the curve tracing algorithm.

The measured and simulated I-V curves were superimposed, as shown in Fig. 3(b). They showed good matching. The band

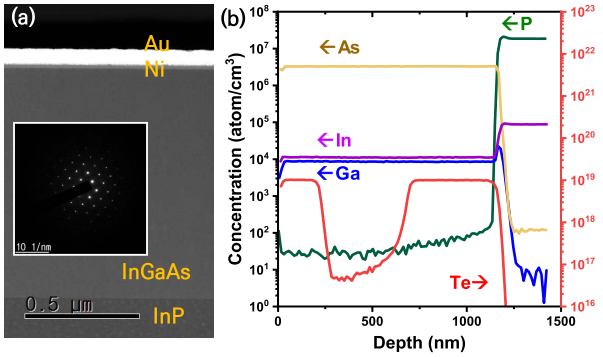

Fig. 2. (a) TEM image of epitaxially grown InGaAs on bulk InP. (b) SIMS profile of Te doping concentration in the InGaAs vertical biristor for an L_B of 400 nm.

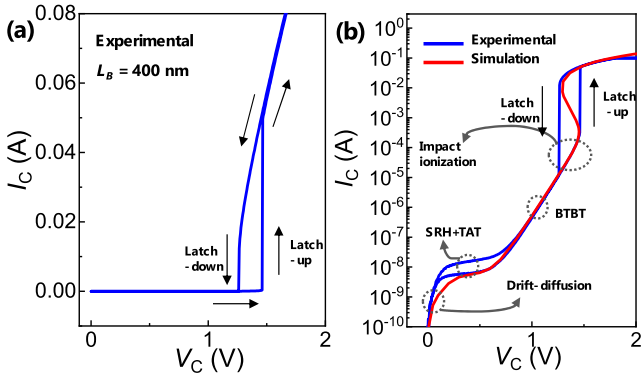

Fig. 3. (a) Measured I-V characteristics (linear scale) of the InGaAs biristor with an L_B of 400 nm. (b) Superimposed measured and simulated I-V characteristics (log scale).

diagram of the investigated biristor is shown in Fig. 4. When V_C is lower than V_{LU}, a low level of leakage current (I_C) is flowing. It is governed by three mechanisms. At a very low V_C, the I_C is dominated by drift and diffusion transport. At an intermediate V_C, it is led by the SRH and TAT current. At a high V_C (dashed lines in Fig. 4), the I_C is attributed to the BTBT, which increases the electron flow through the base-collector junction. With the further increase of the applied voltage (above V_{LU}), due to the impact ionization mechanism, the carrier concentration increases, and the base barrier lowers (dotted lines in Fig. 4), drastically increasing the current. This simulation-based analysis can contribute to finding a way to further lower the I_C and to improve the off-state characteristics of the InGaAs biristor. In present work, there was no size effect because of large mesa dimension of $80 \times 80\ \mu m^2$. However, future scaled device will be affected by the surface recombination due to the increased surface/area ratio, indicating surface passivation on the sidewall will be very important to guarantee the reasonable off-state characteristics [13].

As reported in previous studies [10], [11], the latch characteristics are significantly affected by the L_B. Fig. 5(a) shows V_{LU} and V_{LD} for various L_B values. They decreased as the L_B was narrowed, and the latch window became too small when the L_B was narrower than 120 nm with increased off-state current (I_{off}).

Based on the simulation results, InGaAs biristors with two different L_B values of 50 nm and 150 nm were fabricated. Fig. 5(b) compares the measured I-V curves of these InGaAs vertical biristors. A V_{LU} of 0.98 V, which is the lowest operating voltage ever reported, was achieved. At the narrow

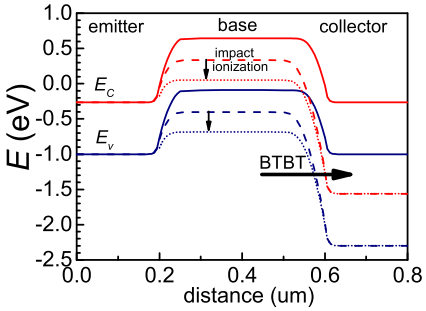

Fig. 4. Simulated band diagram of the InGaAs biristor.

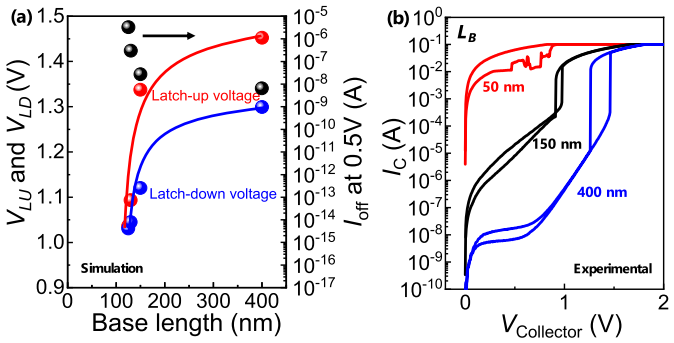

Fig. 5. Measured and simulated characteristics of the vertical InGaAs biristor for L_B of 50 nm, 150 nm, and 400 nm, respectively.

TABLE I
COMPARISON OF LATCH-UP VOLTAGE

Structure, Material	Methodology	V_{LU}	Ref.
Planar, SiGe	Simulation	1.7 V	[10]
Planar, Si	Simulation	2.14 V	[17]
Planar, Si	Simulation	2.0 V	[15]
Planar, Si	Simulation	1.62 V	[16]
Vertical, Si	Simulation	1.68 V	[11]
Vertical, InGaAs	**Simulation**	**1.09 V**	**This work**
Planar, Si	Experiment	5.45	[5]
Vertical, Si	Experiment	5.97	[4]
Planar, Si	Experiment	4.94	[7]
Vertical, InGaAs	**Experiment**	**0.98 V**	**This work**

L_B of 50 nm, the leakage current increased, and the latch window disappeared, as seen in the simulations.

Finally, the reported V_{LU} values for various structured biristors composed of Si, SiGe, and InGaAs (this work) are compared in Table I because V_{LU} is one of the most important figure-of-merit of this type of devices. The InGaAs biristor significantly reduced the V_{LU} in comparison to Si-based biristors [11], [12], [14], [15] and a SiGe biristor [10] regardless of a planar or vertical structure. The InGaAs biristor can be used for future gate-less and capacitor-less DRAM or neuronal devices with the benefit of sub-1 V operation.

IV. Conclusion

A vertical InGaAs biristor showed significantly enhanced latch characteristics to operate at a record-low V_{LU}, enabled by its relatively low bandgap and a narrow base length with an abrupt p-n junction formed by epitaxial growth. Simulation showed the physical mechanism of the carrier transport in the InGaAs biristor corresponding to the collector voltage and predicted the V_{LU} scaling with decreasing base length. The experimentally demonstrated InGaAs biristor operated at a V_{LU} of 0.98 V at the base length of 150 nm, which is an 80% reduction in operating voltage compared to conventional Si(Ge)-based biristors. This work demonstrated the possibility of a vertical biristor operating at low power with a high packing density. Thanks to epitaxial growth, the vertical biristor can not only be a breakthrough in DRAM technology but also can be used in 3D integrated applications, such as stacked neuronal devices in artificial neural networks.

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References

[1] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A capacitor-less 1T-DRAM cell," *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 85–87, Feb. 2002.

[2] M. Aoulaiche, N. Collaert, R. Degraeve, Z. Lu, B. De Wachter, G. Groeseneken, M. Jurczak, and L. Altimime, "BJT-mode endurance on a 1T-RAM bulk FinFET device," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1380–1382, Dec. 2010.

[3] M. Reisch, "On bistable behavior and open-base breakdown of bipolar transistors in the avalanche regime-modeling and applications," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1398–1409, Jun. 1992.

[4] D.-I. Moon, S.-J. Choi, J.-Y. Kim, S.-W. Ko, M.-S. Kim, J.-S. Oh, G.-S. Lee, M.-H. Kang, Y.-S. Kim, J.-W. Kim, and Y.-K. Choi, "Highly endurable floating body cell memory: Vertical biristor," in *IEDM Tech. Dig.*, Dec. 2012, pp. 749–752, doi: 10.1109/IEDM.2012.6479147.

[5] J.-W. Han and Y.-K. Choi, "Biristor—Bistable resistor based on a silicon nanowire," *IEEE Electron Device Lett.*, vol. 31, no. 8, pp. 797–799, Aug. 2010.

[6] D.-I. Moon, S.-J. Choi, S. Kim, J.-S. Oh, Y.-S. Kim, and Y.-K. Choi, "Vertically integrated unidirectional biristor," *IEEE Electron. Device Lett.*, vol. 32, no. 11, pp. 1483–1485, Nov. 2011.

[7] J.-W. Han and Y.-K. Choi, "Bistable resistor (biristor)-gateless silicon nanowire memory," in *VLSI Symp. Tech. Dig.*, Jun. 2010, pp. 171–172, doi: 10.1109/VLSIT.2010.5556215.

[8] J.-W. Han and M. Meyyappan, "Leaky integrate-and-fire biristor neuron," *IEEE Electron Device Lett.*, vol. 39, no. 9, pp. 1457–1460, Sep. 2018.

[9] S. K. Kim, Y. Jeong, P. Bidenko, H.-R. Lim, Y.-R. Jeon, H. Kim, Y. J. Lee, D.-M. Geum, J. Han, C. Choi, H.-J. Kim, and S. Kim, "3D stackable synaptic transistor for 3D integrated artificial neural networks," *ACS Appl. Mater. Interface*, vol. 12, no. 6, pp. 7372–7380, Jan. 2020.

[10] J.-B. Moon, D.-I. Moon, and Y.-K. Choi, "A bandgap-engineered silicon-germanium biristor for low-voltage operation," *IEEE Trans. Electron Devices*, vol. 61, no. 1, pp. 2–7, Jan. 2014.

[11] J. W. Son, J. Hur, W.-K. Kim, G.-B. Lee, and Y.-K. Choi, "A strategy for optimizing low operating voltage in a silicon biristor," *IEEE Trans. Nanotechnol.*, vol. 19, pp. 5–10, 2020.

[12] C. Navarro, S. Karg, C. Marquez, S. Navarro, C. Convertino, C. Zota, L. Czornomaz, and F. Gamiz, "Capacitor-less dynamic random access memory based on a III–V transistor with a gate length of 14 nm," *Nature Electron.*, vol. 2, no. 9, pp. 412–419, Sep. 2019.

[13] S. K. Kim, D.-M. Geum, H.-R. Lim, H. Kim, J.-H. Han, D. K. Hwang, J. D. Song, H.-J. Kim, and S. Kim, "Improved characteristics of MOS interface between $In_{0.53}Ga_{0.47}As$ and insulator by H_2 annealing with Pt gate electrode," *Appl. Phys. Lett.*, vol. 115, no. 14, Sep. 2019, Art. no. 143502.

[14] J. F. Klem, J. K. Kim, M. J. Cich, G. A. Keeler, S. D. Hawkins, and T. R. Fortune, "Mesa-isolated InGaAs photodetectors with low dark current," *Appl. Phys. Lett.*, vol. 95, no. 3, Jul. 2009, Art. no. 031112.

[15] M. J. Kumar, M. Maheedhar, and P. P. Varma, "Junctionless biristor: A bistable resistor without chemically doped P-N junctions," *IEEE J. Electron Devices Soc.*, vol. 3, no. 4, pp. 311–315, Jul. 2015.

[16] M. J. Kumar, M. Maheedhar, and P. P. Varma, "Schottky biristor: A metalsemiconductor-metal bistable resistor," *IEEE Trans. Electron. Devices*, vol. 62, no. 7, pp. 2360–2363, Jul. 2015.

[17] M. J. Kumar, M. Maheedhar, and P. P. Varma, "A silicon biristor with reduced operating voltage: Proposal and analysis," *IEEE J. Electron Devices Soc.*, vol. 3, no. 2, pp. 67–72, Mar. 2015.