數位系統設計 (Digital System Design)
Homework 2

A. BCD-to-Binary Converter (Synchronous Sequential Circuit)

Design a BCD-to-binary converter running **reversed double dabble algorithm**. Initially a 3-digit BCD number is placed in the 12-bit register, *A*. When an *St* signal is received, conversion to binary takes place and the resulting binary number is stored in the 10-bit register, *B*. The maximum value of *B* will be 999 (in binary). At each step of the conversion, the entire BCD number (along with the binary number) is shifted one place to the right. If the result in a given decade is greater than or equal to 1000, the correction circuit subtracts 0011 from that decade. (If the result is less than 1000, the correction circuit leaves the contents of the decade unchanged.) A shift counter is provided to count the number of shifts. When conversion is complete, *Done* signal is raised for one clock cycle and outputs the answer *binary*.

(a) Illustrate the algorithm starting with the BCD number 857. Showing A and B register in each step.

(b) Draw the **block diagram** of the BCD-to-binary converter module. Use the following control signals. ***St***: start conversion; ***Shr***: shift right; ***Cor*** subtract correction if necessary; ***C9***: counter is count to 9, starting from 0. Define other control signals or status bits, if necessary.

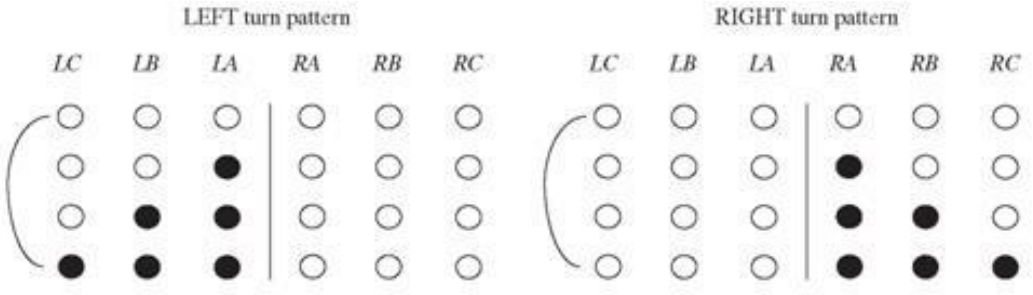
(c) Draw the **state graph** for the converter.

(d) Write the **Verilog circuit module**. Be sure to add adequate comments in your Verilog code. The circuit module should be named as *HW2_BDC_to_Binary_Converter*, and its file should be named as *HW2_BCD_to_Binary_Converter.v*. The order of the port list of this Verilog module must be *CLK*, *St*, *BCD*, *Done, Binary*.

(e) Write a **test bench** to test the circuit module designed in (d). The testbench module should be named *t_HW2_BDC_to_Binary_Converter*, and its file should be named as *t_HW2_BDC_to_Binary_Converter.v* . Simulate your Verilog design using the following three BCD number test cases at least: 857, 998, 021.

B. Tail-Light Controller (Synchronous Sequential Circuit)

An older model Thunderbird car has three left (LA, LB, LC) and three right (RA, RB, RC) tail lights, which flash in unique patterns to indicate left and right turns.



Design a Moore sequential circuit to control these lights. The circuit has three inputs: LEFT, RIGHT, and HAZ. LEFT and RIGHT come from the driver's turn signal switch and cannot be 1 at the same time. As indicated in the diagram, when LEFT = 1 the lights flash in a pattern LA on, LA and LB on, LA, LB, and LC on, all off; then the sequence repeats. When RIGHT = 1, a similar sequence appears on lights RA, RB, and RC, as indicated on the right side of the diagram. If a switch from LEFT to RIGHT (or vice versa) occurs in the middle of a flashing sequence, the circuit should immediately go to the IDLE (lights off) state and then start the new sequence. HAZ comes from the hazard switch, and when HAZ = 1, all six lights flash on and off in unison. HAZ takes precedence if LEFT or RIGHT is also on.

(a) Draw the **block diagram** of this Moore sequential circuit.

(b) Draw the **state graph** of the Moore sequential circuit.

(c) Write a **behavioral Verilog description** for this sequential circuit according to the state diagram or the state table of the circuit. The circuit module should be named as *HW2_Light_Controller*, and its file should be named as *HW2_Light_Controller.v*. The order of the port list this Verilog module must be *LEFT, RIGHT, HAZ, CLK, LA, LB, LC, RA, RB, RC*.

(d) Write a **test bench** to test the circuit modules designed in (c). The test bench module should be named as *t_HW2_Light_Controller*, and its file should be named as *t_HW2_Light_Controller.v* Start the test from the initial state. Each input should change 1/4 clock period after the rising edge of the clock. After saving the modules, compile and simulate the modules and observe the waveform of the simulation result.

◆ 作業及 HDL 模組繳交 (Hand in)

- **作業報告繳交： pdf 檔，命名為 HW2_學號_姓名。包含下列內容：**
  Submit you homework report in a pdf file, named HW2_StudentID_Name, including the following contents:

  A. BCD-to-Binary Converter (50%)

  i. 以採 BCD 編碼之十進位數值 857 為例，演示此演算法如何產生對應之二進位數字；在每個步驟中顯示出暫存器 A 與暫存器 B 之內容。此外，並說明為何此演算法是正確的。
  Illustrate the algorithm starting with the BCD number 857. Showing A and B register in each step. Moreover, describe the reason why this algorithm is correct.

  ii. 說明你的設計，繪製 A(b)的方塊圖與 A(c)的狀態圖。
  Describe your design. Draw the **block diagram** in A(b) and the **state graph** in A(c).

  iii. 附上 A(d)模擬結果之波型圖，解釋波形圖是否正確，並列出每筆測資需要幾個 cycles 完成。
  Show the waveform of the simulation results for the circuit module in A(d), explain whether the results are correct or not, and indicate how many cycles are required to complete the computation of each test case.

  B. Tail-Light Controller (40%)

  i. 說明你的設計，繪製 B(a)的方塊圖與 B(b)的狀態圖。
  Describe your design. Draw the **block diagram** in B(a) and the **state graph** in B(b).

  ii. 說明你的測資，附上 B(d)模擬結果之波型圖，並解釋波形圖是否正確。
  Describe your test data. Show the waveform of the simulation results for the circuit module in B(d), and explain whether the results are correct or not.

  C. 心得感想、結論、及討論 (10%)
  Conclusions and Discussions

- **Verilog modules 檔案繳交：Hand in the following Verilog modules (4 .v files)**
  HW2_BDC_to_Binary_Converter.v
  t_HW2_BDC_to_Binary_Converter.v
  HW2_Light_Controller.v
  t_HW2_Light_Controller.v

◆ 注意事項與繳交截止日期 (Notes and Deadline)

- 可用任意開發環境，但請在報告中說明你使用哪個模擬器。
  Use any simulator you want and explain which one you choose in the report.
- 請務必依照各題中之規定命名模組及檔案，並遵循各電路模組之輸出入順序。
  Be sure to name the modules and files and follow the order of the port list as described above.
- 助教會使用不同的測試模組來驗證同學的電路模組正確性。
  After you hand in your code, TA will use similar Testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.
- 本作業為一人一組。請將 Verilog 電路模組(.v)與作業報告 pdf 檔全部壓縮成一個 zip，命名為「HW2_學號_姓名」(如 ： 「HW2_110550100_王大明」)，並上傳至 e3 平台。作業報告如為手寫，請務必用深色筆書寫，並確認掃描後檔案清晰易讀。
  This homework is one student per group. Please compress the Verilog circuit modules and the pdf file described above all into one **zip** file, name the compressed file as "HW2_StudentID_Name" (for example, "HW2_110550100_KentChang"), and upload the compressed file onto e-Campus platform. If your homework report is handwritten, please use the dark colored pen and make sure that it is clearly and legibly after scan.
- 繳交截止日期為 2022/11/16 (三) 23:55。每遲交一天，本作業扣總分 10%，至多可遲交四天。
  The deadline is **2022/11/16 (Wed.) 23:55.** The penalty of late hand-in is 10% deduction of the total point per day, and four days late at most.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point