數位系統設計

(Digital System Design)
Homework 3

A. Realize the SM chart shown in Figure 1 using a microprogramming structure.

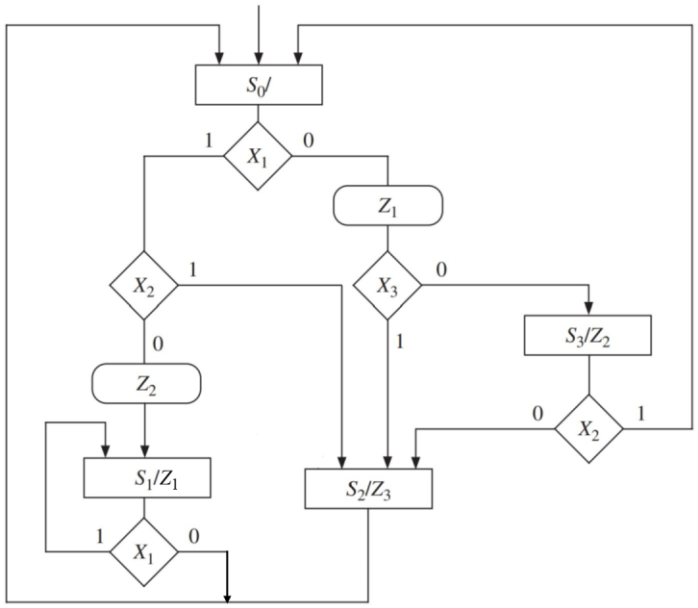
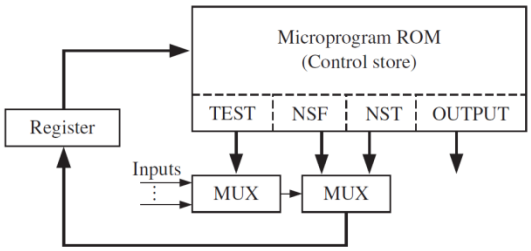


Figure 1: An SM chart.

(a) Realize the SM chart using the **two-address** microprogramming structure. A typical block diagram for microprogramming with a single qualifier per state and two next-state addresses (SQTA) is shown below and the multiplexer inputs are selected as shown in the table beside the block diagram:



TEST	
00	1
01	X_1
10	X_2
11	X_3

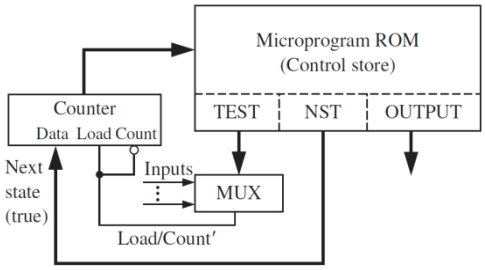
i. Convert the SM chart to the proper form by adding a minimum number of states to the given chart.

ii. Define the format of the two-address control word clearly and write the microprogram, i.e., the ROM table, required to implement the circuit.

iii. What is the size of the ROM (number of words × number of bits per word) required for the two-address microprogramming?

iv. What is the size of the ROM if the **traditional ROM method** (**LUT method**) is used to implement the original SM chart?

(b) Realize the SM chart using the **one-address** microprogramming structure. A typical block diagram for microprogramming with a single qualifier per state and one next-state addresses (SQSA) is shown below:



TEST	
00	1
01	X_1
10	X_2
11	X_3

i. Convert the SM chart to the proper form by adding a minimum number of extra states to the chart derived in (a). Make a suitable state assignment, and modify the definition of the TEST field, if necessary.

ii. Define the format of the one-address control word clearly and write the microprogram, i.e., the ROM table, required to implement the circuit.

iii. What is the size of the ROM (number of words × number of bits per word) required for the one-address microprogramming?

(c) Please write the **Verilog circuit module** for the **two-address** microprogrammed controller derived in (a). The circuit module should be named as *HW3_SQTA_microprogram*, and its file should be named as *HW3_SQTA_microprogram.v* .
The order of the port list of this Verilog module must be *Clk*, Rst, *X*1, *X*2, *X*3, *Z*1, *Z*2, *Z*3.

(d) Please write a **test bench** to test the circuit module designed in (c). The testbench module should be named as *t_HW3_SQTA_microprogram*, and its file should be named as *t_HW3_SQTA_microprogram.v* . **Start the test from the initial state S0**. *Xi* should change 1/4 clock period after the rising edge of the clock. After saving the modules, compile and simulate the modules and observe the waveform of the simulation result.
The test bench should include the following input sequence at least:

Clk	X1	X2	X3
0	1	1	0
1	1	0	1
2	0	1	0
3	0	0	1
4	1	1	0
5	0	1	0
6	1	0	0
7	0	0	1
8	0	0	0
9	1	1	1

B. Design a floating-point subtractor that performs $(F_1 \times 2^{E1}) - (F_2 \times 2^{E2})$. Each floating-point number consists of an 8-bit fraction (including sign) and a 5-bit exponent (including sign), with negative numbers represented in 2's complement. A zero fraction should be associated with the negative exponent with the largest magnitude. Assume that the fractions are initially normalized (or zero) and the final result, i.e., the difference $(F_d \times 2^{E_d})$, should be normalized (or zero). Set an overflow flag (*Ovf*) if the final answer is overflow, i.e., the final answer has an exponent overflow. Assume that all registers (F_1 , E_1 , F_2 , and E_2) can be loaded in one clock time when a start signal (*St*) is received. (Hint: Do not transform negative numbers to positive ones before operation. Perform subtraction by 2's-complement addition.)

(a) Draw the **block diagram**. If $E_1 > E_2$, the control signal *GT* = 1, and if $E_1 < E_2$, the control signal LT = 1. Define all other control signals and status signals used. Include the special case where |E1 – E2 | > 7.

(b) Draw the **SM chart**.

(c) Write the behavioral **Verilog circuit module** for this floating-point subtractor. The circuit module should be named as *HW3_FP_subtractor*, and its file should be named as *HW3_FP_subtractor.v* .
The order of the port list of this Verilog module must be *Clk*, *St*, *F1*, *E1*, *F2*, *E2*, *Fd*, *Ed*, *Done*, *Ovf*.

(d) Please determine the correct fractions and exponents of the differences for the subtraction of the data shown in the following table. Then, write a **test bench** to test the circuit module designed in (c) including these testcases at least. Name the testbench module as *t_HW3_FP_subtractor* and its file as *t_HW3_FP_subtractor.v* . After saving, compile, and simulate these modules, observe the waveform of the simulation results and compare the simulation results with that of your calculation.

Testcase	Minuend 被減數		Subtrahend 減數	
	F1	E1	F2	E2
1	01010000	00101	01100000	00010
2	01111100	00010	01000010	00011
3	10110000	00110	10101000	01000
4	01110011	01000	10100000	00110
5	10010010	11011	01010000	11001
6	01110011	01111	10011000	01111
7	10001001	01111	01100000	01100
8	11100010	10011	10011100	11111
9	00000000	10000	10100111	10110
10	01100000	10010	01100000	10010

◆ 作業及 HDL 模組繳交 (Hand in)

- **作業繳交： pdf 檔，命名為 HW3_學號_姓名。**內容包含下列項目：
  Submit your homework report in a pdf file, named HW3_StudentID_Name , including the following items:

  A. (45%)

  i. 繪製 A(a)的 **SM chart**、說明 **two-address control word** 之格式、撰寫其 microprogram、並決定 microprogram ROM 之大小 (# words × # bits/word)。此外，根據最初的 SM chart，決定此電路若採傳統 LUT 設計所需之 **ROM size**。
  For A(a), draw the **modified SM chart** for the two-address microprogramming structure, describe the format of its control word, and write the microprogram, i.e., the ROM table, required to implement the circuit. Moreover, determine the size of the microprogram ROM and the ROM size of the traditional LUT method for implementing the original SM chart.

  ii. 繪製 A(b)的 **SM chart**、說明 **one-address control word** 之格式、撰寫其 microprogram、並決定 microprogram ROM 之大小。
  For A(b), draw the **modified SM chart** for the one-address microprogramming structure, describe the format of its control word, write the microprogram, and determine the microprogram ROM size.

  iii. 附上 A(d)模擬結果之波型圖，並解釋波形圖是否正確。
  Show the waveform of the simulation results for the circuit module in A(d), and explain whether the results are correct or not.

  B. (45%)

  i. 說明你的設計，包括控制訊號與狀態訊號的定義。繪製 B(a)(b)的**方塊圖**及 **SM chart**。
  Describe your design for Problem B and define the control signals and status signals used. Draw the **block diagram** and **the SM chart** in B(a)(b).

  ii. 附上 B(d)各組測資之計算答案及模擬結果的波型圖，並解釋波形圖是否正確。
  Show the answer calculated by you and the waveform of the simulation result for each testcase of the circuit module design in B(c), and explain whether the simulation results are correct or not.

  C. 心得感想、結論、及討論 (10%)
  Conclusions and Discussions

- **Verilog modules 檔案繳交：Hand in the following Verilog modules**
  HW3_SQTA_microprogram.v
  t_HW3_SQTA_microprogram.v
  HW3_FP_subtractor.v
  t_HW3_FP_subtractor.v

◆ 注意事項與繳交截止日期 (Notes and Deadline)

- 可用任意開發環境，但請在報告中說明你使用哪個模擬器。
  Use any simulator you want and explain which one you choose in the report.
- 請務必依照各題中之規定命名模組及檔案，並遵循各電路模組之輸出入順序。
  Be sure to name the modules and files and follow the order of the port list as described above.
- 助教會使用不同的測試模組來驗證同學的電路模組正確性。
  After you hand in your code, TA will use similar Testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.
- 本作業為一人一組。請將 Verilog 電路模組(.v)與作業報告 pdf 檔全部壓縮成一個 zip 或 rar 檔，命名為「HW3_學號_姓名」(如 ： 「HW3_110550100_王大明」)，並上傳至 e3 平台。作業報告如為手寫，請務必用深色筆書寫，並確認掃描後檔案清晰易讀。
  This homework is one student per group. Please compress the Verilog circuit modules and the word file described above all into one **zip** or **rar** file, name the compressed file as "HW3_StudentID_Name" (for example, "HW3_110550100_Kent Chang"), and upload the compressed file onto e-Campus platform. If your homework report is handwritten, please use the dark colored pen and make sure that it is clearly and legibly after scan.
- 繳交截止日期為 2022/12/21 (三) 23:55。每遲交一天，本作業扣總分 10%，至多可遲交四天。
  The deadline is **2022/12/21 (Wed.) 23:55.** The penalty of late hand-in is 10% deduction of the total point per day, and four days late at most.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point