數位系統設計 (Digital System Design)

Homework 1

A. The logic diagram of a combinational circuit is shown in Figure 1. Please write the Verilog circuit module and test bench for this circuit. The order of the port list of the Verilog circuit module should be *F*, *A*, *B*, *C*, *D*.

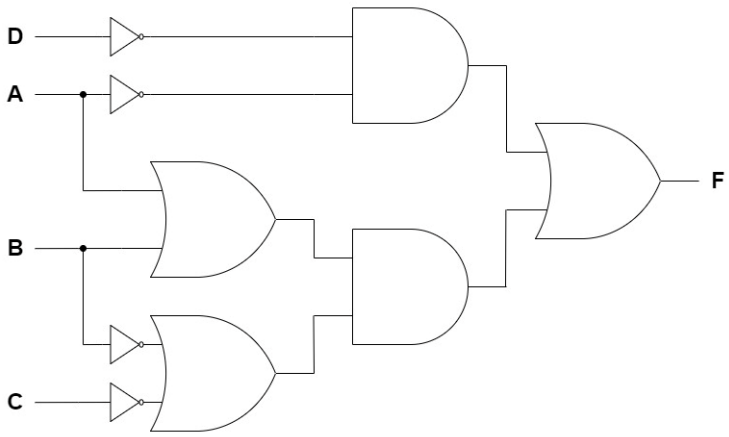


Figure 1: The logic diagram of the combinational circuit.

$$F(A, B, C, D) = A'D' + (A + B)(B' + C')$$

(a) Write the Verilog circuit module in **dataflow modeling** by using **assign** concurrent statements. The circuit module should be named as *HW1_comb_dataflow*, and its file should be named as *HW1_comb_dataflow.v* .

(b) Write the Verilog circuit module in **gate-level modeling** by using **built-in primitives**. The propagation delay (inertial delay) of a gate , including AND, OR, and NOT (inverter) gate, is set to 10 ns. The circuit module should be named as *HW1_comb_gatelevel*, and its file should be named as *HW1_comb_gatelevel.v* .

(c) Check whether the circuit shown in Figure 1 has ***static hazards*** (static 1- or 0-hazards) or not. Explain your reasons. If the circuit has static hazards, identify the hazards and redesign the circuit to eliminate the hazards. Write the Verilog circuit module for the corresponding ***hazard-free*** circuit in **gate-level modeling** with the same delays of gates expressed in (b). The circuit module should be named as *HW1_comb_hf_gatelevl*, and its file should be named as *HW1_comb_hf_gatelevel.v* .

(d) Write a testbench to test the two/three circuit modules designed above thoroughly including hazard detection. The testbench module should be named as *t_HW1_comb*, and its file should be named as *t_HW1_comb.v* . After saving the modules, compile and simulate the modules and observe the waveform of the simulation result.

B. Write a Verilog code to observe the waveforms of the following five statements.

i.
```
always @(A, B)
begin
#5 C1 <= A ^ B;
end
```

ii.
```
always @(A, B)
begin
#5 C2 = A ^ B;
end
```

iii.
```
always @(A, B)
begin
C3 <= #5 A ^ B;
end
```

iv.
```
always @(A, B)
begin
C4 = #5 A ^ B;
end
```

v.
```
assign #5 C5 = A ^ B;
```

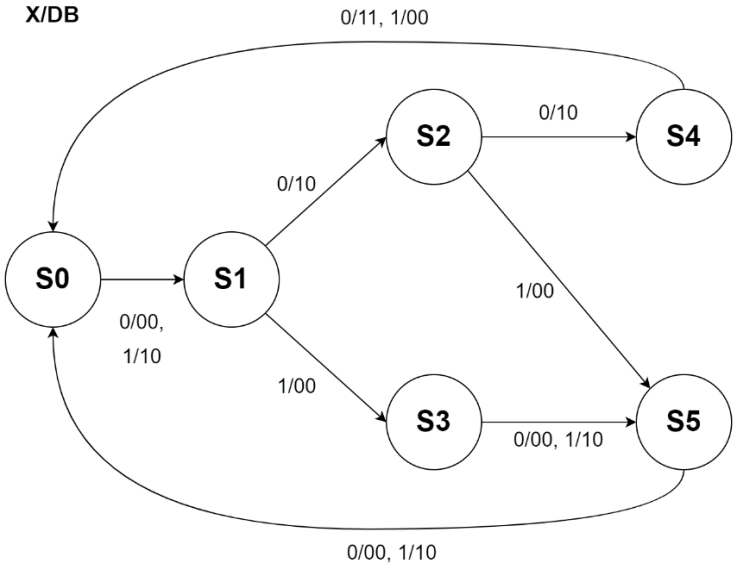
(a) Write a Verilog circuit module including the five statements given above. The order of the port list of the Verilog circuit module should be *C1, C2, C3, C4, C5, A, B*. The circuit module should be named as *HW1_delay*, and its file should be named as *HW1_delay.v* .

(b) Write a testbench to test the circuit module designed in (a) with A = 1 as the simulation starts and the value of B should be the same as the following simulator command:

force B 0 0, 1 4, 0 10, 1 15, 0 20, 1 30, 0 40

The testbench module should be named as *t_HW1_delay*, and its file should be named as *t_HW1_delay.v* . After saving the modules, compile and simulate the modules and observe the waveform of the simulation result.

C. Design a Mealy-type synchronous sequential circuit with one input (X) and two outputs (D and B). X represents a 4-bit binary number N, which is input least significant bit first. D represents a 4-bit binary number equal to $N - 2$, which is output least significant bit first. At the time the fourth input occurs, $B = 1$ if $N - 2$ is negative; otherwise, $B = 0$. The circuit always resets after the fourth bit of X has been received. The state diagram and state table of this Mealy-type synchronous sequential circuit are shown below. S0 is the initial state.



Present State	Next State		Output (DB)	
	X = 0	X = 1	X = 0	X = 1
S0	S1	S1	00	10
S1	S2	S3	10	00
S2	S4	S5	10	00
S3	S5	S5	00	10
S4	S0	S0	11	00
S5	S0	S0	00	10

Figure 2: The state diagram and state table of the synchronous sequential circuit.

We choose D flip-flops for the state register, and assign states as follows:

S0 = 000, S1 = 001, S2 = 010, S3 =011, S4 = 100, S5 = 101 $(Q_2Q_1Q_0)$

The memory input equations and the output equations for this circuit are listed as follows:

$$\mathbf{D_2 = Q_2^+ = Q_1}$$
$$\mathbf{D_1 = Q_1^+ = Q_2'Q_1'Q_0}$$
$$\mathbf{D_0 = Q_0^+ = Q_2'Q_1'Q_0' + Q_2'X + Q_1Q_0}$$
$$\mathbf{D = Q_2'Q_1'Q_0'X + Q_2'Q_1'Q_0X' + Q_1Q_0'X' + Q_2Q_0'X' + Q_1Q_0X + Q_2Q_0X}$$
$$\mathbf{B = Q_2Q_0'X'}$$

This synchronous sequential circuit is positive edge triggered with an active-LOW asynchronous clear (*CLR*). **Ignore the delay issue** and do **comply with the guidelines of writing synthesizable Verilog code**. The order of the port list of the Verilog circuit modules must be *D, B, X*, *CLK*, *CLR*.

(a) Write a **behavioral** Verilog description for this sequential circuit according to the state diagram or the state table of the circuit. The behavioral module should have **two always blocks**, one for the combinational part of the circuit and another for the state register. The circuit module should be named as *HW1_sub2_behavioral*, and its file should be named as *HW1_ sub2_behavioral.v.*

(b) Verify the memory input equations (D_0, D_1, D_2) and output equations (D, B) of this circuit given above. If there is any mistake, correct it. Write the Verilog circuit module in **data flow modeling** according to the next-state equations and output equations. The circuit module should be named as *HW1_sub2_dataflow*, and its file should be named as *HW1_sub2_dataflow.v.*

(c) Draw the logic circuit diagram of this synchronous sequential circuit according to the memory input equations and the output equations of this circuit. Label the number of each gate and flip-flop, and name each intermediate point in the circuit. Write the Verilog circuit module for this circuit by **structural modeling** according to your logic circuit diagram. The circuit module should be named as *HW1_sub2_structural*, and its file should be named as *HW1_sub2_structural.v*. Note that this circuit module requires to instantiate the circuit module of D flip-flop. You may design the D flip-flop module which is positive edge triggered with an active-LOW asynchronous clear by yourself or apply the module provided in the textbook. The D flip-flop module should be named as *D_ff*, and its file should be named as *D_ff.v* .

(d) Write a test bench to test the circuit modules designed in (a), (b), and (c). The test bench module should be named as *t_HW1_sub2*, and its file should be named as *t_HW1_sub2.v*. The test bench module should include the following input sequence at least:

X = 1 0 0 1 0 0 0 0 1 1 0 1 1 1 0 0 0 0 1 0 ...

Start the test from the initial state S0. *X* should change 1/4 clock period after the rising edge of the clock. After saving the modules, compile and simulate the modules and observe the waveform of the simulation result.

◆ 注意事項 (Notes)

- **可用任意開發環境，但請在報告中說明你使用哪個模擬器。**
  Use any simulator you want and explain which one you choose in the report.
- **請務必依照各題中之規定命名模組及檔案，並遵循各電路模組之輸出入順序。**
  Be sure to name the modules and files and follow the order of the port list as described above.

- **助教會使用不同的測試模組來驗證同學的電路模組正確性。**
  After you hand in your code, TA will use similar Testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

◆ 作業及 HDL 模組繳交 (Hand in)

- **作業繳交： pdf 檔，命名為 HW1_學號_姓名。**包含下列內容：
  A. i. 說明圖 1 之電路是否有 static hazards (static 1-hazards 及/或 static 0-hazards)。若此電路有 static hazards，請說明甚麼情況下會發生，並敘述如何設計出其相對的 hazard-free 電路。
  ii. 列出 A(d)模擬結果之波型圖，說明各電路模組的波形圖是否正確，並標示輸出訊號在何處發生 static hazards。
  B. 列出模擬結果的波形圖，並說明各電路模組的波形圖是否正確及形成原因。
  C. i. 請問前文中提供的同步順序電路之 memory input equations 及 output equations 是否有誤？若有誤，請說明你的更正。
  ii. 畫出此電路之 logic circuit diagram，標示 gates 及 flip-flops 的編號，並標示各中間點的命名。
  iii. 列出 C(d) 模擬結果之波型圖，並說明各電路模組的波形圖是否正確。
  D. 心得感想、結論、及討論

  Hand in a pdf file, named HW1_StudentID_Name , including the following contents:
  A. i. Describe whether the circuit shown in Figure 1 has static hazards (static 1- or 0-hazards) or not. Explain your reasons. If the circuit has static hazards, identify the hazards and describe your design of its corresponding hazard-free circuit step by step.
  ii. Show the waveform of the simulation results for the circuit modules tested in A(d), explain whether the results are correct or not, and indicate the occurrences of hazards, if any.
  B. Show the waveform of the simulation results for the circuit modules tested, and explain whether the results are correct or not and the reason of the result.
  C. i. Is there any mistake in the memory input equations and the output equation of the synchronous sequential circuit given above? If yes, describe your correction clearly.
  ii. Draw the logic circuit diagram of this synchronous sequential circuit according to the memory input equations and the output equations of this circuit. Label the number of each gate and flip-flop, and name each intermediate point in the circuit.
  iii. Show the waveform of the simulation results for the circuit modules tested in C(d), and explain whether the results are correct or not.
  D. Conclusions and Discussions

- **Verilog modules 檔案繳交：Hand in the following Verilog modules (11 .v files)**
  HW1_comb_dataflow.v,
  HW1_comb_gatelevel.v,
  HW1_comb_hf_gatelevel.v
  t_HW1_comb.v

HW1_delay.v
t_HW1_delay.v
HW1_sub2_behavioral.v,
HW1_sub2_dataflow.v,
HW1_sub2_structural.v,
D_ff.v,
t_HW1_sub2.v

◆ 繳交注意事項與截止日期 (Deadline)

- **本作業為一人一組，請將報告及 Verilog 檔案上傳至 e3 平台。報告如為手寫，請務必用深色筆書寫，並確認掃描後檔案清晰易讀。**
  This homework is one student per group. Please upload your HDL code (.v files) and report (a word file) onto e-Campus platform. If your homework report is handwritten, please use the dark colored pen and make sure that it is clearly and legibly after scan.

- **請將報告 pdf 檔及 Verilog 模組(.v)全部壓縮成一個 zip 檔，並以「HW1_學號_姓名」的方式命名，如 ： 「HW1_109550600_王大明」。**
  Please compress the pdf file and the Verilog modules (.v) and described above all into one zip file, and name the compressed file as "HW1_StudentID_Name" , for example, "HW1_109550600_MingWang".

- **繳交截止日期為 2022/10/19 (三) 23:55。每遲交一天，本作業扣總分 10%，至多可遲交四天。**
  The deadline is **2022/10/19 (Wed.) 23:55.** The penalty of late hand-in is 10% deduction of the total point per day, and four days late at most.

- **禁止抄襲，違者(不論抄襲者或被抄襲者)以 0 分計算。**
  Any assignment work by fraud will get a zero point