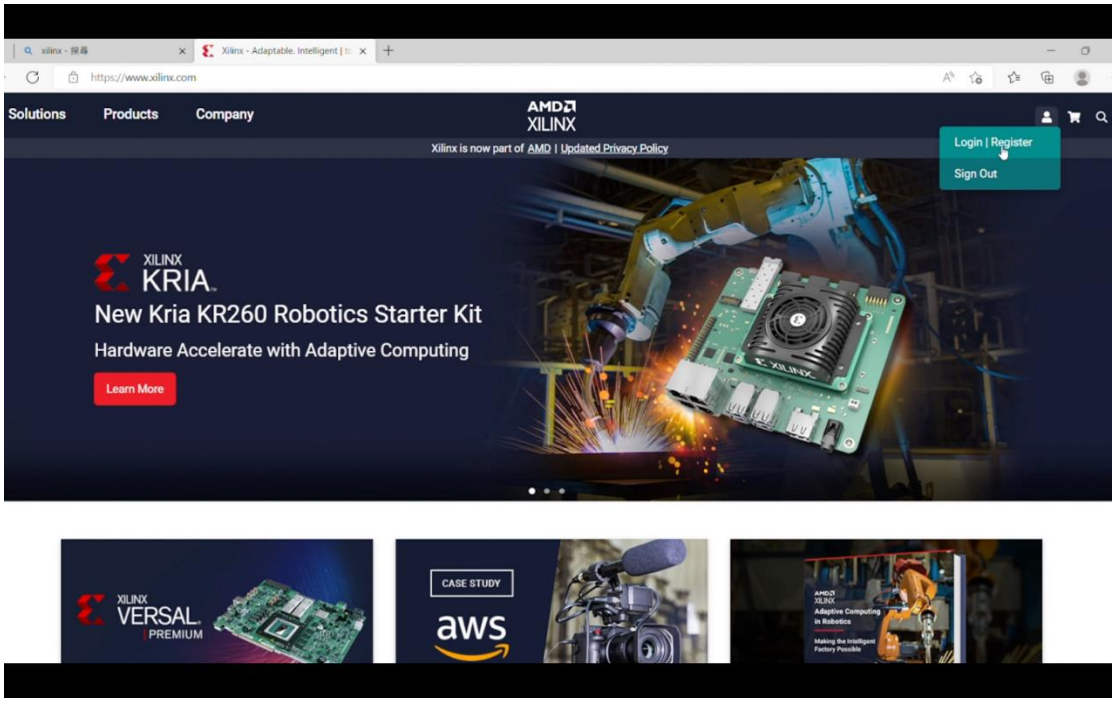
Verilog HDL 模擬 Vivado 與 Icarus Verilog 之安裝與使用(The Setup and Use of Verilog Simulators, Vivado and Icarus Verilog)

A. Vivado (Recommended)

在 Windows 系統下推薦使用(Alowed only under Windows)

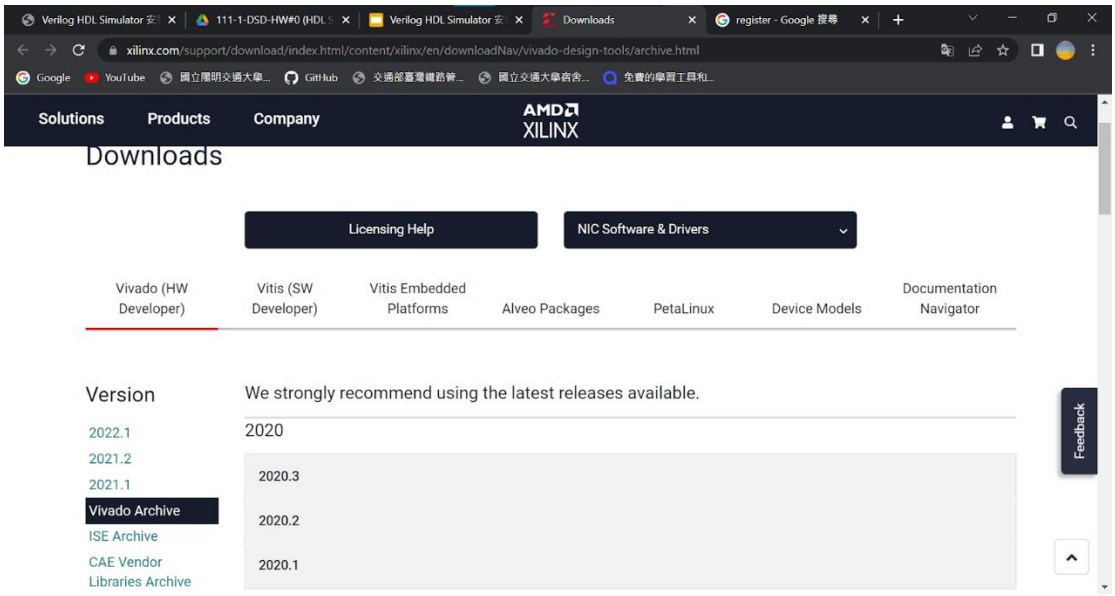
一、 Vivado 之下載、安裝及取得授權 (Download, Setup, and Authorization of Vivado)

(a) 連結至「 https://www.xilinx.com」，如下圖所示，點選右上角 Login | Register。Link to https://www.xilinx.com , click Login | Register button on the upper right corner.

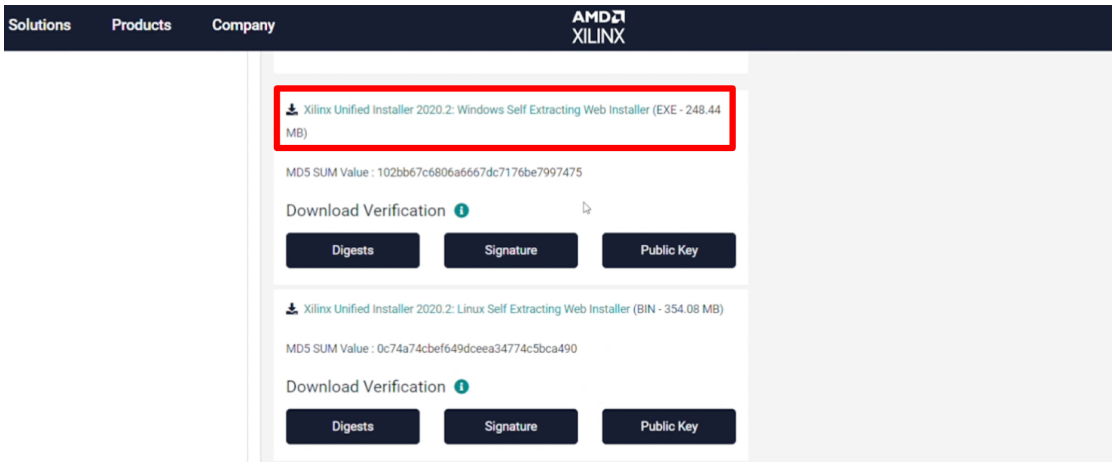


(b) 如果沒有帳號，按『創建密碼』創建帳號並以學校的電子郵件註冊之。創建完成之後輸入帳號密碼登入。If you do not have an account yet, create one by clicking “create password”. You are recommended to use the email provided by NYCU as your account.

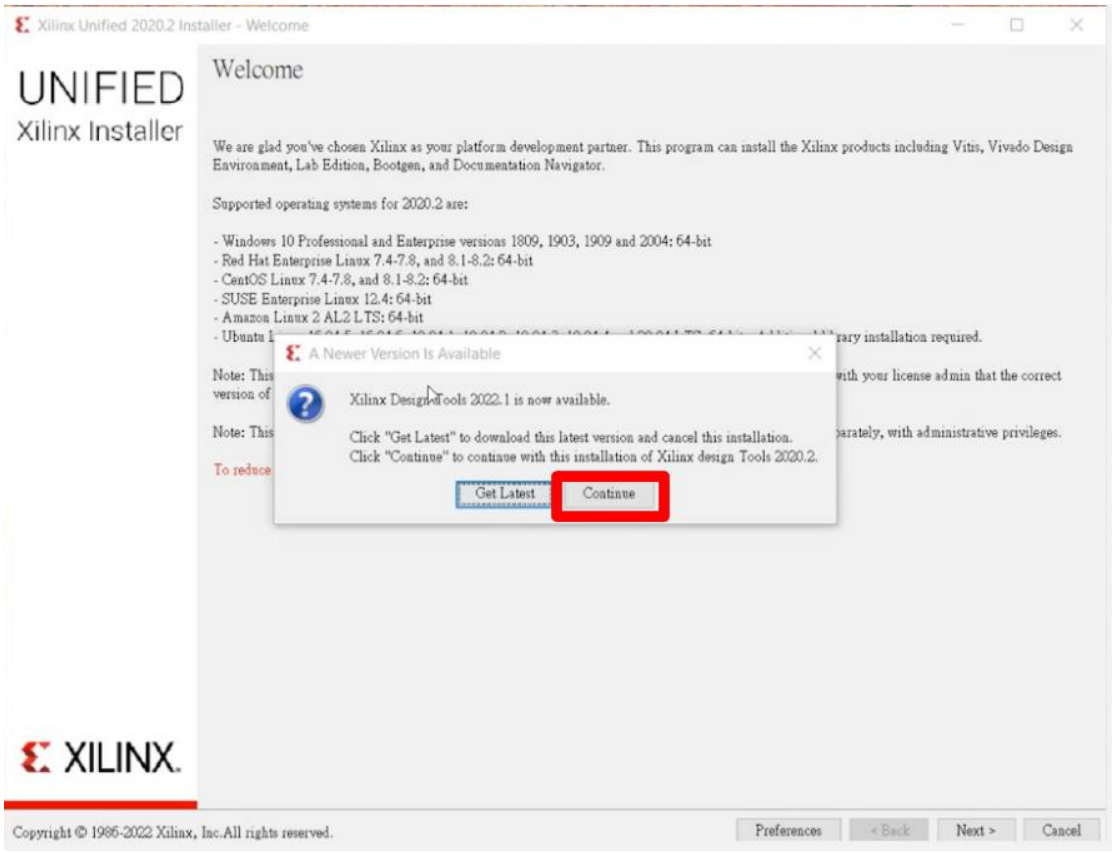
(c) 連結至「https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.html」，如下圖所示，點選 Vivado Archive 並找到 2020.2 版本。Link to https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.htmlhttps://www.xilinx.com/support/download.html, and the following page will be shown, make sure to download version 2020.2.



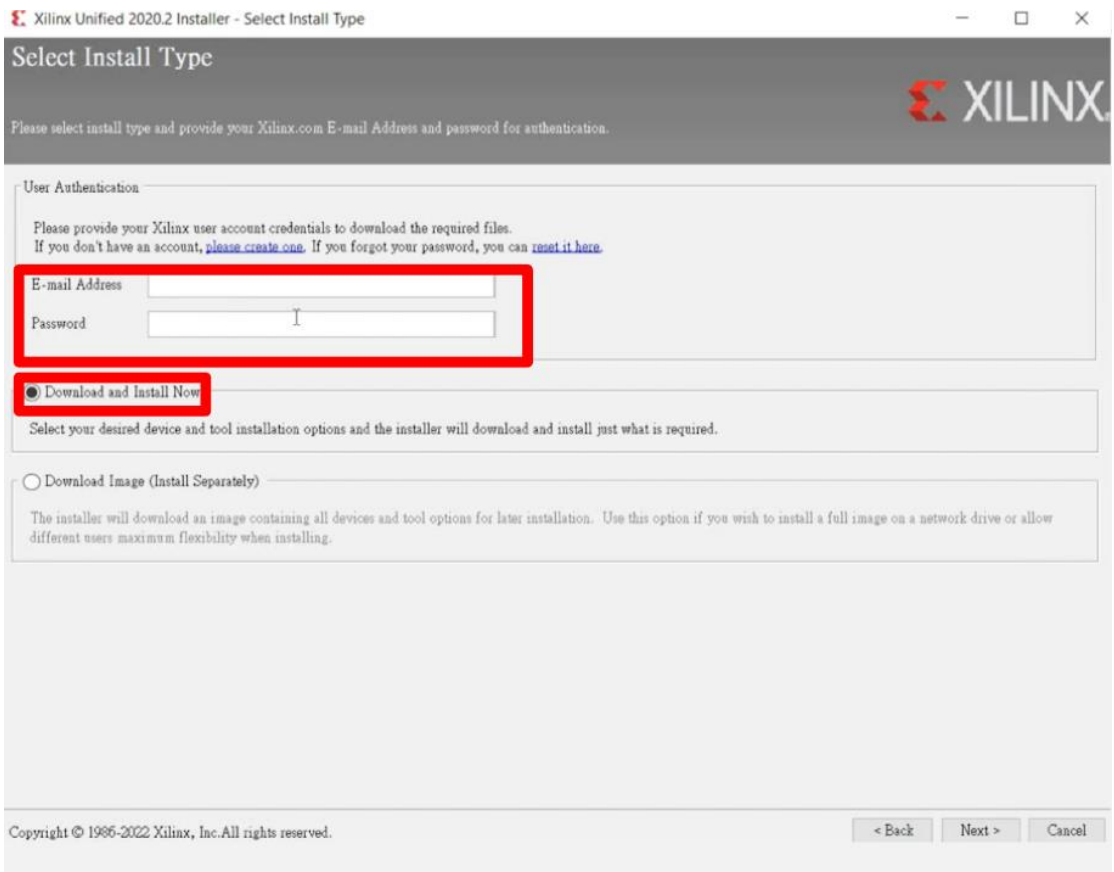
(d) 點選下載 Windows 版本。Windows Self Extracting Installer is the one to download



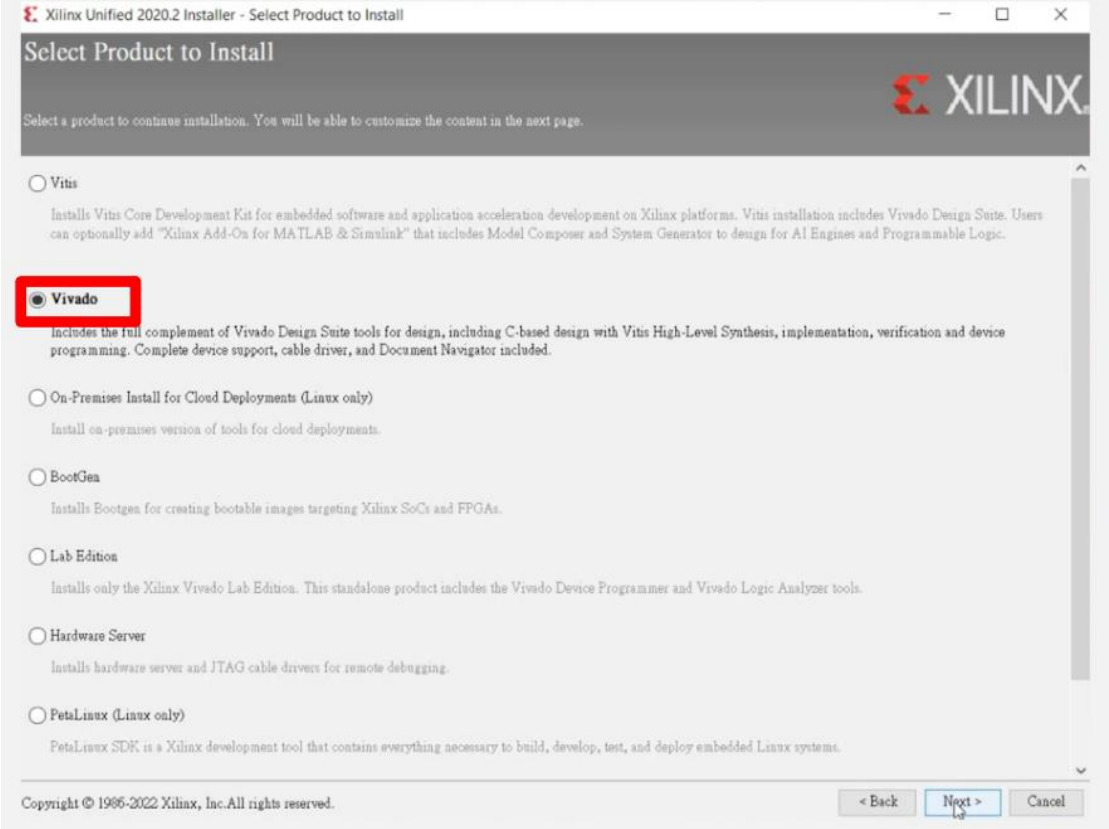
(e) 下載完成後打開安裝包，並按『continue』繼續安裝。Click on the downloaded installer, and click on “continue” to carry on the installation process.



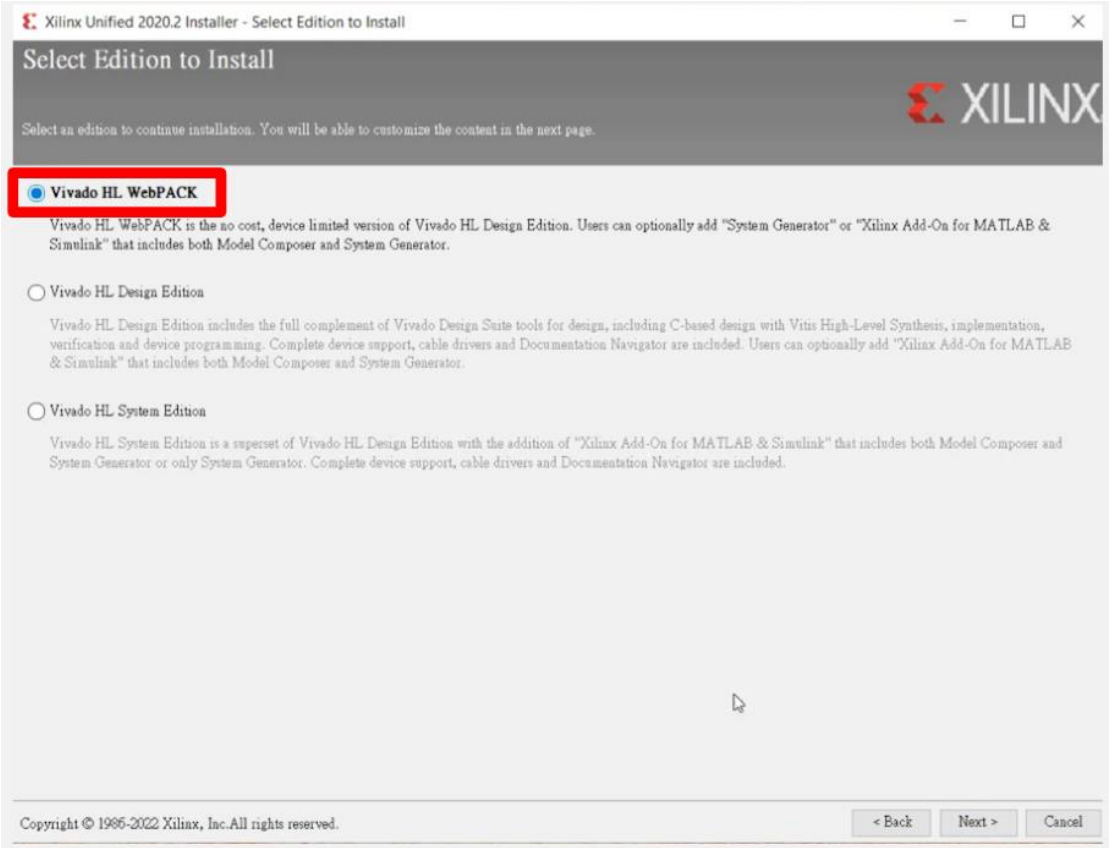
(f) 輸入帳號密碼完成認證，並點選『Download and Install Now』繼續下載。
Authenticate your download by entering your account and password you registered at Xilinx. And press “Download and Install Now”.



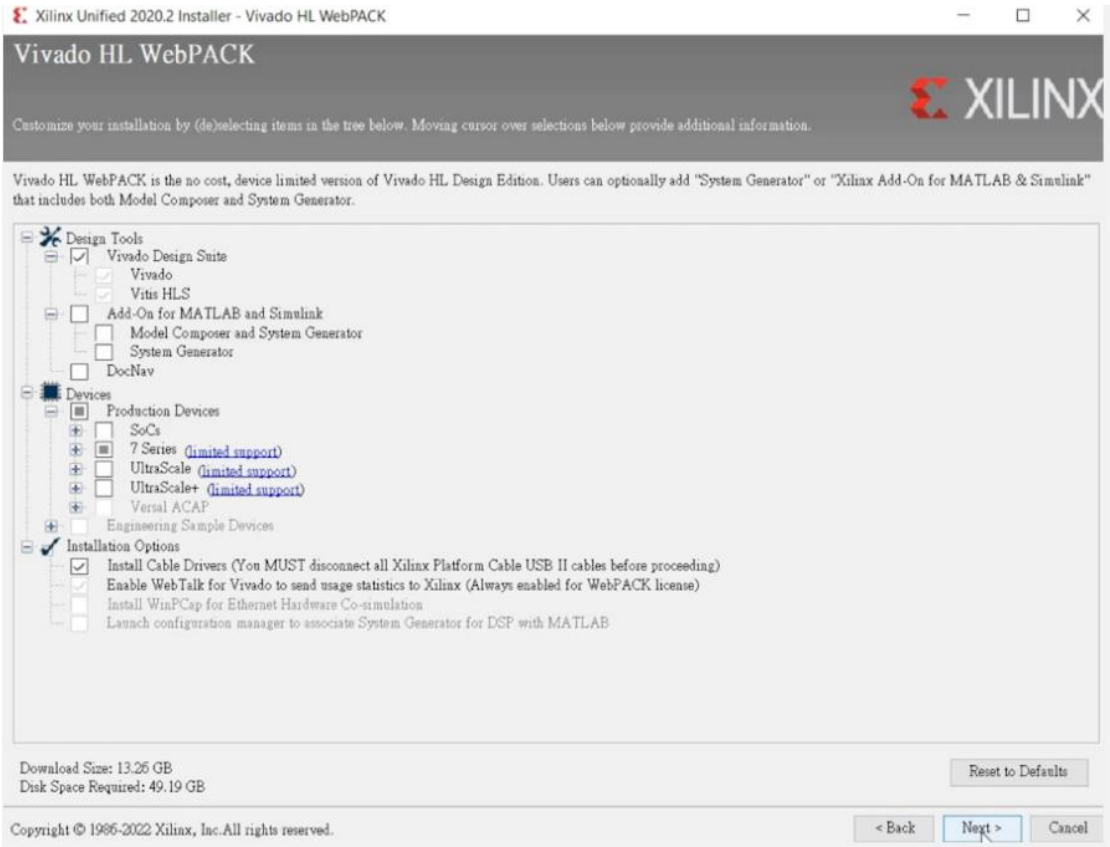
(g) 在產品選擇時選擇 Vivado。Choose Vivado at “Select Product to Install”



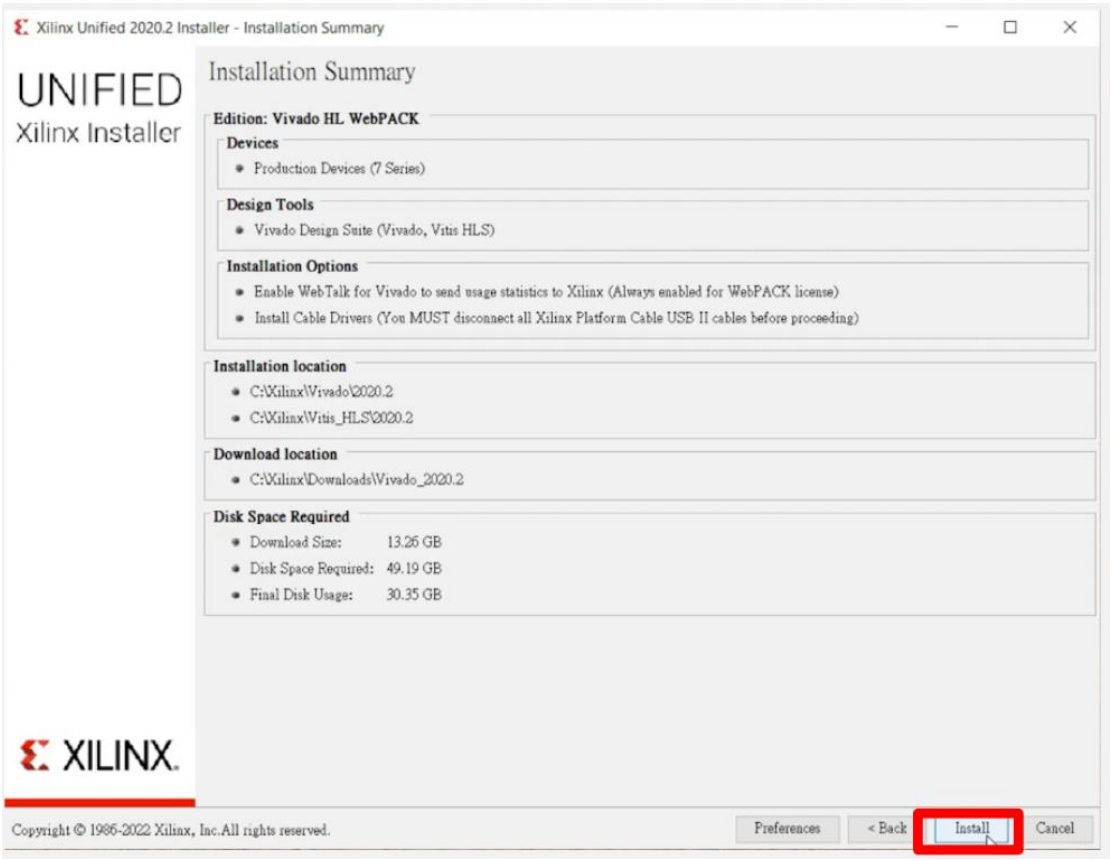
(h) 在版本選擇時請選 Vivado HL WebPACK。Choose Vivado HL WebPACK at “Select Edition to Install”.



(i) 之後的選擇如下圖所示。Check the checkboxes as the image showed below



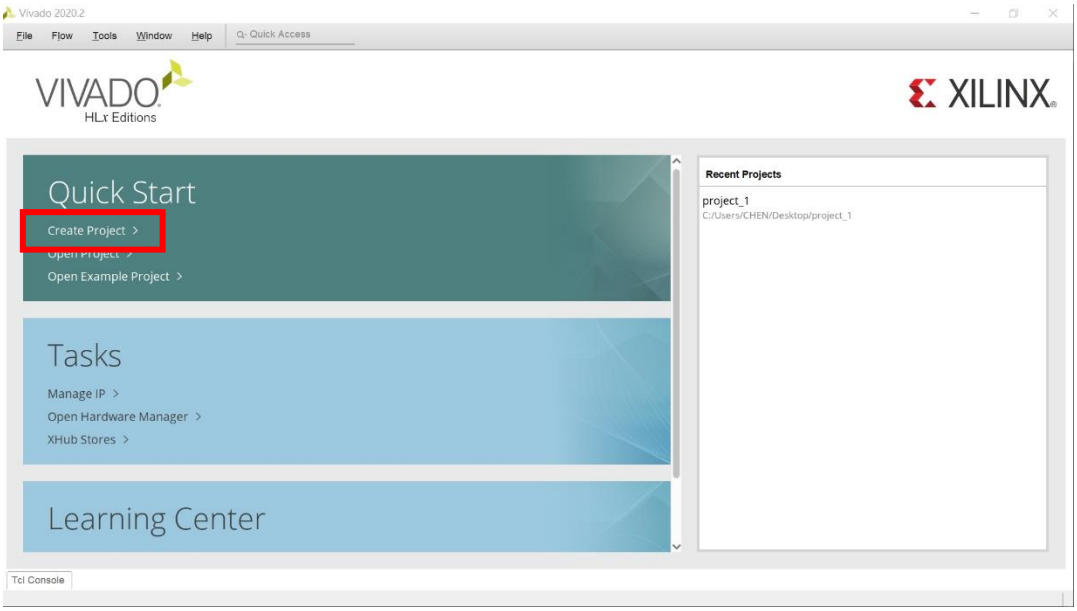
(j) 開始下載。Initiate the download.



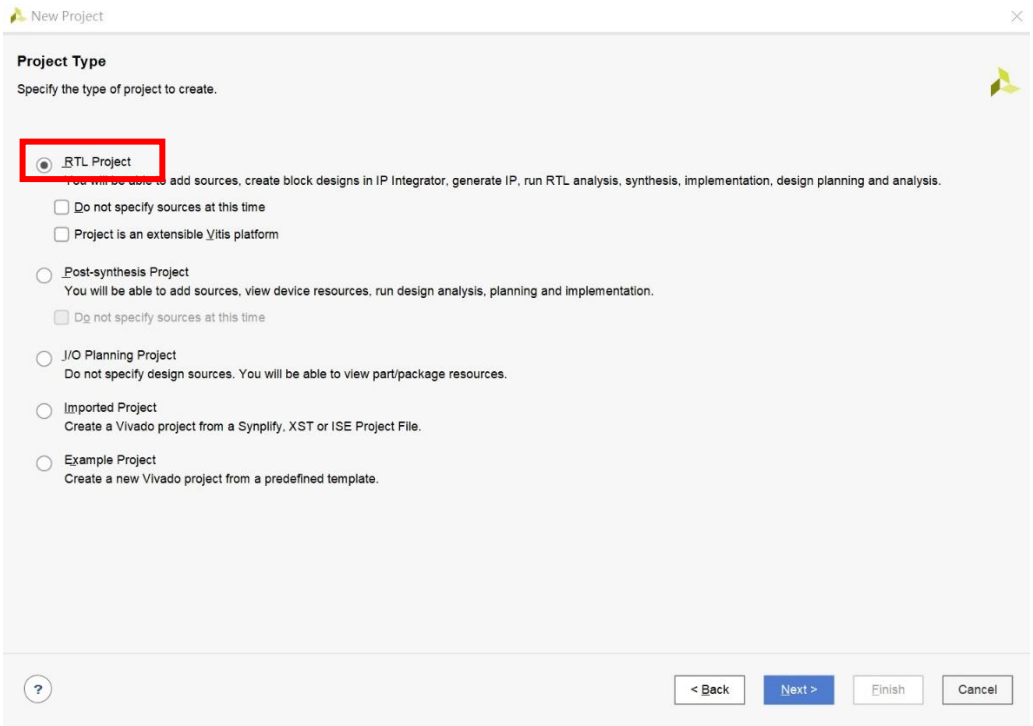
二、 Vivado 之專案建立、程式編譯及執行模擬 (Project Creation、Program Compilation and Simulation on Vivado)

I. 建立專案 (Project Creation)

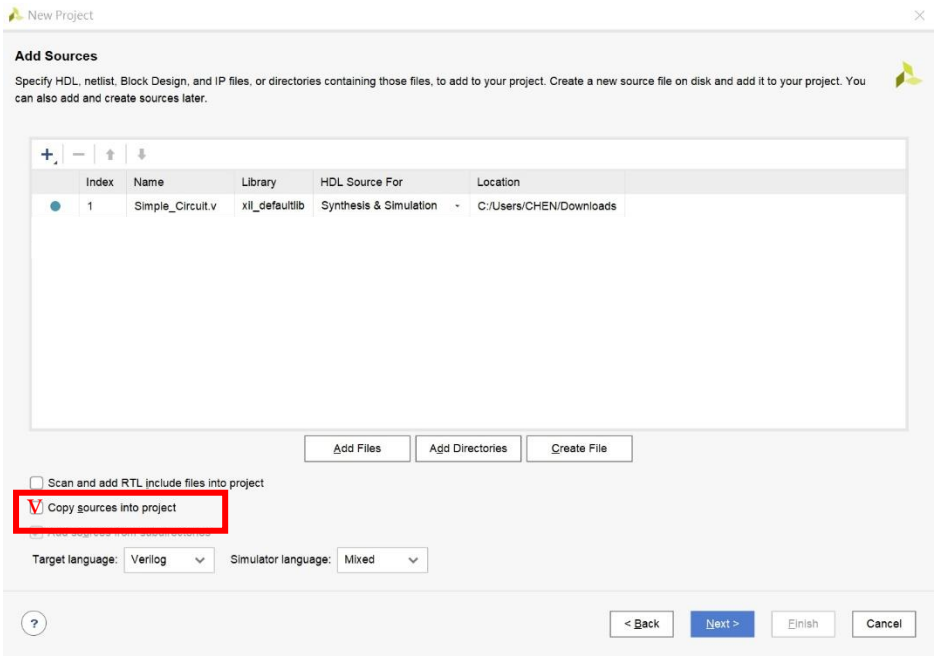
(a) 打開 Vivado 在初始頁面點擊 Create Project 建立新專案 (Open Vivado and click on “Create project” on the Quick Start block)



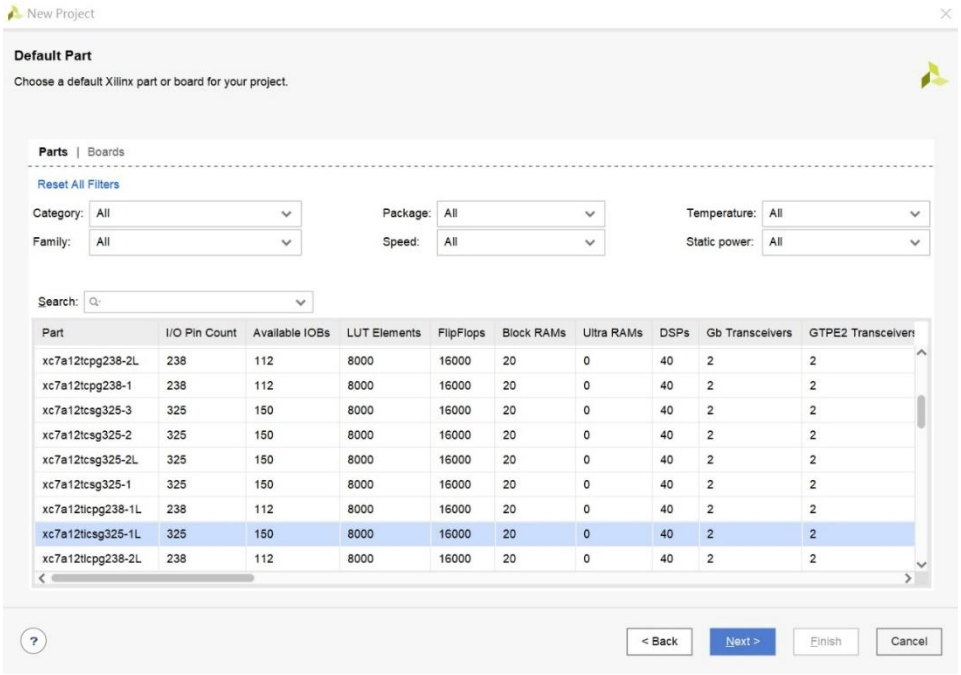
(b) 選擇 RTL Project (Choose RTL Project)



(c) 加入相關檔案或創建檔案 (Add source files or create some files) 建議勾選"Copy sources into project"，才能在 srcs 目錄下找到.v 檔，以免遺失。We suggest that clicking "copy sources into project" so you can find your .v files under srcs directory.

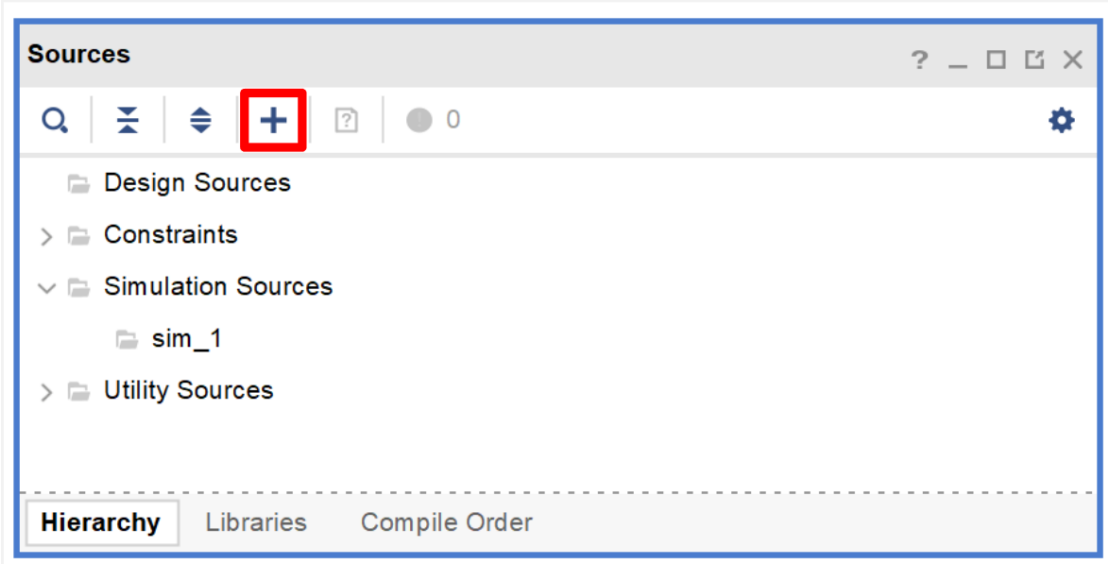


(d) Default Part 不需作更改，任選一個都可以 (No need to make changes in the "Default Part")

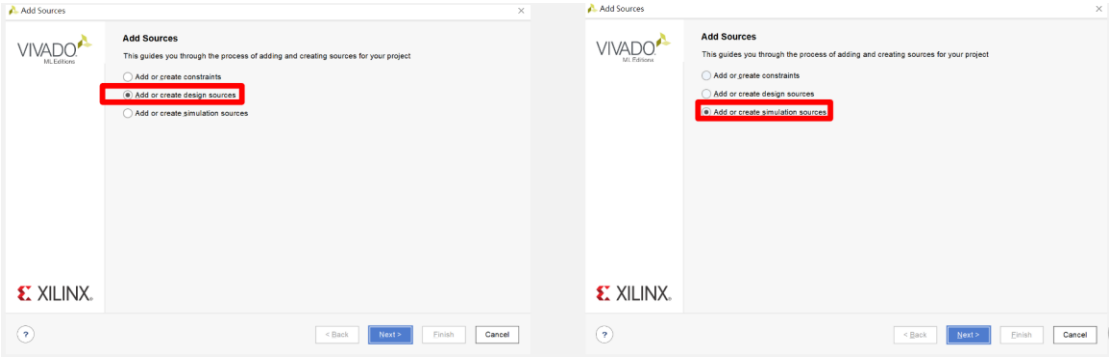


II. 新建檔案

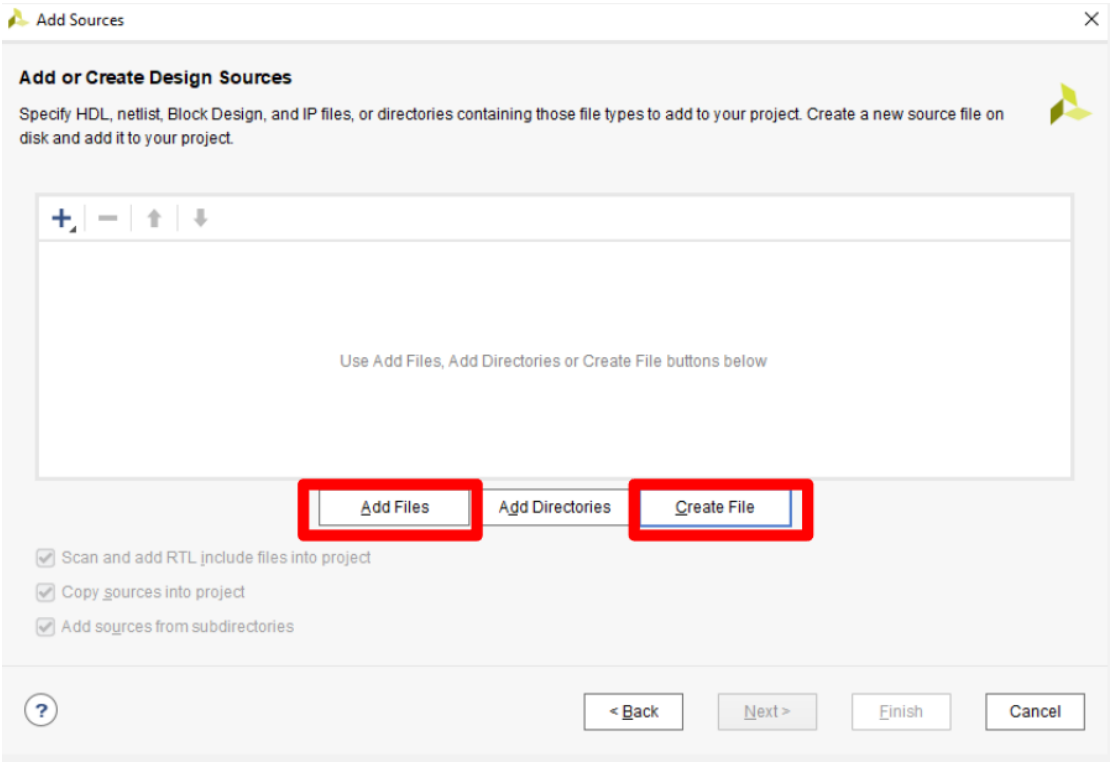
(e) 按下 Sources 控制區中按下「＋」按鈕 (Click the ＋ button shown on top of the screen in the "Sources" section.)



(f) 如果要創建的是模組的檔案，點擊第二個選項 - Add or create design sources，如左圖所示。創建 testbench 則選擇第三個 - Add or create simulation sources，如右圖所示(To add design sources, which is the files including non-testbench modules, check the second checkbox shown in the left screenshot. If it's testbench files you would like to add, the third option is the way to go, shown in the right)

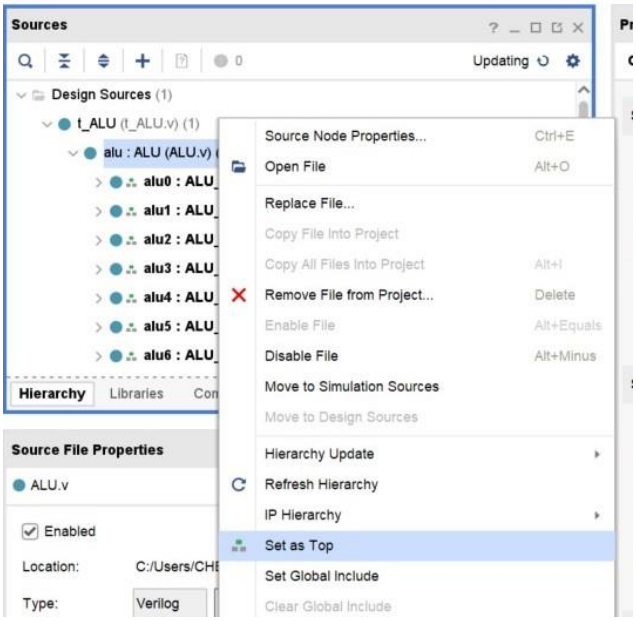


(g) 欲導入已經存在的檔案，按 "Add Files" 並從資料夾中選擇加入，建議勾選 "Copy sources into project"。如欲新創檔案，按 "create files" 並輸入檔案名稱(To add files that already exist to the project, click the "Add Files" button. In order to create files, press the 'Create File" button"



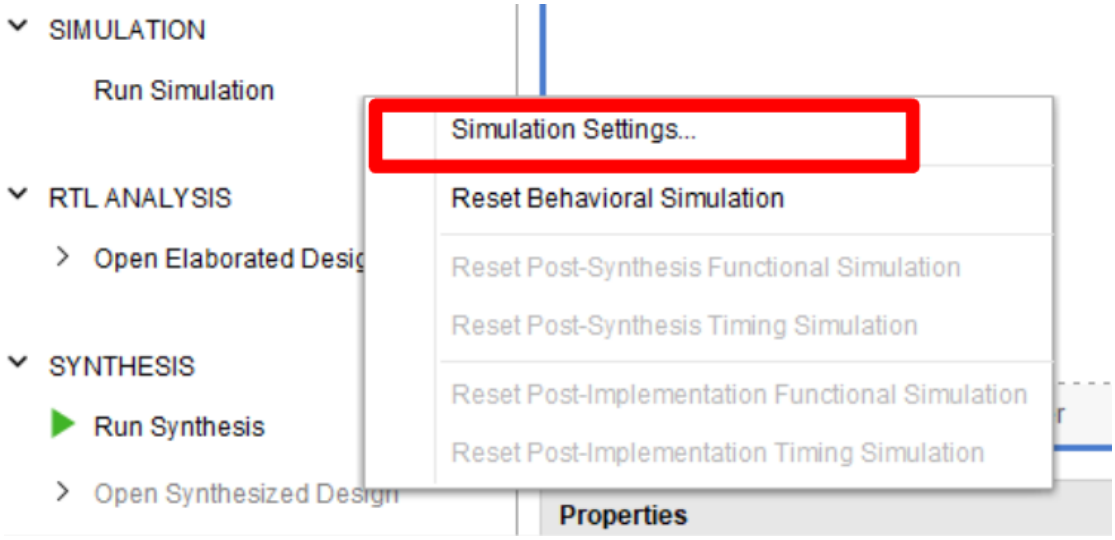
III. 執行模擬

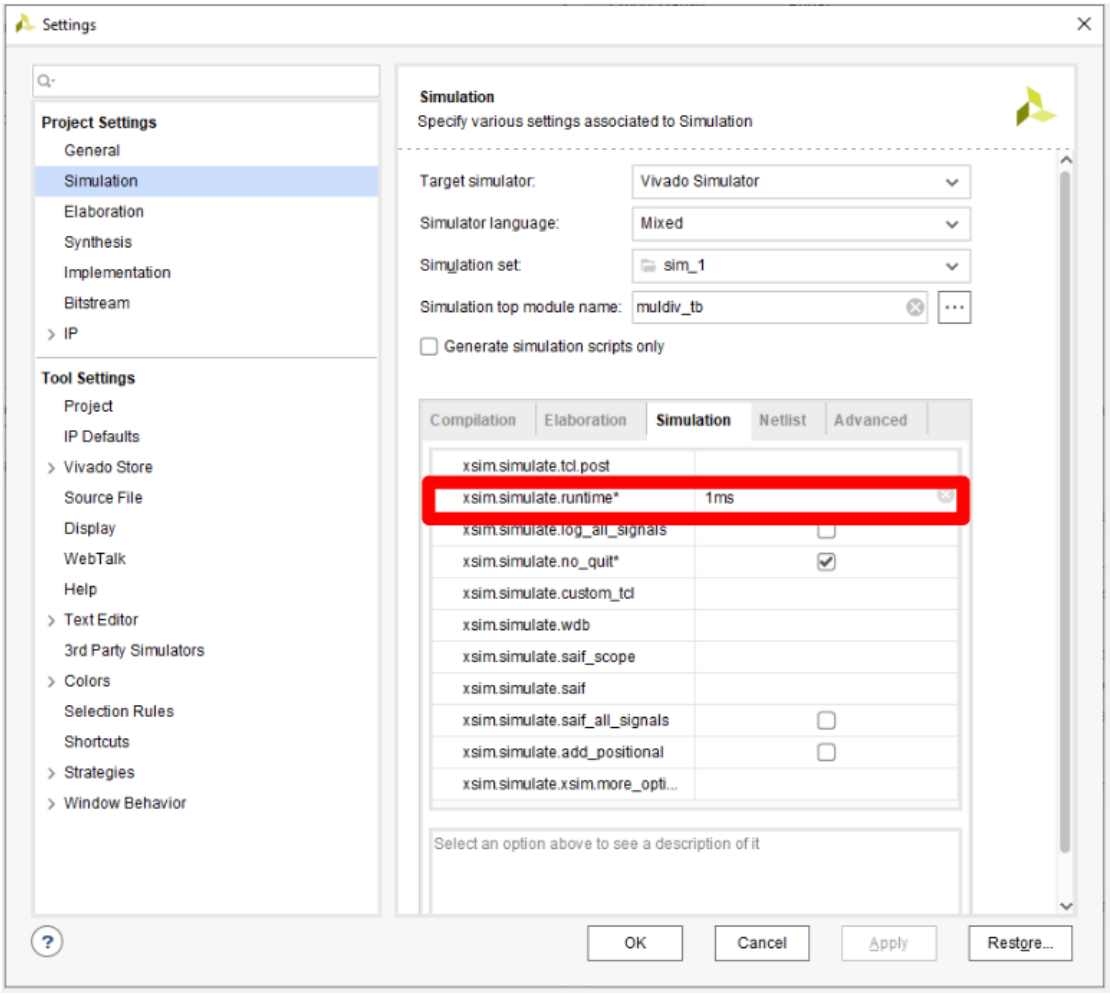
(a) 當有多層 Module 時，要確定 Hierarchy 有設定好。要確定把主要的模組”Set as top”來設定為 top module。When using multiple modules, use “Set as top” to set your top module.



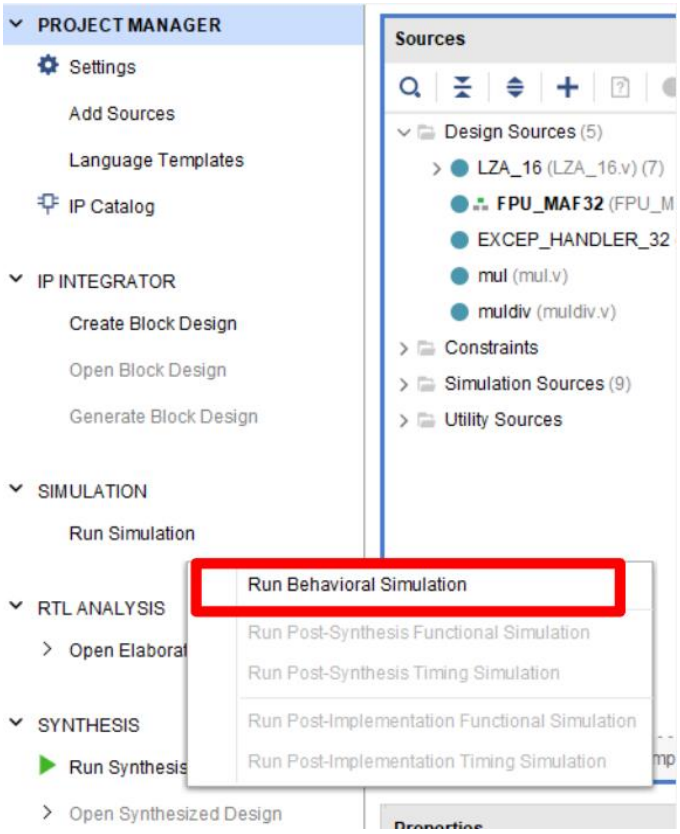
(b) 進到 Flow Navigator (左邊控制欄) > Simulation > (按右鍵) > Simulation Settings，確認模擬的時間 (xsim.simulate.runtime) 足夠長。(Navigate to the Flow Navigator, under the Simulation tag, right click to enter Simulation Settings. In the settings window, make sure that the simulation time is long

enough to simulate your module.)

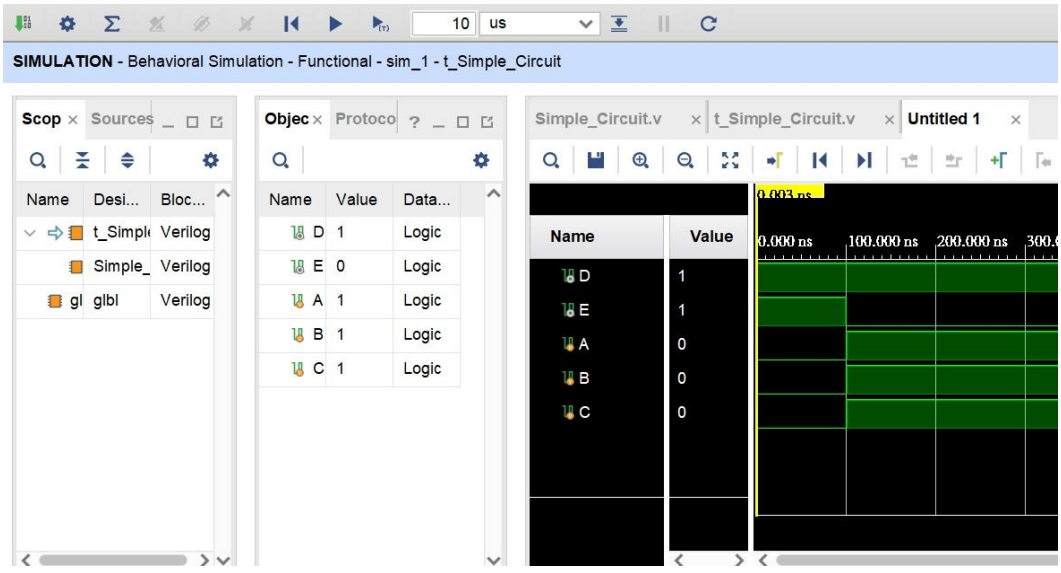




(c) 進到 Flow Navigator(左邊控制欄) > Simulation > Run Simulation > (按左鍵) >Run Behavioral Simulation。(Initiate the Simulation by navigate to the Flow Navigator located on the left side bar, left click Run Simulation button under the Simulation tag)



(d) 完成模擬，觀察結果之波形圖 (Complete simulation and observe the waveform of simulation results.)



三、 注意事項 (Notice)

當 Simulation 跑很久還沒跑出來時，可能是被防毒軟體擋下來了，可以把防毒軟體關起來試試 When it runs simulation for a long time, it may be blocked by your antvirus software. Turn it off and try.

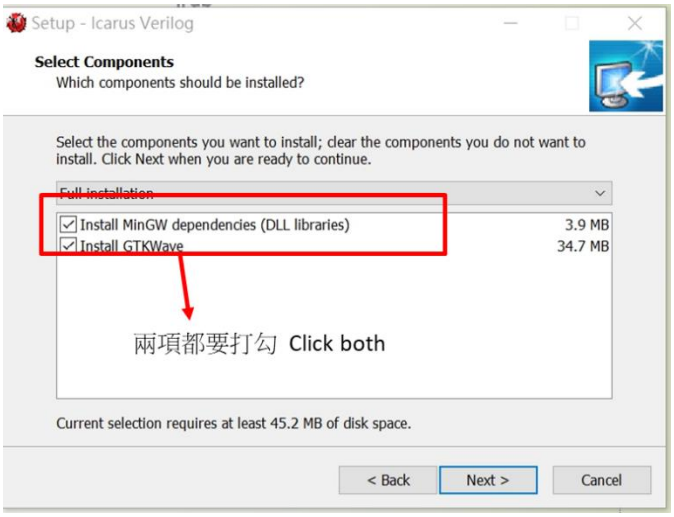
B. Icarus Verilog (iVerilog) & gtkwave Icarus Verilog (iverilog) & gtkwave

一、 Windows 環境下的安裝 (Download under Windows system)

I. 下載網址(Download here)：http://bleyer.org/icarus/

- 64 bit：iverilog-10.1.1-x64_setup.exe [9.77MB]
- 32 bit：iverilog-10.0-x86_setup.exe [11.1MB]

II. 安裝步驟 (Installation Steps)



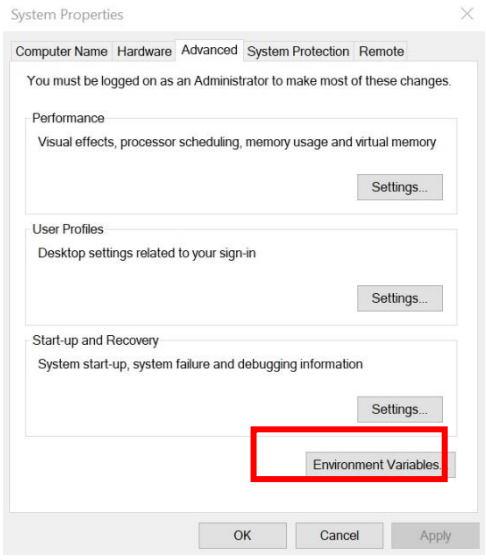
III. 新增環境變數(Add Environment Variable)

(a) 打開控制台 (System(Control Panel))

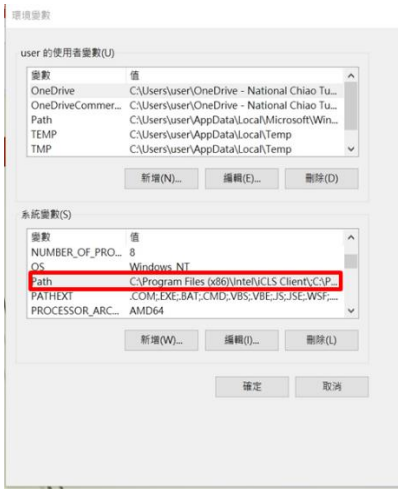
(b) 搜尋「進階系統設定」(search Advanced system settings)

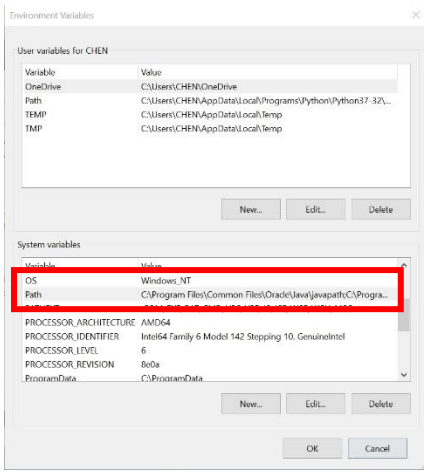
(c) 點選「檢視進階系統設定」(Click View advanced system settings)

(d) 點選「環境變數」(Click Environment Variables)

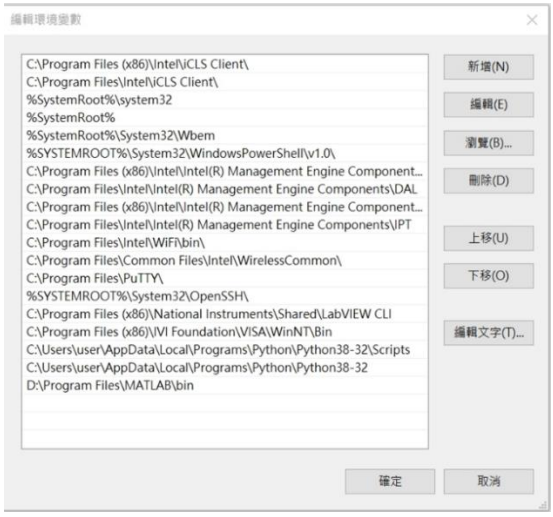


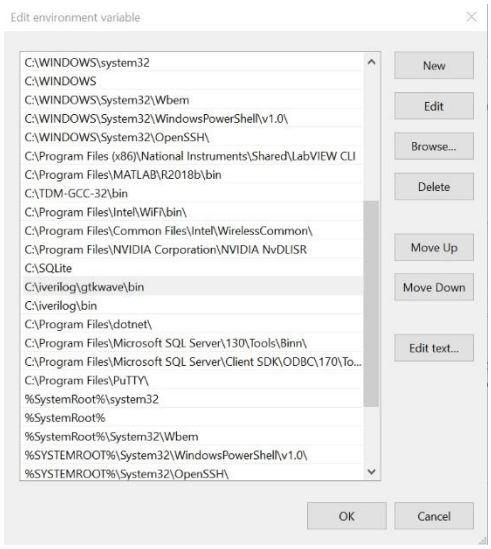
(e) 於系統變數中找到「Path」，點一下後按編輯 (Find **PATH** in the section System Variables. Click it and edit.)



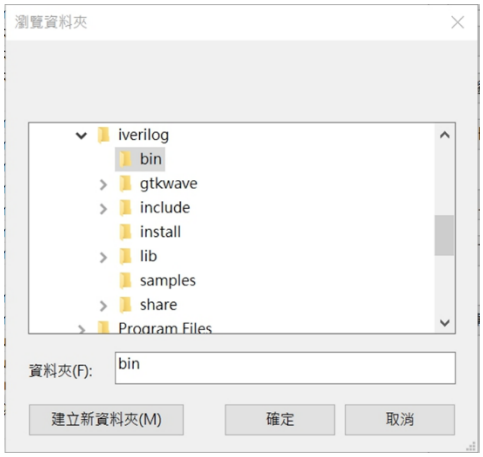


(f) 點選「新增」，之後點選「瀏覽」(Click **New**, and then click **Browse**.)





(g) 找到 iverilog/bin 後按確定 (Find iverilog/bin and click OK.)



(h) 點選「新增」(Click **New)** 之後點選「瀏覽」(Click **Browse)**，找到 iverilog/bin 後按確定(Find **iverilog/gtkwave/bin** and click OK)

(i) 按確定後即新增成功，之後須將電腦重新啟動 (After clicking OK, restart the computer)

二、 MacOS 環境下的安裝(Download under MacOS system)

I. 安裝 iverilog (Download iverilog)

(a) Install Homebrew

$ /usr/bin/ruby -e "$(curl -fsSL https://raw.githubusercontent.com/Homebrew/install/master/install)"

(b) Install icarus-Verilog

$ brew install icarus-Verilog

(c) 版本過舊問題 (Version Error)

若安裝過程遇到 CLT (CommandLineTools) 版本過舊的問題，可以執行下面兩條指令解決

Following two commands can solve the CLT version Error

$ sudo rm -rf /Library/Developer/CommandLineTools

刪除原有的 CLT (delete own CLT)

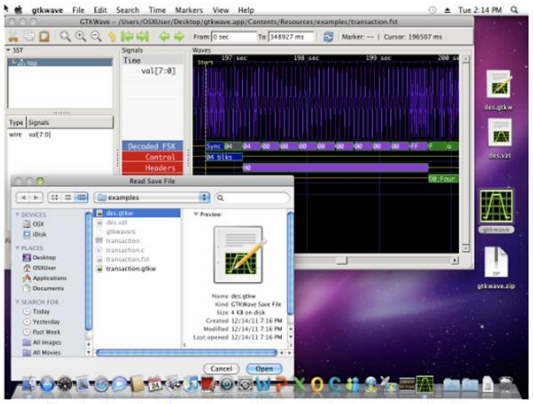
$ sudo xcode-select --install # 安裝新的 CLT (Install new CLT)

```
Error: Your CLT does not support macOS 11.2.
It is either outdated or was modified.
Please update your CLT or delete it if no updates are available.
```

II. 安裝 gtkwave (Download gtkwave)

(a) 下載網址 Download here：http://gtkwave.sourceforge.net/

點選 download (click **download**)



Simply download, unzip, and it is ready to run on the Mac...

(b) 解壓縮 gtkwave.zip，會看到應用程式 gtkwave
按住 **control**，打開 gtkwave
Unzip **gtkwave.zip** you'll see gtkwave
Press **control** and open gtkwave

(c) 接著會跳出警告視窗，點選打開
Click open on the warning window

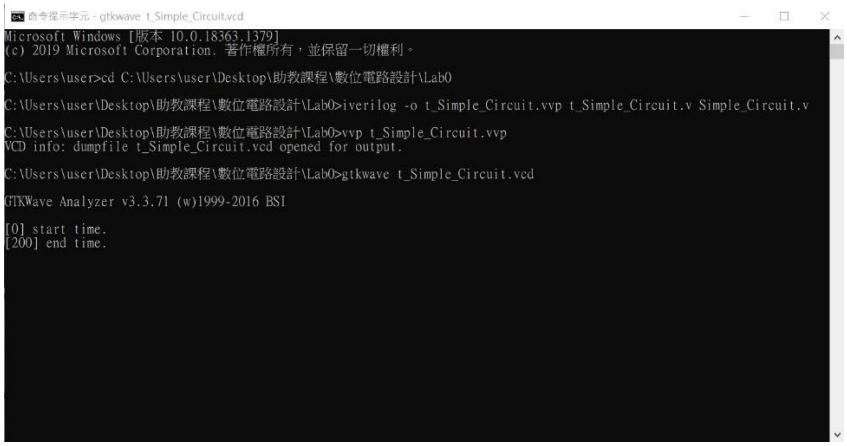
III. Iverilog 與 gtkwave 使用方式(Usage of iverilog and gtkwave)

(a) 下載提供的兩個檔案: Simple_Circuit.v 和 t_Simple_Circuit.v
Download files provided on E3 (Simple_Circuit.v & t_Simple_Circuit.v)

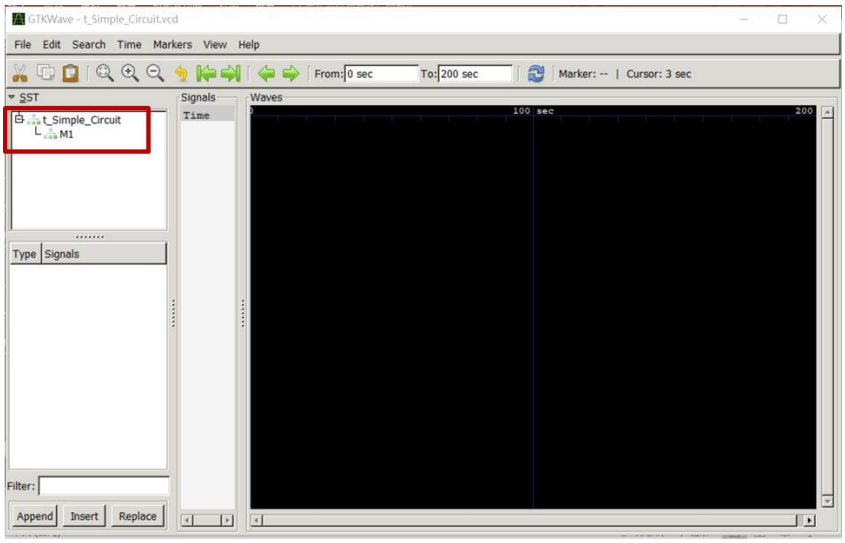
(b) 打開「命令提示字元」(終端機)
open Command Prompt

(c) 使用 cd [路徑]到達 Simple_Circuit.v 和 t_Simple_Circuit.v 所在資料夾
move to the directory your files at

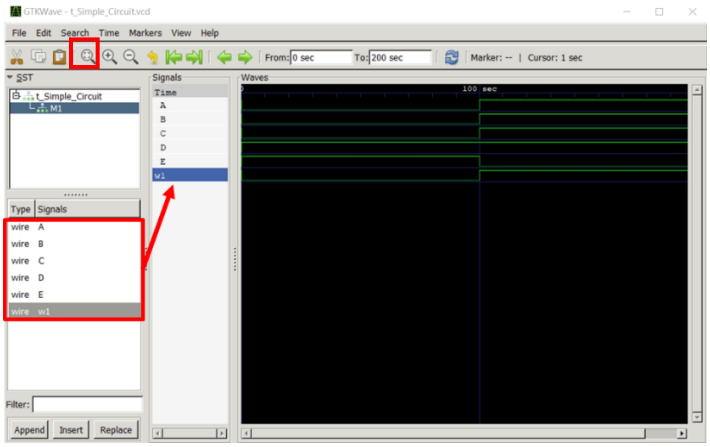
- iverilog -o t_Simple_Circuit.vvp t_Simple_Circuit.v Simple_Circuit.v
- vvp t_Simple_Circuit.vvp
- gtkwave t_Simple_Circuit.vcd



(d) gtkwave 視窗出現之後，點選 t_Simple_Circuit 旁邊的 +
並點選 M1
click + next to t_Simple_Circuit and click M1



將下方出現的五個變數拖至右側 Signals 欄
點選左上方的 讓波型以最適合螢幕大小的方式顯示
Drag variables below to the **Signals** section
Click so the waveform fit the window size properly.



IV. 撰寫 verilog 並編譯及執行的步驟 (Steps to compile Verilog code and run)

(a) 使用任意文字編輯器撰寫 module 及 testbench 並將副檔名皆存成.v
Use any text editot to finish your module and testbench. Stores them as .v file
E.g. notepad++、VSCode…

(b) 撰寫 testbench 務必於 initial begin 之後加入
Remember to add following lines in testbench after initial begin

```
$dumpfile("filenameA.vcd");
$dumpvars;
```

(c) 打開命令提示字元，使用 cd [路徑]到達.v 所在資料夾
Open Command Prompt and move to the directory your .v files at

```
iverilog -o filenameB.vvp testbench_filename.v module_filename.v
vvp filenameB.vvp
gtkwave filenameA.vcd
```