Control inputs : St

Control signal : Shr, Done, L, E, SL, EC

0 → no sht, 1 → Sht A[0] to B[9]

0 → load BCD

1 → load 經過處理好的A

clock : CLK

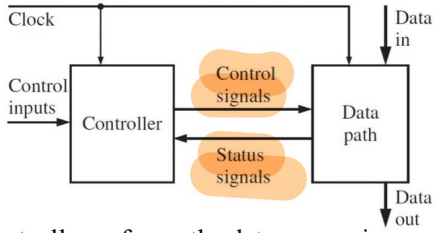
Data in : BCD

Data out : Binary

Status signal : c9

Traditional Design Methodology

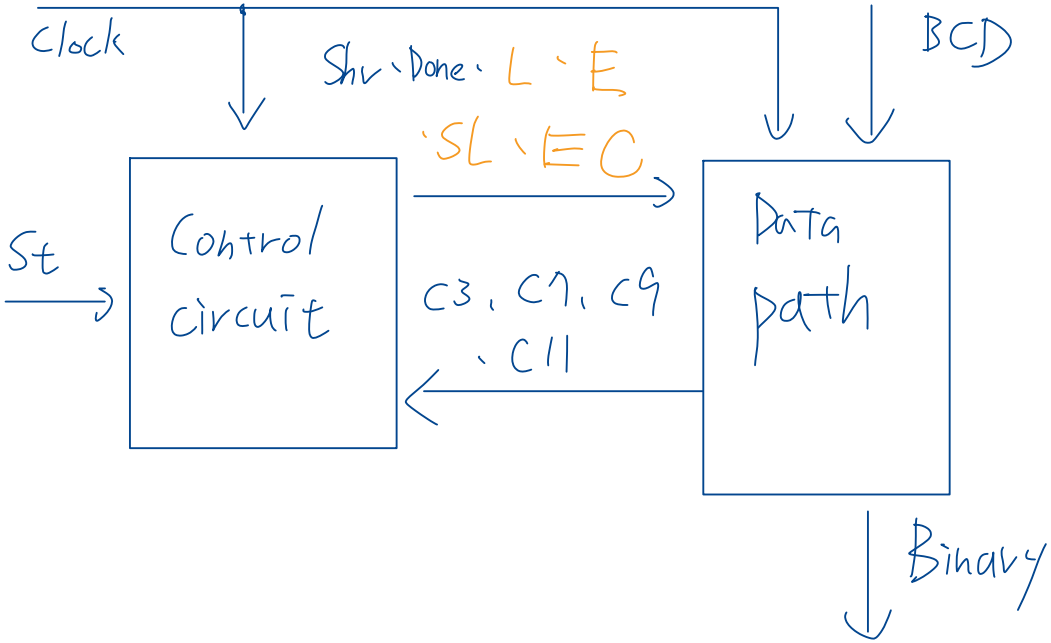
- Traditional design methodology:



- ***Data path***:
  - hardware that actually performs the data processing.
  - For microprocessor: the arithmetic and logic unit (ALU)
- ***Controller***:
  - sends ***control signals*** or commands to the data path.
  - can obtain feedback, ***status signals***, from the data path.
  - Many modifications can be made here.

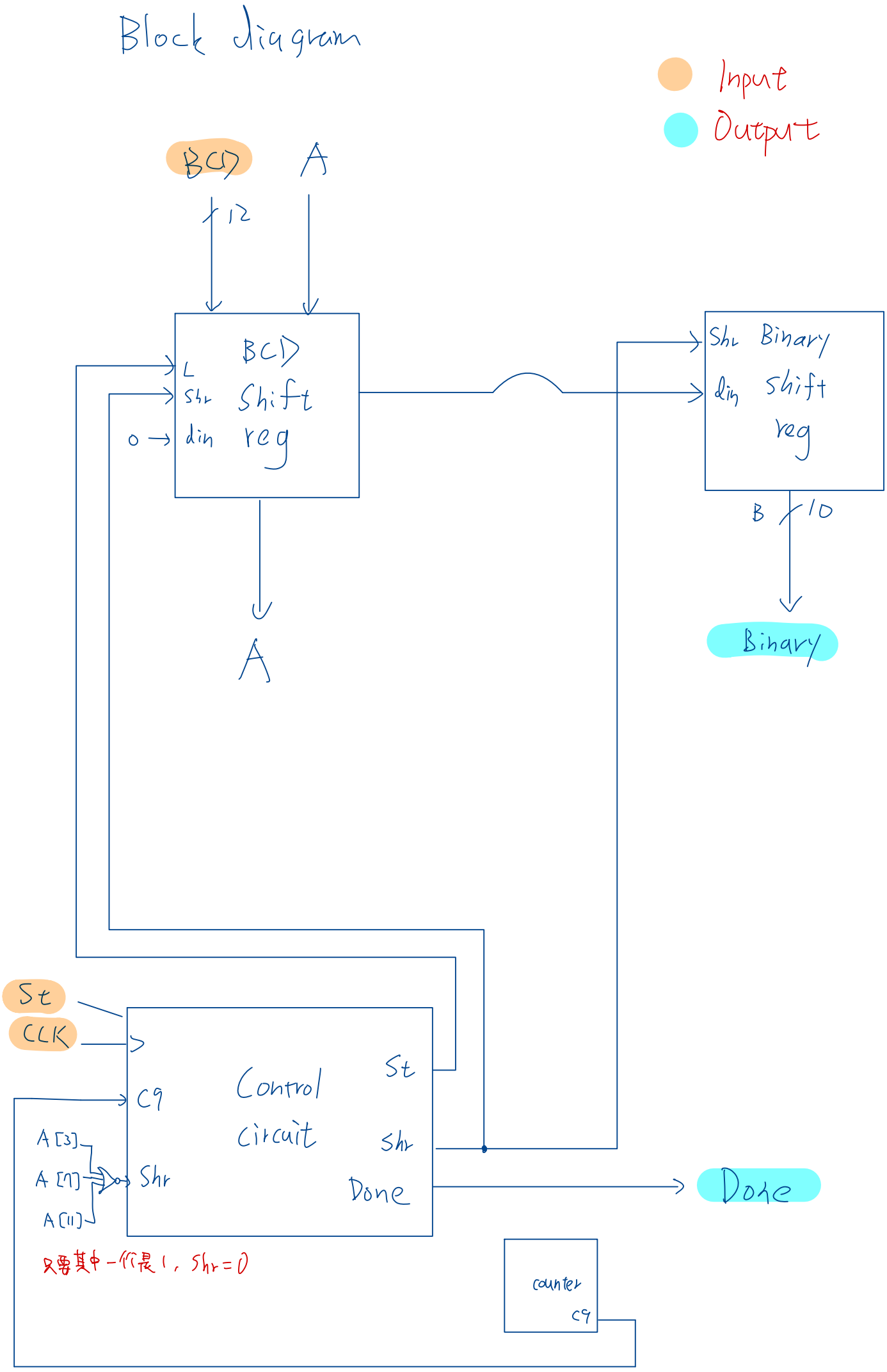
4-5

5



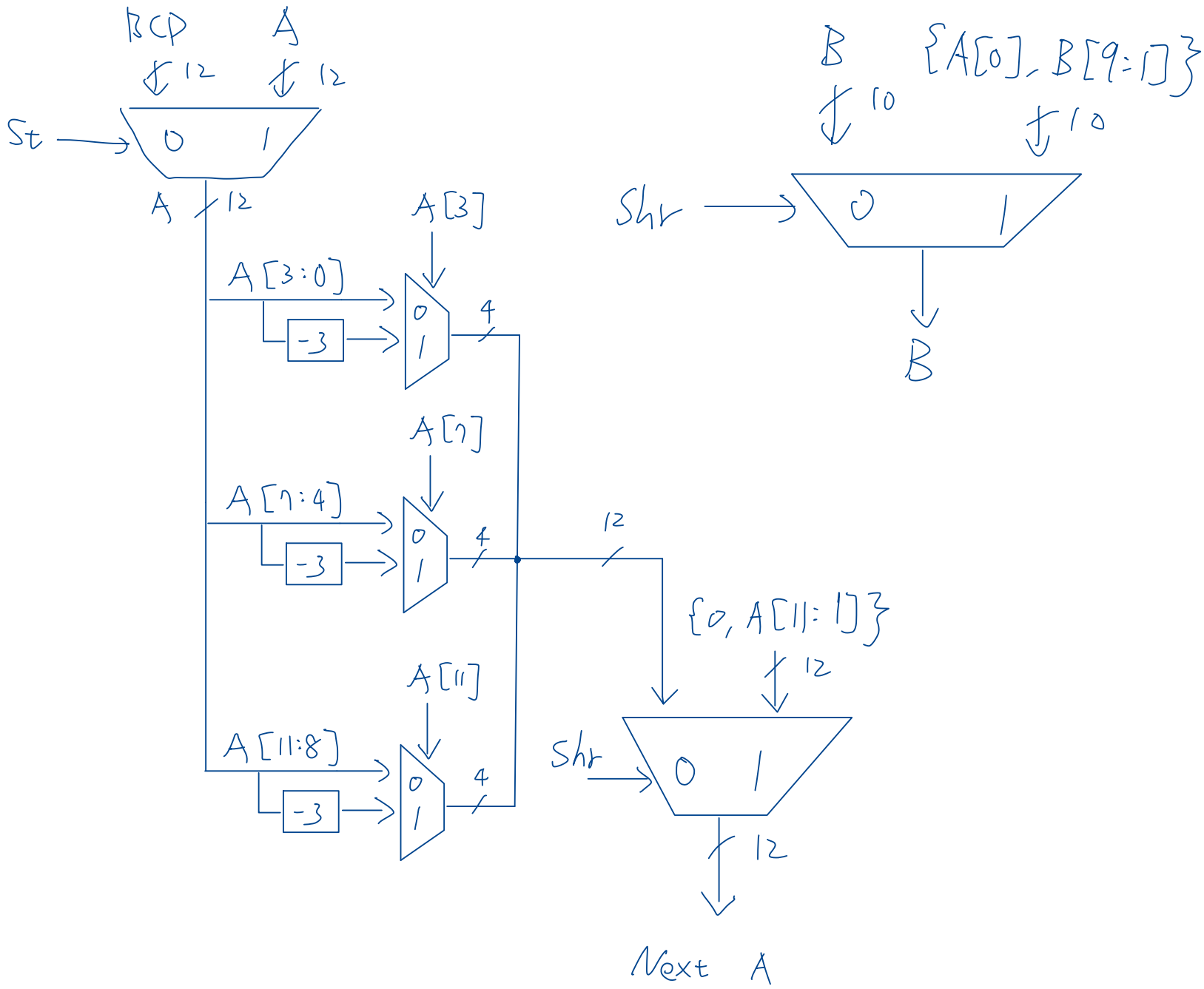
A	B	Do
1000	00000000	load A, B=0
0101		
0111		
0100	10000000	Shr
1000		Cor
0010	01000000	Shr
0001		
0000	00100000	Shr
+1010		Cor
0111		
0011	10010000	Shr
+1000		Cor
0101		
0010	11001000	Shr
+1001		Cor
0110		
0011	01100100	Shr
0000		
+1001	10110010	Shr
0110		Cor
0011	01011001	Shr
0001	10101100	Shr
0000	11010110	Shr

Block diagram

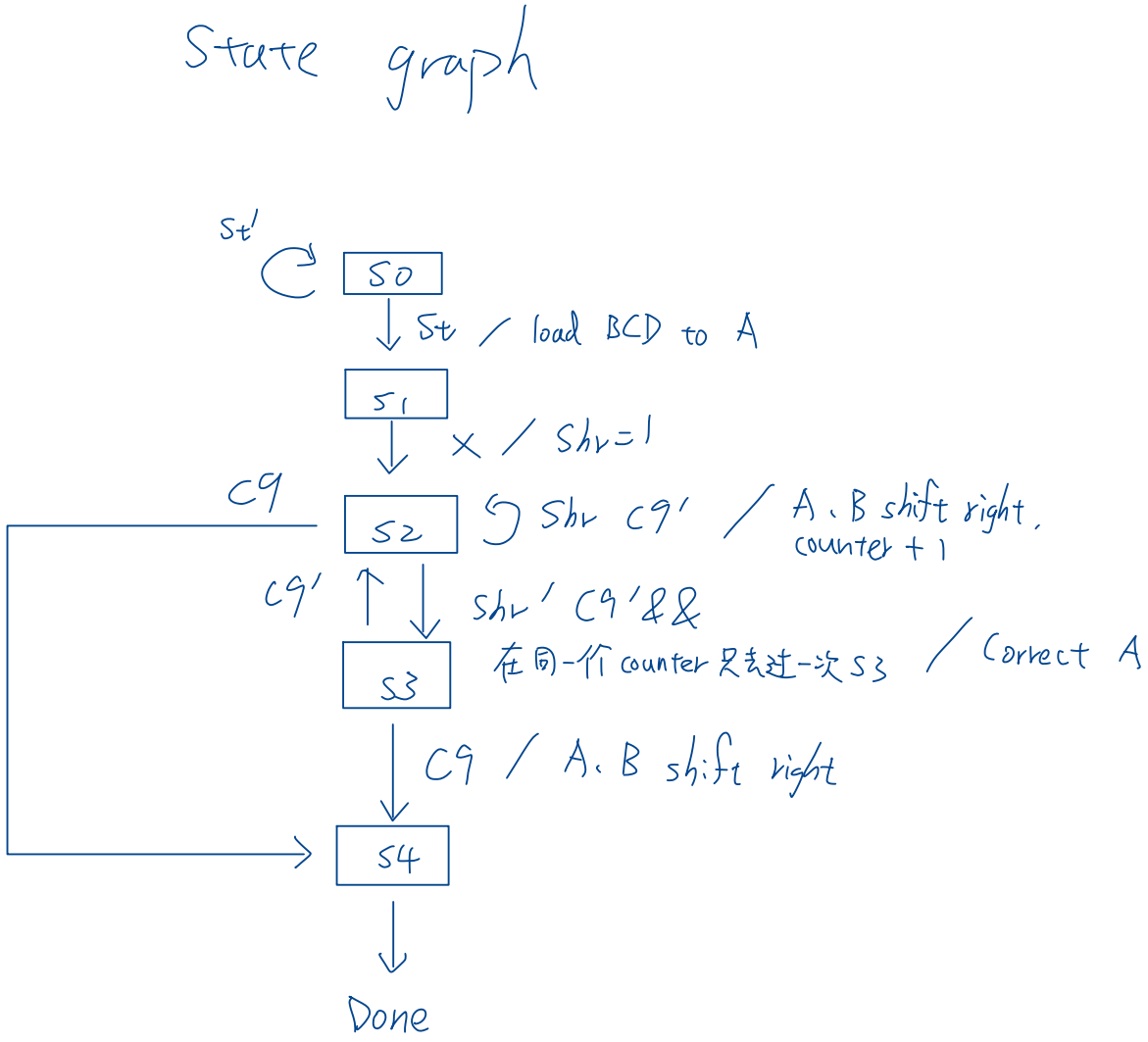


BCD shift reg

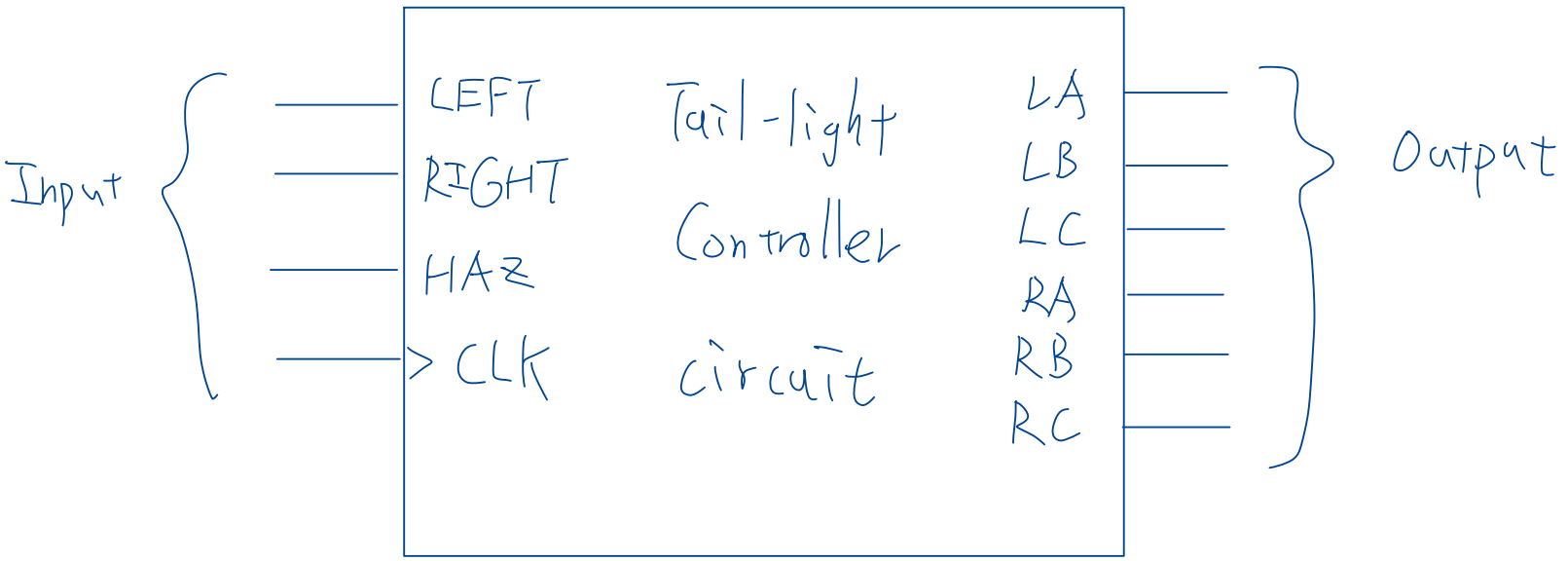
Binary shift reg

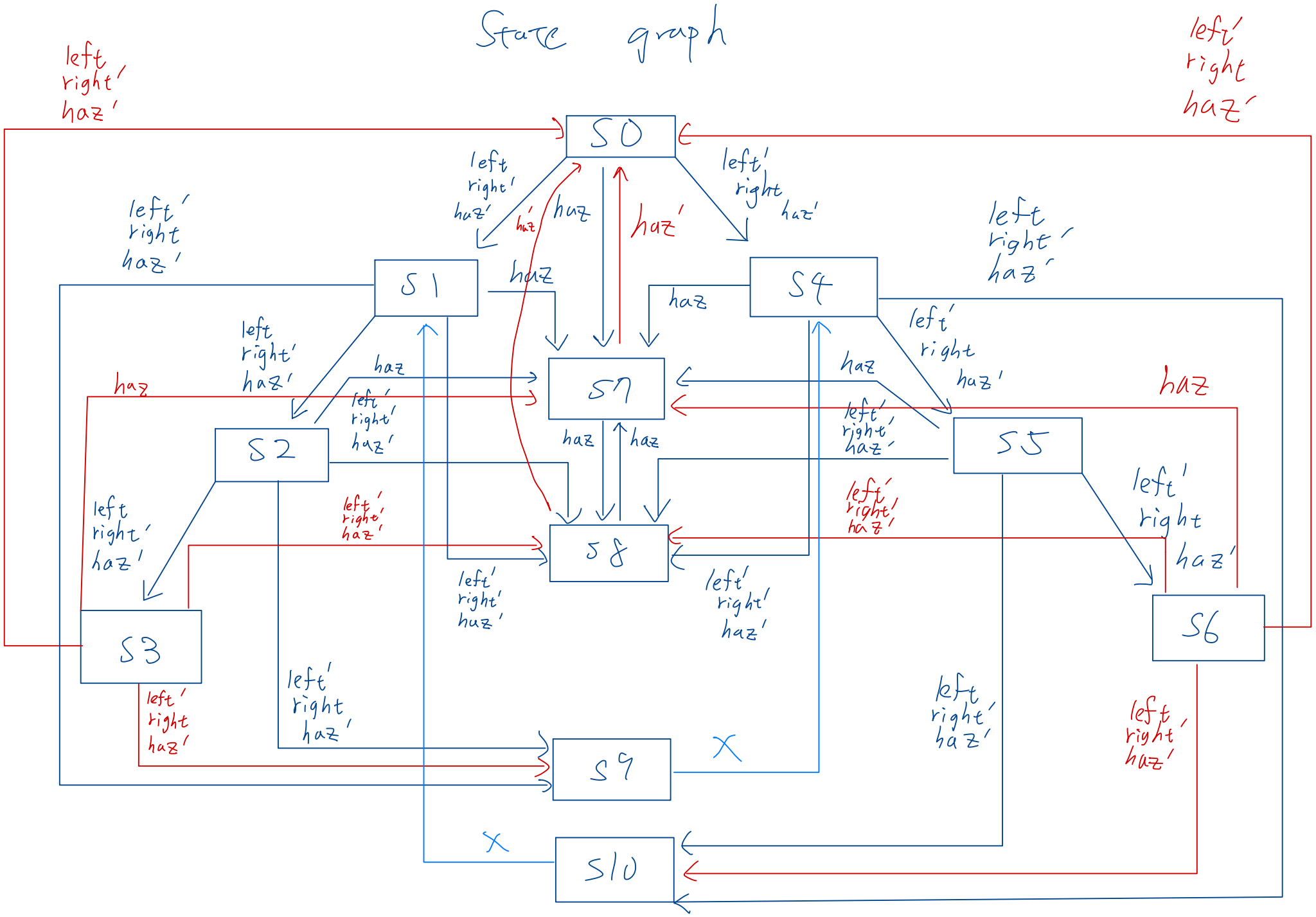


State graph


St'
S0
St / load BCD to A
S1
x / Shr=1
C9
S2
Shr C9' / A、B shift right, counter + 1
C9'
Shr' C9'&&
S3
在同一个 counter 只走过一次 S3 / Correct A
C9 / A、B shift right
S4
Done

Block diagram




State graph
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
left' right' haz'
haz
X