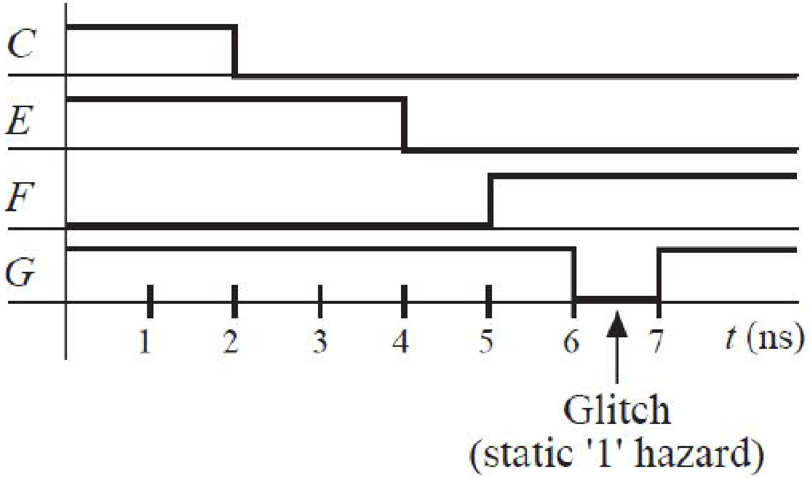
8.3 (a)



8.3 (b) Modified circuit (to avoid hazards)

CD \ AB	00	01	11	10
00				
01	1	1		
11		1	1	
10		1	1	

G = A'C'D + B C + A'BD

8.4 $A = 1; B = \mathsf{Z}; C = 1 \cdot \mathsf{Z} = \mathsf{X}; D = 1 + \mathsf{Z} = 1;$
$E = \mathsf{X}' = \mathsf{X}; F = 1' = 0; G = \mathsf{X} \cdot 0 = 0;$
$H = \mathsf{X} + 0 = \mathsf{X}$

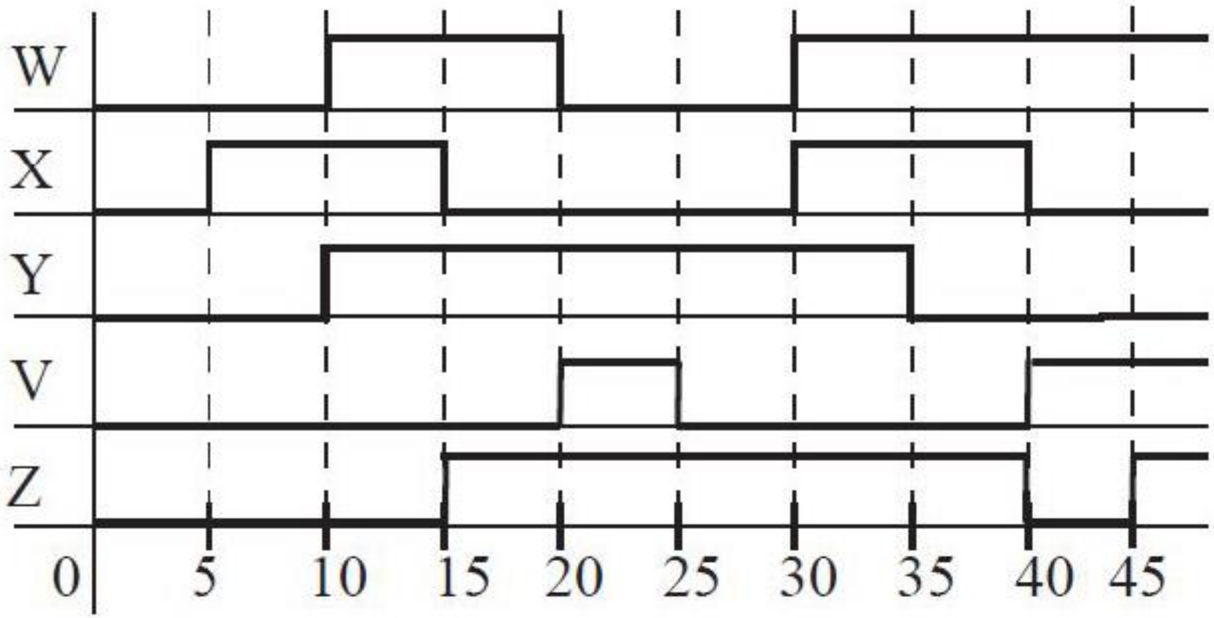
See FLD Table 8-1, p. 241.

8.5 $A = B = 0, C = D = 1$

So $F = AB'D + BC'D' + BCD = 0$

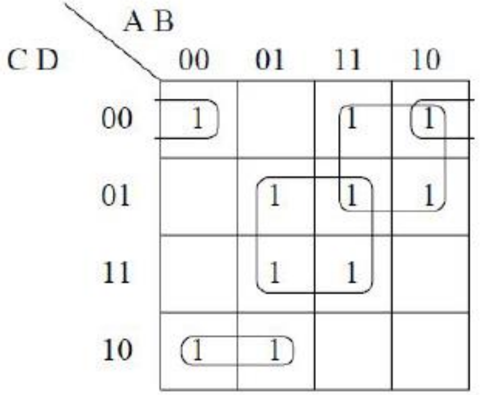
But in the figure, gate 4 outputs F = 1, indicating something is wrong. For the last NAND gate, F = 0 only when all its inputs are 1. But the output of gate 3 is 0. Therefore, gate 4 is working properly, but gate 3 is connected incorrectly or is malfunctioning.

8.10

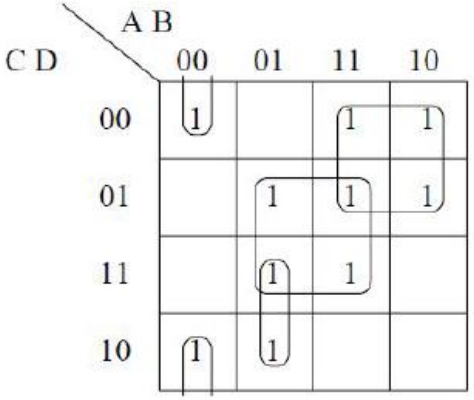


8.16 (a) $F(A, B, C, D) = \sum m(0, 2, 5, 6, 7, 8, 9, 12, 13, 15)$

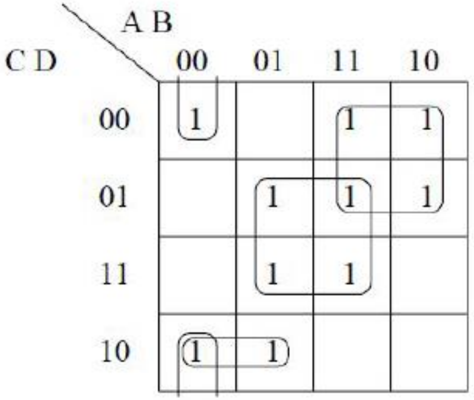
There are 3 different minimum AND-OR solutions to this problem. The problem asks for any two of these.



F = B D + A C' + A'C D' + B'C'D'



F = B D + A C' + A'B'D' + A'B C



F = B D + A C' + A'B'D' + A'C D'

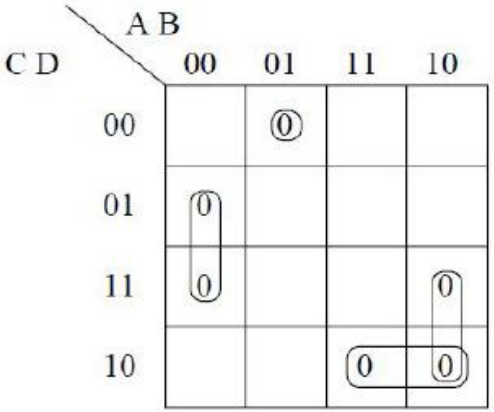
Solution 1: 1-hazards are between 0000↔0010 and 0111↔0110

Solution 2: 1-hazards are between 0010↔0110 and 0000↔1000

Solution 3: 1-hazards are between 0111↔0110 and 0000↔1000

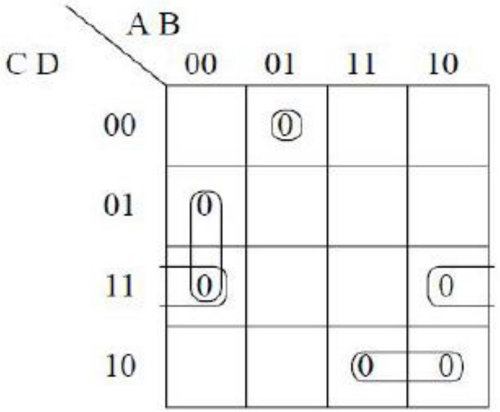
Without hazards: $F^t = BD + AC' + B'C'D' + A'CD' + A'B'D' + A'BC$

8.16 (b)



$F = (A + B + D')\,(A + B' + C + D)\,(A' + C' + D)$
$\quad (A' + B + C')$

0-hazard is between 1011↔0011



$F = (A + B + D')\,(A + B' + C + D)\,(A' + C' + D)$
$\quad (B + C' + D')$

0-hazard is between 1011↔1010

Either way, without hazard:

$F^t = (A + B + D')\,(A + B' + C + D)\,(A' + C' + D)$
$(B + C' + D')\,(A' + B + C')$

8.A

$ABCD$	X_1	X_2	X_3	X_4	X_5	X_6	X_7
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	0	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	0	0	1	1

$X_1 = B'D' + B\,D + A + C\,D = \underline{B'D'} + \underline{BC'D} + A + \underline{CD}$ (used in circuit)

$X_1 = B'D' + B\,D + A + B'C$

$X_2 = B' + \underline{C'D'} + \underline{C\,D}$

$X_3 = C' + D + B$

$X_4 = \underline{B'D'} + \underline{B'C} + \underline{B\,C'D} + \underline{C\,D'}$

$X_5 = \underline{B'D'} + \underline{C\,D'}$

$X_6 = \underline{C'D'} + \underline{B\,C'} + B\,D' + A$

$X_7 = \underline{B'C} + \underline{B\,C'} + A + \underline{C\,D'}$ (used in circuit)

$X_7 = B'C + B\,C' + A + B\,D'$

This solution uses 15 gates and 41 gate inputs.

Students are allowed to use a <u>maximum</u> of 18 gates.