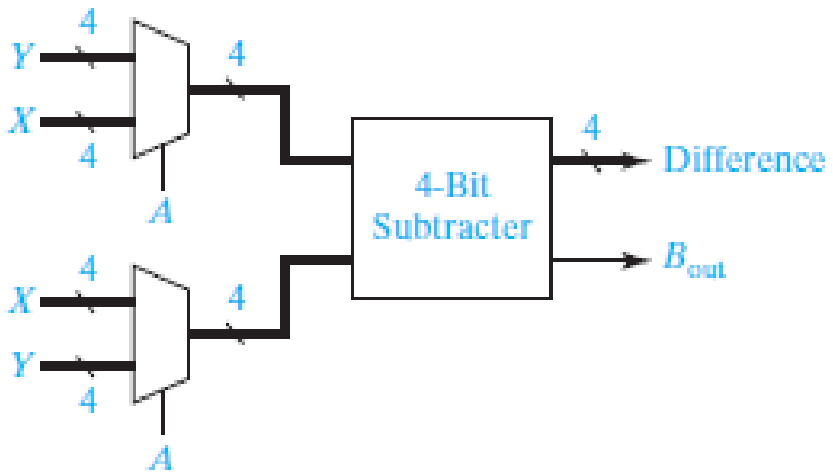
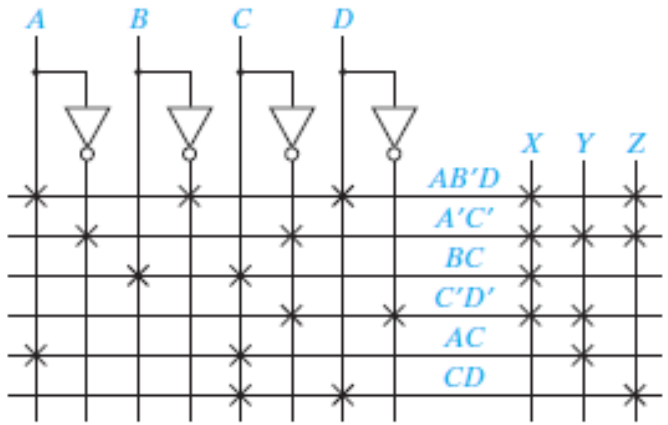
9.2



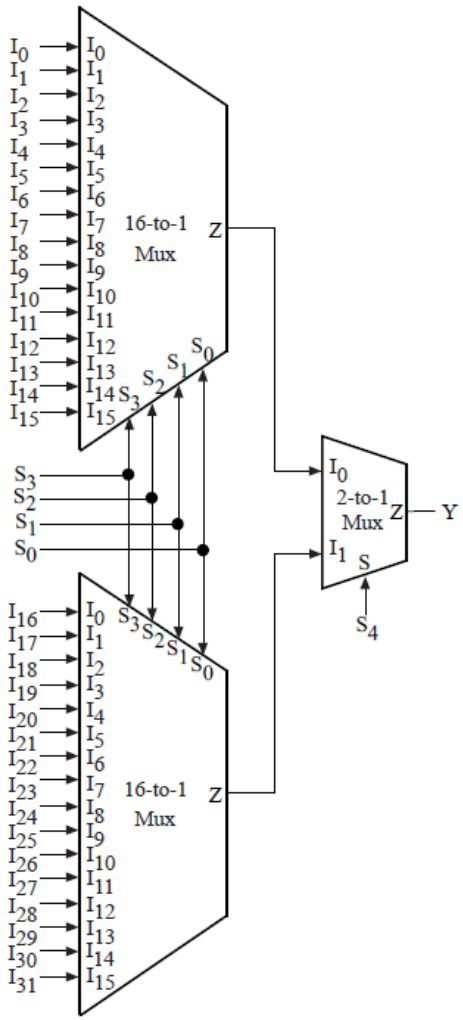
9.8 (a)



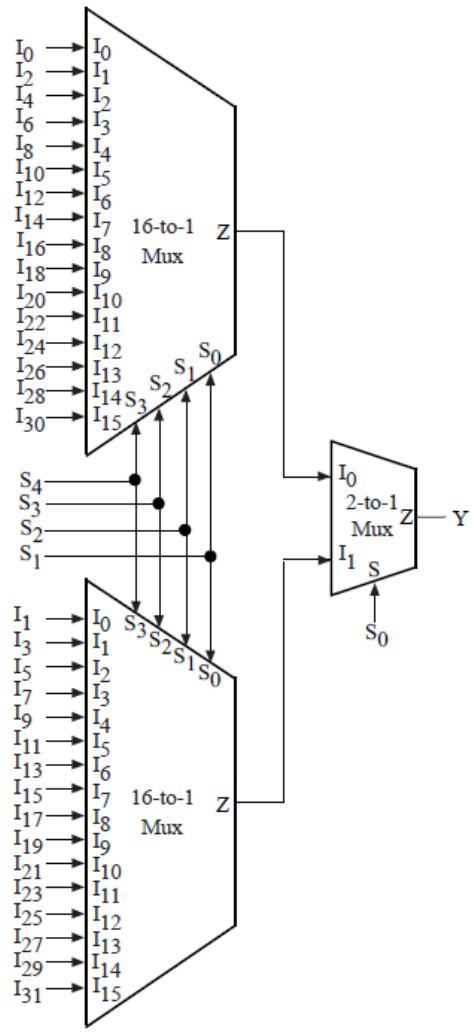
(b) Truth Table for the ROM

A	B	C	D	X	Y	Z
0	0	0	0	1	1	1
0	0	0	1	1	1	1
0	0	1	0	0	0	0
0	0	1	1	0	0	1
0	1	0	0	1	1	1
0	1	0	1	1	1	1
0	1	1	0	1	0	0
0	1	1	1	1	0	1
1	0	0	0	1	1	0
1	0	0	1	1	0	1
1	0	1	0	0	1	0
1	0	1	1	1	1	1
1	1	0	0	1	1	0
1	1	0	1	0	0	0
1	1	1	0	1	1	0
1	1	1	1	1	1	1

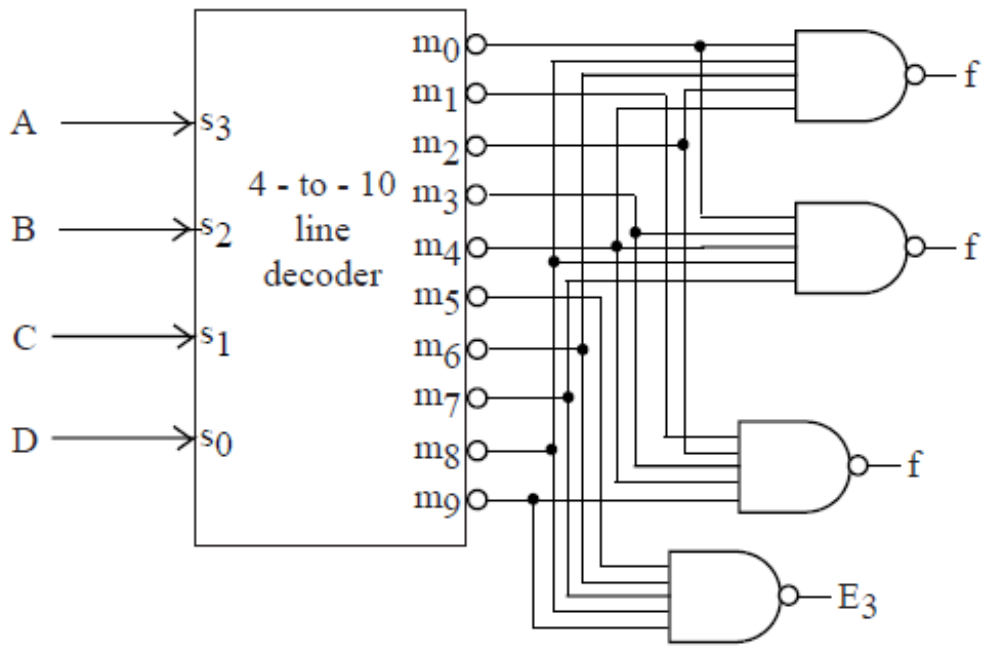
9.16


I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14 I15
16-to-1 Mux
Z
S3 S2 S1 S0
I16 I17 I18 I19 I20 I21 I22 I23 I24 I25 I26 I27 I28 I29 I30 I31
16-to-1 Mux
Z
I0 I1
2-to-1 Mux
Z
Y
S
S4

9.16 cont.

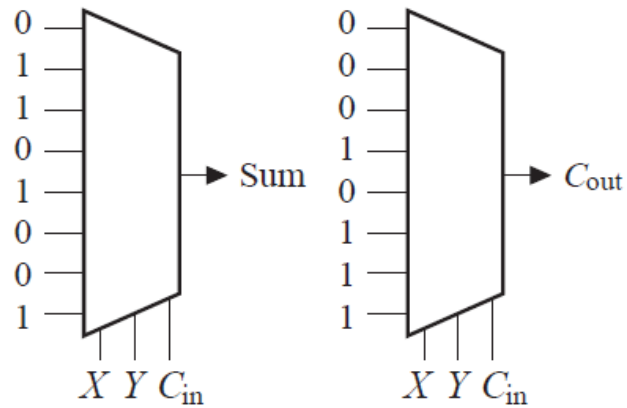

I0 I2 I4 I6 I8 I10 I12 I14 I16 I18 I20 I22 I24 I26 I28 I30
16-to-1 Mux
Z
S4 S3 S2 S1
I1 I3 I5 I7 I9 I11 I13 I15 I17 I19 I21 I23 I25 I27 I29 I31
16-to-1 Mux
Z
I0 I1
2-to-1 Mux
Z
Y
S
S0

9.18 Since the decoder outputs are negative, NAND gates are required. The excess-3 outputs are Σ m(5,6,7,8,9), Σ m(1,2,3,4,9), Σ m(0,3,4,7,8), and Σ m(0,2,4,6,8) so four 5-input NAND gates are needed with inputs corresponding to the minterms of the excess-3 outputs.

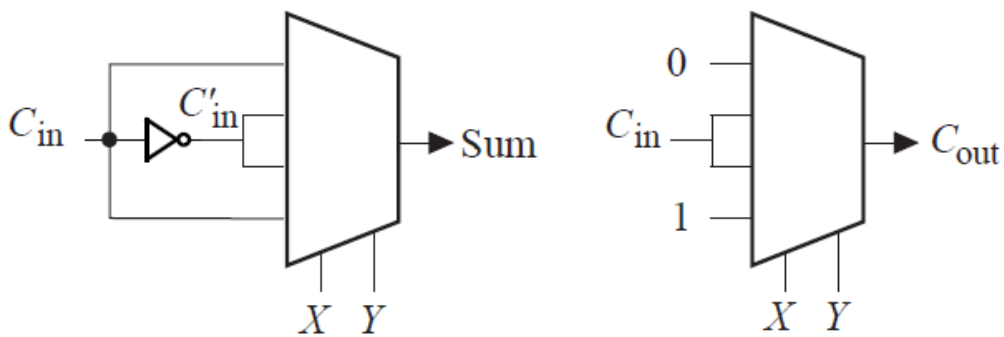


9.21 (a)

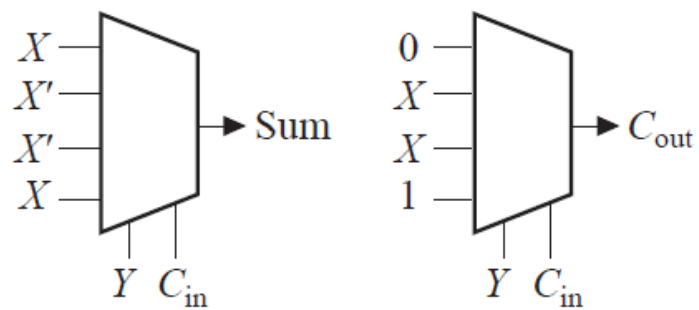
$x\ y\ c_{in}$	$Sum\ C_{out}$
0 0 0	0 0
0 0 1	1 0
0 1 0	1 0
0 1 1	0 1
1 0 0	1 0
1 0 1	0 1
1 1 0	0 1
1 1 1	1 1



9.21 (b)

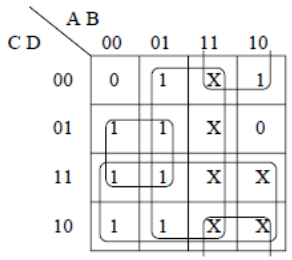


9.21(c)

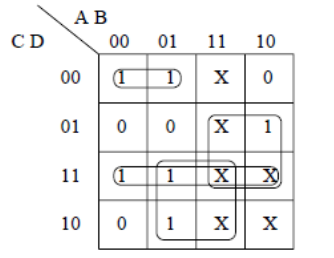


9.32 (a)

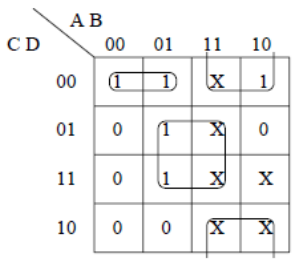
A B C D	W X Y Z
0 0 0 0	0 1 1 1
0 0 0 1	1 0 0 0
0 0 1 0	1 0 0 1
0 0 1 1	1 1 0 0
0 1 0 0	1 1 1 0
0 1 0 1	1 0 1 0
0 1 1 0	1 1 0 1
0 1 1 1	1 1 1 1
1 0 0 0	1 0 1 1
1 0 0 1	0 1 0 1



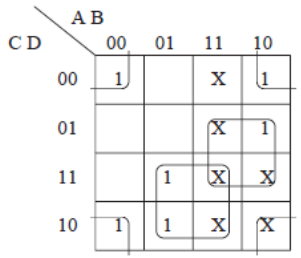
$W = A'D + C + B + \underline{AD'}$



$X = \underline{\underline{A'C'D'}} + C\,D + \underline{A\,D} + \underline{\underline{B\,C}}$

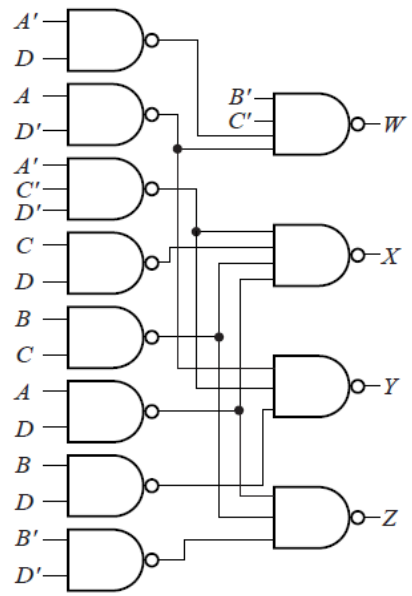


$Y = \underline{A\,D'} + B\,D + \underline{\underline{A'C'D'}}$



$Z = \underline{A\,D} + \underline{\underline{B\,C}} + B'D'$

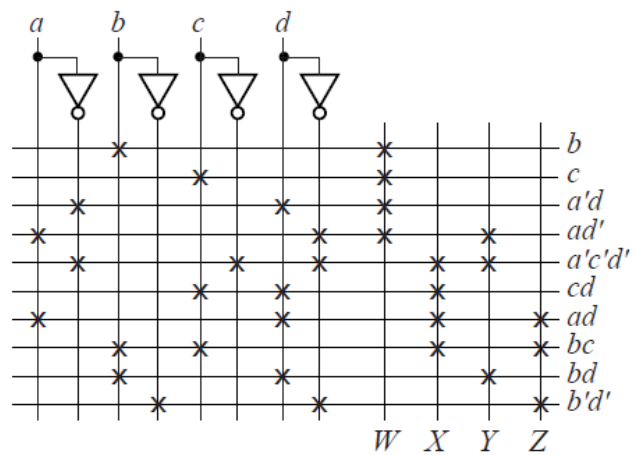
Alt: $Z = A + \underline{\underline{B\,C}} + B'D'$



9.32 (b)

a b c d	W X Y Z
- 1 - -	1 0 0 0
- - 1 -	1 0 0 0
0 - - 1	1 0 0 0
1 - - 0	1 0 1 0
0 - 0 0	0 1 1 0
- - 1 1	0 1 0 0
1 - - 1	0 1 0 1
- 1 1 -	0 1 0 1
- 1 - 1	0 0 1 0
- 0 - 0	0 0 0 1

9.32 (c)



9.46 (a) The decoder outputs are $Y_0 = A'B'$, $Y_1 = A'B$, $Y_2 = AB'$, $Y_3 = AB$. The mux outputs are $f = I_0'C'D' + I_1'C'D + I_2'CD' + I_3'CD$. So

$$\begin{aligned} f(A,B,C,D) &= Y_0'C'D' + Y_1'C'D + Y_2'CD' + Y_3'CD \\ &= (A + B)C'D' + (A + B')C'D + (A' + B)CD' \\ &\quad + (A' + B')CD \\ &= AC'D' + BC'D' + AC'D + B'C'D + A'CD' \\ &\quad + BCD' + A'CD + B'CD \\ &= AC' + BD' + B'D + A'C. \end{aligned}$$

9.46 (b) The decoder outputs are minterms of A and B active low: $Y_0 = A'B'$, $Y_1 = A'B$, $Y_2 = AB'$, $Y_3 = AB$. The mux output is selected by select inputs S1 = C and S0 = D: $f = I_0'C'D' + I_1'C'D + I_2'CD' + I_3'CD$ and the mux inputs are $I_0 = Y_0'$, $I_1 = Y_1'$, $I_2 = Y_2'$ and $I_3 = Y_3'$. So $f(A,B,C,D)$

$$\begin{aligned} &= Y_0'C'D' + Y_1'C'D + Y_2'CD' + Y_3'CD \\ &= A'B'C'D' + A'BC'D + AB'CD' + ABCD. \end{aligned}$$

This can be made easier by moving the inversion on the output of the mux to all inputs of the mux, and noticing that the two inversions in series between the decoder and mux cancel.