mid2

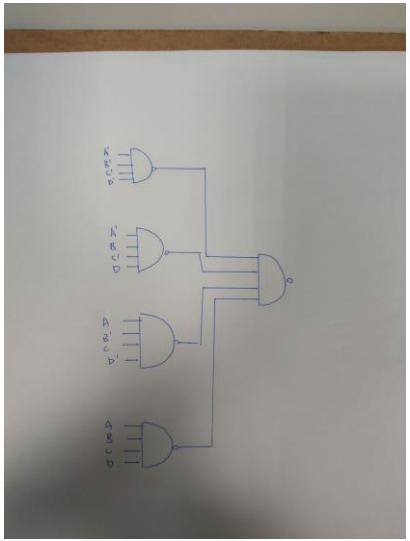
1.

(a) F = A’B’C’D’+ A’BC’D+ AB’CD’+ ABCD

= ((A’B’C’D’)’ (A’BC’D)’ (AB’CD’)’ (ABCD)’)’

CD \ AB	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1



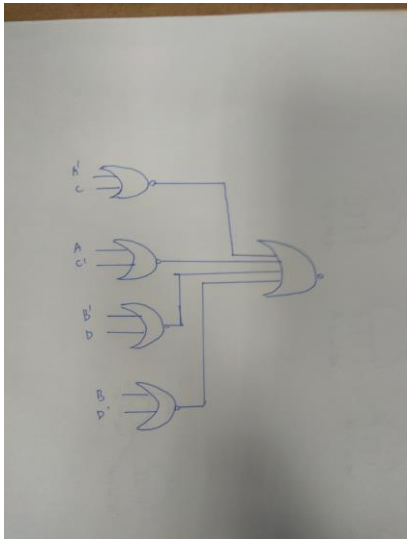
1.

(b) F = (A'+C)(A+C')(B'+D)(B+D')

=((A'+C)' + (A+C')' + (B'+D)' + (B+D')')'

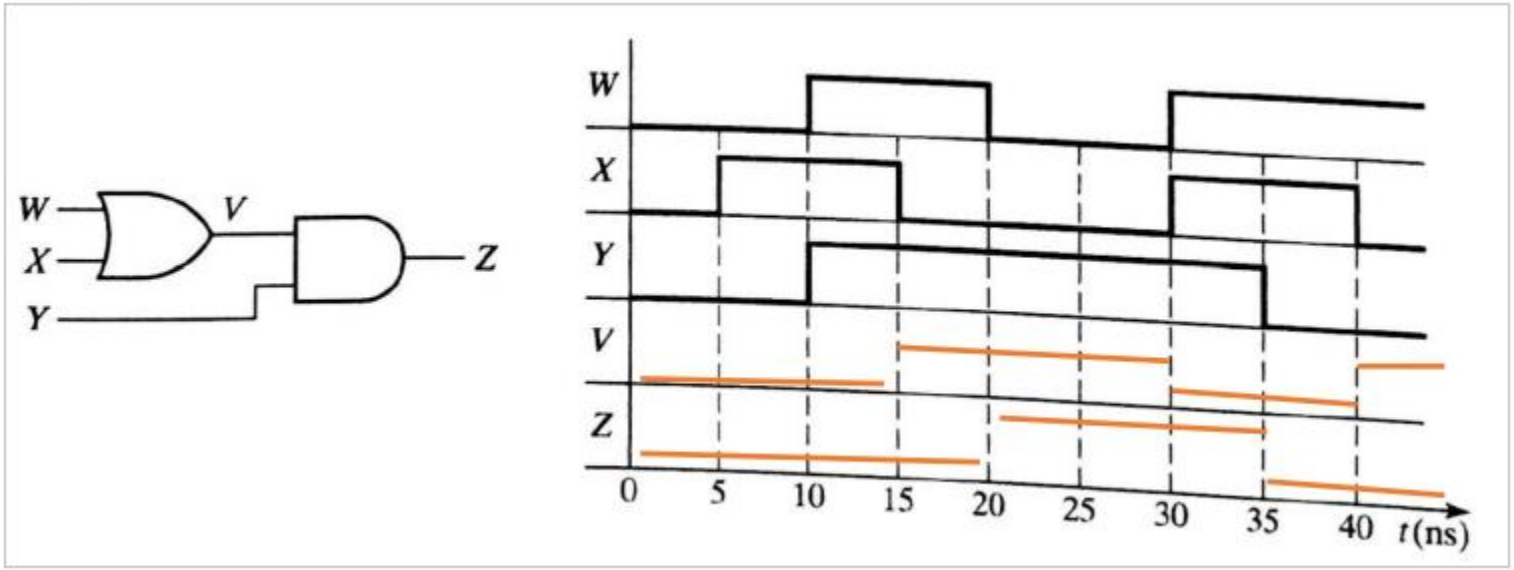
AB / CD	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1

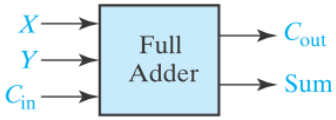


2.

2. Sol:

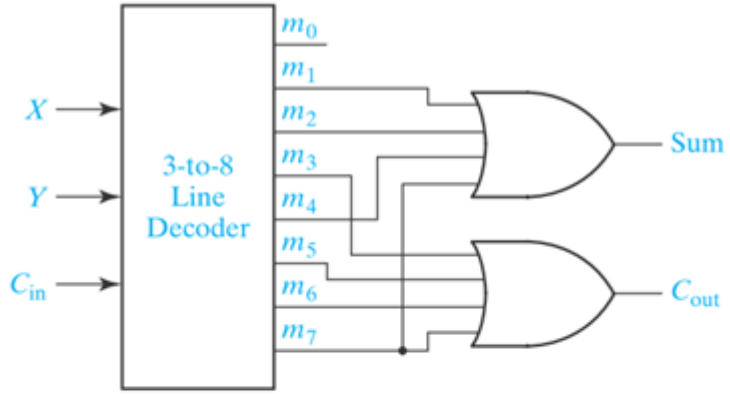


3.

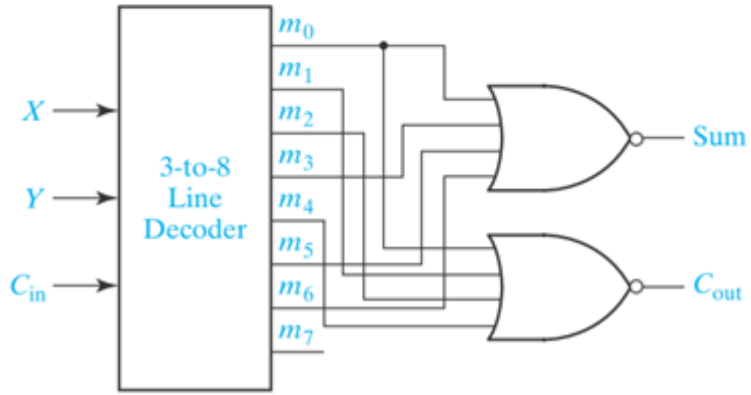


X	Y	C_{in}	C_{out}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a)



(b)



4.

4.

A	B	C	D	G	Y_1	Y_0	Z_3	Z_2	Z_1	Z_0
I_3	I_2	I_1	I_0							
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0	1
0	0	1	–	1	0	1	0	0	1	0
0	1	–	–	1	1	0	0	1	0	0
1	–	–	–	1	1	1	1	0	0	0

$\Rightarrow Z_3 = A$

$Z_2 = A'B$

$Z_1 = A'B'C$

$Z_0 = A'B'C'D$

5.

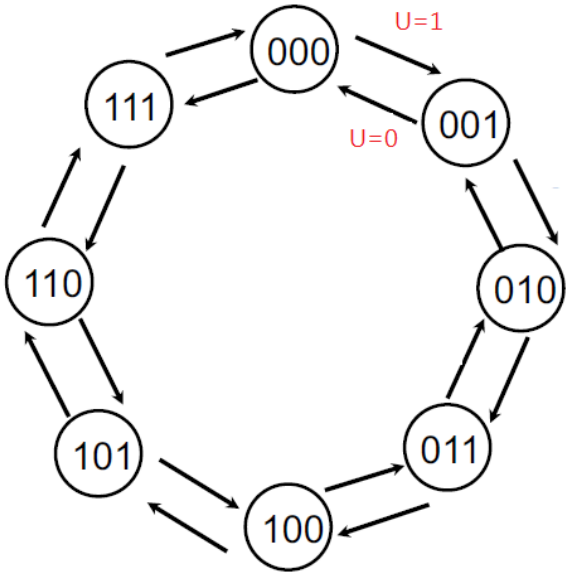
write the Verilog code

```
module HA(a, b, sum, c_out);
input wire a, b;
output wire sum, c_out;
xor (sum, a, b);
and (c_out, a, b);
endmodule

module FA(a, b, c_in, sum, c_out);
input   a, b, c_in;
output  sum, c_out;
wire   w1, w2, w3;
HA M1(.a(a), .b(b), .sum(w1), .c_out(w2));
HA M2(.a(w1), .b(c_in), .sum(sum), .c_out(w3));
or (c_out, w2, w3);
endmodule
```

6.

2分



2分

$Q_2Q_1Q_0$	$Q_2^+Q_1^+Q_0^+$	
	U=1	U=0
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

6.

- U=1

  $D_{Q0}= Q_0^+=Q_0'$ 1分

  $D_{Q1}= Q_1^+=Q_1Q_0' + Q_1'Q_0=Q_1 \oplus Q_0$ 1分

  $D_{Q2}= Q_2^+=Q_2'Q_1Q_0+ Q_2Q_1'+Q_2Q_0'= Q_2'Q_1Q_0+Q_2(Q_1Q_0)'=Q_2 \oplus Q_1Q_0$ 1分

- U=0

  $D_{Q0}= Q_0^+=Q_0'$ 1分

  $D_{Q1}= Q_1^+=Q_1Q_0+Q_1'Q_0'= Q_1 \oplus Q_0'$ 1分

  $D_{Q2}= Q_2^+=Q_2'Q_1'Q_0'+Q_2Q_1+Q_2Q_0=Q_2'Q_1'Q_0'+Q_2 (Q_1'Q_0')'= Q_2 \oplus Q_1'Q_0'$ 1分

6.

$D_{Q0}=Q_0^+=Q_0 \oplus U=Q_0'$ 2分

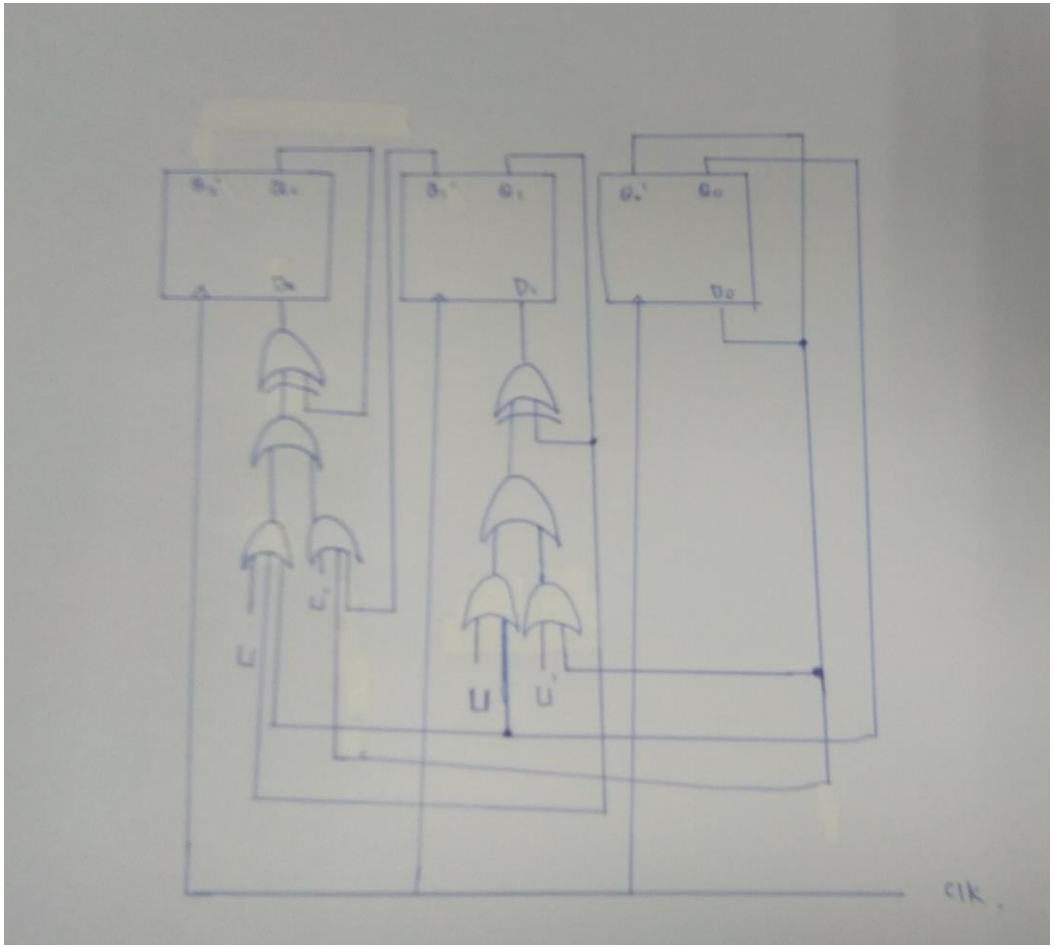
$D_{Q1}=Q_1^+=Q_1 \oplus (UQ_0+ U'Q_0')=UQ_1'Q_0+U'Q_1Q_0+UQ_1Q_0'+U'Q_1'Q_0'$ 2分

$D_{Q2}=Q_2^+=Q_2 \oplus (UQ_1Q_0+U'Q_1'Q_0')$

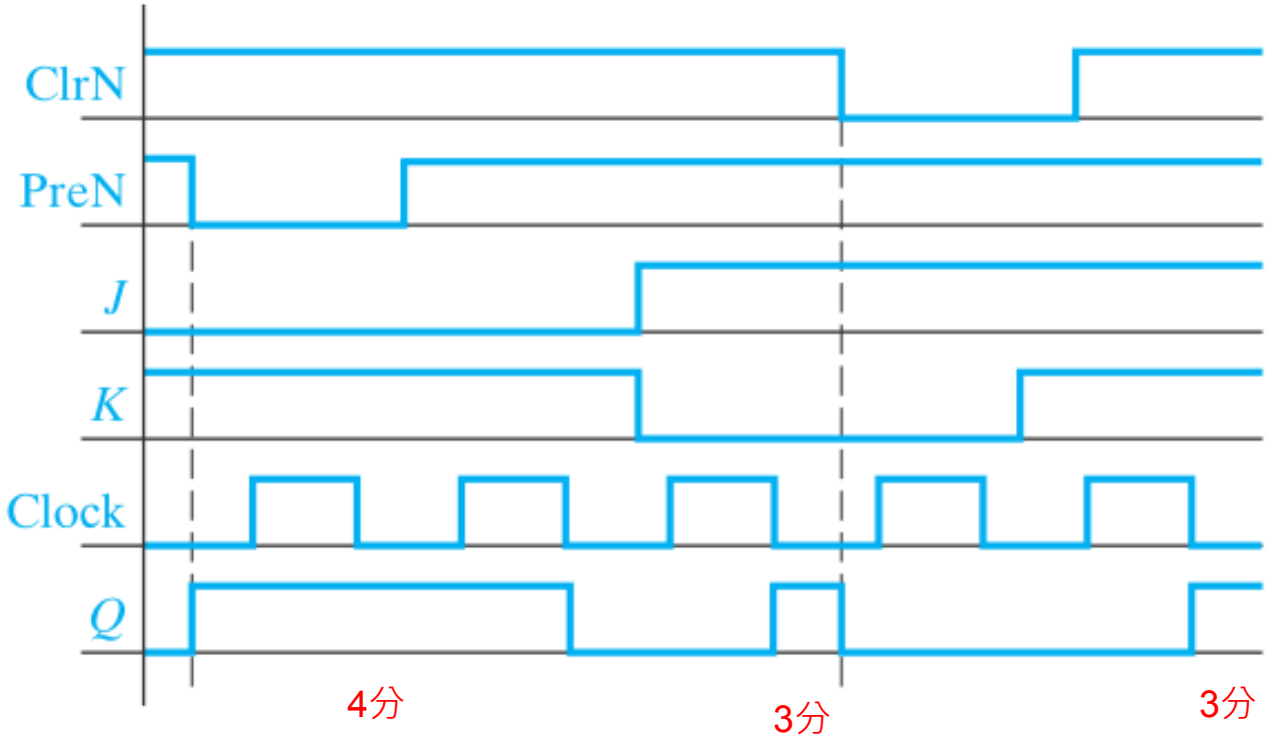
$=U'Q_2Q_1Q_0+U'Q_2'Q_1'Q_0'+UQ_2Q_1'Q_0'+UQ_2'Q_1Q_0+Q_2Q_1'Q_0+Q_2Q_1Q_0$‘

$=UQ_2Q_1'+U'Q_2Q_0+Q_2Q_1Q_0'+UQ_2'Q_1Q_0+U'Q_2'Q_1'Q_0'$ 2分

6.

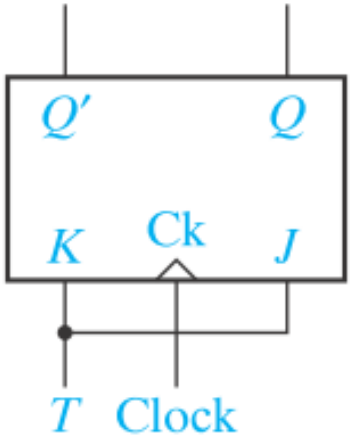


7.



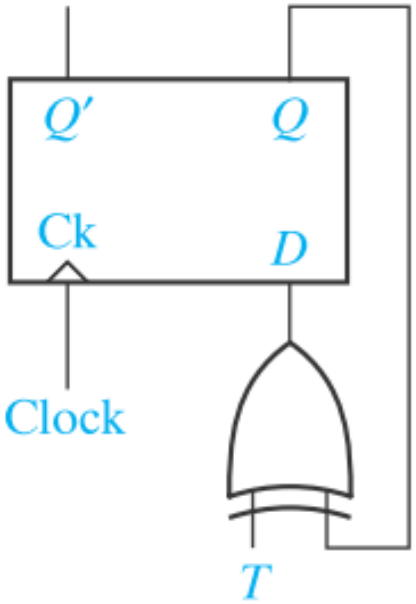
8.

5分



(a) Conversion of J-K to T

5分



(b) Conversion of D to T

9.

沒用gate_level 扣3分

```
input [3:0]  bcd;
output [3:0] ex3;
wire cd,c_d_0,c_d,b_0;
wire temp1,temp2,temp3;
```

1分
1分
1分

```
not n1(ex3[0],bcd[0]);//(1)
and a1(cd,bcd[1],bcd[0]);//(2)
or  o1(c_d,bcd[1],bcd[0]);//(3)
not n3(b_0,bcd[2]);//(4)
not n2(c_d_0,c_d);//(5)
or  o2(ex3[1],cd,c_d_0);//(6)
and a2(temp1,bcd[2],c_d_0);//(7)
and a3(temp2,b_0,c_d);//(8)
and a4(temp3,bcd[2],c_d);//(9)
or  o3(ex3[2],temp1,temp2);//(10)
or  o4(ex3[3],temp3,bcd[3]);//(11)
```

6分(一個0.5)
1分(標1-11gate)

10.

```
reg [3:0] t_bcd;
wire [3:0] t_ex3;
integer i;

BCD_to_EX3 bcdex3(.bcd(t_bcd), .ex3(t_ex3));
```

1分 1分 1分

Excess-3				BCD			
w	x	y	z	A	B	C	D
0	0	0	0	X	X	X	X
0	0	0	1	X	X	X	X
0	0	1	0	X	X	X	X
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

```
initial
begin
    i=0;
    t_bcd = 4'd7;
    #0.1;
    t_bcd = 4'd9;
    #0.1;
    t_bcd = 4'd0;
    #0.3;
    t_bcd = 4'd2;
    #0.2;
    t_bcd = 4'd4;
    #0.2;
    t_bcd = 4'd6;
    #0.2;
    t_bcd = 4'd8;
    #0.3;
    t_bcd = 4'd3;
    #0.1;

    $finish;
end
```

```
initial
begin
    i=0;
    t_bcd = 4'd7;
    #0.1;
    t_bcd = 4'd9;
    #0.1;
    t_bcd = 4'd0;
    #0.1;
    for(i=0; i<10; i=i+2)
    begin
      t_bcd = i;
      #0.2;
    end
    t_bcd = 4'd8;
    #0.1;
    t_bcd = 4'd3;
    #0.1;

    $finish;
end
```

1分

5分

1分