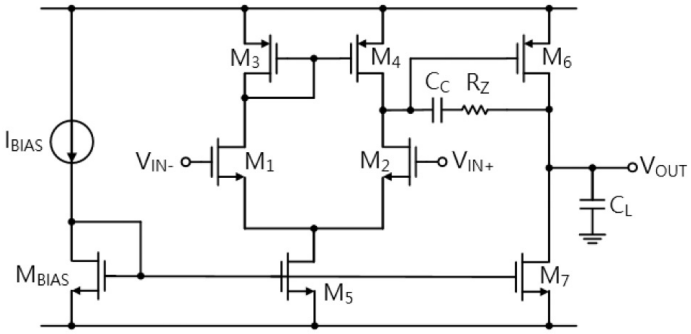
Two Stage Operational Amplifier Design

指導教授：廖育德教授　學生：陳子祈

Introduction

設計一個運算放大器在類比電路設計中非常重要。就二階運算放大器來說，有一個優點是：因為經過兩次放大電壓增益，在高增益放大電路的配置下，運算放大器能產生一個比輸入端電勢差大數十萬倍的輸出電勢。另外兩個優點是如果使用差極模式可消除共模雜訊、有很大的output voltage swing可使運算放大器有非常大的工作範圍。

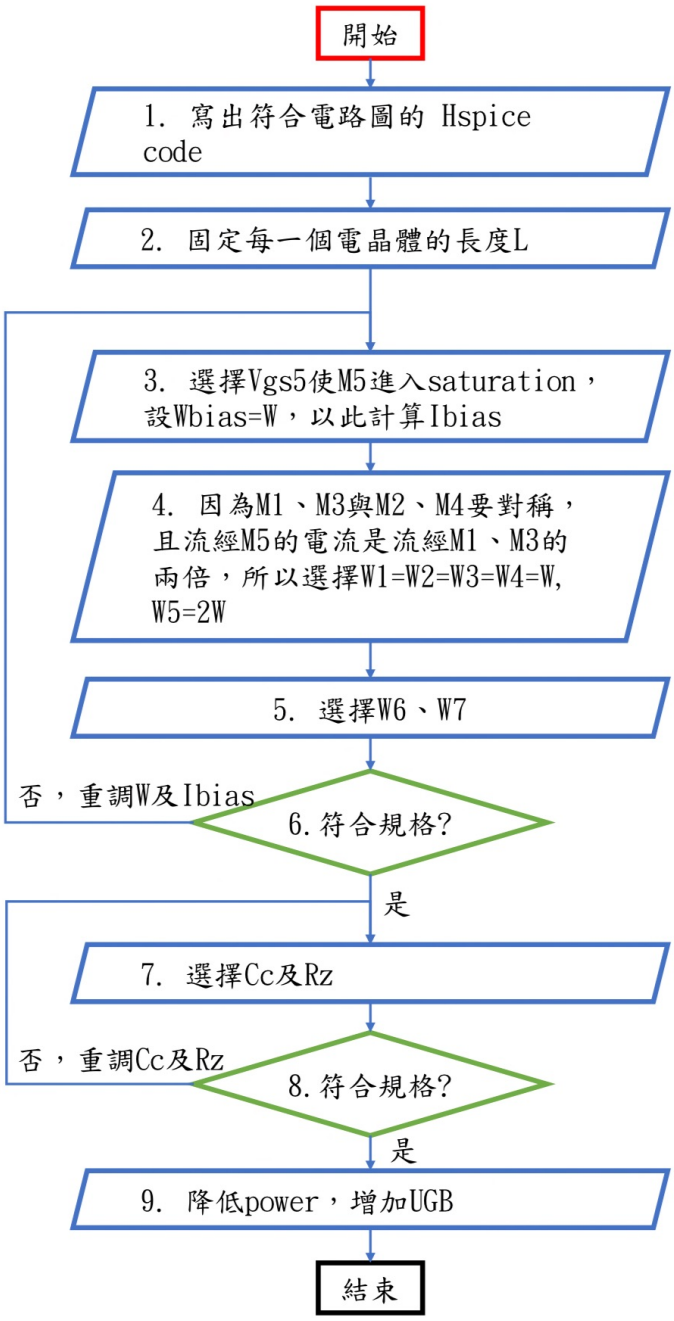
Circuit



Specification

	Specification
Supply voltage	<1.8V
Power (with biasing)	<20μW
CL	1pF
CC	<10pF
DC gain	>60dB
Unity-Gain BW	>5MHz
Phase margin	>60°
Slew-rate	>3V/μsec
Output swing	>1.2V_{pp}
PSRR	As large as possible
CMRR	As large as possible
FoM (2π*UGB/Power)	>8Mrad/μW

Design flow



Design flow 說明

◇ 關於第5點及第7點的選擇

調高M6、M7的width，讓電流變大、放電速度變快，slew rate才會提高，不過電流變大，power也會上升，所以M6、M7的width不要調太多，而且調高M6、M7的width之後讓phase margin變小，為了讓phase margin提高，調低Rz，但是phase margin提高會造成Unit-gain bandwidth變小，Fom也會變小，所以Rz不能調太多，我調到200k差不多剛好可以讓phase margin大於60度。

formula

- Slew rate: $SR = \frac{I_5}{C_c}$
- First-stage Gain: $A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$
- Second-stage Gain: $A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)}$
- Gain Bandwidth (GB): $GB = \frac{g_{m1}}{C_c}$
- Output Pole: $p_2 = \frac{-g_{m6}}{C_L}$
- RHP zero: $z_1 = \frac{g_{m6}}{C_c}$
- Positive CMR (Common-mode Range):

$$V_{in,\max} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T3}|(\max) + V_{T1}(\min)$$

- Negative CMR: $V_{in,\min} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max) + V_{DS5}(\text{sat})$
- Saturation Voltage: $V_{DS}(\text{sat}) = \sqrt{\frac{2I_{ds}}{\beta}}$

Result – final design value

	W	L	m	Region	I_D	gm
M1	1.2u	0.4u	1	Saturation	1.8709u	36.4900u
M2	1.2u	0.4u	1	Saturation	1.8709u	36.4900u
M3	1.2u	0.4u	1	Saturation	-1.8709u	23.3384u
M4	1.2u	0.4u	1	Saturation	-1.8709u	23.3384u
M5	2.4u	0.4u	1	Saturation	3.7417u	72.5703u
M6	2.4u	0.4u	1	Saturation	-4.2245u	51.2839u
M7	2.4u	0.4u	1	Saturation	4.2245u	80.3233u
M_{BIAS}	1.2u	0.4u	1	Saturation	599.999n	11.6345u
	Size					
C_C	0.1p					
R_Z	200k					

Performance

	Specification	Simulation Result
Supply voltage	<1.8V	1.8V
Power (with biasing)	<20μW	15.4193uW
CL	1pF	1pF
CC	<10pF	0.1pF
DC gain	>60dB	60.3dB
Unity-Gain BW	>5MHz	39.6725MHz
Phase margin	>60°	63.9226°
Slew-rate	>3V/μsec	3.81MV/sec
Output swing	>1.2V_{pp}	1.42V
PSRR	As large as possible	72dB
CMRR	As large as possible	63.63dB
FoM (2π*UGB/Power)	>8Mrad/μW	16.166 Mrad/μW

Result