Hanqing Zhu

Graduate Research Assistant - University of Texas at Austin
zhuhanqing.github.io hqzhu@utexas.edu (512) 200-6791

Research Interests

VLSI design automation, efficient and robust AI computing system with emerging technology, hardware-efficient machine learning.

Education

University of Texas at Austin(UT-Austin) **Austin, TX**
Ph.D., Dept. of Electrical and Computer Engineering *Sept. 2020 - Present*
Advisor: David Z. Pan
Co-advisor: Ray T. Chen
GPA: 3.95/4.00

Shanghai Jiao Tong University(SJTU) **Shanghai, China**
B.E., Dept. of Microelectronics Science and Technology *Sept. 2016 - Jun. 2020*
Overall GPA: 3.81/4.00 (Rank: 2^{nd}/57)

Research Experience

University of Texas at Austin **Austin, TX**
Graduate Research Assistant (UTDA Lab), advised by Prof. David Z. Pan *Sept. 2020 - Present*

- **VLSI Placement**
  - On-going project on understanding the optimality of SOTA placement algorithms.
- **Efficient and Robust AI Computing System with Photonics** [M2, C5, C4, C2, C1]
  - Proposed an synergistic aging-aware co-optimization framework for emerging photonic in-memory computing paradigm; achieved $> 40\times$ dynamic energy cost and $> 20\times$ write operations reduction of the novel PCM-based neurocomputing paradigm; significantly enhanced the lifetime of neurocomputing engine under the wearing out pressure.
  - Collaborated on efficient on-chip learning protocol, *L2ight*, for optical computing system; proposed a subspace learning procedure with multi-level sparsity to enable *in-situ* gradient evaluation and low computation cost; achieved 3-order-of-magnitude higher scalability and over $30\times$ better efficiency than previous optical on-chip training tools.
  - Collaborated on quantization-aware training scheme in the unitray manifold to enable robust optical neural networks; achieved better accuracy and robustness with limited control resolution and device-level variations.
- **Hardware-efficient Machine Learning** [C3]
  - Worked on memory-efficient neural network designs for emerging neurocomputing system via multi-level in-situ parameters generation; Achieved $10 \sim 20\times$ memory efficiency with comparable accuracy with SOTA designs.
- **Photonics Neural Chip Tape-out** [M1]
  - Worked on photonic neural chip tape-out for novel ONN architectures using Advanced Micro Foundry (AMF); collaborated on the full-stack schematic design, layout, validation, tape-out, and measurement of photonic neural chips using PyTorch, Lumerical toolkits, and Synopsys optodesigner.

Shanghai Jiao Tong University **Shanghai, China**
Undergraduate Research Assistant, advised by Prof. Guanghui He *Sept. 2019 - Aug. 2020*

- **Design Space Exploration for FPGA-based Electromagnetic Transient Simulation System Auto-Builder**
  - Proposed an automatic design space exploration methodology to search for the optimal design parameters to automatically build FPGA-based electromagnetic transient smulation system.
  - Established a coarse-grained resource usage and delay estimation model based on extracted parameters to represent hardware structure with 2.0% and 5.1% estimation error on LUT and DSP usage.
  - Designed a Box-based local Pareto filtering algorithm to automate the parameters selection from the large design space of the multi-objective optimization problem.

Honors and Awards

A. Richard Newton Young Student Fellow	DAC	2021
Shanghai Outstanding Graduate	Shanghai City	2020
Department Excellent Undergraduate Thesis	Shanghai Jiao Tong University	2020
Hongyi Scholarship	Shanghai Jiao Tong University	2019
Outstanding Undergraduate Scholarship	Shanghai Jiao Tong University	2019
Samsung Scholarship	Shanghai Jiao Tong University	2018
Zhiyuan College Honors Scholarship	Shanghai Jiao Tong University	2018
1st Prize, National Mathematical Contest in Modeling	Shanghai Division	2018
Academic Excellence Scholarship	Shanghai Jiao Tong University	2017, 2018, 2019

Publications

Conference Papers

[C5] **Hanqing Zhu**, Jiaqi Gu, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "ELight: Enabling Efficient Photonic In-Memory Neurocomputing with Life Enhancement," in *IEEE/ACM Asia and South Pacific Design Automation Conference* (*ASP-DAC*), Jan. 2022.

[C4] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "L2ight: Enabling On-Chip Learning for Optical Neural Networks via Efficient in-situ Subspace Optimization," in *Conference on Neural Information Processing Systems* (*NeurIPS*), Dec. 2021.

[C3] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "Towards Memory-Efficient Neural Networks via Multi-Level in situ Generation," in *International Conference on Computer Vision* (*ICCV*), Oct. 2021.

[C2] Chenghao Feng, Jiaqi Gu, **Hanqing Zhu**, David Z. Pan, and Ray T. Chen, "Experimental Demonstration of a WDM-based Integrated Optical Decoder for Compact Optical Computing," in *Conference on Lasers and Electro-Optics*, May 2021.

[C1] Jiaqi Gu, Zheng Zhao, Chenghao Feng, **Hanqing Zhu**, Ray T. Chen, and David Z. Pan, "ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls," in *IEEE/ACM Proceedings Design, Automation and Test in Europe* (*DATE*), Mar. 2020.

Preprint Papers

[M2] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Zixuan Jiang, Mingjie Liu, Shuhan Zhang, Ray T. Chen, and David Z. Pan, "ADEPT: Automatic Differentiable DEsign of Photonic Tensor Cores," in *arXiv preprint 2112.08703*, 2021

[M1] Chenghao Feng*, Jiaqi Gu*, **Hanqing Zhu**, Zhoufeng Ying, Zheng Zhao, David Z. Pan, and Ray T. Chen, "Silicon photonic subspace neural chip for hardware-efficient deep learning," in *arXiv preprint 2111.06705*, 2021

Courses

○ EE381V: Combinatorial Optimization	*Prof. Constantine Caramanis*
○ EE382M: VLSI CAD and Optimization	*Prof. David Z. Pan*
○ EE382N: Computer Architecture: Parallelism/Locality	*Prof. Mattan Erez*
○ EE381V: Advanced Topics in Computer Vision	*Prof. Zhangyang (Atlas) Wang*
○ EE381K: Convex Optimization	*Prof. Constantine Caramanis*
○ EE382M: VLSI I	*Prof. David Z. Pan*
○ EE382M: VLSI Physical Design Automation (In progress)	*Prof. David Z. Pan*

Skills

- **Programming Languages:** Python, C++, CUDA, Verilog
- **Deep Learning Toolkits:** Pytorch
- **EDA tools:** Cadence Virtuoso, Synopsys Design Compiler, Hspice, Xilinx Vivado Design Suite

Professional Services

Reviewer

- IEEE Transactions on Neural Networks and Learning Systems (TNNLS'22)

Teaching Experience

- EE316: Digital Logic Design — Fall 2022