Hanqing Zhu

Graduate Research Assistant - University of Texas at Austin
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Research Interests

Efficient and robust AI computing system with emerging technology, hardware-efficient machine learning, and VLSI design automation.

Education

University of Texas at Austin(UT-Austin) **Austin, TX, USA**
Ph.D., Dept. of Electrical and Computer Engineering *Sept. 2020 - Present*
Advisor: David Z. Pan
Co-advisor: Ray T. Chen
GPA: 3.95/4.00

Shanghai Jiao Tong University(SJTU) **Shanghai, China**
B.E., Dept. of Microelectronics Science and Technology *Sept. 2016 - Jun. 2020*
Overall GPA: 3.81/4.00 (Rank: 2nd/57)

Research Experience

University of Texas at Austin **Austin, TX, USA**
Graduate Research Assistant (UTDA Lab), advised by Prof. David Z. Pan *Sept. 2020 - Present*

- **VLSI Placement**
  - **Quality Improvement of DREAMPlace**: Investigated the optimality of DREAMPlace; on-going attempt to use Reinforcement Learning (RL) to tune parameters of the global placement phase.
- **Efficient and Robust AI Computing System with Emerging technology**
  - **Robust Photonic In-Memory Neurocomputing**: Proposed an aging-aware co-optimization framework to enable aging-resilient photonic in-memory computing; achieved **40**× dynamic energy cost and >**20**× programming operations reduction; significantly enhanced energy efficiency and executing lifetime of the photonic computing engine. [J2, C5]
  - **Automatic Photonic Tensor Core Design**: Proposed a fully differentiable method to automatically search Photonic tensor core (PTC) circuit topology; achieved **2**×-**30**× higher footprint compactness with competitive matrix representability; opened the possibility to move beyond the manual design paradigm and nurture photonic neurocomputing with AI and design automation. [C6]
  - **NN On-chip Learning**: Proposed an efficient on-chip learning protocol, *L2ight*, for optical computing system; devised a subspace learning procedure with multi-level sparsity to enable *in-situ* gradient evaluation and low computation cost; achieved 3-order-of-magnitude higher scalability and over **30**× better efficiency than previous optical on-chip training tools. [C4]
- **Hardware-aware Machine Learning**
  - **Memory-efficient NN Design**: Designed memory-efficient neural network with *in-situ* weight generation; proposed multi-level low-rank weight generation methodology with mixed-precision quantization; Achieved **10**×-**20**× memory on-chip memory cost for emerging NN accelerators. [C3]
  - **NN Quantization and Robustness**: Collaborated on quantization-aware training scheme in the unitray manifold to enable robust optical neural networks; achieved better accuracy and robustness with limited control resolution and device-level variations. [C1]
- **Photonics Neural Chip Tape-out**
  - Worked on photonic neural chip tape-out for novel ONN architectures using Advanced Micro Foundry (AMF); collaborated on the full-stack schematic design, layout, validation, tape-out, and measurement of photonic neural chips using PyTorch, Lumerical toolkits, and Synopsys optodesigner. [P1]

Shanghai Jiao Tong University **Shanghai, China**
Undergraduate Research Assistant, advised by Prof. Guanghui He *Sept. 2019 - Aug. 2020*

- **Design Space Exploration for FPGA-based Electromagnetic Transient Simulation System Auto-Builder**
  - Established a resource usage and delay estimation model; Proposed an automatic search method to find optimal design parameters of the FPGA-based electromagnetic transient smulation system.

Honors and Awards

A. Richard Newton Young Student Fellow	DAC	2021
Shanghai Outstanding Graduate	Shanghai City	2020
Department Excellent Undergraduate Thesis	Shanghai Jiao Tong University	2020
Hongyi Scholarship	Shanghai Jiao Tong University	2019
Outstanding Undergraduate Scholarship	Shanghai Jiao Tong University	2019
Samsung Scholarship	Shanghai Jiao Tong University	2018
Zhiyuan College Honors Scholarship	Shanghai Jiao Tong University	2018
1st Prize, National Mathematical Contest in Modeling	Shanghai Division	2018
Academic Excellence Scholarship	Shanghai Jiao Tong University	2017, 2018, 2019

Publications

Conference Papers

[C8] Chenghao Feng, Jiaqi Gu, **Hanqing Zhu**, Zhoufeng Ying, Zheng Zhao, David Z. Pan, and Ray T. Chen, "Optoelectronically Interconnected Hardware-Efficient Deep Learning using Silicon Photonic Chips," in *Smart Photonic and Optoelectronic Integrated Circuits* (*SPIE*), Mar., 2022

[C7] Chenghao Feng, Jiaqi Gu, **Hanqing Zhu**, David Z. Pan, and Ray T. Chen, "Design and Experimental Demonstration of A Hardware-Efficient Integrated Optical Neural Network," in *Smart Photonic and Optoelectronic Integrated Circuits* (*SPIE*), Mar., 2022

[C6] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Zixuan Jiang, Mingjie Liu, Shuhan Zhang, Ray T. Chen, and David Z. Pan, "ADEPT: Automatic Differentiable DEsign of Photonic Tensor Cores," in *ACM/IEEE Design Automation Conference* (*DAC*), Jul., 2022

[C5] **Hanqing Zhu**, Jiaqi Gu, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "ELight: Enabling Efficient Photonic In-Memory Neurocomputing with Life Enhancement," in *IEEE/ACM Asia and South Pacific Design Automation Conference* (*ASP-DAC*), Jan. 2022.

[C4] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "L2ight: Enabling On-Chip Learning for Optical Neural Networks via Efficient in-situ Subspace Optimization," in *Conference on Neural Information Processing Systems* (*NeurIPS*), Dec. 2021.

[C3] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "Towards Memory-Efficient Neural Networks via Multi-Level in situ Generation," in *International Conference on Computer Vision* (*ICCV*), Oct. 2021.

[C2] Chenghao Feng, Jiaqi Gu, **Hanqing Zhu**, David Z. Pan, and Ray T. Chen, "Experimental Demonstration of a WDM-based Integrated Optical Decoder for Compact Optical Computing," in *Conference on Lasers and Electro-Optics*, May 2021.

[C1] Jiaqi Gu, Zheng Zhao, Chenghao Feng, **Hanqing Zhu**, Ray T. Chen, and David Z. Pan, "ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls," in *IEEE/ACM Proceedings Design, Automation and Test in Europe* (*DATE*), Mar. 2020.

Journal Papers

[J2] **Hanqing Zhu**, Jiaqi Gu, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "ELight: Towards Efficient and Aging-Resilient Photonic In-Memory Neurocomputing," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), May, 2022.

[J1] Jiaqi Gu, Chenghao Feng, **Hanqing Zhu**, Ray T. Chen and David Z. Pan, "Light in AI: Toward Efficient Neurocomputing with Optical Neural Networks - A Tutorial," in *IEEE Transactions on Circuits and Systems–II: Express Briefs* (*TCAS-II*), Apr., 2022.

Preprint Papers

[P1] Chenghao Feng*, Jiaqi Gu*, **Hanqing Zhu**, Zhoufeng Ying, Zheng Zhao, David Z. Pan, and Ray T. Chen, "Silicon photonic subspace neural chip for hardware-efficient deep learning," in *arXiv preprint 2111.06705*, 2021.

Professional Services

Reviewer
- Nature Photonics
- Photonic Network Communications
- IEEE Transactions on Neural Networks and Learning Systems (TNNLS'22)
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS'22)

Teaching & Volunteer Experiences

Graduate Teaching Assistant
- EE316: Digital Logic Design — Fall 2022

Volunteer
- Conference Volunteer, the IEEE International Symposium on Circuits and Systems — 2022
- Volunteer Teacher, Eryuan No.2 high school, Yunnan, China — Aug. 2017- Sept. 2017
  - Awarded with "Color for love" bronze prize of Chinese college students' rural supporting education

Courses

- EE381V: Combinatorial Optimization — *Prof. Constantine Caramanis*
- EE382M: VLSI CAD and Optimization — *Prof. David Z. Pan*
- EE382N: Computer Architecture: Parallelism/Locality — *Prof. Mattan Erez*
- EE381V: Advanced Topics in Computer Vision — *Prof. Zhangyang (Atlas) Wang*
- EE381K: Convex Optimization — *Prof. Constantine Caramanis*
- EE382M: VLSI I — *Prof. David Z. Pan*
- EE382M: VLSI Physical Design Automation — *Prof. David Z. Pan*

Skills

- **Programming Languages:** Python, C++, CUDA, Verilog
- **Deep Learning Toolkits:** Pytorch
- **EDA tools:** Cadence Virtuoso, Synopsys Design Compiler, Hspice, Xilinx Vivado Design Suite