

Hanqing Zhu

Graduate Research Assistant - University of Texas at Austin

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Research Interests

Efficient and robust AI computing system with emerging technology, hardware-efficient machine learning, VLSI design automation.

Education

University of Texas at Austin(UT-Austin)

Ph.D., Dept. of Electrical and Computer Engineering

Advisor: David Z. Pan

Co-advisor: Ray T. Chen

GPA: 3.95/4.00

Austin, TX, USA

Sept. 2020 - Present

Shanghai Jiao Tong University(SJTU)

B.E., Dept. of Microelectronics Science and Technology

Overall GPA: 3.81/4.00 (Rank: 2nd/57)

Shanghai, China

Sept. 2016 - Jun. 2020

Research Experience

University of Texas at Austin

Graduate Research Assistant (UTDA Lab), advised by Prof. David Z. Pan

Austin, TX, USA

Sept. 2020 - Present

o VLSI Placement

- On-going project on understanding the optimality of SOTA placement algorithms.

o Efficient and Robust AI Computing System with Photonics [C6, C5, C4, C2, C1]

- Proposed an synergistic aging-aware co-optimization framework for emerging photonic in-memory computing paradigm; achieved **40×** dynamic energy cost and **>20×** write operations reduction of the novel PCM-based neurocomputing paradigm; significantly enhanced the executing lifetime of neurocomputing engine under the wearing out pressure.
- Collaborated on work to automatically search Photonic tensor core (PTC) circuit topology; achieved **2×**-**30×** higher footprint compactness with competitive matrix representability; opened the possibility to move beyond the manual design paradigm and nurture photonic neurocomputing with AI and design automation.
- Collaborated on efficient on-chip learning protocol, *L2ight*, for optical computing system; proposed a subspace learning procedure with multi-level sparsity to enable *in-situ* gradient evaluation and low computation cost; achieved 3-order-of-magnitude higher scalability and over **30×** better efficiency than previous optical on-chip training tools.
- Collaborated on quantization-aware training scheme in the unitray manifold to enable robust optical neural networks; achieved better accuracy and robustness with limited control resolution and device-level variations.

o Hardware-efficient Machine Learning [C3]

- Worked on memory-efficient neural network designs for emerging neurocomputing system via multi-level in-situ parameters generation; Achieved **10×**-**20×** memory efficiency with comparable accuracy with SOTA designs.

o Photonics Neural Chip Tape-out [M1]

- Worked on photonic neural chip tape-out for novel ONN architectures using Advanced Micro Foundry (AMF); collaborated on the full-stack schematic design, layout, validation, tape-out, and measurement of photonic neural chips using PyTorch, Lumerical toolkits, and Synopsys optodesigner.

Shanghai Jiao Tong University

Undergraduate Research Assistant, advised by Prof. Guanghui He

Shanghai, China

Sept. 2019 - Aug. 2020

- o **Design Space Exploration for FPGA-based Electromagnetic Transient Simulation System Auto-Builder**
 - Proposed an automatic design space exploration methodology to search for the optimal design parameters to automatically build FPGA-based electromagnetic transient simulation system.
 - Established a coarse-grained resource usage and delay estimation model based on extracted parameters to represent hardware structure with 2.0% and 5.1% estimation error on LUT and DSP usage.
 - Designed a Box-based local Pareto filtering algorithm to automate the parameters selection from the large design space of the multi-objective optimization problem.

Honors and Awards

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| A. Richard Newton Young Student Fellow | DAC | 2021 |
| Shanghai Outstanding Graduate | Shanghai City | 2020 |
| Department Excellent Undergraduate Thesis | Shanghai Jiao Tong University | 2020 |
| Hongyi Scholarship | Shanghai Jiao Tong University | 2019 |
| Outstanding Undergraduate Scholarship | Shanghai Jiao Tong University | 2019 |
| Samsung Scholarship | Shanghai Jiao Tong University | 2018 |
| Zhiyuan College Honors Scholarship | Shanghai Jiao Tong University | 2018 |
| 1st Prize, National Mathematical Contest in Modeling | Shanghai Division | 2018 |
| Academic Excellence Scholarship | Shanghai Jiao Tong University | 2017, 2018, 2019 |

Publications

Conference Papers

[C6] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Zixuan Jiang, Mingjie Liu, Shuhan Zhang, Ray T. Chen, and David Z. Pan, “[ADEPT: Automatic Differentiable DDesign of Photonic Tensor Cores](#),” in *ACM/IEEE Design Automation Conference (DAC)*, Jul., 2022

[C5] **Hanqing Zhu**, Jiaqi Gu, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, “[ELight: Enabling Efficient Photonic In-Memory Neurocomputing with Life Enhancement](#),” in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2022.

[C4] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Zixuan Jiang, Ray T. Chen, and David Z. Pan, “[L2ight: Enabling On-Chip Learning for Optical Neural Networks via Efficient in-situ Subspace Optimization](#),” in *Conference on Neural Information Processing Systems (NeurIPS)*, Dec. 2021.

[C3] Jiaqi Gu, **Hanqing Zhu**, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, “[Towards Memory-Efficient Neural Networks via Multi-Level in situ Generation](#),” in *International Conference on Computer Vision (ICCV)*, Oct. 2021.

[C2] Chenghao Feng, Jiaqi Gu, **Hanqing Zhu**, David Z. Pan, and Ray T. Chen, “[Experimental Demonstration of a WDM-based Integrated Optical Decoder for Compact Optical Computing](#),” in *Conference on Lasers and Electro-Optics*, May 2021.

[C1] Jiaqi Gu, Zheng Zhao, Chenghao Feng, **Hanqing Zhu**, Ray T. Chen, and David Z. Pan, “[ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls](#),” in *IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE)*, Mar. 2020.

Preprint Papers

[M1] Chenghao Feng*, Jiaqi Gu*, **Hanqing Zhu**, Zhoufeng Ying, Zheng Zhao, David Z. Pan, and Ray T. Chen, “[Silicon photonic subspace neural chip for hardware-efficient deep learning](#),” in *arXiv preprint 2111.06705*, 2021

Professional Services

Reviewer

- o IEEE Transactions on Neural Networks and Learning Systems (TNNLS'22)
- o IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS'22)

Teaching Experience

Graduate Teaching Assistant

- o EE316: Digital Logic Design Fall 2022

Volunteer Teacher

- o Summer school at Eryuan No.2 high school, Yunnan, China Aug. 2017- Sept. 2017
 - Awarded with "Color for love" bronze prize of Chinese college students' rural supporting education

Courses

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| o EE381V: Combinatorial Optimization | <i>Prof. Constantine Caramanis</i> |
| o EE382M: VLSI CAD and Optimization | <i>Prof. David Z. Pan</i> |
| o EE382N: Computer Architecture: Parallelism/Locality | <i>Prof. Mattan Erez</i> |
| o EE381V: Advanced Topics in Computer Vision | <i>Prof. Zhangyang (Atlas) Wang</i> |
| o EE381K: Convex Optimization | <i>Prof. Constantine Caramanis</i> |
| o EE382M: VLSI I | <i>Prof. David Z. Pan</i> |
| o EE382M: VLSI Physical Design Automation (In progress) | <i>Prof. David Z. Pan</i> |

Skills

- o **Programming Languages:** Python, C++, CUDA, Verilog
- o **Deep Learning Toolkits:** Pytorch
- o **EDA tools:** Cadence Virtuoso, Synopsys Design Compiler, Hspice, Xilinx Vivado Design Suite