OmniVision

OV2659

datasheet

PRODUCT SPECIFICATION

1/5" color CMOS UXGA (2 megapixel) image sensor
with OmniPixel3-HS™ technology

Copyright © 2010 OmniVision Technologies, Inc. All rights reserved.

Trademark Information

color CMOS UXGA (2 megapixel) image sensor with OmniPixel3-HS™ technology

datasheet (CSP3)
PRODUCT SPECIFICATION

version 2.0
august 2010

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

features

- ultra low power and low cost
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, and windowing
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555, YUV422, YCbCr422 and GBR422

- support for images sizes: UXGA, SVGA and 720p
- support for video operations
- support for horizontal and vertical sub-sampling, binning
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- on-chip phase lock loop (PLL)
- programmable I/O drive capability
- built-in regulator for DVDD

key specifications

- **active array size:** 1632 x 1212
- **power supply:**
  core: 1.5VDC ± 5%
  analog: 2.6 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: 224 mW
  standby: 75 µA
- **temperature range:**
  operating: -20°C to 70°C (see **table 8-2**)
  stable image: 0°C to 50°C (see **table 8-2**)
- **output formats (8-bit):** YUV422 / YCbCr422, GBR422, RGB565/555, 8-/10-bit raw RGB data
- **lens size:** 1/5"
- **lens chief ray angle:** 25.7° (see **figure 10-2**)
- **input clock frequency:** 6 ~ 27 MHz
- **S/N ratio:** 36 dB

- **dynamic range:** 66 dB
- **maximum image transfer rate:**
  UXGA (1600x1200): 15 fps
  SVGA (800x600): 30 fps
  720p (1280x720): 30 fps
  1366x768 (1366x768): 24 fps
- **sensitivity:** 960 mV/Lux-sec
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 1228 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 1.75 µm x 1.75 µm
- **well capacity:** 6.3 Ke⁻
- **dark current:** 4 mV/sec @ 60ºC
- **fixed pattern noise (FPN):** 1% of $V_{PEAK-TO-PEAK}$
- **image area:** 2856 µm x 2121 µm
- **package dimensions:** 4735 µm x 4385 µm

table of contents

list of figures

list of tables

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV2659 image sensor. The package information is shown in **section 9**.

table 1-1   signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description
A1	DOGND	ground	ground for I/O circuit
A2	PWDN	input	power down (active high with internal pull down resistor)
A3	DOVDD	power	power for I/O circuit
A4	SVDD	power	power for array circuit
A5	SGND	ground	ground for array circuit
A6	VN	reference	internal analog reference
A7	VH	reference	internal analog reference
B1	AVDD	power	power for analog circuit
B2	RESETB	input	reset (active low with internal pull up resistor)
B3	TM	input	test mode (active high with internal pull down resistor)
B4	NC	–	no connect
B5	NC	–	no connect
B6	NC	–	no connect
B7	AVDD	power	power for analog circuit
C1	AGND	ground	ground for analog circuit
C2	NC	–	no connect
C6	NC	–	no connect
C7	AGND	ground	ground for analog circuit
D1	NC	–	no connect
D2	NC	–	no connect
D6	NC	–	no connect
D7	PVDD	reference	power for PLL circuit
E1	DVDD	reference	power for digital circuit
E2	NC	–	no connect
E6	NC	–	no connect

table 1-1   signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description
E7	XVCLK	input	system input clock
F1	DGND	ground	ground for digital circuit
F2	HREF	I/O	DVP HREF output
F3	D6	I/O	DVP data output port 6
F4	NC	–	no connect
F5	D3	I/O	DVP data output port 3
F6	SIOC	input	SCCB input clock
F7	SIOD	I/O	SCCB data
G1	VSYNC	I/O	DVP VSYNC output
G2	D4	I/O	DVP data output port 4
G3	D0	I/O	DVP data output port 0
G4	PCLK	I/O	DVP PCLK output
G5	DVDD	reference	power for digital circuit
G6	D7	I/O	DVP data output port 7
G7	DGND	ground	ground for digital circuit
H1	D8	I/O	DVP data output port 8
H2	D2	I/O	DVP data output port 2
H3	DOGND	ground	ground for I/O circuit
H4	DOVDD	power	power for I/O circuit
H5	D1	I/O	DVP data output port 1
H6	D5	I/O	DVP data output port 5
H7	D9	I/O	DVP data output port 9

figure 1-1   pin diagram
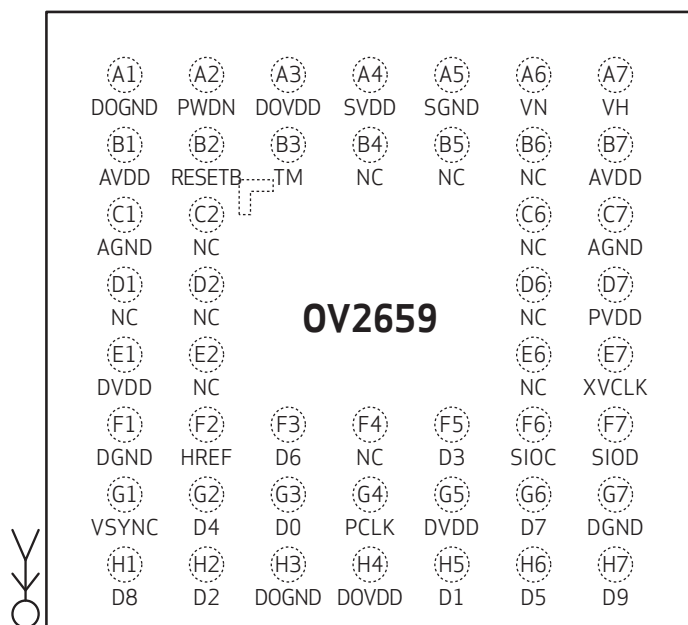
(A1) DOGND	(A2) PWDN	(A3) DOVDD	(A4) SVDD	(A5) SGND	(A6) VN	(A7) VH
(B1) AVDD	(B2) RESETB	(B3) TM	(B4) NC	(B5) NC	(B6) NC	(B7) AVDD
(C1) AGND	(C2) NC				(C6) NC	(C7) AGND
(D1) NC	(D2) NC		OV2659		(D6) NC	(D7) PVDD
(E1) DVDD	(E2) NC				(E6) NC	(E7) XVCLK
(F1) DGND	(F2) HREF	(F3) D6	(F4) NC	(F5) D3	(F6) SIOC	(F7) SIOD
(G1) VSYNC	(G2) D4	(G3) D0	(G4) PCLK	(G5) DVDD	(G6) D7	(G7) DGND
(H1) D8	(H2) D2	(H3) DOGND	(H4) DOVDD	(H5) D1	(H6) D5	(H7) D9

2659_CSP_DS_1_1

2 system level description

2.1 overview

The OV2659 (color) image sensor is a low voltage, high-performance 1/5-inch 2.0 megapixel CMOS image sensor that provides the full functionality of a single chip UXGA (1600x1200) camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or cropped 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV2659 has an image array capable of operating at up to 15 frames per second (fps) in UXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. In addition, Omnivision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.2 architecture

The OV2659 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV2659 image sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1   OV2659 block diagram
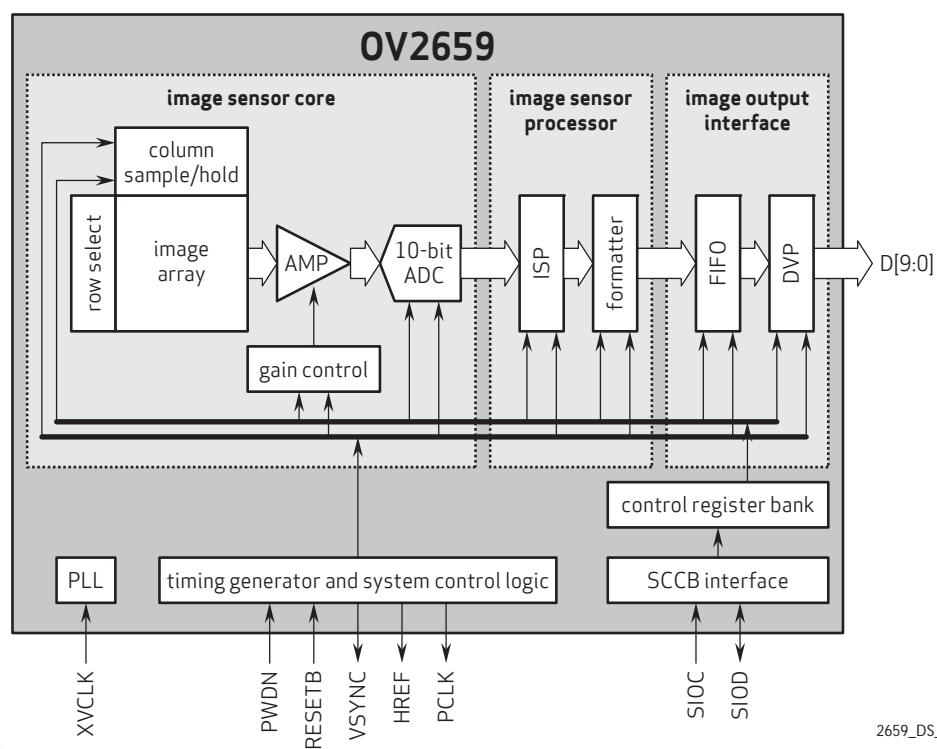
2.3 I/O control

The OV2659 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pins.

table 2-1   driving capability and direction control for I/O pins (sheet 1 of 2)

address	register name	default value	R/W	description
0x3011	OUTPUT DRIVE CAPABILITY CTRL	0x02	RW	Pad Control Bit[7:6]: Output drive capability for PCLK, VSYNC, HREF, D[9:0] 00: 1x 01: 2x 10: 3x 11: 4x
0x3000	IO CTRL00	0x00	RW	GPIO Direction Control (0: input; 1: output) Bit[1:0]: DVP D[9:8] output enable
0x3001	IO CTRL01	0x00	RW	GPIO Direction Control (0: input; 1: output) Bit[7:0]: DVP D[7:0] output enable
0x3002	IO CTRL02	0x00	RW	GPIO Direction Control (0: input; 1: output) Bit[7]: VSYNC output enable Bit[6]: HREF output enable Bit[5]: PCLK output enable
0x3008	OUTPUT VALUE00	0x00	RW	Bit[1:0]: DVP D[9:8] value for output
0x3009	OUTPUT VALUE01	0x00	RW	Bit[7:0]: DVP D[7:0] value for output
0x300D	OUTPUT VALUE02	0x00	RW	Bit[7]: VSYNC value for output Bit[6]: HREF value for output Bit[5]: PCLK value for output
0x300E	OUTPUT SELECT00	0x00	RW	GPIO Output Select (0: select DVP; 1: select from registers) Bit[1:0]: DVP D[9:8] output select
0x300F	OUTPUT SELECT01	0x00	RW	GPIO Output Select (0: select DVP; 1: select from registers) Bit[7:0]: DVP D[7:0] output select
0x3010	OUTPUT SELECT02	0x00	RW	GPIO Output Select (0: select DVP; 1: select from registers) Bit[7]: VSYNC output select Bit[6]: HREF output select Bit[5]: PCLK output select
0x302D	INPUT READOUT00	–	R	Bit[1]: TM input readout Bit[0]: PWDN input readout

table 2-1   driving capability and direction control for I/O pins (sheet 2 of 2)

address	register name	default value	R/W	description
0x302E	INPUT READOUT01	–	R	Bit[6]: SIOC input readout Bit[5]: SIOD input readout Bit[4]: VSYNC input readout Bit[3]: HREF input readout Bit[2]: PCLK input readout Bit[1:0]: DVP D[9:8] input readout
0x302F	INPUT READOUT02	–	R	Bit[7:0]: DVP D[7:0] input readout

2.4 format and frame rate

table 2-2   format and frame rate

format	resolution	frame rate	scaling method	parallel port data rate (RAW/YUV)
UXGA	1600x1200	15 fps	full	36/72 MHz
SVGA	800x600	30 fps	down sampling	24/48 MHz
VGA	640x480	30 fps	scaling	24/48 MHz
400x300	400x300	30 fps	subsample	18/36 MHz
200x150	200x150	30 fps	subsample	18/36 MHz
720p	1280x720	30 fps	cropping	36/72 MHz
1366x768	1366x768	24 fps	cropping	36/72 MHz

2.5 power up sequence

Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred.

2.5.1 power up with internal DVDD and I2C access during power up period

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. if DOVDD and AVDD are turned ON at the same time, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high if I2C is accessed during the power up period
4. for PWDN to go low, power must first become stable (AVDD to PWDN $\geq$ 1 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power up period once DOVDD is up

figure 2-2   power up timing with internal DVDD and I2C access during power up period
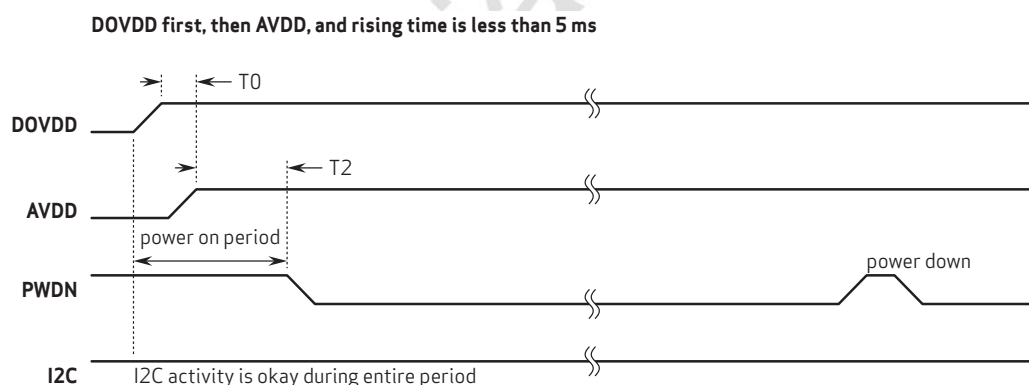
DOVDD first, then AVDD, and rising time is less than 5 ms

note   T0 $\geq$ 0 ms: delay from DOVDD stable to AVDD stable
T2 $\geq$ 1 ms: delay from AVDD stable to sensor power up stable   2659_DS_2_2

2.5.2 power up with internal DVDD and no I2C access during power up period

For powering up with the internal DVDD and no I2C access during the power ON period, the following conditions must occur:

1. if DOVDD and AVDD are turned ON at the same time, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is not required if there is no I2C access during the power up period
3. no I2C activity is allowed during the power up period (see gray area in **figure 2-3**)
4. RESETB is active low with an asynchronized design
5. state of RESETB does not matter during power up period once DOVDD is up

figure 2-3   power up timing with internal DVDD and no I2C access during power up period
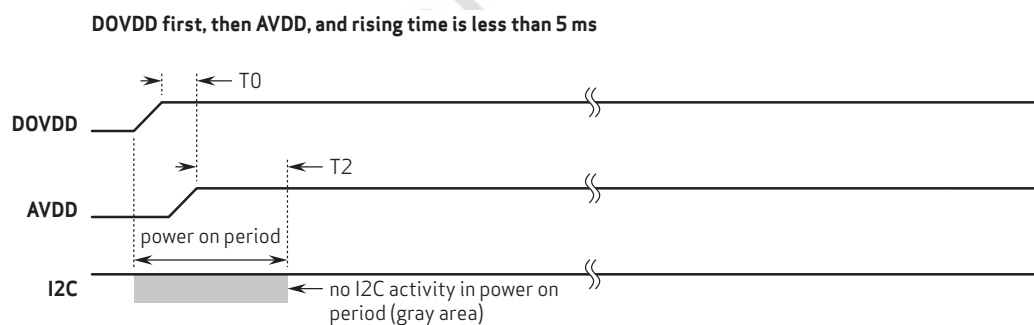
DOVDD first, then AVDD, and rising time is less than 5 ms

note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T2 ≥ 1 ms: delay from AVDD stable to sensor power up stable

2659_DS_2_3

2.5.3 power up with external DVDD source and I2C access during power up period

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

1. if DOVDD and AVDD are turned ON at the same time, make sure DOVDD becomes stable before AVDD becomes stable
2. if AVDD and DVDD are turned ON at the same time, make sure AVDD becomes stable before DVDD becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power must first become stable (DVDD to PWDN $\geq$ 1 ms)
5. all powers are cut off when the camera is not in use (power down mode is not recommended
6. RESETB is active low with an asynchronized design
7. state of RESETB does not matter during power up period once DOVDD is up

figure 2-4   power up timing with external DVDD source and I2C access during power up period
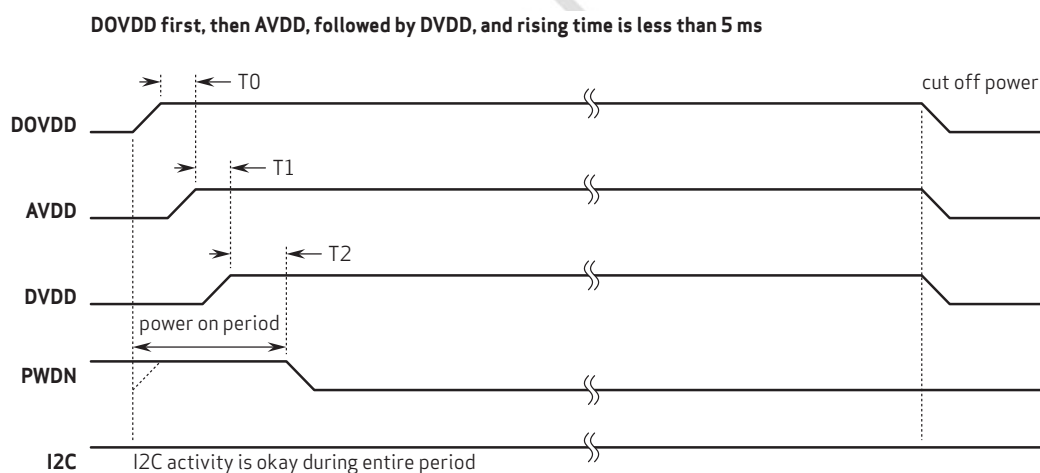
DOVDD first, then AVDD, followed by DVDD, and rising time is less than 5 ms

note T0 $\geq$ 0 ms: delay from DOVDD stable to AVDD stable
T1 $\geq$ 0 ms: delay from AVDD stable to DVDD stable
T2 $\geq$ 1 ms: delay from DVDD stable to sensor power up stable

2659_DS_2_4

2.5.4 power up with external DVDD and no I2C access during power up period

For powering up with an external DVDD source and no I2C access during the power ON period, the following conditions must occur:

1. if DOVDD and AVDD are turned ON at the same time, make sure DOVDD becomes stable before AVDD becomes stable
2. if AVDD and DVDD are turned ON at the same time, make sure AVDD becomes stable before DVDD becomes stable
3. all powers are cut off when the camera is not in use (power down mode is not recommended
4. RESETB is active low with an asynchronized design
5. state of RESETB does not matter during power up period once DOVDD is up

figure 2-5   power up timing with external DVDD source and I2C access during power up period
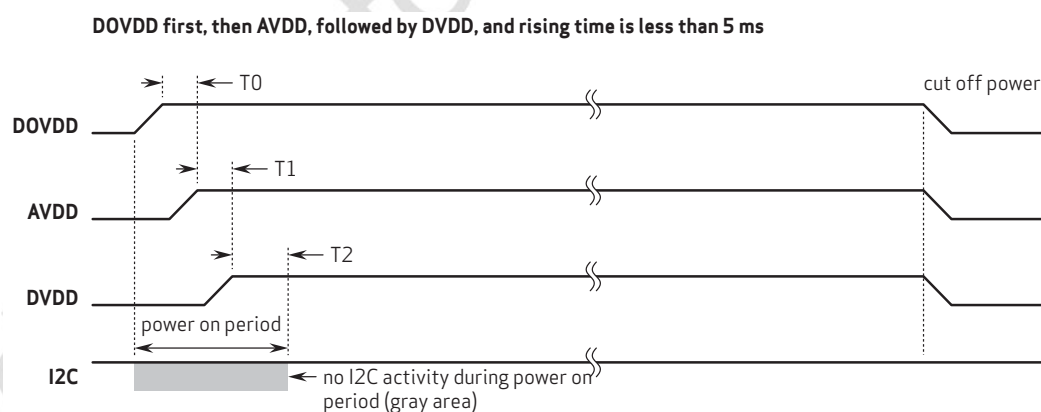
DOVDD first, then AVDD, followed by DVDD, and rising time is less than 5 ms

note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T1 ≥ 0 ms: delay from AVDD stable to DVDD stable
T2 ≥ 1 ms: delay from DVDD stable to sensor power up stable   2659_DS_2_5

2.6 reset

The OV2659 sensor includes a RESETB pin that forces a complete hardware reset when it is pulled low (GND). The OV2659 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x0103[0] to high.

The whole chip will be reset during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power up reset is included. The hard reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 1 ms.

table 2-3   software reset control

address	register name	default value	R/W	description
0x0103	SOFTWARE RESET	0x00	RW	Bit[0]: Software reset 1: reset

2.7 hardware standby and software standby

Two suspend modes are available for the OV2659:

- hardware standby
- software standby

2.7.1 hardware standby

To initiate hardware standby mode, PWDN pin must be tied to high (see **figure 2-6**).

figure 2-6   power down/ wake up sequence
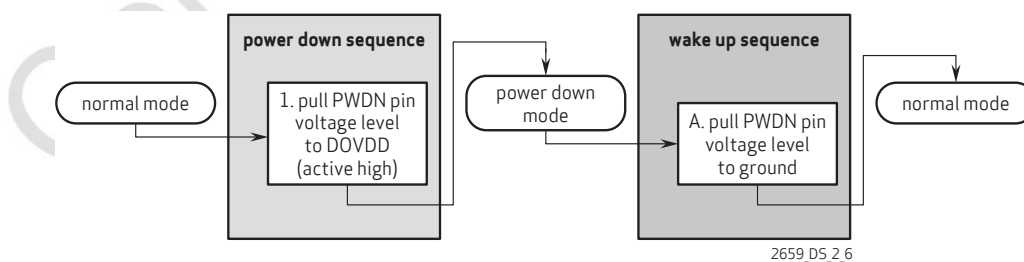
2659_DS_2_6

figure 2-7   power down timing diagram
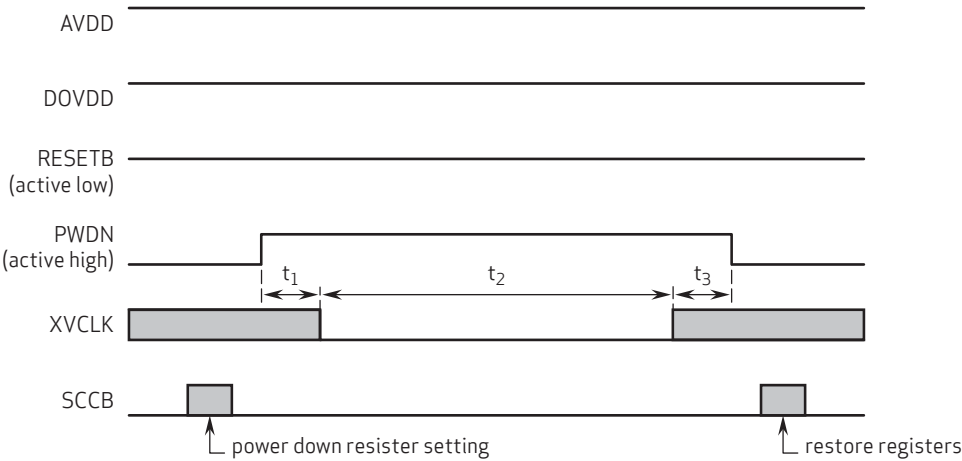
note   t$_1$: XVCLK should keep more than 0.1ms after PWDN is pulled high
t$_2$: power down period should last more than 1 VSYNC period
t$_3$: XVCLK should come more than 0.1ms before PWDN is pulled low

2659_DS_2_7

When this occurs, the OV2659 internal device clock is halted and all internal counters are reset and registers are maintained.

2.7.2 software standby

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

table 2-4   software standby control

address	register name	default value	R/W	description
0x0100	SOFTWARE STANDBY	0x00	RW	Bit[0]: Software standby 0: Software standby 1: Streaming

2.8 power OFF sequence

Powering off timing for the OV2659 sensor is described in **figure 2-8**.

figure 2-8   power OFF timing diagram

2659_DS_2_8
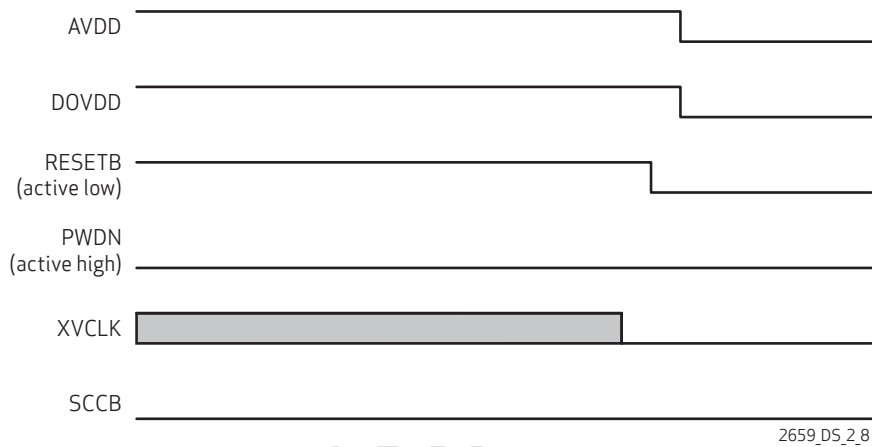
2.9 system clock control

The OV2659 PLL allows for an input clock frequency ranging from 6~27 MHz.

The PLL can be bypassed by setting register 0x3005[7] to 1.

table 2-5   system clock control

address	register name	default value	R/W	description
0x3005	SC CMMN PLL CTRL2	0x24	RW	Bit[7]: PLL_bypass Bit[5:0]: Multiplier
0x3006	SC CMMN PLL CTR13	0x0D	RW	Bit[4:3]: System divider 00: Div 1x 01: Div 2x 10: Div 8x 11: Div 16x Bit[2:0]: Pre-divider 000: 1x 001: 1.5x 010: 2x 011: 3x 100: 2x 101: 3x 110: 4x 111: 6x

2.10 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.11 group hold

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV2659 supports up to four groups. These groups share 128 byte RAM and the size of each group is programmable by adjusting the start address. The group hold start addresses are range from 0x00 to 0x07, where the unit is 16 bytes.

note
Group 2 and group 3 default values are incorrect. If these groups need to be used, please change the default values.

table 2-6   group sharing function control

address	register name	default value	R/W	description
0x3200	GROUP ADDRESS 00	0x00	RW	SRAM Group Address 0
0x3201	GROUP ADDRESS 01	0x04	RW	SRAM Group Address 1
0x3202	GROUP ADDRESS 02	0x08	RW	SRAM Group Address 2
0x3203	GROUP ADDRESS 03	0x0B	RW	SRAM Group Address 3

The group write function is controlled by register 0x3208.

table 2-7   group hold/write function control

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: Group control 0000: Group hold start 0001: Group hold end 1010: Group launch Bit[3:0]: Group ID 0000: Group bank 0 Default start from address 0x00 0001: Group bank 1 Default start from address 0x40 0010: Group bank 2 Default start from address 0x80 0011: Group bank 3 Default start from address 0xB0

The SCCB will enter group write mode after writing to register with a valid group ID. The subsequent registers will be held to the buffer specified by the group_id instead of writing to the registers. Make sure the number of registers does not exceed the capacity of the group. Setting group_hold_end to 1 will exit the group write mode. After that, setting both group_launch and group_launch_en to 1 will write the buffered values to the real registers. Multiple groups of registers can be prepared before writing to the real registers but be sure the correct group_id is specified when the group write is launched.

The following is an example demonstrating the group write operation:

60 3208 00;	Enable group0
60 3600 00;	Write registers to be held in group0
60 3601 01	
60 3208 10	End group0
60 3208 01	Enable group1
60 3602 02	Write registers to be held in group1
60 3603 03	
60 3208 11	End group1
Other direct register access	
60 3208 02	Enable group2
60 3604 04	Write registers to be held in group2
60 3605 05	
60 3208 12	End group2
60 3208 A0	Launch group0
Other direct register access	
60 3208 03	Enable group3
60 3606 06	Write registers to be held in group3
60 3607 07	
60 3208 13	End group3
60 3208 A1	Launch group1
60 3208 A2	Launch group2
60 3208 A3	Launch group3

3   block level description

3.1   pixel array structure

The OV2659 sensor has an image array of 1632 columns by 1212 rows (1,977,984 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 1,977,984 pixels, 1,920,000 (1600x1200) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1   sensor array region color filter layout
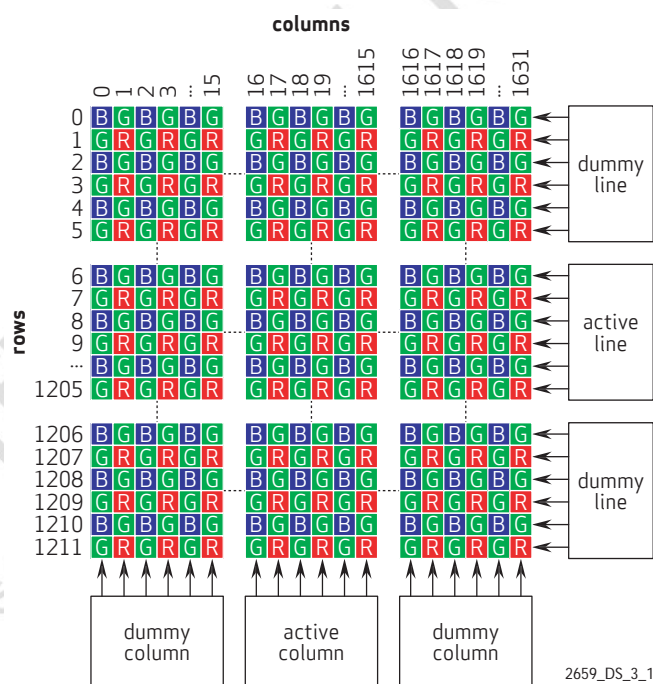
2659_DS_3_1

4   image sensor core digital functions

4.1 mirror and flip

The OV2659 provides Mirror and Flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**). In mirror, since the Bayer order changes from BGBG... to GBGB..., the OV2659 usually automatically delays the read-out sequence by one pixel. In flip, the OV2659 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make necessary adjustments.

figure 4-1   mirror and flip samples

| original image | mirrored image | flipped image | mirrored and flipped image |
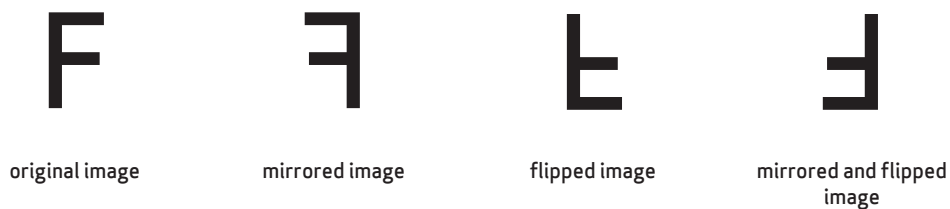
2659_DS_4_1

table 4-1   mirror and flip function control

function	register	description
mirror	0x3820	Timing Control Bit[2]: ISP vflip Bit[1]: Sensor vflip
flip	0x3821	Timing Control Bit[2]: ISP mirror Bit[1]: Sensor mirror

4.2 image windowing

In the OV2659, image windowing is defined by registers 0x3800~0x3813. Figure 4-2 illustrated how those registers define the windowing size. Physical pixel size is the total pixel array size in the sensor. The ISP input size is the total pixel data read from the pixel array. Typically, the larger ISP input size is, the less maximum frame rate can be reached. The data output size is the image output size of the OV2659. This size is windowed from ISP input size and is defined by x_offset and y_offset as shown in **figure 4-2** shows.

figure 4-2   image windowing

2659 DS 4 2
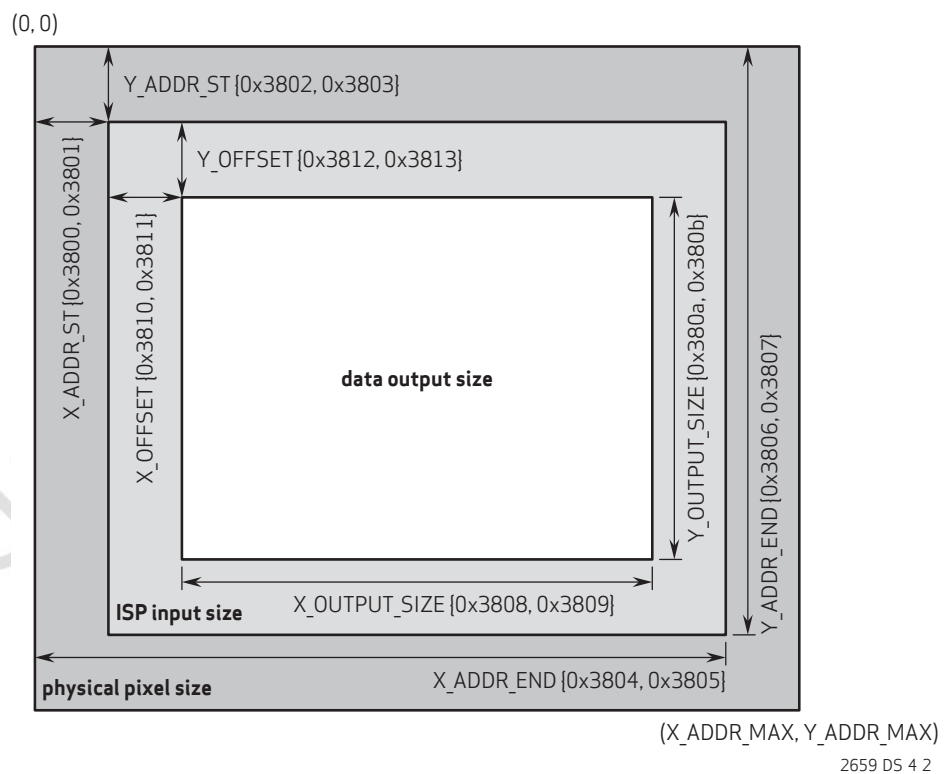
figure 4-3 shows the windowing configuration when scaling function is enabled. The pre-scaling image size is the ISP input size subtracted by two times of offsets for both horizontal and vertical.

figure 4-3 image windowing with scaling

2659_DS_4_3
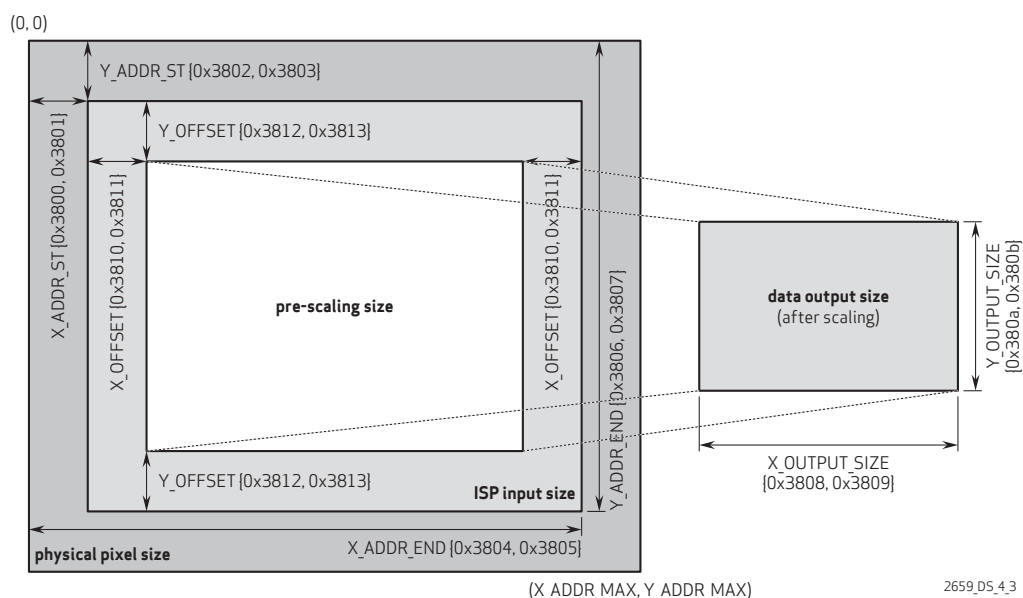
table 4-2 image windowing control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x00	RW	Bit[2:0]: X address start[10:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: X address start[7:0]
0x3802	TIMING VS	0x00	RW	Bit[2:0]: Y address start[10:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: Y address start[7:0]
0x3804	TIMING HW	0x00	RW	Bit[2:0]: X address end[10:8]
0x3805	TIMING HW	0x5F	RW	Bit[7:0]: X address end[7:0]
0x3806	TIMING VH	0x04	RW	Bit[2:0]: Y address end[10:8]
0x3807	TIMING VH	0xBB	RW	Bit[7:0]: Y address end[7:0]
0x3808	TIMING DVPHO	0x06	RW	Bit[2:0]: DVP output horizontal width[10:8]
0x3809	TIMING DVPHO	0x40	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x04	RW	Bit[2:0]: DVP output vertical height[10:8]
0x380B	TIMING DVPVO	0xB0	RW	Bit[7:0]: DVP output vertical height[7:0]
0x380C	TIMING HTS	0x07	RW	Bit[7:0]: Total horizontal size[15:8]
0x380D	TIMING HTS	0x9C	RW	Bit[7:0]: Total horizontal size[7:0]

table 4-2   image windowing control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x380E	TIMING VTS	0x04	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING VTS	0xD0	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING HOFFSET	0x00	RW	Bit[2:0]: ISP horizontal offset[10:8]
0x3811	TIMING HOFFSET	0x10	RW	Bit[7:0]: ISP horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x00	RW	Bit[2:0]: ISP vertical offset[10:8]
0x3813	TIMING VOFFSET	0x06	RW	Bit[7:0]: ISP vertical offset[7:0]

4.3 test pattern

For testing purposes, the OV2659 offers one type of test pattern, color bar.

figure 4-4   test pattern
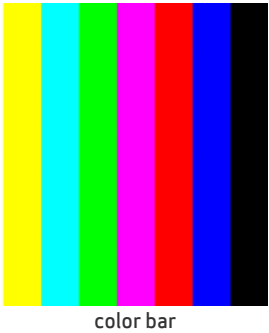
color bar

table 4-3   test pattern selection control

function	register	description
color bar	0x50A0	Bit[7]: color bar enable 0: color bar OFF 1: color bar enable

4.4 AEC/AGC algorithms

4.4.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-4**.

table 4-4 AEC/AGC control functions

address	register name	default value	R/W	description
0x3500	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[3:0]: Exposure[19:16]
0x3501	AEC PK EXPOSURE	0x02	RW	Exposure Output Bit[7:0]: Exposure[15:8]
0x3502	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[7:0]: Exposure[7:0]
0x3503	AEC PK MANUAL	0x00	RW	AEC Manual Mode Control Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x350A	AEC PK REAL GAIN	0x00	RW	Real Gain Bit[1:0]: Real gain[9:8] The value divided by 16 is the actual gain
0x350B	AEC PK REAL GAIN	0x10	RW	Real Gain Bit[7:0]: Real gain[7:0] The value divided by 16 is the actual gain
0x3506	AEC PK ADD VTS	0x00	RW	AEC ADD VTS Output Bit[7:0]: ADD VTS[15:8]
0x3507	AEC PK ADD VTS	0x00	RW	AEC ADD VTS Output Bit[7:0]: ADD VTS[7:0]

4.4.2 average-based algorithm

The average-based AEC controls image luminance using registers **0x3A0F**, **0x3A10**, **0x3A1B**, and **0x3A1E**. In average-based mode, the value of register **0x3A0F** indicates the high threshold value, and the value of register **0x3A10** indicates the low threshold value. The value of register **0x3A1B** indicates the high threshold value for image change from stable state to unstable state and the value of register **0x3A1E** indicates the low threshold value for image change from stable state to unstable state. When the target image luminance average value AVG READOUT (**0x5237**) is within the

range specified by registers **0x3A1B** and **0x3A1E**, the AEC keeps the image exposure and gain. When register AVG READOUT (**0x5237**) is greater than the value in register **0x3A1B**, the AEC will decrease the image exposure and gain until it falls into the range of {**0x3A10**, **0x3A0F**}. When register AVG READOUT (**0x5237**) is less than the value in register **0x3A1E**, the AEC will increase the image exposure and gain until it falls into the range of {**0x3A10**, **0x3A0F**}. Accordingly, the value in register **0x3A0F** should be greater than the value in register **0x3A10**. The gap between the values of registers **0x3A1B** and **0x3A1E** controls the image stability.

The AEC function supports both manual and auto speed selections in order to bring the image exposure into the range set by the values in registers **0x3A0F** and **0x3A10**. For manual mode, the speed supports both normal and fast speed selection. AEC set to normal mode will allow for the slowest step increment or decrement in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increment or decrement in the image exposure to maintain the specified range. For auto mode, the speed step will automatically be adjusted according to the difference between the target and present values. The auto ratio of steps can be set by register bits AVG READOUT (**0x5237**); thus, the AEC speed can be adjusted automatically by the image average value or controlled manually.

Register **0x3A11** and register **0x3A1F** controls the fast AEC range in manual speed selection made. If the target image AVG READOUT (**0x5237**) is greater than **0x3A11**, AEC will decrease by half. If register AVG READOUT (**0x5237**) is less than **0x3A1F**, AEC will double.

As shown in desired convergence, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size of fast and slow conditions.

figure 4-5   desired convergence
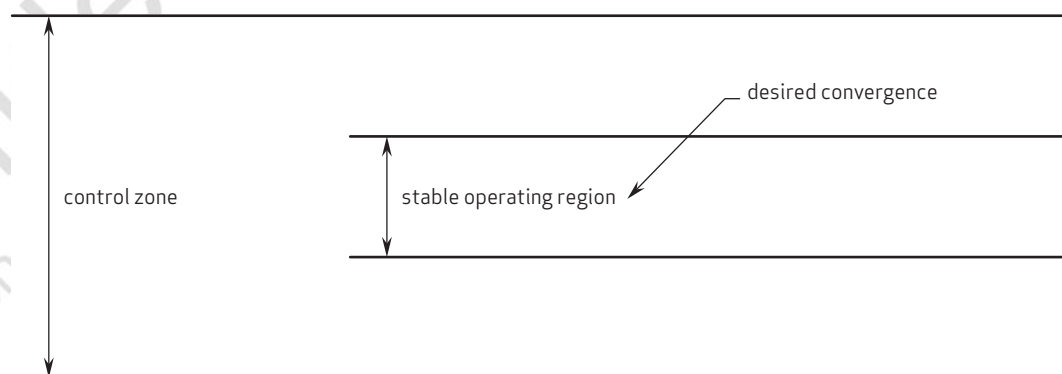
As for auto mode, the AEC will automatically calculate the steps needed based on the difference between target and current values. So, the outer control zone is meaningless for this mode.

table 4-5   AEC/AGC control

address	register name	default value	R/W	description
0x3A0F	AEC CTRL0F	0x78	RW	Bit[7:0]: Upper bound of stable range (set 1)
0x3A10	AEC CTRL10	0x68	RW	Bit[7:0]: Lower bound of stable range (set 1)
0x3A11	AEC CTRL11	0xD0	RW	Bit[7:0]: Upper bound of the range to determine step value in manual step calculation
0x3A1B	AEC CTRL1B	0x78	RW	Bit[7:0]: Upper bound of stable range (set 2)
0x3A1E	AEC CTRL1E	0x68	RW	Bit[7:0]: Lower bound of stable range (set 2)
0x3A1F	AEC CTRL1F	0x40	RW	Bit[7:0]: Lower bound of the range to determine step value in manual step calculation
0x5237	AVG READOUT	–	R	Bit[7:0]: Image average readout

For the average-based AEC/AGC algorithm, the measured window is divided by sixteen (4x4) zones (see average-based window definition). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones. average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. The AVG window is full image automatically. Also there is manual mode to set window, by manually setting x_start, x_end, y_start, and y_end as shown in average-based window definition, a 4x4 grid average window is defined. It will automatically divide each zone into 4x4 zones. The average value is the weighted average of the 16 sections lists the corresponding registers.

4.4.2.1 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting HS, VS, HW, and VH as shown in **figure 4-6**, a 4x4 grid window is defined. The value is the weighted average of the 16 sections. **table 4-6** lists the corresponding registers.

figure 4-6   average-based window definition
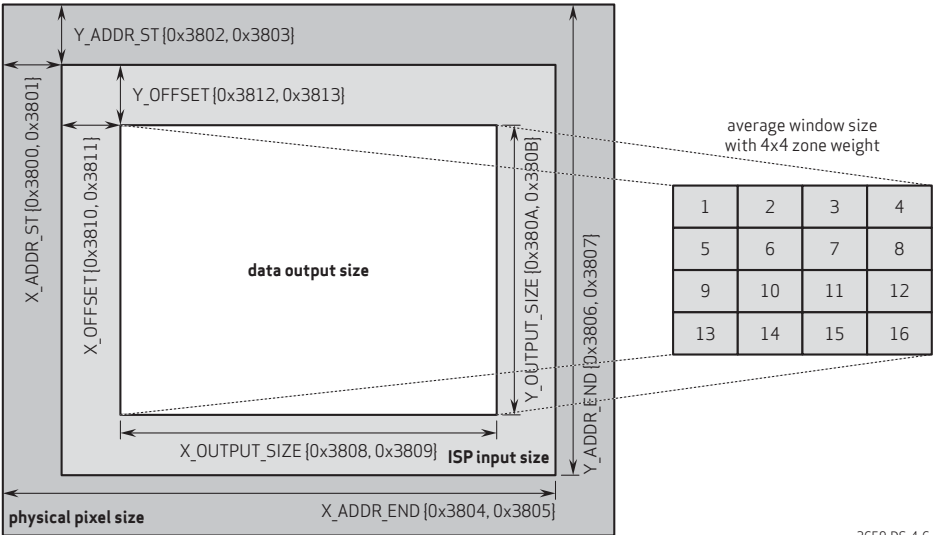
2659_DS_4_6

table 4-6   image size control

address	register name	default value	R/W	description
0x3810	TIMING HOFFSET	0x00	RW	Bit[2:0]: ISP horizontal offset[10:8]
0x3811	TIMING HOFFSET	0x04	RW	Bit[7:0]: ISP Horizontal offset[7:0]
0x3812	TIMING VOFFSET	0x11	RW	Bit[2:0]: ISP vertical offset[10:8]
0x3813	TIMING VOFFSET	0x11	RW	Bit[7:0]: ISP vertical offset[7:0]
0x3808	TIMING DVPHO	0x07	RW	Bit[2:0]: DVP output horizontal width[10:8]
0x3809	TIMING DVPHO	0x98	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x0B	RW	Bit[2:0]: DVP output vertical height[10:8]
0x380B	TIMING DVPVO	0x1C	RW	Bit[7:0]: DVP output vertical height[7:0]

<table 4-7>

table 4-7   average control

address	register name	default value	R/W	description
0x5060	AVG CONTROL 00	0x55	RW	Bit[7:6]: Average weight00 Bit[5:4]: Average weight01 Bit[3:2]: Average weight02 Bit[1:0]: Average weight03
0x5061	AVG CONTROL 01	0x55	RW	Bit[7:6]: Average weight10 Bit[5:4]: Average weight11 Bit[3:2]: Average weight12 Bit[1:0]: Average weight13
0x5062	AVG CONTROL 02	0x55	RW	Bit[7:6]: Average weight20 Bit[5:4]: Average weight21 Bit[3:2]: Average weight22 Bit[1:0]: Average weight23
0x5063	AVG CONTROL 03	0x55	RW	Bit[7:6]: Average weight30 Bit[5:4]: Average weight31 Bit[3:2]: Average weight32 Bit[1:0]: Average weight33

4.5 AEC/AGC steps

The AEC and AGC work together to obtain adequate exposure/gain based on the current environmental illumination. In order to achieve the best SNR, extending the exposure time is always preferred to raising the analog gain when the current illumination is going brighter. Vice versa, under bright conditions, the action to decrease the gain is always taken prior to shorten the exposure time.

4.5.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row period. In extremely dark situations, the VAEC activates, allowing integration time to be larger than one frame period.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall in some bands.

4.5.1.1 LAEC

If the integration time is only one row period but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to the minimum of 1/16 row. LAEC ON/OFF can be set in register bit 0x3A00[6].

4.5.1.2 banding mode ON with AEC

In Banding ON mode, the exposure time will fall in steps of integer multiples of the period of light intensity. This design is to reject image flickering when the light source is not steady but periodical.

For a given light flickering frequency, the band step can be expressed in units of row period.

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'.

The band steps for 50Hz and 60Hz light sources can be set in registers {0x3A08[1:0], 0x3A09[7:0]} and {0x3A0A[1:0], 0x3A0B[7:0]}, respectively. Use 0x3A05[7] to select 50 Hz (1'b0) or 60 Hz (1'b1).

When auto-banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto-banding is disabled, the minimum integration time is one band step. Auto banding can be set in register bit 0x3A00[4].

4.5.1.3 banding mode OFF with AEC

When Banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode or becomes twice/half of the previous step in fast mode.

4.5.1.4 night mode

The OV2659 supports long integration time such as 1 frame, 2 frames, 3 frames, 4 frames, 5 frames, 6 frames, 7 frames, and 8 frames in dark conditions. This is achieved by slowing down the original frame rate and waiting for exposure. Night mode ceiling can be set in register bits {0x3A02[7:0], 0x3A03[7:0]}. Night mode can be disabled by setting register bit 0x3A00[2] to 0. Also, when in night mode, the increase and decrease step can be based on band or frames, depending on register 0x3A05[6]. The minimum increase/decrease step can be one band. The step can be based both on bands and frames.

4.5.1.5 manual exposure control

To manually change exposure value, you must first set both 0x3503[0] and 0x3503[1], where 0x3503[0] enables manual exposure control and 0x3503[1] enables manual frame length - the number of lines in each frame or maximum exposure time, which is defined by registers {0x380E,0x380F}+{0x3506,0x3507}. In auto exposure mode, the extra exposure values (larger than 1 frame) in registers 0x3506/0x3507 automatically change. In manual exposure mode, these registers will not automatically change. The manually set exposure in registers 0x3500~0x03502 must be less than the maximum exposure value in {0x380E,0x380F}+{0x3506,0x3507}. The exposure value in registers 0x3500~0x3502 is in units of line*16 - the low 4 bits (0x3502[3:0]) is the fraction of line, the maximum value in {0x380E+0x380F}+{0x3506,0x3507} is in unit of line. If the manually set exposure value is less than one pre-defined frame period (e.g., 1/15 second in 15 fps), there is no need to change 0x380E/0x380F. If the exposure value needs to be set beyond the pre-defined frame period; in other words, if the frame period needs to be extended to extend exposure time, then the maximum frame value in 0x380E/0x380F needs to be set first, then the exposure can be set in registers 0x3500~0x3502 accordingly.

4.5.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise. Thus, AGC usually starts after AEC is full. However, in cases where adjacent AEC step changes are too large (>1/16), AGC steps should be inserted in between; otherwise, the integration time will keep switching between two adjacent steps and the image flickers.

4.5.2.1 integration time between 1~16 rows
When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between.

4.5.2.2 gain insertion between AEC banding steps
When banding mode is ON, the integration time changes in step of the period of light intensity. For the first 16 band steps, since the exposure time change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.5.2.3 gain insertion between night mode steps
Between night mode steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16.

4.5.2.4 when AEC reaches maximum
When AEC reaches its maximum while the image is still too dark, the gain starts to increase until the new frame average falls into the stable range or AGC reaches its maximum. The AGC ceiling can be set in {0x3A18[9:8], 0x3A19[7:0]}.

4.5.2.5 manual gain control
To manually change gain, first set register bit 0x3503[1] to enable manual control, then change the values in 0x350A/0x350B for the manual gain. The OV2659 has a maximum of 64x gain.

4.6 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration. There are three main functions of the BLC:

- adjusting all normal pixel values based on the values of the black levels
- applying multiplication to all pixel values based on digital gain

Black level adjustments can be made with registers 0x4000 through 0x401E.

table 4-8   BLC control

address	register name	default value	R/W	description
0x4000	BLC CONTROL 00	0x89	RW	Bit[0]: Offset compensation enable 0: Disable 1: Enable
0x4001	BLC START LINE	0x00	RW	Bit[5:0]: BLC start line
0x4002	BLC CONTROL 02	0x45	RW	Bit[7]: Format change enable 0: Disable 1: Enable
0x4003	BLC CONTROL 03	0x08	RW	Bit[7]: BLC redo enable Set to 1 will trigger a BLC redo n frames begin Bit[6]: BLC freeze Bit[5:0]: Manual frame number
0x4004	BLC LINE NUMBER	0x08	RW	Bit[5:0]: BLC line number
0x4009	BLC TARGET	0x10	RW	Black Target Level

4.7 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

5 image sensor processor digital functions

5.1 ISP_TOP

The ISP_TOP includes all module enable signals, buffer power down and cen control, top level control signals as well as ISP modules that require control bytes (DPC, UV_AVG, and pre-ISP).

- DPC: Defective Pixel Canceling is used to detect and remove white and black defect pixels.
- UV_AVG: U and V average module is used to smooth chrominance to let color image looks better around edge. It has two options to do: average with five consecutive U or V and get median value from five consecutive U or V.
- pre-ISP: This module is used to latch data, crop window, append dummy lines and create pixel order signal for ISP data path. It can also generate some test patterns for debug, such as color bar, color or black square block and random image.

table 5-1   ISP TOP control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xFB	RW	Bit[7]: ISP enable 0: Disable 1: Enable Bit[6]: Raw gamma enable 0: Disable 1: Enable Bit[5]: AWB statistic enable 0: Disable 1: Enable Bit[4]: AWB gain enable 0: Disable 1: Enable Bit[3]: LENC enable 0: Disable 1: Enable Bit[2]: LCD adjustment enable 0: Disable 1: Enable Bit[1]: Black pixel canceling enable 0: Disable 1: Enable Bit[0]: White pixel canceling enable 0: Disable 1: Enable

table 5-1   ISP TOP control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x17	RW	Bit[5]: UV average selection Bit[4]: LENC gain enable 0: Disable 1: Enable Bit[3]: special digital effect enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Color interpolation enable 0: Disable 1: Enable
0x5002	ISP CONTROL 02	0x00	RW	Bit[4]: Scale enable 0: Disable 1: Enable
0x5007	ISP CONTROL 07	0x3F	RW	Bit[7:6]: Reserved Bit[5]: LENC bias plus Bit[4]: LENC bias on Bit[3]: Gamma bias plus Bit[2]: Gamma bias on Bit[1]: LCD bias plus Bit[0]: LCD bias on
0x50A0	PRE ISP CTRL00	0x00	RW	Bit[7]: ISP test enable Bit[6]: ISP test - rolling horizontal bar enable Bit[5]: ISP test - test image plus real image Bit[4]: Reserved Bit[3:2]: Color bar style 00: Normal bar 01: Vertical changed bar 10: Horizontal changed bar style 1 11: Horizontal changed bar style 2

5.2 lens correction (LENC)

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens center, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

table 5-2 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x500C	LENC RED X0	0x03	RW	Bit[2:0]: LENC red pixel x0[10:8]
0x500D	LENC RED X0	0x30	RW	Bit[7:0]: LENC red pixel x0[7:0]
0x500E	LENC RED Y0	0x02	RW	Bit[2:0]: LENC red pixel y0[10:8]
0x500F	LENC RED Y0	0x5C	RW	Bit[7:0]: LENC red pixel y0[7:0]
0x5010	LENC RED A1	0x00	RW	Bit[6:0]: LENC red pixel a1
0x5011	LENC RED B1	0x00	RW	Bit[7:0]: LENC red pixel b1
0x5012	LENC RED A2 AND B2	0xFF	RW	Bit[7:4]: LENC red pixel b2 Bit[3:0]: LENC red pixel a2
0x5013	LENC GREEN X0	0x03	RW	Bit[2:0]: LENC green pixel x0[10:8]
0x5014	LENC GREEN X0	0x30	RW	Bit[7:0]: LENC green pixel x0[7:0]
0x5015	LENC GREEN Y0	0x02	RW	Bit[2:0]: LENC green pixel y0[10:8]
0x5016	LENC GREEN Y0	0x5C	RW	Bit[7:0]: LENC green pixel y0[7:0]
0x5017	LENC GREEN A1	0x00	RW	Bit[6:0]: LENC green pixel a1
0x5018	LENC GREEN B1	0x00	RW	Bit[7:0]: LENC green pixel b1
0x5019	LENC GREEN A2 AND B2	0xFF	RW	Bit[7:4]: LENC green pixel b2 Bit[3:0]: LENC green pixel a2
0x501A	LENC BLUE X0	0x03	RW	Bit[2:0]: LENC blue pixel x0[10:8]
0x501B	LENC BLUE X0	0x30	RW	Bit[7:0]: LENC blue pixel x0[7:0]
0x501C	LENC BLUE Y0	0x02	RW	Bit[2:0]: LENC blue pixel y0[10:8]
0x501D	LENC BLUE Y0	0x5C	RW	Bit[7:0]: LENC blue pixel y0[7:0]
0x501E	LENC BLUE A1	0x00	RW	Bit[6:0]: LENC blue pixel a1
0x501F	LENC BLUE B1	0x00	RW	Bit[7:0]: LENC blue pixel b1
0x5020	LENC BLUE A2 AND B2	0xFF	RW	Bit[7:4]: LENC blue pixel b2 Bit[3:0]: LENC blue pixel a2
0x5021	LENC CONTROL 00	0x0C	RW	Bit[4:0]: LENC gain high threshold

table 5-2   LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5022	LENC CONTROL 01	0x06	RW	Bit[7]: LENC gain coefficient manual enable 0: Disable 1: Enable Bit[4:0]: LENC gain low threshold
0x5023	COEFFICIENT THRESHOLD	0x80	RW	Bit[7:0]: LENC coefficient threshold
0x5024	COEFFICIENT MANUAL VALUE	0x80	RW	Bit[7:0]: LENC coefficient manual value

5.3 gamma

Gamma converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

table 5-3   gamma control

address	register name	default value	R/W	description
0x5025	GAMMA YST1	0x05	RW	Bit[7:0]: Gamma yst1
0x5026	GAMMA YST2	0x0C	RW	Bit[7:0]: Gamma yst2
0x5027	GAMMA YST3	0x1C	RW	Bit[7:0]: Gamma yst3
0x5028	GAMMA YST4	0x2A	RW	Bit[7:0]: Gamma yst4
0x5029	GAMMA YST5	0x39	RW	Bit[7:0]: Gamma yst5
0x502A	GAMMA YST6	0x45	RW	Bit[7:0]: Gamma yst6
0x502B	GAMMA YST7	0x52	RW	Bit[7:0]: Gamma yst7
0x502C	GAMMA YST8	0x5D	RW	Bit[7:0]: Gamma yst8
0x502D	GAMMA YST9	0x68	RW	Bit[7:0]: Gamma yst9
0x502E	GAMMA YST10	0x7F	RW	Bit[7:0]: Gamma yst10
0x502F	GAMMA YST11	0x91	RW	Bit[7:0]: Gamma yst11
0x5030	GAMMA YST12	0xA5	RW	Bit[7:0]: Gamma yst12
0x5031	GAMMA YST13	0xC6	RW	Bit[7:0]: Gamma yst13
0x5032	GAMMA YST14	0xDE	RW	Bit[7:0]: Gamma yst14
0x5033	GAMMA YST15	0xEF	RW	Bit[7:0]: Gamma yst15
0x5034	GAMMA YSLP	0x16	RW	Bit[7:0]: Gamma yslp

5.4 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. There are two main functions AWB: AWB_stat and AWB_gain.

- AWB_stat is used to automatically generate digital gain for different light sources
- AWB_gain is used to apply the AWB_stat gain information on RAW data to remove unrealistic color

table 5-4 AWB control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5035	AWB CONTROL 00	0x5C	RW	Bit[7:6]: AWB step fast (when sub register 0x5037[7] = 1) Bit[5:4]: AWB step local Bit[3]: AWB g enable Bit[2]: AWB simple mode 　0: Advance mode 　1: Simple mode Bit[1] AWB one zone mode Bit[0]: AWB average all mode
0x5036	AWB CONTROL 01	0x00	RW	Bit[7:4]: Max fast count (when sub register 0x5037[7] = 1) Bit[3:0]: Max local count
0x5037	AWB CONTROL 02	0x92	RW	Bit[7]: AWB fast enable 　0: Disable 　1: Enable Bit[6:4]: AWB count limit control Bit[3:0]: AWB stable range
0x5038	AWB CONTROL 03	0x21	RW	Bit[7:6]: AWB count area select Bit[5]: AWB sim select 　0: After AWB gain 　1: After gamma Bit[4]: AWB rblue Bit[3]: AWB slope 8x Bit[2]: AWB slope 4x Bit[1:0]: AWB count threshold
0x5039	AWB CONTROL 04	0x70	RW	Bit[7]: AWB simf Bit[6]: AWB bias plus Bit[5]: AWB bias on Bit[4]: AWB bias statistics Bit[3]: AWB freeze Bit[2]: AWB preset Bit[1:0]: AWB window mode
0x503A	AWB LOCAL LIMIT	0x02	RW	Bit[7:0]: AWB local limit
0x503C~ 0x5048	AWB CONTROL	–	RW	Advanced AWB Control Registers

table 5-4   AWB control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5049	AWB CONTROL 12	0xF0	RW	Bit[7:0]: AWB red gain limit
0x504A	AWB CONTROL 13	0xF0	RW	Bit[7:0]: AWB green gain limit
0x504B	AWB CONTROL 14	0xF0	RW	Bit[7:0]: AWB blue gain limit
0x3400	AWB R GAIN	0x04	RW	Bit[3:0]: AWB R GAIN[11:8]
0x3401	AWB R GAIN	0x00	RW	Bit[7:0]: AWB R GAIN[7:0]
0x3402	AWB G GAIN	0x04	RW	Bit[3:0]: AWB G GAIN[11:8]
0x3403	AWB G GAIN	0x00	RW	Bit[7:0]: AWB G GAIN[7:0]
0x3404	AWB B GAIN	0x04	RW	Bit[3:0]: AWB B GAIN[11:8]
0x3405	AWB B GAIN	0x00	RW	Bit[7:0]: AWB B GAIN[7:0]
0x3406	AWb MANUAL CONTROL	0x00	RW	Bit[0]: AWB gain manual enable 0: Auto 1: Manual

5.5 defect pixel canceling (DPC)

The main purpose of the Defect Pixel Canceling (DPC) function is to automatically remove the white and black defect pixels in the image.

table 5-5   DPC control

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xFB	RW	Bit[1]: Black pixel canceling enable 0: Disable 1: Enable Bit[0]: White pixel canceling enable 0: Disable 1: Enable
0x5054	DPC CTRL 00	0x1C	RW	Bit[7:0]: Debug control Changing these register bits is not recommended

5.6 Y average

The main purpose of the Y average function is to calculate the Y average weighted by 16 zones for Y contrast function in the SDE module. Refer to **figure 4-6** for the definition of the 16 zones.

table 5-6   average control

address	register name	default value	R/W	description
0x5060	AVG CONTROL 00	0x55	RW	Bit[7:6]: Average weight00 Bit[5:4]: Average weight01 Bit[3:2]: Average weight02 Bit[1:0]: Average weight03
0x5061	AVG CONTROL 01	0x55	RW	Bit[7:6]: Average weight10 Bit[5:4]: Average weight11 Bit[3:2]: Average weight12 Bit[1:0]: Average weight13
0x5062	AVG CONTROL 02	0x55	RW	Bit[7:6]: Average weight20 Bit[5:4]: Average weight21 Bit[3:2]: Average weight22 Bit[1:0]: Average weight23
0x5063	AVG CONTROL 03	0x55	RW	Bit[7:6]: Average weight30 Bit[5:4]: Average weight31 Bit[3:2]: Average weight32 Bit[1:0]: Average weight33
0x5237	AVG READOUT	–	R	Bit[7:0]: Image average readout

5.7 color interpolation (CIP), DNS and sharpen

The color interpolation (CIP) functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

figure 5-1   DNS_TH diagram

2659_DS_5_1

figure 5-2   sharpen_MT diagram

2659_DS_5_2

figure 5-3   sharpen_TH diagram

2659_DS_5_3

table 5-7   CIP/DNS/sharpen control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5064	SHARPENMT THRESHOLD1	0x08	RW	Bit[7:0]: Sharpenmt threshold1 Low gain threshold for calculating sharpen strength automatically, T1<T2)
0x5065	SHARPENMT THRESHOLD2	0x48	RW	Bit[7:0]: Sharpenmt threshold2 High gain threshold for calculating sharpen strength automatically, T1<T2)
0x5066	SHARPENMT OFFSET1	0x18	RW	Bit[6:0]: Sharpenmt offset1[6:0] / MANUAL SHARPEN THRESHOLD Maximum sharpen strength in auto mode, shared with manual sharpen strength
0x5067	SHARPENMT OFFSET2	0x0E	RW	Bit[6:0]: Sharpenmt offset2 Minimum sharpen strength in auto mode, Offset1>Offset2
0x5068	DENOISE THRESHOLD1	0x08	RW	Bit[7:0]: Denoise threshold1 Low gain threshold for calculating denoise threshold automatically, T1<T2
0x5069	DENOISE THRESHOLD2	0x48	RW	Bit[7:0]: Denoise threshold2 High gain threshold for calculating denoise threshold automatically, T1<T2

table 5-7   CIP/DNS/sharpen control (sheet 2 of 2)

address	register name	default value	R/W	description	
0x506A	DENOISE OFFSET1	0x09	RW	Bit[6:0]:	Denoise offset1/ MANUAL DNS THRESHOLD Maximum denoise threshold in auto mode, shared with manual denoise threshold
0x506B	DENOISE OFFSET2	0x16	RW	Bit[6:0]:	Denoise offset2
0x506C	SHARPEN THRESHOLD1	0x08	RW	Bit[7:0]:	Sharpen threshold1 Low gain threshold for calculating sharpen threshold automatically, T1 < T2
0x506D	SHARPEN THRESHOLD2	0x48	RW	Bit[7:0]:	Sharpen threshold2 High gain threshold for calculating sharpen threshold automatically, T1<T2
0x506E	CIP CONTROL 00	0x44	RW	Bit[7]: Bit[5]: Bit[4:0]:	CIP edge mt manual enable 0: Disable 1: Enable CIP denoise manual enable 0: Disable 1: Enable Sharpen offset1/ MANUAL SHARPENTH THRESHOLD Maximum sharpen threshold in auto mode, shared with manual sharpen threshold
0x506F	CIP CONTROL 01	0xA	RW	Bit[7:5]: Bit[4:0]:	Threshold RB sharpen Sharpen offset2 Minimum sharpen threshold in auto mode, Offset1<Offset2

5.8 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to convert images from the RGB domain to YUV domain.

table 5-8   CMX control

address	register name	default value	R/W	description
0x5070	CMX1	0x33	RW	Bit[7:0]: CMX1
0x5071	CMX2	0x41	RW	Bit[7:0]: CMX2
0x5072	CMX3	0x0F	RW	Bit[7:0]: CMX3
0x5073	CMX4	0x0B	RW	Bit[7:0]: CMX4
0x5074	CMX5	0x44	RW	Bit[7:0]: CMX5
0x5075	CMX6	0x50	RW	Bit[7:0]: CMX6
0x5076	CMX7	0x55	RW	Bit[7:0]: CMX7
0x5077	CMX8	0x3A	RW	Bit[7:0]: CMX8
0x5078	CMX9	0x1C	RW	Bit[7:0]: CMX9
0x5079	CMX SIGN	0x98	RW	Bit[7:0]: CMX sign for CMX1 ~ CMX8
0x507A	CMX CTRL 00	0x21	RW	Bit[7:2]: Reserved Bit[1]: CMX double Bit[0]: CMX sign for CMX9

5.9 special digital effects (SDE) and UV adjust (UV_ADJ)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V manually using the Sat_u and Sat_v registers. The UV adjust module is merged with the saturate UV function. Calculate Y using Y offset, Y gain, and Y bright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, reddish and other image effects which combine the effects already listed.

UV adjust (UV_ADJ) is used to reduce chrominance values in low light conditions to improve image quality. The higher AGC gain is, the lower the chrominance values. UV_ADJ has an automatic and manual mode, where the latter is equal to the above manual UV saturation.

figure 5-4   UV adjust value diagram

table 5-9   SDE control

address	register name	default value	R/W	description	
0x507A	MISC CTRL 00	0x21	RW	Bit[5]:	UV adjustment threshold2[8]
0x507B	SDE CTRL 00	0x00	RW	Bit[7]: Bit[6]: Bit[5]: Bit[4]: Bit[3]: Bit[2]: Bit[1]: Bit[0]:	Fixed Y Negative Black and white Fixed U Fixed V Y contrast enable 0: Disable 1: Enable Saturate enable 0: Disable 1: Enable Hue enable 0: Disable 1: Enable
0x507C	SDE CTRL 01	0x80	RW	Bit[7:0]:	Hue cosine
0x507D	SDE CTRL 02	0x00	RW	Bit[7:0]:	Hue sine
0x507E	SDE CTRL 03	0x40	RW	Bit[7:0]:	Adjust value1 Manual saturate U or fixed U
0x507F	SDE CTRL 04	0x00	RW	Bit[7:0]:	Adjust value2 Manual saturate V or fixed V
0x5080	SDE CTRL 05	0x00	RW	Bit[7:0]:	Manual Y offset
0x5081	SDE CTRL 06	0x20	RW	Bit[7:0]:	Y contrast gain 0x20: 1x
0x5082	SDE CTRL 07	0x00	RW	Bit[7:0]:	Y brightness
0x5083	SDE CTRL 08	0x01	RW	Bit[5:0]:	Sign set Hue: SGN0=1, SGN1=0, SGN4=SGN5=0 => $0<q<p/2$ SGN0=0, SGN1=1, SGN4=SGN5=0 => $-p/2<q<0$ SGN0=1, SGN1=0, SGN4=SGN5=1 => $-p/2<q<p$ SGN0=0, SGN1=1, SGN4=SGN5=1 => $-p<q<-p/2$ Y_contrast: SGN2: YOFFSET SGN3: YBRIGHTNESS
0x5084	SDE CTRL 09	0x10	RW	Bit[7:0]:	UV adjustment threshold1
0x5085	SDE CTRL 0A	0x00	RW	Bit[7:0]:	UV adjustment threshold2[7:0]

5.10 scaling

The main purpose of the scaling function is to zoom out the image. According to the new width and height of the new image, the module uses the values of several adjacent pixels to generate the values of one pixel. The scaling function supports up to 32x scaling, see **table 5-10**.

table 5-10   scale control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5600	SCALE CTRL 0	0x10	RW	Bit[6]: Vfirst 0: Select the second U and first V in YUV444to422 module 1: Select the first U and second V in YUV444to422 module Bit[5]: uv_drop YUV444to422 drop mode or average mode selection 0: Average mode 1: Drop mode Bit[4]: Auto mode Scale auto or manual mode selection 0: Manual mode 1: Auto mode Bit[3]: Hround 0: No horizontal rounding 1: Horizontal rounding in average mode Bit[2]: Hdrop 0: Horizontal average mode 1: Horizontal drop mode Bit[1]: Vround 0: No vertical rounding 1: Vertical rounding in average mode Bit[0]: Vdrop 0: Vertical average mode 1: Vertical drop mode

table 5-10   scale control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5601	SCALE CTRL 1	0x00	RW	Bit[7]: Debug mode Bit[6:4]: Hdiv Horizontal DCW scale times 000: DCW 1 time 001: DCW 2 times 010: DCW 4 times 011: DCW 8 times 100: DCW 16 times others: DCW 16 times Bit[2:0]: Vdiv Vertical DCW scale times 000: DCW 1 time 001: DCW 2 times 010: DCW 4 times 011: DCW 8 times 100: DCW 16 times others: DCW 16 times
0x5602	XSC HIGH	0x02	RW	Bit[7:2]: Debug mode Bit[1:0]: XSC[9:8]
0x5603	XSC LOW	0x00	RW	Bit[7:0]: XSC[7:0]
0x5604	YSC HIGH	0x02	RW	Bit[7:2]: Debug mode Bit[1:0]: YSC[9:8]
0x5605	YSC LOW	0x00	RW	Bit[7:0]: YSC[7:0]
0x5606	VOFFSET	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Voffset Select which line to output in vertical drop mode

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported, and extended features including test pattern output.

table 6-1   DVP control registers

address	register name	default value	R/W	description
0x4704	DVP CTRL01	0x00	RW	Bit[3:2]: VSYNC output mode select Bit[1]: VSYNC3 mode enable VSYNC generate by EOF, unset by first internal HREF Bit[0]: VSYNC2 mode enable VSYNC generated by EOF Width controlled by register Default VSYNC1 mode enable VSYNC generate by SOF Width controlled by register
0x4708	DVP CTRL02	0x01	RW	Bit[5]: VSYNC gate clock enable Bit[4]: HREF gate clock enable Bit[2]: HREF polarity Bit[1]: VSYNC polarity Bit[0]: PCLK gate low enable
0x4709	DVP CTRL03	0x00	RW	Bit[7]: Video FIFO bypass mode Bit[6:4]: Data bit swap 000: Output data is the same order as input, that is [9:0] 001: Output data is reversed, [0:9] 010: Output data is reorder as {[2:9], [1:0]} 011: Output data is reorder as {[7:0], [9:8]} 100: Output data is reorder as {[9:8], [0:7]} 101: Output data is reorder as {[9], [0:8]} 110: Output data is reorder as {[1:9], [0]} 111: Output data is reorder as {[8:0], [9]} Bit[3]: Test mode Bit[2]: Test mode 10-bit Bit[1]: Test mode 8-bit Bit[0]: Test mode enable

6.1.2 DVP timing

figure 6-1   DVP timing diagram

table 6-2   DVP timing specifications

mode	max frame rate	format	timing
UXGA 1600 x 1200	15 fps	RAW	(1) 2386366 tp (2) 528 tp (3) 13554 tp (4) 1948 tp (5) 49114 tp (6) 1600 tp (7) 348 tp
SVGA 800 x 600	30 fps	RAW	(1) 800800 tp (2) 528 tp (3) 3298 tp (4) 1300 tp (5) 17474 tp (6) 800 tp (7) 500 tp
720p 1280 x 720	30 fps	RAW	(1) 1199968 tp (2) 528 tp (3) 5754 tp (4) 1948 tp (5) 26546 tp (6) 800 tp (7) 1148 tp

6.1.3 DVP image formats

6.1.3.1 YUV422 format

Uncompressed YUV422 data is sent out through D[9:2] and the sequence can be YUYV, UYVY, YVYU, VYUY.

6.1.3.2 RGB565 format

Uncompressed RGB565 data is sent out through D[9:2].

table 6-3   RGB565 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	G2	B7	B6	B5	B4	B3

6.1.3.3 RGB555 format

table 6-4   RGB555 format

bytes	D9	D8	D7	D6	D	D4	D3	D2
even	0	R7	R6	R5	R4	R3	G7	G6
odd	G5	G4	G3	B7	B6	B5	B4	B3

The formats can be selected through register 0x4300.

table 6-5   format control register

address	register name	default value	R/W	description
0x4300	FORMAT CTRL00	0xF8	RW	Bit[7:4]: Output format selection 0x0: RAW 0x3: YUV422 0x4: YUV420 0x5: YUV420 legacy 0x6: RGB565 0x9: gb444 format1 0xF: byp_fmt Bit[3:0]: Pixel order control

6.1.4 data clipping

The OV2659 supports four options for data clipping. The option can be select though register 0x4301.

table 6-6   clipping control register

address	register name	default value	R/W	description
0x4301	CLIPPING CONTROL	0x00	RW	Bit[3:2]: Data limitation option 00: No limitation (0x000~0x3FF) 01: Limit data to 0x004~0x3FB 10: Limit data to 0x3F0~0x010 11: Limit data to 0x040~0x3C0 Bit[1:0]: YUV422 UV control 00: U/V generate from average 01: U/V generate from 1st pixel 11: U/V generate from 2nd pixel

7   register tables

The following tables provide descriptions of the device control registers contained in the OV2659. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x60 for write and 0x61 for read.

table 7-1   I/O control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0100	SOFTWARE STANDBY	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Software standby 0: Software standby 1: Streaming
0x0103	SOFTWARE RESET	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Software reset 1: Reset
0x3011	OUTPUT DRIVE CAPABILITY CTRL	0x02	RW	Pad Control Bit[7:6]: Output drive capability for PCLK, VSYNC, HREF, D[9:0] 00: 1x 01: 2x 10: 3x 11: 4x Bit[5:0]: Not used
0x3000	IO CTRL00	0x00	RW	GPIO Direction Control (0: input; 1: output) Bit[7:2]: Debug mode Bit[1:0]: DVP D[9:8] output enable
0x3001	IO CTRL01	0x00	RW	GPIO Direction Control (0: input; 1: output) Bit[7:0]: DVP D[7:0] output enable
0x3002	IO CTRL02	0x00	RW	GPIO Direction Control (0: input; 1: output) Bit[7]: VSYNC output enable Bit[6]: HREF output enable Bit[5]: PCLK output enable Bit[4:0]: Debug mode
0x3003~0x3007	DEBUG MODE	–	–	Debug Mode
0x3008	OUTPUT VALUE00	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: DVP D[9:8] value for output
0x3009	OUTPUT VALUE01	0x00	RW	Bit[7:0]: DVP D[7:0] value for output
0x300A~0x300C	DEBUG MODE	–	–	Debug Mode
0x300D	OUTPUT VALUE02	0x00	RW	Bit[7]: VSYNC value for output Bit[6]: HREF value for output Bit[5]: PCLK value for output Bit[4:0]: Debug mode

table 7-1 I/O control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x300E	OUTPUT SELECT00	0x00	RW	GPIO Output Select (0: select DVP; 1: select from registers) Bit[7:2]: Debug mode Bit[1:0]: DVP D[9:8] output select
0x300F	OUTPUT SELECT01	0x00	RW	GPIO Output Select (0: select DVP; 1: select from registers) Bit[7:0]: DVP D[7:0] output select
0x3010	OUTPUT SELECT02	0x00	RW	GPIO Output Select (0: select DVP; 1: select from registers) Bit[7]: VSYNC output select Bit[6]: HREF output select Bit[5]: PCLK output select Bit[4:0]: Debug mode
0x3011~ 0x3022	DEBUG MODE	–	–	Debug Mode
0x3024~ 0x302C	DEBUG MODE	–	–	Debug Mode
0x302D	INPUT READOUT00	–	R	Bit[7:2]: Debug mode Bit[1]: TM input readout Bit[0]: PWDN input readout
0x302E	INPUT READOUT01	–	R	Bit[7]: Debug mode Bit[6]: SIOC input readout Bit[5]: SIOD input readout Bit[4]: VSYNC input readout Bit[3]: HREF input readout Bit[2]: PCLK input readout Bit[1:0]: DVP D[9:8] input readout
0x302F	INPUT READOUT02	–	R	Bit[7:0]: DVP D[7:0] input readout

table 7-2   system registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3014	SC CMMN PWC	0x00	RW	Bit[7:6]: Debug mode Bit[5]: Bypass regulator Bit[4:0]: Debug mode
0x301A	SC CMMN CLKRST0	0x00	RW	For clock: (0: disable; 1: enable clock) For reset: (0: disable; 1: enable reset) Bit[7:2]: Debug mode Bit[1]: AEC reset Bit[0]: TC reset
0x301B	SC CMMN CLKRST1	0x00	RW	For reset: (0: disable; 1: enable reset) Bit[7:4]: Debug mode Bit[3]: BLC reset Bit[2]: ISP reset Bit[1]: AVG reset Bit[0]: VFIFO reset
0x301C	SC CMMN CLKRST2	0x00	RW	For reset: (0: disable; 1: enable reset) Bit[7:4]: Debug mode Bit[3]: DVP reset Bit[2]: Not used Bit[1]: Sensor sync reset Bit[0]: Not used
0x301D	SC CMMN CLKRST3	0x00	RW	For reset: (0: disable; 1: enable reset) Bit[7:4]: Debug mode Bit[3]: ISP frame control reset Bit[2]: Group hold reset Bit[1]: BIST reset Bit[0]: AC reset
0x301E~ 0x3029	DEBUG MODE	–	–	Debug Mode
0x302A	SC CMMN SUB ID	0x00	RW	Bit[7:4]: Process number Bit[3:0]: Revision number
0x302B	SC CMMN SCCB ID	0x60	RW	SCCB ID
0x300A	SC CMMN CHIP ID	0x26	R	CHIP ID High Byte (see **sidebar note**)
0x300B	SC CMMN CHIP ID	0x56	R	CHIP ID Low Byte (see **sidebar note**)

note

The part ID 0x2656 could be confused with the second revision of the OV2655. The OV2656 has since been officially changed to part ID OV2659. This change to OV2659 was implemented after the physical silicon was assembled.

Please contact your local OmniVision FAE support team, should this raise concern in your design process.

table 7-2   system registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3003	SC CMMN PLL CTRL0	0x00	RW	Bit[7:6]: Frequency divider 　　00: Bypass 　　01: Div 1.5x 　　10: Div 2x 　　11: Div 3x Bit[5:3]: PLL charge pump Bit[2]: Debug mode Bit[1:0]: Bit 8 divider 　　00: Bypass 　　01: Div 1x 　　10: Div 4x 　　11: Div 5x
0x3004	SC CMMN PLL CTRL1	0x10	RW	Bit[7:4]: System divider 　　Real divide ratio = 2 x bit[7:4] Bit[3:0]: Scale divider
0x3005	SC CMMN PLL CTRL2	0x24	RW	Bit[7]: PLL_bypass Bit[6]: Debug mode Bit[5:0]: Multiplier
0x3006	SC CMMN PLL CTR13	0x0D	RW	Bit[7:5]: Debug mode Bit[4:3]: System divider 　　00: Div 1x 　　01: Div 2x 　　10: Div 8x 　　11: Div 16x Bit[2:0]: Pre-divider 　　000: 1x 　　001: 1.5x 　　010: 2x 　　011: 3x 　　100: 2x 　　101: 3x 　　110: 4x 　　111: 6x

table 7-3   group hold/write function control (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADDRESS 00	0x00	RW	SRAM Group Address 0
0x3201	GROUP ADDRESS 01	0x04	RW	SRAM Group Address 1
0x3202	GROUP ADDRESS 02	0x08	RW	SRAM Group Address 2
0x3203	GROUP ADDRESS 03	0x0B	RW	SRAM Group Address 3

table 7-3   group hold/write function control (sheet 2 of 2)

address	register name	default value	R/W	description
0x3204~ 0x3207	DEBUG MODE	–	–	Debug Mode
0x3208	GROUP ACCESS	–	W	Bit[7:4]: Group control 0000: Group hold start 0001: Group hold end 1010: Group launch others: Debug mode Bit[3:0]: Group ID 0000: Group bank 0 Default start from address 0x00 0001: Group bank 1 Default start from address 0x40 0010: Group bank 2 Default start from address 0x80 0011: Group bank 3 Default start from address 0xB0 others: Debug mode

table 7-4   AWB gain registers

address	register name	default value	R/W	description
0x3400	AWB R GAIN	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: AWB R GAIN[11:8]
0x3401	AWB R GAIN	0x00	RW	Bit[7:0]: AWB R GAIN[7:0]
0x3402	AWB G GAIN	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: AWB G GAIN[11:8]
0x3403	AWB G GAIN	0x00	RW	Bit[7:0]: AWB G GAIN[7:0]
0x3404	AWB B GAIN	0x04	RW	Bit[7:4]: Debug mode Bit[3:0]: AWB B GAIN[11:8]
0x3405	AWB B GAIN	0x00	RW	Bit[7:0]: AWB B GAIN[7:0]
0x3406	AWb MANUAL CONTROL	0x00	RW	Bit[7:1]: Debug mode Bit[0]: AWB gain manual enable 0: Auto 1: Manual

table 7-5   timing control (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: HREF horizontal start point[10:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: HREF horizontal start point[7:0]
0x3802	TIMING VS	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: HREF vertical start point[10:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: HREF vertical start point[7:0]
0x3804	TIMING HW	0x06	RW	Bit[7:3]: Debug mode Bit[2:0]: HREF horizontal width[10:8]
0x3805	TIMING HW	0x5F	RW	Bit[7:0]: HREF horizontal width[7:0]
0x3806	TIMING VH	0x04	RW	Bit[7:3]: Debug mode Bit[2:0]: HREF vertical height[10:8]
0x3807	TIMING VH	0xBB	RW	Bit[7:0]: HREF vertical height[7:0]
0x3808	TIMING DVPHO	0x06	RW	Bit[7:3]: Debug mode Bit[2:0]: DVP output horizontal width[10:8]
0x3809	TIMING DVPHO	0x40	RW	Bit[7:0]: DVP output horizontal width[7:0]
0x380A	TIMING DVPVO	0x04	RW	Bit[7:3]: Debug mode Bit[2:0]: DVP output vertical height[10:8]
0x380B	TIMING DVPVO	0xB0	RW	Bit[7:0]: DVP output vertical height[7:0]
0x380C	TIMING HTS	0x07	RW	Bit[7:0]: Total horizontal size[15:8]
0x380D	TIMING HTS	0x9C	RW	Bit[7:0]: total horizontal size[7:0]
0x380E	TIMING VTS	0x04	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING VTS	0xD0	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING HOFFS	0x00	RW	Timing Control Register Bit[7:3]: Debug mode Bit[2:0]: ISP horizontal windowing offset[10:8]
0x3811	TIMING HOFFS	0x10	RW	Bit[7:0]: ISP horizontal windowing offset[7:0]
0x3812	TIMING VOFFS	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: ISP vertical windowing offset[10:8]
0x3813	TIMING VOFFS	0x06	RW	Bit[7:0]: ISP vertical windowing offset[7:0]
0x3814	TIMING XINC	0x11	RW	Timing Control Register Bit[7:4]: Horizontal odd increase number Bit[3:0]: Horizontal even increase number
0x3815	TIMING YINC	0x11	RW	Timing Control Register Bit[7:4]: Vertical odd increase number Bit[3:0]: Vertical even increase number
0x3816~0x381F	DEBUG MODE	–	–	Debug Mode

table 7-5   timing control (sheet 2 of 2)

address	register name	default value	R/W	description
0x3820	TIMING FORMAT	0x80	RW	Bit[7:3]: Debug mode Bit[2]: Vertical flip for digital Bit[1]: Vertical flip for array Bit[0]: Vertical binning enable
0x3821	TIMING FORMAT	0x00	RW	Bit[7:3]: Debug mode Bit[2]: Horizontal mirror for digital Bit[1]: Horizontal mirror for array Bit[0]: Horizontal binning enable

table 7-6   AEC/AGC control (sheet 1 of 5)

address	register name	default value	R/W	description

0x3500	AEC PK EXPOSURE	0x00	RW	Exposure Output
				    Bit[7:4]: Debug mode
				    Bit[3:0]: Exposure[19:16]

0x3501	AEC PK EXPOSURE	0x02	RW	Exposure Output Bit[7:0]: Exposure[15:8]
0x3502	AEC PK EXPOSURE	0x00	RW	Exposure Output Bit[7:0]: Exposure[7:0]

0x3503	AEC PK MANUAL	0x00	RW	AEC Manual Mode Control
				    Bit[7:6]: Debug mode
				    Bit[5]: Gain delay options
				        0: First frame latch
				        1: Delay 1 frame latch
				    Bit[4]: Choose delay option
				        0: Delay disable
				        1: Delay enable
				    Bit[3:2]: Debug mode
				    Bit[1]: AGC manual
				        0: Auto enable
				        1: Manual enable
				    Bit[0]: AEC manual
				        0: Auto enable
				        1: Manual enable

0x3504	AEC MANUAL SENSOR GAIN HIGH BYTE	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Manual sensor gain[9:8]
0x3505	AEC MANUAL SENSOR GAIN LOW BYTE	0x00	RW	Bit[7:0]: Manual sensor gain[7:0]
0x3506	AEC ADD VTS HIGH BYTE	0x00	RW	Bit[7:0]: AEC ADD VTS[15:8]
0x3507	AEC ADD VTS LOW BYTE	0x00	RW	Bit[7:0]: AEC ADD VTS[7:0]

table 7-6   AEC/AGC control (sheet 2 of 5)

address	register name	default value	R/W	description	
0x3508	AEC PK CTRL 08	0x84	RW	Bit[7]: Bit[6:0]:	Pk diff enable Diff min
0x3509	AEC PK CTRL 09	0x10	RW	Bit[7:5]: Bit[4]: Bit[3]: Bit[2]: Bit[1:0]:	Debug mode Convert enable Gain manual enable Digital gain manual enable Digital gain manual
0x350A	AEC PK REAL GAIN	0x00	RW	Real Gain Bit[7:2]: Bit[1:0]:	Debug mode Real gain[9:8] Value divided by 16 is the actual gain
0x350B	AEC PK REAL GAIN	0x10	RW	Real Gain Bit[7:0]:	Real gain[7:0] The value divided by 16 is the actual gain
0x350C~ 0x350F	DEBUG MODE	–	–	Debug Mode	
0x3510	AEC REAL GAIN READOUT	–	R	Bit[7:2]: Bit[1:0]:	Debug mode Real gain[9:8] readout
0x3511	AEC REAL GAIN READOUT	–	R	Bit[7:0]:	Real gain[7:0] readout
0x3512	AEC SNR GAIN READOUT	–	R	Bit[7:2]: Bit[1:0]:	Debug mode Sensor gain[9:8] readout
0x3513	AEC SNR GAIN READOUT	–	R	Bit[7:0]:	Sensor gain[7:0] readout
0x3A00	AEC CTRL00	0x78	RW	Bit[7]: Bit[6]: Bit[5]: Bit[4]: Bit[3]: Bit[2]: Bit[1]: Bit[0]:	Debug mode Enable the function that exposure can be less than 1 line Enable banding effect remove Enable function that exposure can be less than 1 band Debug mode Enable night mode Select new balance method Enable freeze mode
0x3A01	AEC CTRL01	0x04	RW	Bit[7:0]:	Minimum exposure (set 1, high 4 bits represent integer lines, low 4 bits represent fraction lines)
0x3A02	AEC CTRL02	0x04	RW	Bit[7:5]: Bit[4:0]:	Debug mode Maximum exposure for 60 Hz (set 1)
0x3A03	AEC CTRL03	0xD0	RW	Bit[7:0]:	Maximum exposure for 60 Hz (set 1, no fraction lines)

table 7-6   AEC/AGC control (sheet 3 of 5)

address	register name	default value	R/W	description	
0x3A05	AEC CTRL05	0x30	RW	Bit[7]: Bit[6]: Bit[5]: Bit[4:0]:	Reverse flag signal of 50/60 Hz Enable frame insertion in night mode Enable automatic step calculation Step ratio in automatic step calculation
0x3A06	AEC CTRL06	0x10	RW	Bit[7:5]: Bit[4:0]:	Debug mode Step 1 in manual step calculation
0x3A07	AEC CTRL07	0x18	RW	Bit[7:4]: Bit[3:0]:	Step 2 in manual step calculation Step 3 in manual step calculation
0x3A08	AEC CTRL08	0x00	RW	Bit[7:2]: Bit[1:0]:	Debug mode Band step for 50 Hz light
0x3A09	AEC CTRL09	0xB8	RW	Bit[7:0]:	Band step for 50 Hz light
0x3A0A	AEC CTRL0A	0x00	RW	Bit[7:2]: Bit[1:0]:	Debug mode Band step for 60 Hz light
0x3A0B	AEC CTRL0B	0x9A	RW	Bit[7:0]:	Band step for 60 Hz light
0x3A0C	AEC CTRL0C	0xE4	RW	Bit[7:4]: Bit[3:0]:	Maximum fraction exposure Minimum fraction exposure
0x3A0D	AEC CTRL0D	0x08	RW	Bit[7:6]: Bit[5:0]:	Debug mode Maximum band number in one frame for 60 Hz light source
0x3A0E	AEC CTRL0E	0x06	RW	Bit[7:6]: Bit[5:0]:	Debug mode Maximum band number in one frame for 50 Hz light source
0x3A0F	AEC CTRL0F	0x78	RW	Bit[7:0]:	Upper bound of stable range (set 1)
0x3A10	AEC CTRL10	0x68	RW	Bit[7:0]:	Lower bound of stable range (set 1)
0x3A11	AEC CTRL11	0xD0	RW	Bit[7:0]:	Upper bound of the range to determine step value in manual step calculation
0x3A12	AEC CTRL12	0x00	RW	Bit[7:0]:	Manual average value
0x3A13	AEC CTRL13	0x90	RW	Bit[7]: Bit[6:0]:	Enable pre sensor gain Value of pre sensor gain Here pre-gain means the output real gain must be larger than pre-gain
0x3A14	AEC CTRL14	0x04	RW	Bit[7:5]: Bit[4:0]:	Debug mode Maximum exposure for 50Hz (set 1)

table 7-6 AEC/AGC control (sheet 4 of 5)

address	register name	default value	R/W	description	
0x3A15	AEC CTRL15	0x50	RW	Bit[7:0]:	Maximum exposure for 50Hz (set 1, no fraction lines)
0x3A17	AEC CTRL17	0x01	RW	Bit[7:2]: Bit[1:0]:	Debug mode Threshold value of gain_night
0x3A18	AEC CTRL18	0x00	RW	Bit[7:2]: Bit[1:0]:	Debug mode Upper bound of output sensor gain
0x3A19	AEC CTRL19	0x7C	RW	Bit[7:0]:	Upper bound of output sensor gain
0x3A1A	AEC CTRL1A	0x00	RW	Bit[7:0]:	Minimum difference between VTS and maximum one frame exposure
0x3A1B	AEC CTRL1B	0x78	RW	Bit[7:0]:	Upper bound of stable range (set 2)
0x3A1C	AEC CTRL1C	0x06	RW	Bit[7:0]:	Added rows number for LED mode
0x3A1D	AEC CTRL1D	0x18	RW	Bit[7:0]:	Added rows number for LED mode
0x3A1E	AEC CTRL1E	0x68	RW	Bit[7:0]:	Lower bound of stable range (set 2)
0x3A1F	AEC CTRL1F	0x40	RW	Bit[7:0]:	Lower bound of the range to determine step value in manual step calculation
0x3A20	AEC CTRL20	0x20	RW	Bit[7]: Bit[6:3]: Bit[2]: Bit[1]: Bit[0]:	Enable function for subtracting black level Black level Enable strobe option Enable manual average Enable the calculation of the case current exposure does not change

table 7-6   AEC/AGC control (sheet 5 of 5)

address	register name	default value	R/W	description
0x3A21	AEC CTRL21	0x78	RW	Bit[7]: Debug mode Bit[6:4]: Maximum inserted frame number in frame insertion method of night mode Bit[3:1]: Debug mode Bit[0]: Gain adjustment option 0: Add 1 to calculated gain if AEC is increase and exposure and gain keep unchanged, subtract 1 to calculated gain if AEC is decrease and exposure and gain keep unchanged 1: No operations of adding 1 or subtracting 1
0x3A22~ 0x3A24	DEBUG MODE	–	–	Debug Mode
0x3A25	AEC CTRL25	0x00	RW	Bit[7:5]: Debug mode Bit[4:2]: Freeze count AEC update once per freeze count frames Bit[1]: Enable fraction constraint in less 1 line state Bit[0]: Enable same auto_step speed in automatic step mode
0x3A26	AEC CTRL26	0x02	RW	Bit[7:0]: Exposure line If exposure is less than exposure line, speed of auto step is step man2; otherwise, speed is step auto

table 7-7   frame control

address	register name	default value	R/W	description
0x4201	FRAME CTRL00	0x00	RW	Control Passed Frame Number When both ON and OFF number is set to 0x00, frame control is in bypass mode Bit[7:4]: Debug mode Bit[3:0]: Frame ON number
0x4202	FRAME CTRL01	0x00	RW	Control Masked Frame Number When both ON and OFF number set to 0x00, frame control is in bypass mode Bit[7:4]: Debug mode Bit[3:0]: Frame OFF number

table 7-8   format control

address	register name	default value	R/W	description
0x4300	FORMAT CTRL00	0xF8	RW	Bit[7:4]: Output format selection 0x0: RAW 0x3: YUV422 0x4: YUV420 0x5: YUV420 legacy 0x6: RGB565 0x9: gb444 format1 0xF: byp_fmt Bit[3:0]: Pixel order control
0x4301	CLIPPING CONTROL	0x00	RW	Bit[7:4]: Debug mode Bit[3:2]: Data limitation option 00: No limitation (0x000~0x3FF) 01: Limit data to 0x004~0x3FB 10: Limit data to 0x3F0~0x010 11: Limit data to 0x040~0x3C0 Bit[1:0]: YUV422 UV control 00: U/V generated from average 01: U/V generated from first pixel 11: U/V generated from second pixel

table 7-9   VFIFO registers

address	register name	default value	R/W	description
0x4601	VFIFO READ CONTROL	0x14	RW	Bit[7:4]: Debug mode Bit[3]: Read from fixed position of each line 　　　　0: Disable 　　　　1: Enable Bit[1]: Read host select 　　　　0: Select SRAM read for DVP 　　　　1: Select MIPI read Bit[0]: Debug mode
0x4602~ 0x4604	DEBUG MODE	–	–	Debug Mode
0x4605	VFIFO CONTROL05	0x08	RW	Bit[7:4]: Not used Bit[3]: Start size auto Bit[2:0]: Not used
0x4606~ 0x4607	DEBUG MODE	–	–	Debug Mode
0x4608	VFIFO READ START00	0x00	RW	Bit[7:0]: Read start[15:8]
0x4609	VFIFO READ START01	0x80	RW	Bit[7:0]: Read start[7:0]

table 7-10   DVP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700~ 0x4703	DEBUG MODE	–	–	Debug Mode
0x4704	DVP CTRL01	0x00	RW	Bit[7:4]: Debug mode Bit[3:2]: VSYNC output mode select Bit[1]: VSYNC3 mode enable 　　　　VSYNC generated by EOF, unset by first internal HREF Bit[0]: VSYNC2 mode enable 　　　　VSYNC generated by EOF 　　　　Width controlled by register 　　　　Default VSYNC1 mode enable 　　　　VSYNC generated by SOF 　　　　Width controlled by register
0x4705~ 0x4707	DEBUG MODE	–	–	Debug Mode

table 7-10   DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4708	DVP CTRL02	0x01	RW	Bit[7:6]: Debug mode Bit[5]: VSYNC gate clock enable Bit[4]: HREF gate clock enable Bit[2]: HREF polarity Bit[1]: VSYNC polarity Bit[0]: PCLK gate low enable
0x4709	DVP CTRL03	0x00	RW	Bit[7]: Video FIFO bypass mode Bit[6:4]: Data bit swap 000: Output data is the same order as input, that is [9:0] 001: Output data is reversed, [0:9] 010: Output data is reorder as {[2:9], [1:0]} 011: Output data is reorder as {[7:0], [9:8]} 100: Output data is reorder as {[9:8], [0:7]} 101: Output data is reorder as {[9], [0:8]} 110: Output data is reorder as {[1:9], [0]} 111: Output data is reorder as {[8:0], [9]} Bit[3]: Test mode Bit[2]: Test mode 10-bit Bit[1]: Test mode 8-bit Bit[0]: Test mode enable

table 7-11   ISP TOP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xFB	RW	Bit[7]: ISP enable 0: Disable 1: Enable Bit[6]: Raw gamma enable 0: Disable 1: Enable Bit[5]: AWB statistic enable 0: Disable 1: Enable Bit[4]: AWB gain enable 0: Disable 1: Enable Bit[3]: LENC enable 0: Disable 1: Enable Bit[2]: LCD adjustment enable 0: Disable 1: Enable Bit[1]: Black pixel canceling enable 0: Disable 1: Enable Bit[0]: White pixel canceling enable 0: Disable 1: Enable
0x5001	ISP CONTROL 01	0x17	RW	Bit[7:6]: Debug mode Bit[5]: UV average selection Bit[4]: LENC gain enable 0: Disable 1: Enable Bit[3]: Special digital effect enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Color interpolation enable 0: Disable 1: Enable
0x5002	ISP CONTROL 02	0x00	RW	Bit[7:5]: Debug mode Bit[4]: Scale enable 0: Disable 1: Enable Bit[3:0]: Debug mode
0x5003~0x5006	DEBUG MODE	–	–	Debug Mode

table 7-11   ISP TOP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5007	ISP CONTROL 07	0x3F	RW	Bit[7:6]: Debug mode Bit[5]: LENC bias plus Bit[4]: LENC bias on Bit[3]: Gamma bias plus Bit[2]: Gamma bias on Bit[1]: LCD bias plus Bit[0]: LCD bias on
0x5008~ 0x509F	DEBUG MODE	–	–	Debug Mode
0x50A0	PRE ISP CTRL00	0x00	RW	Bit[7]: ISP test enable Bit[6]: ISP test - rolling horizontal bar enable Bit[5]: ISP test - test image plus real image Bit[4]: Debug mode Bit[3:2]: Color bar style 00: Normal bar 01: Vertical changed bar 10: Horizontal changed bar style 1 11: Horizontal changed bar style 2 Bit[1:0]: Debug mode

table 7-12   BLC control (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC CONTROL 00	0x89	RW	Bit[7:1]: Debug mode Bit[0]: Offset compensation enable 0: Disable 1: Enable
0x4001	BLC START LINE	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: BLC start line
0x4002	BLC CONTROL 02	0x45	RW	Bit[7]: Format change enable 0: Disable 1: Enable Bit[6:0]: Debug mode
0x4003	BLC CONTROL 03	0x08	RW	Bit[7]: BLC redo enable Set to 1 will trigger a BLC redo n frames begin Bit[6]: BLC freeze Bit[5:0]: Manual frame number
0x4004	BLC LINE NUMBER	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: BLC line number

table 7-12   BLC control (sheet 2 of 2)

address	register name	default value	R/W	description
0x4005~ 0x4007	DEBUG MODE	–	–	Debug Mode
0x4009	BLC TARGET	0x10	RW	Black Target Level

table 7-13   LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x500A~ 0x500B	DEBUG MODE	–	–	Debug Mode
0x500C	LENC RED X0	0x03	RW	Bit[7:3]: Debug mode Bit[2:0]: LENC red pixel x0[10:8]
0x500D	LENC RED X0	0x30	RW	Bit[7:0]: LENC red pixel x0[7:0]
0x500E	LENC RED Y0	0x02	RW	Bit[7:3]: Debug mode Bit[2:0]: LENC red pixel y0[10:8]
0x500F	LENC RED Y0	0x5C	RW	Bit[7:0]: LENC red pixel y0[7:0]
0x5010	LENC RED A1	0x00	RW	Bit[7]: Debug mode Bit[6:0]: LENC red pixel a1
0x5011	LENC RED B1	0x00	RW	Bit[7:0]: LENC red pixel b1
0x5012	LENC RED A2 AND B2	0xFF	RW	Bit[7:4]: LENC red pixel b2 Bit[3:0]: LENC red pixel a2
0x5013	LENC GREEN X0	0x03	RW	Bit[7:3]: Debug mode Bit[2:0]: LENC green pixel x0[10:8]
0x5014	LENC GREEN X0	0x30	RW	Bit[7:0]: LENC green pixel x0[7:0]
0x5015	LENC GREEN Y0	0x02	RW	Bit[7:3]: Debug mode Bit[2:0]: LENC green pixel y0[10:8]
0x5016	LENC GREEN Y0	0x5C	RW	Bit[7:0]: LENC green pixel y0[7:0]
0x5017	LENC GREEN A1	0x00	RW	Bit[7]: Debug mode Bit[6:0]: LENC green pixel a1
0x5018	LENC GREEN B1	0x00	RW	Bit[7:0]: LENC green pixel b1
0x5019	LENC GREEN A2 AND B2	0xFF	RW	Bit[7:4]: LENC green pixel b2 Bit[3:0]: LENC green pixel a2
0x501A	LENC BLUE X0	0x03	RW	Bit[7:3]: Debug mode Bit[2:0]: LENC blue pixel x0[10:8]

table 7-13   LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x501B	LENC BLUE X0	0x30	RW	Bit[7:0]: LENC blue pixel x0[7:0]
0x501C	LENC BLUE Y0	0x02	RW	Bit[7:3]: Debug mode Bit[2:0]: LENC blue pixel y0[10:8]
0x501D	LENC BLUE Y0	0x5C	RW	Bit[7:0]: LENC blue pixel y0[7:0]
0x501E	LENC BLUE A1	0x00	RW	Bit[7]: Debug mode Bit[6:0]: LENC blue pixel a1
0x501F	LENC BLUE B1	0x00	RW	Bit[7:0]: LENC blue pixel b1
0x5020	LENC BLUE A2 AND B2	0xFF	RW	Bit[7:4]: LENC blue pixel b2 Bit[3:0]: LENC blue pixel a2
0x5021	LENC CONTROL 00	0x0C	RW	Bit[7:5]: Debug mode Bit[4:0]: LENC gain high threshold
0x5022	LENC CONTROL 01	0x06	RW	Bit[7]: LENC gain coefficient manual enable 0: Disable 1: Enable Bit[6:5]: Debug mode Bit[4:0]: LENC gain low threshold
0x5023	COEFFICIENT THRESHOLD	0x80	RW	Bit[7:0]: LENC coefficient threshold
0x5024	COEFFICIENT MANUAL VALUE	0x80	RW	Bit[7:0]: LENC coefficient manual value

table 7-14   gamma control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5025	GAMMA YST1	0x05	RW	Bit[7:0]: Gamma yst1
0x5026	GAMMA YST2	0x0C	RW	Bit[7:0]: Gamma yst2
0x5027	GAMMA YST3	0x1C	RW	Bit[7:0]: Gamma yst3
0x5028	GAMMA YST4	0x2A	RW	Bit[7:0]: Gamma yst4
0x5029	GAMMA YST5	0x39	RW	Bit[7:0]: Gamma yst5
0x502A	GAMMA YST6	0x45	RW	Bit[7:0]: Gamma yst6
0x502B	GAMMA YST7	0x52	RW	Bit[7:0]: Gamma yst7
0x502C	GAMMA YST8	0x5D	RW	Bit[7:0]: Gamma yst8

table 7-14   gamma control (sheet 2 of 2)

address	register name	default value	R/W	description
0x502D	GAMMA YST9	0x68	RW	Bit[7:0]: Gamma yst9
0x502E	GAMMA YST10	0x7F	RW	Bit[7:0]: Gamma yst10
0x502F	GAMMA YST11	0x91	RW	Bit[7:0]: Gamma yst11
0x5030	GAMMA YST12	0xA5	RW	Bit[7:0]: Gamma yst12
0x5031	GAMMA YST13	0xC6	RW	Bit[7:0]: Gamma yst13
0x5032	GAMMA YST14	0xDE	RW	Bit[7:0]: Gamma yst14
0x5033	GAMMA YST15	0xEF	RW	Bit[7:0]: Gamma yst15
0x5034	GAMMA YSLP	0x16	RW	Bit[7:0]: Gamma yslp

table 7-15   AWB control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5035	AWB CONTROL 00	0x5C	RW	Bit[7:6]: AWB step fast (when sub register 0x5037[7] = 1) Bit[5:4]: AWB step local Bit[3]: AWB g enable Bit[2]: AWB simple mode 　　0:　Advance mode 　　1:　Simple mode Bit[1]: AWB one zone mode Bit[0]: AWB average all mode
0x5036	AWB CONTROL 01	0x00	RW	Bit[7:4]: Max fast count (when sub register 0x5037[7] = 1) Bit[3:0]: Max local count
0x5037	AWB CONTROL 02	0x92	RW	Bit[7]: AWB fast enable 　　0:　Disable 　　1:　Enable Bit[6:4]: AWB count limit control Bit[3:0]: AWB stable range
0x5038	AWB CONTROL 03	0x21	RW	Bit[7:6]: AWB count area select Bit[5]: AWB sim select 　　0:　After AWB gain 　　1:　After gamma Bit[4]: AWB rblue Bit[3]: AWB slope 8x Bit[2]: AWB slope 4x Bit[1:0]: AWB count threshold

table 7-15   AWB control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5039	AWB CONTROL 04	0x70	RW	Bit[7]: AWB simf Bit[6]: AWB bias plus Bit[5]: AWB bias on Bit[4]: AWB bias statistics Bit[3]: AWB freeze Bit[2]: AWB preset Bit[1]: AWB preset Bit[0]: AWB window mode
0x503A	AWB LOCAL LIMIT	0x02	RW	Bit[7:0]: AWB local limit
0x503C~0x5048	AWB CONTROL	–	RW	Advanced AWB Control Registers
0x5049	AWB CONTROL 12	0xF0	RW	Bit[7:0]: AWB red gain limit
0x504A	AWB CONTROL 13	0xF0	RW	Bit[7:0]: AWB green gain limit
0x504B	AWB CONTROL 14	0xF0	RW	Bit[7:0]: AWB blue gain limit

table 7-16   DPC control

address	register name	default value	R/W	description

0x5000	ISP CONTROL 00	0xFB	RW	Bit[7:2]: Debug mode
				Bit[1]: Black pixel canceling enable
				            0: Disable
				            1: Enable
				Bit[0]: White pixel canceling enable
				            0: Disable
				            1: Enable

0x5054	DPC CTRL 00	0x1C	RW	Bit[7:0]: Debug control Changing these registers is not recommended

table 7-17 average control

address	register name	default value	R/W	description
0x5060	AVG CONTROL 00	0x55	RW	Bit[7:6]: Average weight00 Bit[5:4]: Average weight01 Bit[3:2]: Average weight02 Bit[1:0]: Average weight03
0x5061	AVG CONTROL 01	0x55	RW	Bit[7:6]: Average weight10 Bit[5:4]: Average weight11 Bit[3:2]: Average weight12 Bit[1:0]: Average weight13
0x5062	AVG CONTROL 02	0x55	RW	Bit[7:6]: Average weight20 Bit[5:4]: Average weight21 Bit[3:2]: Average weight22 Bit[1:0]: Average weight23
0x5063	AVG CONTROL 03	0x55	RW	Bit[7:6]: Average weight30 Bit[5:4]: Average weight31 Bit[3:2]: Average weight32 Bit[1:0]: Average weight33
0x5237	AVG READOUT	–	R	Bit[7:0]: Image average readout

table 7-18 CIP/DNS/sharpen control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5064	SHARPENMT THRESHOLD1	0x08	RW	Bit[7:0]: Sharpenmt threshold1 Low gain threshold for calculating sharpen strength automatically, T1<T2)
0x5065	SHARPENMT THRESHOLD2	0x48	RW	Bit[7:0]: Sharpenmt threshold2 High gain threshold for calculating sharpen strength automatically, T1<T2)
0x5066	SHARPENMT OFFSET1	0x18	RW	Bit[7]: Debug mode Bit[6:0]: Sharpenmt offset1[6:0] / MANUAL SHARPEN THRESHOLD Maximum sharpen strength in auto mode, shared with manual sharpen strength
0x5067	SHARPENMT OFFSET2	0x0E	RW	Bit[7]: Debug mode Bit[6:0]: Sharpenmt offset2 Minimum sharpen strength in auto mode, Offset1>Offset2
0x5068	DENOISE THRESHOLD1	0x08	RW	Bit[7:0]: Denoise threshold1 Low gain threshold for calculating denoise threshold automatically, T1<T2

table 7-18   CIP/DNS/sharpen control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5069	DENOISE THRESHOLD2	0x48	RW	Bit[7:0]: Denoise threshold2 High gain threshold for calculating denoise threshold automatically, T1<T2
0x506A	DENOISE OFFSET1	0x09	RW	Bit[7]: Debug mode Bit[6:0]: Denoise offset1/ MANUAL DNS THRESHOLD Maximum denoise threshold in auto mode, shared with manual denoise threshold
0x506B	DENOISE OFFSET2	0x16	RW	Bit[7]: Debug mode Bit[6:0]: Denoise offset2
0x506C	SHARPEN THRESHOLD1	0x08	RW	Bit[7:0]: Sharpen threshold1 Low gain threshold for calculating sharpen threshold automatically, T1 < T2
0x506D	SHARPEN THRESHOLD2	0x48	RW	Bit[7:0]: Sharpen threshold2 High gain threshold for calculating sharpen threshold automatically, T1<T2
0x506E	CIP CONTROL 00	0x44	RW	Bit[7]: CIP edge mt manual enable 0: Disable 1: Enable Bit[6]: Debug mode Bit[5]: CIP denoise manual enable 0: Disable 1: Enable Bit[4:0]: Sharpen offset1/ MANUAL SHARPENTH THRESHOLD Maximum sharpen threshold in auto mode, shared with manual sharpen threshold
0x506F	CIP CONTROL 01	0xA	RW	Bit[7:5]: Threshold RB sharpen Bit[4:0]: Sharpen offset2 Minimum sharpen threshold in auto mode, Offset1<Offset2

table 7-19   CMX control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5070	CMX1	0x33	RW	Bit[7:0]: CMX1
0x5071	CMX2	0x41	RW	Bit[7:0]: CMX2
0x5072	CMX3	0x0F	RW	Bit[7:0]: CMX3
0x5073	CMX4	0x0B	RW	Bit[7:0]: CMX4

table 7-19   CMX control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5074	CMX5	0x44	RW	Bit[7:0]: CMX5
0x5075	CMX6	0x50	RW	Bit[7:0]: CMX6
0x5076	CMX7	0x55	RW	Bit[7:0]: CMX7
0x5077	CMX8	0x3A	RW	Bit[7:0]: CMX8
0x5078	CMX9	0x1C	RW	Bit[7:0]: CMX9
0x5079	CMX SIGN	0x98	RW	Bit[7:0]: CMX sign for CMX1 ~ CMX8
0x507A	MISC CTRL 00	0x21	RW	Bit[7:2]: Reserved Bit[1]: CMX double Bit[0]: CMX sign for CMX9

table 7-20   SDE control (sheet 1 of 2)

address	register name	default value	R/W	description
0x507A	MISC CTRL 00	0x21	RW	Bit[7:6]: Debug mode Bit[5]: UV adjustment threshold2[8] Bit[4:2]: Debug mode Bit[1:0]: CMX usage

0x507B	SDE CTRL 00	0x00	RW	Bit[7]: Fixed Y
				Bit[6]: Negative
				Bit[5]: Black and white
				Bit[4]: Fixed U
				Bit[3]: Fixed V
				Bit[2]: Y contrast enable
				   0: Disable
				   1: Enable
				Bit[1]: Saturate enable
				   0: Disable
				   1: Enable
				Bit[0]: Hue enable
				   0: Disable
				   1: Enable

0x507C	SDE CTRL 01	0x80	RW	Bit[7:0]: Hue cosine
0x507D	SDE CTRL 02	0x00	RW	Bit[7:0]: Hue sine
0x507E	SDE CTRL 03	0x40	RW	Bit[7:0]: Adjust value1 Manual saturate U or fixed U
0x507F	SDE CTRL 04	0x00	RW	Bit[7:0]: Adjust value2 Manual saturate V or fixed V

table 7-20   SDE control (sheet 2 of 2)

address	register name	default value	R/W	description	
0x5080	SDE CTRL 05	0x00	RW	Bit[7:0]:	Manual Y offset
0x5081	SDE CTRL 06	0x20	RW	Bit[7:0]:	Y contrast gain 0x20: 1x
0x5082	SDE CTRL 07	0x00	RW	Bit[7:0]:	Y brightness
0x5083	SDE CTRL 08	0x01	RW	Bit[7:6]: Bit[5:0]:	Debug mode Sign set Hue: SGN0=1, SGN1=0, SGN4=SGN5=0 => 0<q<p/2 SGN0=0, SGN1=1, SGN4=SGN5=0 => -p/2<q<0 SGN0=1, SGN1=0, SGN4=SGN5=1 => -p/2<q<p SGN0=0, SGN1=1, SGN4=SGN5=1 => -p<q<-p/2 Y_contrast: SGN2: YOFFSET SGN3: YBRIGHTNESS
0x5084	SDE CTRL 09	0x10	RW	Bit[7:0]:	UV adjustment threshold1
0x5085	SDE CTRL 0A	0x00	RW	Bit[7:0]:	UV adjustment threshold2[7:0]

table 7-21 scale control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5600	SCALE CTRL 0	0x10	RW	Bit[7]: Debug mode Bit[6]: Vfirst 0: Select the second U and first V in YUV444to422 module 1: Select the first U and second V in YUV444to422 module Bit[5]: uv_drop YUV444to422 drop mode or average mode selection 0: Average mode 1: Drop mode Bit[4]: Auto mode Scale auto or manual mode selection 0: Manual mode 1: Auto mode Bit[3]: Hround 0: No horizontal rounding 1: Horizontal rounding in average mode Bit[2]: Hdrop 0: Horizontal average mode 1: Horizontal drop mode Bit[1]: Vround 0: No vertical rounding 1: Vertical rounding in average mode Bit[0]: Vdrop 0: Vertical average mode 1: Vertical drop mode
0x5601	SCALE CTRL 1	0x00	RW	Bit[7]: Debug mode Bit[6:4]: Hdiv Horizontal DCW scale times 000: DCW 1 time 001: DCW 2 times 010: DCW 4 times 011: DCW 8 times 100: DCW 16 times others: DCW 16 times Bit[2:0]: Vdiv Vertical DCW scale times 000: DCW 1 time 001: DCW 2 times 010: DCW 4 times 011: DCW 8 times 100: DCW 16 times others: DCW 16 times
0x5602	XSC HIGH	0x02	RW	Bit[7:2]: Debug mode Bit[1:0]: XSC[9:8]
0x5603	XSC LOW	0x00	RW	Bit[7:0]: XSC[7:0]

table 7-21   scale control (sheet 2 of 2)

address	register name	default value	R/W	description	
0x5604	YSC HIGH	0x02	RW	Bit[7:2]: Bit[1:0]:	Debug mode YSC[9:8]
0x5605	YSC LOW	0x00	RW	Bit[7:0]:	YSC[7:0]
0x5606	VOFFSET	0x00	RW	Bit[7:4]: Bit[3:0]:	Debug mode Voffset Select which line to output in vertical drop mode

8 operating specifications

8.1 absolute maximum ratings

table 8-1   absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2   functional temperature

parameter	range
operating temperature range[a]	-20°C to +70°C
stable operating temperature range[b]	0°C to +50°C

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3   DC characteristics (T_A = 23°C ± 2°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I_{DD-A}	active (operating) current		25	30	mA
I_{DD-IO}[b]			40	50	mA
$I_{DDS-SCCB}$	standby current		30	75	µA
$I_{DDS-PWDN}$			30	75	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}[c]	SIOC and SIOD	1.26	1.8	2.3	V

a.   using the internal regulator is strongly recommended for minimum power down currents

b.   active current is based on sensor resolution at full size and full speed

c.   based on DOVDD = 1.8V.

8.4 AC characteristics

table 8-4　　AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

8.5 timing characteristics

table 8-5　　timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27(54[a])	MHz
t_r, t_f	clock input rise/fall time			5 (10[b])	ns

a.　if using the internal clock pre-scaler

b.　if using the internal PLL
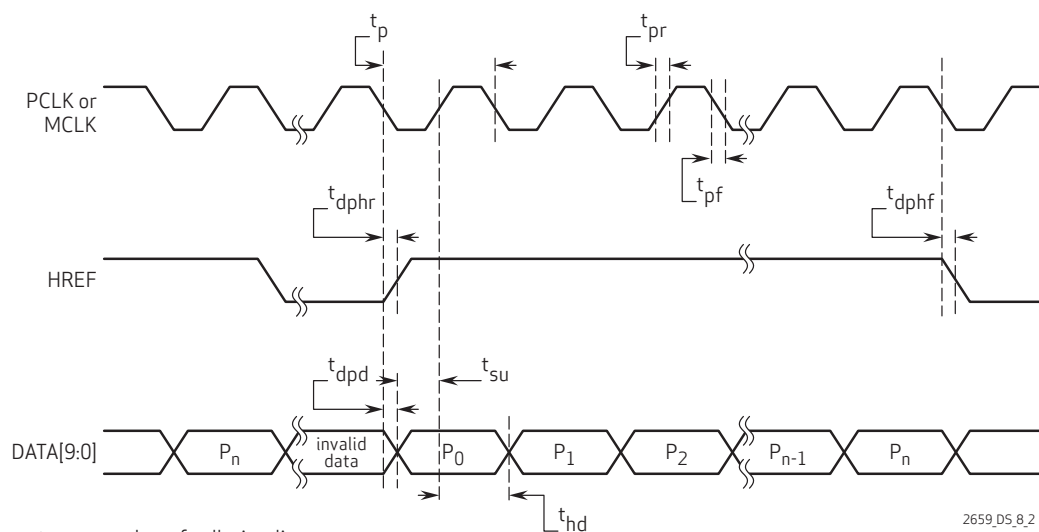
figure 8-1   SCCB interface timing

2659_DS_8_1

table 8-6   SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

figure 8-2 line/pixel output timing

note n = number of pclks in a line

2659_DS_8_2

table 8-7 pixel timing specifications[a]

symbol	parameter	min	typ	max	unit
t_p	PCLK period[b]		13.89		ns
t_{pr}	PCLK rising time[b]		1.33		ns
t_{pf}	PCLK falling time[b]		2.41		ns
t_{dphr}	PCLK negative edge to HREF rising edge		1		ns
t_{dphf}	PCLK negative edge to HREF negative edge		1		ns
t_{dpd}	PCLK negative edge to data output delay	0		4	ns
t_{su}	data bus setup time	5	7		ns
t_{hd}	data bus hold time	5	7		ns

a. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%,
    timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the
    beginning of the rising edge or/and of the falling edge signifies 90%

b. PCLK running at 72 MHz, C_L = 10pF, and DOVDD = 2.8V

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

top view
(bumps down)

bottom view
(bumps up)

center of BGA =
center of the package

side view

note 1 part marking code:
W - OVT product version
X - year part was assembled
Y - month part was assembled
Z - wafer number
ABCD - last four digits of lot number

2659_CSP_DS_9_1

table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	4710	4735	4760	µm
package body dimension y	B	4360	4385	4410	µm
package height	C	690	750	810	µm
ball height	C1	100	130	160	µm
package body thickness	C2	575	620	665	µm
thickness of glass surface to wafer	C3	425	445	465	µm
ball diameter	D	220	250	280	µm
total pin count	N		47 (11 NC)		
pin count x-axis	N1		7		
pin count y-axis	N2		8		
pins pitch x-axis	J1		600		µm
pins pitch y-axis	J2		500		µm
edge-to-pin center distance analog x	S1	538	568	598	µm
edge-to-pin center distance analog y	S2	413	443	473	µm

9.2 IR reflow specifications
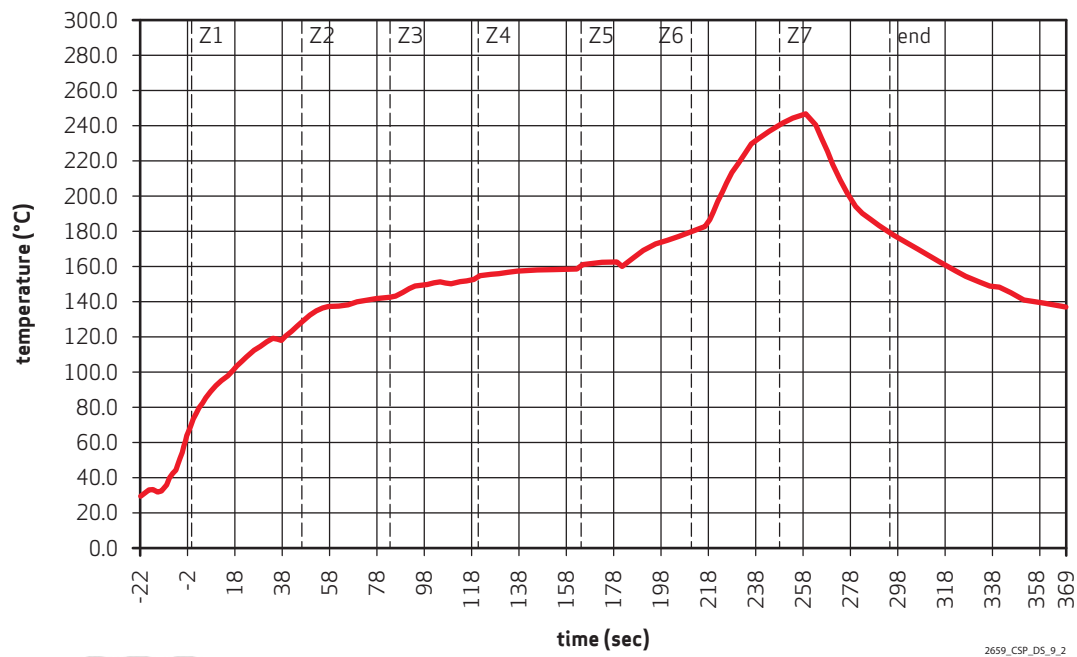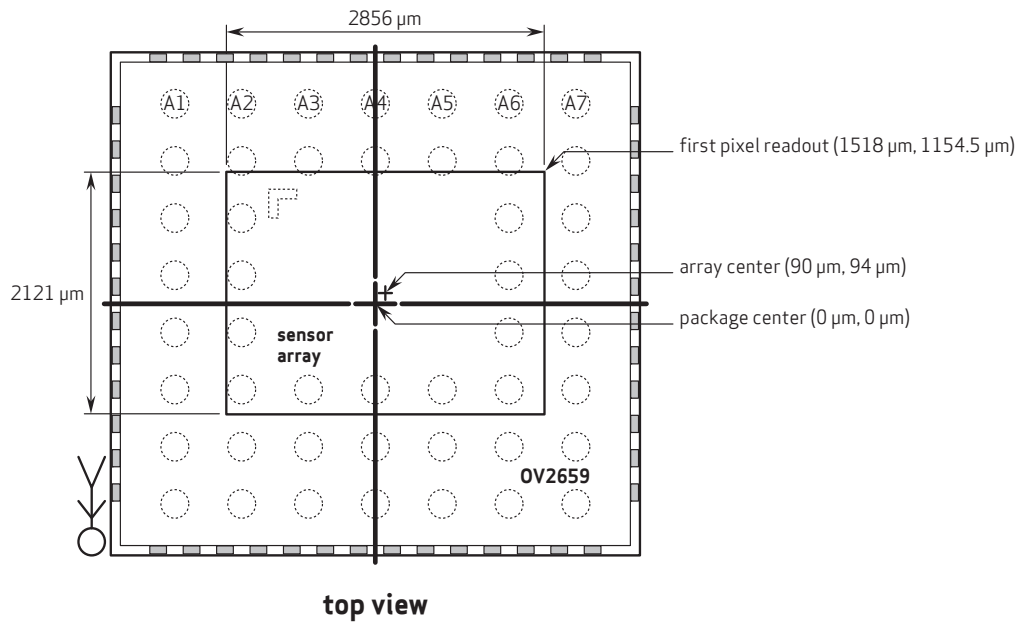
figure 9-2   IR reflow ramp rate requirements

2659_CSP_DS_9_2

table 9-2   reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1   sensor array center

top view

note 1   this drawing is not to scale and is for reference only.

note 2   as most optical assemblies invert and mirror the image, the chip is
typically mounted with pins A1 to A7 oriented down on the PCB.
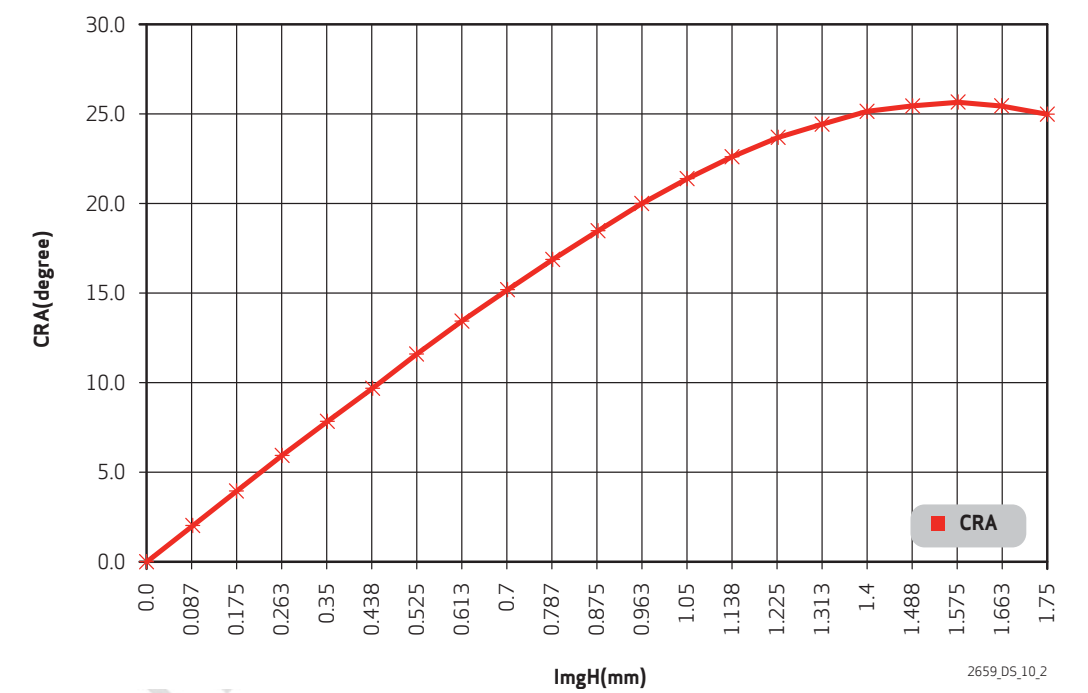
2659_CSP_DS_10_1

figure 10-2   chief ray angle diagram

2659_DS_10_2

table 10-1   CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.087	2
0.1	0.175	3.9
0.15	0.263	5.9
0.2	0.35	7.8
0.25	0.438	9.7
0.3	0.525	11.6
0.35	0.613	13.4
0.4	0.7	15.2
0.45	0.787	16.9
0.5	0.875	18.5
0.55	0.963	20

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.6	1.05	21.4
0.65	1.138	22.6
0.7	1.225	23.7
0.75	1.313	24.5
0.8	1.4	25.2
0.85	1.488	25.5
0.9	1.575	25.7
0.95	1.663	25.5
1	1.75	25

revision history

version 1.0   04.08.2010

- initial release

version 1.1   05.06.2010

- in chapter 4, updated all descriptions of table 4-2 image windowing control functions
- in chapter 4, updated table 4-4 AEC/AGC control functions; changed registers 0x350C and 0x350D to 0x3506 and 0x3507
- in chapter 4, updated all descriptions of table 4-6 image windowing control functions registers 0x3810~0x380A
- in chapter 4, updated section 4.5.1.2 and section 4.5.1.5
- in chapter 5, updated table 5-1 register 0x5007 by adding Bit[0]
- in chapter 5, updated table 5-2 register 0x5021
- in chapter 5, updated table 5-4 register 0x5039
- in chapter 5, removed from table 5-4 registers 0x504C~0x504E and replaced with registers 0x3400~0x3406
- in chapter 5, added register 0x506C in table 5-7
- in chapter 5, removed from table 5-10 registers 0x5607 and 0x5608
- in chapter 7, added to table 7-3 registers 0x3400 to 0x3406
- in chapter 7, updated table 7-5 register 0x3A13
- in chapter 7, updated table 7-5 registers 0x3512 and 0x3513
- in chapter 7, updated table 7-10 register 0x5007
- in chapter 7, updated table 7-10 register 0x504C to 0x504E
- in chapter 7, added register 0x506C in table 7-17
- in chapter 7, removed from table 7-20 registers 0x5607 and 0x5608

version 2.0   08.30.2010

- in the key specifications section, updated all TBD values
- in chapter 2, updated the entire section 2.5 power up sequence
- in chapter 2, updated section 2-5 group hold and added a sidebar note
- in chapter 4, updated table 4-4 AEC/AGC control functions registers 0x350A and 0x350B
- in chapter 4, updated section 4.5.1.2 banding mode ON with AEC
- in chapter 7, added register 0x3014 to table 7-2 system registers
- in chapter 7, updated table 7-5 timing control registers 0x380C and 0x380E
- in chapter 7, updated table 7-6 AEC/AGC control registers 0x350A and 0x350B
- in chapter 8, updated all TBD information in table 8-3 DC characteristics
- in chapter 8, updated table 8-6 SCCB interface timing specifications $t_{SU:STA}$
- in chapter 8, updated all TBD information in table 8-7 pixel timing specifications
- in chapter 9, update the S2 minimum and typical values

the clear advantage™

OmniVision Technologies, Inc.

UNITED STATES

4275 Burton Drive
Santa Clara, CA 95054

tel: + 1 408 567 3000
fax: + 1 408 567 3001
email: salesamerican@ovt.com

UNITED KINGDOM

Hampshire + 44 1256 744 610

FINLAND

Mouhijärvi + 358 3 341 1898

GERMANY

Munich +49 89 63 81 99 88

CHINA

Beijing + 86 10 6580 1690
Shanghai + 86 21 6105 5100
Shenzhen + 86 755 8384 9733
Hong Kong + 852 2403 4011

JAPAN

Tokyo + 81 3 5765 6321

KOREA

Seoul + 82 2 3478 2812

SINGAPORE + 65 6562 8250

TAIWAN

Taipei + 886 2 2657 9800 -
ext.#100

website: **www.ovt.com**