{% if site.google_scholar_stats_use_cdn %}
{% assign gsDataBaseUrl = "https://cdn.jsdelivr.net/gh/" | append: site.repository | append: "@" %}
{% else %}
{% assign gsDataBaseUrl = "https://raw.githubusercontent.com/" | append: site.repository | append: "/" %}
{% endif %}
{% assign url = gsDataBaseUrl | append: "google-scholar-stats/gs_data_shieldsio.json" %}

I am currently a PhD student in the School of Microelectronics department of Southern University of Science and Technology. I obtained my BEng degree in Microelectronic Science and Engineering from Southern University of Science and Technology in 2022, advised by Prof. Fengwei An. My research realm focuses on Stereo vision, computer architecture, low-power and high-performance VLSI circuit design and software-hardware co-design. You can find more information through my CV. Welcome to contact with me if you have any interests.
E-mail: 12231167@sustech.edu.cn | WeChat: zhuoyu936

📖 Educations

- *2022.09 - Present*, PhD in Microelectronics Science and Engineering, Southern University of Science and Technology.
- *2018.08 - 2022.06*: 🎉 🎉 BEng in Microelectronics Science and Engineering, School of Microelectronics, Southern University of Science and Technology. GPA: 3.52/4.00 RANK: 4/35
- *2015.09 - 2018.06*: 🎉 🎉 Xi'an Tie Yi High School

🔥 News

- *2024.11.11*: 🥂 One paper "A 3.9 pJ/pixel Trinocular Vision System with Cascadable Binocular Stereo Processor and Pixel-wise Disparity Fusion for Ultra-Wide Depth Sensing" has been submitted to IEEE CICC 2025.
- *2024.5.18*: 🎉 🎉 One paper "Live Demostration: A 1920×1080 129fps 4.3pJ/pixel Stereo-Matching Processor for Low-power Applications" has been accepted by IEEE ISCAS 2024! And we successfully demonstrated the demo on the conference.
- *2023.5.24*: 🎉 🎉 One paper "A 1920×1080 129fps 4.3pJ/Pixel Stereo-Matching Processor for Pico Aerial Vehicles" has been accepted by IEEE ESSDERC/ESSCIRC 2023!
- *2022.6.6*: 🎉 🎉 Our stereo depth coprocessor has sucessfully been taped out in TSMC 28nm CMOS technology!

📝 Main Publications

ISCAS
[Live Demonstration: A 1920×1080 129fps 4.3pJ/pixel Stereo-Matching Processor for Low-power Applications](https://ieeexplore.ieee.org/abstract/document/10558420)

Zhuoyu Chen; Shengming Zhou; Pingcheng Dong; Ke Li; Wenyue Zhang; Fengwei An; Lei Chen.

2024, *IEEE International Symposium on Circuits and Systems (ISCAS)*

ESSCIRC

A 1920×1080 129fps 4.3pJ/Pixel Stereo-Matching Processor for Pico Aerial Vehicles

Pingcheng Dong†, **Zhuoyu Chen**†, Ke Li, Lei Chen, Kwang-Ting Cheng, Fengwei An.

2023, *IEEE 49th European Solid State Circuits Conference (ESSCIRC)*

† These authors contributed equally to this work and should be considered co-first authors

TCAS-I

A 4.29 nJ/pixel stereo depth coprocessor with pixel level pipeline and region optimized semi-global matching for IoT application

Pingcheng Dong†, **Zhuoyu Chen**†, Zhuoao Li, Yuzhe Fu, Lei Chen, Fengwei An.

2021, *IEEE Transactions on Circuits and Systems I: Regular Papers*

† These authors contributed equally to this work and should be considered co-first authors

SOCC

Real-Time FPGA-Based Binocular Stereo Vision System with Semi-Global Matching Algorithm

Zhuoyu Chen, Pingchen Dong, Zhuoao Li, Ruoheng Yao, Yunhao Ma, Xiwei Fang, Huanshihong Deng, Wenyue Zhang, Lei Chen, Fengwei An.

2021, *IEEE International System-on-Chip Conference (SOCC)*

TCAS-II

Configurable Image Rectification and Disparity Refinement for Stereo Vision

Pingcheng Dong†, **Zhuoyu Chen**†, Zhuoao Li, Ruoheng Yao, Wenyue Zhang, Yangyi Zhang, Lei Chen, Chao Wang, Fengwei An.

2022, *IEEE Transactions on Circuits and Systems II: Express Briefs*

† These authors contributed equally to this work and should be considered co-first authors

A 139 fps pixel-level pipelined binocular stereo vision accelerator with region-optimized semi-global matching

Pingcheng Dong, Zhuoao Li, **Zhuoyu Chen**, Ruoheng Yao, Huanshihong Deng, Wenyue Zhang, Yangyi Zhang, Lei Chen, Chao Wang, Fengwei An.

2021, *IEEE Asian Solid-State Circuits Conference (A-SSCC)*

📝 Collaborative Publications

A compact hardware architecture for bilateral filter with the combination of approximate computing and look-up table. Ruoheng Yao, Lei Chen, Pingcheng Dong, **Zhuoyu Chen**, Fengwei An. **2022**, *IEEE Transactions on Circuits and Systems II: Express Briefs*

A 320 FPS Pixel-Level Pipelined Stereo Vision Accelerator with Regional Optimization and Multi-direction Hole Filling. Ke Li, Xinyu Guan, Pingcheng Dong, **Zhuoyu Chen**, Lei Chen, Fengwei An. **2022**, *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*

🎖 Honors and Awards

- *2022* Outstanding Graduate of College
- *2021* The Second Prize of Outstanding Students in Shuli College of SUSTech (Top 10% in SUSTech)
- *2020* The Second prize of National College Students FPGA Innovation Design Competition
- *2018* The Second Prize of Outstanding Students in SUSTech (Top 20% in SUSTech)

💻 Internships

- *2022.05 - Present*, future vison, China.