Zhuoyu Chen

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Research Interests

Stereo vision, image processing, machine learning, hardware acceleration for vision algorithm, low-power and high-performance VLSI circuit design..

Education

- *2022.09 - (Expected 2027)*, PhD in Microelectronics Science and Engineering, Southern University of Science and Technology.
- *2018.08 - 2022.06*: 🎉 🎉 BEng in Microelectronics Science and Engineering, School of Microelectronics, Southern University of Science and Technology. GPA: 3.52/4.00 RANK: 4/35
- *2015.09 - 2018.06*: 🎉 🎉 Xi'an Tie Yi High School

Research Experience

Processor of multi-view stereo vision fusion
SME Lab of Intelligent Perception **|** 2023 – present**

- Developed a trinocular vision system with a cascadable binocular stereo processor, featuring a multi-baseline stereo rectification method, and a pixel-wise disparity fusion architecture using variable baselines and fov.

ASIC design of stereo depth coprocessor in 28nm CMOS technology
SME Lab of Intelligent Perception | **2020 – 2023**

- In charge of the front-end design for the top-level architecture, including sensor configuration, Ethernet real-time video transmission circuits, stereo rectification circuits, and stereo matching circuits.

Hardware accelerator for stereo vision algorithm
SUSTech Lab of Embedded Systems | **2019 – 2020**

- Proposed a four-layer parallel pipeline hardware architecture and implemented it on FPGA platform which can extract depth information in real-time at 156MHz and 508fps under VGA resolution.

Publications

- **[A 3.9 pJ/pixel Trinocular Vision System with Cascadable Binocular Stereo Processor and Pixel-wise Disparity Fusion for Ultra-Wide Depth Sensing]**
  CICC 2025 (First Author)**(Under Review)**
- **[Live Demonstration: A 1920×1080 129fps 4.3pJ/pixel Stereo-Matching Processor for Low-power Applications]**
  ISCAS 2024 (First Author)

- **[A 1920×1080 129fps 4.3pJ/Pixel Stereo-Matching Processor for Pico Aerial Vehicles]**
  ESSCIRC 2023(Co-First Author)
- **[Configurable Image Rectification and Disparity Refinement for Stereo Vision]**
  TCAS II 2022 (Co-First Author)
- **[A 4.29 nJ/pixel stereo depth coprocessor with pixel level pipeline and region optimized semi-global matching for IoT application]**
  TCAS I 2021 (Co-First Author)
- **[Real-Time FPGA-Based Binocular Stereo Vision System with Semi-Global Matching Algorithm]**
  SOCC 2021 (First Author)

Skills

- **Programming Languages:** Python, C++
- **Tools & Frameworks:** Git, MATLAB, VCS, VIVADO, Altera, Vitis
- **Hardware Design:** RTL Design, FPGA, VHDL, Verilog

Honors & Awards

- *2022* Outstanding Graduate of College
- *2021* The Second Prize of Outstanding Students in Shuli College of SUSTech (Top 10% in SUSTech)
- *2020* Third Prize, National College Students Robomaster Competition, DJI Technology Co., Ltd
- *2020* The Second Prize, National College Students FPGA Innovation Design Competition, Chinese Institute of Electronics
- *2020* The Second prize of National College Students FPGA Innovation Design Competition
- *2019* The First Place, HKUST-SUSTech Joint Business Training Program, School of System Design and Intelligent Manufacturing
- *2018* The Second Prize of Outstanding Students in SUSTech (Top 20% in SUSTech)

Additional Information

- **Languages:** English (TOEFL:89), Mandarin (Native), Japanese (N2:132)
- **Internships:** *2022.05 - Present*, future vison, China.
- **Teaching Assistant:** *Digital Integrated Circuits, Fundamentals of Integrated Circuits* (Fall 2022)
  Digital System Design (Spring 2024)