Zhuoyu Chen

- PhD student of SUSTech, Focusing on Stereo vision, AI chip and hardware accelerator.
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Education

- *2022.09 - Present*, PhD in Microelectronics Science and Engineering, Southern University of Science and Technology.
- *2018.08 - 2022.06*: 🎉 🎉 BEng in Microelectronics Science and Engineering, School of Microelectronics, Southern University of Science and Technology. GPA: 3.52/4.00 RANK: 4/35
- *2015.09 - 2018.06*: 🎉 🎉 Xi'an Tie Yi High School

Research Interests

Stereo vision, image processing, machine learning, hardware acceleration for vision algorithm, low-power and high-performance VLSI circuit design

Research Experiences

2022 - present: Algorithm of multiocular stereo vision

Researching in the MVS and multiocular calibration.

2020 - 2022: ASIC design of stereo depth coprocessor in 28nm CMOS technology.

Developed a pixel-level pipeline hardware architecture of proposed region┐optimized semi-global matching algorithm.

2019- 2020: Hardware accelerator for stereo vision algorithm.

1. Proposed a region-optimized stereo matching strategy improving the speed of traditional semi-global matching algorithm by 5 times while ensuring the accuracy.
2. Proposed a four-layer parallel pipeline hardware architecture and implemented it on FPGA platform which can extract depth information in real-time at 156MHz and 508fps under VGA resolution.

Main Publications

A 4.29 nJ/pixel stereo depth coprocessor with pixel level pipeline and region optimized semi-global matching for IoT application

Pingcheng Dong†, **Zhuoyu Chen**†, Zhuoao Li, Yuzhe Fu, Lei Chen, Fengwei An.

2021, *IEEE Transactions on Circuits and Systems I: Regular Papers*

† These authors contributed equally to this work and should be considered co-first authors

Real-Time FPGA-Based Binocular Stereo Vision System with Semi-Global Matching Algorithm

Zhuoyu Chen, Pingchen Dong, Zhuoao Li, Ruoheng Yao, Yunhao Ma, Xiwei Fang, Huanshihong Deng, Wenyue Zhang, Lei Chen, Fengwei An.

2021, *IEEE International System-on-Chip Conference (SOCC)*

Configurable Image Rectification and Disparity Refinement for Stereo Vision

Pingcheng Dong†, **Zhuoyu Chen**†, Zhuoao Li, Ruoheng Yao, Wenyue Zhang, Yangyi Zhang, Lei Chen, Chao Wang, Fengwei An.

2022, *IEEE Transactions on Circuits and Systems II: Express Briefs*

† These authors contributed equally to this work and should be considered co-first authors

A 1920×1080 129fps 4.3pJ/Pixel Stereo-Matching Processor for Pico Aerial Vehicles

Pingcheng Dong†, **Zhuoyu Chen**†, Ke Li, Lei Chen, Kwang-Ting Cheng, Fengwei An.

2023, *IEEE 49th European Solid State Circuits Conference (ESSCIRC)*

† These authors contributed equally to this work and should be considered co-first authors

A 139 fps pixel-level pipelined binocular stereo vision accelerator with region-optimized semi-global matching. Pingcheng Dong, Zhuoao Li, **Zhuoyu Chen**, Ruoheng Yao, Huanshihong Deng, Wenyue Zhang, Yangyi Zhang, Lei Chen, Chao Wang, Fengwei An. . **2021**, *IEEE Asian Solid-State Circuits Conference (A-SSCC)*

Collaborative Publications

A compact hardware architecture for bilateral filter with the combination of approximate computing and look-up table. Ruoheng Yao, Lei Chen, Pingcheng Dong, **Zhuoyu Chen**, Fengwei An. **2022**, *IEEE Transactions on Circuits and Systems II: Express Briefs*

A 320 FPS Pixel-Level Pipelined Stereo Vision Accelerator with Regional Optimization and Multi-direction Hole Filling. Ke Li, Xinyu Guan, Pingcheng Dong, **Zhuoyu Chen**, Lei Chen, Fengwei An. **2022**, *IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*

Honors and Awards

- *2022* Outstanding Graduate of College
- *2021* The Second Prize of Outstanding Students in Shuli College of SUSTech (Top 10% in SUSTech)
- *2020* The Second prize of National College Students FPGA Innovation Design Competition
- *2018* The Second Prize of Outstanding Students in SUSTech (Top 20% in SUSTech)

Internships

- *2022.05 - Present*, future vison, China.