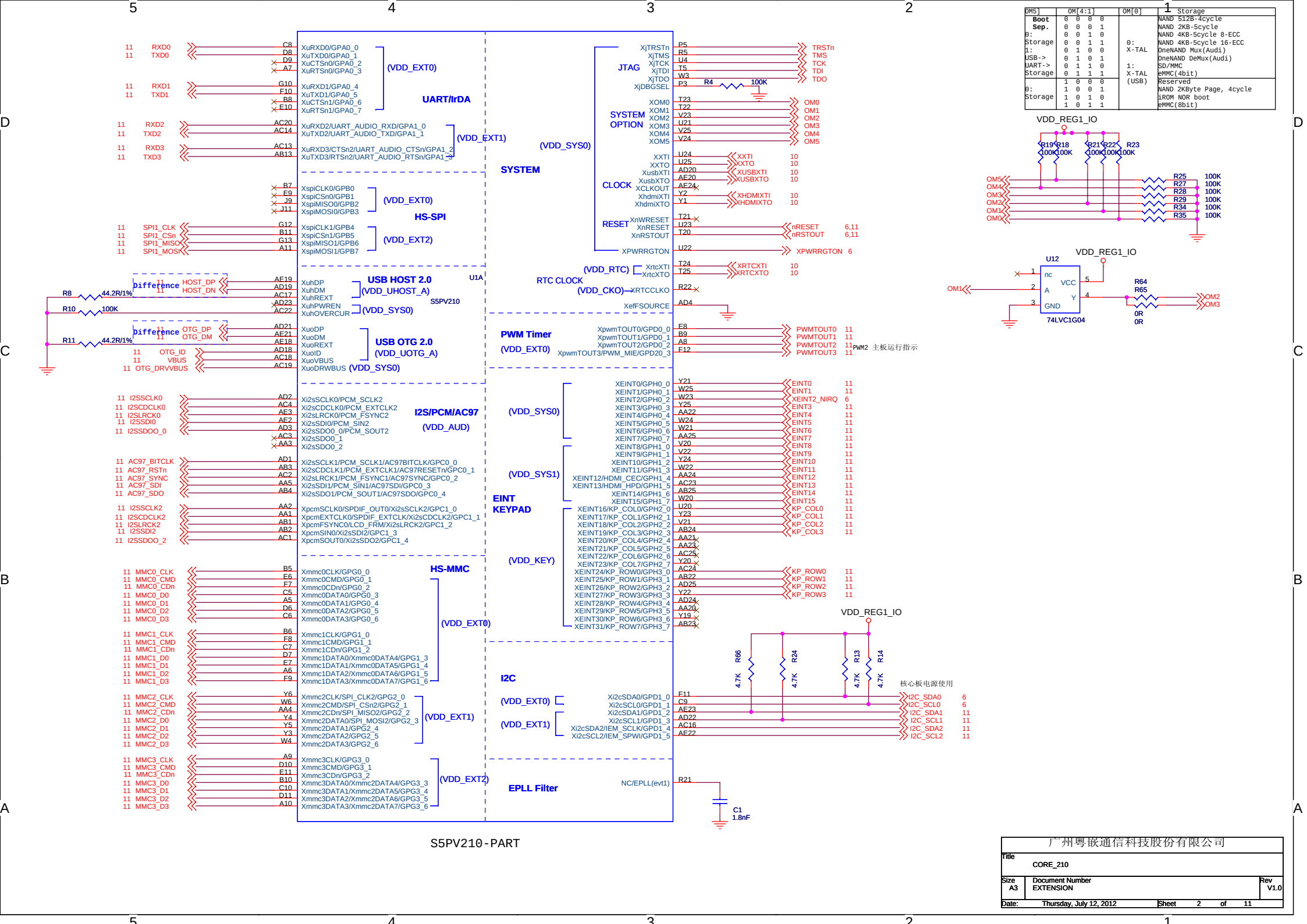
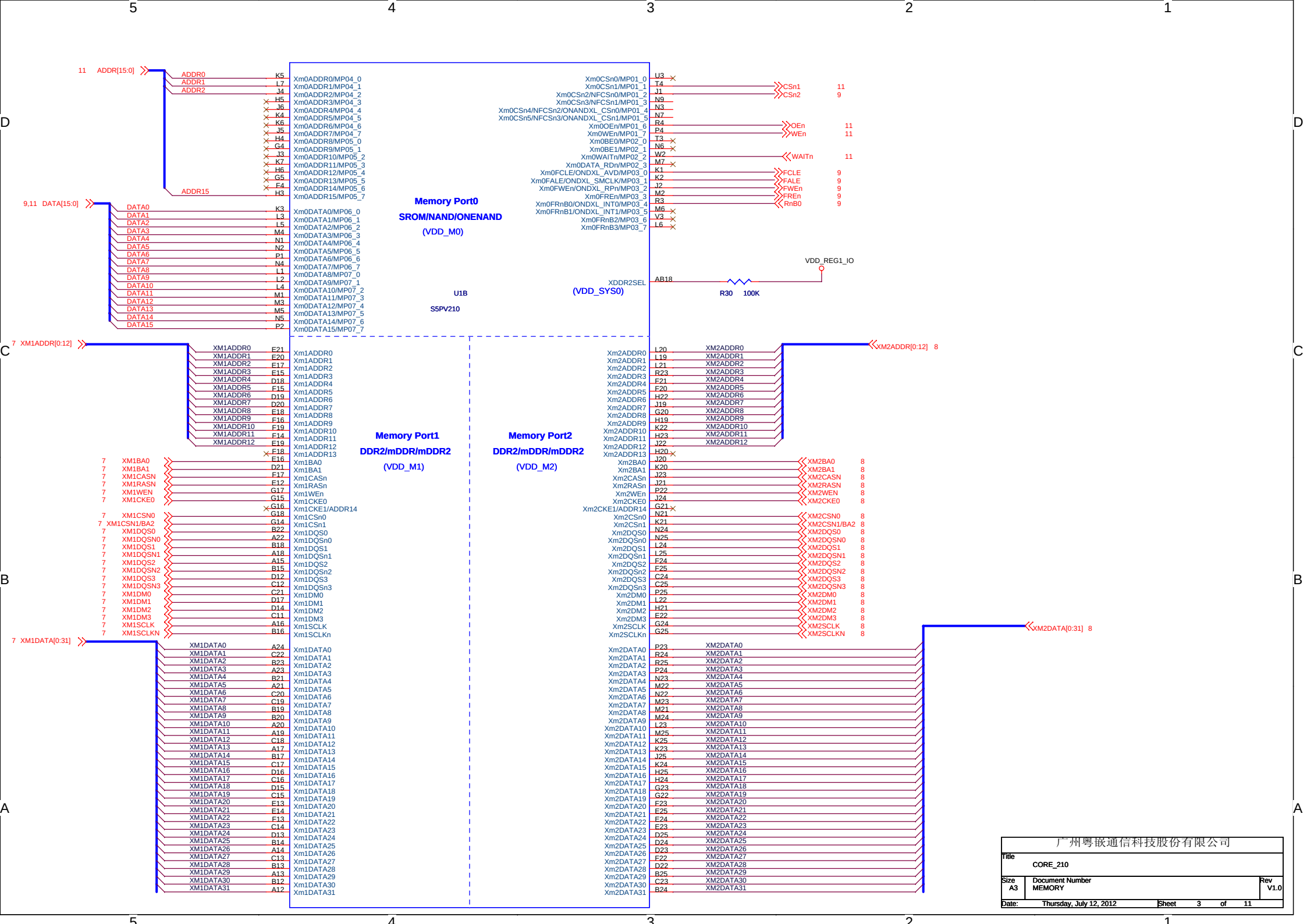
Version History

Version	Modify Content	Responsibility	Date
V1.0			2011/11/07


S5PV210-PART
U1A
S5PV210
UART/IrDA
HS-SPI
USB HOST 2.0
USB OTG 2.0
I2S/PCM/AC97
HS-MMC
SYSTEM
JTAG
SYSTEM OPTION
CLOCK
RESET
RTC CLOCK
PWM Timer
EINT
KEYPAD
I2C
EPLL Filter
VDD_REG1_IO
74LVC1G04
PWM2 主板运行指示
核心板电源使用
广州粤嵌通信科技股份有限公司
CORE_210
EXTENSION
Thursday, July 12, 2012


Memory Port0
SROM/NAND/ONENAND
(VDD_M0)
U1B
S5PV210
Memory Port1
DDR2/mDDR/mDDR2
(VDD_M1)
Memory Port2
DDR2/mDDR/mDDR2
(VDD_M2)
(VDD_SYS0)
VDD_REG1_IO
R30 100K
广州粤嵌通信科技股份有限公司
CORE_210
MEMORY
V1.0
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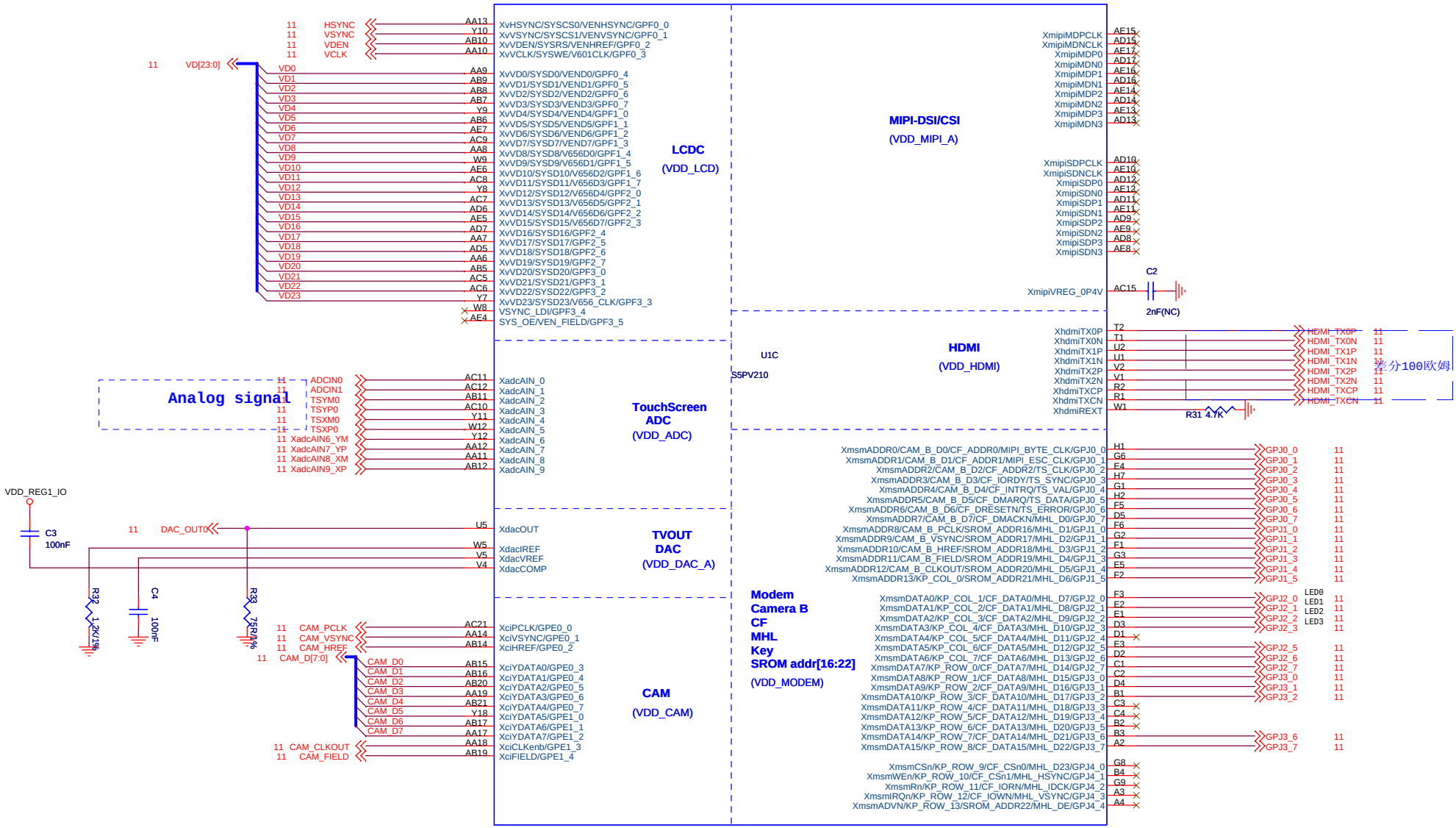

广州粤嵌通信科技股份有限公司	
Title	CORE_210
Size A3	Document Number MEDIA
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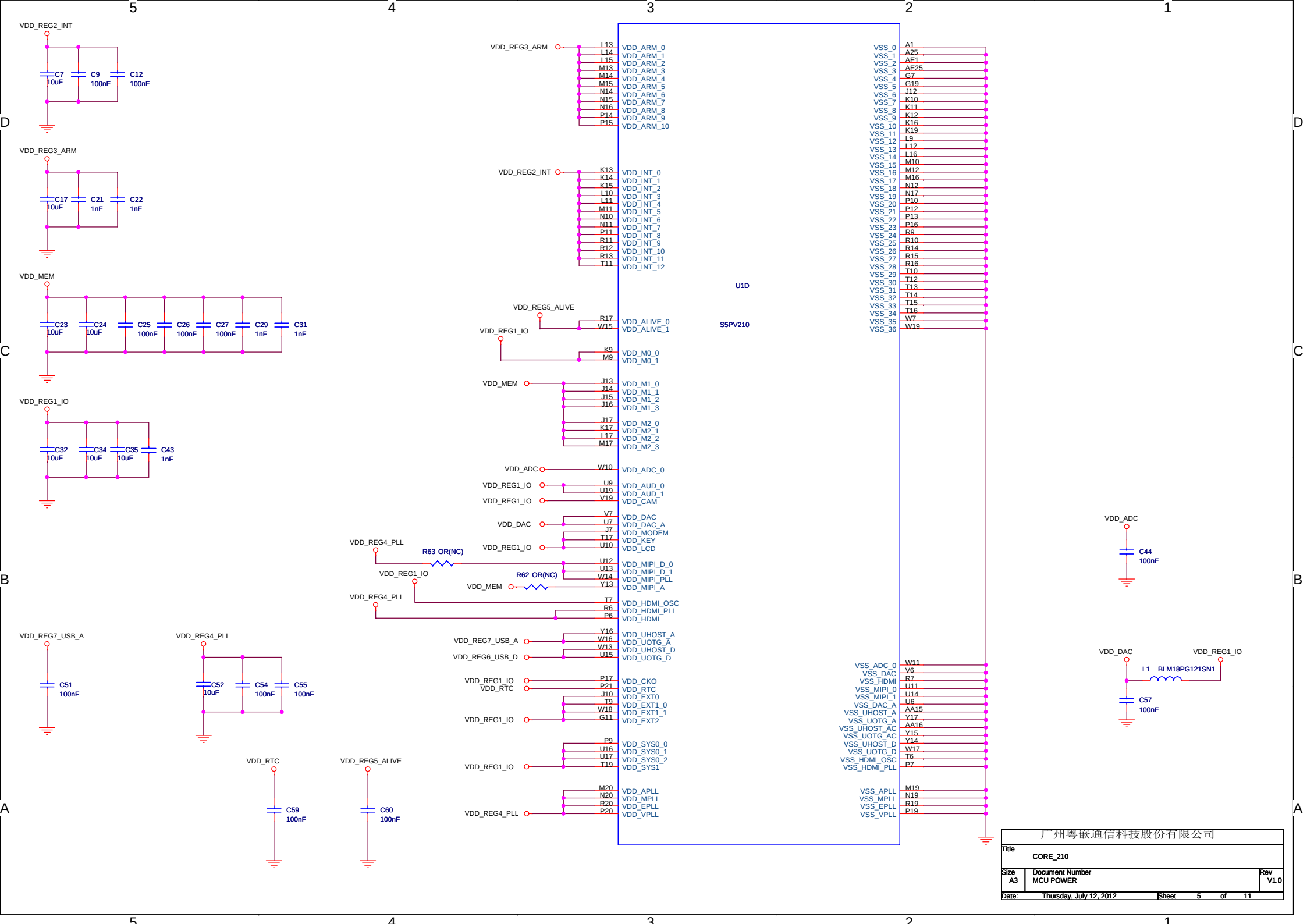

广州粤嵌通信科技股份有限公司

Title	CORE_210	
Size A3	Document Number MCU POWER	Rev V1.0
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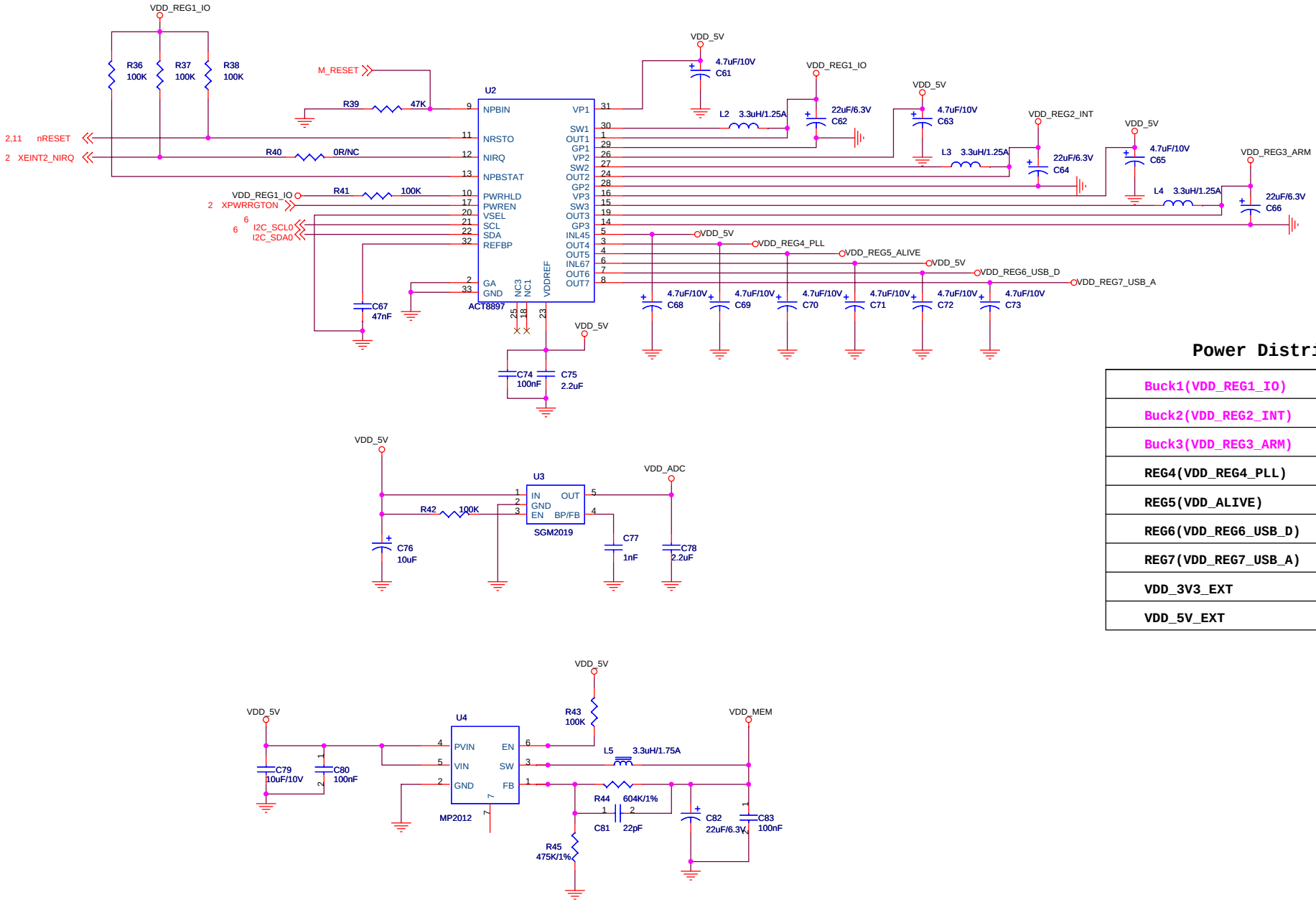

Power Distribute table

Buck1(VDD_REG1_IO)	3.3V/1100mA
Buck2(VDD_REG2_INT)	1.1V/1100mA
Buck3(VDD_REG3_ARM)	1.25V/1200mA
REG4(VDD_REG4_PLL)	1.1V/150mA
REG5(VDD_ALIVE)	1.1V/150mA
REG6(VDD_REG6_USB_D)	1.1V/250mA
REG7(VDD_REG7_USB_A)	3.3V/250mA
VDD_3V3_EXT	3.3V/1500mA
VDD_5V_EXT	5.0V/2000mA

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Title	CORE_210	
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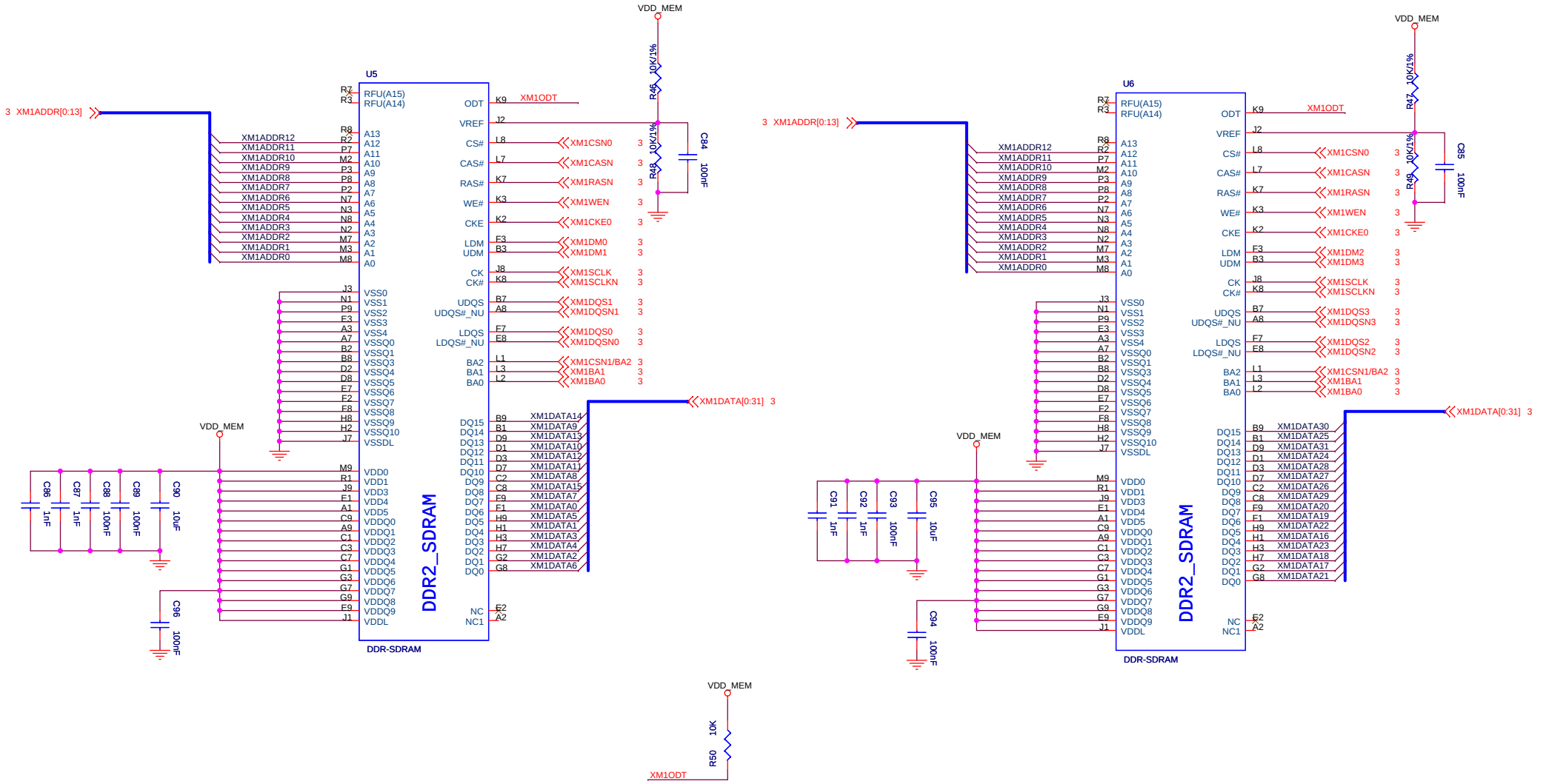

广州粤嵌通信科技股份有限公司		
Title: CORE_210		
Size: A3	Document Number: DDR2-CHANNEL1	Rev: V1.0
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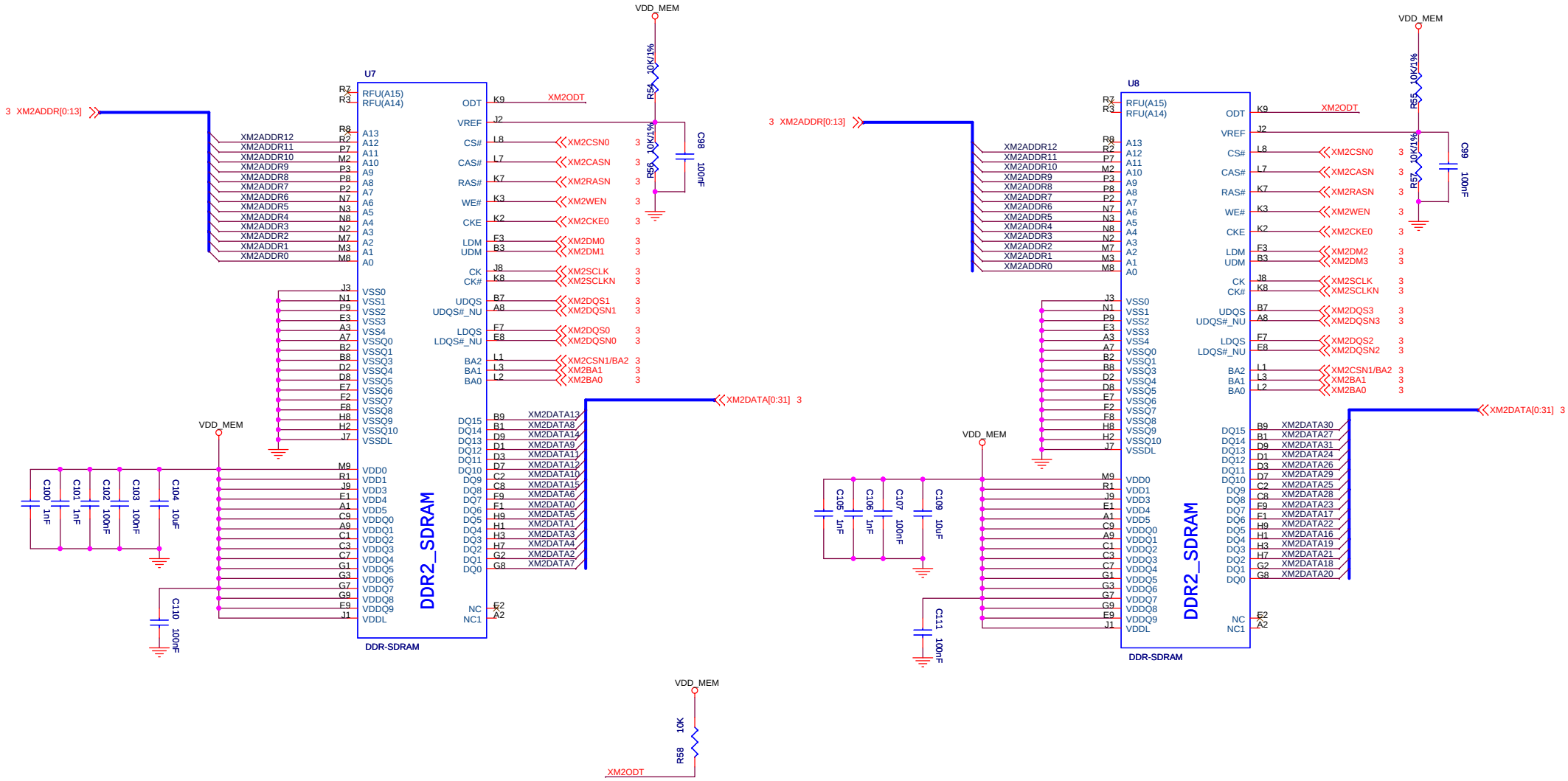

广州粤嵌通信科技股份有限公司		
Title: CORE_210		
Size: A3	Document Number: DDR2-CHANNEL2	Rev: V1.0
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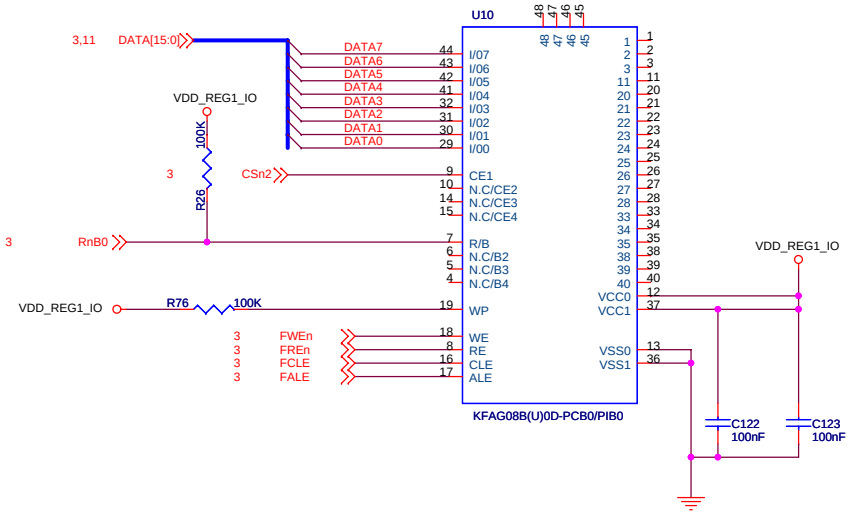
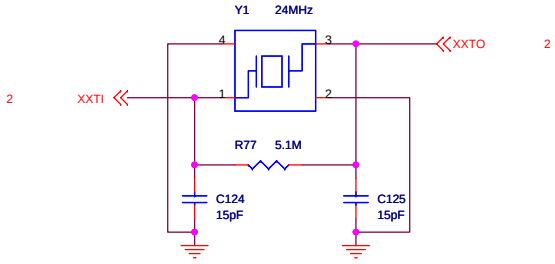
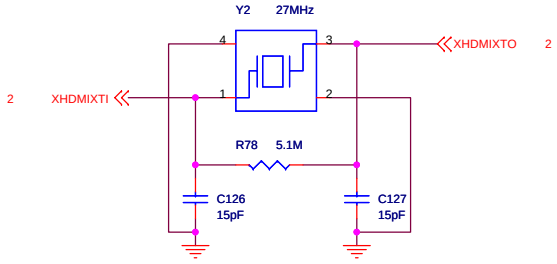
NAND FLASH



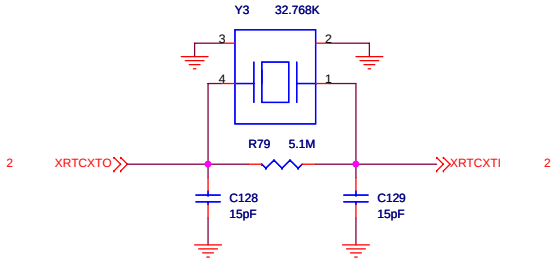
广州粤嵌通信科技股份有限公司		
Title: CORE_210		
Size: A3	Document Number: INAND & NAND FLASH	Rev: V1.0
Date: Thursday, July 12, 2012	Sheet 9 of 11	



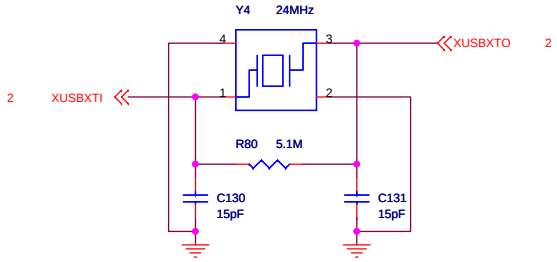
FED MAIN



FED HDMI



FED RTC



FED USB

广州粤嵌通信科技股份有限公司		
Title: CORE_210		
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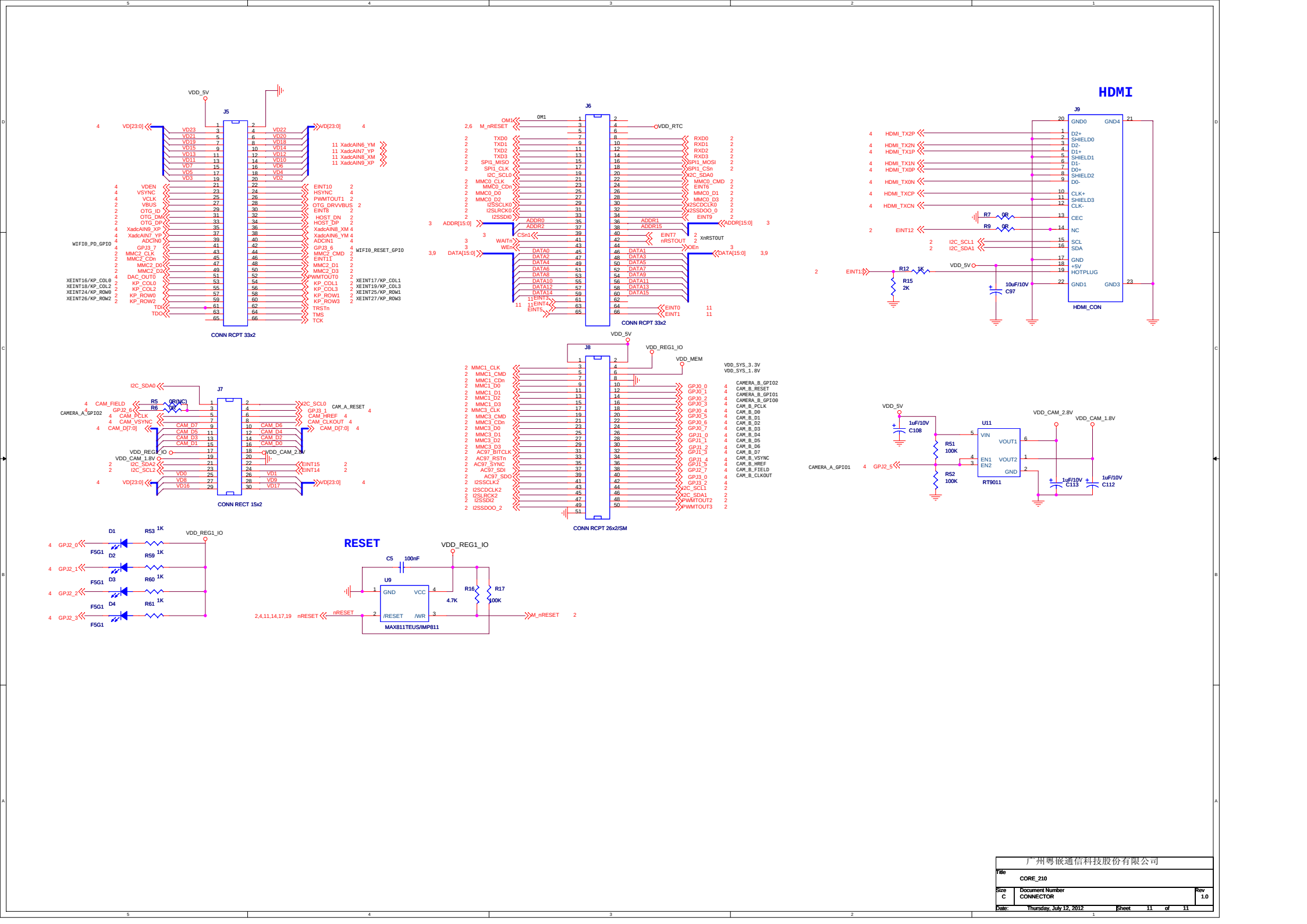
HDMI
J5
CONN RCPT 33x2
J6
CONN RCPT 33x2
J9
HDMI_CON
J7
CONN RECT 15x2
J8
CONN RCPT 26x2/SM
RESET
MAX811TEUS/IMP811
U11
RT9011
VDD_5V
VDD_REG1_IO
VDD_MEM
VDD_CAM_1.8V
VDD_CAM_2.8V
广州粤嵌通信科技股份有限公司
CORE_210
CONNECTOR
Thursday, July 12, 2012