Report - Project 1

Course: 431 Intro to Compute Architecture

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1. Method

Given an initial 18-dimensional parameters, we 'd like to explore the best parameters for some specific object function in the process of designing computer architecture. The 18-dimensional parameter vector is defined in the 'runprojectsuite.sh' file like the size of L1 instruction set, choice of branch predictor and so on. An exhaustive DSE simply tries out all possible combinations of parameter values to

find the absolute best design. However it will be very time-consuming. Thus we explore the parameters in a heuristic way. Actually it is a greedy method to find the best value for each dimension one by one. More specifically, we can test all the possible values in one dimension by priority and fix the values in other dimensions. Then select the best local value for the tested dimension. Doing this search method recursively until the performance won't be improved anymore or it meets one of terminal conditions.

In our case, we set the priority of parameters as [BP, Cache, Core, FPU]. That is, we test all the possible values in the dimensions related to BP first. Then find each local step for each dimension by the order of Cache, Core, FPU. After exploring all the 18 dimensions, go back to the initial state and restart exploring by the latest parameters we get from last iteration.

Two kinds of parameters are explored in order to optimize the two object functions: The "best" performing overall design (in term of the geometric mean of normalized execution time normalized across all benchmarks) and The most energy-efficient design (as measured by the lowest geometric mean of normalized energy-delay product [units of energy delay product are joule-seconds] across all benchmarks).

2. List of design point chosed by DSE

To optimize the best execution time, we have 70 design points.

iter	0	1	2	3	4	5	6
width	1	1	1	1	1	1	1
scheduling	r true	r true	r true	r true	r true	issue:inorde r true issue:wrong path false	r true
11block	8	8	8	8	8	8	8
dl1sets	1024	1024	1024	1024	1024	1024	1024
dllassoc	1	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024	1024
ul2block	64	64	64	64	64	64	64
ul2assoc	4	4	4	4	4	4	4
replacepoli cy	1	1	1	1	1	1	1
fpwidth	2	2	2	2	2	2	2
branchsetti ngs	bpred bimod bpred:bimod 2048	bpred 2lev bpred:2lev 1 1024 8 0	bpred 2lev bpred:2lev 4 256 8 0	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024
ras	2	2	2	2	1	4	8
btb	512 4	512 4	512 4	512 4	512 4	512 4	512 4
dl1lat	3	3	3	3	3	3	3
il11at	3	3	3	3	3	3	3
ul2lat	10	10	10	10	10	10	10
iter	7	8	<u>(</u>)	10	11	12
width	1	1		1	1	1	1
scheduling	issue:inor true	der issue:in true			ie:inorder is true	sue:inorder true	issue:inorder true

	issue:wrongpa					
	th false	th false	th false	th false	th false	th false
11block	8	8	8	8	16	32
dl1sets	1024	1024	1024	1024	1024	1024
dl1assoc	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	64	64	64	64	64	64
ul2assoc	4	4	4	4	4	4
replacepolic y	1	1	1	1	1	1
fpwidth	2	2	2	2	2	2
branchsettin gs	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024
ras	8	8	8	8	8	8
btb	128 16	256 8	1024 2	2048 1	2048 1	2048 1
dl1lat	3	3	3	3	4	5
il1lat	3	3	3	3	4	5
ul2lat	10	10	10	10	10	10
iter	13	14	15	16	17	18
iter width	13 1	14 1	15 1	16 1	17 1	18 1
	1	1	1	16 1 issue:inorder	1	1
width	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true
	issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	issue:inorder true issue:wrongpa
width scheduling	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false
width scheduling l1block	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32
width scheduling l1block dl1sets	issue:inorder true issue:wrongpa th false 32 64	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 256	issue:inorder true issue:wrongpa th false 32 512	issue:inorder true issue:wrongpa th false 32 2048	issue:inorder true issue:wrongpa th false 32 128
width scheduling l1block dl1sets dl1assoc	issue:inorder true issue:wrongpa th false 32 64 1	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 256	issue:inorder true issue:wrongpa th false 32 512	issue:inorder true issue:wrongpa th false 32 2048	1 issue:inorder true issue:wrongpa th false 32 128 2
width scheduling l1block dl1sets dl1assoc il1sets	issue:inorder true issue:wrongpa th false 32 64 1 1024	issue:inorder true issue:wrongpa th false 32 128 1	1 issue:inorder true issue:wrongpa th false 32 256 1 1024	1 issue:inorder true issue:wrongpa th false 32 512 1 1024	issue:inorder true issue:wrongpa th false 32 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 2 1024
width scheduling l1block dl1sets dl1assoc il1sets il1assoc	issue:inorder true issue:wrongpa th false 32 64 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 1024 1	issue:inorder true issue:wrongpa th false 32 256 1 1024 1	issue:inorder true issue:wrongpa th false 32 512 1 1024	issue:inorder true issue:wrongpa th false 32 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 2 1024 1
width scheduling llblock dllsets dllassoc illsets illassoc ul2sets	issue:inorder true issue:wrongpa th false 32 64 1 1024 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 1024 1 1024	1 issue:inorder true issue:wrongpa th false 32 256 1 1024 1 1024	1 issue:inorder true issue:wrongpa th false 32 512 1 1024 1 1024	issue:inorder true issue:wrongpa th false 32 2048 1 1024 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 2 1024 1 1024
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block	1 issue:inorder true issue:wrongpa th false 32 64 1 1024 1 1024 64	1 issue:inorder true issue:wrongpa th false 32 128 1 1024 1 1024 64	1 issue:inorder true issue:wrongpa th false 32 256 1 1024 1 1024 64	1 issue:inorder true issue:wrongpa th false 32 512 1 1024 1 1024 64	1 issue:inorder true issue:wrongpa th false 32 2048 1 1024 1 1024 64	1 issue:inorder true issue:wrongpa th false 32 128 2 1024 1 1024 64
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width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic	issue:inorder true issue:wrongpa th false 32 64 1 1024 1 1024 64 4	issue:inorder true issue:wrongpa th false 32 128 1 1024 1 1024 64 4	issue:inorder true issue:wrongpa th false 32 256 1 1024 1 1024 64 4 1 2	issue:inorder true issue:wrongpa th false 32 512 1 1024 1 1024 64 4	issue:inorder true issue:wrongpa th false 32 2048 1 1024 1 1024 64 4	1 issue:inorder true issue:wrongpa th false 32 128 2 1024 1 1024 64 4
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth	issue:inorder true issue:wrongpa th false 32 64 1 1024 1 1024 64 4 1 2 bpred comb	issue:inorder true issue:wrongpa th false 32 128 1 1024 1 1024 64 4 1 2 bpred comb	issue:inorder true issue:wrongpa th false 32 256 1 1024 1 1024 64 4 1 2 bpred comb	issue:inorder true issue:wrongpa th false 32 512 1 1024 1 1024 64 4 1 2 bpred comb	issue:inorder true issue:wrongpa th false 32 2048 1 1024 1 1024 64 4 1 2 bpred comb	issue:inorder true issue:wrongpa th false 32 128 2 1024 1 1024 64 4 1 2 bpred comb
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth branchsettin	issue:inorder true issue:wrongpa th false 32 64 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 256 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 512 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 2048 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 2 1024 1 1024 64 4 1 2 bpred comb bpred:comb
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth branchsettin gs	issue:inorder true issue:wrongpa th false 32 64 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb 1024	l issue:inorder true issue:wrongpa th false 32 128 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb 1024	issue:inorder true issue:wrongpa th false 32 256 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb 1024	issue:inorder true issue:wrongpa th false 32 512 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb 1024	issue:inorder true issue:wrongpa th false 32 2048 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb 1024	l issue:inorder true issue:wrongpa th false 32 128 2 1024 1 1024 64 4 1 2 bpred comb bpred:comb 1024
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth branchsettin	issue:inorder true issue:wrongpa th false 32 64 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 256 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 512 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 2048 1 1024 1 1024 64 4 1 2 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 2 1024 1 1024 64 4 1 2 bpred comb bpred:comb

dl1lat	1	2	3	4	6	4
il1lat	5	5	5	5	5	5
ul2lat	10	10	10	10	10	10
iter	19	20	21	22	23	24
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
seneduning	issue:wrongpa					
	th false					
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dl1assoc	4	1	1	1	1	1
il1sets	1024	64	128	256	512	2048
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	64	64	64	64	64	64
ul2assoc	4	4	4	4	4	4
replacepolic y	1	1	1	1	1	1
fpwidth	2	2	2	2	2	2
branchsettin gs	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	6	2	2	2	2	2
il1lat	5	1	2	3	4	6
ul2lat	10	10	10	10	10	10
iter	25	26	27	28	29	30
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true issue:wrongpa	true	true	true	true	true
	th false					
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dllassoc	1	1	1	1	1	1
	2048	2048	2048	2048	2048	2048
il1sets	2010					
il1sets il1assoc	1	1	1	1	1	1
		1 4096	1 1024	1 1024	1 1024	1024

ul2assoc	4	4	4	2	8	2
replacepolic y	1	1	1	1	1	f
fpwidth	2	2	2	2	2	2
branchsettin gs	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dlllat	2	2	2	2	2	2
il1lat	6	6	6	6	6	6
ul2lat	11	12	11	9	13	9
iter	31	32	33	34	35	36
width	1	2	4	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	false	true	true
senedumg	issue:wrongpa					
	th false	th false	th false	th true	th false	th false
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dl1assoc	1	1	1	1	1	1
il1sets	2048	2048	2048	2048	2048	2048
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	2	2
replacepolic y	r	r	r	r	1	1
fpwidth	2	2	2	2	1	4
branchsettin gs	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dlllat	2	2	2	2	2	2
il1lat	6	6	6	6	6	6
ul2lat	9	9	9	9	9	9
iter	37	38	39	40	41	42
width	1	1	1	1	1	1
scheduling	issue:inorder true	issue:inorder true	issue:inorder true	issue:inorder true	issue:inorder true	issue:inorder true

	issue:wrongpa	issue:wrongpa	issue:wrongpa	issue:wrongpa	issue:wrongpa	issue:wrongpa
	th false	th false	th false	th false	th false	th false
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dl1assoc	1	1	1	1	1	1
il1sets	2048	2048	2048	2048	2048	2048
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	2	2
replacepolic y	1	1	1	1	1	1
fpwidth	8	1	1	1	1	1
branchsettin gs	bpred comb bpred:comb 1024	bpred nottaken	bpred bimod bpred:bimod 2048	bpred 2lev bpred:2lev 1 1024 8 0	bpred 2lev bpred:2lev 4 256 8 0	bpred comb bpred:comb 1024
ras	8	8	8	8	8	1
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	2	2	2	2
il1lat	6	6	6	6	6	6
ul2lat	9	9	9	9	9	9
iter	43	44	45	46	47	48
iter width	43 1	44 1	45 1	46 1	47 1	48 1
	1	1	1	1	47 1 issue:inorder	1
width	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true	1 issue:inorder true
	issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	1 issue:inorder true issue:wrongpa	issue:inorder true issue:wrongpa
width scheduling	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false	1 issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false	issue:inorder true issue:wrongpa th false
width scheduling l1block	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32	issue:inorder true issue:wrongpa th false 32
width scheduling l1block dl1sets	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128
width scheduling l1block dl1sets dl1assoc	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	issue:inorder true issue:wrongpa th false 32 128	1 issue:inorder true issue:wrongpa th false 32 128 1
width scheduling l1block dl1sets dl1assoc il1sets	issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048	issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048
width scheduling llblock dllsets dllassoc illsets illassoc	issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048	issue:inorder true issue:wrongpa th false 32 128 1 2048	1 issue:inorder true issue:wrongpa th false 32 128 1 2048
width scheduling llblock dllsets dllassoc illsets illassoc ul2sets	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024
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width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1	l issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1	l issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1 bpred comb	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 the product of the comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1 bpred comb	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1 bpred comb	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1 bpred comb
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth branchsettin	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth branchsettin gs	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb 1024	l issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 l bpred comb bpred:comb 1024	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1 bpred comb bpred:comb 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb 1024	1 issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb 1024
width scheduling 11block dl1sets dl1assoc il1sets il1assoc ul2sets ul2block ul2assoc replacepolic y fpwidth branchsettin	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb	issue:inorder true issue:wrongpa th false 32 128 1 2048 1 1024 128 2 1 bpred comb bpred:comb

dl1lat	2	2	2	2	2	2
il11at	6	6	6	6	6	6
ul2lat	9	9	9	9	9	9
		-				-
iter	49	50	51	52	53	54
width	1	1	1	1	1	1
***	issue:inorder	issue inorder	issue inorder	issue:inorder	issue inorder	issue inorder
1 1 1.	true	true	true	true	true	true
scheduling	issue:wrongpa					
	th false					
11block	16	32	32	32	32	32
dl1sets	128	64	256	512	1024	2048
dl1assoc	1	1	1	1	1	1
il1sets	2048	2048	2048	2048	2048	2048
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	2	2
replacepolic	_	_	_	_	_	_
у	1	1	1	1	1	1
fpwidth	1	1	1	1	1	1
branchsettin	bpred comb					
gs	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb
53	1024	1024	1024	1024	1024	1024
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	1	1	3	4	5	6
il1lat	5	6	6	6	6	6
ul2lat	9	9	9	9	9	9
iter	55	56	57	58	59	60
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
scheduning	issue:wrongpa					
	th false					
11block	32	32	32	32	32	32
dllsets	128	128	128	128	128	128
dl1assoc	2	4	1	1	1	1
il1sets	2048	2048	64	128	256	512
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	128	128	128	128	128	128

ul2assoc	2	2	2	2	2	2
replacepolic y	1	1	1	1	1	1
fpwidth	1	1	1	1	1	1
branchsettin gs	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	4	6	2	2	2	2
il1lat	6	6	1	2	3	4
ul2lat	9	9	9	9	9	9
iter	61	62	63	64	65	66
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
senedaning	issue:wrongpa i					
	th false					
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dl1assoc	1	1	1	1	1	1
il1sets	1024	2048	2048	2048	2048	2048
il1assoc	1	1	1	1	1	1
ul2sets	1024	2048	4096	1024	1024	1024
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	4	8	2
replacepolic y	1	1	1	1	1	f
fpwidth	1	1	1	1	1	1
branchsettin gs	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dlllat	2	2	2	2	2	2
il1lat	5	6	6	6	6	6
ul2lat	9	10	11	11	13	9
iter	67	68	69	70)	
width	1	2	4	1		
scheduling	issue:inorde true	r issue:inore true	der issue:inc true	order issue:in		

i	ssue:wrongpath	issue:wrongpath	issue:wrongpath	issue:wrongpath
	false	false	false	true
11block	32	32	32	32
dl1sets	128	128	128	128
dl1assoc	1	1	1	1
il1sets	2048	2048	2048	2048
il1assoc	1	1	1	1
ul2sets	1024	1024	1024	1024
ul2block	128	128	128	128
ul2assoc	2	2	2	2
replacepolicy	r	r	r	r
fpwidth	1	1	1	1
branchsettings	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024
ras	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	2	2
il1lat	6	6	6	6
ul2lat	9	9	9	9

To explore energy efficient, we have 73 design points.

iter	0	1	2	3	4	5
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat :	issue:wrongpat	issue:wrongpat
	h false	h false	h false	h false	h false	h false
11block	8	8	8	8	8	8
dl1sets	1024	1024	1024	1024	1024	1024
dllassoc	1	1	1	1	1	1
il1 sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	64	64	64	64	64	64
ul2assoc	4	4	4	4	4	4
replacepolicy	1	1	1	1	1	1
fpwidth	2	2	2	2	2	2

branchsetting s	bpred bimod bpred:bimod 2048	bpred 2lev bpred:2lev 1 1024 8 0	bpred 2lev bpred:2lev 4 256 8 0	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024
ras	2	2	2	2	1	4
btb	512 4	512 4	512 4	512 4	512 4	512 4
dl1lat	3	3	3	3	3	3
il11at	3	3	3	3	3	3
ul2lat	10	10	10	10	10	10
iter	6	7	8	9	10	11
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
Scheduling	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat
	h false	h false	h false	h false	h false	h false
11block	8	8	8	8	8	16
dl1sets	1024	1024	1024	1024	1024	1024
dllassoc	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	1024	1024	1024	1024	1024	1024
ul2block	64	64	64	64	64	64
ul2assoc	4	4	4	4	4	4
replacepolicy	1	1	1	1	1	1
fpwidth	2	2	2	2	2	2
branchsetting s	bpred comb	bpred comb	bpred comb	bpred comb	bpred comb	bpred comb bpred:comb
	1024	1024	1024 8	1024 8	1024	1024
ras	8	8			8	8
btb	512 4	128 16	256 8	1024 2	2048 1	2048 1
dlllat	3	3	3	3	3	4
il1lat	3	3	3	3	3	4
ul21at	10	10	10	10	10	10
iter	12	13	14	15	16	17
width	1	1	1	1	1	1
scheduling	issue:inorder true	issue:inorder true	issue:inorder true	issue:inorder true	issue:inorder true	issue:inorder true

	issue·wr	ongnat issue	-wrongnat is	ssue·wrongn:	at issue·wron	nonat issue·v	wrongnat iss	ue:wrongpat
	h fal		n false	h false	h false		alse	h false
11block	32		32	32	32		32	32
dl1sets	102		64	128	256		512	2048
dl1assoc	2 1		1	1	1		1	1
il1sets	102	24	1024	1024	1024		024	1024
illassoc	1		1	1	1		1	1
ul2sets	102	24	1024	1024	1024	10	024	1024
ul2block	k 64	:	64	64	64	(64	64
ul2assoc	2 4		4	4	4		4	4
replacepoli	icy 1		1	1	1		1	1
fpwidth	2		2	2	2		2	2
1 1 4	. bpred	comb bp	red comb	bpred comb	bpred co	omb bpre	d comb	opred comb
branchsetti s	ing bpred:	comb bpi	red:comb	bpred:comb	bpred:co	mb bpred	d:comb b	pred:comb
3	102	24	1024	1024	1024	10	024	1024
ras	8		8	8	8		8	8
btb	2048	3 1 2	2048 1	2048 1	2048	1 20	48 1	2048 1
dl1lat	5		1	2	3		4	6
il11at	5		5	5	5		5	5
ul2lat	10)	10	10	10		10	10
iter	18	19	20	21	22	23	24	25
width	1	1	1	1	1	1	1	1
schedulin g	er true issue:wron	er true issue:wron	issue:inord er true issue:wron gpath false	er true issue:wron	er true issue:wron	er true issue:wron	er true issue:wron	
11block	32	32	32	32	32	32	32	32
dllsets	128	128	128	128	128	128	128	128
dl1assoc	2	4	1	1	1	1	1	1
il1sets	1024	1024	64	128	256	512	2048	1024
illassoc	1	1	1	1	1	1	1	2
ul2sets	1024	1024	1024	1024	1024	1024	1024	1024
ul2block	64	64	64	64	64	64	64	64
ul2assoc	4	4	4	4	4	4	4	4
replacepol icy		1	1	1	1	1	1	1
fpwidth	2	2	2	2	2	2	2	2

	bpred							
branchsett	comb							
ings	bpred:com							
	b 1024							
ras	8	8	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	4	6	2	2	2	2	2	2
il1lat	5	5	1	2	3	4	6	7
ul2lat	10	10	10	10	10	10	10	10

iter	26	27	28	29	30	31
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
scheduning	$is sue \hbox{:} wrong pat$	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat
	h false	h false	h false	h false	h false	h false
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dllassoc	1	1	1	1	1	1
il1 sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	512	2048	4096	512	512	512
ul2block	64	64	64	128	128	128
ul2assoc	4	4	4	4	2	8
replacepolicy	1	1	1	1	1	1
fpwidth	2	2	2	2	2	2
branchsetting	bpred comb	bpred comb	bpred comb	bpred comb	bpred comb	bpred comb
S	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb
S .	1024	1024	1024	1024	1024	1024
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	2	2	2	2
il11at	5	5	5	5	5	5
ul2lat	9	11	12	10	8	12

iter	32	33	34	35	36	37
width	1	1	1	2	4	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	false
scheduning	issue:wrongpat i	issue:wrongpat i	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat
	h false	h true				
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dl1assoc	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	512	512	512	512	512	512
ul2block	128	128	128	128	128	128
ul2assoc	16	2	2	2	2	2
replacepolicy	1	f	r	r	r	r
fpwidth	2	2	2	2	2	2
branchsetting s	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	2	2	2	2
il1lat	5	5	5	5	5	5
ul2lat	14	8	8	8	8	8
iter	38	39	40	41	42	43
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
\mathcal{E}	issue:wrongpat					
	h false					
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dl1assoc	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	512	512	512	512	512	512

ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	2	2
replacepolicy	1	1	1	1	1	1
fpwidth	1	4	8	1	1	1
branchsetting s	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred nottaken	bpred bimod bpred:bimod 2048	bpred 2lev bpred:2lev 1 1024 8 0
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	2	2	2	2
il11at	5	5	5	5	5	5
ul2lat	8	8	8	8	8	8
iter	44	45	46	47	48	49
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
م ماه م طبرانه م	true	true	true	true	true	true
scheduling	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat
	h false	h false	h false	h false	h false	h false
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dllassoc	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	512	512	512	512	512	512
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	2	2
replacepolicy	1	1	1	1	1	1
fpwidth	1	1	1	1	1	1
branchsetting s	bpred 2lev bpred:2lev 4 256 8 0	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024	bpred comb bpred:comb 1024
ras	8	1	2	4	8	8
btb	2048 1	2048 1	2048 1	2048 1	128 16	256 8
dl1lat	2	2	2	2	2	2
il11at	5	5	5	5	5	5
ul2lat	8	8	8	8	8	8
iter	50	51	52	53	54	55

width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
scheduning	issue:wrongpat	issue:wrongpat :	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat
	h false	h false	h false	h false	h false	h false
11block	32	32	16	32	32	32
dl1sets	128	128	128	64	256	512
dllassoc	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	512	512	512	512	512	512
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	2	2
replacepolicy	1	1	1	1	1	1
fpwidth	1	1	1	1	1	1
branchaattina	bpred comb	bpred comb	bpred comb	bpred comb	bpred comb	bpred comb
branchsetting s	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb
5	1024	1024	1024	1024	1024	1024
ras	8	8	8	8	8	8
btb	512 4	1024 2	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	1	1	3	4
il1lat	5	5	4	5	5	5
ul2lat	8	8	8	8	8	8
iter	56	57	58	59	60	61
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
scheduling	issue:wrongpat:	issue:wrongpat :	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat
	h false	h false	h false	h false	h false	h false
11block	32	32	32	32	32	32
dl1sets	1024	128	128	128	128	128
dl1assoc	1	2	4	1	1	1
il1sets	1024	1024	1024	64	128	256
il1assoc	1	1	1	1	1	1
ul2sets	512	512	512	512	512	512
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	2	2
replacepolicy	1	1	1	1	1	1
fpwidth	1	1	1	1	1	1

branchsetting s	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	5	4	6	2	2	2
il1lat	5	5	5	1	2	3
ul2lat	8	8	8	8	8	8
iter	62	63	64	65	66	67
width	1	1	1	1	1	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
scheduling	true	true	true	true	true	true
scheduling	issue:wrongpat i	issue:wrongpat i	issue:wrongpat	issue:wrongpat	issue:wrongpat :	issue:wrongpat
	h false					
11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dl1assoc	1	1	1	1	1	1
il1sets	512	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	512	1024	2048	4096	512	512
ul2block	128	128	128	128	128	128
ul2assoc	2	2	2	2	4	8
replacepolicy	1	1	1	1	1	1
fpwidth	1	1	1	1	1	1
branchsetting s	bpred comb bpred:comb 1024					
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	2	2	2	2
il1lat	4	5	5	5	5	5
ul2lat	8	9	10	11	10	12
iter	68	69	70	71	72	73
width	1	1	1	2	4	1
	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder	issue:inorder
a als a declines	true	true	true	true	true	false
scheduling	issue:wrongpat i	issue:wrongpat i	issue:wrongpat	issue:wrongpat	issue:wrongpat	issue:wrongpat
	h false	h true				

11block	32	32	32	32	32	32
dl1sets	128	128	128	128	128	128
dllassoc	1	1	1	1	1	1
il1sets	1024	1024	1024	1024	1024	1024
il1assoc	1	1	1	1	1	1
ul2sets	512	512	512	512	512	512
ul2block	128	128	128	128	128	128
ul2assoc	16	2	2	2	2	2
replacepolicy	1	f	r	r	r	r
fpwidth	1	1	1	1	1	1
branchsetting	bpred comb					
S	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb	bpred:comb
5	1024	1024	1024	1024	1024	1024
ras	8	8	8	8	8	8
btb	2048 1	2048 1	2048 1	2048 1	2048 1	2048 1
dl1lat	2	2	2	2	2	2
il11at	5	5	5	5	5	5
ul2lat	14	8	8	8	8	8

3. Table

Select the best parameters for Performance and EDP as the following:

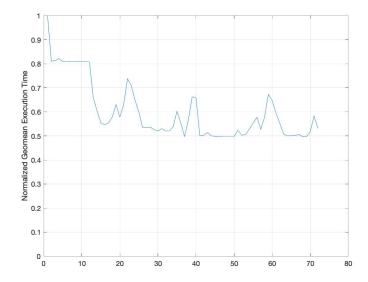
Parameters	Performance	EDP
width	Value: 1 Reason: More instruction pipeline increases instruction latency hence to choose a less instruction pipeline value will improve performance.	Value: 1 Reason: More instruction pipeline is more hard to make a correct prediction, it means higher energy consume. Hence the less instruction pipeline can save energy.
scheduling	Value: issue:inorder true issue:wrongpath false Reason: Under In-order instruction execution, instructions are statically scheduled by the hardware. It means faster clock cycle and improves the performance.	Value: issue:inorder true issue:wrongpath false Reason: Under In-order instruction execution, instructions are statically scheduled by the hardware. It means fewer transistors and saves the energy.
l1block	Value:32 Reason: Larger block size means a greater bandwidth efficiency and improves the accuracy of prediction. It means it can perform faster.	Value:32 Reason: Larger block size means a greater bandwidth efficiency and improves the accuracy of prediction. It means less energy consume.
dl1sets	Value:32 Reason: A block of memory replacement is restricted to a set of	Value:32 Reason: A block of memory replacement is restricted to a set of cache lines by cache

	cache lines by cache replacement policy. To have less sets means higher hit rate when it try to find the target block. In sum, less set	replacement policy. To have less sets means higher hit rate when it try to find the target block. In sum, less set saves energy of finding the correct target block.
dl1assoc	improves the performance. Value:1 Reason: One way set-associative is also called direct mapped. It has less comparators and multiplexer. So, it can perform faster.	Value:1 Reason: One way set-associative is also called direct mapped. It has less comparators and multiplexer. So, the energy consume will be less.
il1sets	Value:2048 Reason: A block of memory replacement is restricted to a set of cache lines by cache replacement policy. To have less sets means higher hit rate when it try to find the target block. In sum, less set improves the performance.	Value:1024 Reason: A block of memory replacement is restricted to a set of cache lines by cache replacement policy. To have less sets means higher hit rate when it try to find the target block. In sum, less set saves energy of finding the correct target block.
il1assoc	Value:1 Reason: One way set-associative is also called direct mapped. It has less comparators and multiplexer. So, it can perform faster.	Value:1 Reason: One way set-associative is also called direct mapped. It has less comparators and multiplexer. So, the energy consume will be less
ul2sets	Value:1024 Reason: A block of memory replacement is restricted to a set of cache lines by cache replacement policy. To have less sets means higher hit rate when it try to find the target block. In sum, less set improves the performance.	Value:512 Reason: A block of memory replacement is restricted to a set of cache lines by cache replacement policy. To have less sets means higher hit rate when it try to find the target block. In sum, less set saves energy of finding the correct target block.
ul2block	Value:128 Reason: Larger block size means a greater bandwidth efficiency and improves the accuracy of prediction. It means it can perform faster.	Value:128 Reason: Larger block size means a greater bandwidth efficiency and improves the accuracy of prediction. It means it saves energy.
ul2assoc	relatively less comparators and multiplexer and relatively high hit rate. So, it improves performance.	Value:2 Reason: Two way set-associative has relatively less comparators and multiplexer and relatively high hit rate. So, it saves energy.
replacepolicy	Value:1 Reason: LRU replaces the page which is least recently used, it increases the hit rate and improves the performance.	Value:1 Reason: LRU replaces the page which is least recently used, it increases the hit rate and saves energy.
fpwidth	Value:1 Reason: Wider floating bit width	Value:1 Reason: Wider floating bit width increases

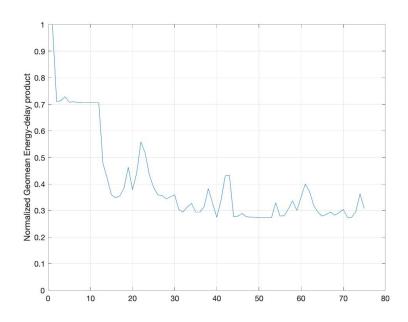
increases accuracy by requiring more accuracy by requiring more FP FP multiplication, it means low multiplication, it means high energy performance. consume. Value: bpred comb bpred:comb 1024 Value: bpred comb bpred:comb 1024 Reason: A combination of Branch branchsettings prediction can achieve a better prediction can achieve a better accuracy on accuracy on prediction. It means prediction. It means low energy consume. high performance. Value:8 Value:8 Reason: Larger stack size means Reason: Larger stack size means more more variable can be store and has a variable can be store and has a faster ras faster response reaction of return the response reaction of return the address. So, address. So, it increases the it saves energy. performance Value: 128 16 Value:1024 2 Reason: It has relatively high hit rate Reason: It has relatively high hit rate with a btb with a relatively low energy relatively low energy consume to maintain. consume to maintain.

4. Plots

1. plot the value of normalized geomean execution time (NGET) during the design space exploration for the best performant design. In the file '/logs/ExecuteTime.log', we draw all the geomean excution time (NGET) as the y-axis.

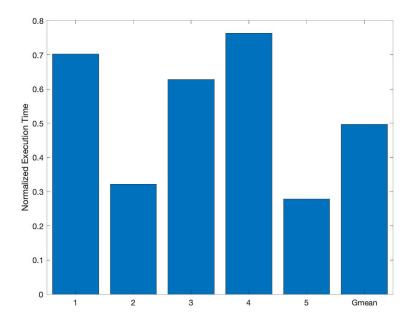


2. normalized geomean of energy-delay product. In the file '/logs/EnergyEfficiency.log', we draw all the normalized geomean of energy-delay product as the y-axis.



3. Bar chart showing normalized per–benchmark execution time and geomean normalized execution time for the best performing design. In the '/logs/ExecuteTime.best', bestPerformantConfig, GeomeanEDPNorm, geomeanExecTimeNorm, GeoEDP, GeoTime, [benchmarkExecTime, benchmarkNormalizedExecTime] (repeated 5 times).

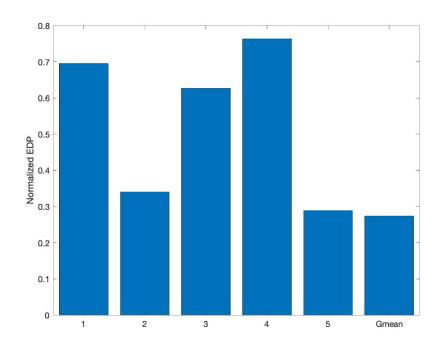
We select 5 benchmarkNormalizedExecTime as the x label (1,2,3,4,5), and compare them to the geomeanExecTimeNorm.



4.Bar chart showing per-benchmark normalized energy-delay product and geomean normalized energy delay product for the most energy-effcient design found. In the '/logs/EnergyEfficiency.best', bestEDPConfig,

GeomeanEDPNorm, geomeanExecTimeNorm, GeoEDP, GeoTime, [benchmarkEDP, benchmarkNormalizedEDP] (repeated 5 times) are presented.

We compare the benchmarkNormalizedEDP to GeomeanEDPNorm as the following bar chart.



5. Instead of testing all the 18 dimensional parameter, maybe we can fix some parameters in advance by the prior knowledge. For example, we always chose a better branch prediction method. Besides, maybe we can chose more initial state to find the best parameters locally, then select the optimal one.

6. Insights gained from this project

- 1. This method will usually give us a local optimal by testing different value one by one dimension separately. However, there are some prior knowledge gained from computer architecture that will be helpful for us to design the parameters. For example, usually more ALUs may increase performance by extracting more ILP. And a better design Branch Prediction method will be helpful to improve it too.
- 2. It doesn't means that the large size of L1 cache or block size or more ALUs can promise a better performance. Parameters are affected to each other. We can't hope to get a better performance by simply enhancing the volume of hardware.