

VgaSim Manual

for 1.0.0 alpha version

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Introduction

VgaSim is an open source project which simulates a VGA screen connected to your VHDL design. Simulated signals from your design will handle the virtual VGA screen such as it were real. The screen will loop the screens you simulate not in real time, the time between screens is no yet implemented and it will depend on your CPU speed.

VgaSim works with VHDL and VeriLog simulators such as ModelSim and GHDL porting the output simulation file as screens handled by a VGA Monitor. It use five signals to generate the images, this are Horizontal Sync, Vertical Sync, Red, Green and Blue.

Arguments

VgaSim is a terminal or command line application, thats why it accepts arguments to select different options. Because VgaSim is in alpha these arguments are limited.

<i>vgasim -h</i> or <i>vgasim --help</i>	prints help message
<i>vgasim -V</i> or <i>vgasim --version</i>	prints VgaSim version information
<i>vgasim -i</i> or <i>vgasim --input</i>	select input file

Although is specify in the help message, pipe function from GHDL is not yet implemented.

Usage

The input file of vgasim must be text file. This file contains the information from the VHDL or VeriLog design to process the VGA Screens, this information is provide by arranging the five signals needed in a sequence of 1's and 0's in the following order HS VS RED GREEN BLUE, each line in the text file represents a 40ns transition, and each line could have any text at the beginning but only the signals states at the end one after another. This is an example file:

```
40ns      00000
80ns      10000
120ns     11000
160ns     11001
.
.
4000ns    10110
```

This file is generated automatically by ModelSim as explained in the following chapter.

Once the data is reeded, the screens will start to appear one after another, not in real time. When the last screen is show, it will loop again to the first one showing an “again” sign in the bottom left corner indicating that the screen are looping again.

Simulating will take some time before starting due to screen conversion, this is normal and it will depends on the simulated time.

As you can notice, it will only display 8 colors, based on the combination on RED, GREEN and BLUE signals. Also the only mode available at the moment is 640x480 @ 60Hz, thats why we use a 40ns basis for the input file.

Input File

The easiest way to get the input file is using ModelSim in GUI Mode, you must generate a test bench of your design having at least the five signals needed. The following steps show how to obtain the file, you must know how to use ModelSim as this manual is not intended for that.

1. Once everything is compiled, you should simulate your design.
2. Add the five signals to the wave.
3. In View open List
4. Drag from wave the five signals in the following order HS VS RED GREEN BLUE as shown in Fig.1. The names of the signals is not important, only the order and the tree arrangement.
5. Configure the List view in Tools → List Preferences... using the following options under Triggers: Deltas: *No Deltas*; Trigger On: *Strobe Only*; Strobe Period: *40ns*; Other options leave untouched, check Fig.2 for details.
6. Simulate the design for a reasonable period, make sense that only one screen takes 16ms approximately to print, thus 100ms – 200ms is a appropriate time for testing.
7. Once simulated and loaded the data in List, save the list in File → Save As → TSSI...
8. Save the file and use it as the input file for VgaSim

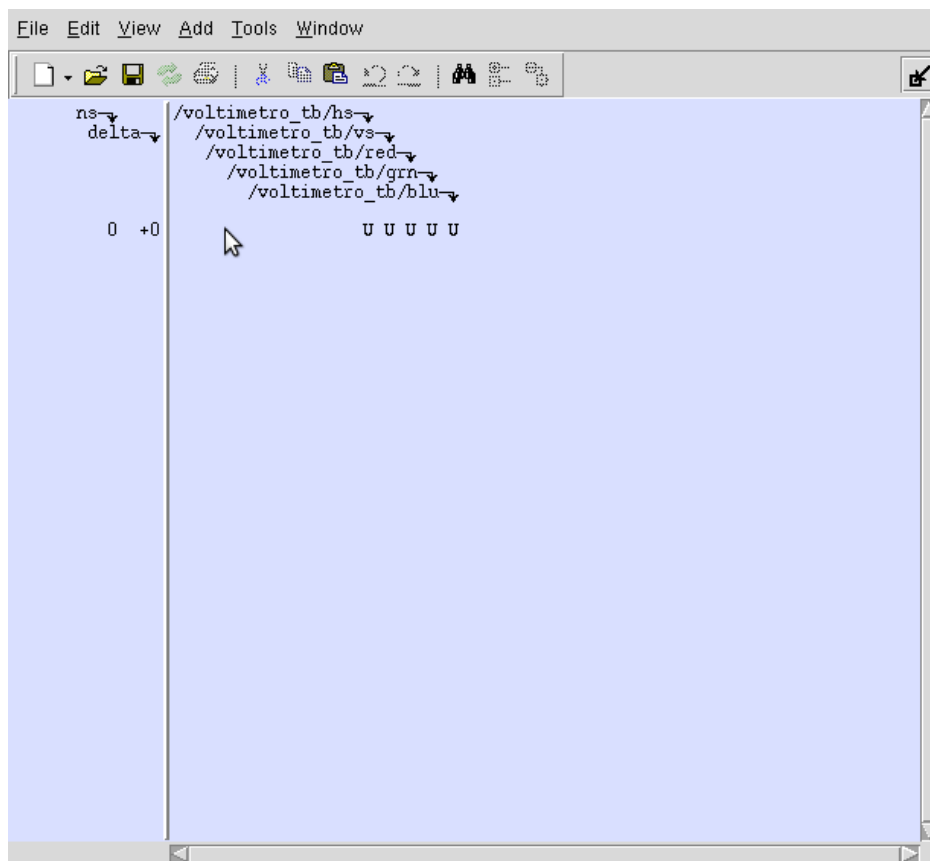


Fig.1, signals arrangement and order.

Window Properties Triggers

Deltas:

☐ Expand Deltas ☐ Collapse Deltas ☒ No Deltas

Trigger On:

☐ Signal Change ☒ Strobe

Strobe Period: 40 ns

First Strobe at: 0 ns

Trigger Gating:

☐ Use Gating Expression

Expression:

On Duration: 0 ns

OK Cancel Apply

Fig.2, List Preferences.