1. \_\_\_\_\_ is not a kind of random access memory.

A. DRAM B. SRAM C. Floppy disk D. Cache

2. \_\_\_\_\_ is not the basic functional unit of a computer.

A. Input unit B. Network interface card C. Memory D. Control unit

3. \_\_\_\_\_ addressing mode only exists in CISC-style processors.

A. Indirect B. Immediate C. Index D. Register indirect

4. \_\_\_\_\_ is not a kind of cache mapping scheme.

A. Fully associative mapping B. set associative mapping

C. Segmentation with paging D. Direct mapping

5. In program-controlled IO, the processor always polls \_\_\_\_\_\_\_ register in the IO interface to see if the IO device is ready.

A. status B. data C. control D. none of above

6. The functions of the IO interface do not include \_\_\_\_\_.

A. device communication B. instruction decoding

C. error detection D. control and signaling

7. Which of the following statements is true for memory-mapped IO?

A. IO devices and memory use separate address spaces.

B. Input/Output operations of the devices look different from memory read/write.

C. The instructions which can access memory can not be used to access IO devices.

D. The address space for the memory is reduced.

8. \_\_\_\_\_ is a kind of DMA transfer mode.

A. Direct mode B. Burst mode C. Indirect mode D. Relative mode

9. Which of the following statements is true in a CISC-style processor.

A. Each instruction fits in a single word.

B. It has a small set of instructions.

C. A load/store architecture is used.

D. Autoincrement addressing mode can be used.

10. A microprogram is stored in \_\_\_\_\_.

A. control store B. microinstructions C. control word D. micro memory

1. Assuming that register R3 contains a number 200, register R5 contains a number 100, and the memory is byte-addressable, what is the effective address in each of the following cases.

(1) -(R5) (2) (R3)+ (3) 20(R3,R5)

2. In a 16-bit floating-point number format, the most significant bit is the sign bit, the following 6 bits are for excess -31 exponent, and the remaining 9 bits are for normalized mantissa with an implied 1 to the left of the binary point.

(1) What is the 16-bit floating-point representation of -36.

(2) What is the decimal equivalent of the floating-point number 0 100010 010100000.

3. Describe the differences between interrupt-service routine and subroutine call.

4. How many types of pipeline hazards. What are they. Which hazard is caused by data dependencies. And which hazard is caused by resource limitation.

1. Design a 32Kx32 memory using 4Kx8 memory chips.

(1) How many rows and columns are the memory chips organized.

(2) How many bits are required for the memory chip select.

(3) Draw the implementation figure of the 32Kx32 memory.

2. Assume that a computer's instruction length is 15 bits, and the length of operand address is 4 bits. Design four types of instructions: three-address instructions, two-address instructions, one-address instructions, and zero-address instruction. Please describe the design of the instruction format and specify the number of each type of instructions.

3. Show A➗B on the 5-bit unsigned numbers A=11010 and B=01001 using non-restoring division.

4. Consider the following instructions at given hexadecimal addresses in the memory.

0x0010 Add R5,R1,R2

0x0014 Subtract R6,R5,#8

0x0018 Add R7,R5,#12

0x001C Subtract R8,R1,R2

Registers R1,R2 and R5 contain decimals 30, 400 and 50 respectively. The instructions are executed in a computer with a five-stage pipeline. The first instruction is fetched in clock cycle 1, and the remaining instructions are fetched in successive cycles.

(1) Draw a diagram showing the flow of the instructions through the pipeline, assuming that the pipeline provides no forwarding paths.

(2) Draw a diagram showing the flow of the instructions through the pipeline, assuming that the pipeline provides forwarding paths to the ALU from registers RY and RZ.

(3) Write down the contents of registers IR, PC, RA, RB, RZ and RY in the pipeline with operand forwarding during cycles 2 to 8.

5. In a 2-way set associative mapped cache consisting of eight words, each cache line can hold two 32-bit words. The memory is byte-addressable. The processor reads data sequentially from the following memory addresses which are represented by hexadecimal numbers: 18, 14, 1C, 20, 2C, 48.

Assume that the cache is initially empty. Show the contents of the cache (denoted by the memory addresses) at the end of each data read. LRU replacement algorithm is used.