SPI Protocol

Team Members:

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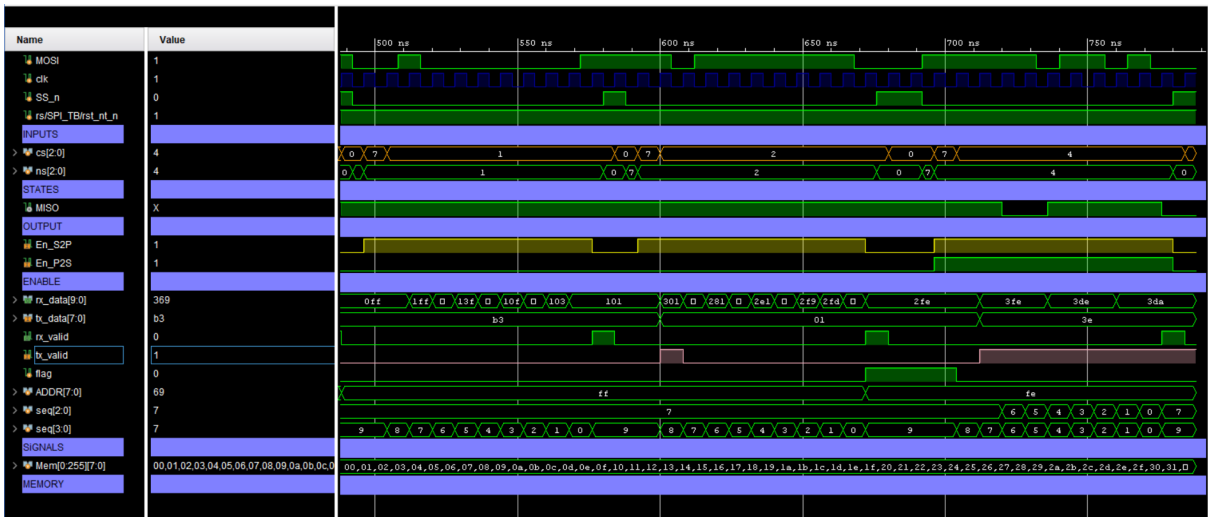
Snippets from the waveforms

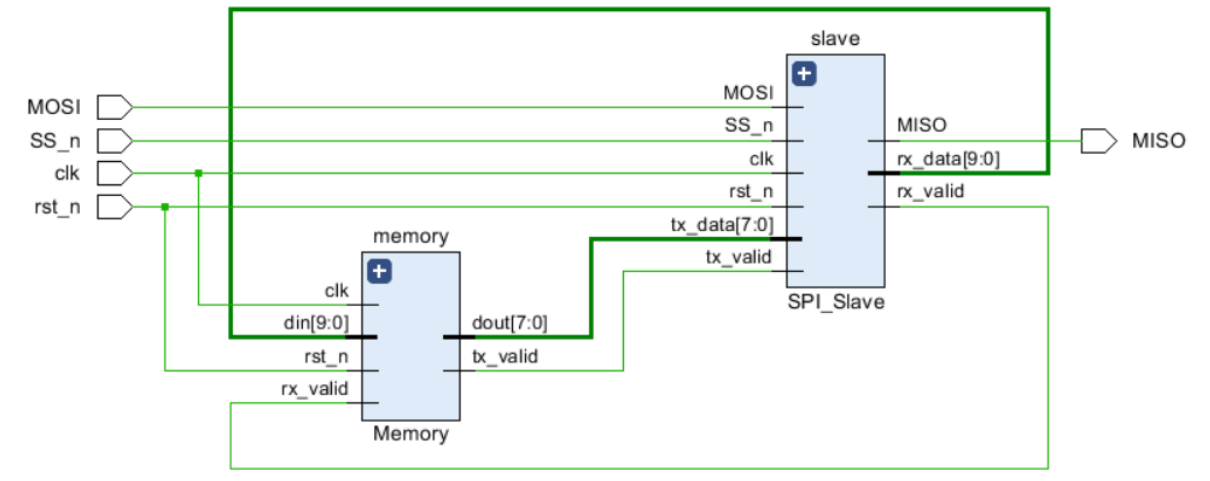
The above Snippet represent a full operation from IDLE→READ_DATA



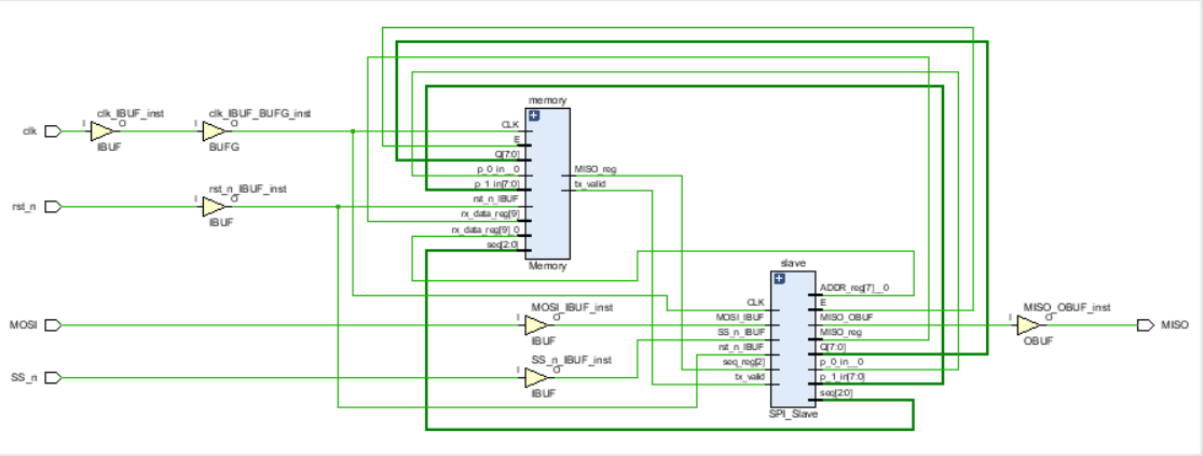
Synthesis and Implementation Results for Each Encoding:

Method_1:

```
reg [2:0] cs,ns;
localparam IDLE = 3'b000;
localparam CHK_CMD = 3'b111;
localparam WRITE = 3'b001;
localparam READ_ADD = 3'b010;
localparam READ_DATA = 3'b100;
```



above figure :Elaboration Result.



above figure: Synthesis shematic.

Summary

Resource	Utilization	Available	Utilization %
LUT	75	20800	0.36
LUTRAM	32	9600	0.33
FF	44	41600	0.11
IO	5	106	4.72

above figure: Utilization Report.

Setup

Worst Negative Slack (WNS):	7.358 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	360

Hold

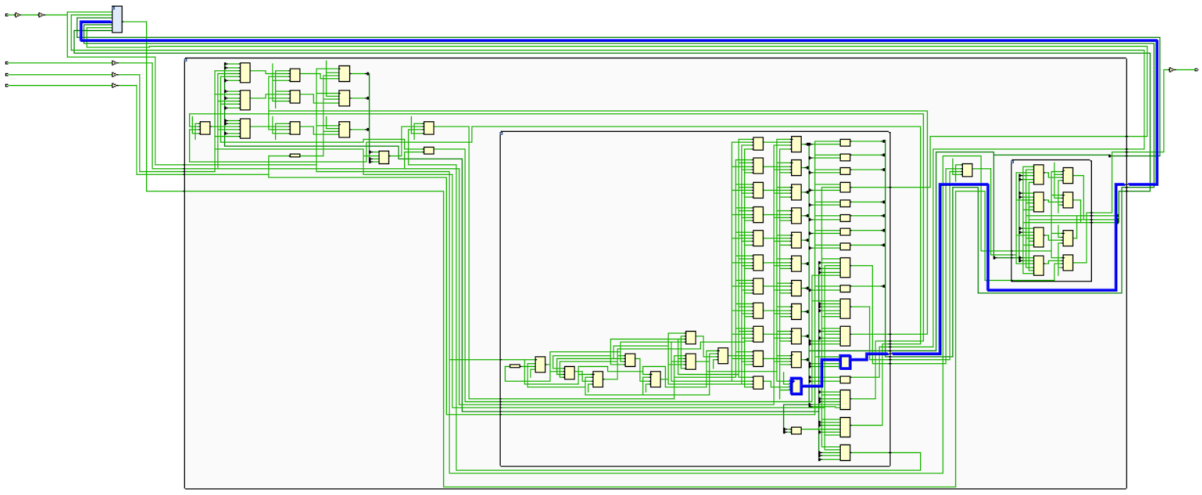
Worst Hold Slack (WHS):	0.097 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	360

Pulse Width

Worst Pulse Width Slack (WPWS):	3.750 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	63

All user specified timing constraints are met.

above figure: Timing Report.



Implementation Report:

utilization Report:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Top	73	44	17	8	32	41	32	12	5	1
memory (Memory)	34	16	17	8	14	2	32	0	0	0
slave (SPI_Slave)	39	28	0	0	22	39	0	11	0	0

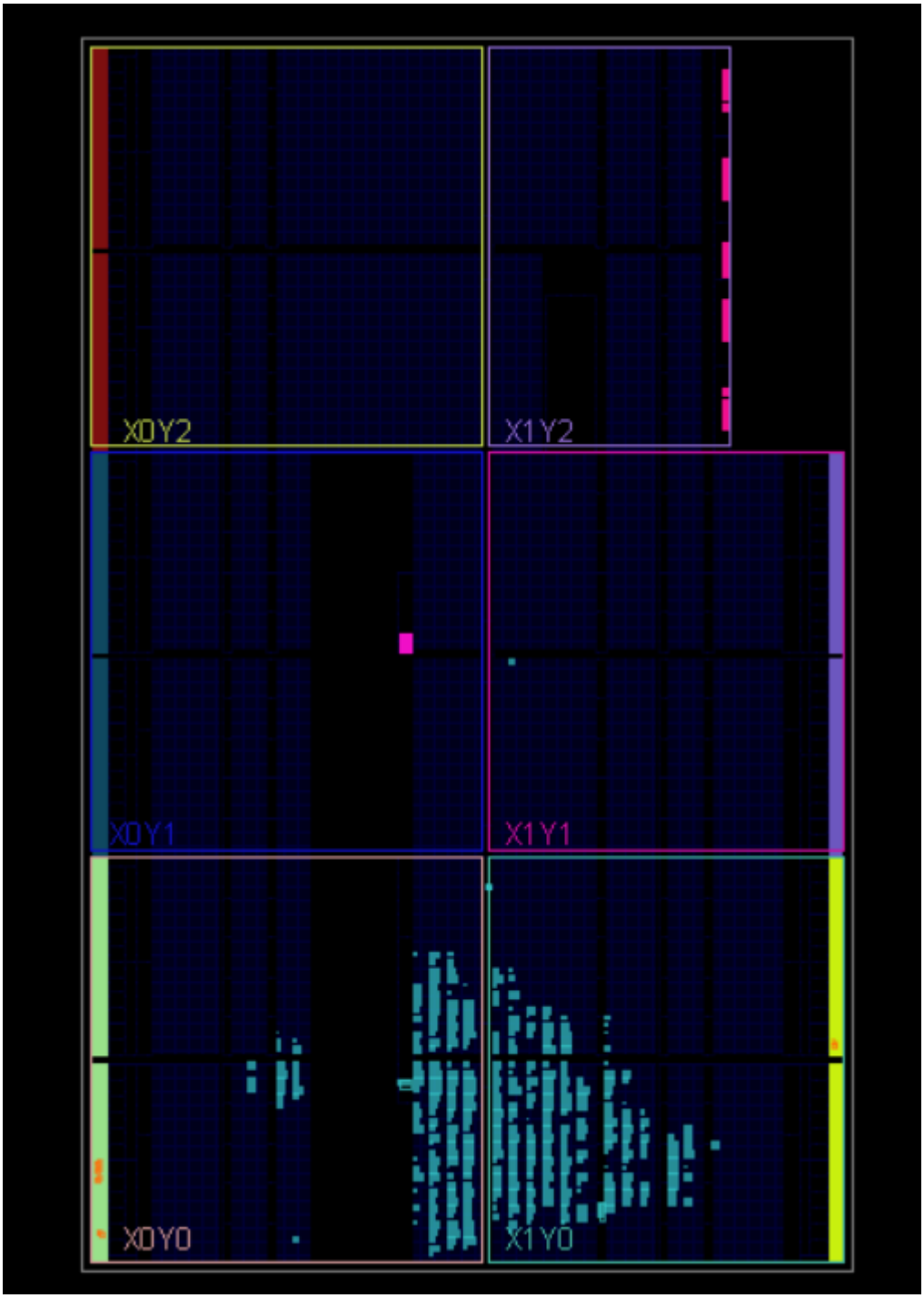
Timing Report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.450 ns	Worst Hold Slack (WHS):	-0.332 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	-0.332 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	1	Number of Failing Endpoints:	0
Total Number of Endpoints:	4145	Total Number of Endpoints:	4129	Total Number of Endpoints:	2163

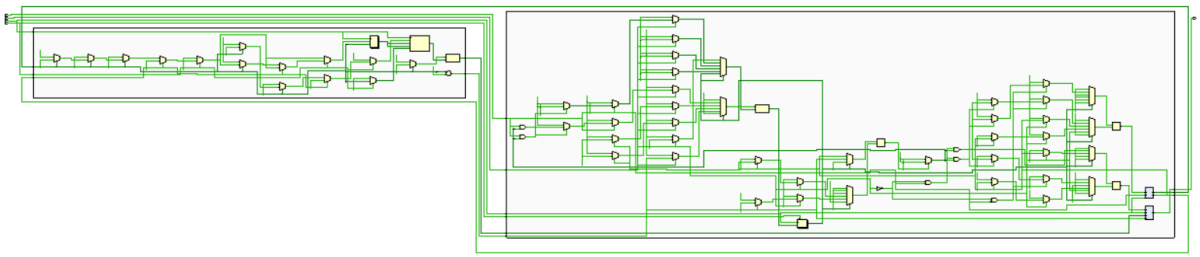
Timing constraints are not met.

FPGA Device:

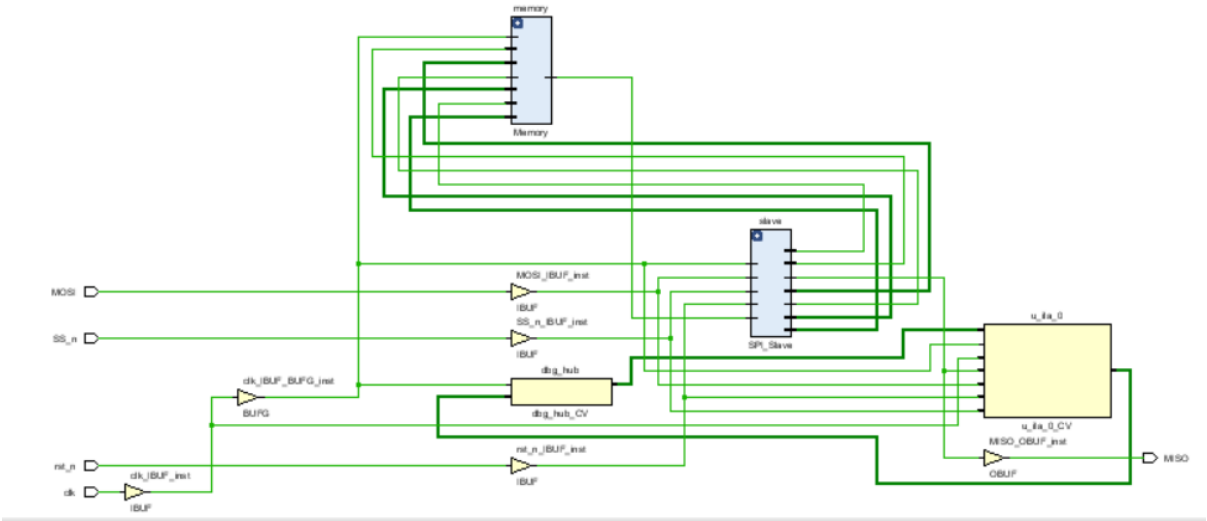


Method 2:

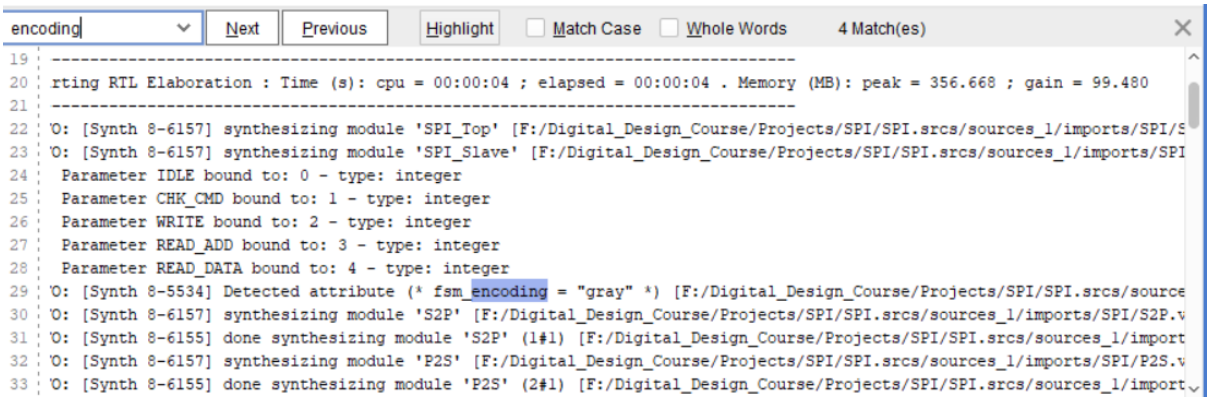
Elaboration Result:



Synthesis Result:



Encoding Used

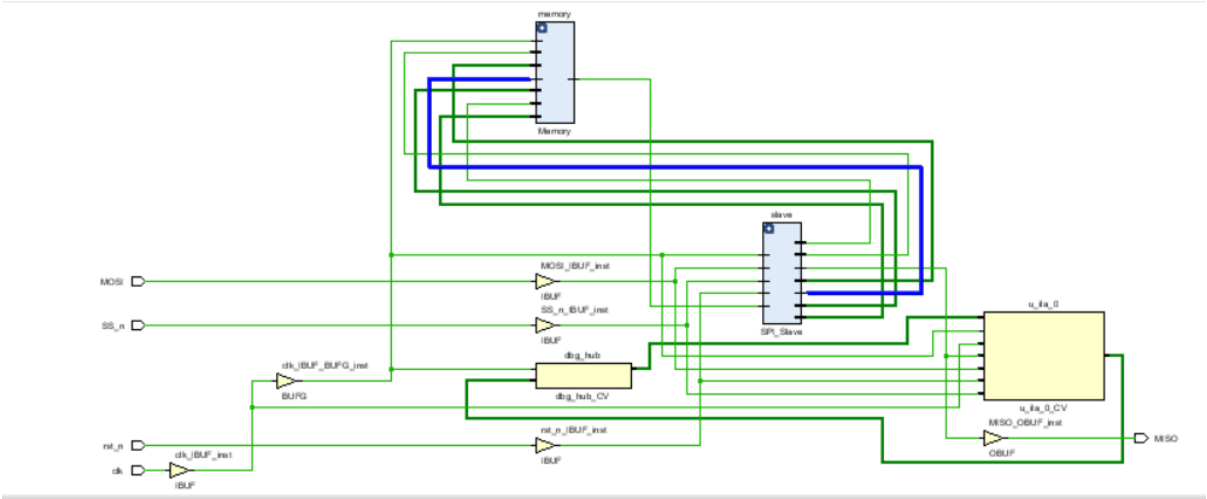


Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	12.358 ns	Worst Hold Slack (WHS):	0.097 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	360	Total Number of Endpoints:	360	Total Number of Endpoints:	63

All user specified timing constraints are met.



Utilization Report

Summary

Resource	Utilization	Available	Utilization %
LUT	1316	20800	6.33
LUTRAM	140	9600	1.46
FF	1960	41600	4.71
BRAM	0.50	50	1.00
IO	5	106	4.72

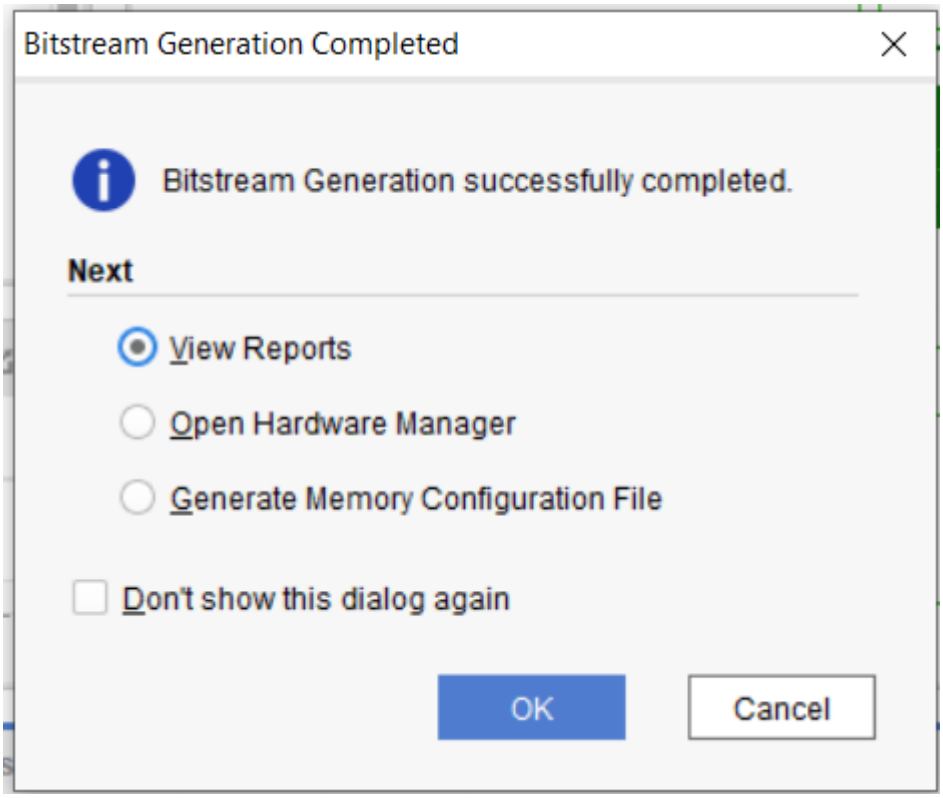
Timing Report

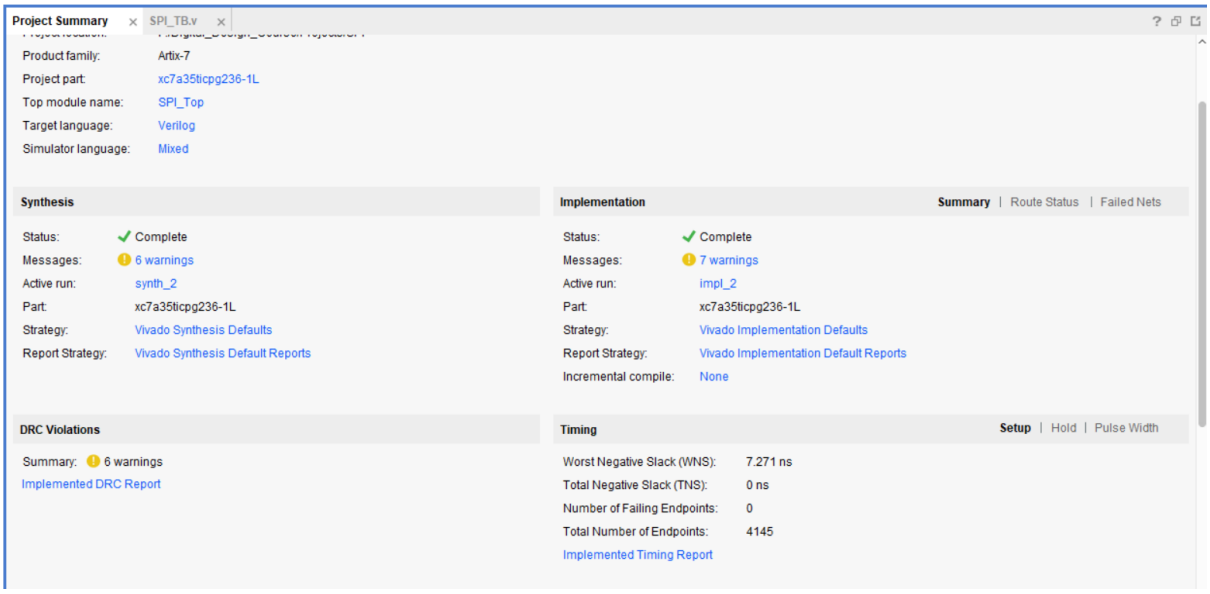
Design Timing Summary

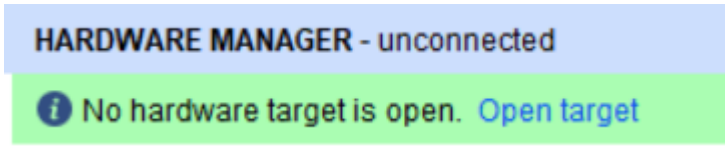
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	7.271 ns	Worst Hold Slack (WHS):	0.028 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4145	Total Number of Endpoints:	4129	Total Number of Endpoints:	2163

All user specified timing constraints are met.

Bitstream and messages

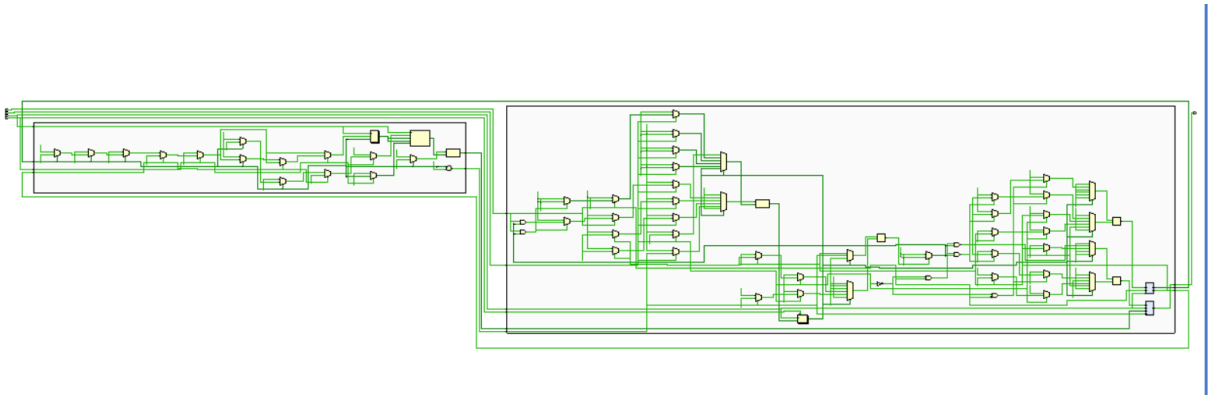




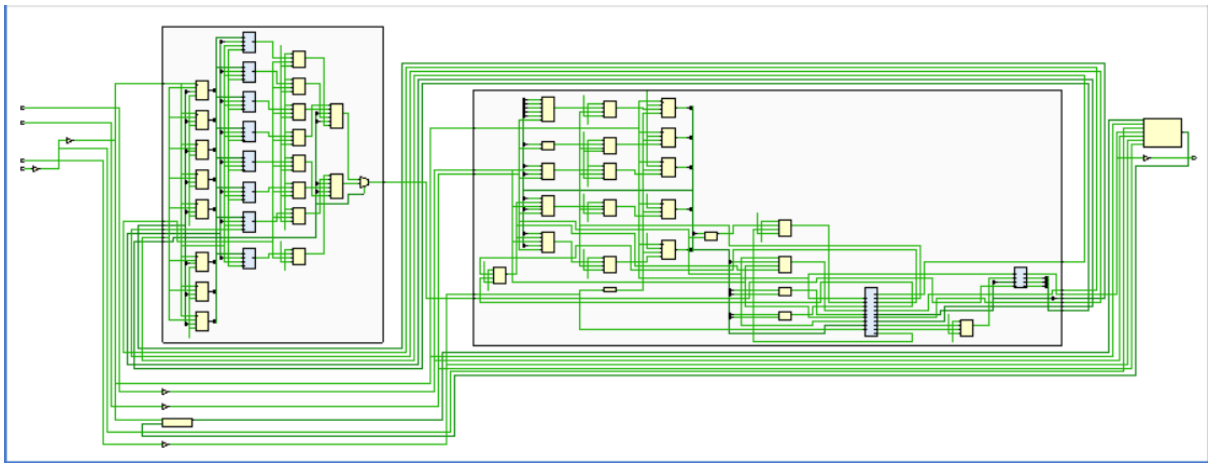


Method 3:

Elaboration Result



Synthesis Result



Encoding Used

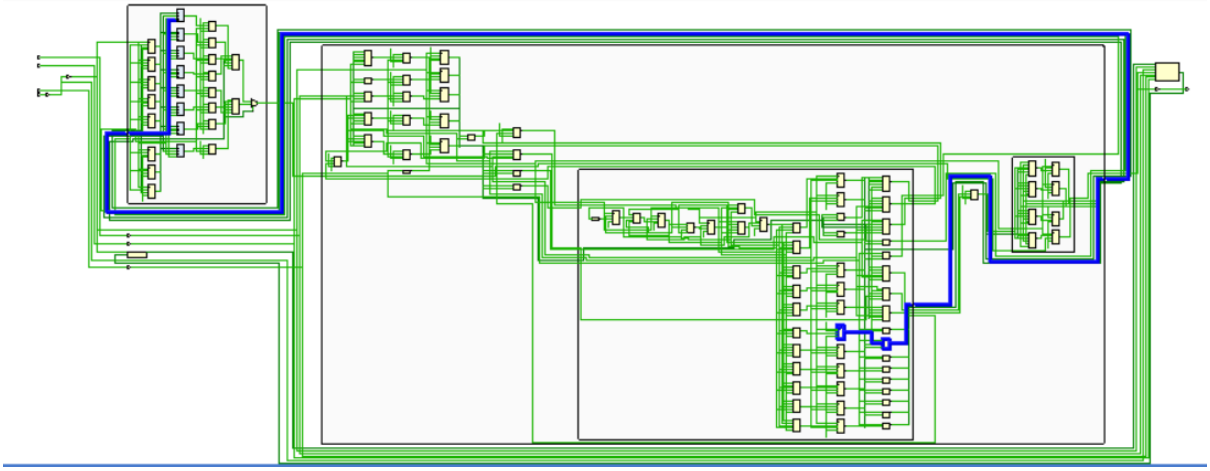
```
16 INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc'
17 INFO: Launching helper process for spawning children vivado processes
18 INFO: Helper process launched with PID 3344
19 ---------------------------------------------------------------------------
20 Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . M
21 ---------------------------------------------------------------------------
22 INFO: [Synth 8-6157] synthesizing module 'SPI_Top' [F:/Digital_Design_Course
23 INFO: [Synth 8-6157] synthesizing module 'SPI_Slave' [F:/Digital_Design_Cou
24     Parameter IDLE bound to: 0 - type: integer
25     Parameter CHK_CMD bound to: 1 - type: integer
26     Parameter WRITE bound to: 2 - type: integer
27     Parameter READ_ADD bound to: 3 - type: integer
28     Parameter READ_DATA bound to: 4 - type: integer
29 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [F:/D
30 INFO: [Synth 8-6157] synthesizing module 'S2P' [F:/Digital_Design_Course/Pro
31 INFO: [Synth 8-6155] done synthesizing module 'S2P' (1#1) [F:/Digital_Design
32 INFO: [Synth 8-6157] synthesizing module 'P2S' [F:/Digital_Design_Course/Pro
```

Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	12.358 ns	Worst Hold Slack (WHS):	0.097 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	360	Total Number of Endpoints:	360	Total Number of Endpoints:	65

All user specified timing constraints are met.



Utilization Report

Summary

Resource	Utilization	Available	Utilization %
LUT	79	20800	0.38
LUTRAM	32	9600	0.33
FF	48	41600	0.12
IO	5	106	4.72

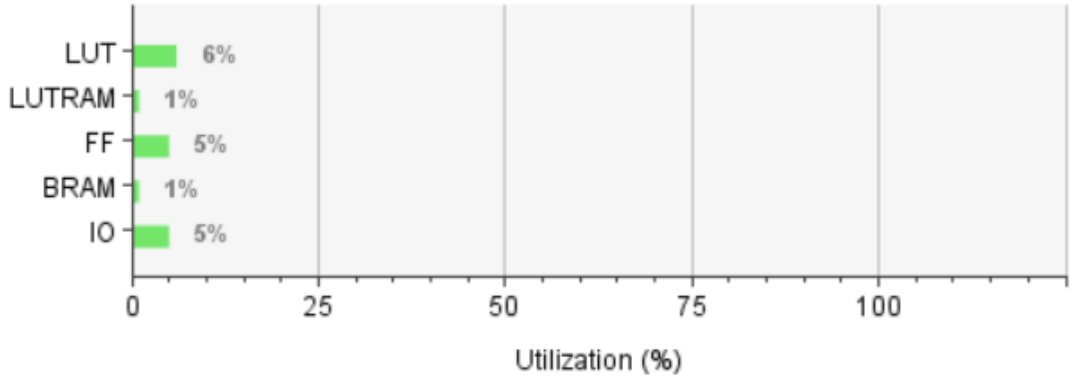
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Top	79	48	17	8	5	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0	0
memory (Memory)	34	16	17	8	0	0
slave (SPI_Slave)	45	32	0	0	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0	0

Implementation Report

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)
N SPI_Top	1315	1964	27	8	607	1175	140	737	0.5	5
dbg_hub (dbg_hub)	474	727	0	0	231	450	24	313	0	0
memory (Memory)	34	16	17	8	14	2	32	0	0	0
slave (SPI_Slave)	44	32	0	0	24	44	0	11	0	0
u_ila_0 (u_ila_0)	763	1189	10	0	349	679	84	411	0.5	0

Summary

Resource	Utilization	Available	Utilization %
LUT	1315	20800	6.32
LUTRAM	140	9600	1.46
FF	1964	41600	4.72
BRAM	0.50	50	1.00
IO	5	106	4.72



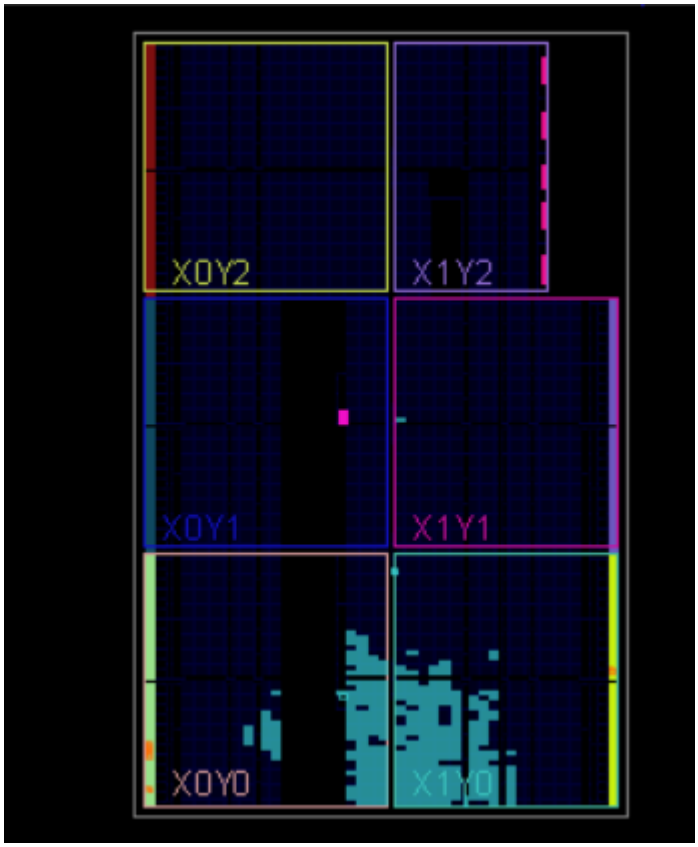
Timing Report

Design Timing Summary

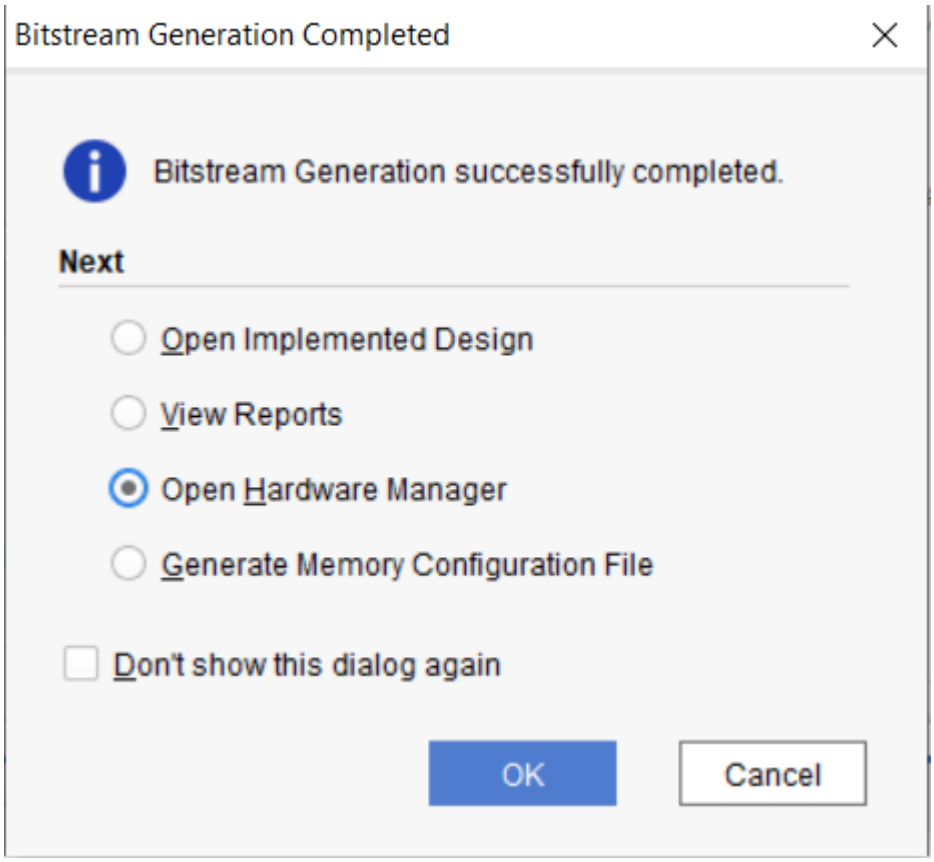
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.949 ns	Worst Hold Slack (WHS):	0.034 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4145	Total Number of Endpoints:	4129	Total Number of Endpoints:	2165

All user specified timing constraints are met.

FPGA Device



Messages and Bitstream




Synthesis
Status: Complete
Messages: 6 warnings
Active run: synth_2
Part: xc7a35ticpg236-1L
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Implementation
Summary | Route Status | Failed Nets
Status: Complete
Messages: 7 warnings
Active run: impl_2
Part: xc7a35ticpg236-1L
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental compile: None
DRC Violations
Summary: 6 warnings
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): 6.949 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 4145
Implemented Timing Report