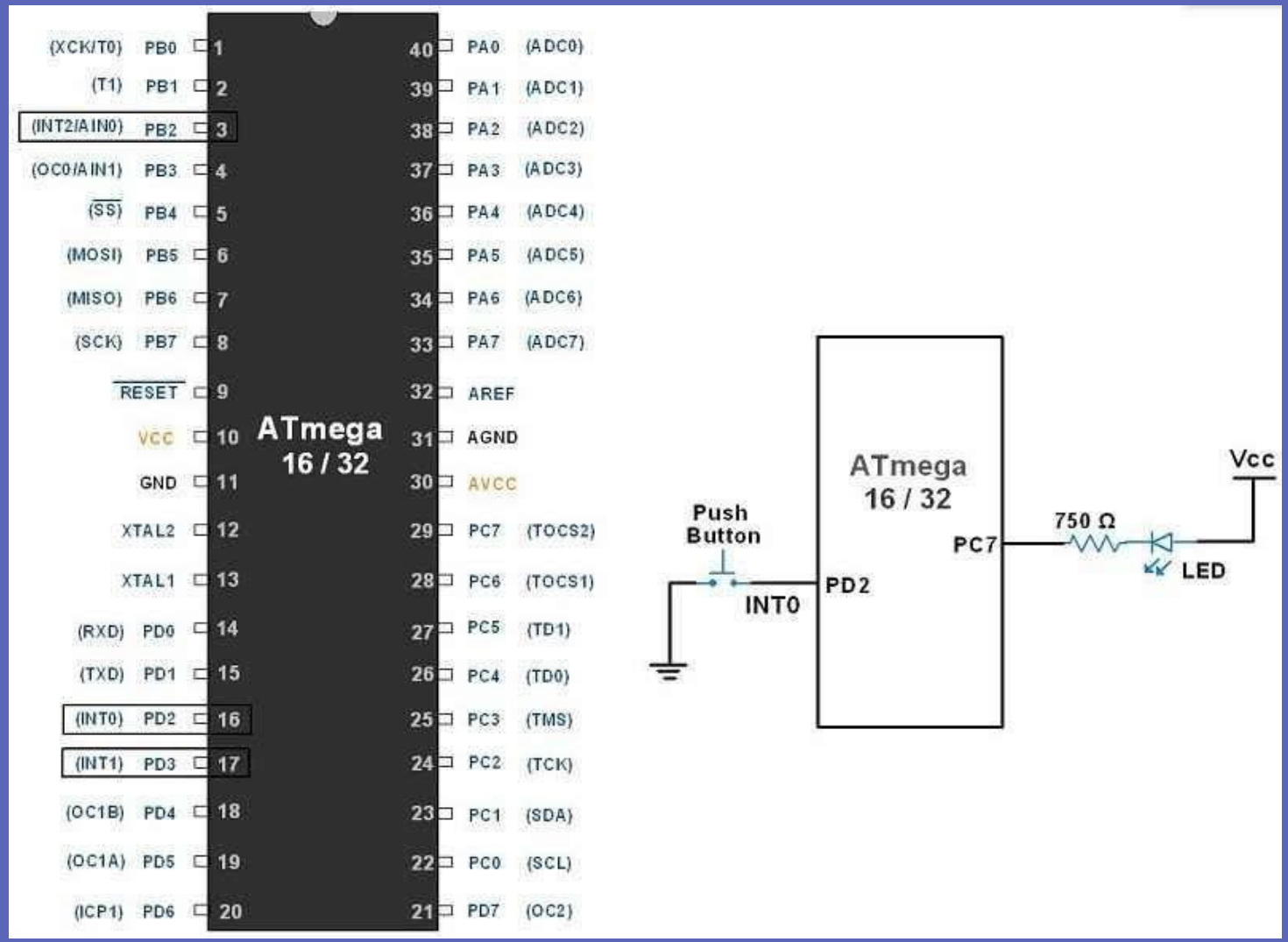
Recall Last session

Interfacing with 7-Segment

Introduction to Interrupt

Start Coding with External Interrupt

External Interrupt Pins in ATmega16/32



Registers of External Interrupt

D-BUGERZ

1.

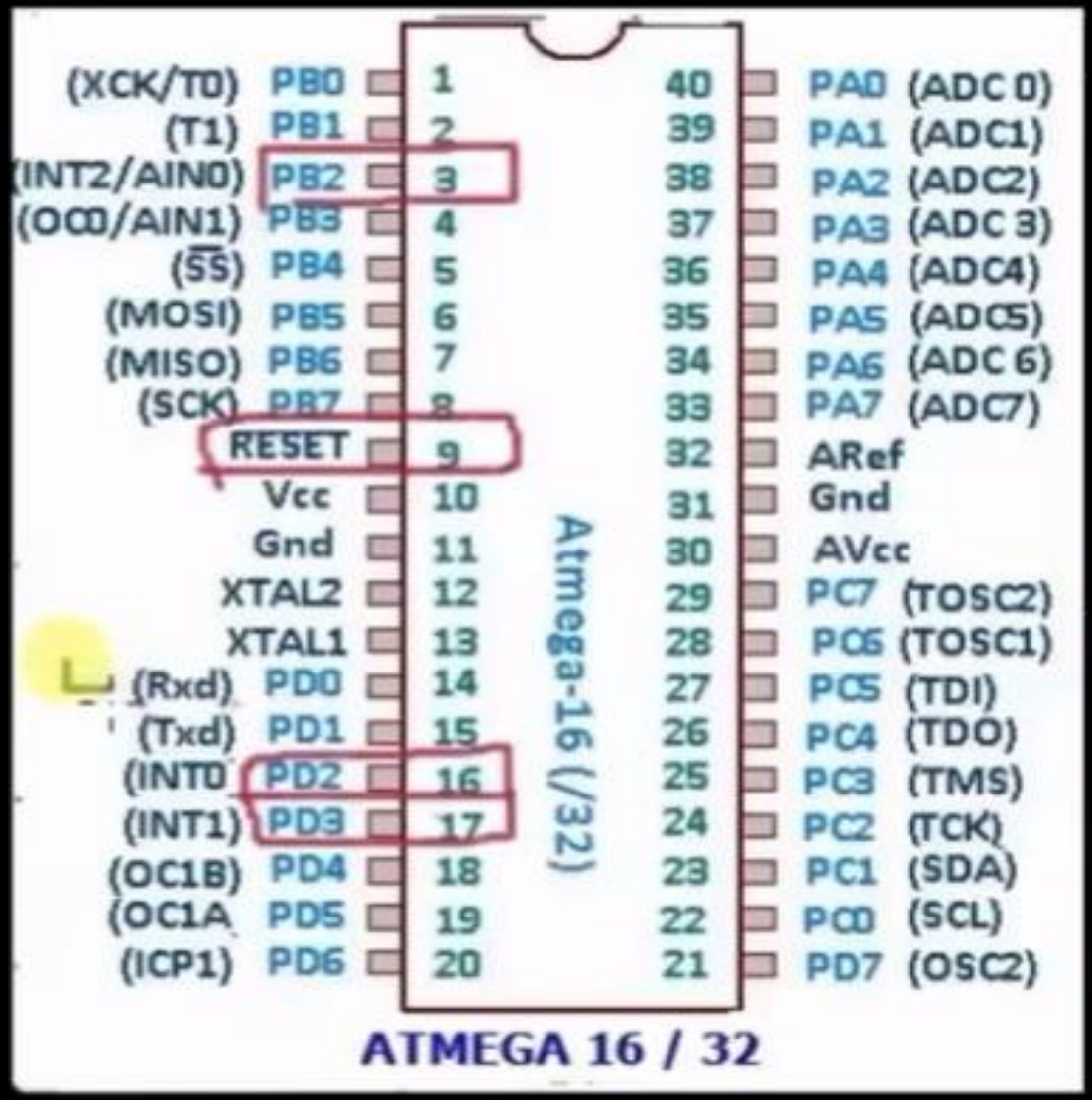
2.

3.

4.

External
INTERRUPTS

RESET
INT0 (PD2)
INT1 (PD3)
INT2 (PB2)



How To Trigger Interrupt Request

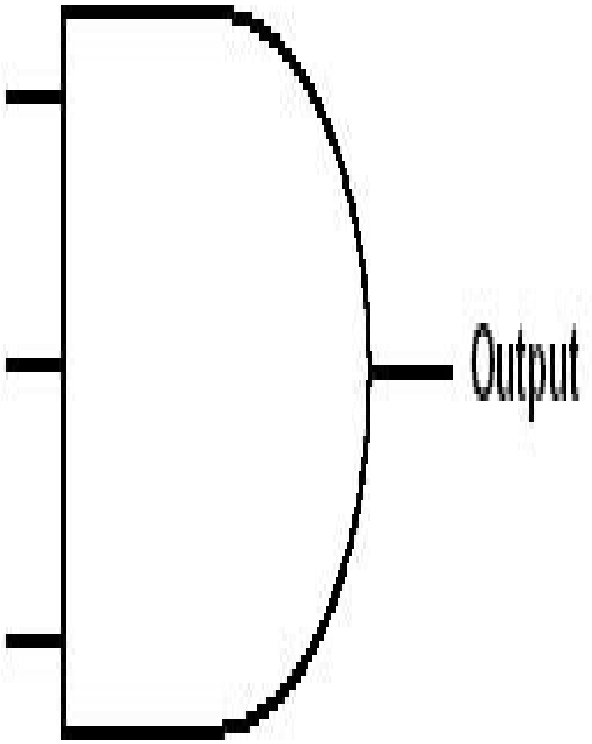
D-BUGERZ

- Each peripheral device has a group of special function registers that must be used to access the device for configuration. For a given peripheral interrupt to take effect, the interrupt for that peripheral must be enabled. The special function registers for that device provide the way to enable the interrupts.

1. In case disable all the interrupts is required just **clear** the **Global Interrupt Enable (GIE).** All Maskable interrupts are disabled whatever the MIE value was 1 or 0.

2. Each Maskable interrupt in the MC has a specific bit called **Module Interrupt Enable (MIE).** It is used to enable or disable the interrupt for this module or peripheral.

3. Also each Maskable interrupt in the microcontroller has a specific bit **called Module Interrupt flag (MIF).** This bit is set whenever the interrupt event occur. Whether or not the interrupt is enabled. This flag is also called Automatic flag as it is set automatically by hardware.



4.

Registers of External Interrupt

D-BUGERZ

- Page 10 in Datasheet

1.
2.
3.
4.

The AVR Status Register – SREG – is defined as:

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

Registers of External Interrupt

D-BUGERZ

- Page 67 in Datasheet

General Interrupt Control Register – GICR

Bit	7	6	5	4	3	2	1	0	
	INT1	INT0	INT2	–	–	–	IVSEL	IVCE	GICR
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

1. Bit 7 - INT1: External Interrupt Request 1 Enable
   - 0: Disable external interrupt 1
   - 1: Enable external interrupt 1
2. Bit 6 - INTO: External Interrupt Request 0 Enable
   - 0: Disable external interrupt 0
   - 1: Enable external interrupt 0
3. Bit 5 - INT2: External Interrupt Request 2 Enable
   - 0: Disable external interrupt 2
   - 1: Enable external interrupt 2
4.
   - **Apart from enabling a specific interrupt, Global Interrupts Enable bit (I-bit) MUST be enabled for the microcontroller to react to the interrupt event.**

Registers of External Interrupt

D-BUGERZ

1.
2.
3.
4.

- Page 67 in Datasheet

MCU Control Register – MCUCR

The MCU Control Register contains control bits for interrupt sense control and general MCU functions.

Bit	7	6	5	4	3	2	1	0	
	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

ISC01	ISC00		Description
0	0		The low level on INT0 pin generates an interrupt request.
0	1		Any logical change on INT0 pin generates an interrupt request.
1	0		The falling edge on INT0 pin generates an interrupt request.
1	1		The rising edge on INT0 pin generates an interrupt request.

Registers of External Interrupt

D-BUGERZ

1.
2.
3.
4.

- Page 67 in Datasheet

MCU Control and Status Register – MCUCSR

Bit	7	6	5	4	3	2	1	0	
	JTD	ISC2	–	JTRF	WDRF	BORF	EXTRF	PORF	MCUCSR
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	See Bit Description					

ISC2	Description
0	The falling edge of INT2 generate an interrupt request
1	The rising edge of INT2 generate an interrupt request

Registers of External Interrupt

D-BUGERZ

- Page 68 in Datasheet

General Interrupt Flag Register – GIFR

Bit	7	6	5	4	3	2	1	0	
	INTF1	INTF0	INTF2	–	–	–	–	–	GIFR
Read/Write	R/W	R/W	R/W	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

1.

2.

3.

4.

- The GIFR register contains the interrupt flags for all the ATmega16/32 external interrupts. Each of these bit are set individually to logic 1 when the interrupt event for the specified interrupt occurs.
- Note that the flag bit of an interrupt is set, whether or not the interrupt is enabled, once the interrupt event occurs.
- If the interrupt is enabled, it's corresponding interrupt flag bit will be cleared after executing it's ISR code. Alternatively, the flag can be cleared by writing a logical one to it

How To Trigger Interrupt Request

D-BUGERZ

1. ❑ **Global Interrupt Enable (GIE).**

The AVR Status Register – SREG – is defined as:

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

2. • **Bit 7 – I: Global Interrupt Enable**

3. ❑ **Module Interrupt Enable (MIE)**

General Interrupt Control Register – GICR

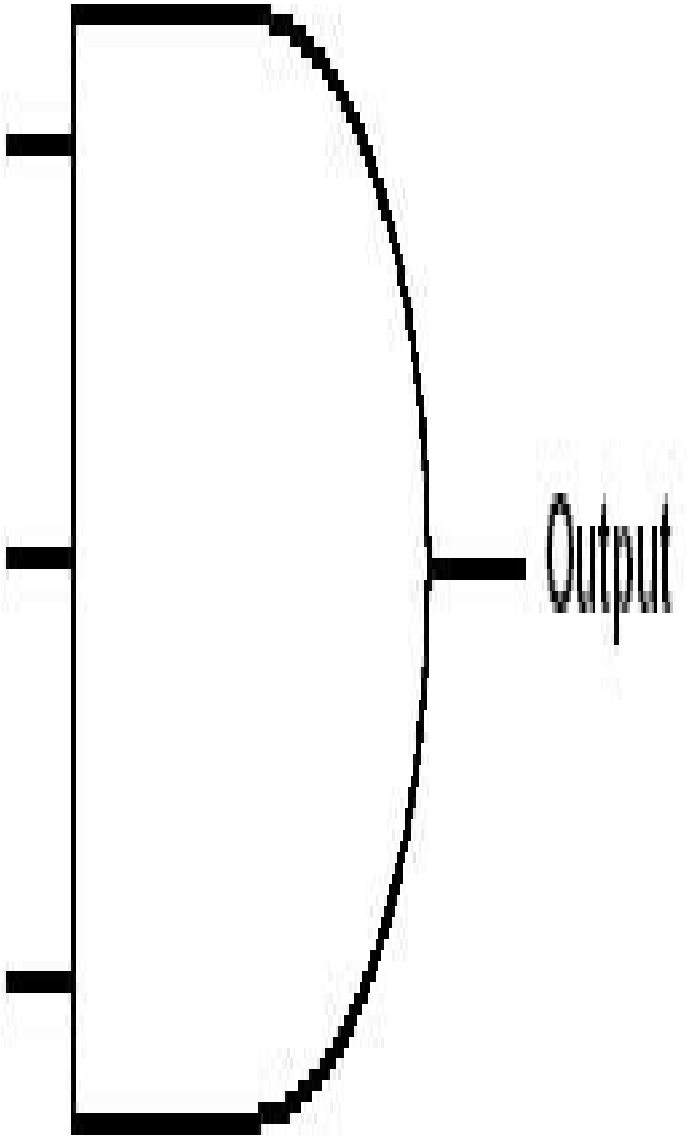
Bit	7	6	5	4	3	2	1	0	
	INT1	INT0	INT2	–	–	–	IVSEL	IVCE	GICR
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

4. → **There are 2nd step here to configure when you want to receive interrupt**

❑ **Module Interrupt flag (MIF).**

General Interrupt Flag Register – GIFR

Bit	7	6	5	4	3	2	1	0	
	INTF1	INTF0	INTF2	–	–	–	–	–	GIFR
Read/Write	R/W	R/W	R/W	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

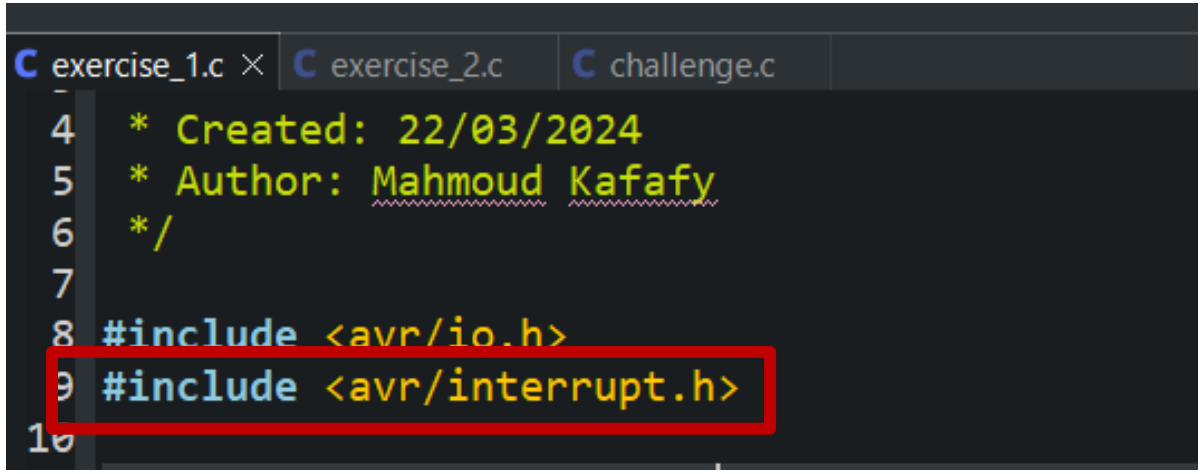


Interrupt Coding Notes

D-BUGERZ

1.
2.
3.
4.

- AVR-GCC compiler needs a library to understand ISR definition



- Write ISR for a specific interrupt using AVR library: