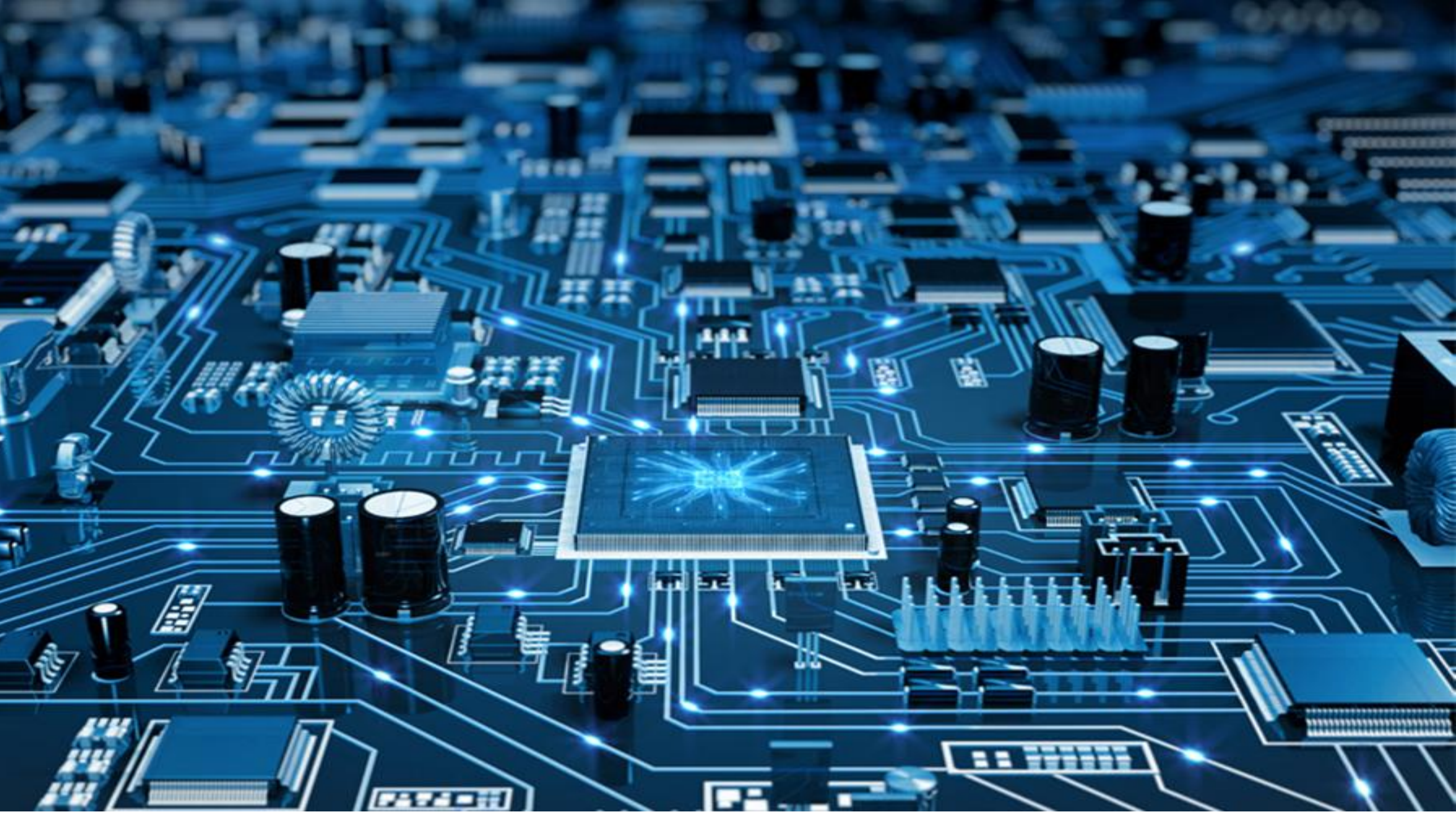
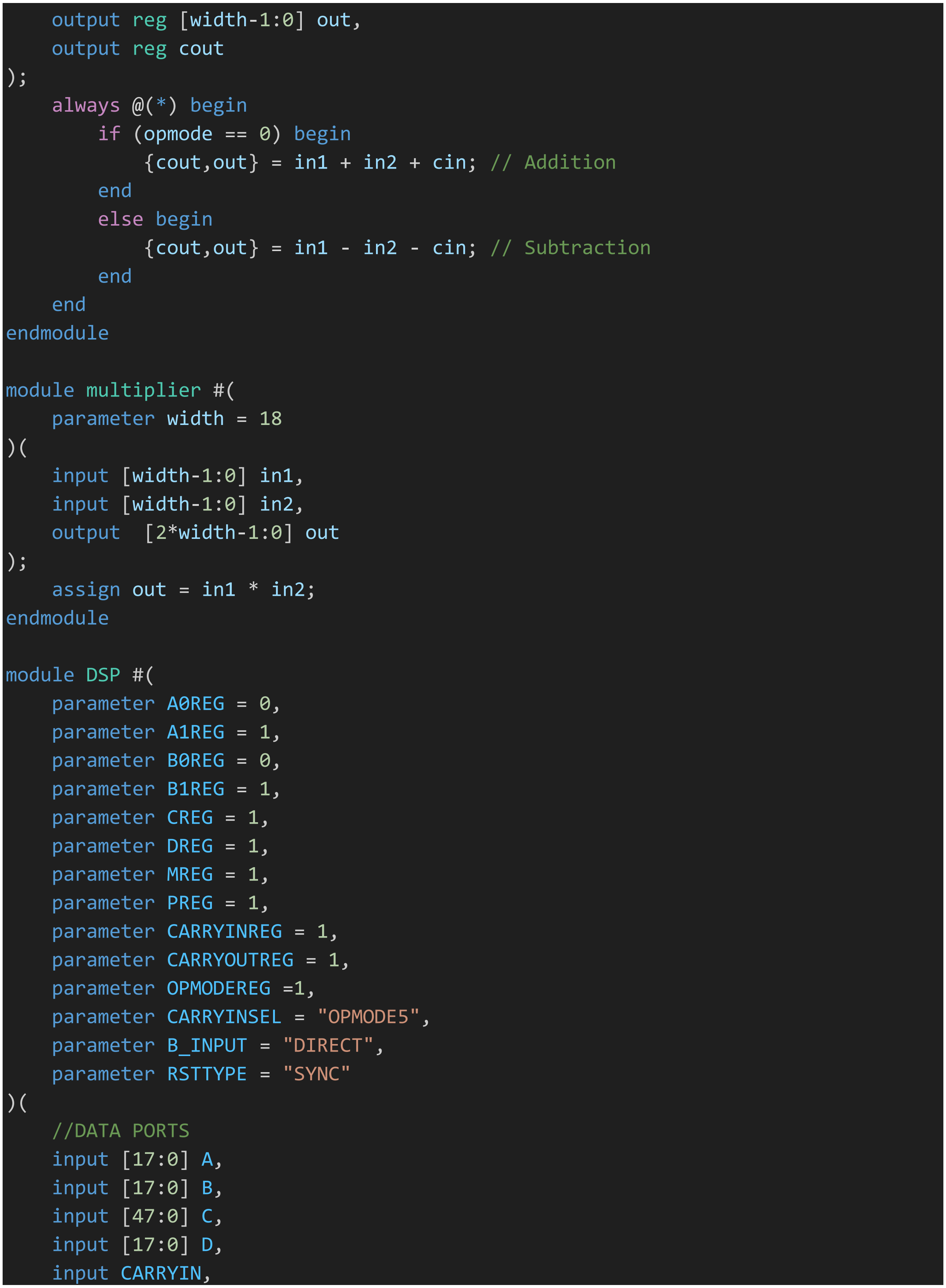


PROJECT 1
Spartan6 - DSP48A1

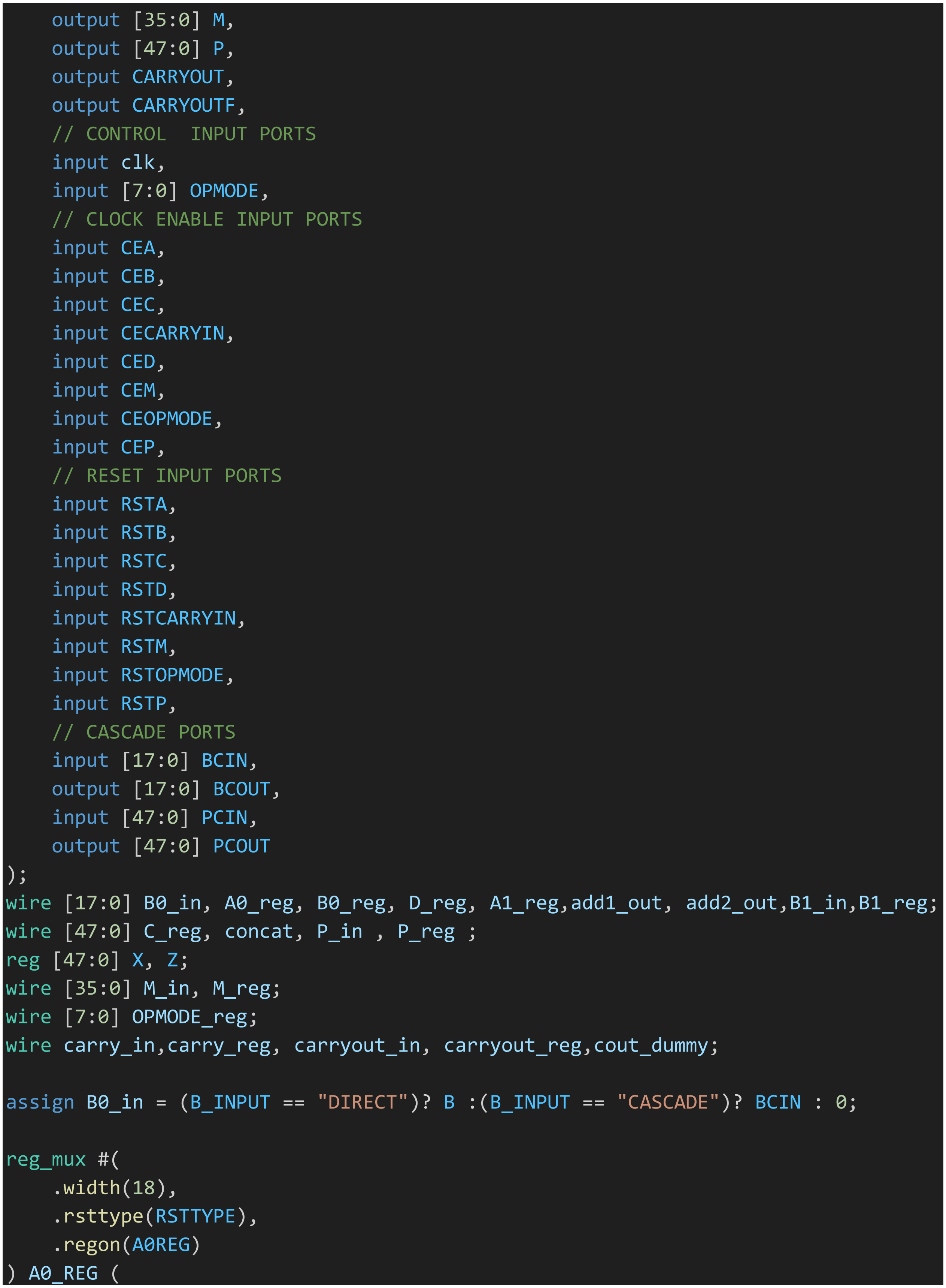
By: Ziad Tamer Ibrahim

Rtl code

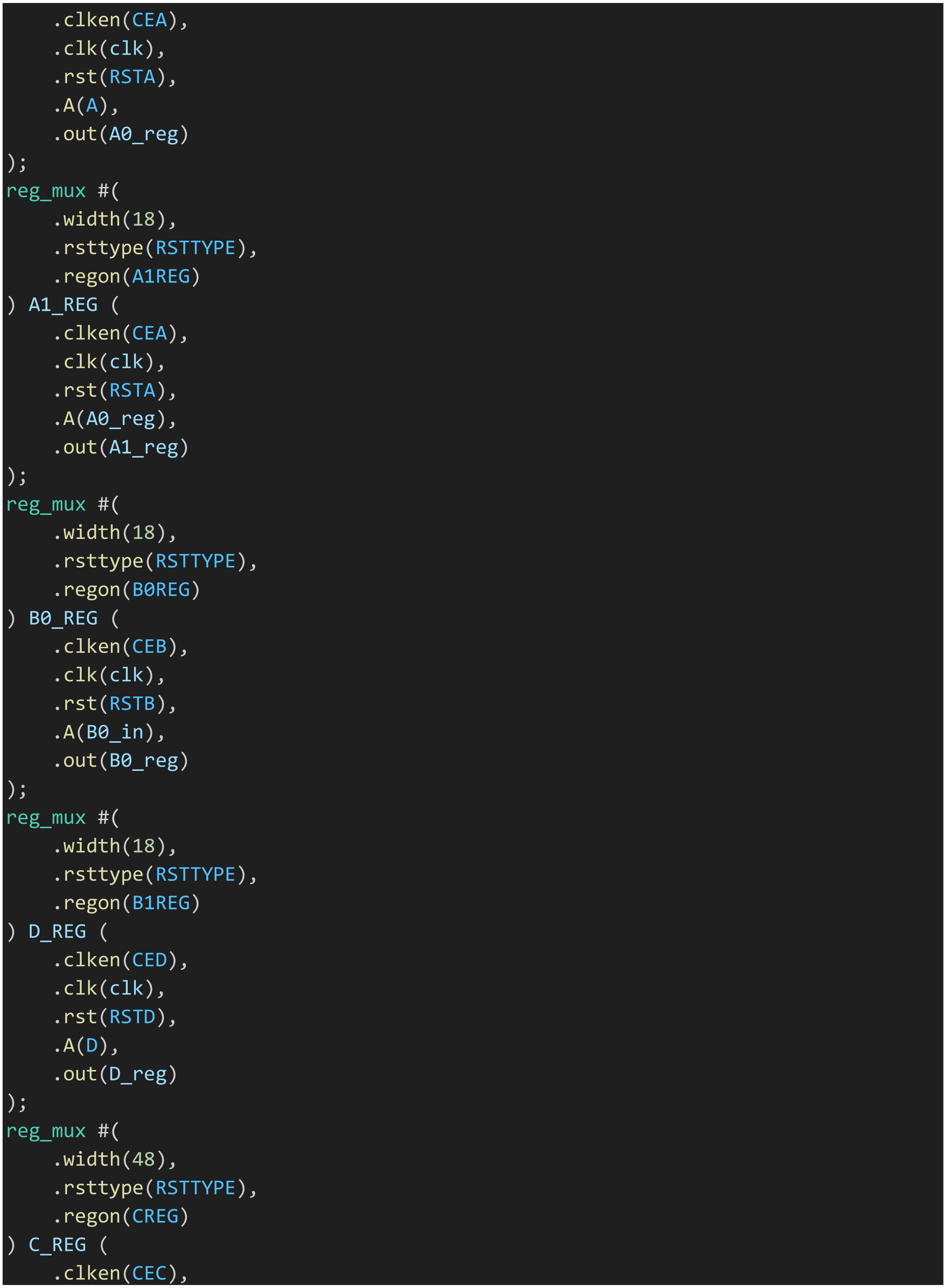
```
module reg_mux #(
    parameter width = 18,
    parameter rsttype = "SYNC",
    parameter regon =1
)(
    input clken,
    input clk,
    input rst,
    input [width-1:0] A,
    output reg [width-1:0] out
);
    generate
        if (regon) begin
            if (rsttype == "SYNC") begin
                always @(posedge clk) begin
                        if (rst) out <= 0;
                        else if (clken)  out <= A;
                end
            end
            else if (rsttype == "ASYNC") begin
                always @(posedge clk or posedge rst) begin
                    if (rst) out <= 0;
                    else if (clken)  out <= A;
                end
            end
        end
        else begin
            always @(*) begin
                out = A;
            end
        end
    endgenerate
endmodule

module add_sub #(
    parameter width = 18
)(
    input [width-1:0] in1,
    input [width-1:0] in2,
    input cin,
    input opmode, // 0 for addition, 1 for subtraction
```



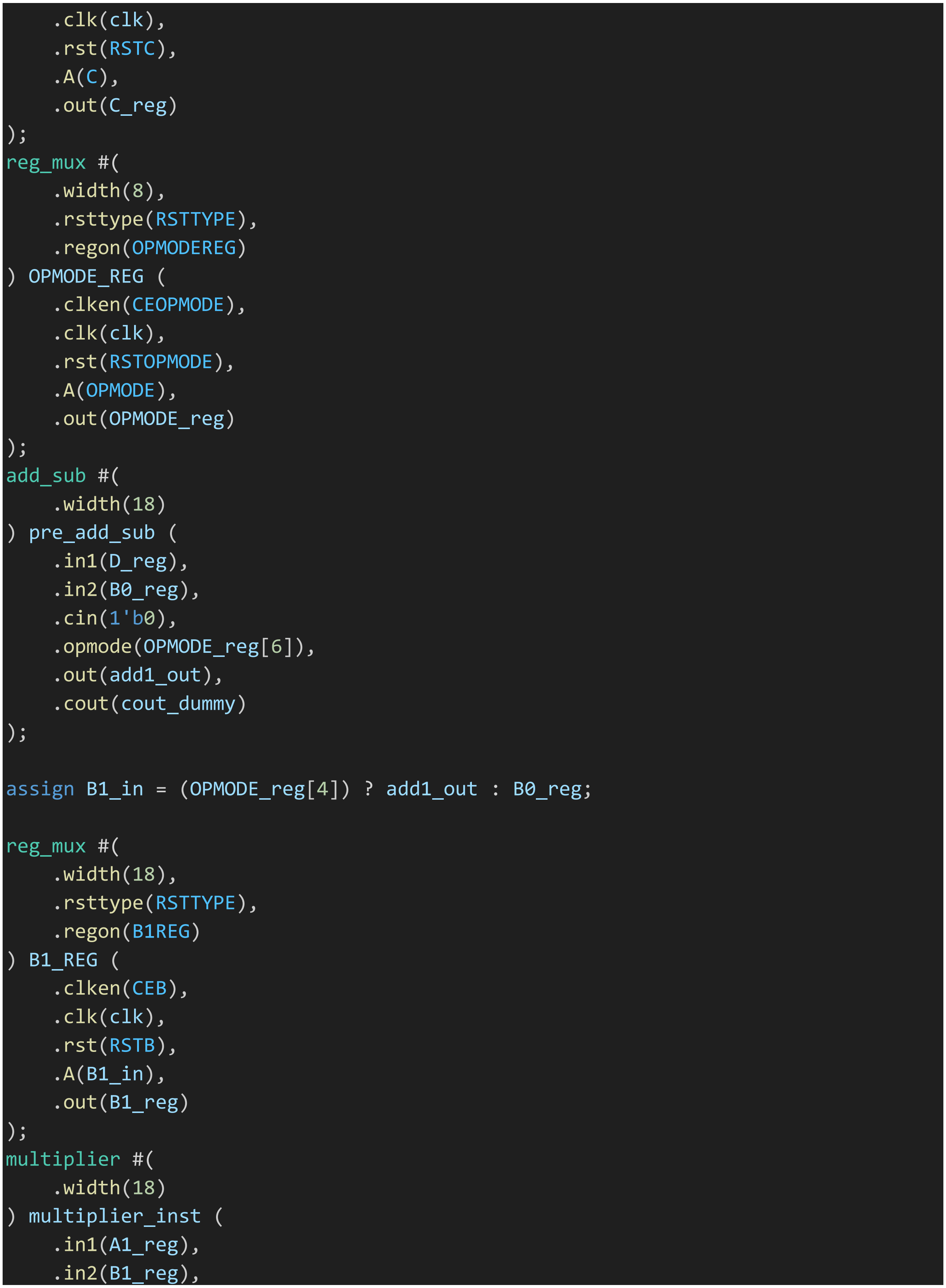
```
    output reg [width-1:0] out,
    output reg cout
);
    always @(*) begin
        if (opmode == 0) begin
            {cout,out} = in1 + in2 + cin; // Addition
        end
        else begin
            {cout,out} = in1 - in2 - cin; // Subtraction
        end
    end
endmodule

module multiplier #(
    parameter width = 18
)(
    input [width-1:0] in1,
    input [width-1:0] in2,
    output  [2*width-1:0] out
);
    assign out = in1 * in2;
endmodule

module DSP #(
    parameter A0REG = 0,
    parameter A1REG = 1,
    parameter B0REG = 0,
    parameter B1REG = 1,
    parameter CREG = 1,
    parameter DREG = 1,
    parameter MREG = 1,
    parameter PREG = 1,
    parameter CARRYINREG = 1,
    parameter CARRYOUTREG = 1,
    parameter OPMODEREG =1,
    parameter CARRYINSEL = "OPMODE5",
    parameter B_INPUT = "DIRECT",
    parameter RSTTYPE = "SYNC"
)(
    //DATA PORTS
    input [17:0] A,
    input [17:0] B,
    input [47:0] C,
    input [17:0] D,
    input CARRYIN,
```



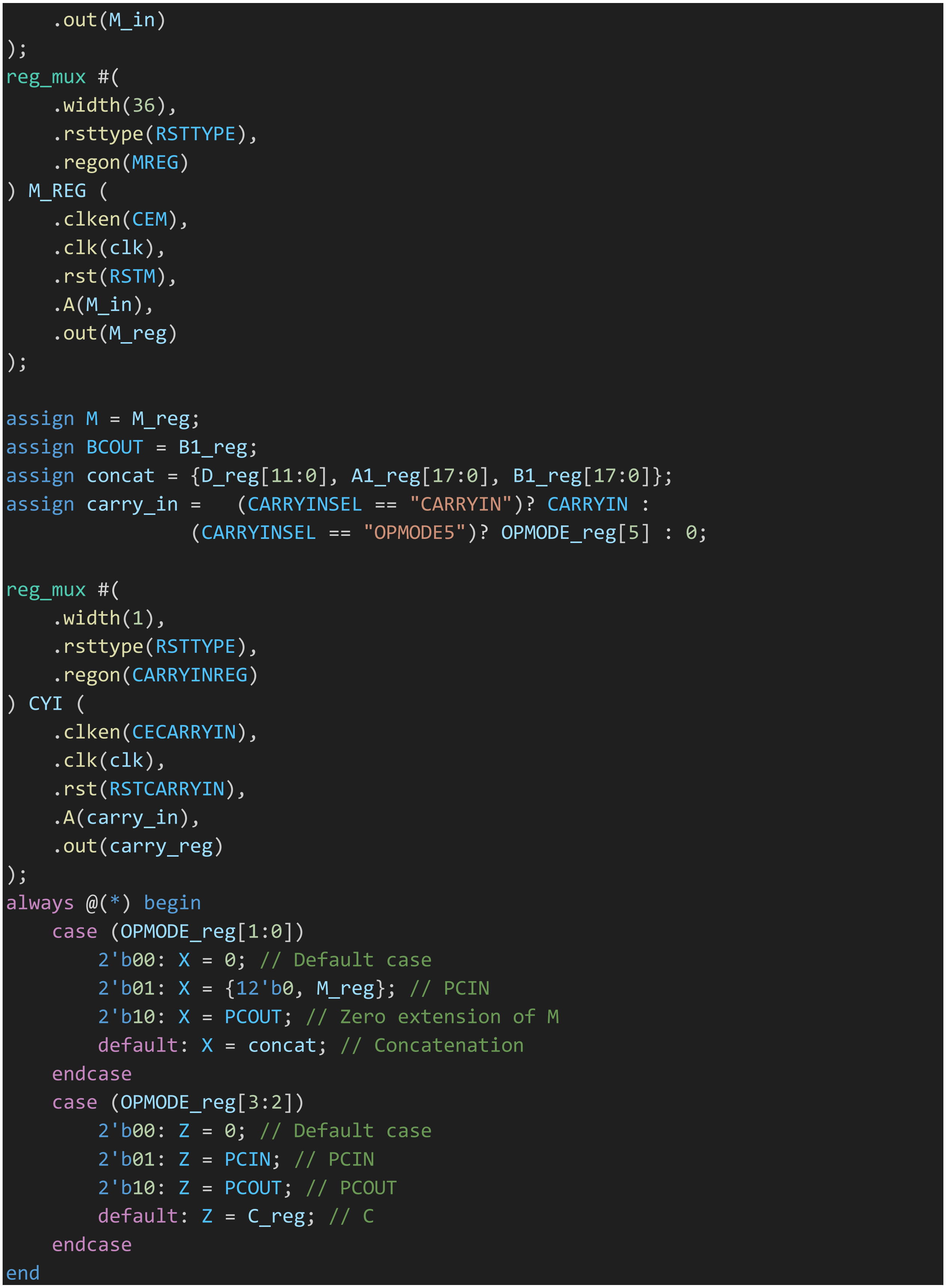
```verilog
    output [35:0] M,
    output [47:0] P,
    output CARRYOUT,
    output CARRYOUTF,
    // CONTROL  INPUT PORTS
    input clk,
    input [7:0] OPMODE,
    // CLOCK ENABLE INPUT PORTS
    input CEA,
    input CEB,
    input CEC,
    input CECARRYIN,
    input CED,
    input CEM,
    input CEOPMODE,
    input CEP,
    // RESET INPUT PORTS
    input RSTA,
    input RSTB,
    input RSTC,
    input RSTD,
    input RSTCARRYIN,
    input RSTM,
    input RSTOPMODE,
    input RSTP,
    // CASCADE PORTS
    input [17:0] BCIN,
    output [17:0] BCOUT,
    input [47:0] PCIN,
    output [47:0] PCOUT
);
wire [17:0] B0_in, A0_reg, B0_reg, D_reg, A1_reg,add1_out, add2_out,B1_in,B1_reg;
wire [47:0] C_reg, concat, P_in , P_reg ;
reg [47:0] X, Z;
wire [35:0] M_in, M_reg;
wire [7:0] OPMODE_reg;
wire carry_in,carry_reg, carryout_in, carryout_reg,cout_dummy;

assign B0_in = (B_INPUT == "DIRECT")? B :(B_INPUT == "CASCADE")? BCIN : 0;

reg_mux #(
    .width(18),
    .rsttype(RSTTYPE),
    .regon(A0REG)
) A0_REG (
```



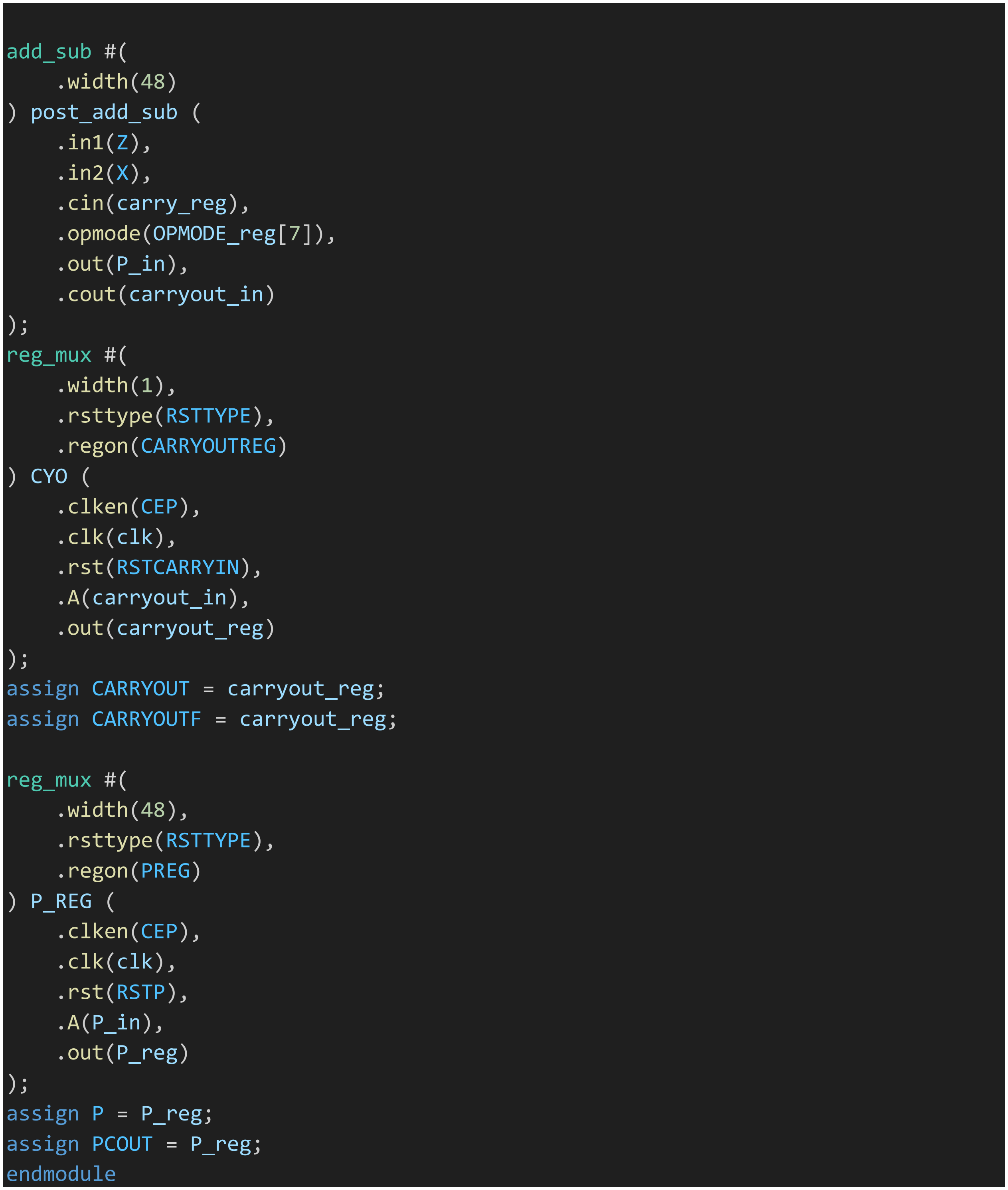
```
    .clken(CEA),
    .clk(clk),
    .rst(RSTA),
    .A(A),
    .out(A0_reg)
);
reg_mux #(
    .width(18),
    .rsttype(RSTTYPE),
    .regon(A1REG)
) A1_REG (
    .clken(CEA),
    .clk(clk),
    .rst(RSTA),
    .A(A0_reg),
    .out(A1_reg)
);
reg_mux #(
    .width(18),
    .rsttype(RSTTYPE),
    .regon(B0REG)
) B0_REG (
    .clken(CEB),
    .clk(clk),
    .rst(RSTB),
    .A(B0_in),
    .out(B0_reg)
);
reg_mux #(
    .width(18),
    .rsttype(RSTTYPE),
    .regon(B1REG)
) D_REG (
    .clken(CED),
    .clk(clk),
    .rst(RSTD),
    .A(D),
    .out(D_reg)
);
reg_mux #(
    .width(48),
    .rsttype(RSTTYPE),
    .regon(CREG)
) C_REG (
    .clken(CEC),
```



```
    .clk(clk),
    .rst(RSTC),
    .A(C),
    .out(C_reg)
);
reg_mux #(
    .width(8),
    .rsttype(RSTTYPE),
    .regon(OPMODEREG)
) OPMODE_REG (
    .clken(CEOPMODE),
    .clk(clk),
    .rst(RSTOPMODE),
    .A(OPMODE),
    .out(OPMODE_reg)
);
add_sub #(
    .width(18)
) pre_add_sub (
    .in1(D_reg),
    .in2(B0_reg),
    .cin(1'b0),
    .opmode(OPMODE_reg[6]),
    .out(add1_out),
    .cout(cout_dummy)
);

assign B1_in = (OPMODE_reg[4]) ? add1_out : B0_reg;

reg_mux #(
    .width(18),
    .rsttype(RSTTYPE),
    .regon(B1REG)
) B1_REG (
    .clken(CEB),
    .clk(clk),
    .rst(RSTB),
    .A(B1_in),
    .out(B1_reg)
);
multiplier #(
    .width(18)
) multiplier_inst (
    .in1(A1_reg),
    .in2(B1_reg),
```



```
    .out(M_in)
);
reg_mux #(
    .width(36),
    .rsttype(RSTTYPE),
    .regon(MREG)
) M_REG (
    .clken(CEM),
    .clk(clk),
    .rst(RSTM),
    .A(M_in),
    .out(M_reg)
);

assign M = M_reg;
assign BCOUT = B1_reg;
assign concat = {D_reg[11:0], A1_reg[17:0], B1_reg[17:0]};
assign carry_in =   (CARRYINSEL == "CARRYIN")? CARRYIN :
                (CARRYINSEL == "OPMODE5")? OPMODE_reg[5] : 0;

reg_mux #(
    .width(1),
    .rsttype(RSTTYPE),
    .regon(CARRYINREG)
) CYI (
    .clken(CECARRYIN),
    .clk(clk),
    .rst(RSTCARRYIN),
    .A(carry_in),
    .out(carry_reg)
);
always @(*) begin
    case (OPMODE_reg[1:0])
        2'b00: X = 0; // Default case
        2'b01: X = {12'b0, M_reg}; // PCIN
        2'b10: X = PCOUT; // Zero extension of M
        default: X = concat; // Concatenation
    endcase
    case (OPMODE_reg[3:2])
        2'b00: Z = 0; // Default case
        2'b01: Z = PCIN; // PCIN
        2'b10: Z = PCOUT; // PCOUT
        default: Z = C_reg; // C
    endcase
end
```

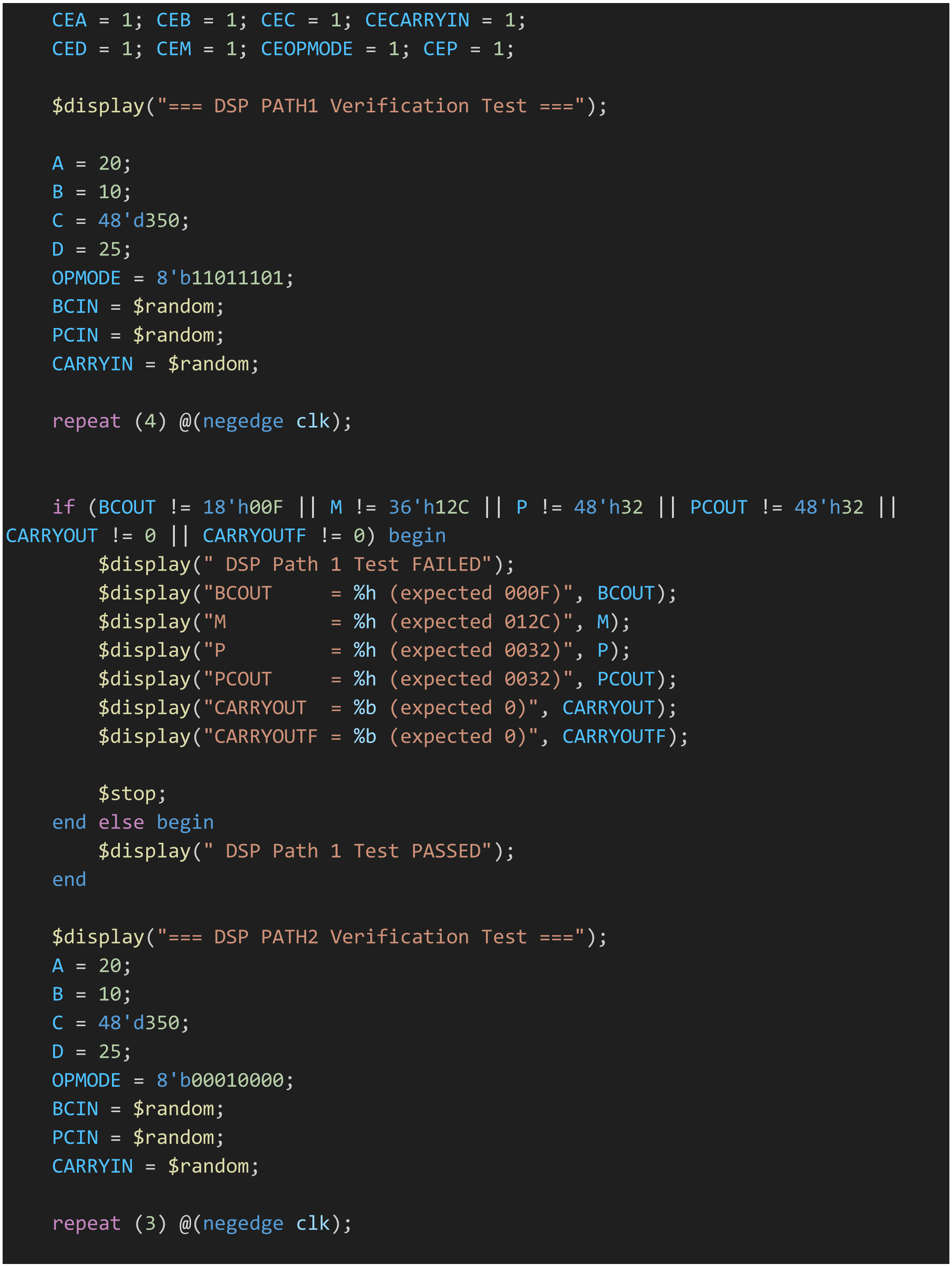


```
add_sub #(
    .width(48)
) post_add_sub (
    .in1(Z),
    .in2(X),
    .cin(carry_reg),
    .opmode(OPMODE_reg[7]),
    .out(P_in),
    .cout(carryout_in)
);
reg_mux #(
    .width(1),
    .rsttype(RSTTYPE),
    .regon(CARRYOUTREG)
) CYO (
    .clken(CEP),
    .clk(clk),
    .rst(RSTCARRYIN),
    .A(carryout_in),
    .out(carryout_reg)
);
assign CARRYOUT = carryout_reg;
assign CARRYOUTF = carryout_reg;

reg_mux #(
    .width(48),
    .rsttype(RSTTYPE),
    .regon(PREG)
) P_REG (
    .clken(CEP),
    .clk(clk),
    .rst(RSTP),
    .A(P_in),
    .out(P_reg)
);
assign P = P_reg;
assign PCOUT = P_reg;
endmodule
```

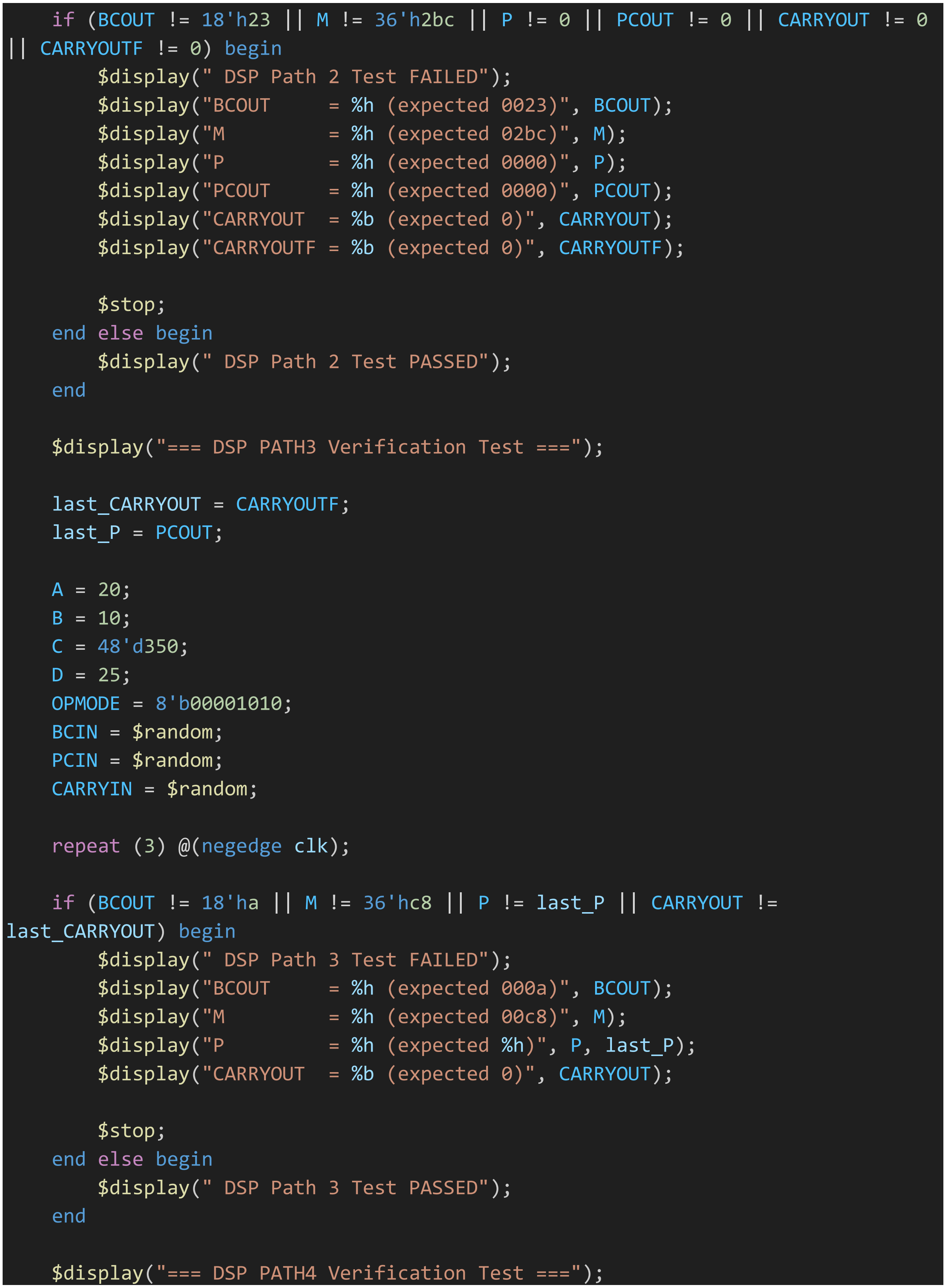
Testbench code

```
`timescale 1ns/1ps

module DSP_tb();

  reg clk;
  reg [17:0] A, B, D;
  reg [47:0] C;
  reg CARRYIN;
  reg [7:0] OPMODE;

  reg CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
  reg RSTA, RSTB, RSTC, RSTD, RSTCARRYIN, RSTM, RSTOPMODE, RSTP;
  reg [17:0] BCIN;
  reg [47:0] PCIN;

  reg [47:0] last_P;
  reg last_CARRYOUT;

  wire [35:0] M;
  wire [47:0] P;
  wire CARRYOUT, CARRYOUTF;
  wire [17:0] BCOUT;
  wire [47:0] PCOUT;

  DSP DUT (
    .A(A), .B(B), .C(C), .D(D), .CARRYIN(CARRYIN),
    .M(M), .P(P), .CARRYOUT(CARRYOUT), .CARRYOUTF(CARRYOUTF),
    .clk(clk), .OPMODE(OPMODE),
    .CEA(CEA), .CEB(CEB), .CEC(CEC), .CECARRYIN(CECARRYIN),
    .CED(CED), .CEM(CEM), .CEOPMODE(CEOPMODE), .CEP(CEP),
    .RSTA(RSTA), .RSTB(RSTB), .RSTC(RSTC), .RSTD(RSTD),
    .RSTCARRYIN(RSTCARRYIN), .RSTM(RSTM), .RSTOPMODE(RSTOPMODE), .RSTP(RSTP),
    .BCIN(BCIN), .BCOUT(BCOUT), .PCIN(PCIN), .PCOUT(PCOUT)
  );

  initial clk = 0;
  always #5 clk = ~clk;

  initial begin
```

```
    $display("=== DSP Reset Verification Test ===");

    A = $random;
    B = $random;
    D = $random;
    C = $random;
    CARRYIN = $random;
    OPMODE = $random;
    BCIN = $random;
    PCIN = $random;

    RSTA = 1;
    RSTB = 1;
    RSTC = 1;
    RSTD = 1;
    RSTCARRYIN = 1;
    RSTM = 1;
    RSTOPMODE = 1;
    RSTP = 1;

    CEA = 0;
    CEB = 0;
    CEC = 0;
    CECARRYIN = 0;
    CED = 0;
    CEM = 0;
    CEOPMODE = 0;
    CEP = 0;


    @(negedge clk);

    if (M !== 0 || P !== 0 || CARRYOUT !== 0 || CARRYOUTF !== 0 || BCOUT !== 0 ||
PCOUT !== 0) begin
        $display(" Reset Test FAILED at time %0t", $time);
        $display("M = %h, P = %h, CARRYOUT = %b, BCOUT = %h, PCOUT = %h", M, P,
CARRYOUT, BCOUT, PCOUT);
        $stop;
    end else begin
        $display(" Reset Test PASSED");
    end

    RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0;
    RSTCARRYIN = 0; RSTM = 0; RSTOPMODE = 0; RSTP = 0;
```



```
    CEA = 1; CEB = 1; CEC = 1; CECARRYIN = 1;
    CED = 1; CEM = 1; CEOPMODE = 1; CEP = 1;

    $display("=== DSP PATH1 Verification Test ===");

    A = 20;
    B = 10;
    C = 48'd350;
    D = 25;
    OPMODE = 8'b11011101;
    BCIN = $random;
    PCIN = $random;
    CARRYIN = $random;

    repeat (4) @(negedge clk);


    if (BCOUT != 18'h00F || M != 36'h12C || P != 48'h32 || PCOUT != 48'h32 ||
CARRYOUT != 0 || CARRYOUTF != 0) begin
        $display(" DSP Path 1 Test FAILED");
        $display("BCOUT     = %h (expected 000F)", BCOUT);
        $display("M         = %h (expected 012C)", M);
        $display("P         = %h (expected 0032)", P);
        $display("PCOUT     = %h (expected 0032)", PCOUT);
        $display("CARRYOUT  = %b (expected 0)", CARRYOUT);
        $display("CARRYOUTF = %b (expected 0)", CARRYOUTF);

        $stop;
    end else begin
        $display(" DSP Path 1 Test PASSED");
    end

    $display("=== DSP PATH2 Verification Test ===");
    A = 20;
    B = 10;
    C = 48'd350;
    D = 25;
    OPMODE = 8'b00010000;
    BCIN = $random;
    PCIN = $random;
    CARRYIN = $random;

    repeat (3) @(negedge clk);
```



```
    if (BCOUT != 18'h23 || M != 36'h2bc || P != 0 || PCOUT != 0 || CARRYOUT != 0
|| CARRYOUTF != 0) begin
        $display(" DSP Path 2 Test FAILED");
        $display("BCOUT     = %h (expected 0023)", BCOUT);
        $display("M         = %h (expected 02bc)", M);
        $display("P         = %h (expected 0000)", P);
        $display("PCOUT     = %h (expected 0000)", PCOUT);
        $display("CARRYOUT  = %b (expected 0)", CARRYOUT);
        $display("CARRYOUTF = %b (expected 0)", CARRYOUTF);

        $stop;
    end else begin
        $display(" DSP Path 2 Test PASSED");
    end

    $display("=== DSP PATH3 Verification Test ===");

    last_CARRYOUT = CARRYOUTF;
    last_P = PCOUT;

    A = 20;
    B = 10;
    C = 48'd350;
    D = 25;
    OPMODE = 8'b00001010;
    BCIN = $random;
    PCIN = $random;
    CARRYIN = $random;

    repeat (3) @(negedge clk);

    if (BCOUT != 18'ha || M != 36'hc8 || P != last_P || CARRYOUT !=
last_CARRYOUT) begin
        $display(" DSP Path 3 Test FAILED");
        $display("BCOUT     = %h (expected 000a)", BCOUT);
        $display("M         = %h (expected 00c8)", M);
        $display("P         = %h (expected %h)", P, last_P);
        $display("CARRYOUT  = %b (expected 0)", CARRYOUT);

        $stop;
    end else begin
        $display(" DSP Path 3 Test PASSED");
    end

    $display("=== DSP PATH4 Verification Test ===");
    A = 5;
    B = 6;
    C = 48'd350;
    D = 25;
    PCIN = 48'd3000;
    OPMODE = 8'b10100111;
    BCIN = $random;
    CARRYIN = $random;

    repeat (3) @(negedge clk);

    if (BCOUT != 18'h6 || M != 36'h1e || P != 48'hfe6fffec0bb1 || PCOUT !=
48'hfe6fffec0bb1 || CARRYOUT != 1 || CARRYOUTF != 1) begin
        $display(" DSP Path 4 Test FAILED");
        $display("BCOUT     = %h (expected 000a)", BCOUT);
        $display("M         = %h (expected 00c8)", M);
        $display("P         = %h (expected fe6fffec0bb1)", P );
        $display("PCOUT     = %h (expected fe6fffec0bb1)", PCOUT);
        $display("CARRYOUT  = %b (expected 1)", CARRYOUT);
        $display("CARRYOUTF = %b (expected 1)", CARRYOUTF);

        $stop;
    end else begin
        $display(" DSP Path 4 Test PASSED");
    end

    $stop;
  end
endmodule
```

Do File

vlib work

vlog DSP.v DSP_tb.v

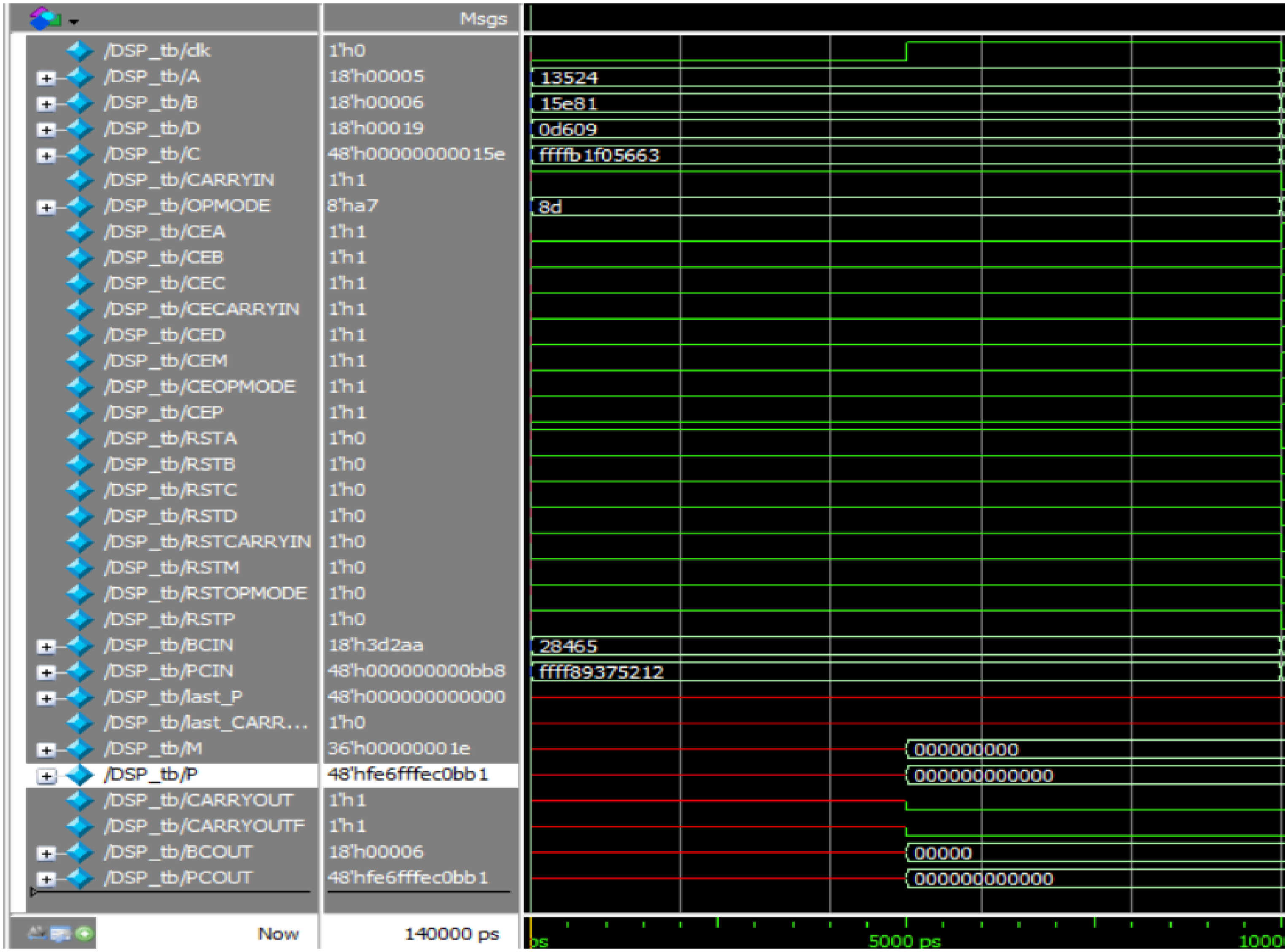
vsim -voptargs=+acc work.DSP_tb

add wave *

run -all

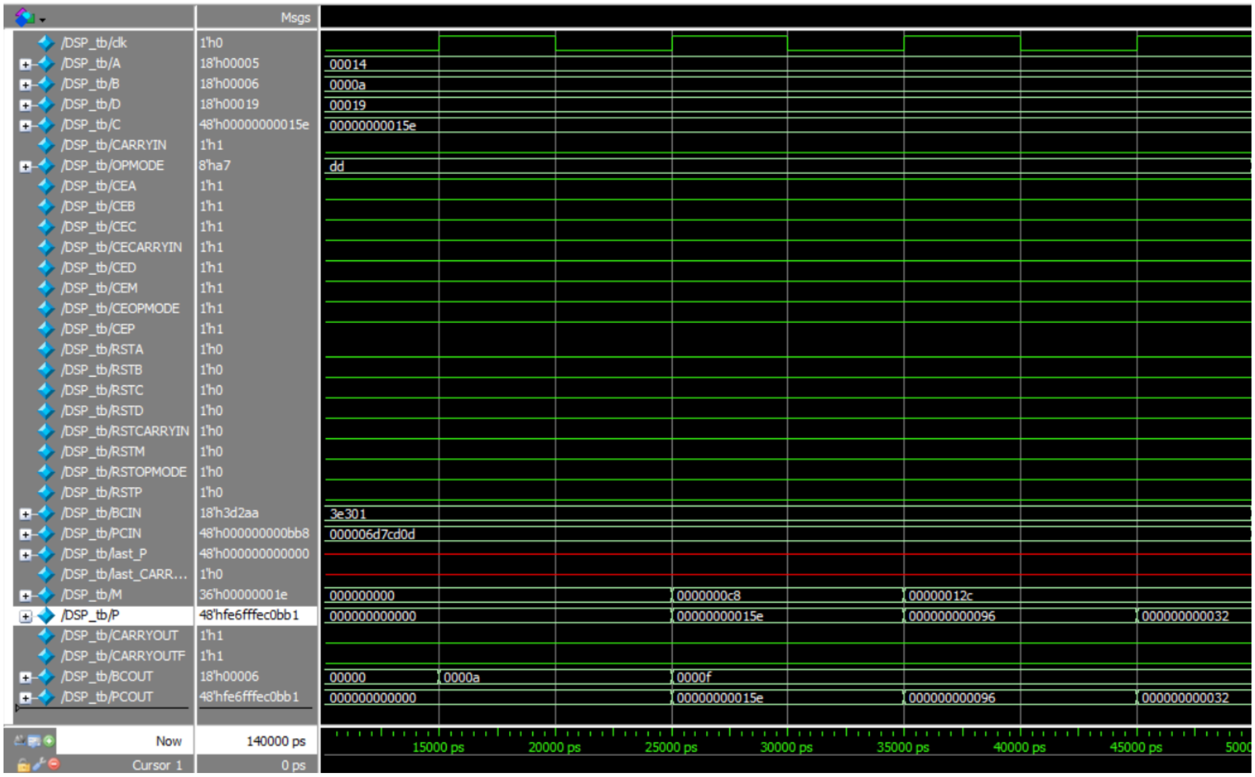
Questasim snippets

Reset Test



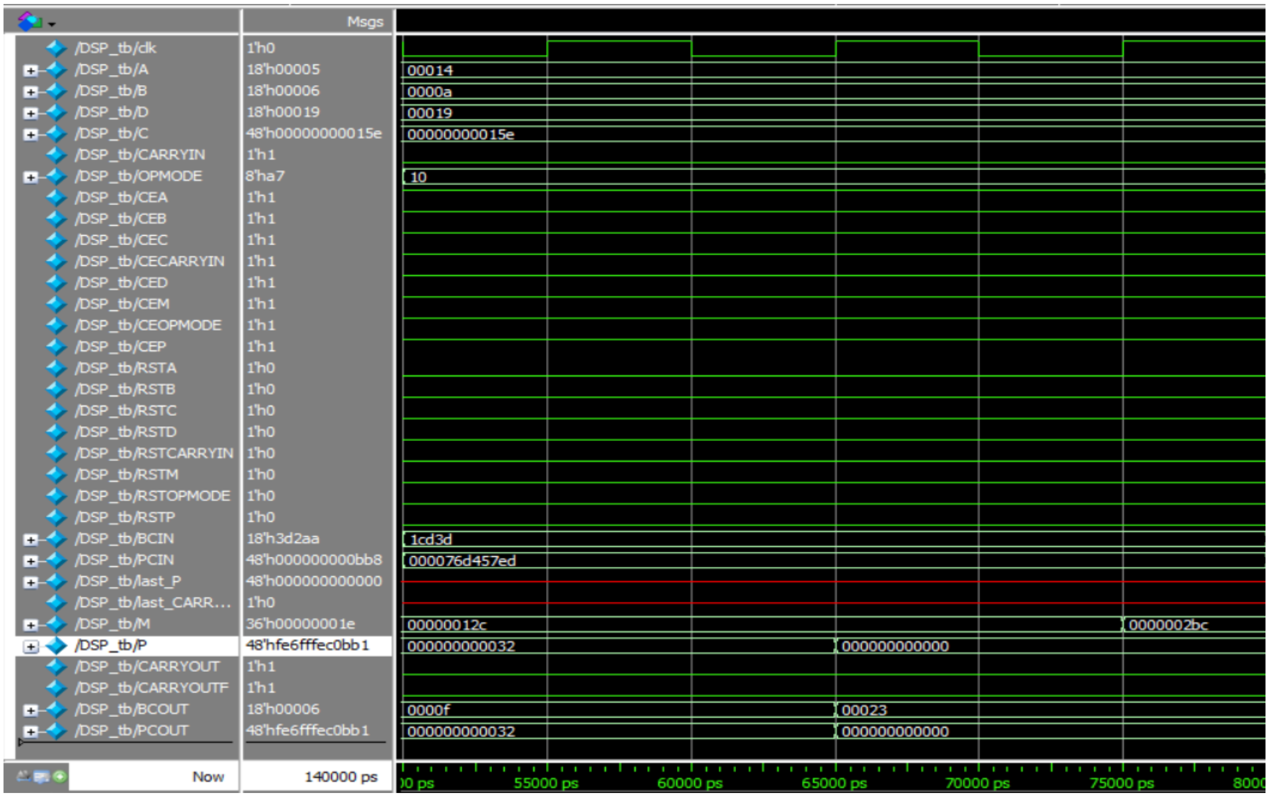
```
                          Msgs
/DSP_tb/clk               1'h0
/DSP_tb/A                 18'h00005
/DSP_tb/B                 18'h00006
/DSP_tb/D                 18'h00019
/DSP_tb/C                 48'h00000000015e
/DSP_tb/CARRYIN           1'h1
/DSP_tb/OPMODE            8'ha7
/DSP_tb/CEA               1'h1
/DSP_tb/CEB               1'h1
/DSP_tb/CEC               1'h1
/DSP_tb/CECARRYIN         1'h1
/DSP_tb/CED               1'h1
/DSP_tb/CEM               1'h1
/DSP_tb/CEOPMODE          1'h1
/DSP_tb/CEP               1'h1
/DSP_tb/RSTA              1'h0
/DSP_tb/RSTB              1'h0
/DSP_tb/RSTC              1'h0
/DSP_tb/RSTD              1'h0
/DSP_tb/RSTCARRYIN        1'h0
/DSP_tb/RSTM              1'h0
/DSP_tb/RSTOPMODE         1'h0
/DSP_tb/RSTP              1'h0
/DSP_tb/BCIN              18'h3d2aa
/DSP_tb/PCIN              48'h000000000bb8
/DSP_tb/last_P            48'h000000000000
/DSP_tb/last_CARR...      1'h0
/DSP_tb/M                 36'h00000001e
/DSP_tb/P                 48'hfe6fffec0bb1
/DSP_tb/CARRYOUT          1'h1
/DSP_tb/CARRYOUTF         1'h1
/DSP_tb/BCOUT             18'h00006
/DSP_tb/PCOUT             48'hfe6fffec0bb1

Now                       140000 ps
```

Path 1 Test



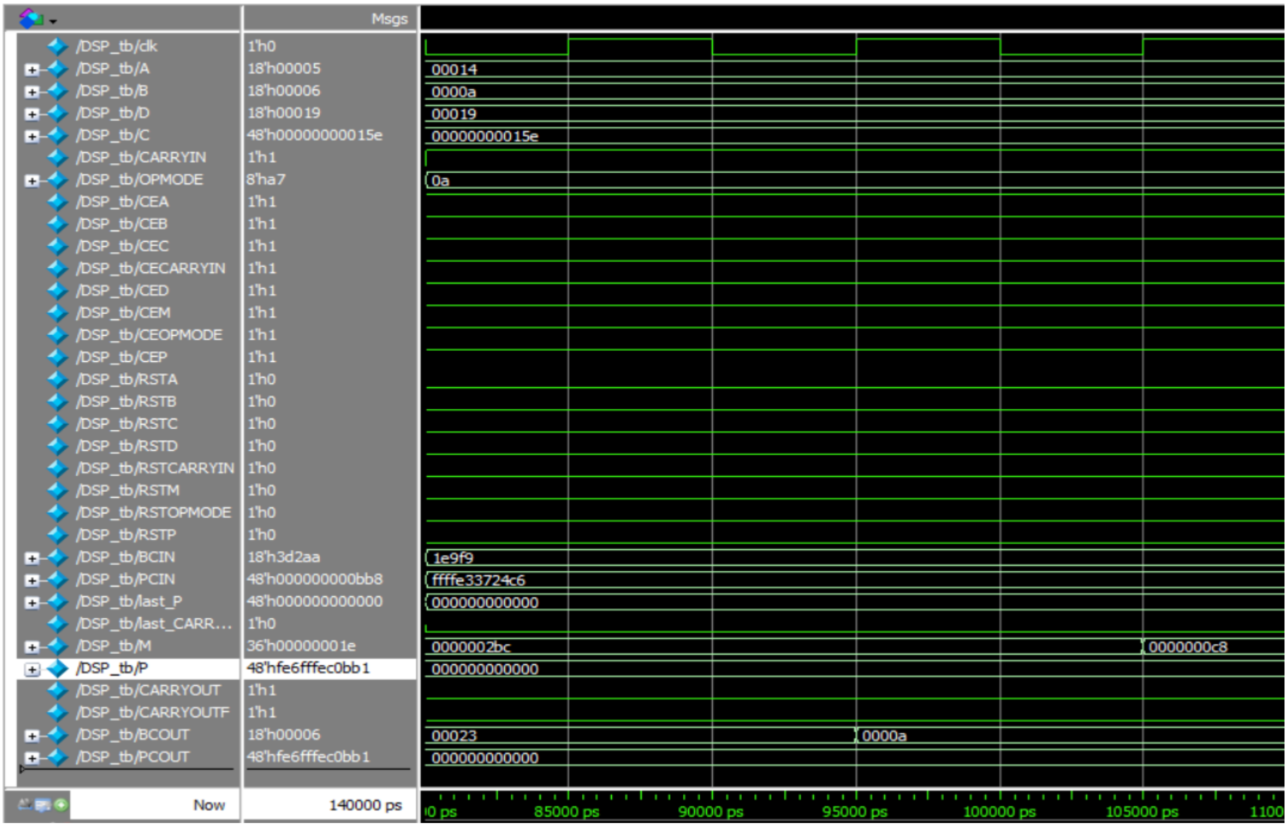
```
                         Msgs
/DSP_tb/clk              1'h0
/DSP_tb/A                18'h00005
/DSP_tb/B                18'h00006
/DSP_tb/D                18'h00019
/DSP_tb/C                48'h00000000015e
/DSP_tb/CARRYIN          1'h1
/DSP_tb/OPMODE           8'ha7
/DSP_tb/CEA              1'h1
/DSP_tb/CEB              1'h1
/DSP_tb/CEC              1'h1
/DSP_tb/CECARRYIN        1'h1
/DSP_tb/CED              1'h1
/DSP_tb/CEM              1'h1
/DSP_tb/CEOPMODE         1'h1
/DSP_tb/CEP              1'h1
/DSP_tb/RSTA             1'h0
/DSP_tb/RSTB             1'h0
/DSP_tb/RSTC             1'h0
/DSP_tb/RSTD             1'h0
/DSP_tb/RSTCARRYIN       1'h0
/DSP_tb/RSTM             1'h0
/DSP_tb/RSTOPMODE        1'h0
/DSP_tb/RSTP             1'h0
/DSP_tb/BCIN             18'h3d2aa
/DSP_tb/PCIN             48'h000000000bb8
/DSP_tb/last_P           48'h000000000000
/DSP_tb/last_CARR...     1'h0
/DSP_tb/M                36'h00000001e
/DSP_tb/P                48'hfe6fffec0bb1
/DSP_tb/CARRYOUT         1'h1
/DSP_tb/CARRYOUTF        1'h1
/DSP_tb/BCOUT            18'h00006
/DSP_tb/PCOUT            48'hfe6fffec0bb1

Now                      140000 ps
Cursor 1                 0 ps
```

Path 2 Test



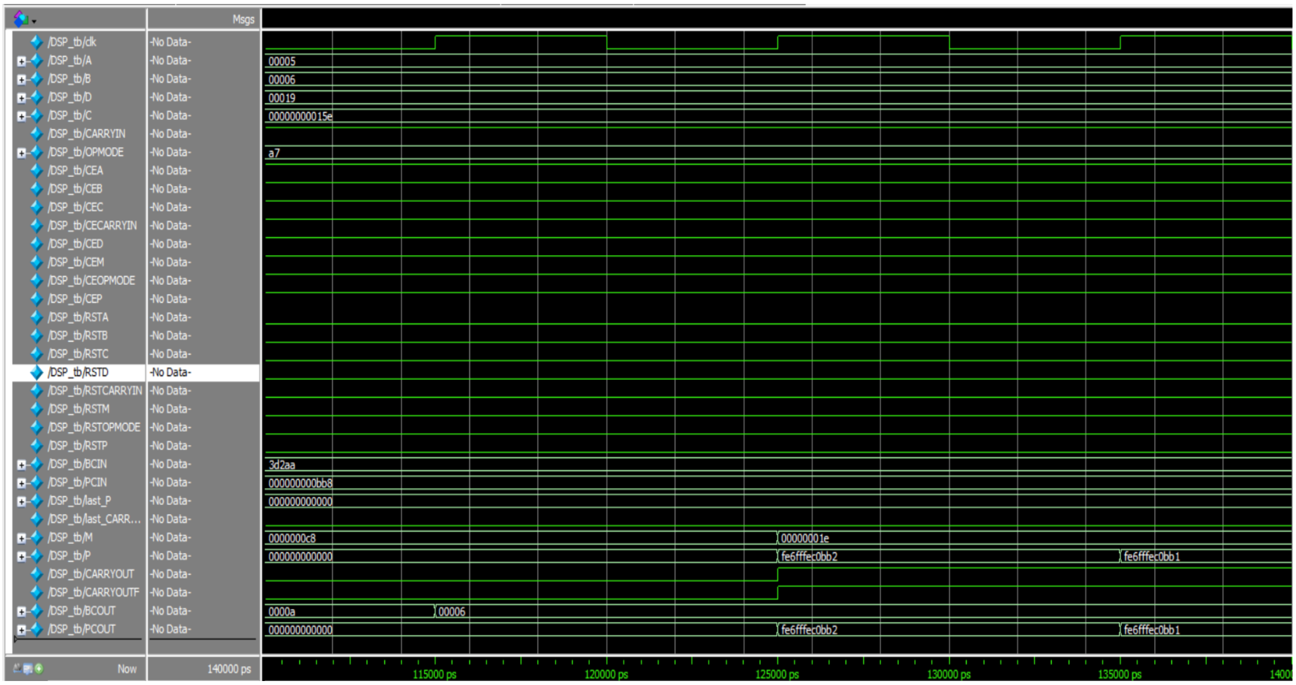
```
                         Msgs
/DSP_tb/clk              1'h0
/DSP_tb/A                18'h00005
/DSP_tb/B                18'h00006
/DSP_tb/D                18'h00019
/DSP_tb/C                48'h00000000015e
/DSP_tb/CARRYIN          1'h1
/DSP_tb/OPMODE           8'ha7
/DSP_tb/CEA              1'h1
/DSP_tb/CEB              1'h1
/DSP_tb/CEC              1'h1
/DSP_tb/CECARRYIN        1'h1
/DSP_tb/CED              1'h1
/DSP_tb/CEM              1'h1
/DSP_tb/CEOPMODE         1'h1
/DSP_tb/CEP              1'h1
/DSP_tb/RSTA             1'h0
/DSP_tb/RSTB             1'h0
/DSP_tb/RSTC             1'h0
/DSP_tb/RSTD             1'h0
/DSP_tb/RSTCARRYIN       1'h0
/DSP_tb/RSTM             1'h0
/DSP_tb/RSTOPMODE        1'h0
/DSP_tb/RSTP             1'h0
/DSP_tb/BCIN             18'h3d2aa
/DSP_tb/PCIN             48'h000000000bb8
/DSP_tb/last_P           48'h000000000000
/DSP_tb/last_CARR...     1'h0
/DSP_tb/M                36'h00000001e
/DSP_tb/P                48'hfe6fffec0bb1
/DSP_tb/CARRYOUT         1'h1
/DSP_tb/CARRYOUTF        1'h1
/DSP_tb/BCOUT            18'h00006
/DSP_tb/PCOUT            48'hfe6fffec0bb1

Now                      140000 ps
```

Path 3 Test



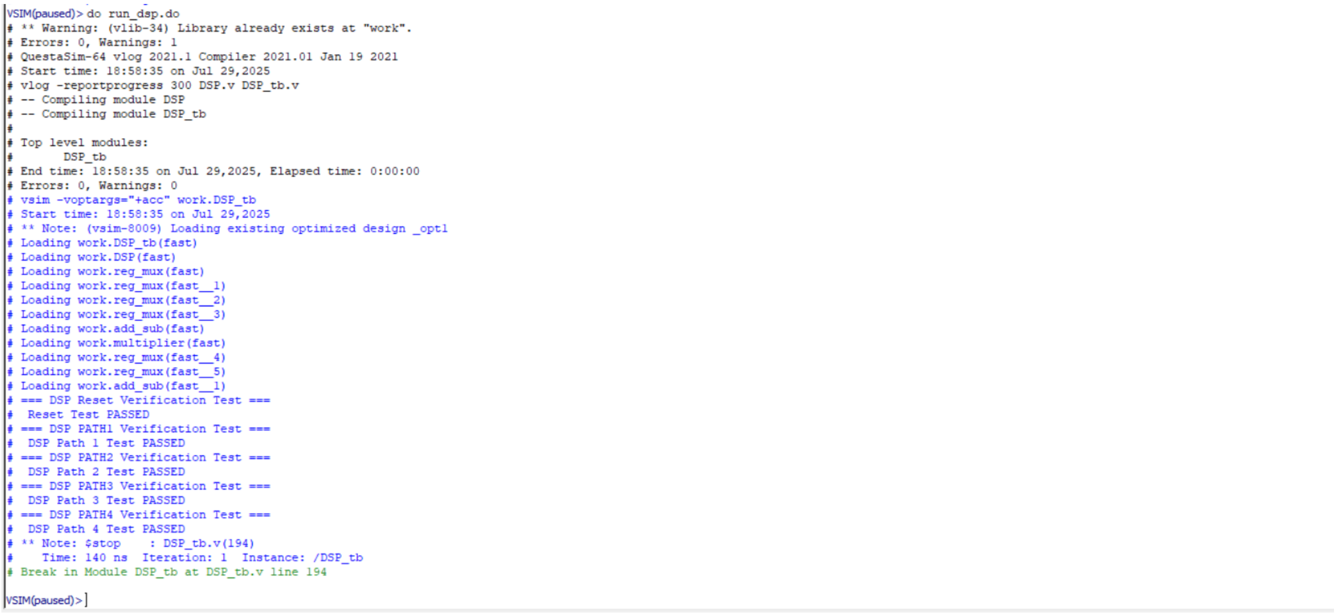
```
                        Msgs
/DSP_tb/clk             1'h0
/DSP_tb/A               18'h00005
/DSP_tb/B               18'h00006
/DSP_tb/D               18'h00019
/DSP_tb/C               48'h00000000015e
/DSP_tb/CARRYIN         1'h1
/DSP_tb/OPMODE          8'ha7
/DSP_tb/CEA             1'h1
/DSP_tb/CEB             1'h1
/DSP_tb/CEC             1'h1
/DSP_tb/CECARRYIN       1'h1
/DSP_tb/CED             1'h1
/DSP_tb/CEM             1'h1
/DSP_tb/CEOPMODE        1'h1
/DSP_tb/CEP             1'h1
/DSP_tb/RSTA            1'h0
/DSP_tb/RSTB            1'h0
/DSP_tb/RSTC            1'h0
/DSP_tb/RSTD            1'h0
/DSP_tb/RSTCARRYIN      1'h0
/DSP_tb/RSTM            1'h0
/DSP_tb/RSTOPMODE       1'h0
/DSP_tb/RSTP            1'h0
/DSP_tb/BCIN            18'h3d2aa
/DSP_tb/PCIN            48'h000000000bb8
/DSP_tb/last_P          48'h000000000000
/DSP_tb/last_CARR...    1'h0
/DSP_tb/M               36'h00000001e
/DSP_tb/P               48'hfe6fffec0bb1
/DSP_tb/CARRYOUT        1'h1
/DSP_tb/CARRYOUTF       1'h1
/DSP_tb/BCOUT           18'h00006
/DSP_tb/PCOUT           48'hfe6fffec0bb1
Now                     140000 ps
```

Path 4 Test



```
                        Msgs
/DSP_tb/clk             -No Data-
/DSP_tb/A               -No Data-
/DSP_tb/B               -No Data-
/DSP_tb/D               -No Data-
/DSP_tb/C               -No Data-
/DSP_tb/CARRYIN         -No Data-
/DSP_tb/OPMODE          -No Data-
/DSP_tb/CEA             -No Data-
/DSP_tb/CEB             -No Data-
/DSP_tb/CEC             -No Data-
/DSP_tb/CECARRYIN       -No Data-
/DSP_tb/CED             -No Data-
/DSP_tb/CEM             -No Data-
/DSP_tb/CEOPMODE        -No Data-
/DSP_tb/CEP             -No Data-
/DSP_tb/RSTA            -No Data-
/DSP_tb/RSTB            -No Data-
/DSP_tb/RSTC            -No Data-
/DSP_tb/RSTD            -No Data-
/DSP_tb/RSTCARRYIN      -No Data-
/DSP_tb/RSTM            -No Data-
/DSP_tb/RSTOPMODE       -No Data-
/DSP_tb/RSTP            -No Data-
/DSP_tb/BCIN            -No Data-
/DSP_tb/PCIN            -No Data-
/DSP_tb/last_P          -No Data-
/DSP_tb/last_CARR...    -No Data-
/DSP_tb/M               -No Data-
/DSP_tb/P               -No Data-
/DSP_tb/CARRYOUT        -No Data-
/DSP_tb/CARRYOUTF       -No Data-
/DSP_tb/BCOUT           -No Data-
/DSP_tb/PCOUT           -No Data-
Now                     140000 ps
```

Transcript



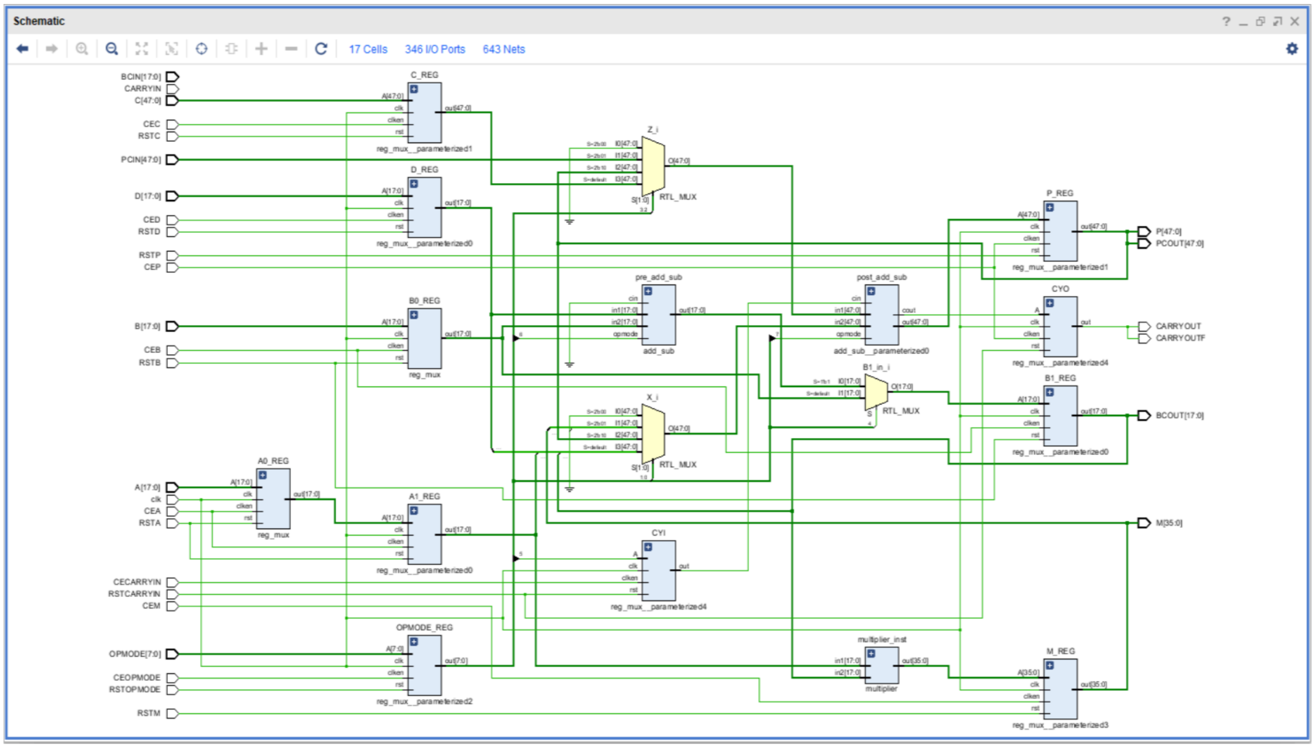
```
VSIM(paused)> do run_dsp.do
# ** Warning: (vlib-34) Library already exists at "work".
# Errors: 0, Warnings: 1
# QuestaSim-64 vlog 2021.1 Compiler 2021.01 Jan 19 2021
# Start time: 18:58:35 on Jul 29,2025
# vlog -reportprogress 300 DSP.v DSP_tb.v
# -- Compiling module DSP
# -- Compiling module DSP_tb
#
# Top level modules:
#       DSP_tb
# End time: 18:58:35 on Jul 29,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vsim -voptargs="+acc" work.DSP_tb
# Start time: 18:58:35 on Jul 29,2025
# ** Note: (vsim-8009) Loading existing optimized design _opt1
# Loading work.DSP_tb(fast)
# Loading work.DSP(fast)
# Loading work.reg_mux(fast)
# Loading work.reg_mux(fast__1)
# Loading work.reg_mux(fast__2)
# Loading work.reg_mux(fast__3)
# Loading work.add_sub(fast)
# Loading work.multiplier(fast)
# Loading work.reg_mux(fast__4)
# Loading work.reg_mux(fast__5)
# Loading work.add_sub(fast__1)
# === DSP Reset Verification Test ===
#  Reset Test PASSED
# === DSP PATH1 Verification Test ===
#  DSP Path 1 Test PASSED
# === DSP PATH2 Verification Test ===
#  DSP Path 2 Test PASSED
# === DSP PATH3 Verification Test ===
#  DSP Path 3 Test PASSED
# === DSP PATH4 Verification Test ===
#  DSP Path 4 Test PASSED
# ** Note: $stop    : DSP_tb.v(194)
#    Time: 140 ns  Iteration: 1  Instance: /DSP_tb
# Break in Module DSP_tb at DSP_tb.v line 194

VSIM(paused)>
```

Constraint file

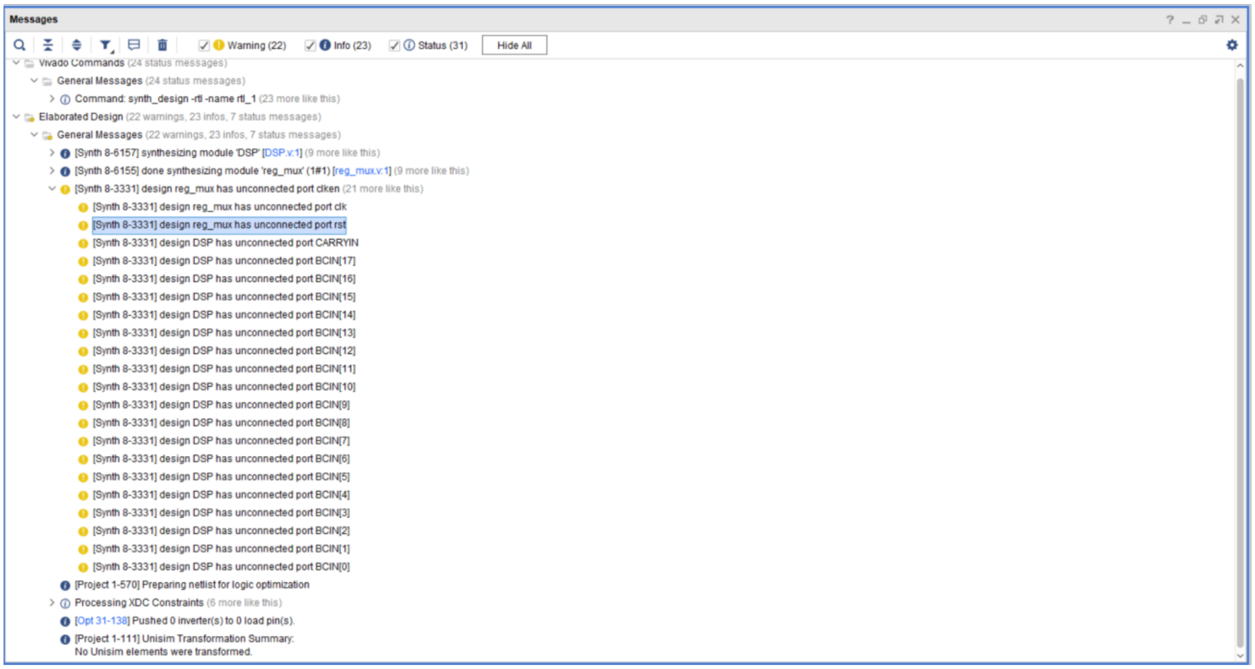
```
## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports clk]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add
[get_ports clk]
```

Elaboration

Schematic



Messages



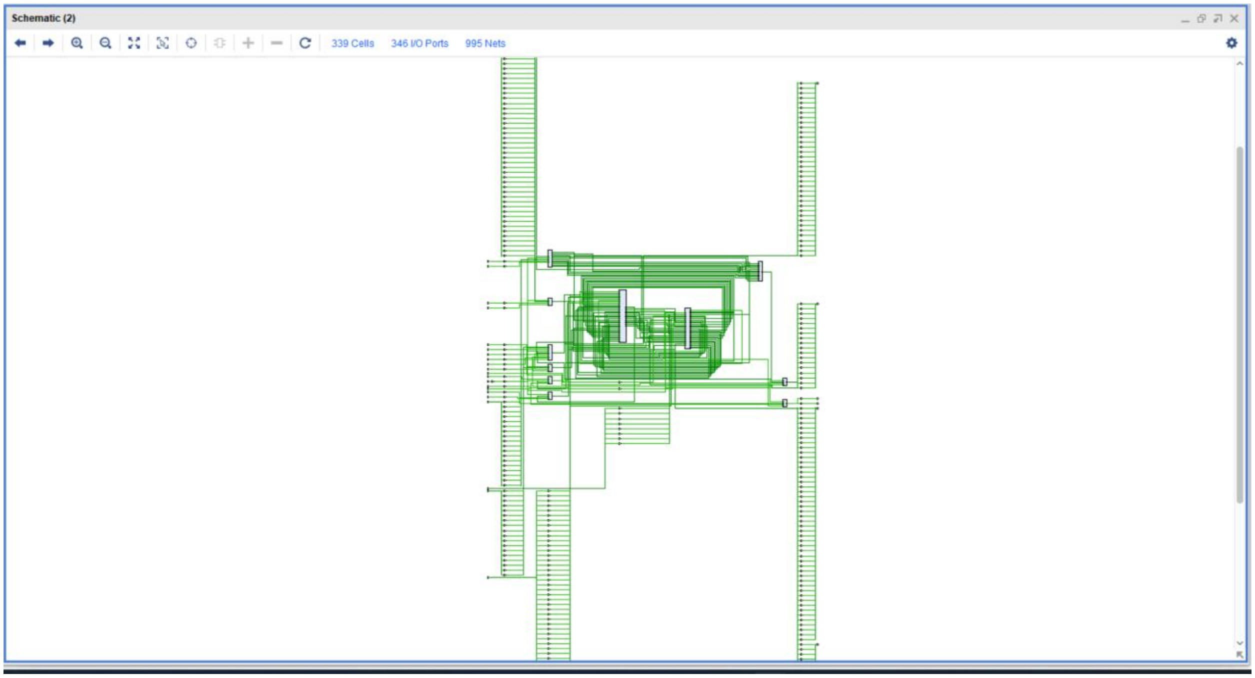
Messages

☑ Warning (22) ☑ Info (23) ☑ Status (31) Hide All

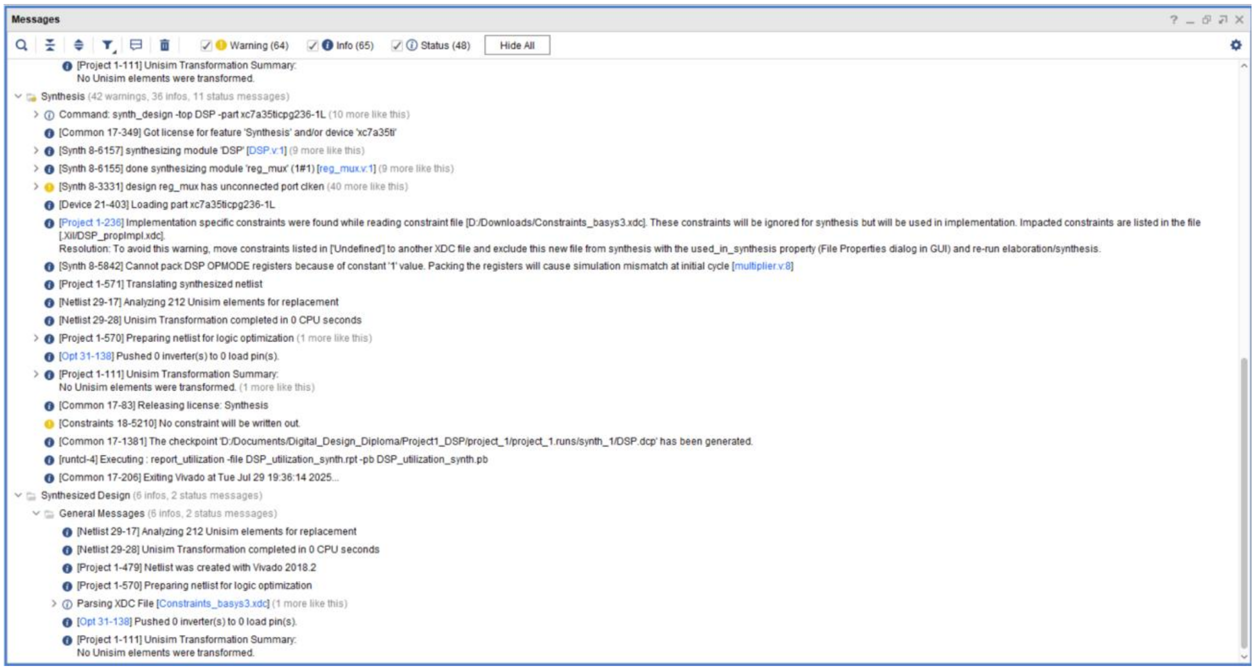
```
Vivado Commands (24 status messages)
  General Messages (24 status messages)
    Command: synth_design -rtl -name rtl_1 (23 more like this)
Elaborated Design (22 warnings, 23 infos, 7 status messages)
  General Messages (22 warnings, 23 infos, 7 status messages)
    [Synth 8-6157] synthesizing module 'DSP' [DSP.v:1] (9 more like this)
    [Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [reg_mux.v:1] (9 more like this)
    [Synth 8-3331] design reg_mux has unconnected port clken (21 more like this)
      [Synth 8-3331] design reg_mux has unconnected port clk
      [Synth 8-3331] design reg_mux has unconnected port rst
      [Synth 8-3331] design DSP has unconnected port CARRYIN
      [Synth 8-3331] design DSP has unconnected port BCIN[17]
      [Synth 8-3331] design DSP has unconnected port BCIN[16]
      [Synth 8-3331] design DSP has unconnected port BCIN[15]
      [Synth 8-3331] design DSP has unconnected port BCIN[14]
      [Synth 8-3331] design DSP has unconnected port BCIN[13]
      [Synth 8-3331] design DSP has unconnected port BCIN[12]
      [Synth 8-3331] design DSP has unconnected port BCIN[11]
      [Synth 8-3331] design DSP has unconnected port BCIN[10]
      [Synth 8-3331] design DSP has unconnected port BCIN[9]
      [Synth 8-3331] design DSP has unconnected port BCIN[8]
      [Synth 8-3331] design DSP has unconnected port BCIN[7]
      [Synth 8-3331] design DSP has unconnected port BCIN[6]
      [Synth 8-3331] design DSP has unconnected port BCIN[5]
      [Synth 8-3331] design DSP has unconnected port BCIN[4]
      [Synth 8-3331] design DSP has unconnected port BCIN[3]
      [Synth 8-3331] design DSP has unconnected port BCIN[2]
      [Synth 8-3331] design DSP has unconnected port BCIN[1]
      [Synth 8-3331] design DSP has unconnected port BCIN[0]
    [Project 1-570] Preparing netlist for logic optimization
    Processing XDC Constraints (6 more like this)
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed.
```

Synthesis

Schematic

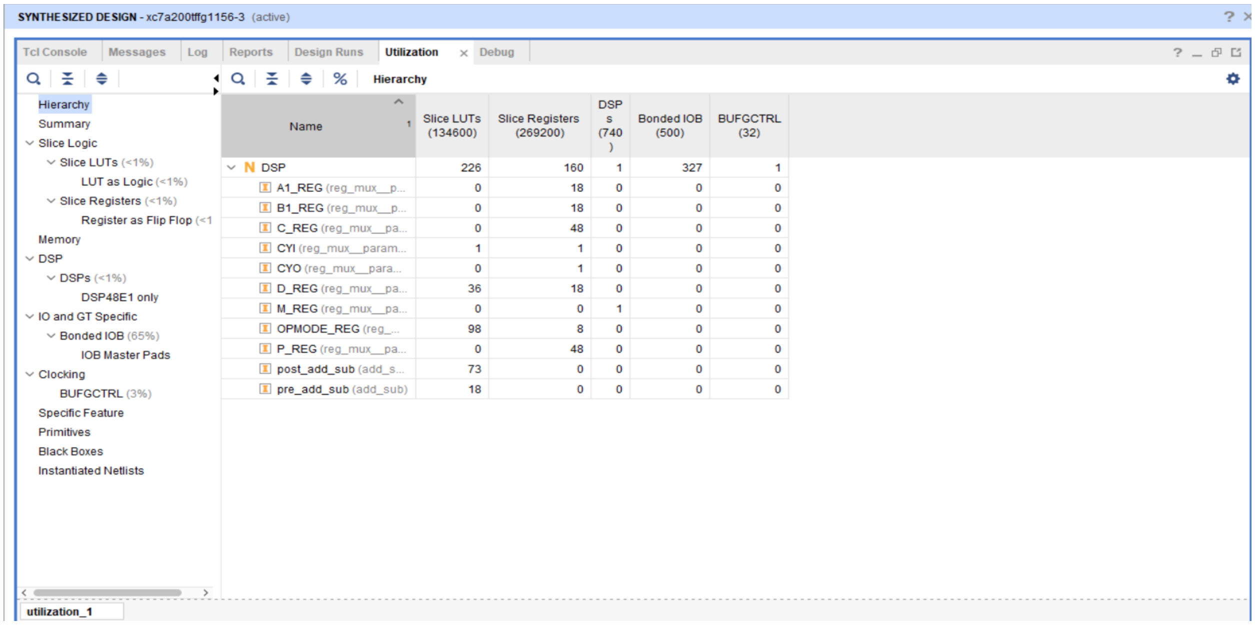


Messages tab



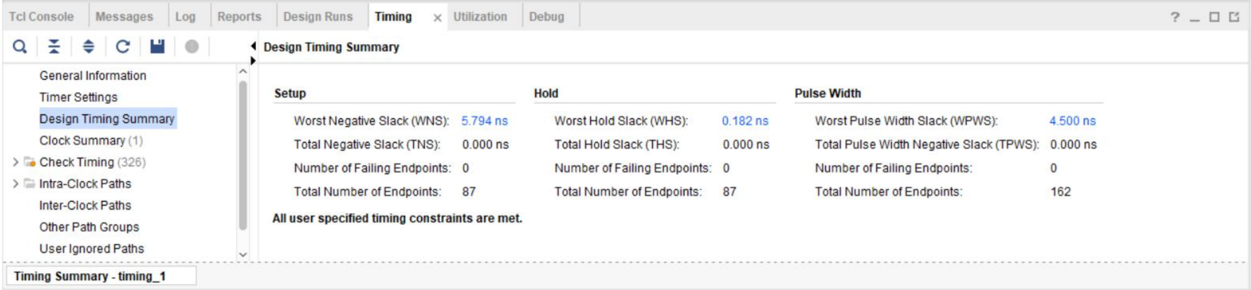
```
    [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed.
Synthesis (42 warnings, 36 infos, 11 status messages)
  Command: synth_design -top DSP -part xc7a35ticpg236-1L (10 more like this)
  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  [Synth 8-6157] synthesizing module 'DSP' [DSP.v:1] (9 more like this)
  [Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [reg_mux.v:1] (9 more like this)
  [Synth 8-3331] design reg_mux has unconnected port clken (40 more like this)
  [Device 21-403] Loading part xc7a35ticpg236-1L
  [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/Downloads/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file
  [.Xil/DSP_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [multiplier.v:8]
  [Project 1-571] Translating synthesized netlist
  [Netlist 29-17] Analyzing 212 Unisim elements for replacement
  [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
  [Common 17-83] Releasing license: Synthesis
  [Constraints 18-5210] No constraint will be written out.
  [Common 17-1381] The checkpoint 'D:/Documents/Digital_Design_Diploma/Project1_DSP/project_1/project_1.runs/synth_1/DSP.dcp' has been generated.
  [runtcl-4] Executing : report_utilization -file DSP_utilization_synth.rpt -pb DSP_utilization_synth.pb
  [Common 17-206] Exiting Vivado at Tue Jul 29 19:36:14 2025...
Synthesized Design (6 infos, 2 status messages)
  General Messages (6 infos, 2 status messages)
    [Netlist 29-17] Analyzing 212 Unisim elements for replacement
    [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    [Project 1-479] Netlist was created with Vivado 2018.2
    [Project 1-570] Preparing netlist for logic optimization
    Parsing XDC File [Constraints_basys3.xdc] (1 more like this)
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed.
```

Utilization report



Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP	226	160	1	327	1
A1_REG (reg_mux__p...	0	18	0	0	0
B1_REG (reg_mux__p...	0	18	0	0	0
C_REG (reg_mux__pa...	0	48	0	0	0
CYI (reg_mux__param...	1	1	0	0	0
CYO (reg_mux__para...	0	1	0	0	0
D_REG (reg_mux__pa...	36	18	0	0	0
M_REG (reg_mux__pa...	0	0	1	0	0
OPMODE_REG (reg_...	98	8	0	0	0
P_REG (reg_mux__pa...	0	48	0	0	0
post_add_sub (add_s...	73	0	0	0	0
pre_add_sub (add_sub)	18	0	0	0	0

Timing report



Design Timing Summary

Setup

Worst Negative Slack (WNS): 5.794 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87

Hold

Worst Hold Slack (WHS): 0.182 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87

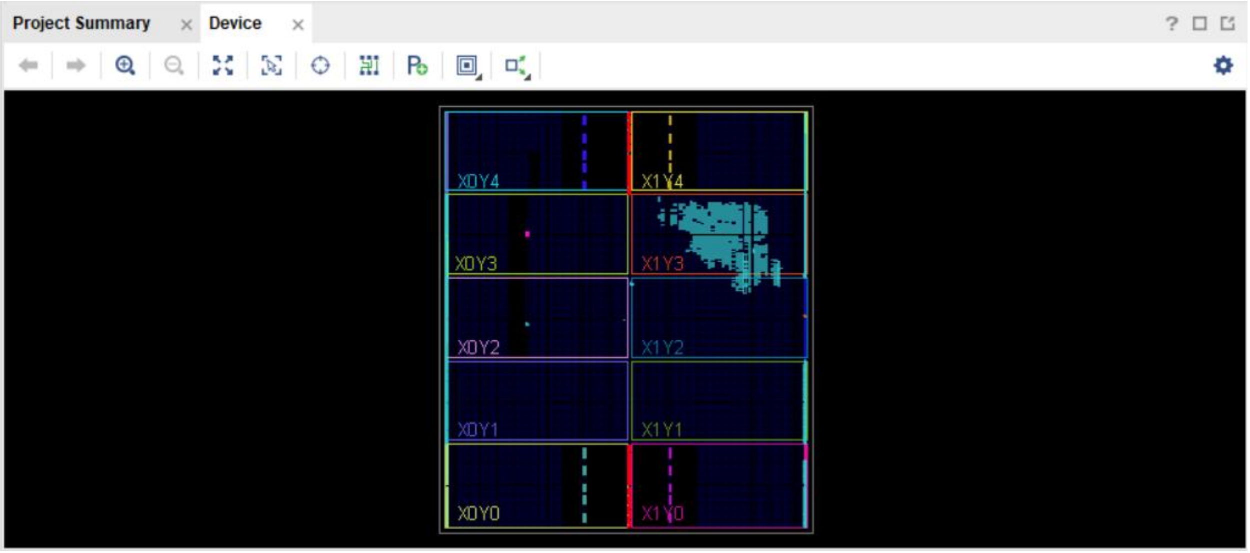
Pulse Width

Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 162

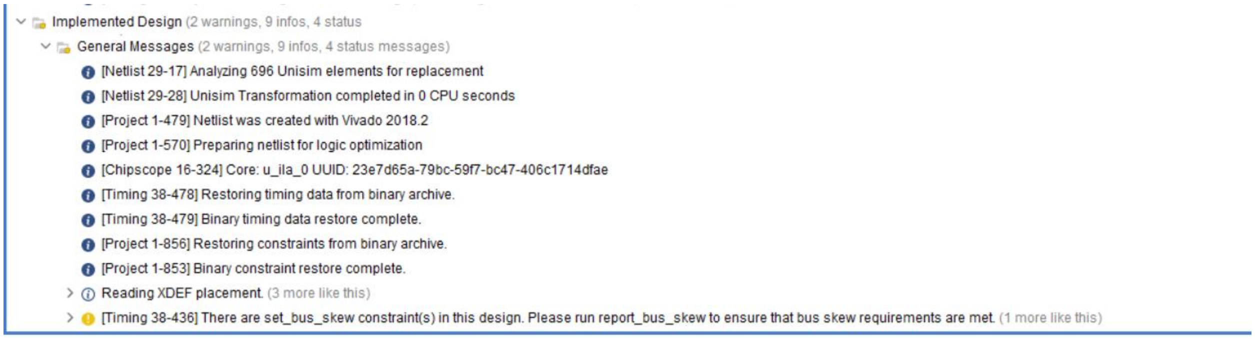
All user specified timing constraints are met.

Implementation

Device schematic



Messages tab

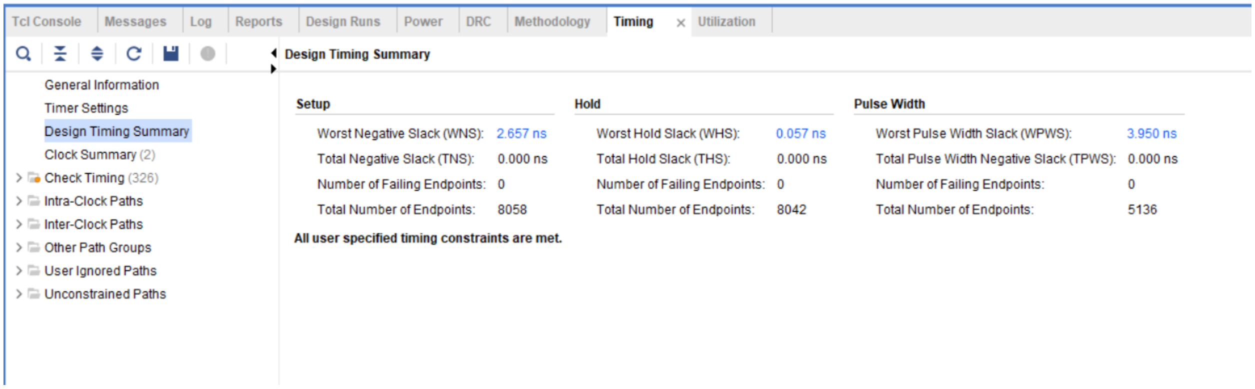


Implemented Design (2 warnings, 9 infos, 4 status

General Messages (2 warnings, 9 infos, 4 status messages)

```
[Netlist 29-17] Analyzing 696 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfae
[Timing 38-478] Restoring timing data from binary archive.
[Timing 38-479] Binary timing data restore complete.
[Project 1-856] Restoring constraints from binary archive.
[Project 1-853] Binary constraint restore complete.
Reading XDEF placement. (3 more like this)
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met. (1 more like this)
```

Timing report

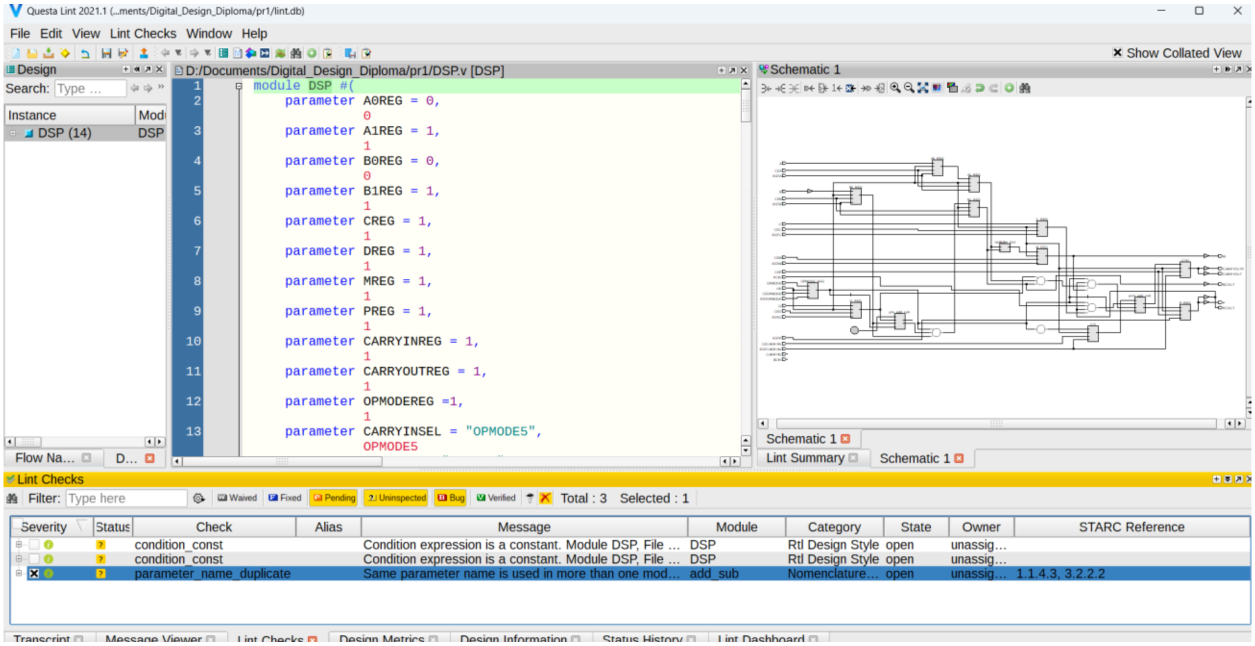


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.657 ns	Worst Hold Slack (WHS):	0.057 ns	Worst Pulse Width Slack (WPWS):	3.950 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8058	Total Number of Endpoints:	8042	Total Number of Endpoints:	5136

All user specified timing constraints are met.

Lint



D:/Documents/Digital_Design_Diploma/pr1/DSP.v [DSP]

```
module DSP #(
    parameter A0REG = 0,
              0
    parameter A1REG = 1,
              1
    parameter B0REG = 0,
              0
    parameter B1REG = 1,
              1
    parameter CREG = 1,
              1
    parameter DREG = 1,
              1
    parameter MREG = 1,
              1
    parameter PREG = 1,
              1
    parameter CARRYINREG = 1,
              1
    parameter CARRYOUTREG = 1,
              1
    parameter OPMODEREG =1,
              1
    parameter CARRYINSEL = "OPMODE5",
              OPMODE5
```

Total : 3 Selected : 1

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
☐	?	condition_const		Condition expression is a constant. Module DSP, File ...	DSP	Rtl Design Style	open	unassig...	
☐	?	condition_const		Condition expression is a constant. Module DSP, File ...	DSP	Rtl Design Style	open	unassig...	
☒	?	parameter_name_duplicate		Same parameter name is used in more than one mod...	add_sub	Nomenclature...	open	unassig...	1.1.4.3, 3.2.2.2