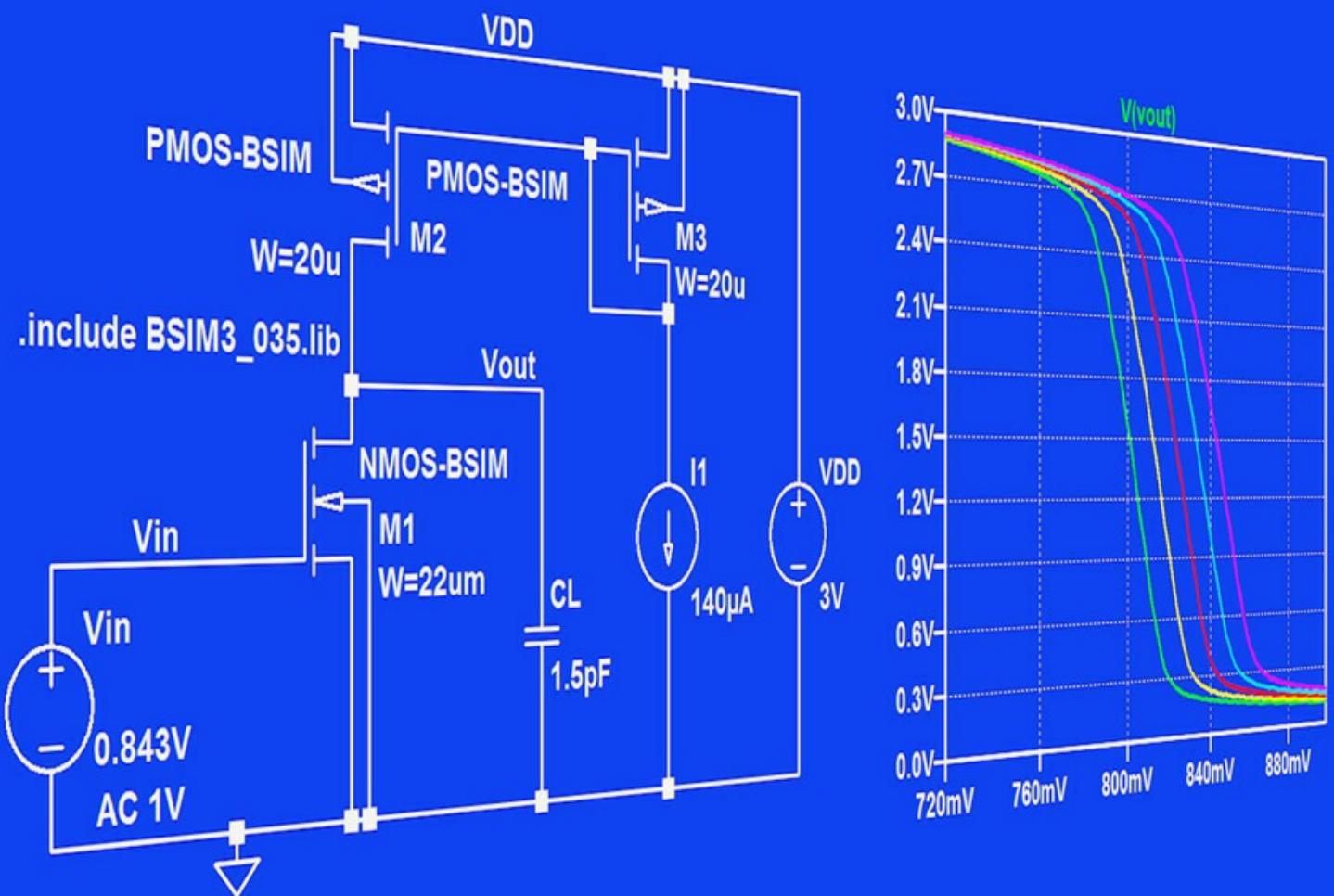


CMOS Integrated Circuit Simulation: Solutions

Erik Bruun



Download free books at

bookboon.com

ERIK BRUUN

CMOS INTEGRATED CIRCUIT SIMULATION: SOLUTIONS

CMOS Integrated Circuit Simulation: Solutions

2nd edition

© 2017 Erik Bruun & bookboon.com

ISBN 978-87-403-1588-2

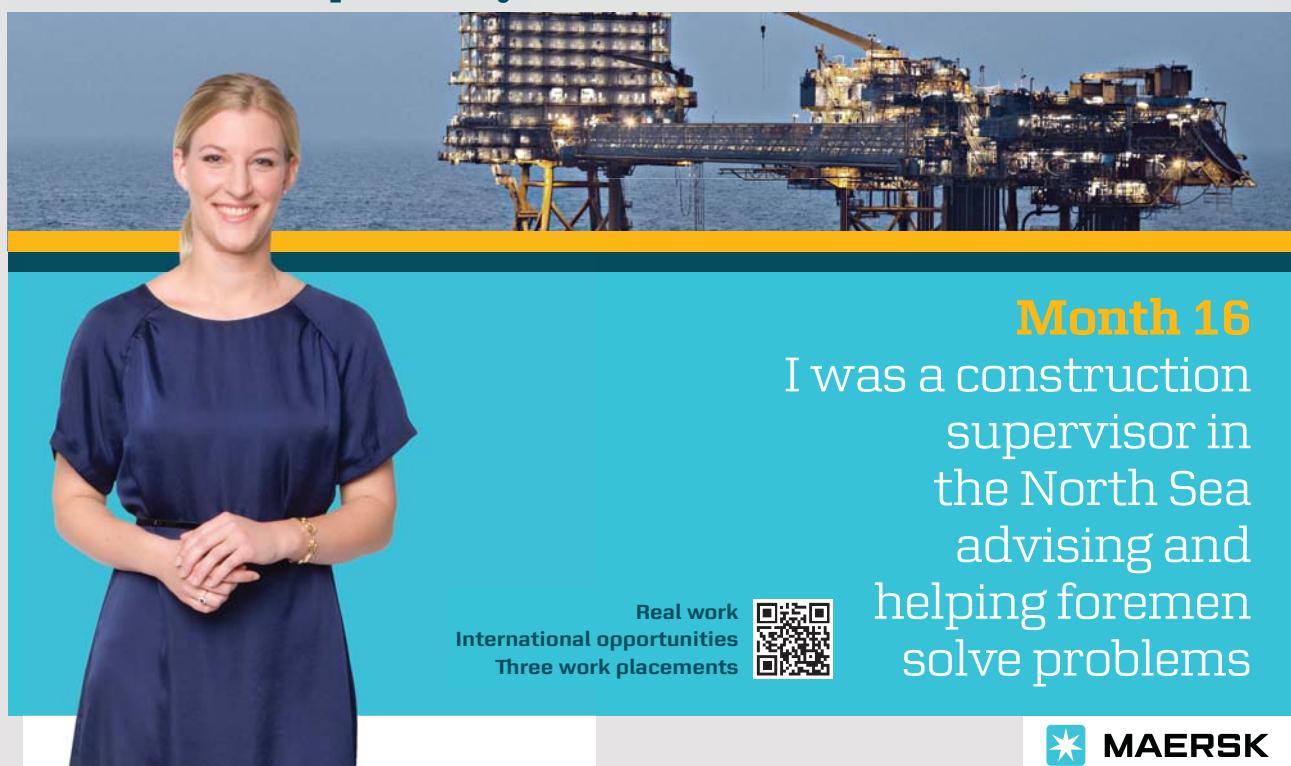
Peer reviewed by Ivan H.H. Jørgensen, Associate Professor, Technical University of Denmark

CONTENTS

Preface	5
Introduction	6
Tutorial 1 – Resistive Circuits	9
Tutorial 2 – Circuits with Capacitors and Inductors	23
Tutorial 3 – MOS Transistors	35
Tutorial 4 – Basic Gain Stages	53
Tutorial 5 – Hierarchical Design	81
Tutorial 6 – Process and Parameter Variations	93
Tutorial 7 – Importing and Exporting Files	109

I joined MITAS because
I wanted **real responsibility**

The Graduate Programme
for Engineers and Geoscientists
www.discovermitas.com



Month 16
I was a construction supervisor in the North Sea advising and helping foremen solve problems

Real work
International opportunities
Three work placements





Preface

This book contains the end-of-chapter problems for each of the tutorials in the book ‘CMOS Integrated Circuit Simulation with LTspice’ (2nd Edition, 2016, also published by Bookboon) and provides solutions to the problems. For each of the problems, corresponding LTspice schematics are shown together with the simulation outputs resulting from running the simulations specified in the schematic. Also, the required interpretation of the simulation results is given.

Often, there is not just one possible way of solving the problems. Several options exist when drawing a schematic in LTspice and several different simulations may be specified in order to arrive at a solution, so the solutions given here should just be taken as examples of how the simulations may be performed.

The problems are reprinted from ‘CMOS Integrated Circuit Simulation with LTspice, 2nd Edition’, and page and figure references given in the problems are to pages and figures from this book. However, for convenience, several of the figures referred to in the problems are also shown here. When the problems refer to the BSIM transistor models from Fig. 3.10 on page 86, Fig. 6.2 on page 193 (or Fig. P3.2 on page 109 and Fig. P3.3 on page 110), you may turn to the Introduction in the present book to find out how to create the model file.

The simulations in this book have been performed using LTspice version XVII, dated 10 October 2016.

I hope you find the problems and solutions useful. If you find typos or errors, I would appreciate your feedback. Suggestions for improvement are also welcome. You may send them to me by email, eb@elektro.dtu.dk.

Erik Bruun

Department of Electrical Engineering, Technical University of Denmark.

Introduction

In many of the solutions to the problems, waveform plots are used to find values of voltages, currents, frequencies, etc. The values are found using the cursors activated by a left-click on the name of the trace appearing above the plot. The cursor position is inserted in the plot by the command ‘Plot Settings → Notes & Annotations → Label Curs. Pos.’ or keyboard shortcut ‘F4’. When inserted, the position is given with a large number of digits, typically eight. In most cases, this does not correspond to a relevant precision, so the position is edited to a reasonable number of digits by an editing of the text appearing in the text window resulting from a right-click on the label with the cursor position.

The file ‘BSIM3_035.lib’ is used in several of the problems in this book. It is derived from the file ‘p35_model_card.inc’ contained in the zip archive ‘p35.zip’ which can be downloaded from (Chan Carusone, Johns & Martin 2014). A few of the parameters in ‘p35_model_card.inc’ are deleted since they are ignored by LTspice anyway, and the parameters VTH0, TOX, U0, CJ, CJSW in ‘p35_model_card.inc’ which depend on process corners are given their nominal values for a typical process. The parameters which are deleted will not influence the simulation results significantly for normal values of transistor geometries. Also, the transistor models are named ‘NMOS-BSIM’ and ‘PMOS-BSIM’ rather than just ‘NMOS’ and ‘PMOS’ in order to emphasize that they are BSIM models, not just the default Spice models.

The following page shows the file ‘p35_model_card.inc’ with the modifications introduced for the model file ‘BSIM3_035.lib’ used in this book.

```
*p35_model_cardBSIM_035.lib
.MODEL NMOS_BSIM NMOS LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = -7.8E-9/proc_delta
+XJ = 1E-07 NCH = 2.18E+17 VTH0 = -0.48+vt_shift
+K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01
+K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07
+DVTOW = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01
+U0 = -360*proc_delta*proc_delta UA = -8.48E-10 UB = 2.27E-18
+UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00
+AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06
+KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01
+RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02
+WWR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10
+XL = -5.00E-08 XW = -1.50E-07 DWG = -4.27E-09
+DWB = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00
+CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00
+CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01
+DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04
+PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-04
+PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02
+DELTA = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.11E-01
+KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09
+UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04
+WLN = 0 WLN = 9.95E-01 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12
+CJ = 1.9e-4/proc_delta PB = 7.95E-01 MJ = 3.53E-01
+CJSW = 1.28e-10/proc_delta PBSW = 7.98E-01 MJSW = 1.73E-01
+CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01
+CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01
+PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03

.MODEL PMOS_BSIM PMOS LEVEL = 49
+VERSION = 3.1 TNOM = 2.69E+01 TOX = -7.8E-9/proc_delta
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = -0.6+vt_shift
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVTOW = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = -150*proc_delta*proc_delta UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WWR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+XL = -4.98E-08 XW = -1.51E-07 DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WLN = 0 WLN = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = 1.4e-4/proc_delta PB = 9.83E-01 MJ = 5.79E-01
+CJSW = 1.32e-10/proc_delta PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

For several of the problems for Tutorial 6, the file ‘BSIM3_035PVT.lib’ is used. This file is derived from the file ‘BSIM3_035.lib’ by introducing the speed parameters ‘SN’ and ‘SP’ for the process dependent parameters VTH0, TOX, U0, CJ, CJSW. The nominal values for typical process parameters are replaced by the expressions given below.

NMOS transistors:

$$\begin{aligned}VTH0 &= \{0.48 - SN/10\} \\TOX &= \{7.8E - 9/(1 + SN/20)\} \\U0 &= \{360 * (1 + SN/20) ** 2\} \\CJ &= \{9e - 4/(1 + SN/20)\} \\CJSW &= \{2.8e - 10/(1 + SN/20)\}\end{aligned}$$

PMOS transistors:

$$\begin{aligned}VTH0 &= \{-0.6 + SP/10\} \\TOX &= \{7.8E - 9/(1 + SP/20)\} \\U0 &= \{150 * (1 + SP/20) ** 2\} \\CJ &= \{14e - 4/(1 + SP/20)\} \\CJSW &= \{3.2e - 10/(1 + SP/20)\}\end{aligned}$$

References

Chan Carusone, T., Johns, D. & Martin, K. 2014, *Analog Integrated Circuit Design, Netlist and model files*. Retrieved from <http://analogicdesign.com/students/netlists-models/>

Tutorial 1 – Resistive Circuits

1.1

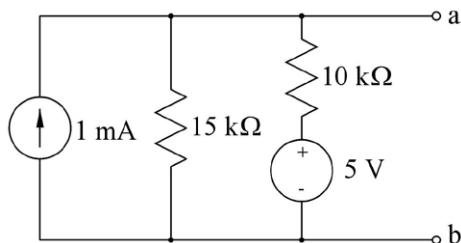
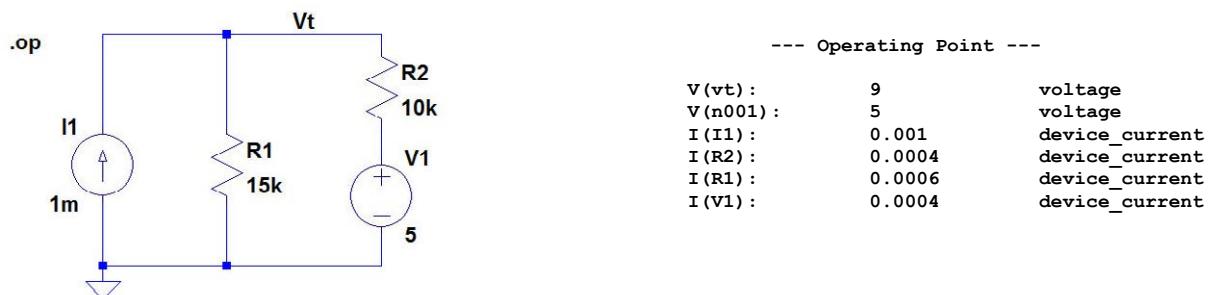


Figure P1.1

Solution:

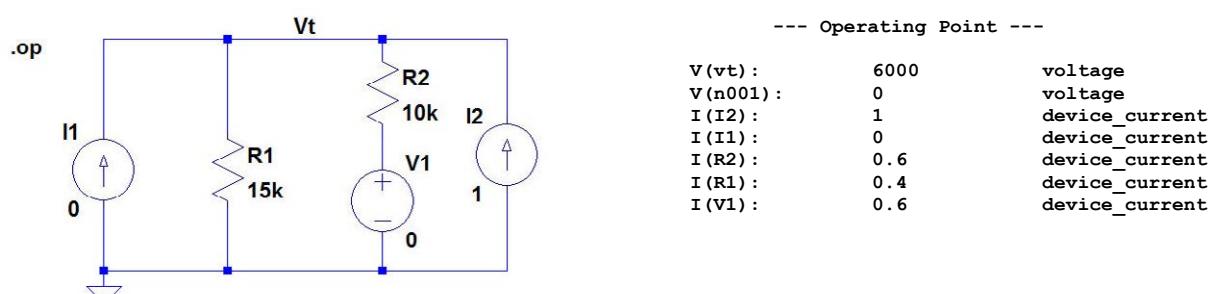
For finding the Thévenin voltage V_t , we run the ‘.op’ simulation shown below.

From the simulation output, we find $V_t = V(vt) = 9 \text{ V}$.



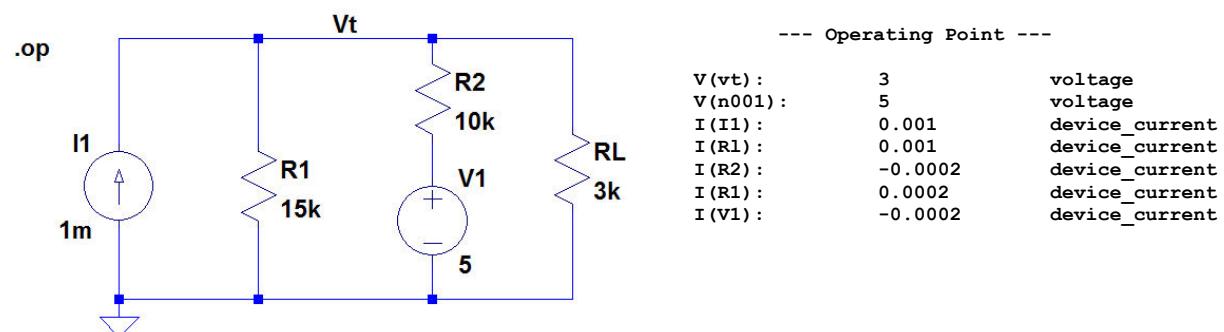
For finding the Thévenin resistance R_t , we reset the voltage source and the current source and apply a current source of 1 A between terminal a and b and find the voltage between a and b as shown below.

From the simulation output, we find $R_t = V(vt)/1 \text{ A} = 6 \text{ k}\Omega$.



For finding the power dissipated in a load resistor of $R_L = 3 \text{ k}\Omega$ connected between the terminals a and b, we run the ‘.op’ simulation shown below.

From the simulation output, we find $P = V(vt)I(RL) = 3 \text{ V} \times 0.001 \text{ A} = 3 \text{ mW}$. By moving the cursor over RL after the simulation, the dissipation can also be read directly in the status bar at the bottom of the LTspice program window.



This advertisement features a collage of professional images. It includes a man working at a computer, two women in business attire, a modern building at night, and a man holding a document. The background has abstract blue and red swooshes. At the bottom, there is a dark blue footer with the text 'www.job.oticon.dk' and the 'oticon' logo with the tagline 'PEOPLE FIRST'.

1.2

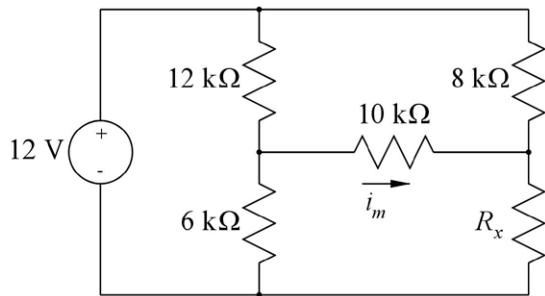
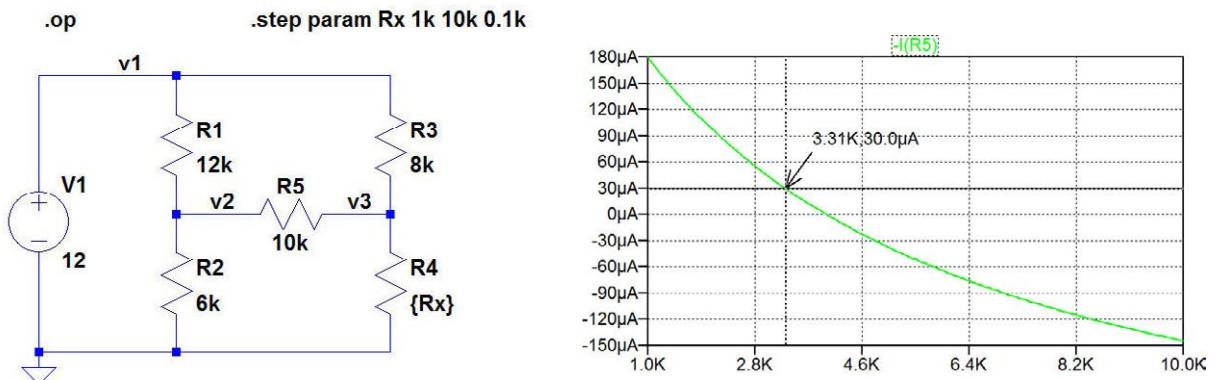


Figure P1.2

Solution:

For this circuit, we run a simulation where R_x is varied over a suitable range, and we plot i_m versus R_x . In the schematic below, $i_m = -I(R_5)$ because R_5 is inserted with just one rotation of the resistor symbol, causing the positive direction of current flow in R_5 to be from right to left. From the simulation plot, we find that $R_x = 3.31 \text{ k}\Omega$ results in $i_m = 30 \mu\text{A}$.



1.3

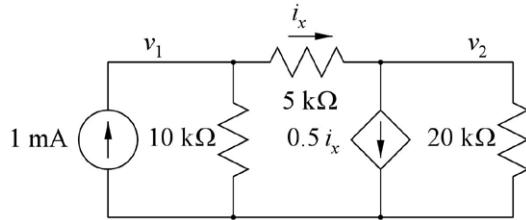
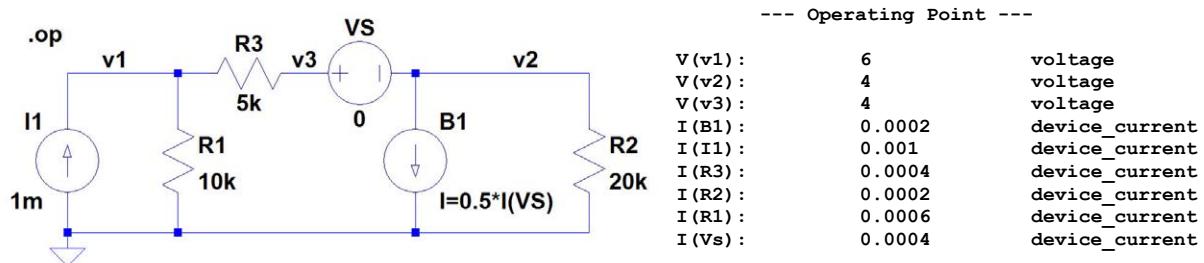


Figure P1.3

Solution:

For this circuit, we need a current controlled current source. This can be achieved using the arbitrary controlled current source as shown below. The voltage source VS is inserted because the controlling current must be the current through a voltage source. The current i_x is the current through VS.

From the output file, we find $v_1 = 6$ V, $v_2 = 4$ V and $i_x = I(VS) = 0.4$ mA.



1.4

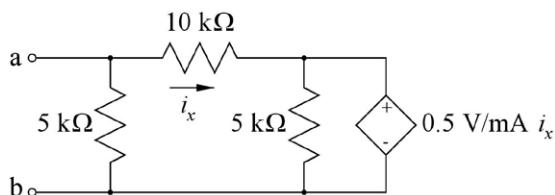
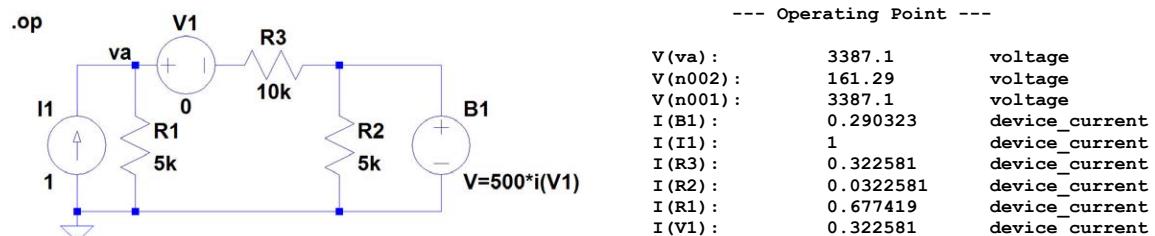


Figure P1.4

Solution:

For this circuit, we need a current controlled voltage source. This can be achieved using the arbitrary controlled voltage source as shown below. The voltage source V_1 is inserted because the controlling current must be the current through a voltage source. Additionally, a current source of 1 A is connected between terminals a and b, and the equivalent resistance is found as the voltage between a and b divided by 1 A. From the output file, we find $R_{ab} = V(va)/1 \text{ A} = 3.387 \text{ k}\Omega$.



In the past four years we have drilled

81,000 km

That's more than **twice** around the world.

Who are we?
We are the world's leading oilfield services company. Working globally—often in remote and challenging locations—we invent, design, engineer, manufacture, apply, and maintain technology to help customers find and produce oil and gas safely.

Who are we looking for?
We offer countless opportunities in the following domains:

- Engineering, Research, and Operations
- Geoscience and Petrotechnical
- Commercial and Business

If you are a self-motivated graduate looking for a dynamic career, apply to join our team.

careers.slb.com

What will you be?

Schlumberger

1.5

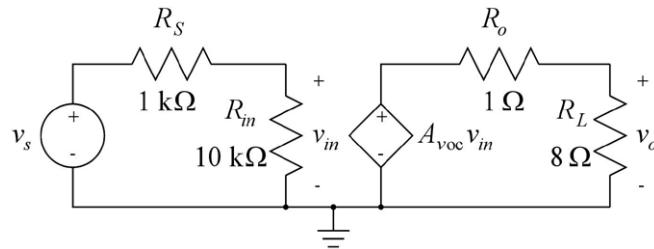


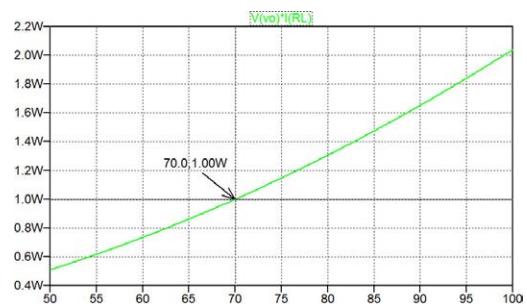
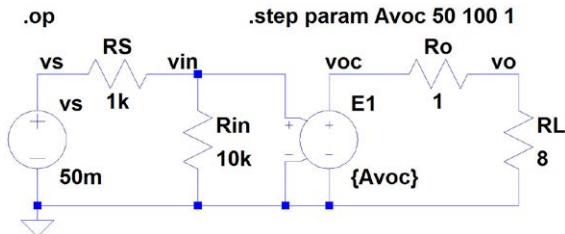
Figure P1.5

For the circuit shown in Fig. P1.5, find the value of the gain A_{voc} which gives an output power in R_L of 1 W when the signal voltage v_s is 50 mV. With this value of A_{voc} , plot the output power versus the signal voltage v_s for v_s in the range from 0 mV to 100 mV.

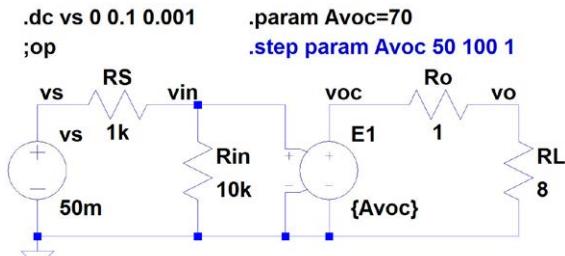
Also plot the output power versus the input voltage v_{in} for v_s in the range from 0 mV to 100 mV.

Solution:

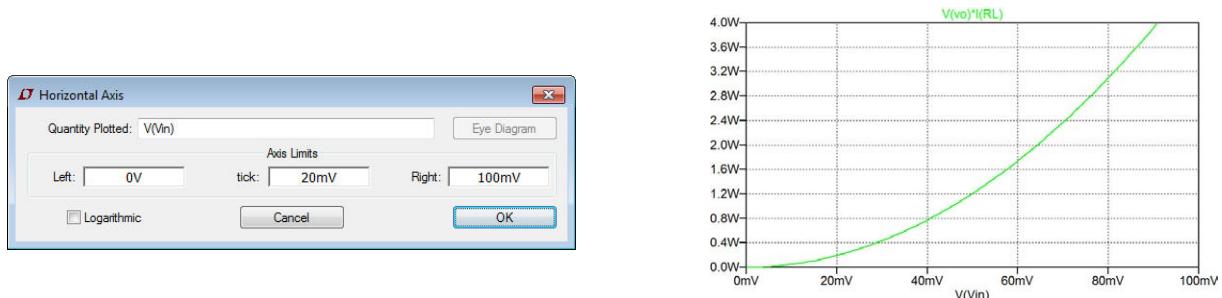
For this circuit, we define A_{voc} as a parameter and step it over a suitable range when running a ‘.op’ simulation. From a plot of $V(v_o)*I(R_L)$, we find that $A_{voc} = 70$ V/V results in a power of 1 W in R_L , see simulation below.



For simulating the output power versus the input voltage, we run a ‘.dc’ simulation with the parameter A_{voc} set to 70, see simulation below, showing the output power versus v_s .



For showing the output power versus v_{in} , we move the cursor in the plot window to the x-axis and apply a right-click on the mouse. This opens a specification window for the x-axis as shown below where we can change the ‘Quantity Plotted’ from V_s to $V(v_{in})$, resulting in a plot of the output power versus v_{in} .



**INDEPENDENT MINDED
LIKE YOU**

We believe in equality, sustainability and a modern approach to learning. How about you?
Apply for a Master's Programme in Gothenburg, Sweden.

PS. Scholarships available for Indian students!

www.gu.se/education

1.6

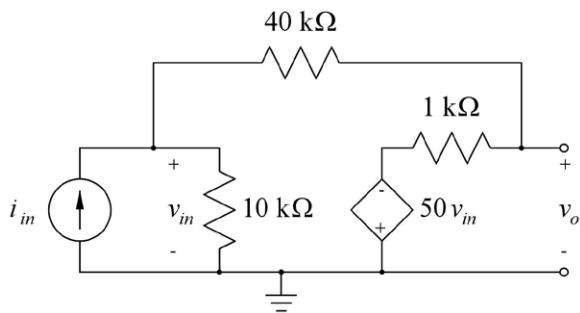


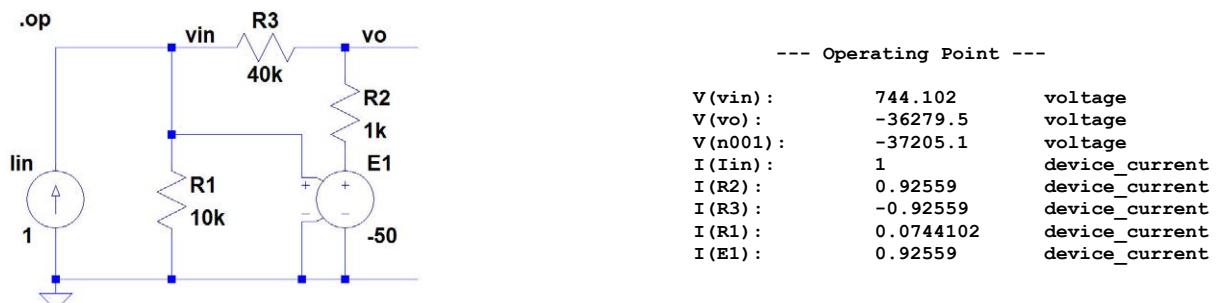
Figure P1.6

The circuit shown in Fig. P1.6 is a transresistance amplifier built from an inverting voltage amplifier with an input resistance of $10\text{ k}\Omega$, an output resistance of $1\text{ k}\Omega$ and an open circuit voltage gain of -50 V/V and a feedback resistor with a value of $40\text{ k}\Omega$. Find the open circuit transresistance R_{moc} , the input resistance R_{in} and the output resistance R_o of the resulting transresistance amplifier.

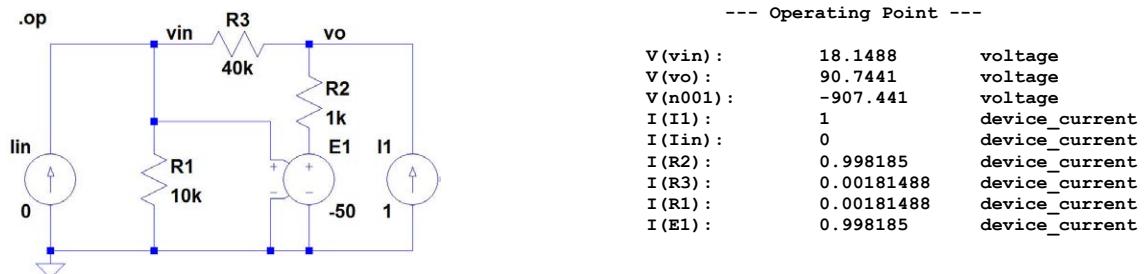
Solution:

For finding the open circuit transresistance R_{moc} and the input resistance R_{in} , we run a ‘.op’ simulation with an input current signal source of 1 A, see below. The input resistance is found as $v_{in}/i_{in} = V(v_{in})/1\text{ A}$, and the transresistance is found as $v_o/i_{in} = V(v_o)/1\text{ A}$.

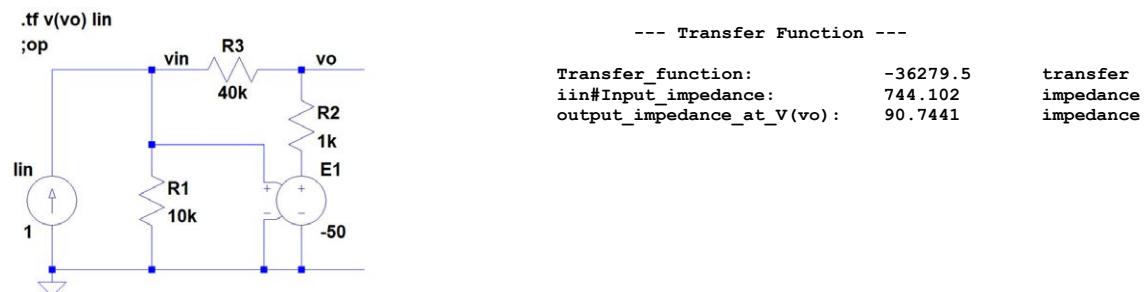
From the output file, we find $R_{moc} = V(v_o)/1\text{ A} = -36.28\text{ k}\Omega$ and $R_{in} = V(v_{in})/1\text{ A} = 744\text{ }\Omega$.



For finding the output resistance R_o , we run a ‘.op’ simulation with a current source of 1 A connected to the output and with the input current source reset. The output resistance is found as $V(v_0)/1 \text{ A}$. From the output file, we find $R_o = V(v_0)/1 \text{ A} = 90.7 \Omega$.



An alternative simulation giving both input resistance, output resistance and transresistance in just one simulation is the ‘.tf’ simulation shown below.



Linköping University – innovative, highly ranked, European

Interested in Engineering and its various branches? Kick-start your career with an English-taught master's degree.

→ Click here!

LINKÖPING
UNIVERSITY

<div style="position: absolute; bottom: 0; left: 45%; width:

1.7

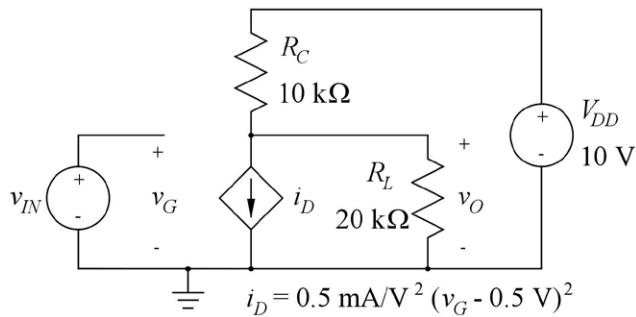


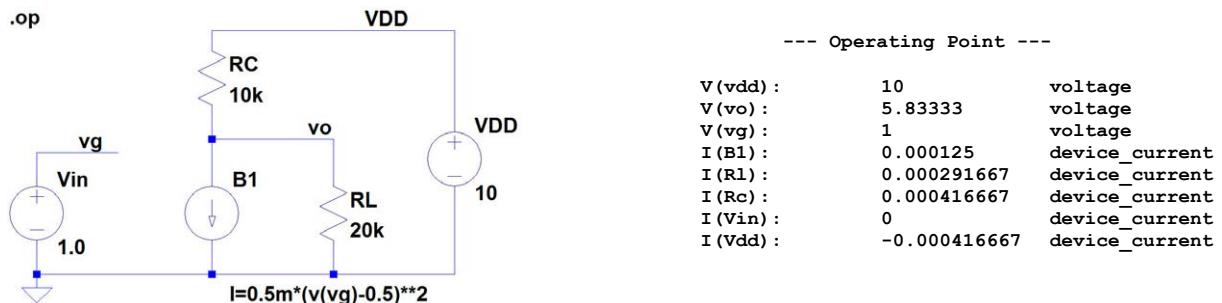
Figure P1.7

Figure P1.7 shows a nonlinear transconductance amplifier. Find the values of bias voltages and currents for an input bias voltage (quiescent voltage) of $V_{IN} = 1.0$ V. Plot the output voltage v_O for the input voltage in the range from 0.5 V to 1.8 V. Find the small-signal voltage gain v_o/v_{in} for an input bias voltage of $V_{IN} = 1.0$ V and plot the small-signal voltage gain as a function of the input bias voltage for the input bias voltage in the range from 0.5 V to 1.8 V.

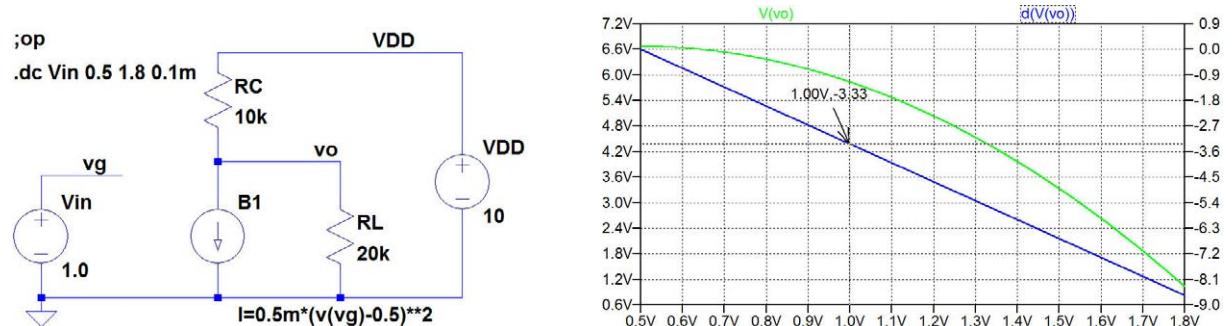
Solution:

For finding the bias voltages and currents, we run a ‘.op’ simulation as shown below.

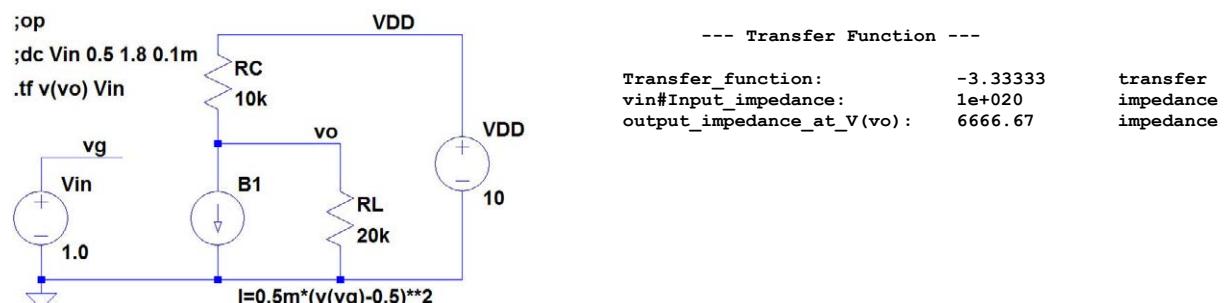
From the output file, we find $I_D = I(B1) = 0.125$ mA, $I_C = I(R_c) = 0.417$ mA, $I_L = I(R_L) = 0.292$ mA and $V_O = V(v_o) = 5.83$ V.



For plotting the output voltage and the small-signal voltage gain versus input bias voltage, we run a ‘.dc’ simulation as shown below. The voltage gain is shown as the derivative of the output voltage, $d(V(vo))$.



The small-signal gain for $V_{IN} = 1.0$ V may be found from the plot above, or it may be found from a ‘.tf’ simulation as shown below. From this, we find a small-signal gain of -3.33 V/V.



1.8

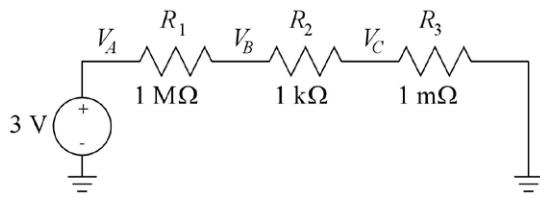


Figure P1.8

Figure P1.8 shows a series connection of three resistors and a voltage source. Try three different ways of drawing the schematic:

(1): Insert the components and draw the connections between them.

(2): Insert the components (including the ground symbols) and draw an unbroken wire (hotkey ‘F3’) from the leftmost ground symbol across the components to the rightmost ground symbol.

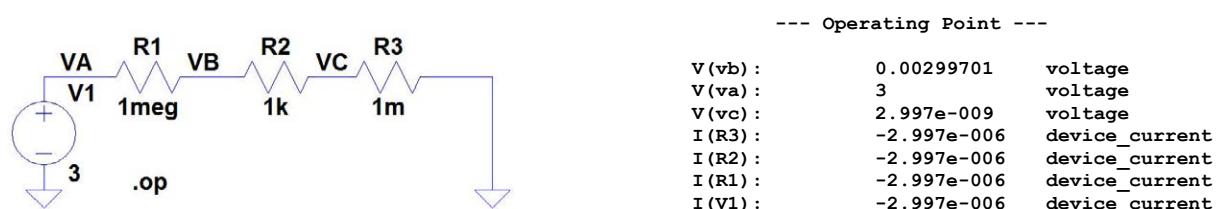
(3): Insert the ground symbols, draw an unbroken wire between them, and then insert the component directly on top of the wire.

Observe how LTspice ‘cleans up’ the wiring.

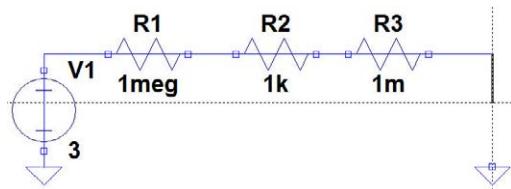
Find the voltages V_A , V_B and V_C .

Solution:

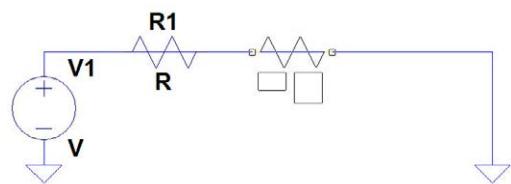
(1) The figure below shows the resulting schematic and the output file for a ‘.op’ simulation. From the output file, we find $V_A = 3.0000 \text{ V}$, $V_B = 2.997 \text{ mV}$ and $V_C = 2.997 \text{ nV}$.



(2) When inserting the components and drawing a wire across the components, the wire appears across the components during the insertion process as shown in the figure below, but when the insertion is completed, the wiring is cleaned up, resulting in the schematic shown above.



(3) When inserting an unbroken wire first and the components afterwards on top of the wire, the cleaning up takes place when completing the insertion. The figure below shows the schematic when the voltage source insertion has been completed and the resistor insertion is in progress.



STUDY FOR YOUR MASTER'S DEGREE IN THE CRADLE OF SWEDISH ENGINEERING

Chalmers University of Technology conducts research and education in engineering and natural sciences, architecture, technology-related mathematical sciences and nautical sciences. Behind all that Chalmers accomplishes, the aim persists for contributing to a sustainable future – both nationally and globally.

Visit us on **Chalmers.se** or **Next Stop Chalmers** on facebook.



1.9

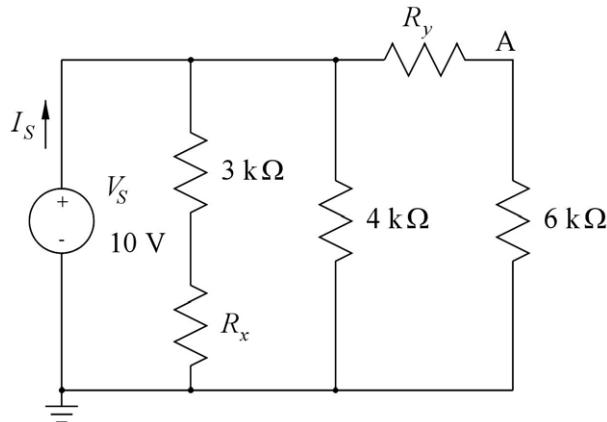
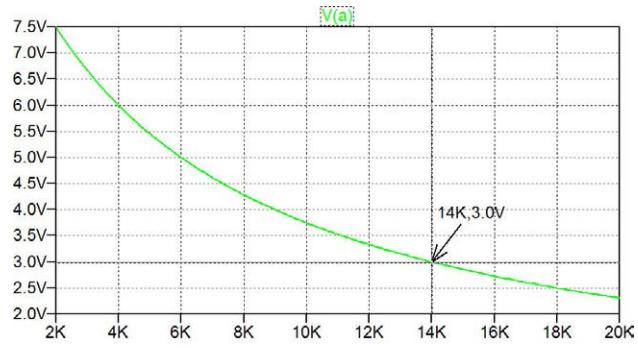
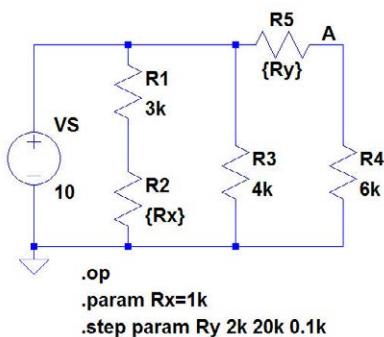


Figure P1.9 shows a simple resistive circuit with five resistors where only three of the resistor values are known. However, the voltage of node A is $V_A = 3$ V, and the current I_S supplied by the dc voltage source V_S is $I_S = 4.25$ mA. Use LTspice to find the values of the two resistors R_x and R_y .

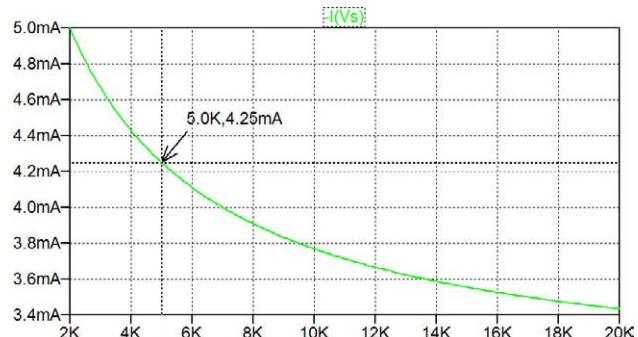
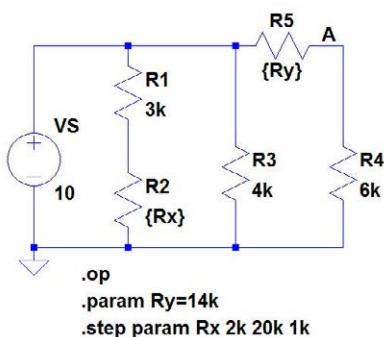
Figure P1.9

Solution:

The figure below shows the LTspice schematic for the circuit with the unknown resistors values R_x and R_y defined as parameters. When inspecting the schematic, we notice that the current I_S depends both on R_x and R_y whereas V_A depends only on R_y . Thus, we can select an arbitrary value for R_x and step R_y through a suitable range of values in a ‘.op’ simulation. In the figure below, R_x is selected to $1\text{ k}\Omega$ and R_y is varied from $1\text{ k}\Omega$ to $20\text{ k}\Omega$ in steps of $0.1\text{ k}\Omega$, and from the ‘.op’ simulation, V_A is shown versus R_y . From the plot, we find that $R_y = 14\text{ k}\Omega$ results in $V_A = 3$ V.



Next, we define R_y to be $14\text{ k}\Omega$ and step R_x from $1\text{ k}\Omega$ to $20\text{ k}\Omega$ in steps of $0.1\text{ k}\Omega$, and from the ‘.op’ simulation, we plot $I_S = -I(V_S)$ versus R_x . We see that $R_x = 5\text{ k}\Omega$ results in $I_S = 4.25$ mA.



Tutorial 2 – Circuits with Capacitors and Inductors

2.1

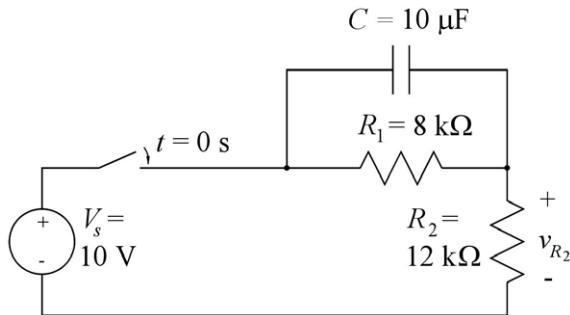
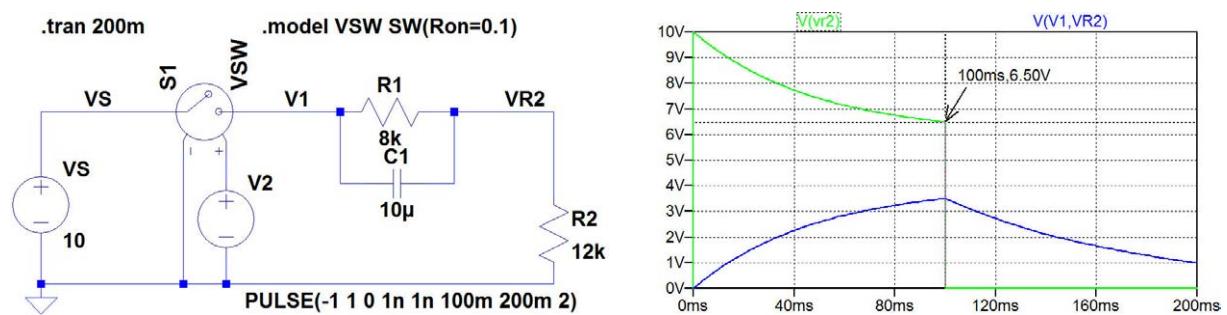


Figure P2.1

For the circuit shown in Fig. P2.1, assume that the switch is closed at time $t = 0$ and re-opened at time $t = 100$ ms. Find the value of the voltage v_{R_2} immediately after the switch is closed. Find the value of v_{R_2} immediately before the switch is re-opened. Find the value of v_{R_2} immediately after the switch is re-opened. Plot v_{R_2} versus time for $0 \leq t \leq 200$ ms. Plot the capacitor voltage versus time and find the time constants for the charging and discharging of the capacitor C .

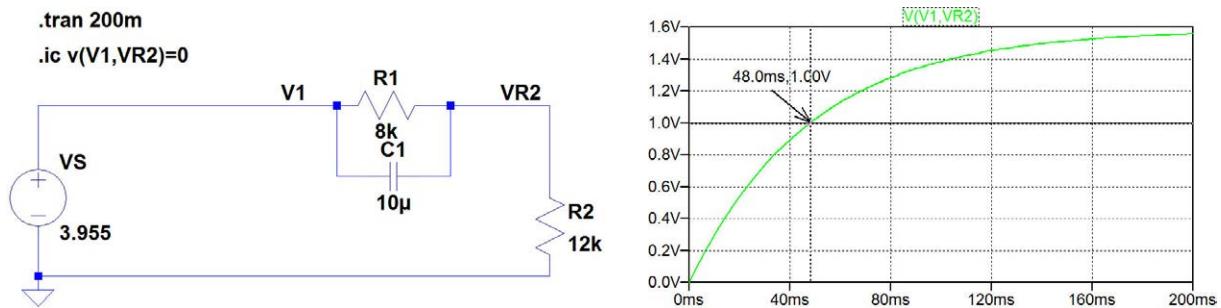
Solution:

The figure below shows the circuit with a voltage controlled switch, controlled by a voltage V_2 specified as a time varying voltage. For the specification, we use a ‘PULSE’ waveform with rise time and fall time of 1 ns which is much shorter than the pulse width of 100 ms. For the voltage controlled switch, a ‘.model’ specification has been inserted, changing the on-resistance from the default value of 1Ω to a value of 0.1Ω . From the figure, we find the value of v_{R_2} immediately after the switch is closed to be 10 V, and we find the value of v_{R_2} immediately before the switch is re-opened to be 6.5 V. The value of v_{R_2} immediately after the switch is re-opened is found to be 0 V.

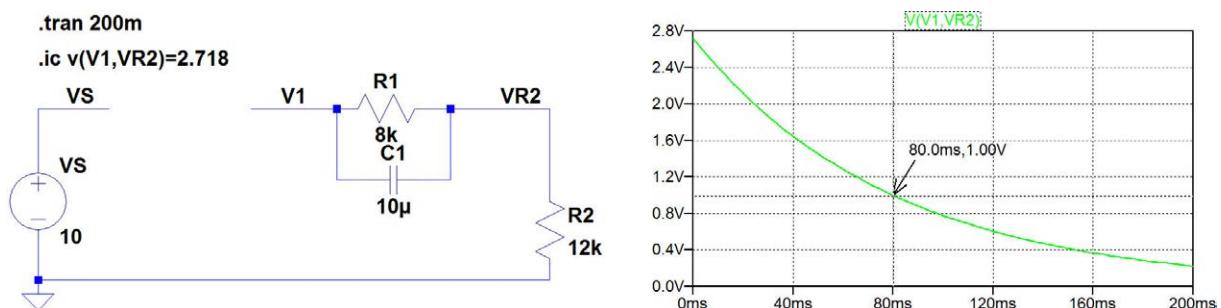


The time constants for charging and discharging of the capacitor may be evaluated from the previous simulation but an easier, alternative approach is to run transient simulations with only dc voltage sources and a specification of initial voltages for the capacitor.

The figure below shows a simulation for finding the charging time constant. As the limiting value of v_{R_2} for $t \rightarrow \infty$ is $V_S R_1 / (R_1 + R_2)$, it is convenient to select $V_S = (1 + R_2/R_1)/(1 - e^{-1}) = 3.955$ V, implying that a capacitor voltage of 1 V is reached for $t = \tau$. Also, the initial value of the capacitor voltage must be specified to 0 V. From the figure, we find $\tau = 48$ ms.



For finding the time constant for discharging with the switch open, we disconnect V_S and specify the initial value of the capacitor voltage to be $e = 2.718$ V so that the capacitor voltage reaches a value of 1 V after $t = \tau$, see figure below. From this simulation, we find $\tau = 80$ ms.



2.2

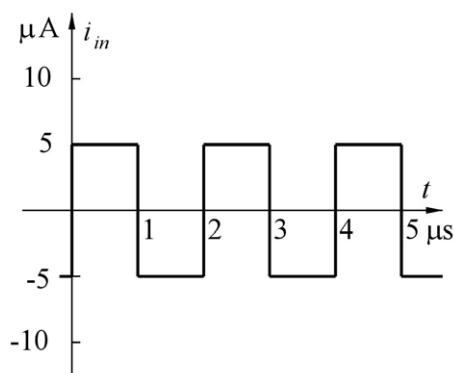
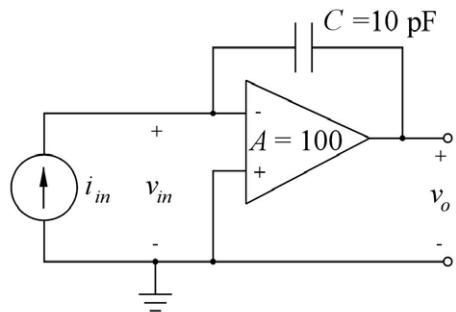
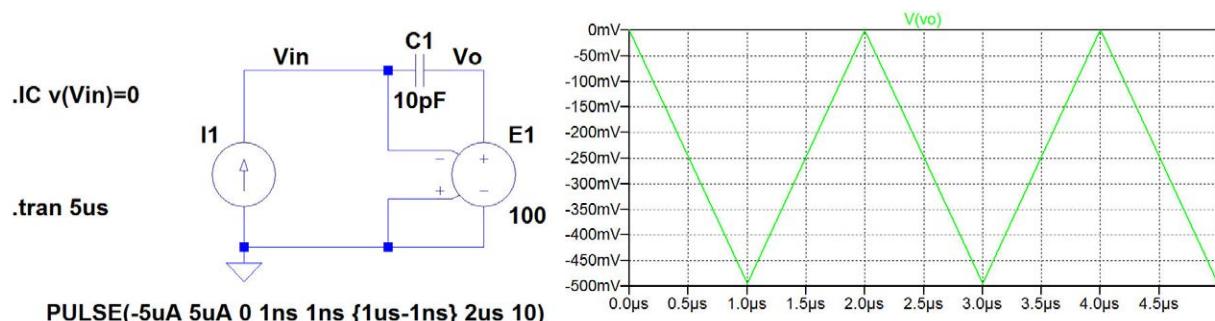


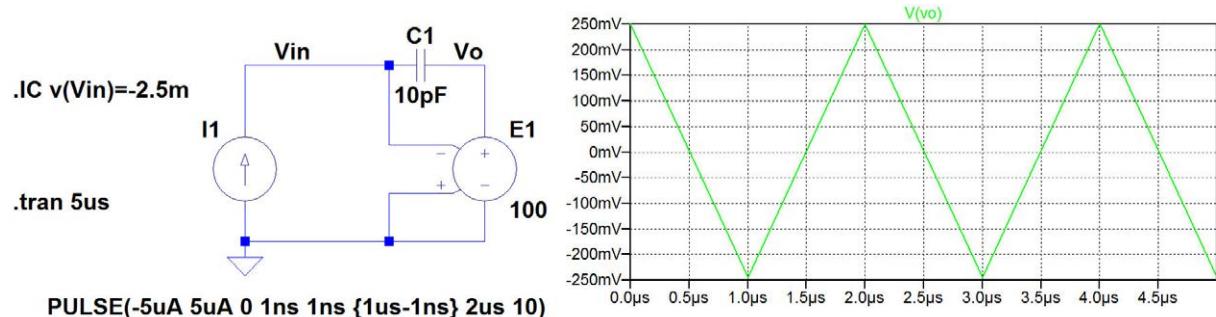
Figure P2.2

Solution:

The figure below shows the circuit with the amplifier modeled by a voltage controlled voltage source. The time varying input current is specified by a ‘PULSE’ waveform with rise time and fall time of 1 ns which is much shorter than the pulse width of 1 μ s, and with the specification shown below, the mean input current is 0. The initial value of the input voltage is set by the ‘.IC’ directive.



From the plot of the resulting output waveform, we find a mean value of -250 mV for the output voltage, so in order to obtain a mean value of 0 V for the output voltage, the initial value of the input voltage must be changed by -2.5 mV since the gain of the inverting voltage controlled voltage source is 100 . Thus, the required initial value of v_{in} is -2.5 mV as confirmed by the simulation shown below.



Striking a match, reconnecting with your family through Skype or over a phone network from Ericsson, refurbishing your apartment at IKEA or driving safely in your Volvo - none of this would be possible if not for Sweden.
Swedish universities offer over 900 international master's programmes taught entirely in English.

Don't just pick a place - pick a future.
[->studyinsweden.se](http://>studyinsweden.se)



2.3

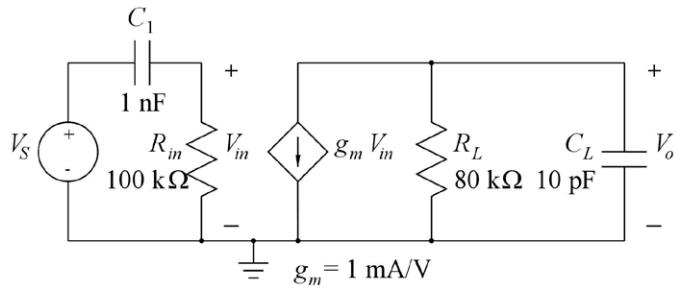
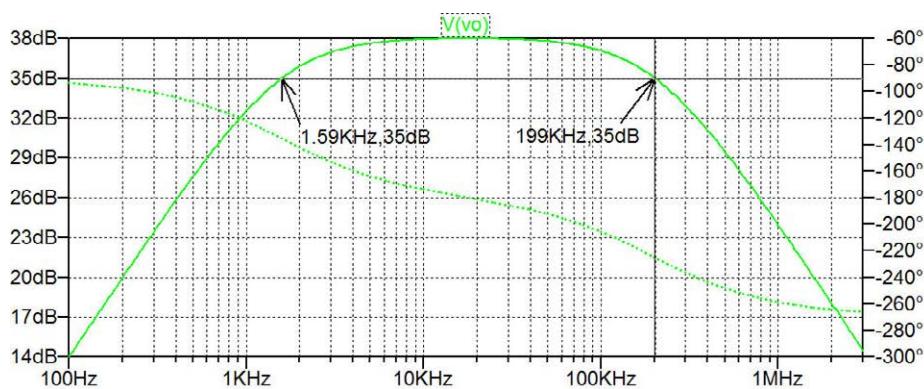
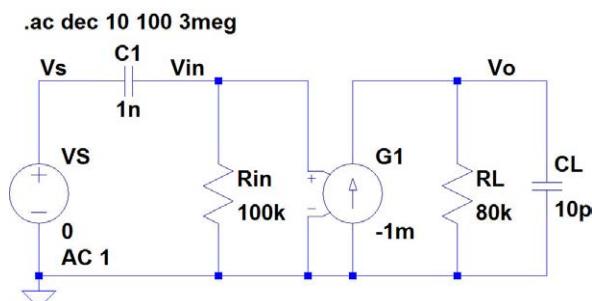


Figure P2.3

For the circuit shown in Fig. P2.3, find the midband gain, the upper and lower half-power (-3 dB) frequencies and the 3 -dB bandwidth. Plot the output voltage V_o versus frequency in a Bode plot covering a frequency range which extends from approximately one decade below the lower half-power frequency to approximately one decade above the upper half-power frequency.

Solution:

The figure below shows the circuit and the simulated Bode plot from 100 Hz to 3 MHz. From the Bode plot, we find a midband gain of 38 dB, a lower -3 dB frequency of 1.59 kHz and an upper -3 dB frequency of 199 kHz. The 3 -dB bandwidth is $199\text{ kHz} - 1.59\text{ kHz} = 197.41\text{ kHz}$.



2.4

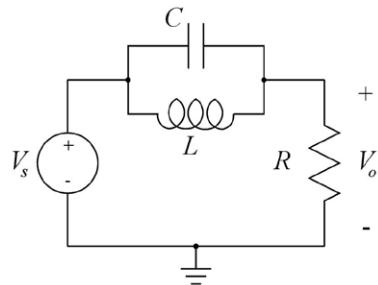


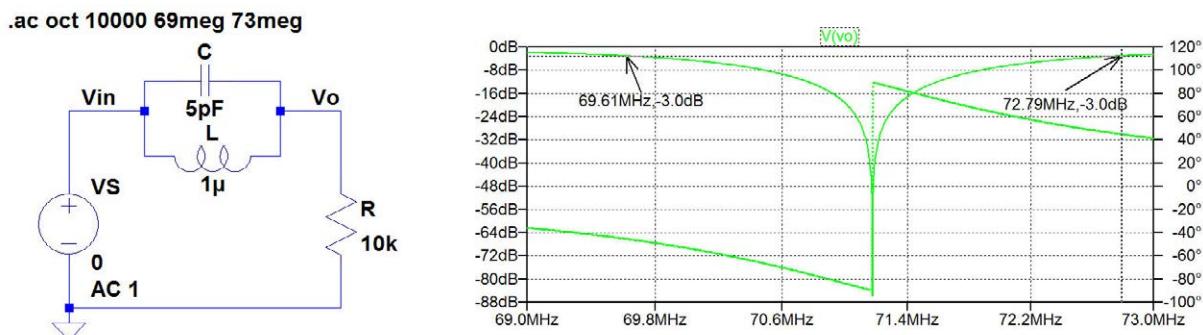
Figure P2.4

For the notch filter shown in Fig. P2.4, plot V_o versus frequency in a frequency range showing the notch and the 3-dB bandwidth. Assume $L = 1 \mu\text{H}$, $C = 5 \text{ pF}$ and $R = 10 \text{ k}\Omega$. From the plot, find the notch frequency, the bandwidth and the quality factor Q .

Solution:

The figure below shows the circuit and the simulated Bode plot from 69 MHz Hz to 73 MHz. Notice that a large number of points per octave has been specified (10000) in order to show the notch. In order to find the frequency range to plot, it may be a good idea to calculate the resonance frequency from $f_{res} = (2\pi\sqrt{LC})^{-1} = 71.18 \text{ MHz}$. From the Bode plot, we find a notch frequency of 71.2 MHz, a 3-dB bandwidth of $(72.79 - 69.61) \text{ MHz} = 3.18 \text{ MHz}$ and a quality factor $Q = 71.2/3.18 = 22.4$.

Analytically, the quality factor is calculated from $Q = R\sqrt{C/L} = 22.4$.



2.5

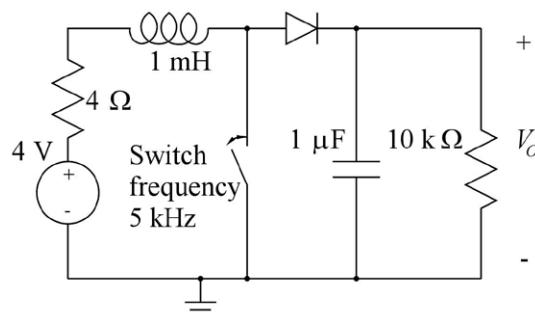


Figure P2.5

The circuit shown in Fig. P2.5 is a dc-dc converter which converts a dc voltage of 4 V into a high voltage V_O . The switch is an electronic switch which opens and closes with a frequency of 5 kHz and a duty cycle of 50%, starting at time $t = 0$. The diode can be assumed to be modeled by the default Shockley diode model. Initially, the current in the inductor is 0 and the output voltage V_O is 0. Find the dc output voltage for $t \rightarrow \infty$ and find the time required for V_O to reach 90% of the final value.

TAKE THE **RIGHT TRACK**

Give your career a head start
by studying with us. Experience the advantages
of our collaboration with major companies like
ABB, Volvo and Ericsson!

Click here
to learn more

Apply by
15 January

World class
research

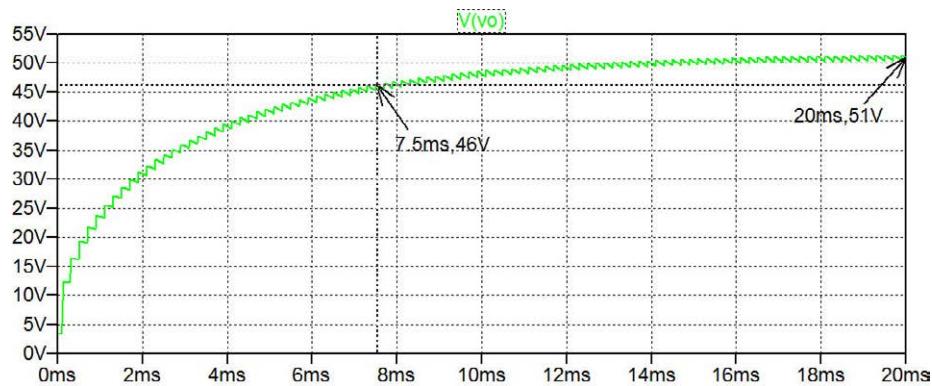
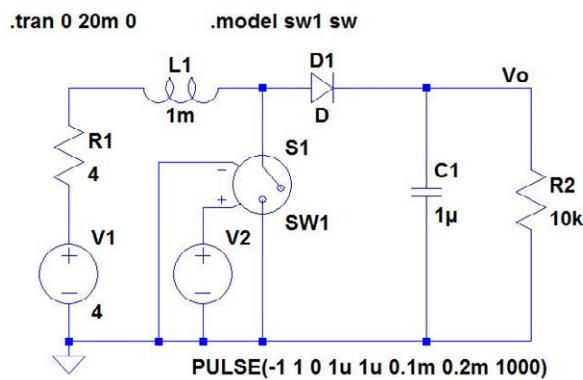
www.mdh.se

MÄLARDALEN UNIVERSITY
SWEDEN

Solution:

The figure below shows the circuit with a voltage controlled switch controlled by a voltage V_2 specified as a time varying voltage. For the specification, a ‘PULSE’ waveform with rise time and fall time much shorter than the pulse width is used. For the diode, no ‘.model’ specification is needed for the default Shockley model. For the voltage controlled switch, a ‘.model’ specification has been inserted using the default switch parameters. If you do not insert the ‘.model’ specification, the simulation will still run with the default switch model but an error message will be produced.

The figure below shows the simulated output voltage from 0 to 20 ms. From the simulation, we find an output voltage of about 51 V for $t \rightarrow \infty$ and a rise time of about 7.5 ms for reaching 90% of the final value.



2.6

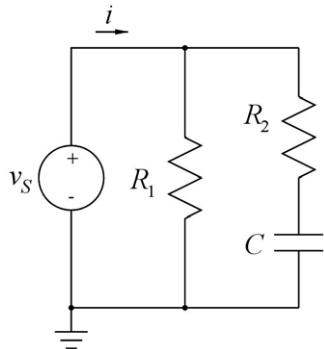


Figure P2.6

For the circuit shown in Fig. P2.6, assume that the voltage v_s is real and has an ac amplitude of 1. Derive expressions for finding R_1 , R_2 and C from a ‘.ac’ simulation over a suitable range of the frequency f , using asymptotic values for $f \rightarrow 0$ and $f \rightarrow \infty$. Verify your results by simulating the circuit with $R_1 = 300 \text{ k}\Omega$, $R_2 = 200 \text{ k}\Omega$ and $C = 2 \text{ nF}$.

Solution:

Assuming that $V_s(j\omega)$ is real, i.e. $V_s(j\omega) = V_s$, we find from Fig. P2.6:

$$\operatorname{Re}(i) + j\operatorname{Re}(i) = V_s \left(\frac{1}{R_1} + \frac{j\omega C}{1 + j\omega R_2 C} \right) = V_s \left(\frac{1}{R_1} + \frac{j\omega C(1 - j\omega R_2 C)}{1 + (\omega R_2 C)^2} \right)$$

Equating the real parts, we find:

$$\operatorname{Re}(i) = V_s \left(\frac{1}{R_1} + \frac{R_2(\omega C)^2}{1 + (\omega R_2 C)^2} \right)$$

From this expression, we find that for $\omega \rightarrow 0$, $\operatorname{Re}(i) \rightarrow V_s/R_1$, so R_1 can be found from a plot of $V_s/\operatorname{Re}(i) = -1/\operatorname{Re}(I(V_s))$ for $f \rightarrow 0$ and an ac amplitude of 1 for V_s .

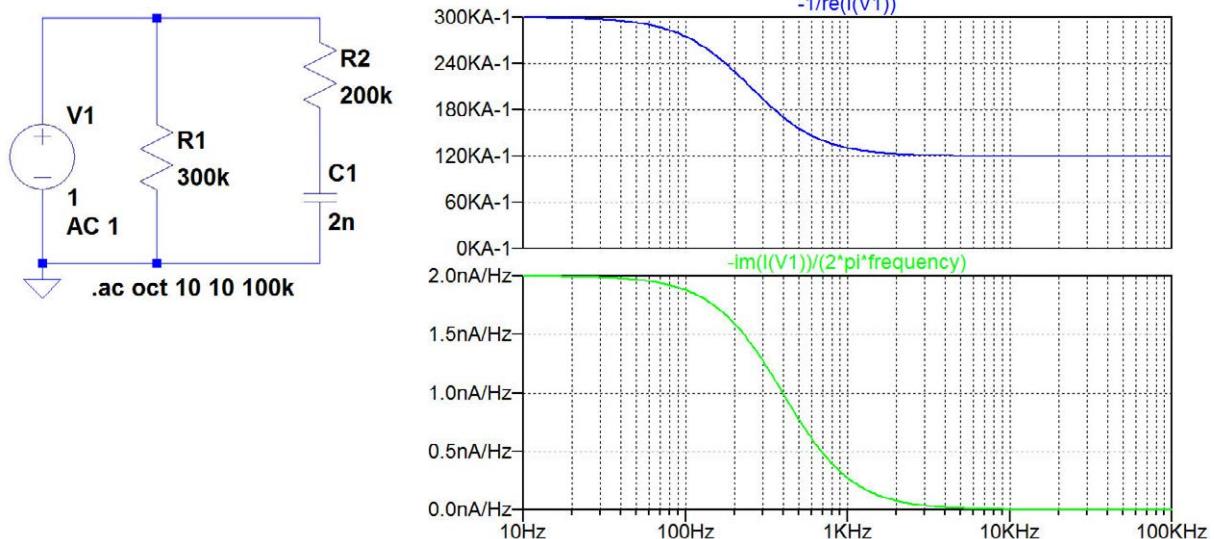
Also from this expression, we find that for $\omega \rightarrow \infty$, $\operatorname{Re}(i) \rightarrow V_s(1/R_1 + 1/R_2)$, so from a plot of $V_s/\operatorname{Re}(i) = -1/\operatorname{Re}(I(V_s))$ for $f \rightarrow \infty$, we find $R_{\text{eq}} = R_1 \parallel R_2$, and R_2 can be found from $R_2 = R_1 R_{\text{eq}} / (R_1 - R_{\text{eq}})$.

Equating the imaginary parts, we find:

$$\operatorname{Im}(i) = V_s \left(\frac{\omega C}{1 + (\omega R_2 C)^2} \right)$$

From this expression, we find that for $\omega \rightarrow 0$, $\operatorname{Im}(i) \rightarrow V_s \omega C$, so C can be found from a plot of $\operatorname{Im}(i)/(\omega V_s) = -\operatorname{Im}(I(V_s))/(2\pi f)$ for $f \rightarrow 0$ and an ac amplitude of 1 for V_s .

The LTspice schematic for the circuit is shown below with the specified values of R_1 , R_2 and C , and also the plots for finding R_1 , R_2 and C are shown (using linear y-axes). From the plots, we verify $C = 2 \text{ nF}$, $R_1 = 300 \text{ k}\Omega$ and $R_{\text{eq}} = 120 \text{ k}\Omega \Rightarrow R_2 = 120 \times 300 \text{ k}\Omega / (300 - 120) = 200 \text{ k}\Omega$.



ADVANCE YOUR CAREER IN UMEÅ!

- modern campus • world class research • 32 000 students
- top class teachers • ranked nr 1 in Sweden by international students

Master's programmes:

- Architecture • Industrial Design • Science • Engineering





UMEÅ
UNIVERSITY

Download
brochure
here!

UMEÅ UNIVERSITY
FACULTY OF SCIENCE & TECHNOLOGY

2.7

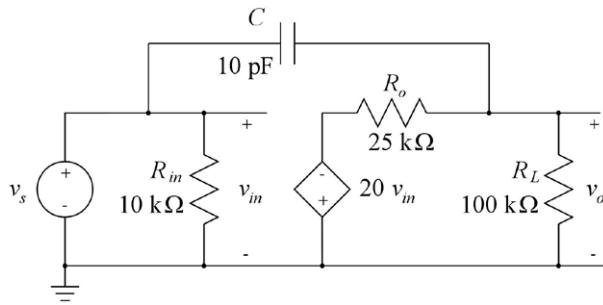


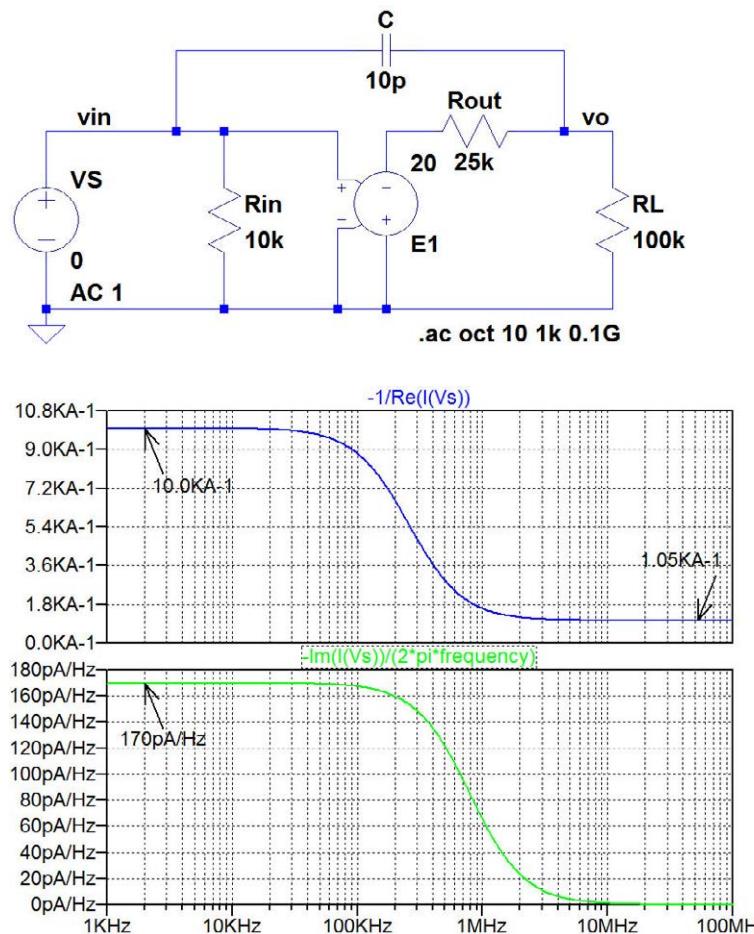
Figure P2.7

Figure P2.7 shows an inverting amplifier similar to the amplifier from Fig. 2.27 on page 69 but with a finite output resistance $R_o = 25\text{ k}\Omega$ for the controlled voltage source. Assuming that the input impedance has a topology as shown in Fig. P2.6, find the values of R_1 , R_2 and C in the input impedance.

Solution:

Applying the results from Problem 2.6, we use a ‘.ac’ simulation for finding the equivalent input impedance. Assuming $Z_{in} = R_1 \parallel (R_2 + 1/(j\omega C))$, we find C from a plot of $-\text{Im}(I(V_s))/(2\pi\text{frequency})$ for $f \rightarrow 0$ with an ac amplitude of 1 for V_s . From a plot of $-1/\text{Re}(I(V_s))$ (with an amplitude of 1 for V_s), we find R_1 for $f \rightarrow 0$ and $R_{eq} = R_1 \parallel R_2$ for $f \rightarrow \infty$.

The LTspice schematic and the plots are shown below. From the plots, we find $C = 170\text{ pF}$, $R_1 = 10\text{ k}\Omega$ and $R_{eq} = 1.05\text{ k}\Omega \Rightarrow R_2 = 1.05 \times 10\text{ k}\Omega / (10 - 1.05) = 1.17\text{ k}\Omega$.



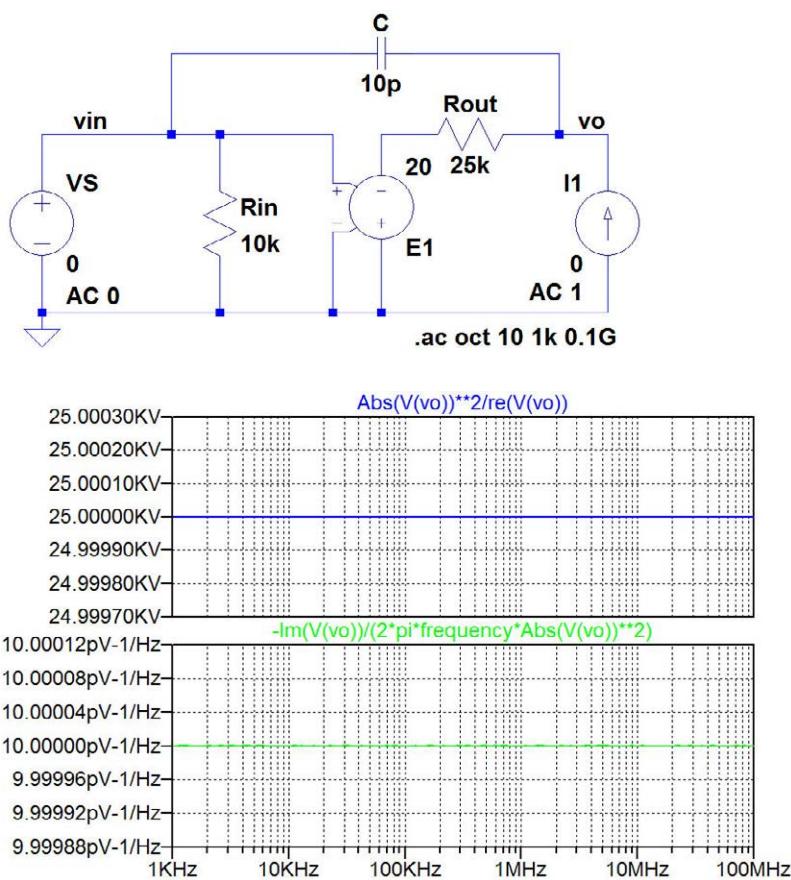
2.8

For the amplifier shown in Fig. P2.7, use a ‘.ac’ simulation to find the output impedance by resetting the input voltage and replacing the load resistor R_L with an ac voltage source. Assume that the output impedance is a parallel connection of a resistor and a capacitor.

Solution:

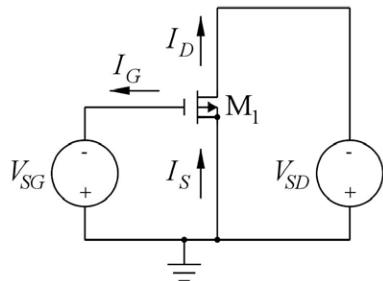
In order to find the output impedance, we run the ‘.ac’ simulation shown in the LTspice schematic below. With the output impedance being a parallel connection of a resistor R_o and a capacitor C_o , the resistor is found from ‘ $\text{Abs}(V(vo))^{**2}/\text{Re}(V(vo))$ ’, compare equation (2.15) on page 65, and the capacitor is found from ‘ $-\text{Im}(V(vo))/(2*\pi*\text{frequency}*\text{Abs}(V(vo))^{**2})$ ’, compare equation (2.16) on page 66 in ‘CMOS Integrated Circuit Simulation with LTspice’.

From the simulation, we find $R_o = 25 \text{ k}\Omega$ and $C_o = 10 \text{ pF}$.



Tutorial 3 – MOS Transistors

3.1



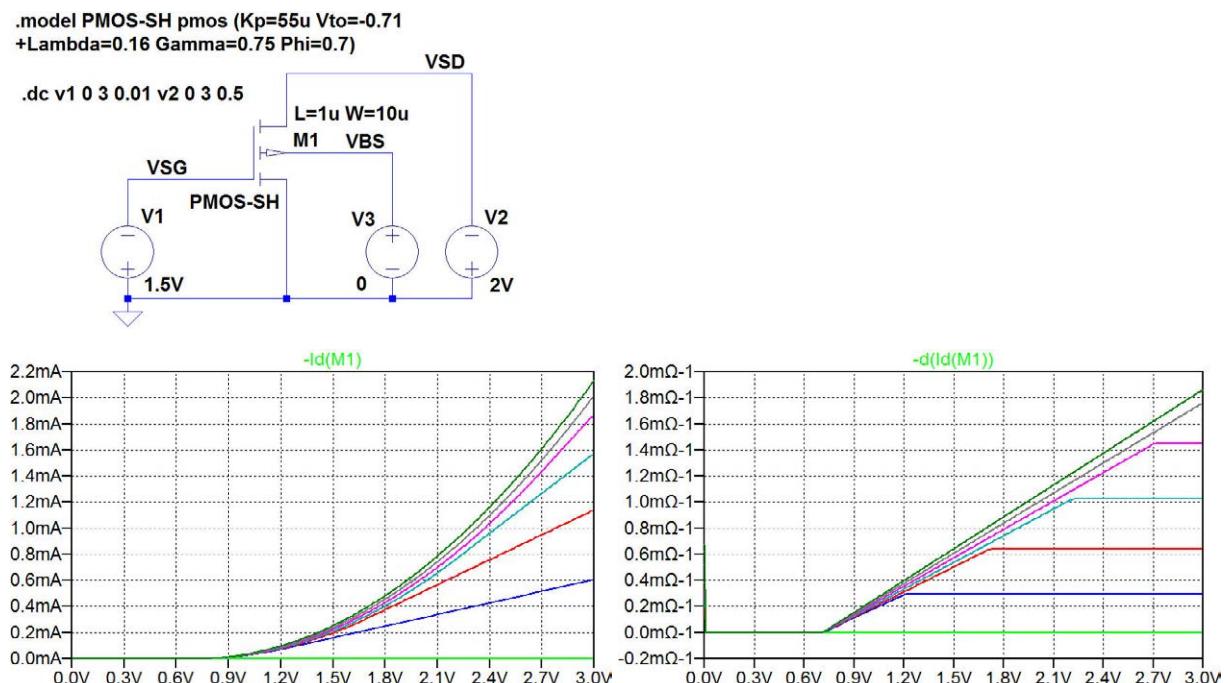
$$\begin{aligned} W &= 10 \mu\text{m}, L = 1 \mu\text{m}, \\ K_p &= 55 \mu\text{A/V}^2, V_{to} = -0.71 \text{ V}, \lambda = 0.16 \text{ V}^{-1}, \\ \gamma &= 0.75 \sqrt{\text{V}}, |2\Phi_F| = 0.7 \text{ V}. \end{aligned}$$

For the PMOS transistor shown in Fig. P3.1, simulate and plot the input characteristics I_D versus V_{SG} and $\partial i_D / \partial v_{SG}$ for $V_{SD} = 0, 0.5, 1.0, 1.5, 2.0, 2.5$ and 3.0 V. Use the model parameters and transistor dimensions shown in the figure. Find the bias current I_D and the small-signal parameters g_m , g_{mb} and g_{ds} for the bias point of $V_{SG} = 1.5$ V and $V_{SD} = 2.0$ V.

Figure P3.1

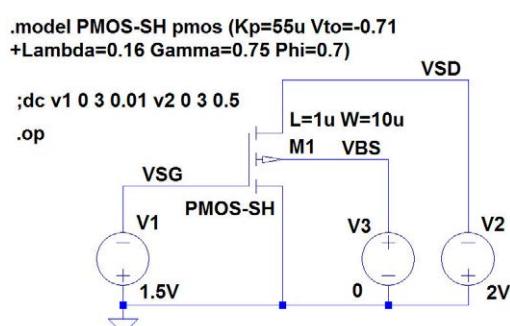
Solution:

The figure below shows the schematic for simulating the input characteristics. Also shown are the resulting plots of I_D versus V_{SG} and $\partial i_D / \partial v_{SG}$ (or g_m) for $V_{SD} = 0$ V (green curves), 0.5 V (blue curves), 1.0 V (red curves), 1.5 V (cyan curves), 2.0 V (purple curves), 2.5 V (grey curves) and 3.0 V (dark green curves). You may notice that when the transistor is in the triode region ($|V_{DS}| < |V_{GS}| - |V_t|$), g_m is independent of V_{SG} , see equation (3.11) in ‘CMOS Integrated Circuit Simulation with LTspice’.



For finding the bias current and the small-signal parameters for a bias point of $V_{SG} = 1.5$ V and $V_{SD} = 2.0$ V, we run a ‘.op’ simulation. The bias values and the small-signal parameters are given in the error log file (‘Ctrl-L’) from this simulation, see below where the requested parameters are underlined.

Notice that in LTspice, the drain current is defined positive into the transistor, whereas in Fig. P3.1, it is defined positive out of the transistor.



Semiconductor Device Operating Points:	
--- MOSFET Transistors ---	
Name:	m1
Model:	pmos-sh
<u>Id:</u>	<u>-2.27e-04</u>
Vgs:	-1.50e+00
Vds:	-2.00e+00
Vbs:	0.00e+00
Vth:	-7.10e-01
Vdsat:	-7.90e-01
Gm:	5.74e-04
Gds:	2.75e-05
Gmb:	2.57e-04

We ask you
**WHERE DO YOU
WANT TO BE?**

TOMTOM

TomTom is a place for people who see solutions when faced with problems, who have the energy to drive our technology, innovation, growth along with goal achievement. We make it easy for people to make smarter decisions to keep moving towards their goals. If you share our passion - this could be the place for you.

Founded in 1991 and headquartered in Amsterdam, we have 3,600 employees worldwide and sell our products in over 35 countries.

For further information, please visit tomtom.jobs

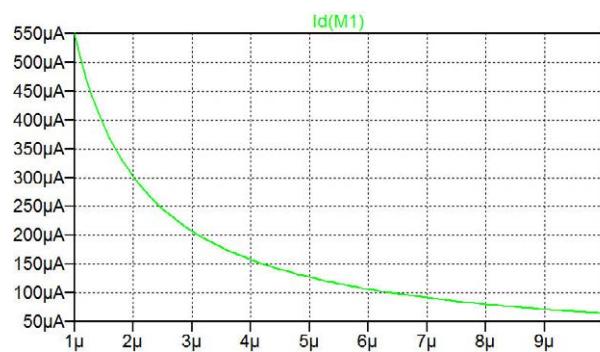
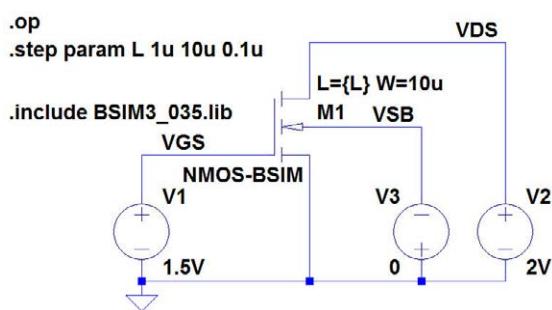
3.2

```
.MODEL NMOS-BSIM NMOS LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 7.8E-9
+XJ = 1E-07 NCH = 2.18E+17 VTH0 = 0.48
+K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01
+K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01
+U0 = 360 UA = -8.48E-10 UB = 2.27E-18
+UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00
+AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06
+KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01
+RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02
+WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10
+DWG = -4.27E-09
+DWB = 4.07E-09 VOFF = -4.14E-02 NFACCTOR = 1.61E+00
+CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00
+CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01
+DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04
+PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-02
+PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02
+DELT = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.11E-01
+KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09
+UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04
+WL = 0 WLN = 9.95E-01 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12
+CJ = 9e-4 PB = 7.95E-01 MJ = 3.53E-01
+CJSW = 2.8e-10 PBSW = 7.98E-01 MJSW = 1.73E-01
+CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01
+CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01
+PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03
```

Figure P3.2

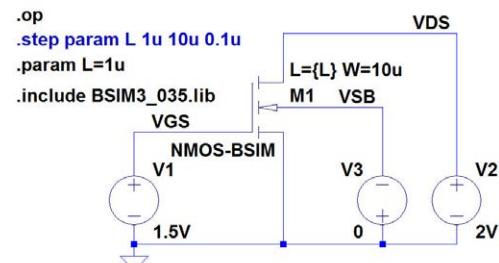
Solution:

The figure below shows the schematic for simulating the drain current. The channel length L is defined as a parameter which is stepped from 1 μm to 10 μm . The transistor model is included in a separate model file, ‘BSIM3_035.lib’. The drain current is found from a ‘.op’ simulation.



For finding the bias current I_D and the small-signal parameters g_m , g_{mb} and g_{ds} for $L = 1 \mu\text{m}$ and for $L = 5 \mu\text{m}$ in the bias point of $V_{GS} = 1.5 \text{ V}$, $V_{DS} = 2.0 \text{ V}$ and $V_{SB} = 0 \text{ V}$, we specify the value of L using a ‘.param’ directive with the ‘.step param’ directive changed into a comment, see the figure on the following page with $L = 1 \mu\text{m}$.

The bias point information is given in the error log file from a ‘.op’ simulation. The error log files for $L = 1 \mu\text{m}$ and $L = 5 \mu\text{m}$ are shown below with an underlining of the requested parameters. We notice that with the BSIM transistor model, neither the bias current, nor the transconductances (g_m and g_{mb}) scale by a factor of 5 as predicted by the Shichman-Hodges model.



L= $1\text{e-}6$:

Semiconductor Device Operating Points:	
--- BSIM3 MOSFETs ---	
Name:	m1
Model:	nmos-bsim
<u>Id:</u>	<u>5.48e-04</u>
Vgs:	1.50e+00
Vds:	2.00e+00
Vbs:	0.00e+00
Vth:	5.43e-01
Vdsat:	6.21e-01
Gm:	9.92e-04
Gds:	1.03e-05
Gmb:	2.63e-04

I= $5\text{e-}6$:

Semiconductor Device Operating Points:	
--- BSIM3 MOSFETs ---	
Name:	m1
Model:	nmos-bsim
<u>Id:</u>	<u>1.27e-04</u>
Vgs:	1.50e+00
Vds:	2.00e+00
Vbs:	0.00e+00
Vth:	5.10e-01
Vdsat:	7.45e-01
Gm:	2.45e-04
Gds:	1.94e-06
Gmb:	6.53e-05

INNOVATIVE LIKE YOU.

If you’re hoping for a truly modern education, one where you’re encouraged to speak your mind and to think long-term, both when it comes to your own future and the future of the planet. Then the University of Gothenburg is the place for you.

Study a Master’s programme in Gothenburg, Sweden | www.gu.se/education



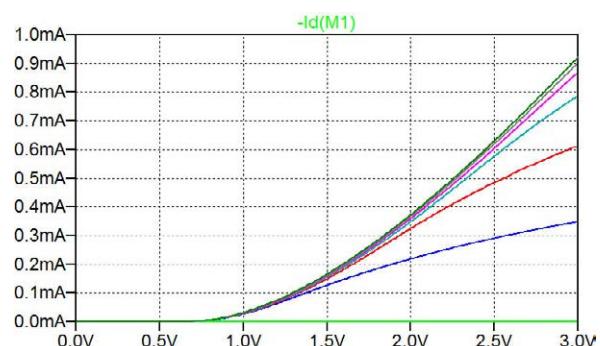
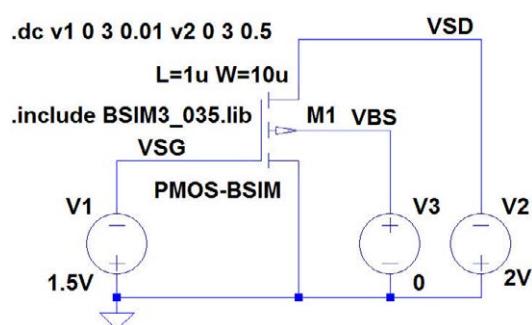
3.3

```
.MODEL PMOS-BSIM PMOS LEVEL = 49
+VERSION = 3.1 TNOM = 2.69E+01 TOX = 7.8E-9
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = -0.6
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0T = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = 150 UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACT = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLNL = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = 14e-4 PB = 9.83E-01 MJ = 5.79E-01
+CJSW = 3.2e-10 PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

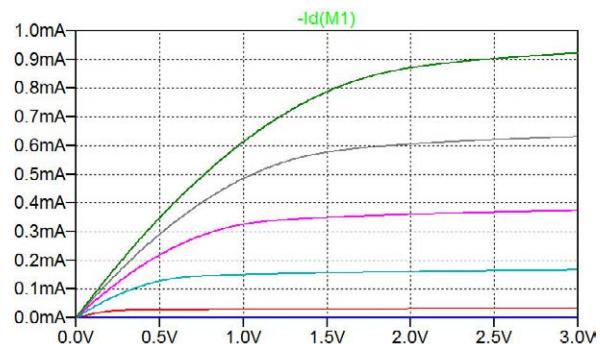
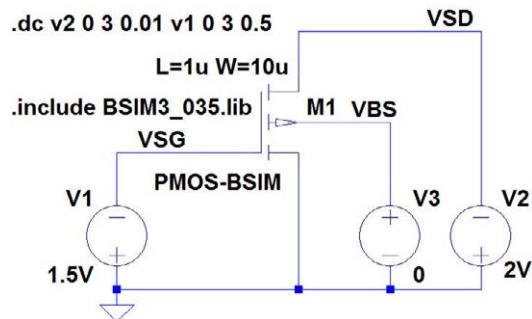
Figure P3.3

Solution:

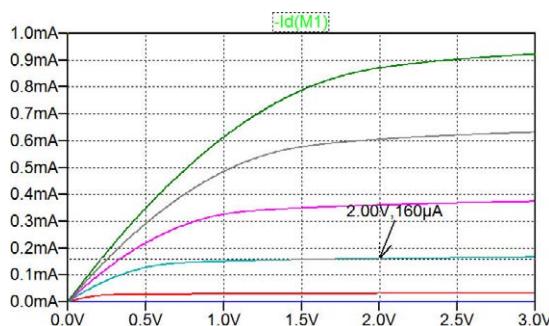
The figure below shows the schematic for simulating the input characteristics. Also shown is the resulting plot of I_D versus V_{SD} for $V_{SD} = 0$ V (green curve), 0.5 V (blue curve), 1.0 V (red curve), 1.5 V (cyan curve), 2.0 V (purple curve), 2.5 V (grey curve) and 3.0 V (dark green curve). Because of the difference in sign conventions between textbooks and LTspice, the plot below shows $-Id(M1)$ which is equal to I_D using the normal textbook convention.



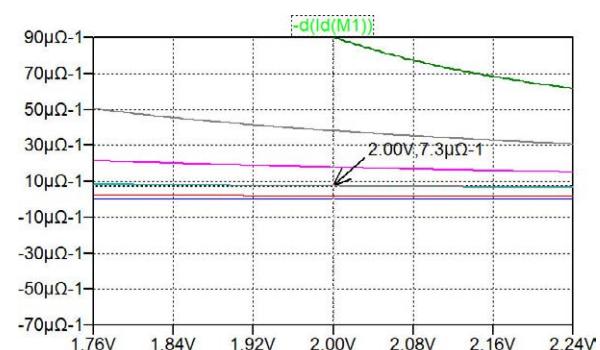
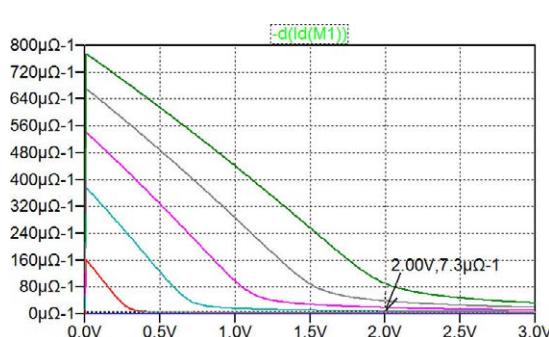
The figure below shows the schematic for simulating the output characteristics. Also shown is the resulting plot of I_D versus V_{SD} for $V_{SG} = 0$ V (green curve, not visible because of the blue curve), 0.5 V (blue curve), 1.0 V (red curve), 1.5 V (cyan curve), 2.0 V (purple curve), 2.5 V (grey curve) and 3.0 V (dark green curve).



For finding I_D for $V_{SG} = 1.5$ V, $V_{BS} = 0$ V and $V_{SD} = 2.0$ V, the output characteristics above are used with a cursor placed on the cyan curve, see figure below. The cursor is shifted from one curve to another by the up/down arrow keys. We find $I_D = 0.16$ mA.



For finding $\partial i_D / \partial v_{SD}$ for $V_{SG} = 1.5$ V, $V_{BS} = 0$ V and $V_{SD} = 2.0$ V, the derivative of I_D is plotted as shown below. It may be a good idea to zoom in on the relevant part of the characteristics as also shown in the figure. We find $\partial i_D / \partial v_{SD} = 7.3 \mu\text{A/V}$.



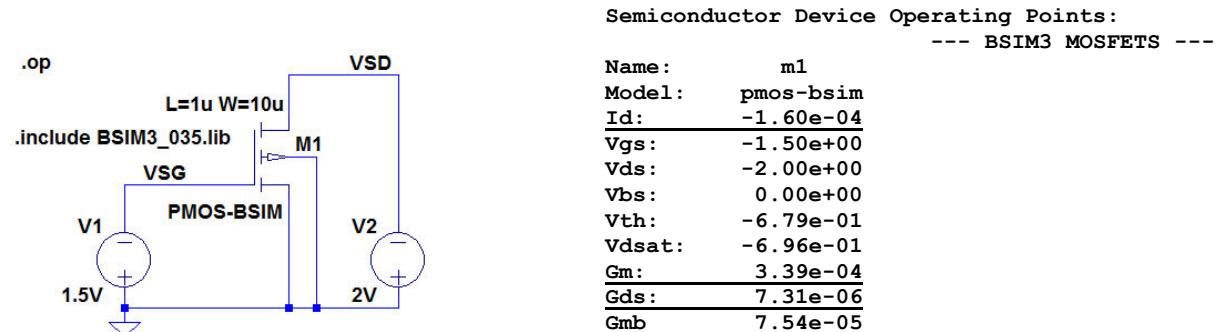
3.4

```
.MODEL PMOS-BSIM PMOS LEVEL = 49
+VERSION = 3.1 TNOM = 2.69E+01 TOX = 7.0E-9
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = -0.6
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVTOW = 0.00E+00 DVT1W = 0 DVT2W = 0.29E-01
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = 150 UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELT = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLNL = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = 14e-4 PB = 9.83E-01 MJ = 5.79E-01
+CJSW = 3.2e-10 PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

Figure P3.4

Solution:

The figure below shows the schematic for simulating the small-signal parameters and the resulting error log file with the relevant parameters underlined.



From the small-signal parameters, the following Shichman-Hodges model parameters are calculated. Beware of the signs. For a PMOS transistor, the easiest solution is to use numeric values in the equations (3.12) to (3.15) in ‘CMOS Integrated Circuit Simulation with LTspice’. Remember that the threshold voltage is negative for a PMOS transistor.

$$\begin{aligned}\lambda &= \frac{g_{ds}}{|I_D| - g_{ds}|V_{DS}|} = 0.05 \text{ V}^{-1} \\ V_{to} &= -\left(|V_{GS}| - \frac{2|I_D|}{g_m}\right) = -0.556 \text{ V} \\ K_p &= \left(\frac{g_m}{|I_D|}\right)^2 \left(\frac{|I_D| - g_{ds}|V_{DS}|}{2(W/L)}\right) = 32.6 \mu\text{A/V}^2 \\ |2\Phi_F| &= 0.7 \text{ V} \\ \gamma &= 2\sqrt{|2\Phi_F|} \frac{g_{mb}}{g_m} = 1.67 \frac{g_{mb}}{g_m} = 0.37 \sqrt{\text{V}}\end{aligned}$$



Scholarships




Lnu.se

Open your mind to new opportunities

With 31,000 students, Linnaeus University is one of the larger universities in Sweden. We are a modern university, known for our strong international profile. Every year more than 1,600 international students from all over the world choose to enjoy the friendly atmosphere and active student life at Linnaeus University. Welcome to join us!

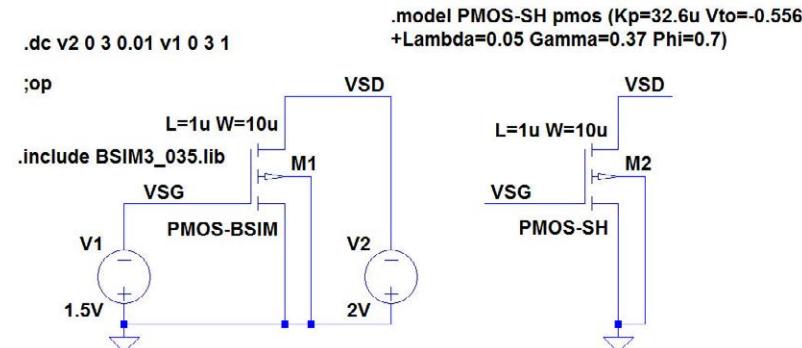
Linnaeus University
Sweden

Bachelor programmes in
Business & Economics | Computer Science/IT |
Design | Mathematics

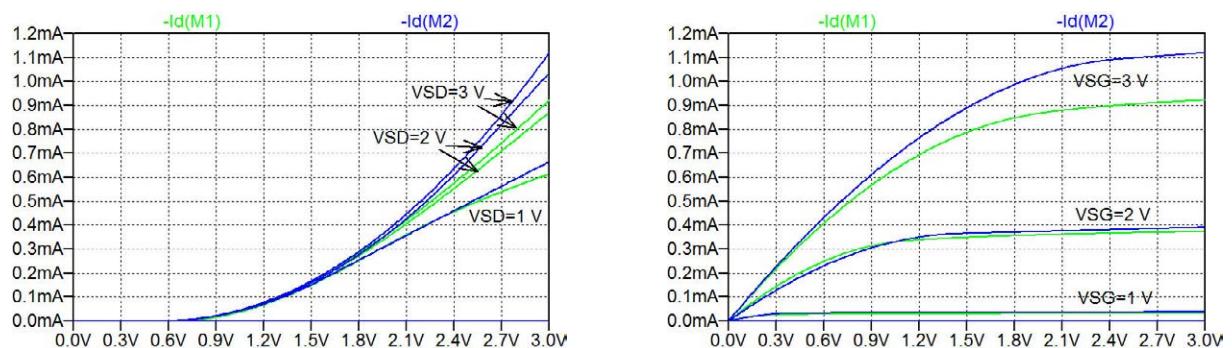
Master programmes in
Business & Economics | Behavioural Sciences | Computer
Science/IT | Cultural Studies & Social Sciences | Design |
Mathematics | Natural Sciences | Technology & Engineering

Summer Academy courses

For simulating the input characteristics and the output characteristics for both the BSIM3 transistor model and the Shichman-Hodges transistor model, the schematic shown below is used. The ‘.dc’ command specification shown gives the output characteristics. For the input characteristics, use V1 as the first source and V2 as the second source.



The simulations result in the characteristics shown below with the green curves for the BSIM3 model and the blue curves for the Shichman-Hodges model.



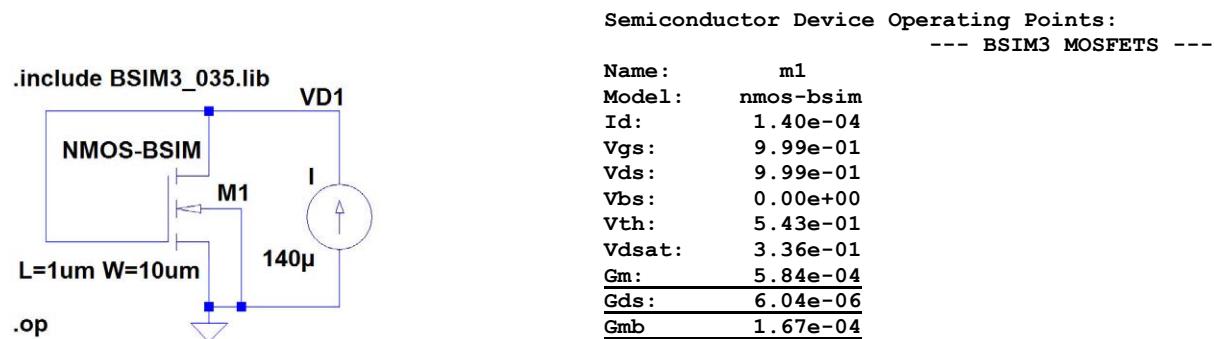
3.5

```
.MODEL NMOS-BSIM NMOS LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 7.8E-9
+XJ = 1E-07 NCH = 2.18E+17 VTH0 = 0.48
+K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01
+K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01
+U0 = 360 UA = -8.48E-10 UB = 2.27E-18
+UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00
+AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06
+KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01
+RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02
+WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10
+DWG = -4.27E-09
+DWB = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00
+CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00
+CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01
+DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04
+PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-02
+PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02
+DELT = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.11E-01
+KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09
+UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04
+WL = 0 WLN = 9.95E-01 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12
+CJ = 9e-4 PB = 7.95E-01 MJ = 3.53E-01
+CJSW = 2.8e-10 PBSW = 7.98E-01 MJSW = 1.73E-01
+CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01
+CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01
+PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03
```

Figure P3.5

Solution:

The figure below shows the schematic for simulating the small-signal parameters and the resulting error log file with the relevant parameters underlined.



From the small-signal parameters, the following Shichman-Hodges model parameters are calculated using equations (3.12) to (3.15) in ‘CMOS Integrated Circuit Simulation with LTspice’.

$$\begin{aligned}\lambda &= \frac{g_{ds}}{I_D - g_{ds}V_{DS}} = 0.045 \text{ V}^{-1} \\ V_{to} &= V_{GS} - \frac{2I_D}{g_m} = 0.520 \text{ V} \\ K_p &= \left(\frac{g_m}{I_D} \right)^2 \left(\frac{I_D - g_{ds}V_{DS}}{2(W/L)} \right) = 117 \text{ } \mu\text{A/V}^2 \\ |2\Phi_F| &= 0.7 \text{ V} \\ \gamma &= 2\sqrt{|2\Phi_F|} \frac{g_{mb}}{g_m} = 1.67 \frac{g_{mb}}{g_m} = 0.48 \sqrt{\text{V}}\end{aligned}$$

Cynthia | AXA Graduate

AXA Global Graduate Program

Find out more and apply

redefining / standards **AXA**

Download free eBooks at bookboon.com

Click on the ad to read more

3.6

$$K_p = 190 \mu\text{A/V}^2, V_{to} = 0.57 \text{ V}, \lambda = 0.16 \text{ V}^{-1}, \\ \gamma = 0.5 \sqrt{\text{V}}, |2\Phi_F| = 0.7 \text{ V}.$$

Figure P3.6

For an NMOS transistor with the Shichman-Hodges parameters shown in Fig. P3.6 and a channel length $L = 1 \mu\text{m}$, simulate and plot g_m and g_{ds} versus the drain current I_D for $W = 10 \mu\text{m}$, $W = 30 \mu\text{m}$ and $W = 50 \mu\text{m}$, and $0 < I_D < 10 \text{ mA}$. Assume a drain-source voltage of $V_{DS} = 1.2 \text{ V}$.

From the plots of g_m and g_{ds} , find the maximum drain current for which the transistor is in the active region for each of the three values of channel width.

Solution:

For simulating the small-signal parameters g_m and g_{ds} , we use a circuit similar to the circuit shown in Fig. 3.30 in ‘CMOS Integrated Circuit Simulation with LTspice’. For convenience, this figure is shown below.

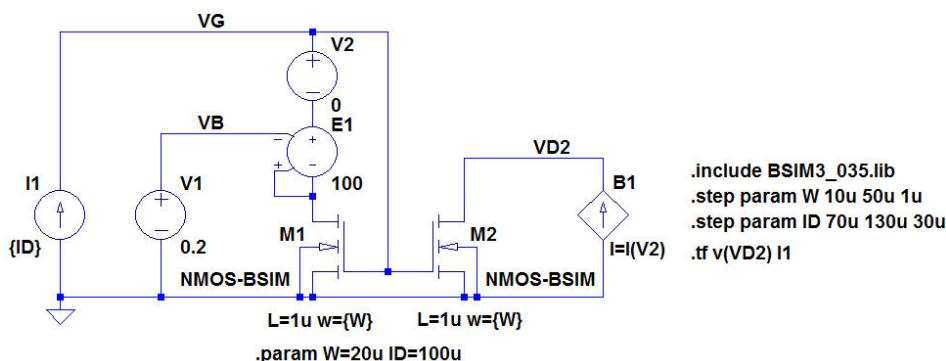
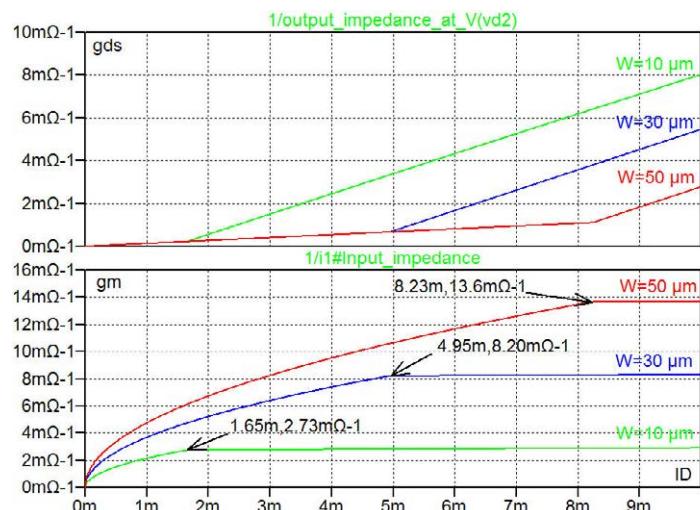
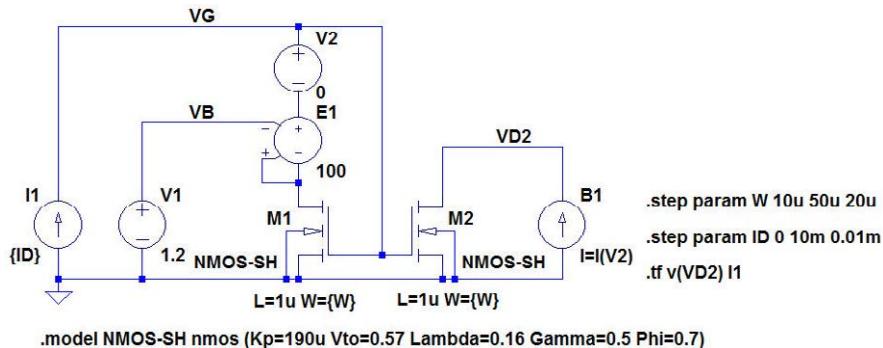


Figure 3.30: NMOS current mirror with voltage buffer for the drain voltage for simulating both g_{ds} and g_m .

For the simulations for finding g_m and g_{ds} versus I_D , the LTspice schematic shown on the next page is used. Two ‘.step’ directives are inserted, one for ID and one for W . The ‘.step’ directive for ID is inserted first in order to define ID as the first parameter to step, i.e. defining the x-axis in the output plot from the simulation. The step size for ID has been chosen to be small, 0.01 mA, in order to get a smooth simulation plot all the way down to 0 mA.

From the ‘.tf’ simulation, the transconductance g_m is found as ‘1/i1#Input_impedance’ and the output conductance g_{ds} is found as ‘1/output_impedance_at_V(vd2)’, both of which are shown on the next page. The green curves are for $W = 10 \mu\text{m}$, the blue curves are for $W = 30 \mu\text{m}$, and the red curves are for $W = 50 \mu\text{m}$.



..... Alcatel-Lucent

www.alcatel-lucent.com/careers

What if you could build your future and create the future?

One generation's transformation is the next's status quo. In the near future, people may soon think it's strange that devices ever had to be "plugged in." To obtain that status, there needs to be "The Shift".



Click on the ad to read more

Clearly, there is a kink in each of the curves, indicating the limit between the active region (small values of drain current) and the triode region (large values of drain current). From the kinks, we find the following maximum values of drain current for which the transistor is in the active region:

$W = 10 \mu\text{m}$: $I_{D\max} = 1.65 \text{ mA}$; $W = 30 \mu\text{m}$: $I_{D\max} = 4.95 \text{ mA}$; $W = 50 \mu\text{m}$: $I_{D\max} = 8.23 \text{ mA}$.

In the active region, g_m is found from

$$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_D (1 + \lambda V_{DS})}$$

showing a square root dependency on I_D (Equation (3.8) in ‘CMOS Integrated Circuit Simulation with LTspice’).

In the triode region, g_m is found from

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right) V_{DS} (1 + \lambda V_{DS})$$

showing that g_m does not depend on I_D (Equation (3.11) in ‘CMOS Integrated Circuit Simulation with LTspice’).

For g_{ds} , we note that in the active region,

$$g_{ds} = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$

showing that g_{ds} is independent of W and linearly increasing with I_D (Equation (3.8) in ‘CMOS Integrated Circuit Simulation with LTspice’).

In the triode region, an approximate expression for g_{ds} (neglecting λ) is

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_t - V_{DS})$$

Using

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) [(V_{GS} - V_t)V_{DS} - V_{DS}^2/2] \Rightarrow V_{GS} - V_t = \frac{I_D/V_{DS}}{\mu_n C_{ox}(W/L)} + V_{DS}/2$$

we find

$$g_{ds} = \frac{I_D}{V_{DS}} - \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) V_{DS}$$

showing that g_{ds} increases linearly with I_D and decreases linearly with W as also found from the simulation.

3.7

$$K_p = 190 \mu\text{A}/\text{V}^2, V_{to} = 0.57 \text{ V}, \lambda = 0.16 \text{ V}^{-1}, \\ \gamma = 0.5 \sqrt{\text{V}}, |2\Phi_F| = 0.7 \text{ V}.$$

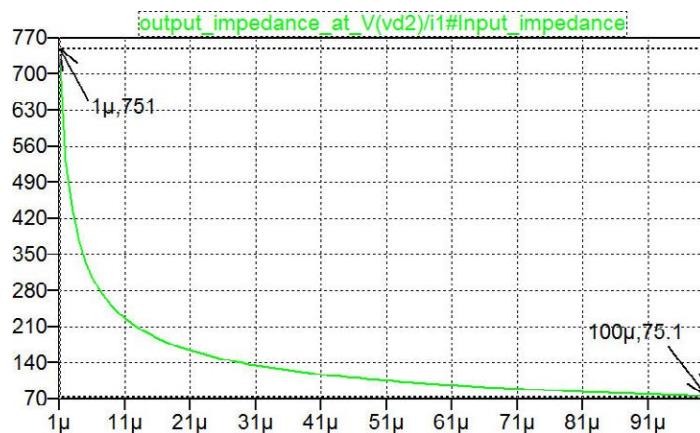
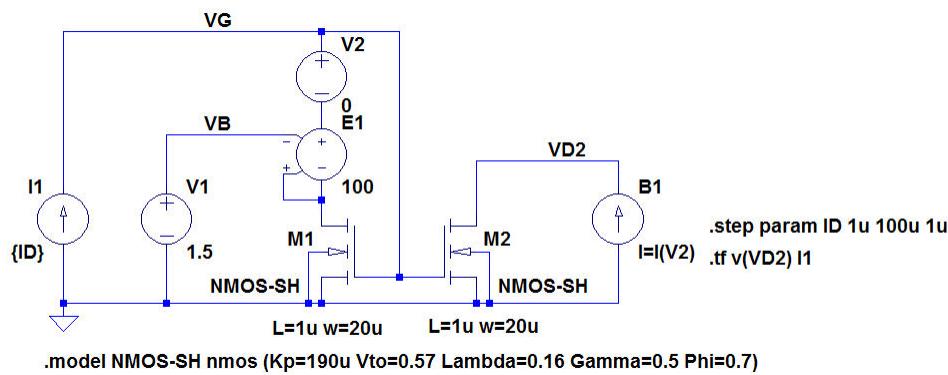
Figure P3.7

For an NMOS transistor with the Shichman-Hodges parameters shown in Fig. P3.7, a channel width $W = 20 \mu\text{m}$ and a channel length $L = 1 \mu\text{m}$, simulate and plot g_m/g_{ds} versus the drain current I_D for $1 \mu\text{A} < I_D < 100 \mu\text{A}$. Assume a drain-source voltage of $V_{DS} = 1.5 \text{ V}$.

Also plot g_m/g_{ds} versus $1/\sqrt{I_D}$. Find g_m/g_{ds} for $I_D = 1 \mu\text{A}$ and $I_D = 100 \mu\text{A}$.

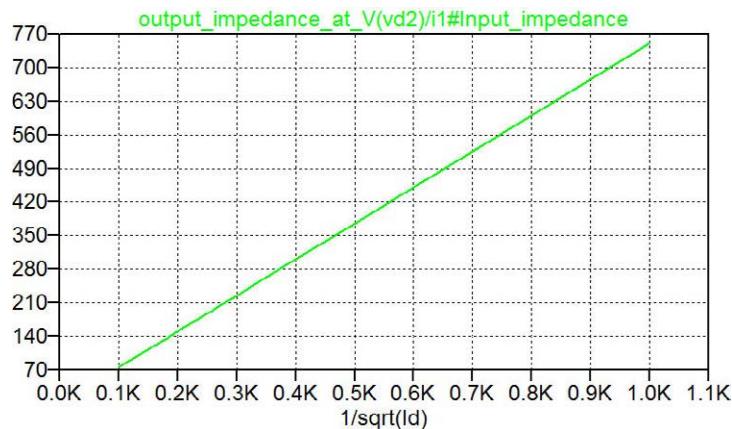
Solution:

For simulating g_m and g_{ds} , we use the circuit shown in Fig. 3.30 in ‘CMOS Integrated Circuit Simulation with LTspice’ (also shown on page 46 in this book). The figure below shows the LTspice schematic and a plot of g_m/g_{ds} shown as ‘output impedance at $V(vd2)/i1#Input impedance$ ’.



From the plot, we find $g_m/g_{ds} = 751$ for $I_D = 1 \mu\text{A}$ and $g_m/g_{ds} = 75.1$ for $I_D = 100 \mu\text{A}$.

In order to show g_m/g_{ds} versus $1/\sqrt{I_D}$, we move the cursor to the horizontal axis and right-click. In the window for ‘Quantity plotted’, we enter ‘1/sqrt(Id)’. The resulting plot is shown below. It is clearly seen that the intrinsic transistor gain g_m/g_{ds} is inversely proportional to $\sqrt{I_D}$ when using the Shichman-Hodges transistor model.



Nido

Luxurious accommodation

Central zone 1 & 2 locations

Meet hundreds of international students

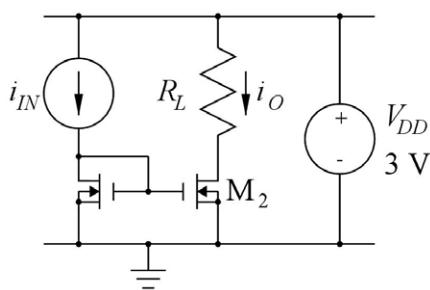
BOOK NOW and get a £100 voucher from voucherexpress

Nido Student Living - London

Visit www.NidoStudentLiving.com/Bookboon for more info.

+44 (0)20 3102 1060

3.8



$$W_1 = W_2 = 20 \mu\text{m}, L_1 = L_2 = 1 \mu\text{m},$$

$$AD_1 = AD_2 = 20 \times 10^{-12} \text{ m}^2,$$

$$PD_1 = PD_2 = 22 \mu\text{m}.$$

Figure P3.8

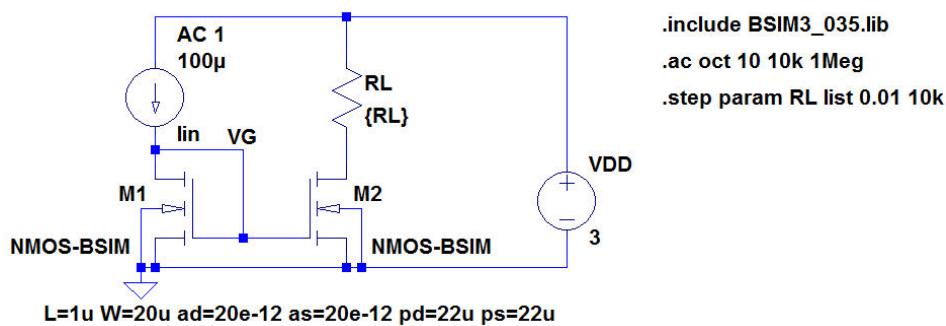
For the current mirror shown in Fig. P3.8, use a ‘.ac’ simulation to find the input resistance and the input capacitance. Assume that the input impedance can be approximated by a parallel connection of a capacitance and a resistance so that the equations shown on page 65 - 66 can be used. Assume a dc value of $100 \mu\text{A}$ for the input current and use the transistor dimensions shown in the figure. Also, use the BSIM3 transistor model shown in Fig. P3.5 on page 112 (BSIM3 0.35 μm model, Fig. 3.10).

Find the input resistance and input capacitance for two different values of the load resistor:

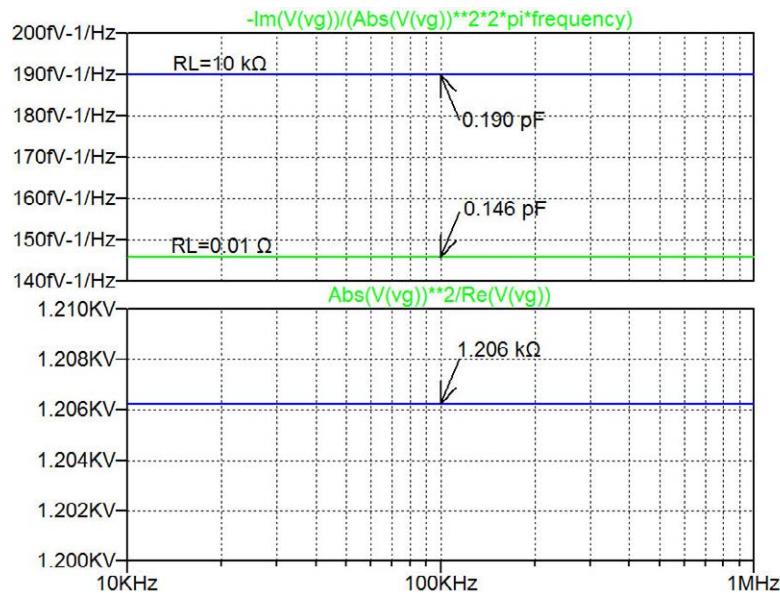
$$R_L = 0 \Omega \text{ and } R_L = 10 \text{ k}\Omega.$$

Solution:

The LTspice schematic for simulating the current mirror is shown below. Notice the ‘.step’ directive for R_L . As LTspice does not accept a value of 0 for a resistor, R_L is stepped between the values 0.01Ω and $10 \text{ k}\Omega$. For finding the input resistance and input capacitance, we plot ‘ $\text{Abs}(V(\text{vg}))^{**2}/\text{Re}(V(\text{vg}))$ ’ and ‘ $-\text{Im}(V(\text{vg}))/(\text{Abs}(V(\text{vg}))^{**2}*2*\pi*\text{frequency})$ ’, respectively, compare equations (2.15) and (2.16) on page 65 - 66 in ‘CMOS Integrated Circuit Simulation with LTspice’. The plots are shown on the following page. From the plots, we find $R_{in} = 1.206 \text{ k}\Omega$, independent of R_L , $C_{in} = 0.146 \text{ pF}$ for $R_L = 0 \Omega$ and $C_{in} = 0.190 \text{ pF}$ for $R_L = 10 \text{ k}\Omega$.



The increase in input capacitance for $R_L = 20 \text{ k}\Omega$ is due to the gain from the gate to the drain of M_2 , causing a Miller effect on the gate-drain capacitance of M_2 , compare for instance the example given in Fig. 2.27 on page 69 in ‘CMOS Integrated Circuit Simulation with LTspice’.



SIMPLY CLEVER
ŠKODA



**WE WILL TURN YOUR CV
INTO AN OPPORTUNITY
OF A LIFETIME**

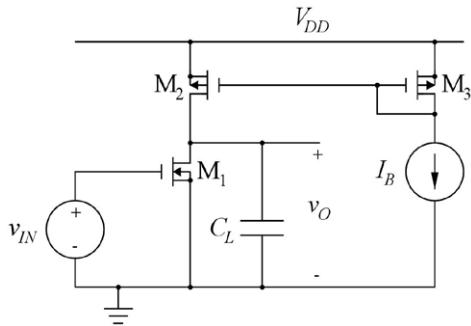
Do you like cars? Would you like to be a part of a successful brand?
As a constructor at ŠKODA AUTO you will put great things in motion. Things that will
ease everyday lives of people all around. Send us your CV. We will give it an entirely
new new dimension.

[Send us your CV on
www.employerforlife.com](http://www.employerforlife.com)



Tutorial 4 – Basic Gain Stages

4.1



$$W_2 = W_3 = 25 \mu\text{m}, L_1 = L_2 = L_3 = 1 \mu\text{m}$$

$$C_L = 3.2 \text{ pF}, V_{DD} = 3 \text{ V}, I_B = 100 \mu\text{A}.$$

Figure P4.1

For the common-source amplifier shown in Fig. P4.1, design M₁ so that the gain-bandwidth product of the stage is 50 MHz. Assume transistor models as specified in Fig. P3.2 on page 109 and Fig. P3.3 on page 110 and use a channel length of L₁ = 1 μm. Use a channel width for M₁ which is a multiple of 1 μm.

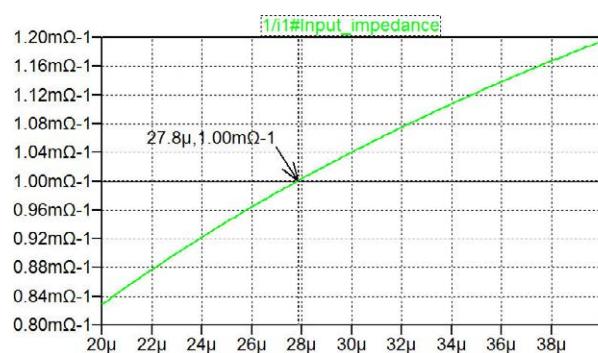
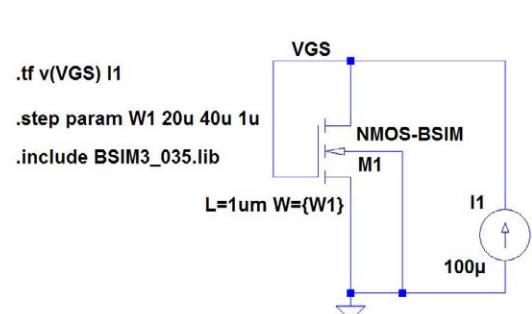
Hint: Design M₁ to have the required g_m for the gain-bandwidth product with I_D = 100 μA. Find g_m versus I_D using the method shown in Example 3.5 on page 100.

Find the dc bias value of the input voltage for which the output voltage is 1.5 V and find the small-signal voltage gain A_v at low frequencies.

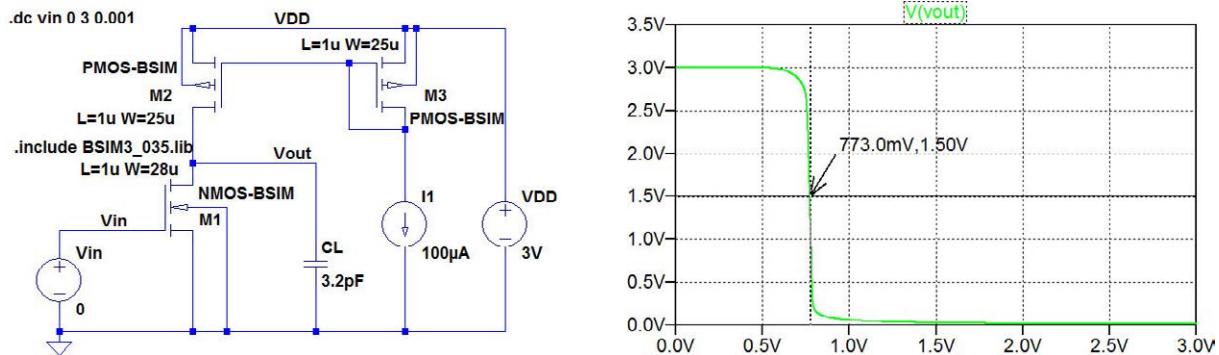
Figures P3.2 and P3.3 are shown on page 37 and 39, respectively, in this book.

Solution:

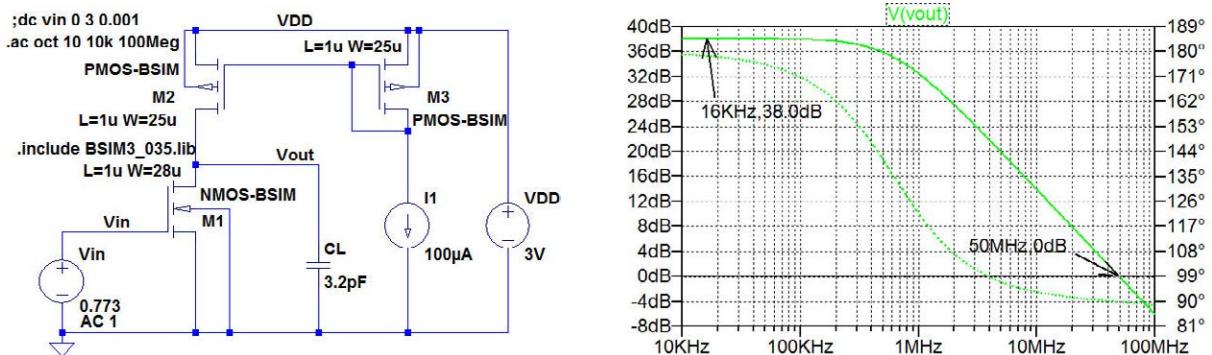
From $2\pi \cdot \text{GBW} = g_m / C_L$, we find $g_m = 1.0 \text{ mA/V}$. In order to find a transistor channel width giving this value of g_m, we run the simulation shown below. From this, we find W₁ = 28 μm.



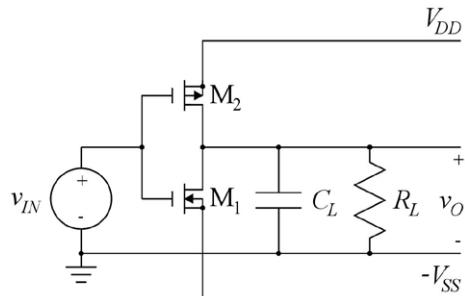
With $W_1 = 28 \mu\text{m}$, the common-source amplifier is shown in the figure below with a specification for a '.dc' simulation. From the resulting simulation, we find an input bias voltage of $V_{IN} = 0.773 \text{ V}$ for an output bias voltage of 1.5 V.



With the bias value for V_{in} inserted and with an ac amplitude of 1 V for V_{in} , a '.ac' simulation will show both the gain at low frequencies and verify the gain-bandwidth product of 50 MHz. The figures below show the schematic and the resulting simulation plot. From the plot, we find a low-frequency gain of 38 dB and a gain-bandwidth product of 50 MHz, found as the frequency where the gain has dropped to 0 dB.



4.2



$$V_{DD} = V_{SS} = 1.5 \text{ V}, L_1 = L_2 = 1 \mu\text{m}$$

$$C_L = 0.5 \text{ pF}, R_L = 10 \text{ k}\Omega$$

Figure P4.2

For the inverting amplifier shown in Fig. P4.2, design M_1 and M_2 so that the dc bias value of the output voltage is within the range $\pm 100 \text{ mV}$ with an input dc bias voltage of 0 V and so that the low-frequency small-signal gain with an input dc bias voltage of 0 V is -10 V/V . Assume transistor models as specified in Fig. P3.2 on page 109 and Fig. P3.3 on page 110 and use a channel length of $L_1 = L_2 = 1 \mu\text{m}$. Use channel widths for M_1 and M_2 which are multiples of $0.5 \mu\text{m}$. What is the low-frequency small-signal gain if the load resistor R_L is omitted? What is the gain-bandwidth product of the amplifier for $R_L = 10 \text{ k}\Omega$ and for $R_L = \infty$?

Figures P3.2 and P3.3 are shown on page 37 and 39, respectively in this book.



UPPSALA
UNIVERSITET

Develop the tools we need for Life Science
Masters Degree in Bioinformatics

Bioinformatics is the exciting field where biology, computer science, and mathematics meet.

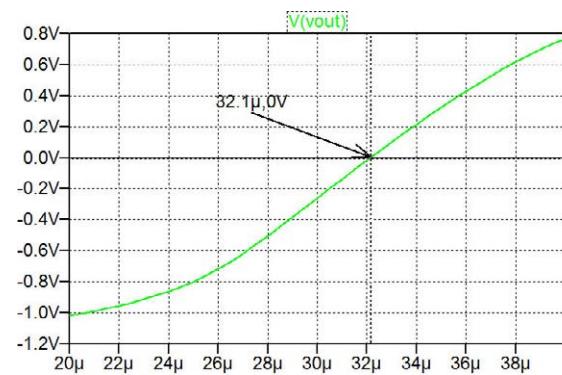
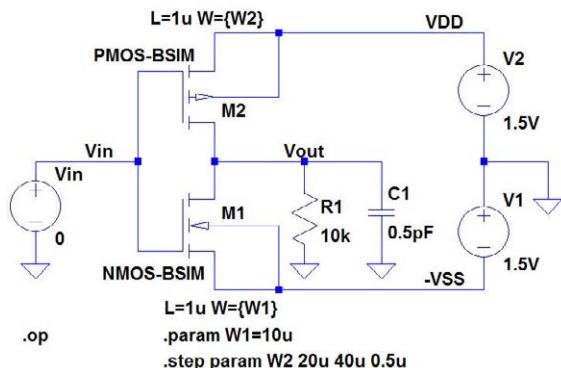
We solve problems from biology and medicine using methods and tools from computer science and mathematics.

Read more about this and our other international masters degree programmes at www.uu.se/master

Solution:

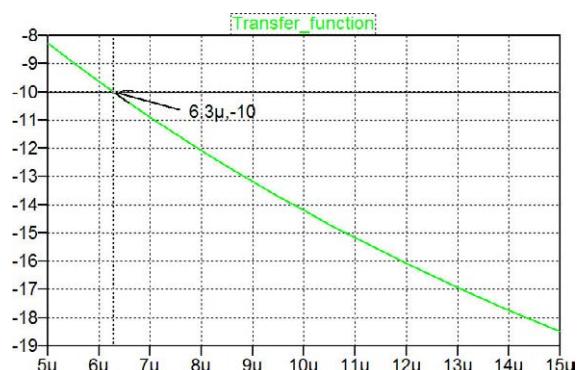
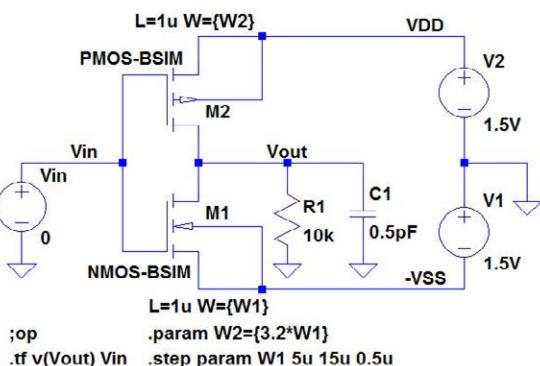
We start the solution by finding a ratio between the channel widths for the NMOS transistor (M_1) and the PMOS transistor (M_2). For this, we may run a simulation as shown below where the channel widths are defined as parameters. The width W_1 is selected to be $10 \mu\text{m}$ while the width W_2 is stepped from $2W_1$ ($20 \mu\text{m}$) to $4W_1$ ($40 \mu\text{m}$). From a ‘.op’ simulation, the output voltage is plotted versus W_2 . The plot below shows that with $W_1 = 10 \mu\text{m}$, W_2 should be $32 \mu\text{m}$ in order to obtain an output voltage of 0 V . Thus, the ratio between W_2 and W_1 is 3.2.

.include BSIM3_035.lib



Next, we define the parameter W_2 to be 3.2 times the parameter W_1 and we step the parameter W_1 over a suitable range ($5 \mu\text{m}$ to $15 \mu\text{m}$) and run a ‘.tf’ simulation in order to find the low-frequency gain as a function of W_1 , see figures below. From the simulation plot, we find that in order to obtain a gain of -10 V/V , W_1 should be $6.3 \mu\text{m}$. Nearest multiple of $0.5 \mu\text{m}$ is $W_1 = 6.5 \mu\text{m}$, and with this value of W_1 , we find $W_2 = 3.2 W_1 = 20.8 \mu\text{m}$. Rounding off to nearest multiple of $0.5 \mu\text{m}$ gives $W_2 = 21 \mu\text{m}$.

.include BSIM3_035.lib



With $W_1 = 6.5 \mu\text{m}$ and $W_2 = 21 \mu\text{m}$, we run a ‘.op’ simulation to verify the bias value of the output voltage and a ‘.tf’ simulation to verify the gain.

The outputs of these simulations are shown below, and we find results reasonably close to the design targets.

Finally, in order to find low-frequency gain and gain-bandwidth product for $R_L = 10 \text{ k}\Omega$ and $R_L = \infty$, we run a ‘.ac’ simulation with R_L stepped between two values, 10k and 10G. From the simulation plot on the following page, we find that with $R_L = \infty$ (10G), the low-frequency gain is 32.6 dB (or -43.6 V/V), and the gain-bandwidth product is 400 MHz, independent of R_L .

UNIVERSITY OF COPENHAGEN



Copenhagen Master of Excellence

Copenhagen Master of Excellence are two-year master degrees taught in English at one of Europe's leading universities

Come to Copenhagen - and aspire!

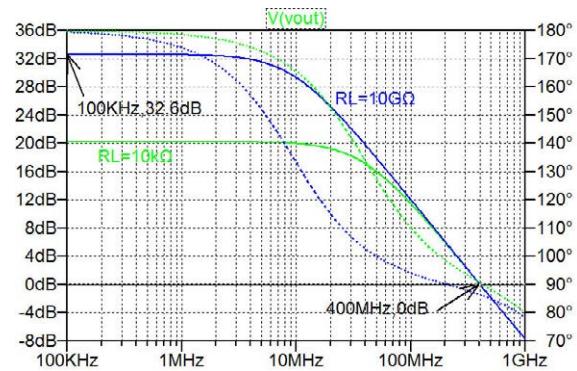
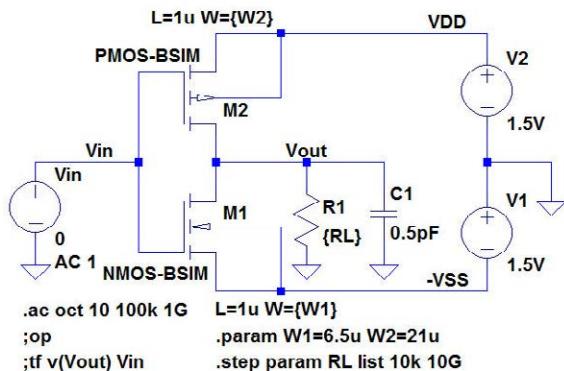
Apply now at
www.come.ku.dk



Download free eBooks at bookboon.com

Click on the ad to read more

.include BSIM3_035.lib

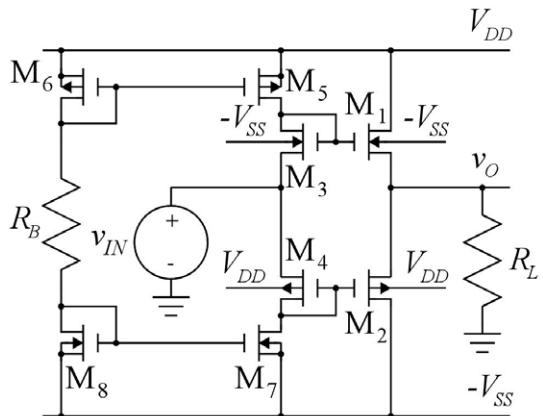


In order to verify that the ‘.ac’ simulation runs from a reasonable bias point, also when $R_L = \infty$, a ‘.op’ simulation with $R_L=10G$ may be run. The output file from this simulation is shown below, confirming that the bias value of V_O is less than 100 mV.

--- Operating Point ---

<u>V(vout) :</u>	0.0856978	<u>voltage</u>
<u>V(vin) :</u>	0	<u>voltage</u>
<u>V(vdd) :</u>	1.5	<u>voltage</u>
<u>V(-vss) :</u>	-1.5	<u>voltage</u>

4.3



$$L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L_7 = L_8 = 0.35 \mu\text{m}$$

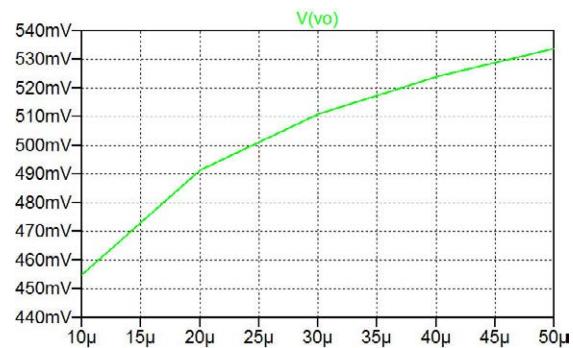
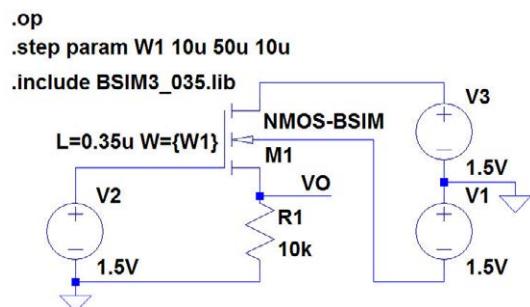
$$R_L = 10 \text{ k}\Omega, V_{DD} = V_{SS} = 1.5 \text{ V}.$$

Figure P4.3

Figure P4.3 shows a class AB buffer amplifier. Design the output transistors M_1 and M_2 so that the amplifier can deliver an output-voltage swing of $\pm 0.5 \text{ V}$ with a load resistor of $10 \text{ k}\Omega$. Assume that the gate voltage of M_1 and M_2 can reach the positive and negative supply voltages, respectively. Select values of the channel widths which are multiples of $10 \mu\text{m}$. Use transistor models as specified in Fig. P3.2 on page 109 and Fig. P3.3 on page 110. Design the bias network M_3 – M_8 and R_B to provide a bias current of $1 \mu\text{A}$ for M_3 – M_8 . M_5 – M_8 should be designed to have a saturation voltage $|V_{DSsat}|$ of less than 50 mV , and the channel widths should be multiples of $10 \mu\text{m}$. M_3 and M_4 should be scaled to channel widths of 0.1 times the channel widths of M_1 and M_2 , respectively. Plot the output voltage versus the input voltage for $-1.5 \text{ V} < v_{IN} < 1.5 \text{ V}$. Find the open-circuit voltage gain and the output resistance of the buffer for an input bias voltage of 0 V . Find the bias current in M_1 and M_2 for an output bias voltage of $V_O = 0 \text{ V}$. Why is the current scaling in M_1 – M_2 / M_3 – M_4 different from the channel width scaling?

Solution:

For finding the channel width W_1 , we run a ‘.op’ simulation on a single NMOS transistor with gate, source, drain and bulk connected to voltages resulting in the highest value of output voltage. Using a ‘.step param’ directive, the output voltage is simulated versus the channel width. The figure below shows the schematic and the simulation plot from which we find $W_1 = 30 \mu\text{m}$ (using multiples of $10 \mu\text{m}$) in order to achieve an output voltage of $+0.5 \text{ V}$.



Brain power

By 2020, wind could provide one-tenth of our planet's electricity needs. Already today, SKF's innovative know-how is crucial to running a large proportion of the world's wind turbines.

Up to 25 % of the generating costs relate to maintenance. These can be reduced dramatically thanks to our systems for on-line condition monitoring and automatic lubrication. We help make it more economical to create cleaner, cheaper energy out of thin air.

By sharing our experience, expertise, and creativity, industries can boost performance beyond expectations.

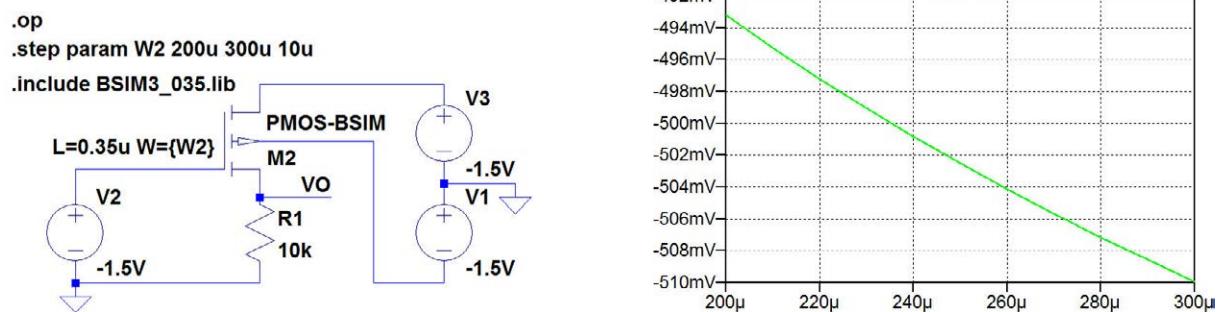
Therefore we need the best employees who can meet this challenge!

The Power of Knowledge Engineering

Plug into The Power of Knowledge Engineering.
Visit us at www.skf.com/knowledge

SKF

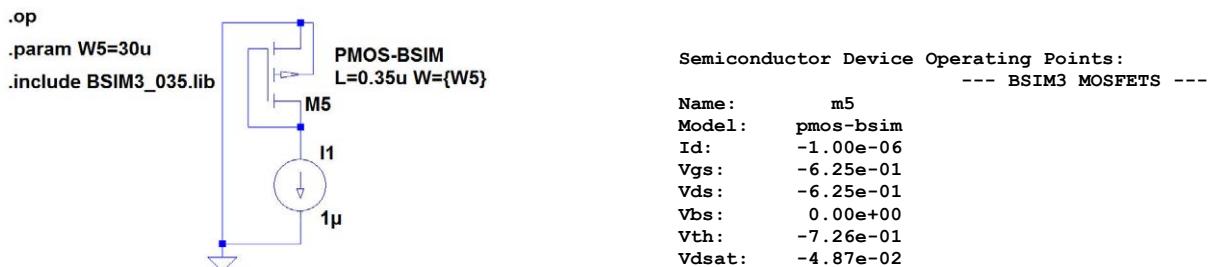
The channel width W_2 is found in the same way as W_1 , running a ‘.op’ simulation on a single PMOS transistor with gate, source, drain and bulk connected to voltages resulting in the lowest value of output voltage. The figure below shows the schematic and the simulation plot from which we find $W_2 = 240 \mu\text{m}$ (using multiples of $10 \mu\text{m}$) in order to achieve an output voltage of -0.5 V .



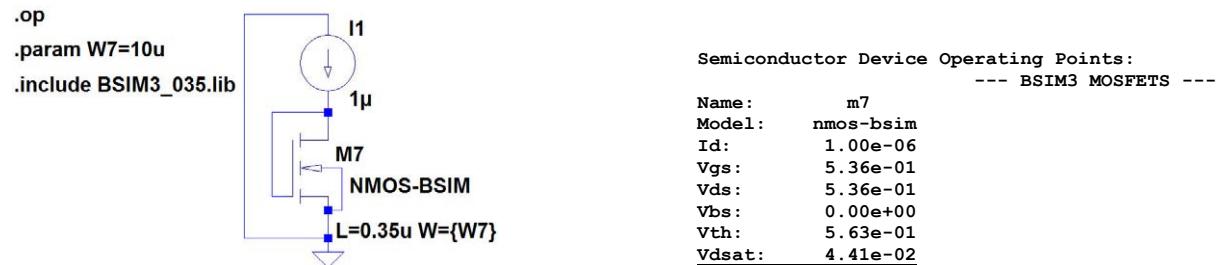
For the bias network, M_3 and M_4 are designed by scaling W_1 and W_2 by a factor of 10, respectively. This gives $W_3 = 3 \mu\text{m}$ and $W_4 = 24 \mu\text{m}$.

The transistors M_5 - M_8 should have a saturation voltage of less than 50 mV for a drain current of $1 \mu\text{A}$.

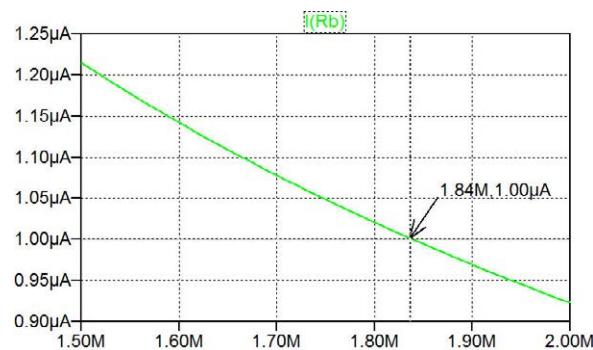
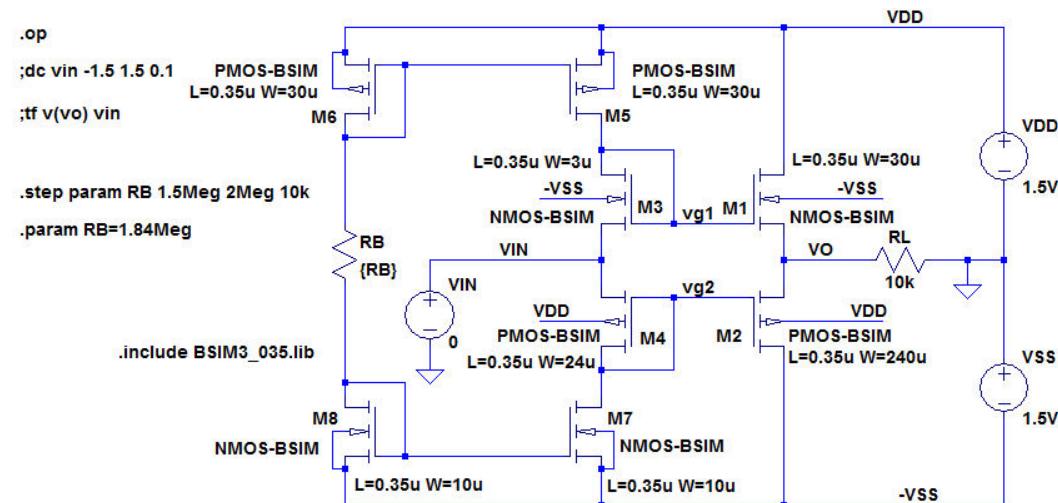
For the PMOS transistors (M_5 and M_6), the channel width is found from the simulation shown in the figure below. The simulation is run with different values of W_5 in multiples of $10 \mu\text{m}$ and the smallest value of W_5 resulting in $|V_{dsat}| < 50 \text{ mV}$ is selected, i.e. $W_5 = W_6 = 30 \mu\text{m}$.



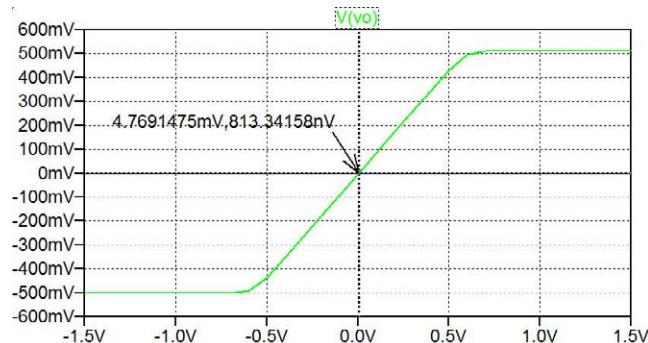
For the NMOS transistors (M_7 and M_8), the channel width is found from the simulation shown in the figure below. The simulation is run with different values of W_7 in multiples of 10 μm and the smallest value of W_7 resulting in $V_{dsat} < 50 \text{ mV}$ is selected, i.e. $W_7 = W_8 = 10 \mu\text{m}$.



With all transistor dimensions in place, the complete schematic can be drawn as shown below. The only device still to be designed is R_B . This can be found from a ‘.op’ simulation with R_B stepped over a suitable range. From the simulation plot shown below, we find that $R_B = 1.84 \text{ M}\Omega$ gives a bias current of 1 μA for M_6 and M_8 .



Next, a ‘.dc’ simulation is run, resulting in the simulation plot shown below. For this simulation, the ‘.step param’ directive is changed into a comment and R_B is defined by the ‘.param’ command shown in the schematic on the previous page.



Trust and responsibility

NNE and Pharmaplan have joined forces to create NNE Pharmaplan, the world's leading engineering and consultancy company focused entirely on the pharma and biotech industries.

Inés Aréizaga Esteva (Spain), 25 years old
Education: Chemical Engineer

– You have to be proactive and open-minded as a newcomer and make it clear to your colleagues what you are able to cope. The pharmaceutical field is new to me. But busy as they are, most of my colleagues find the time to teach me, and they also trust me. Even though it was a bit hard at first, I can feel over time that I am beginning to be taken seriously and that my contribution is appreciated.



NNE Pharmaplan is the world's leading engineering and consultancy company focused entirely on the pharma and biotech industries. We employ more than 1500 people worldwide and offer global reach and local knowledge along with our all-encompassing list of services.

nnepharmaplan.com

nne pharmaplan®



For finding the open circuit voltage gain and output resistance for an input bias voltage of 0 V, we run a ‘.tf’ simulation with R_L disconnected. The output file is shown below, and we find $A_{VOC} = 0.95$ V/V and $r_o = 1005 \Omega$.

```
--- Transfer Function ---

Transfer function:          0.951633      transfer
vin#Input impedance:        674020       impedance
output impedance at V(vo) : 1005.47      impedance
```

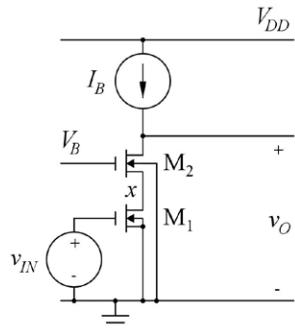
For finding the bias currents in M_1 and M_2 for an output voltage of 0 V, we use the ‘.dc’ simulation shown on the previous page to find the value of the input voltage resulting in $V(v_o) = 0$. From the plot, we find an input voltage of 4.769 mV. With this value of V_{IN} , we run a ‘.op’ simulation, and the error log file from this gives all the transistor bias currents as shown below.

```
Semiconductor Device Operating Points:
    --- BSIM3 MOSFETS ---
Name:      m6      m5      m2      m4      m8
Model:    pmos-bsim  pmos-bsim  pmos-bsim  pmos-bsim  nmos-bsim
Id:      -9.99e-07 -1.01e-06 -1.89e-05 -1.05e-06  9.99e-07
Vgs:     -6.25e-01 -6.25e-01 -8.82e-01 -8.86e-01  5.36e-01
Vds:     -6.25e-01 -6.35e-01 -1.50e+00 -8.86e-01  5.36e-01
Vbs:      0.00e+00  0.00e+00  1.50e+00  1.50e+00  0.00e+00
Vth:     -7.26e-01 -7.26e-01 -9.53e-01 -9.77e-01  5.63e-01
Vdsat:   -4.87e-02 -4.87e-02 -5.94e-02 -5.54e-02  4.41e-02

Name:      m7      m3      m1
Model:    nmos-bsim  nmos-bsim  nmos-bsim
Id:      1.05e-06  1.01e-06  1.89e-05
Vgs:     5.36e-01  8.60e-01  8.65e-01
Vds:     6.18e-01  8.60e-01  1.50e+00
Vbs:      0.00e+00 -1.50e+00 -1.50e+00
Vth:     5.62e-01  8.45e-01  8.32e-01
Vdsat:   4.43e-02  5.94e-02  6.62e-02
```

We notice that the current scaling in $M_1 - M_2 / M_3 - M_4$ is larger than the channel width scaling. This is caused by the larger $|V_{DS}|$ values for $M_1 - M_2$ than for $M_3 - M_4$, by the input offset voltage, and by the smaller threshold voltages for $M_1 - M_2$ than for $M_3 - M_4$.

4.4



$L_1 = L_2 = 1 \mu\text{m}$, $W_1 = W_2 = 10 \mu\text{m}$
 $I_B = 20 \mu\text{A}$, $V_B = 1.5 \text{ V}$, $V_{DD} = 3 \text{ V}$.

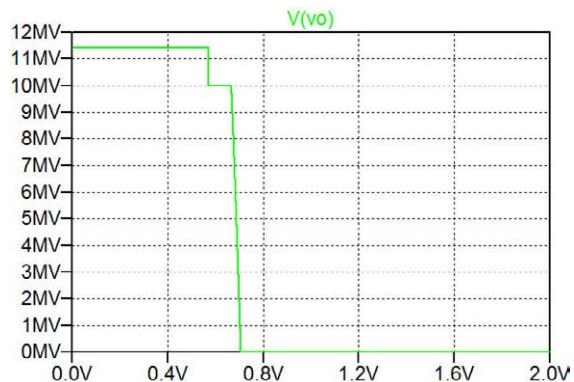
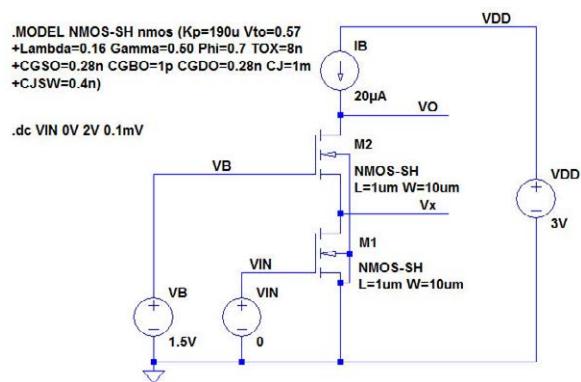
```
.MODEL NMOS-SH nmos (Kp=190u Vto=0.57
+Lambda=0.16 Gamma=0.50 Phi=0.7 TOX=8n
+CGSO=0.28n CGBO=1p CGDO=0.28n CJ=1m
+CJSW=0.4n)
```

Figure P4.4

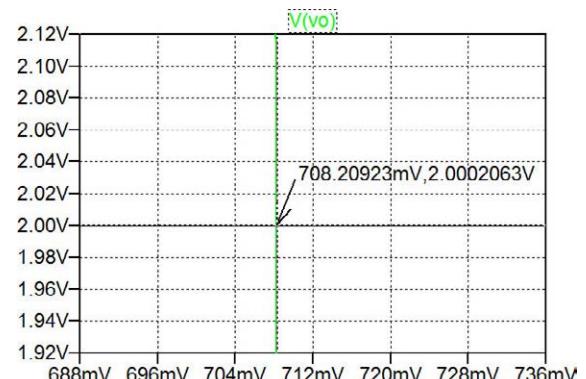
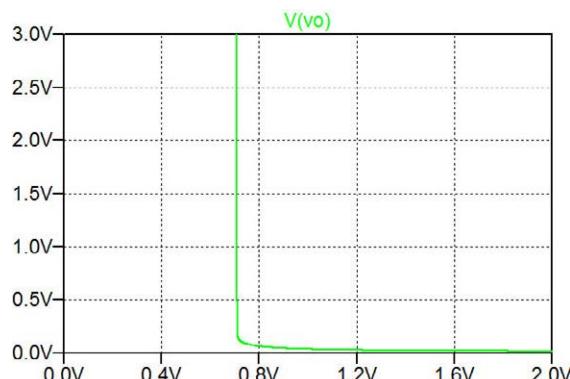
For the telescopic cascode shown in Fig. P4.4, find the bias value of V_{IN} required to give an output voltage of 2 V. Also find the small-signal gain A_{voc} and output resistance r_o at low frequencies. Find the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1 . Assume a transistor model as shown in Fig. P4.4.

Solution:

The figure below shows the cascode stage with a specification for a ‘.dc’ simulation. Also shown is the resulting plot of the output voltage. Apparently, the simulation generates unrealistically high output voltages, several MV. This is due to the fact that the drain of M_2 is connected directly to an ideal dc current source.



In order to see $V(v_o)$ in a realistic range of output voltages, we set the range of the y-axis to 3 V, either by the command ‘Plot Settings → Manual Limits’ or by moving the cursor to the y-axis and using a right-click on the mouse. The resulting plot is shown below, left plot. We see that the output voltage changes abruptly for an input voltage of about 0.7 V, and in order to find the exact input voltage, we zoom in on a small part of the plot, see right plot below. From this, we find $V_{IN} = 708.21$ mV. Notice that this value has been specified with a resolution exceeding the step size in the ‘.dc’ command, so it is based on an interpolation.



This e-book
is made with
SetaPDF



PDF components for PHP developers

www.setasign.com

In order to verify the bias point, we run a ‘.op’ simulation with a dc value of V_{IN} specified to 708.21 mV. The output file from this is shown below, and we see that $V(V_o)$ is sufficiently close to 2 V.

```
--- Operating Point ---

V(vx) :      0.638226      voltage
V(vin) :     0.70821       voltage
V(vo) :      1.97479       voltage
V(vb) :      1.5           voltage
V(vdd) :      3             voltage
```

With the bias point in place, the small-signal gain A_{voc} and output resistance r_o at low frequencies are found from a ‘.tf’ simulation with $V(V_O)$ as the output and VIN as the source. The output file from this ‘.tf’ simulation is shown below. From this, we find a gain of -14065 V/V or 83 dB and an output resistance of $49 \text{ M}\Omega$.

```
--- Transfer Function ---

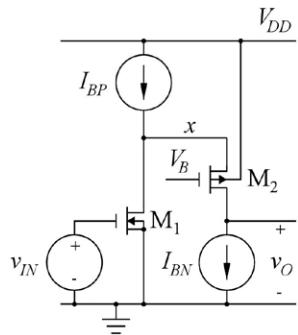
Transfer function:      -14065.1      transfer
vin#Input_impedance:    1e+020      impedance
output impedance at V(vo) : 4.89777e+007  impedance
```

For finding the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1 , we run a ‘.tf’ simulation with $V(V_x)$ as the output and VIN as the source. The output file from this ‘.tf’ simulation is shown below. From this, we find a resistance r_x of $344 \text{ k}\Omega$.

```
--- Transfer Function ---

Transfer function:      -99.6727      transfer
vin#Input_impedance:    1e+020      impedance
output impedance at V(vx) : 344394  impedance
```

4.5



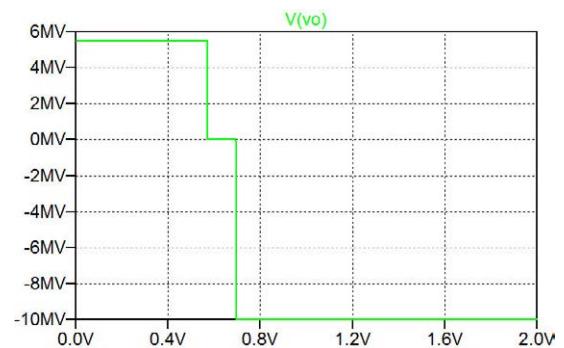
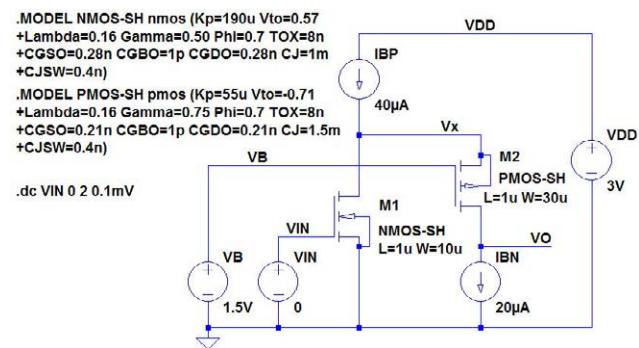
$L_1 = L_2 = 1 \mu\text{m}$, $W_1 = 10 \mu\text{m}$, $W_2 = 30 \mu\text{m}$
 $I_{BP} = 40 \mu\text{A}$, $I_{BN} = 20 \mu\text{A}$, $V_B = 1.5 \text{ V}$, $V_{DD} = 3 \text{ V}$.
.MODEL PMOS-SH pmos (Kp=55u Vto=-0.71
+Lambda=0.16 Gamma=0.75 Phi=0.7 TOX=8n
+CGSO=0.21n CGBO=1p CGDO=0.28n CJ=1.5m
+CJSW=0.4n)

Figure P4.5

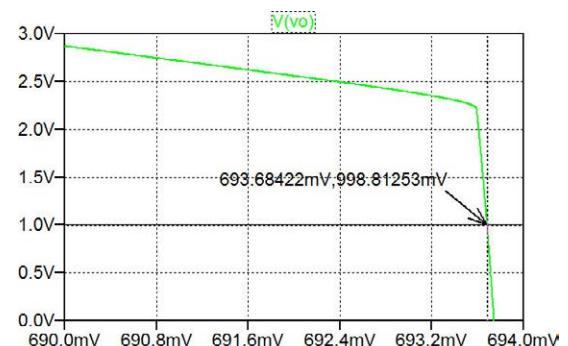
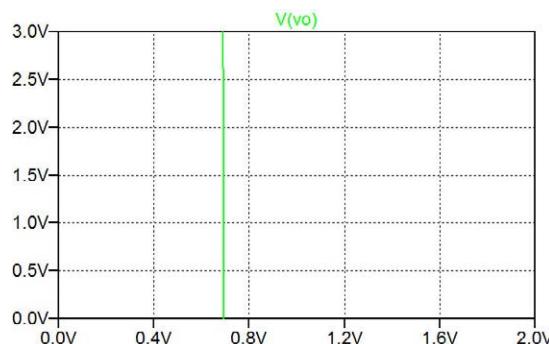
For the folded cascode shown in Fig. P4.5, find the bias value of V_{IN} required to give an output voltage of 1 V. Also find the small-signal gain A_{voc} and output resistance r_o at low frequencies. Find the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1 . Assume transistor models as shown in Figs. P4.4 and P4.5.

Solution:

The figure below shows the folded-cascode stage with a specification for a ‘.dc’ simulation. Also shown is the resulting plot of the output voltage. Apparently, the simulation generates unrealistically high output voltages, several MV. This is due to the biasing by two ideal dc current sources. You may also notice that the simulation time is quite long, and examining the error log file, you find that LTspice has some challenges in finding the operating points for the values of input voltage giving unrealistic values of output voltage.



In order to see $V_{(vo)}$ in a realistic range of output voltages, we set the range of the y-axis to 3 V, either by the command ‘Plot Settings → Manual Limits’ or by moving the cursor to the y-axis and using a right-click on the mouse. The resulting plot is shown below, left plot. We see that the output voltage changes abruptly for an input voltage of about 0.7 V. Even when zooming in on a small part of the plot, it is difficult to find the value of V_{IN} resulting in an output voltage of 1 V, so in order to improve the accuracy, we run a ‘.dc’ simulation from 690 mV to 694 mV with a step size of 1 μ V. From this, we find $V_{IN} = 693.684$ mV.



Sharp Minds - Bright Ideas!

Employees at FOSS Analytical A/S are living proof of the company value - First - using new inventions to make dedicated solutions for our customers. With sharp minds and cross functional teamwork, we constantly strive to develop new unique products - Would you like to join our team?

FOSS works diligently with innovation and development as basis for its growth. It is reflected in the fact that more than 200 of the 1200 employees in FOSS work with Research & Development in Scandinavia and USA. Engineers at FOSS work in production, development and marketing, within a wide range of different fields, i.e. Chemistry, Electronics, Mechanics, Software, Optics, Microbiology, Chemometrics.

We offer

A challenging job in an international and innovative company that is leading in its field. You will get the opportunity to work with the most advanced technology together with highly skilled colleagues.

Read more about FOSS at www.foss.dk - or go directly to our student site www.foss.dk/sharpminds where you can learn more about your possibilities of working together with us on projects, your thesis etc.

FOSS

The Family owned FOSS group is the world leader as supplier of dedicated, high-tech analytical solutions which measure and control the quality and production of agricultural, food, pharmaceutical and chemical products. Main activities are initiated from Denmark, Sweden and USA with headquarters domiciled in Hillerød, DK. The products are marketed globally by 23 sales companies and an extensive net of distributors. In line with the corevalue to be 'First', the company intends to expand its market position.



Dedicated Analytical Solutions

FOSS
Slangerupgade 69
3400 Hillerød
Tel. +45 70103370

www.foss.dk



In order to verify the bias point, we run a ‘.op’ simulation with a dc value of V_{IN} specified to 693.684 mV. The output file from this is shown below, and we see that $V(v_o)$ is sufficiently close to 1 V, and also the voltage at the intermediate node x has a reasonable value within the supply voltage range.

```
--- Operating Point ---

V(vx) :      2.3512      voltage
V(vin) :     0.693684    voltage
V(vdd) :      3          voltage
V(vb) :      1.5         voltage
V(vo) :     1.00213     voltage
```

With the bias point in place, the small-signal gain A_{voc} and output resistance r_o at low frequencies are found from a ‘.tf’ simulation with $V(VO)$ as the output and VIN as the source. The output file from this ‘.tf’ simulation is shown below. From this, we find a gain of -15109 V/V or 84 dB and an output resistance of $47\text{ M}\Omega$.

```
--- Transfer Function ---

Transfer function:      -15108.9      transfer
vin#Input impedance:   1e+020       impedance
output impedance at V(vo) : 4.70983e+007  impedance
```

For finding the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1 , we run a ‘.tf’ simulation with $V(Vx)$ as the output and VIN as the source. The output file from this ‘.tf’ simulation is shown below. From this, we find a resistance r_x of $430\text{ k}\Omega$.

```
--- Transfer Function ---

Transfer function:      -139.083      transfer
vin#Input impedance:   1e+020       impedance
output impedance at V(vx) : 430060      impedance
```

4.6

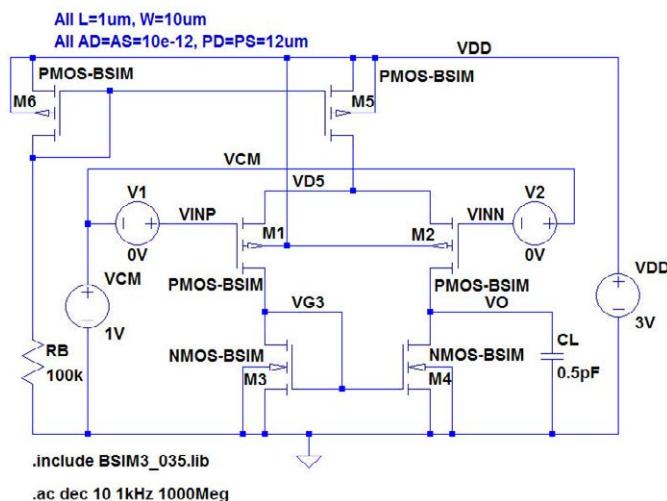
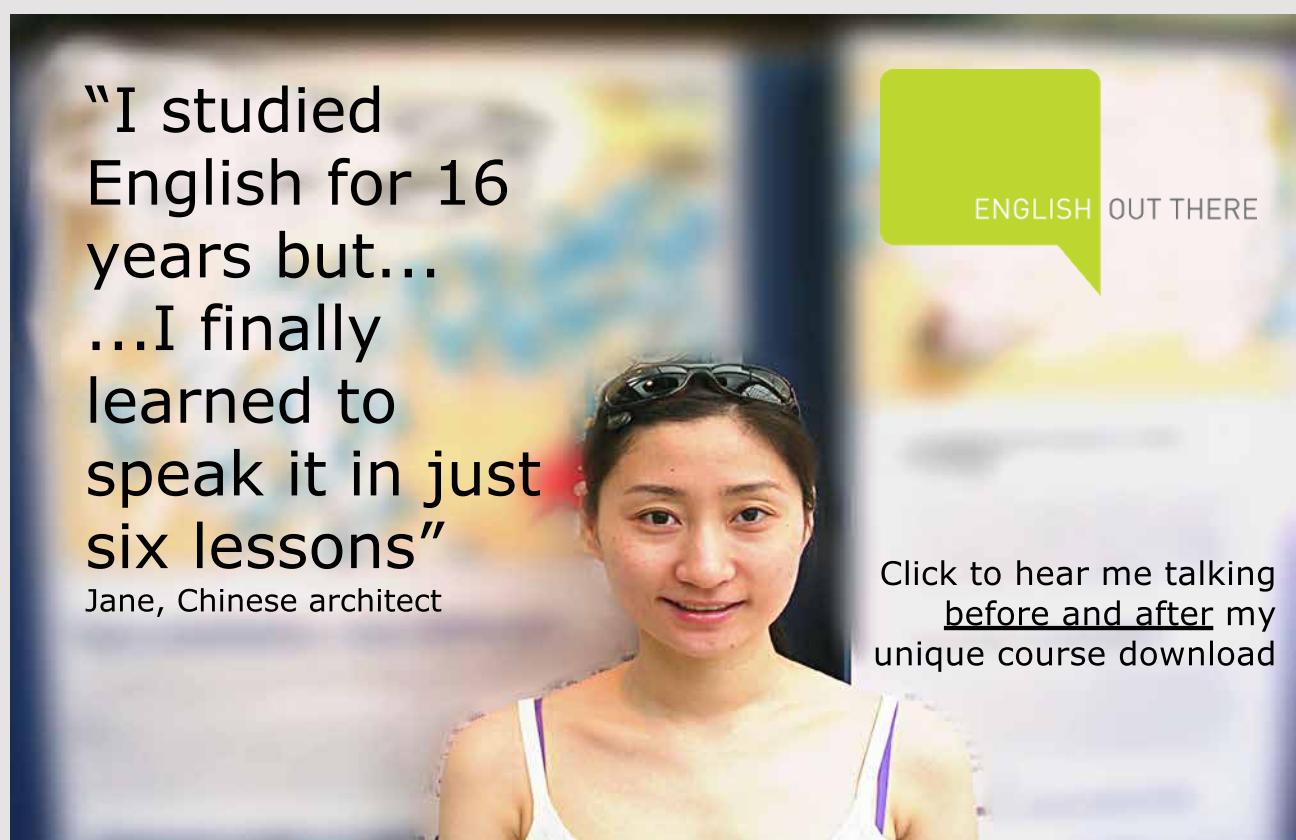


Figure P4.6

Figure P4.6 shows an alternative version of the LTspice schematic from Fig. 4.23 with a different arrangement for the input voltages. Define the ac amplitudes of ‘VCM’, ‘V1’, ‘V2’ and ‘VDD’ such that the ‘.ac’ simulation shows the differential gain and compare your simulation to Fig. 4.27. Next, define the ac amplitudes of ‘VCM’, ‘V1’, ‘V2’ and ‘VDD’ such that the ‘.ac’ simulation shows the common-mode gain and compare your simulation to Fig. 4.28. Finally, define the ac amplitudes of ‘VCM’, ‘V1’, ‘V2’ and ‘VDD’ such that the ‘.ac’ simulation shows the power-supply rejection and compare your simulation to Fig. 4.29.



For convenience, Fig. 4.23 is shown below.

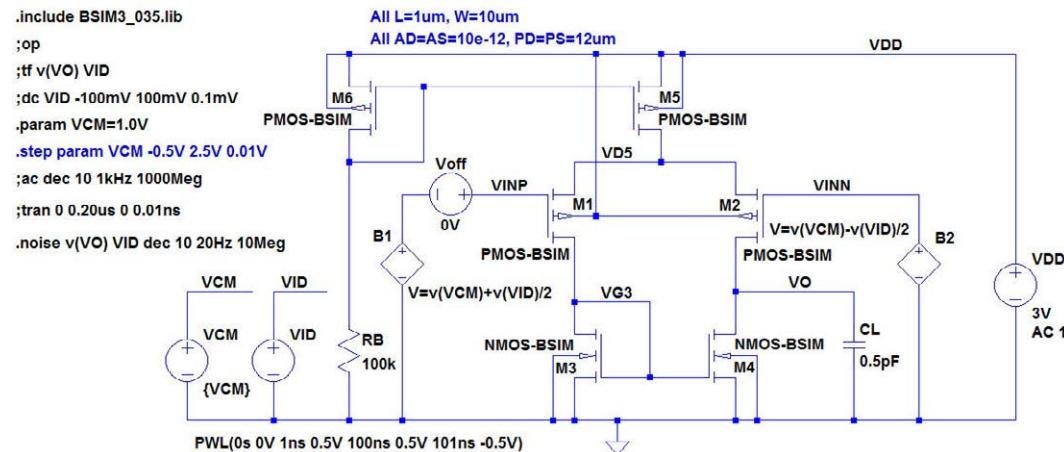


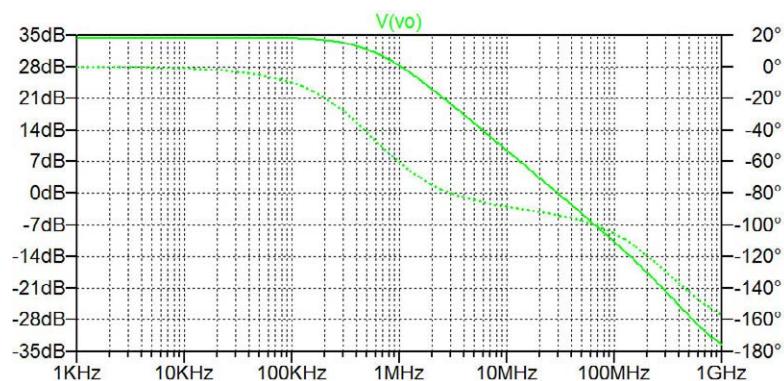
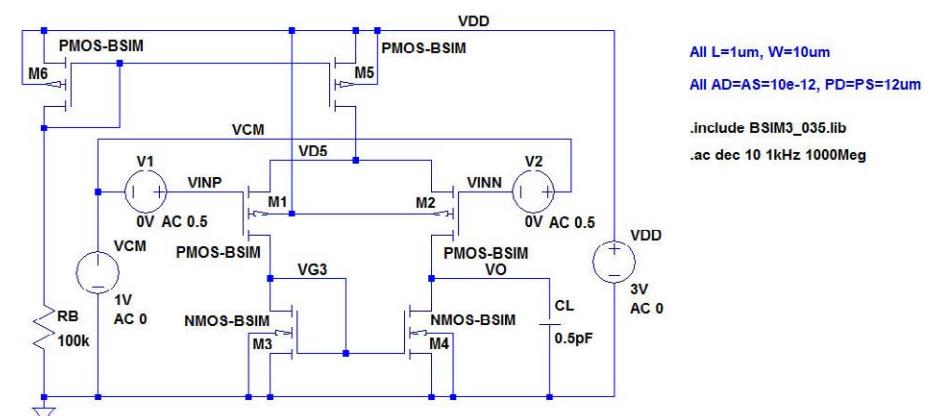
Figure 4.23: LTspice schematic for simulations of a PMOS differential pair with NMOS active load.

Solution:

For the differential gain, we define the ac amplitudes in Fig. P4.6 as follows:

VCM: AC Amplitude = 0, V1: AC Amplitude = 0.5, V2: AC Amplitude = 0.5, VDD: AC Amplitude = 0.

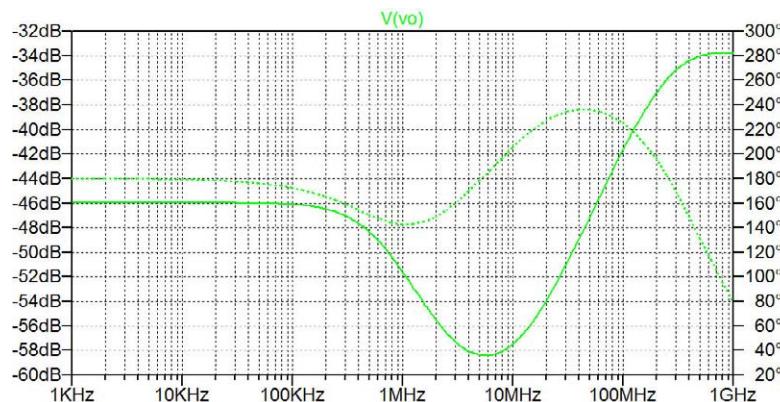
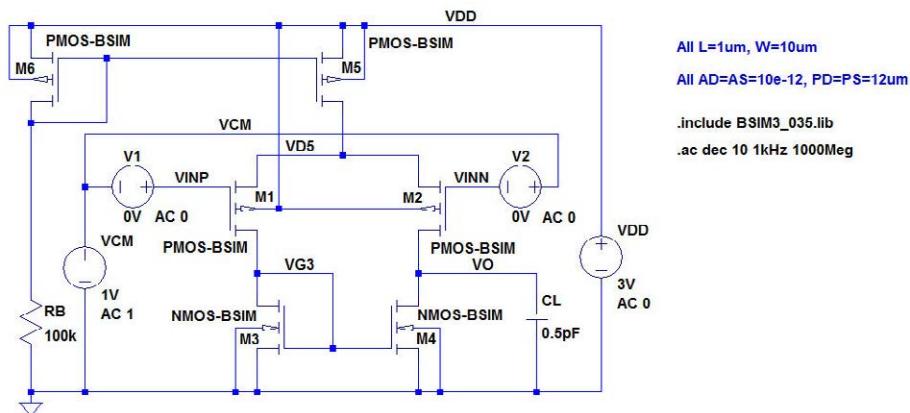
The resulting schematic and simulation plot is shown below. The simulation plot is identical to Fig. 4.27 in ‘CMOS Integrated Circuit Simulation with LTspice’.



For the common-mode gain, we define the ac amplitudes in Fig. P4.6 as follows:

VCM: AC Amplitude = 1, V1: AC Amplitude = 0, V2: AC Amplitude = 0, VDD: AC Amplitude = 0.

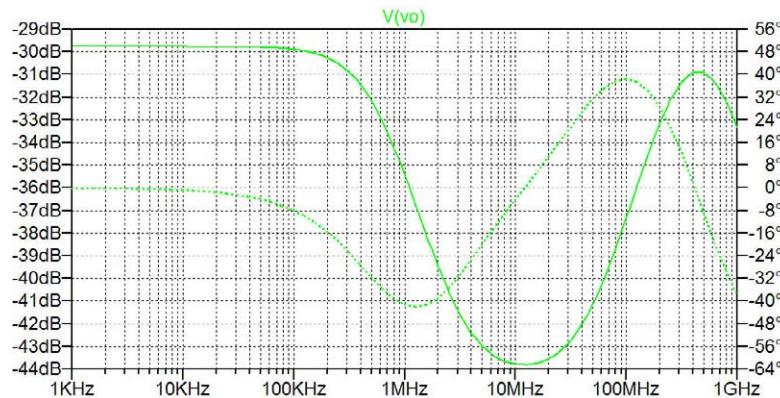
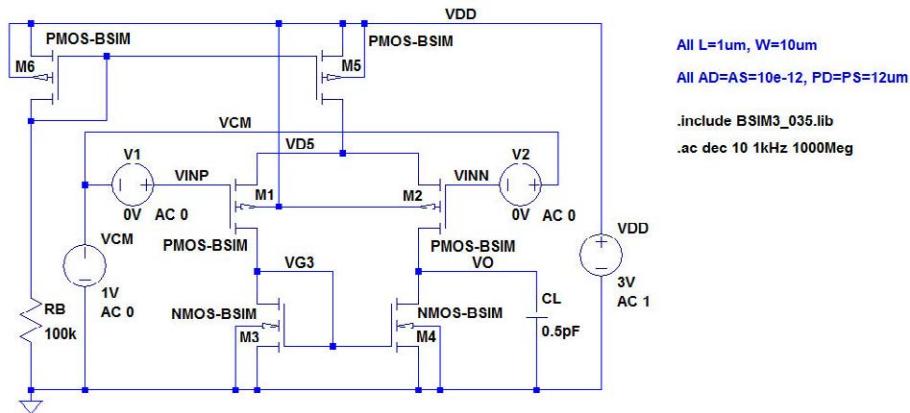
The resulting schematic and simulation plot is shown below. The simulation plot is identical to Fig. 4.28 in ‘CMOS Integrated Circuit Simulation with LTspice’.



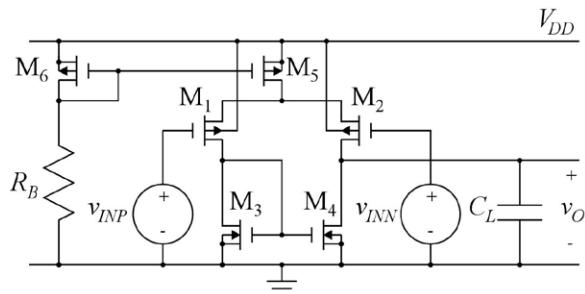
For the power supply rejection, we define the ac amplitudes in Fig. P4.6 as follows:

VCM: AC Amplitude = 0, V1: AC Amplitude = 0, V2: AC Amplitude = 0, VDD: AC Amplitude = 1.

The resulting schematic and simulation plot is shown below. The simulation plot is identical to Fig. 4.29 in ‘CMOS Integrated Circuit Simulation with LTspice’.



4.7



$$L_1 = L_2 = L_3 = L_4 = L_5 = 1 \mu\text{m}$$

$$W_1 = 30 \mu\text{m}, W_2 = 33 \mu\text{m}, W_3 = W_4 = W_5 = W_6 = 10 \mu\text{m}$$

$$AD_1 = AS_1 = AD_2 = AS_2 = 30 (\mu\text{m})^2$$

$$AD_3 = AS_3 = AD_4 = AS_4 = AD_5 = AS_5 = AD_6 = AS_6 = 10 (\mu\text{m})^2$$

$$PD_1 = PS_1 = PD_2 = PS_2 = 32 \mu\text{m}$$

$$PD_3 = PS_3 = PD_4 = PS_4 = PD_5 = PS_5 = PD_6 = PS_6 = 12 \mu\text{m}$$

$$R_B = 100 \text{ k}\Omega, C_L = 0.5 \text{ pF}, V_{DD} = 3.0 \text{ V}, V_{CM} = 1 \text{ V}$$

Figure P4.7

For the differential pair shown in Fig. P4.7, we assume that a layout error has resulted in a mismatch between M_1 and M_2 such that $W_1 = 30 \mu\text{m}$ and $W_2 = 33 \mu\text{m}$. Find the input offset voltage caused by this error for a common-mode input voltage of $V_{CM} = 1 \text{ V}$ and an output voltage of 0.7 V. Use the Shichman-Hodges transistor model from Figs. P4.4 and P4.5. Next, plot the differential gain and the common-mode gain versus frequency. Find the gain-bandwidth product and calculate the common-mode rejection ratio at low frequencies. Also plot the gain from the power-supply to the output and calculate the power-supply rejection ratio at low frequencies.

Figures P4.4 and P4.5 are shown on page 65 and 68, respectively, in this book.

The Wake

the only emission we want to leave behind

Low-speed Engines Medium-speed Engines Turbochargers Propellers Propulsion Packages PrimeServ

The design of eco-friendly marine power and propulsion solutions is crucial for MAN Diesel & Turbo. Power competencies are offered with the world's largest engine programme – having outputs spanning from 450 to 87,220 kW per engine. Get up front! Find out more at www.mandieselturbo.com

Engineering the Future – since 1758.
MAN Diesel & Turbo

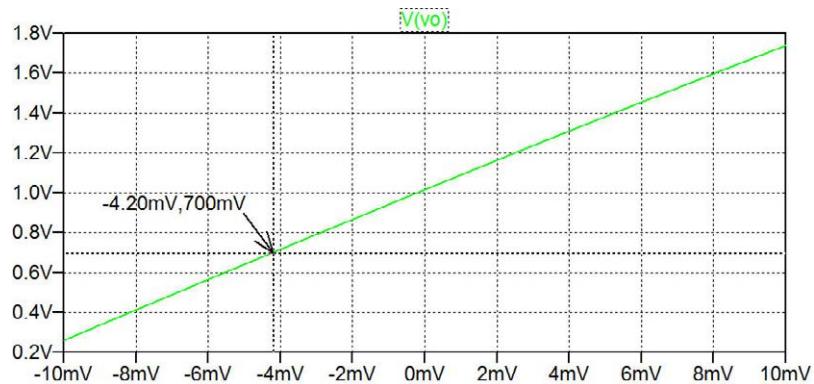
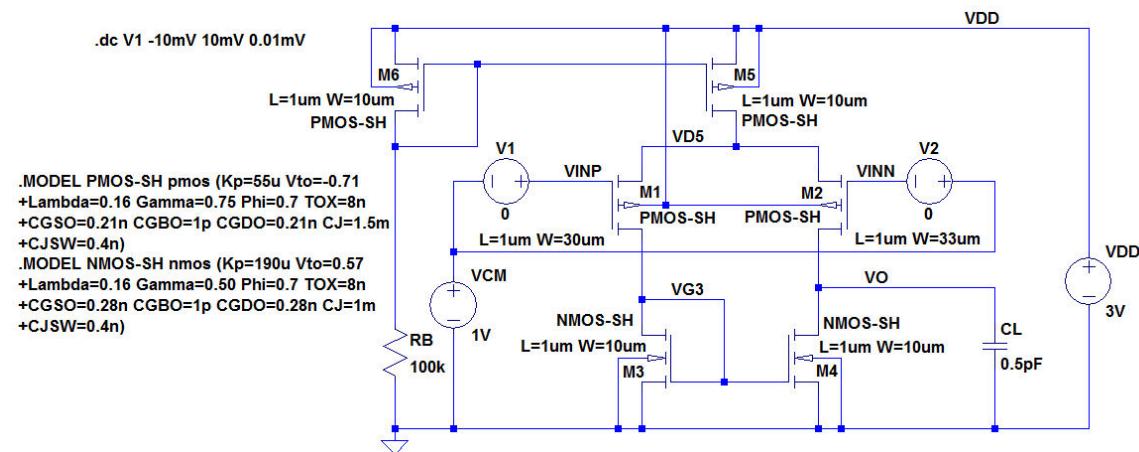




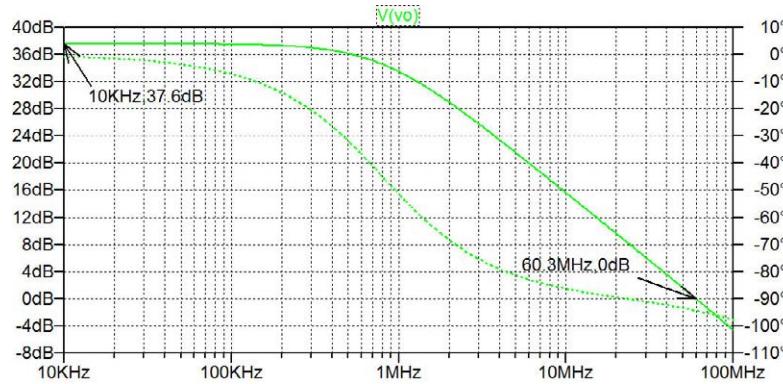
Click on the ad to read more

Solution:

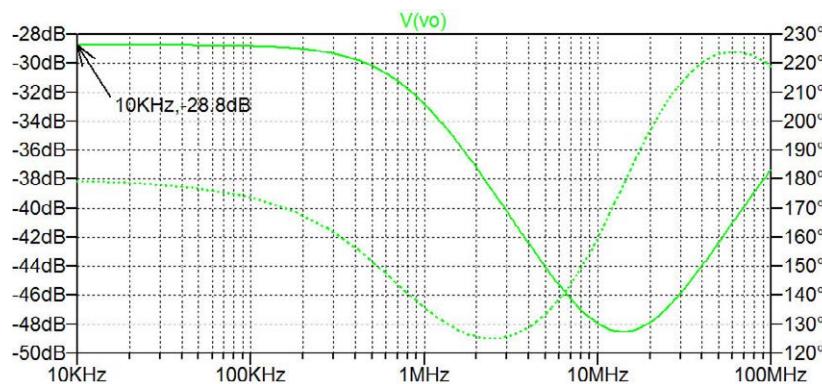
The figure below shows the schematic in LTspice. For finding the offset voltage, we use a ‘.dc’ simulation with the input voltage V_1 to the noninverting input as the source to sweep. From the simulation plot below, we find that a dc input voltage of -4.2 mV results in an output voltage of 0.7 V. Thus, $V_{off} = -4.2$ mV.



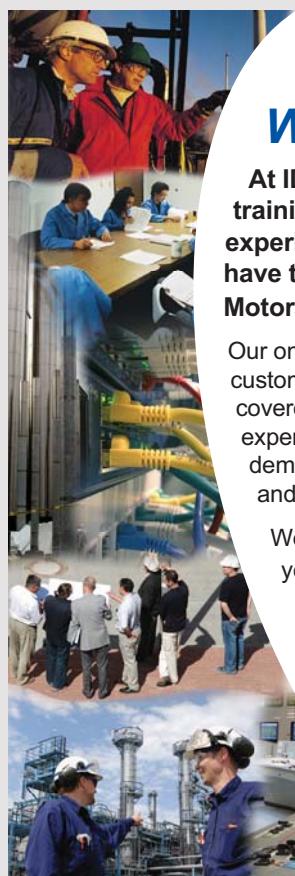
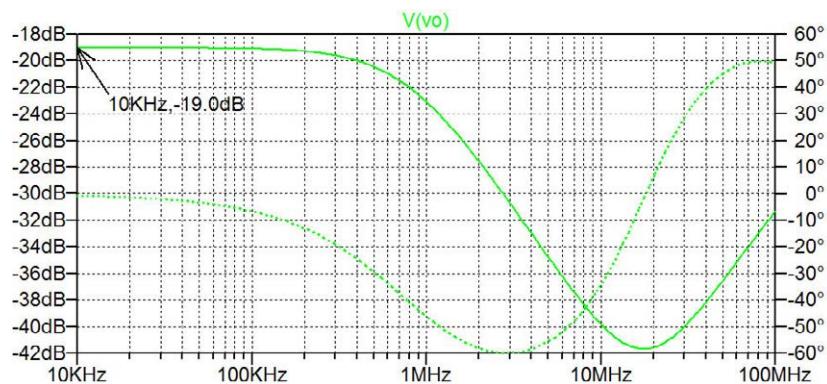
For finding the differential gain, we specify a dc value of -4.2 mV for V1 and an ac amplitude of 0.5 V for both V1 and V2 in the schematic on the previous page. We use a ‘.ac’ simulation with a start frequency of 10 kHz and a stop frequency of 100 MHz: ‘.ac oct 10 10k 100Meg’. This results in the output plot below where we find the differential low-frequency gain to be 37.6 dB and the gain-bandwidth product to be 60.3 MHz.



For finding the common-mode gain, we specify a dc value of -4.2 mV for V1 and an ac amplitude of 0 V for both V1 and V2 in the schematic on the previous page. Also, we specify an ac amplitude of 1 V for VCM. We use a ‘.ac’ simulation with a start frequency of 10 kHz and a stop frequency of 100 MHz: ‘.ac oct 10 10k 100Meg’. This results in the output plot below where we find the common-mode low-frequency gain to be -28.8 dB, so the common-mode rejection ratio is $\text{CMRR} = 37.6 \text{ dB} + 28.8 \text{ dB} = 66.4 \text{ dB}$.



For finding the power supply rejection, we specify a dc value of -4.2 mV for V₁ and an ac amplitude of 0 V for both V₁, V₂ and V_{CM}. Also, we specify an ac amplitude of 1 V for V_{DD}. We use a ‘.ac’ simulation with a start frequency of 10 kHz and a stop frequency of 100 MHz: ‘.ac oct 10 10k 100Meg’. This results in the output plot below where we find the power supply rejection at low frequency to be 19.0 dB, so the power supply rejection ratio is PSRR = 37.6 dB + 19.0 dB = 56.6 dB



Technical training on *WHAT* you need, *WHEN* you need it

At IDC Technologies we can tailor our technical and engineering training workshops to suit your needs. We have extensive experience in training technical and engineering staff and have trained people in organisations such as General Motors, Shell, Siemens, BHP and Honeywell to name a few.

Our onsite training is cost effective, convenient and completely customisable to the technical and engineering areas you want covered. Our workshops are all comprehensive hands-on learning experiences with ample time given to practical sessions and demonstrations. We communicate well to ensure that workshop content and timing match the knowledge, skills, and abilities of the participants.

We run onsite training all year round and hold the workshops on your premises or a venue of your choice for your convenience.

For a no obligation proposal, contact us today
at training@idc-online.com or visit our website
for more information: www.idc-online.com/onsite/

Phone: +61 8 9321 1702
Email: training@idc-online.com
Website: www.idc-online.com

OIL & GAS
ENGINEERING

ELECTRONICS

AUTOMATION &
PROCESS CONTROL

MECHANICAL
ENGINEERING

INDUSTRIAL
DATA COMMS

ELECTRICAL
POWER



4.8

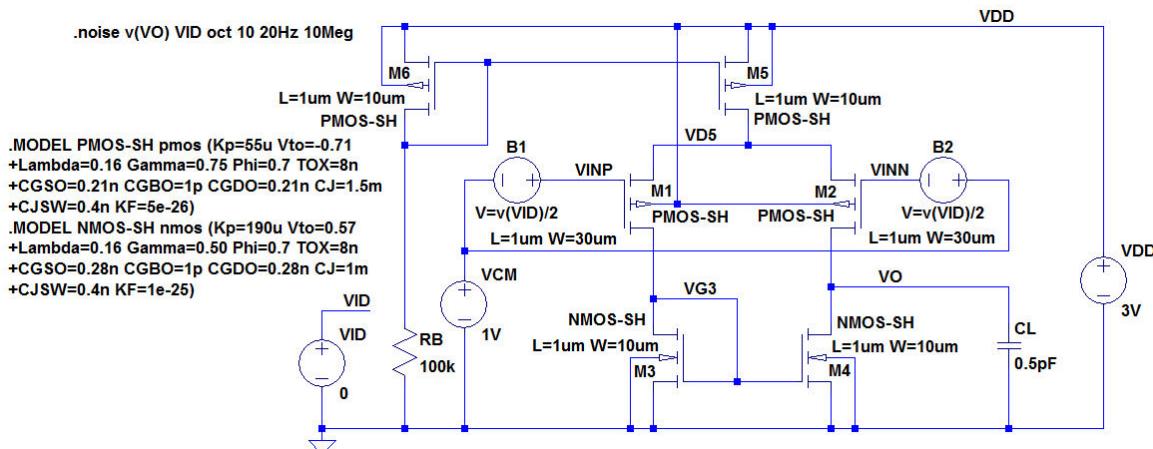
```
.MODEL PMOS-SH pmos (Kp=55u Vto=-0.71
+Lambda=0.16 Gamma=0.75 Phi=0.7 TOX=8n
+CGSO=0.21n CGBO=1p CGDO=0.21n CJ=1.5m
+CJSW=0.4n KF=5e-26)
.MODEL NMOS-SH nmos (Kp=190u Vto=0.57
+Lambda=0.16 Gamma=0.50 Phi=0.7 TOX=8n
+CGSO=0.28n CGBO=1p CGDO=0.28n CJ=1m
+CJSW=0.4n KF=1e-25)
```

Figure P4.8

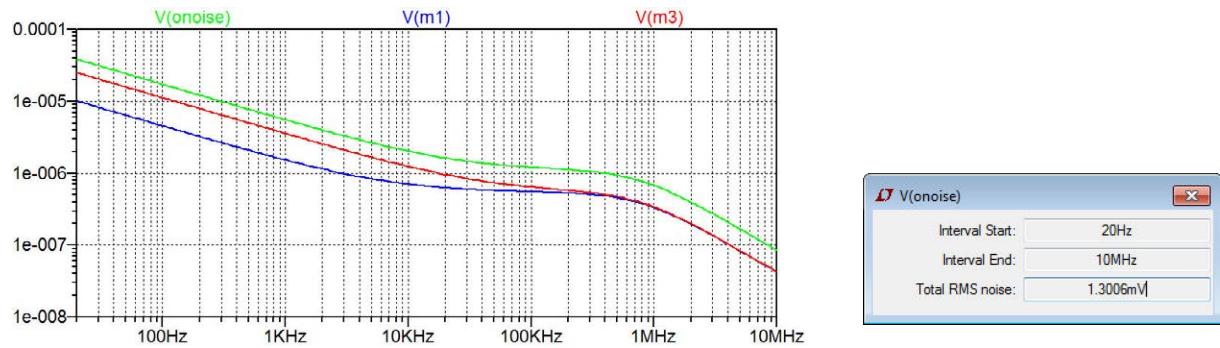
For the differential pair shown in Fig. P4.7 with $W_1 = W_2 = 30 \mu\text{m}$, assume the transistor models shown in Fig. P4.8 which include parameters for the flicker noise modeling. Plot the total noise spectral density of the output voltage and the noise contributions from M_1 and M_3 in the frequency range 20 kHz to 10 MHz, using logarithmic axes. Find the total RMS output noise voltage in this frequency range. Also plot the input referred noise spectral density and find the total RMS input referred noise voltage in this frequency range.

Solution:

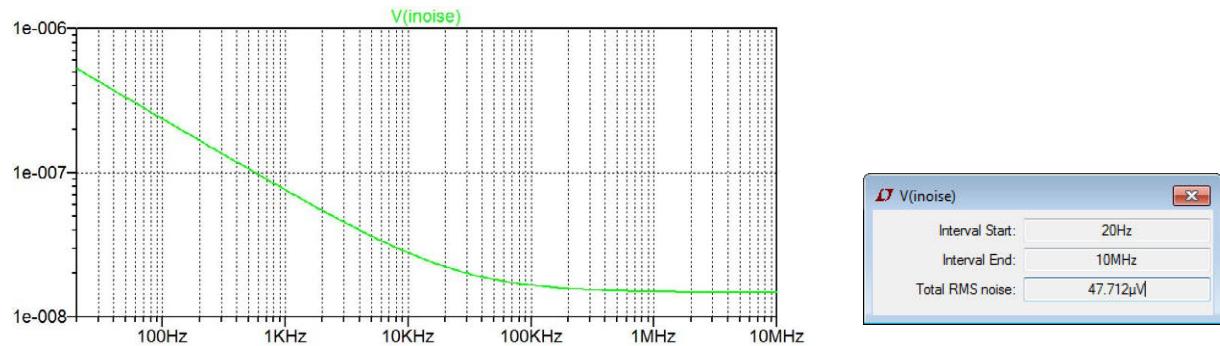
The figure below shows the schematic in LTspice. For finding the noise voltage, we use a ‘.noise’ simulation with VID as the input and $v(\text{VO})$ as the output.



When plotting the noise contribution, remember to change the y-axis to logarithmic scale and use reasonable top and bottom limits. The output voltage is selected by pointing to the output node. The noise contributions from transistors M_1 and M_3 are selected by pointing to the transistors. The total output noise voltage is found by pointing to the green label ‘ $V(\text{onoise})$ ’ above the plot and using a ‘Ctrl-left-click’. This opens the information window shown below, and we find $V_{on(\text{rms})} = 1.3 \text{ mV}$.

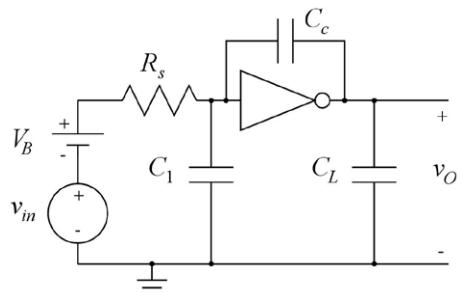


The input referred spectral noise density is selected in the plot window by the command ‘Plot Settings → Visible Traces’ and is shown below together with the information window resulting from a ‘Ctrl-left-click’ on the label above the plot. We find a total equivalent input noise of $V_{in(\text{rms})} = 48 \mu\text{V}$.



Tutorial 5 – Hierarchical Design

5.1



$R_s = 1 \text{ M}\Omega$, $V_{DD} = 3 \text{ V}$,
 $C_1 = 0.2 \text{ pF}$, $C_c = 0.7 \text{ pF}$, $C_L = 1.5 \text{ pF}$.

Figure P5.1

An inverter as shown in Fig. 5.25 on page 181 may be used as an inverting amplifier. Design a test bench as shown in Fig. P5.1 using a supply voltage of 3 V, a minimum length of ‘Lmin=0.35μ’, a fanout of ‘Fanout=1’ and the BSIM3 transistor model from Fig. 3.10 on page 86. Find an input bias voltage V_B which gives an output bias voltage of 1.5 V. With this value of V_B , simulate the ac response and find the dominant pole. Also, use the Miller approximation (Chan Carusone, Johns & Martin 2012) to calculate the dominant pole and compare to the simulated value.

gaiteye®
Challenge the way we run

EXPERIENCE THE POWER OF FULL ENGAGEMENT...

**RUN FASTER.
RUN LONGER..
RUN EASIER...**

**READ MORE & PRE-ORDER TODAY
WWW.GAITEYE.COM**

For convenience, Figs. 5.25 and 3.10 are shown below.

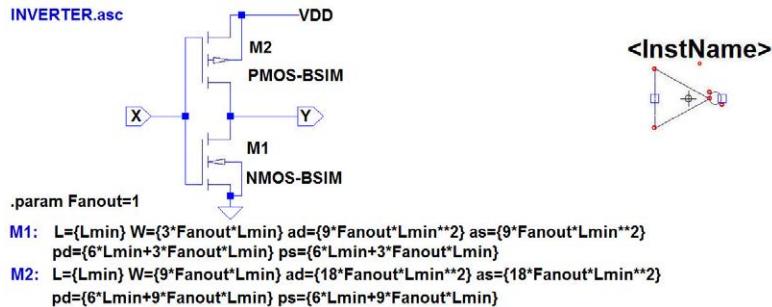


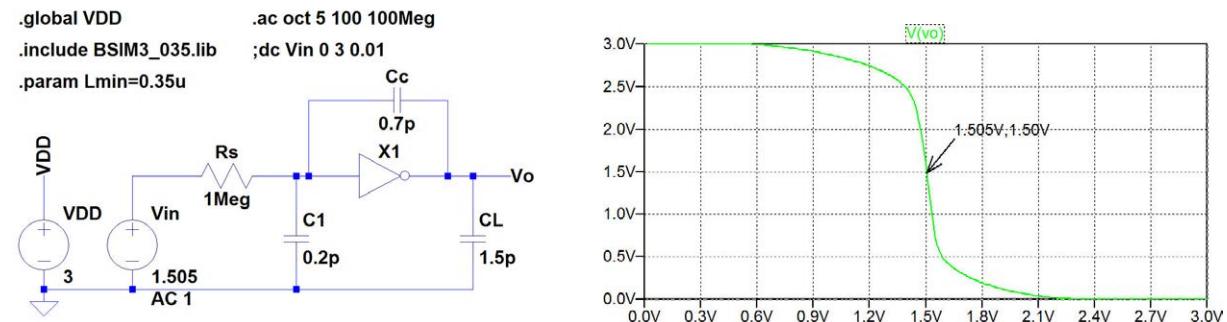
Figure 5.25: Inverter, schematic and symbol.

Generic BSIM3 model for 0.35 μm CMOS process. Adapted from (Carusone, Johns & Martin 2014).	
<pre> *BSIM3_035.lib .MODEL NMOS-BSIM NMOS LEVEL = 49 +VERSION = 3.1 TNOM = 27 TOX = 7.8E-9 +XJ = 1E-07 NCH = 2.18E+17 VTH0 = 0.48 +K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01 +K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07 +DVT0W = 0 DVT1W = 0 DVT2W = 0 +DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01 +U0 = 360 UA = -8.48E-10 UB = 2.27E-18 +UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00 +AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06 +KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01 +RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02 +WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10 +DWG = -4.27E-09 +DWB = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00 +CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00 +CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01 +DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04 +PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-04 +PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02 +DELTA = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1 +PRT = 0 UTE = -1.5 KT1 = -1.11E-01 +KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09 +UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04 +WL = 0 WLN = 9.95E-01 WW = 0 +WWN = 1.00E+00 WWL = 0 LL = 0 +LLN = 1 LW = 0 LWN = 1 +LWL = 0 CAPMOD = 2 XPART = 0.5 +CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12 +CJ = 9e-4 PB = 7.95E-01 MJ = 3.53E-01 +CJSW = 2.8e-10 PBSW = 7.98E-01 MJSW = 1.73E-01 +CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01 +CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01 +PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03 </pre>	<pre> .MODEL PMOS-BSIM PMOS LEVEL = 49 +VERSION = 3.1 TNOM = 2.69E+01 TOX = 7.8E-9 +XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = -0.6 +K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01 +K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07 +DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0 +DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01 +U0 = 150 UA = 1E-10 UB = 1.75E-18 +UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00 +AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06 +KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00 +RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03 +WR = 1 WINT = 1.47E-07 LINT = 1.04E-10 +DWG = -1.09E-08 +DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00 +CIT = 0 CDSC = 2.40E-04 CDSCD = 0 +CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03 +DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03 +PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04 +PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15 +DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1 +PRT = 0 UTE = -1.5 KT1 = -1.09E-01 +KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09 +UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04 +WL = 0 WLN = 1 WW = 0 +WWN = 1.00E+00 WWL = 0 LL = 0 +LLN = 1 LW = 0 LWN = 1 +LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5 +CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12 +CJ = 14e-4 PB = 9.83E-01 MJ = 5.79E-01 +CJSW = 3.2e-10 PBSW = 9.92E-01 MJSW = 3.60E-01 +CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01 +CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01 +PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03 </pre>

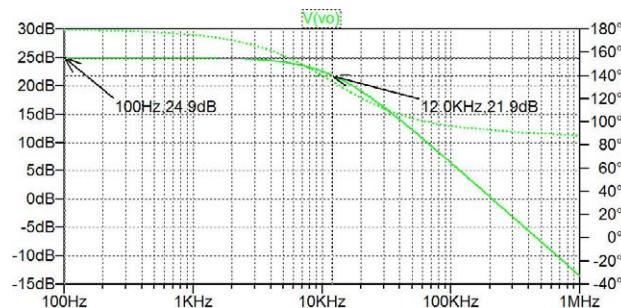
Figure 3.10: Library file with BSIM3 models for a generic 0.35 μm CMOS process, adapted from (Chan Carusone, Johns & Martin 2014).

Solution:

The figure below shows the schematic drawn in LTspice. For finding the bias input voltage, we run a ‘.dc’ simulation, the result of which is also shown below. From this, we find that a bias voltage of $V_B = 1.505$ V results in an output voltage of 1.5 V.



With 1.505 V inserted as the dc value for V_{in} , we run a ‘.ac’ simulation from which we find a low-frequency gain of 24.9 dB (or $A_v = -17.6$ V/V) and a dominant pole of 12 kHz, see simulation plot below.



A calculation of the dominant gives $f_p = (2\pi R_s ((1 - A_v) C_c + C_1))^{-1} = 12$ kHz.

5.2

$$A_v(s) = \frac{\omega_{ta}(1 - s/\omega_z)}{s(1 + s/\omega_{p2})}$$

$$\omega_{ta} = 2\pi \times 120 \text{ MHz},$$

$$\omega_z = 2\pi \times 200 \text{ MHz},$$

$$\omega_{p2} = 2\pi \times 76 \text{ MHz}.$$

Figure P5.2

Simulate the ac response of the closed-loop gain and the loop gain for the opamp shown in Figs. 5.10 and 5.11 with $C_1 = 1 \text{ pF}$, $C_2 = 0.2 \text{ pF}$ and $C_L = 1.5 \text{ pF}$ using the generic filter blocks from Table 5.3. Assume a transfer function for the opamp as specified in Fig. P5.2.

Find the phase margin and the closed-loop bandwidth and compare to the results found in Example 5.2.

For convenience, Figs. 5.10, 5.11 and Table 5.3 are shown on the next page.

I joined MITAS because
I wanted **real responsibility**

The Graduate Programme
for Engineers and Geoscientists
www.discovermitas.com

Month 16

I was a construction supervisor in the North Sea advising and helping foremen solve problems

Real work
International opportunities
Three work placements

www.discovermitas.com

MAERSK

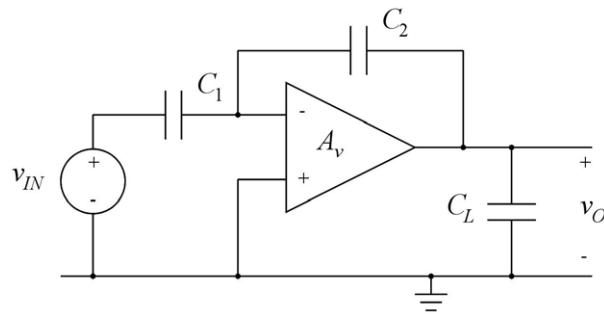


Figure 5.10: Inverting opamp configuration with capacitive feedback.

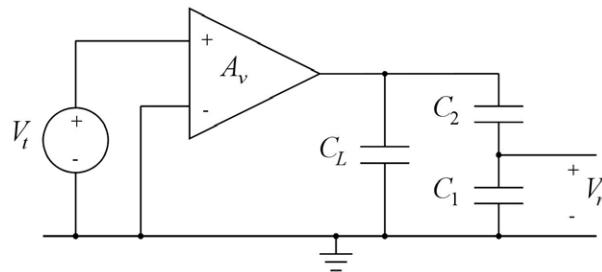


Figure 5.11: Open loop circuit for finding the loop gain $L(s) = V_r(s)/V_t(s)$.

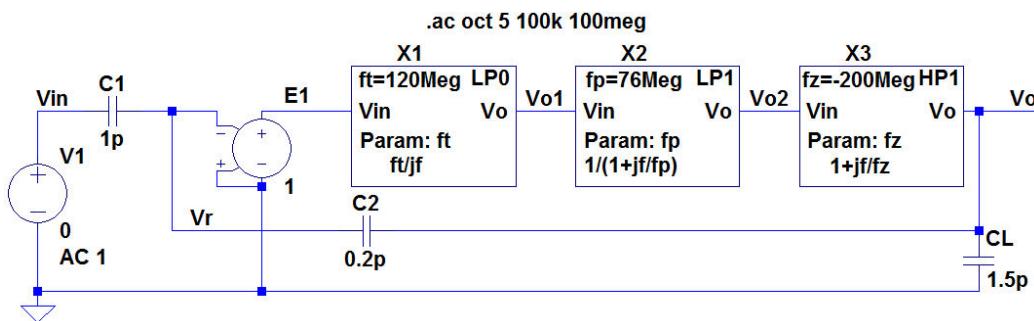
Transfer function	Schematic	Symbol	Parameter
Zero in 0 $T(jf) = jf/f_t$			Unity-gain frequency f_t
Real zero $T(jf) = 1 + jf/f_z$			Zero frequency f_z
Pole in 0 $T(jf) = f_t/(jf)$			Unity-gain frequency f_t
Real pole $T(jf) = \frac{1}{1+jf/f_p}$			Pole frequency f_p
Biquad $T(jf) = \frac{1}{(jf)^2 + (jf)f_0/Q + f_0^2}$			Resonance frequency f_0 and quality factor Q

Table 5.3: Generic filter blocks defined as subcircuits.

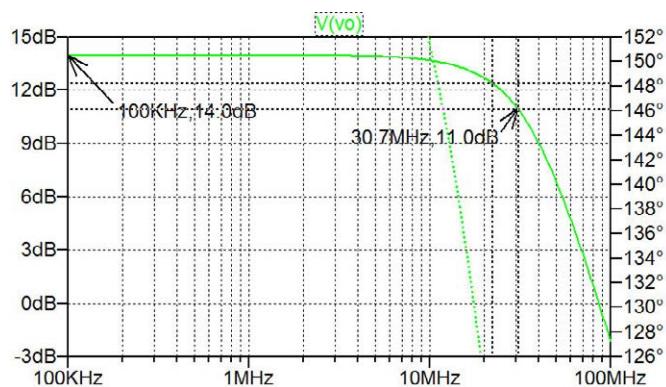
Solution:

The opamp transfer function comprises a factor with a pole in 0, a factor with a real pole and a factor with a real zero. The corresponding filter blocks from Table 5.3 in ‘CMOS Integrated Circuit Simulation with LTspice’ are LP0, LP1 and HP1.

The figure below shows the LTspice schematic corresponding to Fig. 5.10 with these filter blocks inserted for the opamp and with parameters as specified in Fig. P5.2. Note that the filter block HP1 has a right half plane zero, so the parameter fz must be specified as a negative frequency. In order to provide an inverting input for the opamp, an inversion is obtained from the voltage controlled voltage source E1.



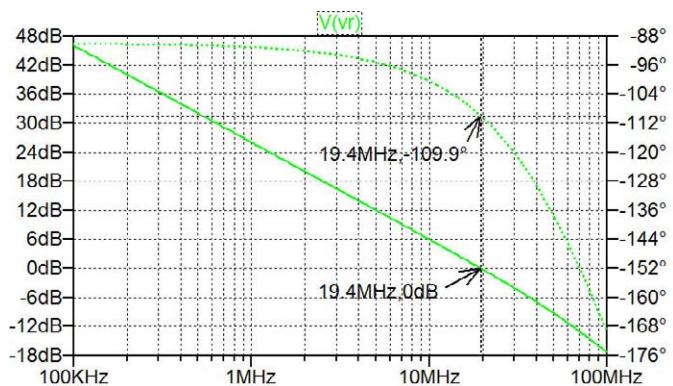
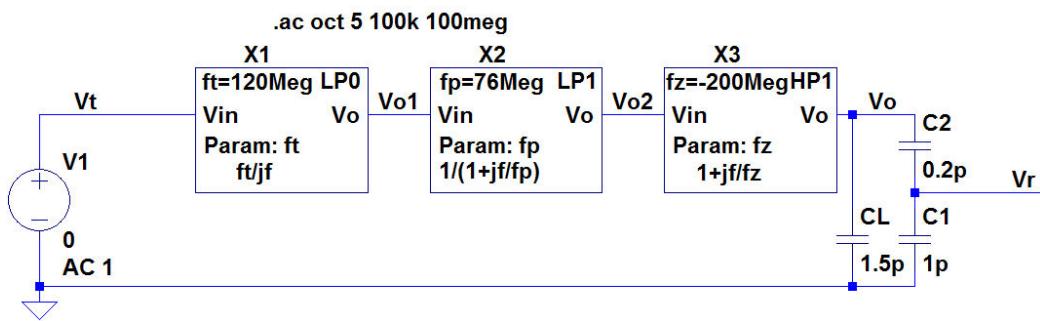
For finding the closed-loop ac response, we run a ‘.ac’ simulation and the result of this is shown below. From the plot, we find a closed-loop bandwidth of 30.7 MHz. This is higher than the bandwidth found in Example 5.2 because higher order poles and zeros are neglected when using the opamp transfer function specified in Fig. P5.2.



The figure on the next page shows the LTspice schematic corresponding to Fig. 5.11.

For finding the loop gain ac response, we run a ‘.ac’ simulation, and the result of this is also shown on the next page. From the plot, we find a phase margin of $180.0^\circ - 109.9^\circ = 70.1^\circ$. This is more than the phase margin found in Example 5.2 because higher order poles and zeros are neglected when using the opamp transfer function specified in Fig. P5.2.

If you open the error log file after the simulations, you will notice some warnings about floating nodes. However, since LTspice assumes a bias voltage of 0 V for these floating nodes, the simulations are not compromised.



5.3

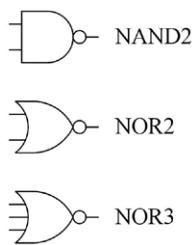


Figure P5.3

Design subcircuits for a two-input NAND gate and two-input and three-input NOR gates similar to the logic gate and inverter designs shown in Example 5.4. Scale the PMOS transistors relative to the NMOS transistors to compensate for the difference in electron mobility and hole mobility, assuming $\mu_n = 3\mu_p$. Use the BSIM3 transistor models from Fig. 3.10 on page 86 with a channel length of $L_{min} = 0.35 \mu m$ and a minimum channel width of $3L_{min}$ for NMOS transistors and $9L_{min}$ for PMOS transistors.

What are the transistor channel widths used for the gates?

For convenience, Fig. 3.10 is shown on page 82 in this book.

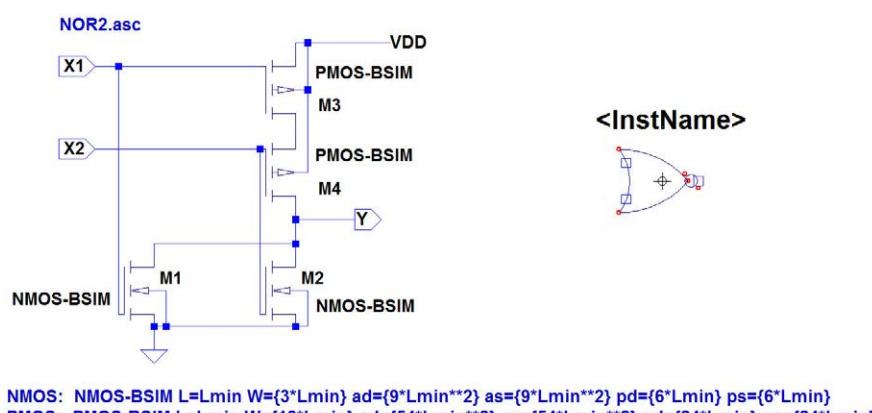
Solution:

The figures below and on the next page show the schematics and symbols for each of the gates NOR2, NOR3 and NAND2. In order to compensate for the difference in hole mobility and electron mobility, the channel widths have been selected as follows:

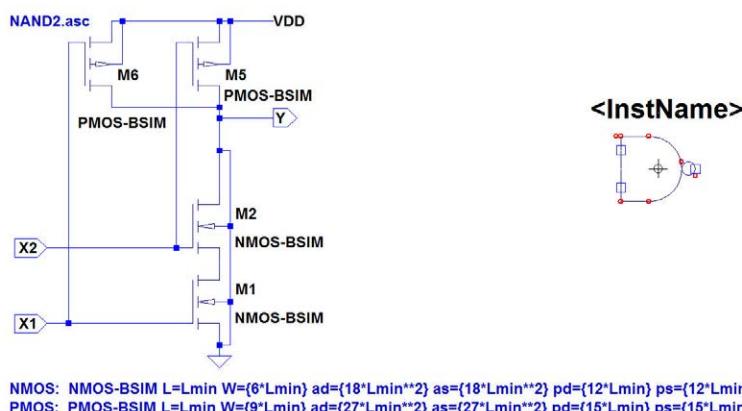
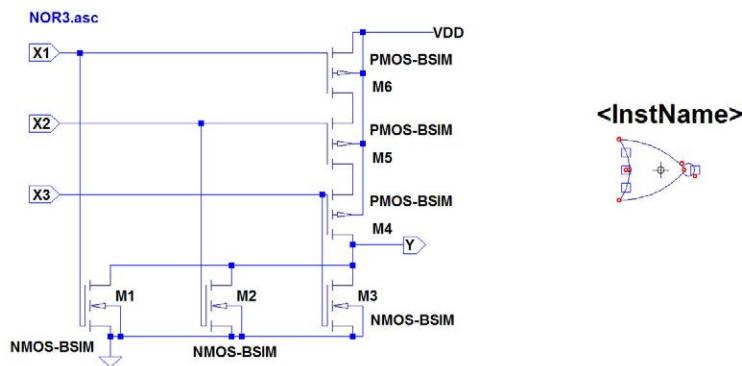
NOR2: $W_n = 3L_{min}$, $W_p = 18L_{min}$;

NOR3: $W_n = 3L_{min}$, $W_p = 27L_{min}$;

NAND2: $W_n = 6L_{min}$, $W_p = 9L_{min}$.



NMOS: NMOS-BSIM L=Lmin W={3*Lmin} ad={9*Lmin**2} as={9*Lmin**2} pd={6*Lmin} ps={6*Lmin}
PMOS: PMOS-BSIM L=Lmin W={18*Lmin} ad={54*Lmin**2} as={54*Lmin**2} pd={24*Lmin} ps={24*Lmin}



5.4

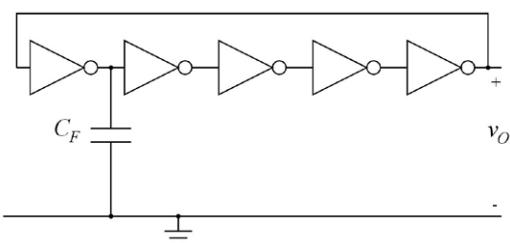


Figure P5.4

Use the inverter from Fig. 5.25 on page 181 to design a ring oscillator as shown in Fig. P5.4. Use the BSIM3 transistor models from Fig. 3.10 on page 86 with a channel length of $L_{\min} = 0.35 \mu\text{m}$ and a supply voltage of 3 V. With ‘Fanout=1’ and $C_F = 0.2 \text{ pF}$, find the frequency of oscillation. Also find the inverter delay for an inverter loaded with an identical inverter. Repeat for ‘Fanout=5’ for all of the inverters.

Hint: To start the oscillation, inject a short current pulse in the output node.

For convenience, Figs. 5.25 and 3.10 are shown on page 82 in this book.

In the past four years we have drilled

81,000 km

That's more than **twice** around the world.

Who are we?
We are the world's leading oilfield services company. Working globally—often in remote and challenging locations—we invent, design, engineer, manufacture, apply, and maintain technology to help customers find and produce oil and gas safely.

Who are we looking for?
We offer countless opportunities in the following domains:

- **Engineering, Research, and Operations**
- **Geoscience and Petrotechnical**
- **Commercial and Business**

If you are a self-motivated graduate looking for a dynamic career, apply to join our team.

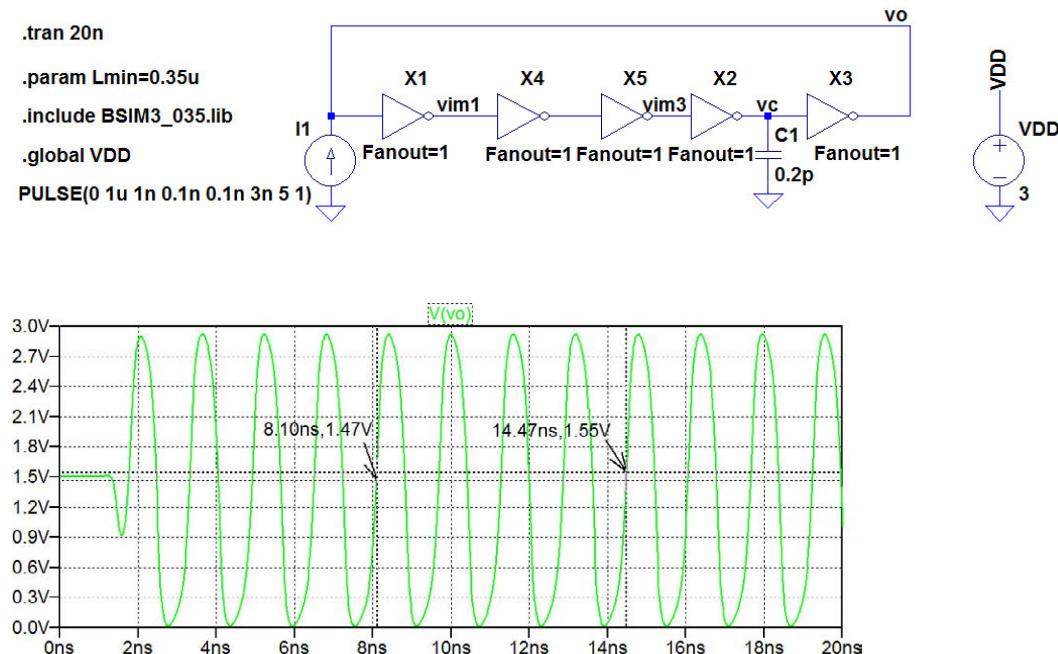
careers.slb.com

What will you be?

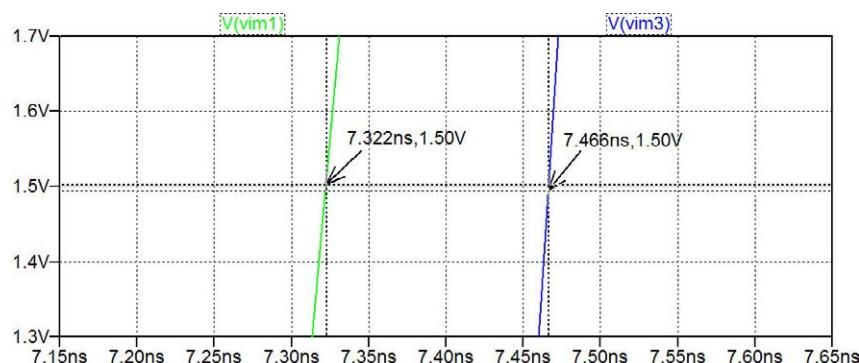
Schlumberger

Solution:

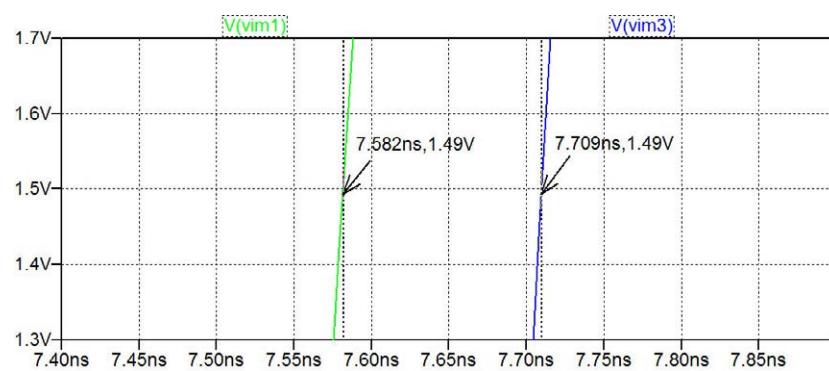
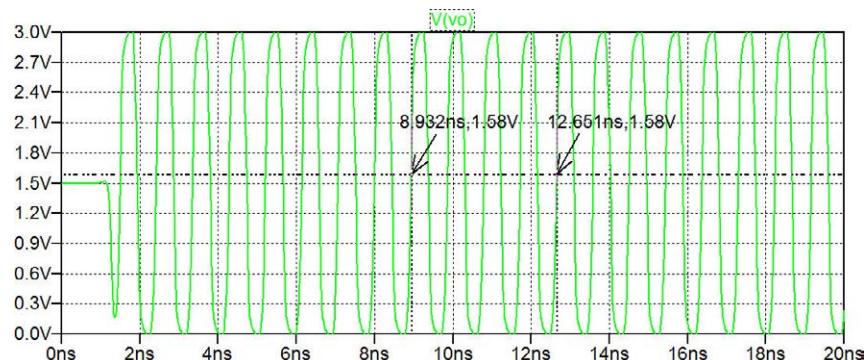
The figure below shows the oscillator schematic in LTspice. For finding the frequency of oscillation, we run a ‘.tran’ simulation. The resulting plot of the output voltage is shown below. Using the cursors, the time for 4 periods of oscillation, $4T$, is found, and the frequency is found as $f_{osc} = 1/T = 4/4T = 4/(14.45 \text{ ns} - 8.09 \text{ ns}) = 629 \text{ MHz}$.



For finding the inverter delay, we plot the voltages vim1 and vim3 defined in the schematic. The delay between rising edges of vim1 and vim3 corresponds to two inverter delays. The figure below shows the simulation plot zoomed in on a short interval around 7.4 ns. Using the cursors, we find the delay from vim1 to vim3 to be 144 ps, so the inverter delay is 72 ps.



Repeating the simulation with a fanout of 5 for the inverters, we find $f_{osc} = 1076$ MHz and $t_d = 64$ ps, see simulations below.



Tutorial 6 – Process and Parameter Variations

6.1

Typical model:

$K_p = 190 \mu A/V^2$, $V_{to} = 0.57$, $\Lambda = 0.16$
 $\Gamma = 0.5$, $\Phi = 0.7$

Slow model:

$K_p = 170 \mu A/V^2$, $V_{to} = 0.65$, $\Lambda = 0.17$
 $\Gamma = 0.5$, $\Phi = 0.7$

Fast model:

$K_p = 220 \mu A/V^2$, $V_{to} = 0.45$, $\Lambda = 0.14$
 $\Gamma = 0.5$, $\Phi = 0.7$

Figure P6.1

For an NMOS transistor, assume that typical, slow and fast models are given by the Shichman-Hodges model parameters shown in Fig. P6.1. Design a transistor model which combines the three models into one, using a speed parameter ‘SN’ with ‘SN’ = −1 for the slow model, 0 for the typical model and 1 for the fast model. Find the gate-source voltage, the transconductance and the output conductance for a transistor with $V_{GS} = V_{DS}$, $I_D = 0.4 \text{ mA}$, $W = 20 \mu \text{m}$ and $L = 1 \mu \text{m}$ for typical model parameters and for slow and fast process corners.

The advertisement features a large, bold text "INDEPENDENT MINDED" stacked above "LIKE YOU" in white. Below this, a group of four diverse young adults (three women and one man) are smiling and taking a selfie with a smartphone. The background shows a city skyline under a clear sky. In the top right corner is a dark blue square containing the University of Gothenburg logo and the text "UNIVERSITY OF GOTHENBURG". At the bottom right is the website "www.gu.se/education".

We believe in equality, sustainability and a modern approach to learning. How about you?
Apply for a Master's Programme in Gothenburg, Sweden.

PS. Scholarships available for Indian students!

www.gu.se/education

Solution:

For the transistor model, we use the basic Shichman-Hodges model with K_p , V_{to} and Λ defined as parameters. The definitions of K_p , V_{to} and Λ are done using equation (6.4) from ‘CMOS Integrated Circuit Simulation with LTspiceIV’:

$$X = \{X_t * (1 - \text{abs}(S)) + X_s * \text{uramp}(-S) + X_f * \text{uramp}(S)\} \quad (6.4)$$

where the values for X_t , X_s and X_f are typical, slow and fast parameters, respectively, and S is the speed parameter (SN for an NMOS transistor and SP for a PMOS transistor).

The resulting model and parameter definitions are shown in the figure below.

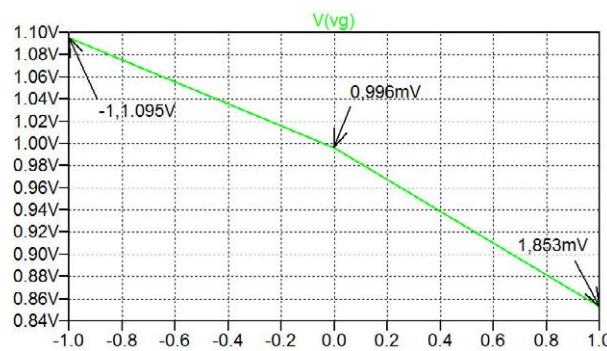
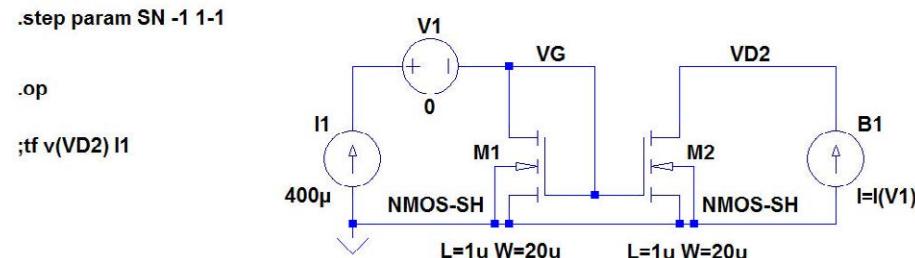
The figure also shows a schematic for simulating V_{GS} , g_{ds} and $g_m + g_{ds}$ using the method described in Example 3.6 (Fig. 3.26).

Running a ‘.op’ simulation results in a plot window where V_{GS} can be shown versus the speed parameter SN. From the plot, we find: $V_{GS} = 0.996$ V for a typical transistor ($SN = 0$), $V_{GS} = 1.095$ V for a slow transistor ($SN = -1$), and $V_{GS} = 0.853$ V for a fast transistor ($SN = 1$).

```

.model NMOS-SH NMOS (Kp={Kp} Vto={Vto} Lambda={Lambda} Gamma=0.5 Phi=0.7)
.param Kp={190u*(1-abs(SN))+170u*uramp(-SN)+220u*uramp(SN)}
.param Vto={0.57*(1-abs(SN))+0.65*uramp(-SN)+0.45*uramp(SN)}
.param Lambda={0.16*(1-abs(SN))+0.17*uramp(-SN)+0.14*uramp(SN)}

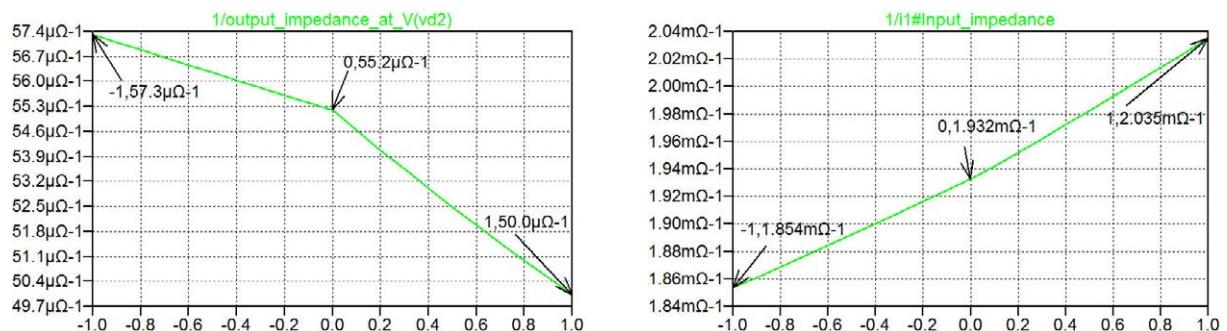
```



For finding the small-signal parameters, we run a ‘.tf’ simulation (shown as a comment in the figure on the previous page).

For g_{ds} , we plot ‘1/output_impedance_at_V(vd2)’. This output conductance is equal to g_{ds} and we find: $g_{ds} = 55.2 \mu\text{A/V}$ for a typical transistor ($\text{SN} = 0$), $g_{ds} = 57.3 \mu\text{A/V}$ for a slow transistor ($\text{SN} = -1$), and $g_{ds} = 50.0 \mu\text{A/V}$ for a fast transistor ($\text{SN} = 1$).

For finding g_m , we plot ‘1/i1#input_impedance’. This conductance is equal to $g_m + g_{ds}$, so subtracting the results for g_{ds} from the readings from the plot, we find $g_m = 1.88 \text{ mA/V}$ for a typical transistor ($\text{SN} = 0$), $g_m = 1.80 \text{ mA/V}$ for a slow transistor ($\text{SN} = -1$), and $g_m = 1.99 \text{ mA/V}$ for a fast transistor ($\text{SN} = 1$).





Linköping University – innovative, highly ranked, European

Interested in Engineering and its various branches? Kick-start your career with an English-taught master's degree.

→ Click here!

LiU LINKÖPING UNIVERSITY



6.2

```
.MODEL PMOS-BSIM PMOS LEVEL = 49
*Speed parameter SP
+VERSION = 3.1 TNOM = 2.69E+01 TOX = {7.8E-9/(1+SP/20)}
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = {-0.6+SP/10}
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = {150*(1+SP/20)**2} UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 AO = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELT = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLN = 1 WW = 0
+WWN = 1.00E+00 WWWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = {14e-4/(1+SP/20)} PB = 9.83E-01 MJ = 5.79E-01
+CJSW = {3.2e-10/(1+SP/20)} PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

Figure P6.2

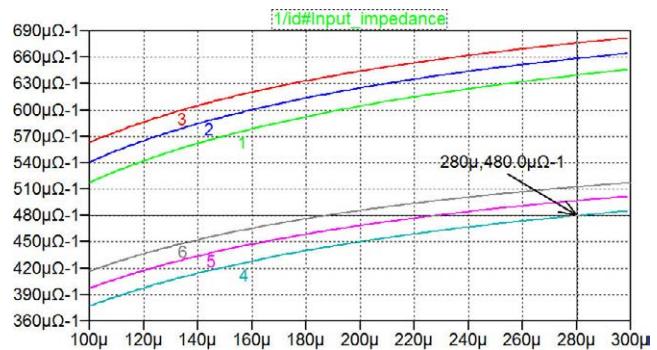
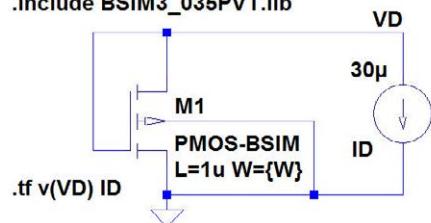
Solution:

For finding g_m versus the channel width W , we use the approach shown in Fig. 6.5. The schematic from Fig. 6.5 is shown on the next page for a PMOS transistor. For a transistor with $L = 1 \mu\text{m}$, we assume $g_m \gg g_{ds}$, so the small-signal resistance of the diode-connected transistor is a good approximation to $1/g_m$.

For showing both temperature variations and process parameter variations, we step both temperature and speed parameter as shown in the schematic on the next page. The ‘.step’ directives are inserted with the W -directive first, so that the x-axis of the plot is W . Next, the SP-directive is inserted and finally the ‘.temp’ directive. Then the three curves for a temperature of -40°C are runs 1 to 3 (starting with $\text{SP} = -1$), and the three curves for a temperature of 85°C are runs 4 to 6 (starting with $\text{SP} = -1$). From the plot of ‘ $1/i1#\text{input_impedance}$ ’, we find that the worst-case corner is a slow transistor operating at 85°C , and we find that $W = 280 \mu\text{m}$ is required to obtain $g_m \geq 0.48 \text{ mA/V}$.

Design a PMOS transistor to provide a g_m of at least 0.48 mA/V with $V_{GS} = V_{DS}$ and $I_D = 30 \mu\text{A}$ using a worst-case combination of temperature and process variations. Assume the BSIM3 model shown in Fig. P6.2 and a temperature range from -40°C to 85°C . Use a channel length of $L = 1 \mu\text{m}$.

```
.step param W 100u 300u 5u
.step param sp -1 1 1
.temp -40 85
.include BSIM3_035PVT.lib
```



STUDY FOR YOUR MASTER'S DEGREE IN THE CRADLE OF SWEDISH ENGINEERING

Chalmers University of Technology conducts research and education in engineering and natural sciences, architecture, technology-related mathematical sciences and nautical sciences. Behind all that Chalmers accomplishes, the aim persists for contributing to a sustainable future – both nationally and globally.

Visit us on **Chalmers.se** or **Next Stop Chalmers** on facebook.



6.3

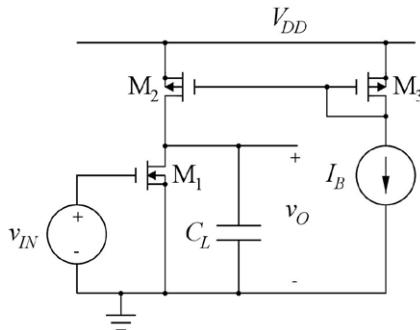


Figure P6.3

For the common-source stage shown in Fig. P6.3, assume $L_1 = L_2 = L_3 = 1 \mu\text{m}$, $W_1 = 22 \mu\text{m}$, $W_2 = W_3 = 20 \mu\text{m}$, $I_B = 140 \mu\text{A}$ and $V_{DD} = 3 \text{ V}$. Assume the BSIM3 models shown in Fig. 6.2 on page 193 and a temperature of 27°C . Also assume that process variations cause C_L to have a value in the range of 1.3 pF to 1.7 pF . Find the process corners for the unity-gain frequency.

For convenience, Fig. 6.2 is shown below.

Generic BSIM3 model for $0.35 \mu\text{m}$ CMOS process with speed parameters SN and SP to define process variations.	
<pre>*BSIM3_035PVTL.lib .MODEL NMOS-BSIM NMOS LEVEL = 49 *Speed parameter SN +VERSION = 3.1 TNOM = 27 TOX = {7.8E-9/(1+SN/10)} +XJ = 1E-07 NCH = 2.18E+17 VT0 = {0.48-SN/10} +K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01 +K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07 +DVT0W = 0 DVT1W = 0 DVT2W = 0 +DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01 +U0 = {360*(1+SN/20)**2} UA = -8.48E-10 UB = 2.27E-00 +UC = 3.27E-11 VSAT = 1.87E+05 AO = 1.22E+00 +AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06 +KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01 +RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02 +WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10 +DWG = -4.27E-09 +DBW = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00 +CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00 +CDSCB = 0 ETAO = 1 ETAB = -1.99E-01 +DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04 +PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-04 +PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02 +DELTA = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1 +PRT = 0 UTE = -1.5 KT1 = -1.11E-01 +KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09 +UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04 +WL = 0 WLN = 9.95E-01 WW = 0 +WWN = 1.00E+00 WWL = 0 LL = 0 +LLN = 1 LW = 0 LWN = 1 +LWL = 0 CAPMOD = 2 XPART = 0.5 +CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12 +CJ = {9e-4/(1+SN/20)} PB = 7.95E-01 MJ = 3.53E-01 +CJSW = {2.8e-10/(1+SN/20)} PBSW = 7.98E-01 MJSW = 1.73E-01 +CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01 +CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01 +PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03</pre>	<pre>.MODEL PMOS-BSIM PMOS LEVEL = 49 *Speed parameter SP +VERSION = 3.1 TNOM = 2.69E+01 TOX = {7.8E-9/(1+SP/20)} +XJ = 1.00E-07 NCH = 8.44E+16 VT0 = {-0.6+SP/10} +K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01 +K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07 +DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0 +DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01 +U0 = {150*(1+SP/20)**2} UA = 1E-10 UB = 1.75E-18 +UC = -2.27E-11 VSAT = 2.01E+05 AO = 1.04E+00 +AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06 +KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00 +RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03 +WRL = 1 WINT = 1.47E-07 LINT = 1.04E-10 +DWG = -1.09E-08 +DBW = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00 +CIT = 0 CDSC = 2.40E-04 CDSCD = 0 +CDSCB = 0 ETAO = 4.07E-02 ETAB = 6.84E-03 +DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03 +PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04 +PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15 +DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1 +PRT = 0 UTE = -1.5 KT1 = -1.09E-01 +KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09 +UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04 +WL = 0 WLN = 1 WW = 0 +WWN = 1.00E+00 WWL = 0 LL = 0 +LLN = 1 LW = 0 LWN = 1 +LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5 +CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12 +CJ = {14e-4/(1+SP/20)} PB = 9.83E-01 MJ = 5.79E-01 +CJSW = {3.2e-10/(1+SP/20)} PBSW = 9.92E-01 MJSW = 3.60E-01 +CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01 +CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01 +PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03</pre>

Figure 6.2: Library file with BSIM3 models for a generic $0.35 \mu\text{m}$ CMOS process with speed parameters SN and SP to define process variations, adapted from (Chan Carusone, Johns & Martin 2014). Speed parameter is 0 for typical model, -1 for slow model and +1 for fast model.

Solution:

For simulating the unity-gain frequency, we need a ‘.ac’ simulation. In order to ensure a correct dc bias point for the ‘.ac’ simulation in all process corners, we apply a dc feedback as shown in Fig. 6.15(a). For convenience, this figure is shown below.

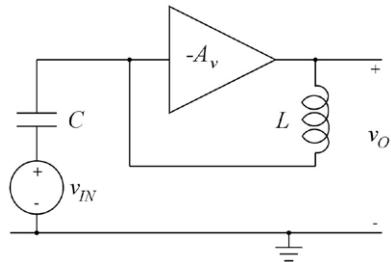
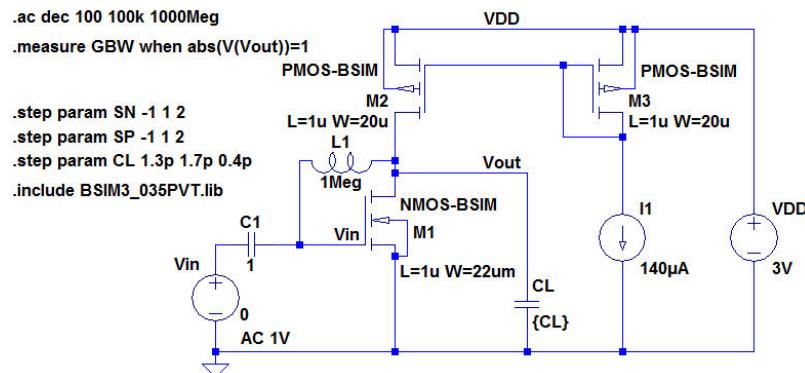
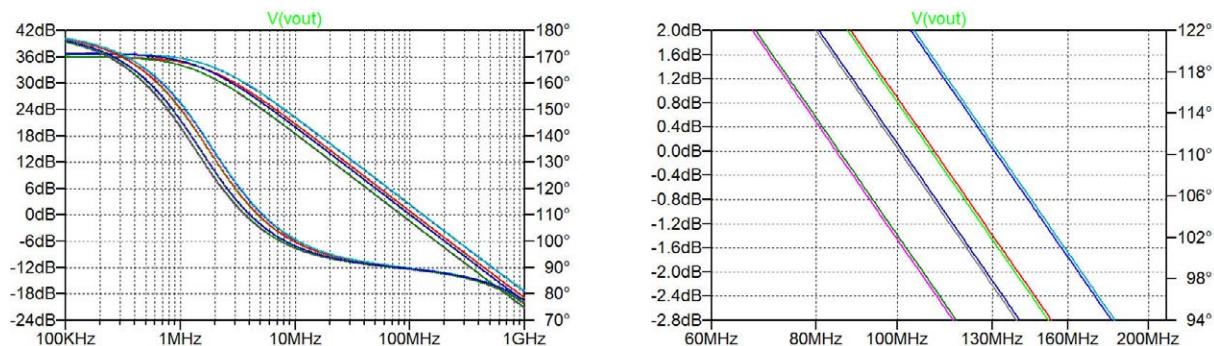


Figure 6.15(a): Inverting amplifier with dc feedback to provide a suitable dc bias point.

For finding the process corners, we step the speed parameters SN and SP between the values -1 and 1 , and we step the capacitor C_L between the two values 1.3 pF (fast) and 1.7 pF (slow) using the ‘.step’ directives shown in the schematic below. The ‘.step’ directives are inserted with the SN-directive first, so that SN is stepped first. Next, the SP-directive is inserted and finally the C_L -directive. We may find the unity-gain frequency from the plots resulting from a ‘.ac’ simulation but it is easier to use a ‘.measure’ directive as shown in the schematic below.



The plot resulting from a ‘.ac’ simulation is shown below. It has a total of eight traces, one for each corner, but some of the traces are almost overlapping. This can be seen from the close-up on the plot around the unity-gain frequency also shown below.



Rather than using the cursors to find the process corners, we use the results from the ‘.measure’ directive found in the error log file (‘Ctrl-L’) shown below.

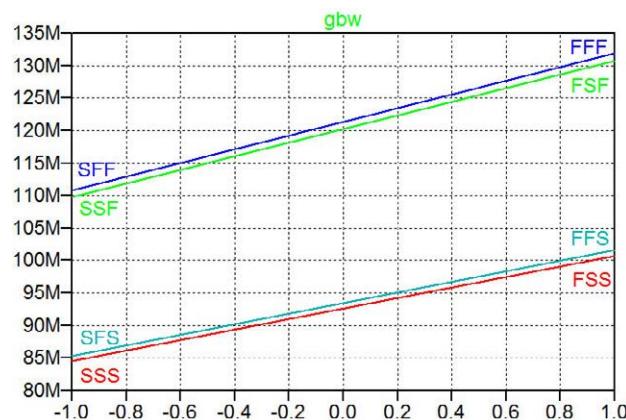
```
Direct Newton iteration for .op point succeeded.
.step sn=-1 sp=-1 cl=1.3e-012
.step sn=1 sp=-1 cl=1.3e-012
.step sn=-1 sp=1 cl=1.3e-012
.step sn=1 sp=1 cl=1.3e-012
.step sn=-1 sp=-1 cl=1.7e-012
.step sn=1 sp=-1 cl=1.7e-012
.step sn=-1 sp=1 cl=1.7e-012
.step sn=1 sp=1 cl=1.7e-012
```

```
Measurement: gbw
step      abs(v(vout))=1
 1        1.09824e+008
 2        1.30765e+008
 3        1.10805e+008
 4        1.31945e+008
 5        8.45606e+007
 6        1.00653e+008
 7        8.52814e+007
 8        1.0155e+008
```

From this, we can compile the following table:

Step	NMOS	PMOS	C_L	Unity-gain frequency
1	slow	slow	fast	109.8 MHz
2	fast	slow	fast	130.8 MHz
3	slow	fast	fast	110.8 MHz
4	fast	fast	fast	131.9 MHz
5	slow	slow	slow	84.6 MHz
6	fast	slow	slow	100.7 MHz
7	slow	fast	slow	85.3 MHz
8	fast	fast	slow	101.6 MHz

The results may also be shown graphically by right-clicking in the error log file and selecting ‘Plot .step’ed .meas data’. The figure below shows this plot with a labeling indicating the process corners.



6.4

For the digital inverter X2 in Fig. 6.18 on page 205, find the worst-case delay time considering both process variations, temperature variations from -40°C to 85°C and supply voltage variations from 2.7 V to 3.3 V.

For convenience, Fig. 6.18 is shown below.

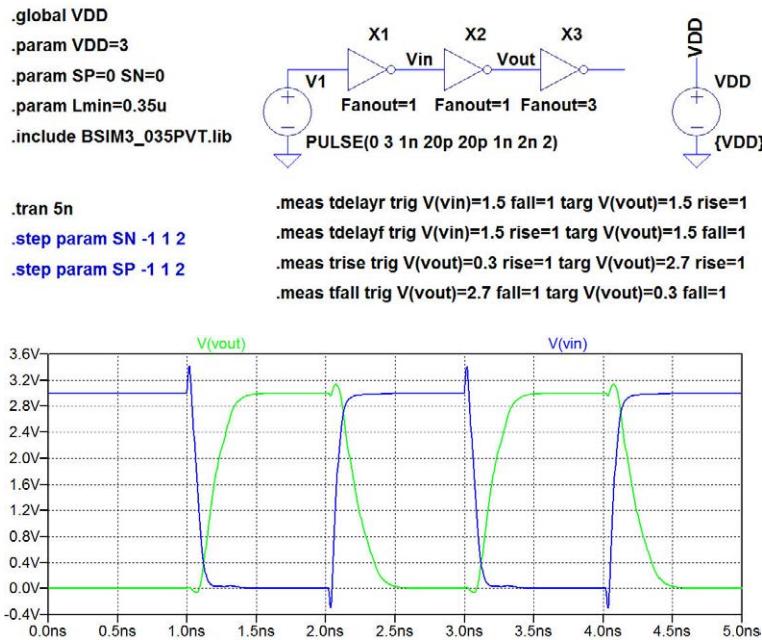
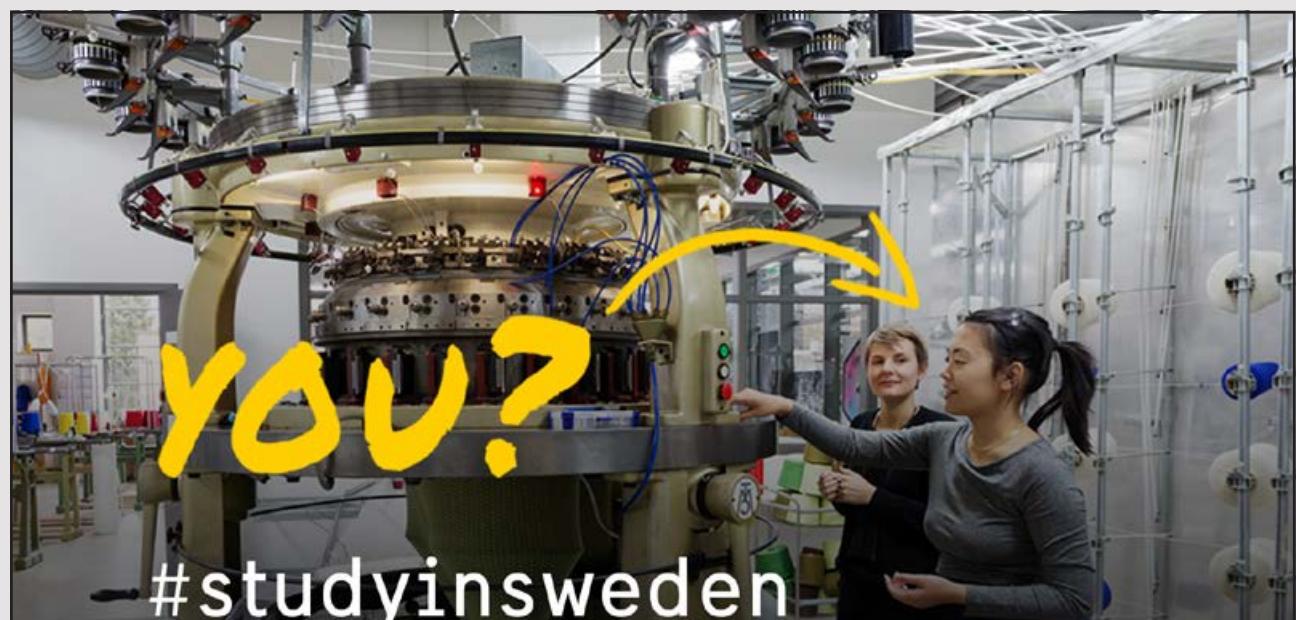


Figure 6.18: LTspice schematic of the inverter used as a digital inverter (top) and the result of a transient simulation (bottom).

Solution:

Compared to the simulation in Fig. 6.18, we need to vary also the temperature and the supply voltage. Thus, we have a total of four parameters to be stepped which is more than LTspice can handle. However, we know from the simulations of the transistor characteristics that the high temperature (85°C) is the more critical one, and – intuitively – a low supply voltage will give longer delays as the transistor over-drive voltages are smaller. Thus, a pragmatic approach is to repeat the simulation from Fig. 6.18 with a temperature of 85°C and a supply voltage of 2.7 V. In the ‘.meas’ directives, the threshold voltages for rising and falling edge should be modified accordingly, i.e. to $V_{DD}/2$ V. Also the threshold voltages for rise time and fall time are modified although rise and fall time simulations are not requested in the problem.

The schematic with these changes are shown on the next page, and also a plot from the transient simulation and the results from the error log file are shown. We find that the worst-case delay occurs for a falling output with a slow NMOS transistor and a fast PMOS transistor. The maximum delay time is 199 ps. Also shown on the next page is a close-up on the falling output edge around 2 ns. The up and down arrow keys are used to place the cursor on the correct trace (step 3) and a right mouse click on the cursor is used to open a window with information about which trace the cursor is following.



Striking a match, reconnecting with your family through Skype or over a phone network from Ericsson, refurbishing your apartment at IKEA or driving safely in your Volvo - none of this would be possible if not for Sweden.
Swedish universities offer over 900 international master's programmes taught entirely in English.

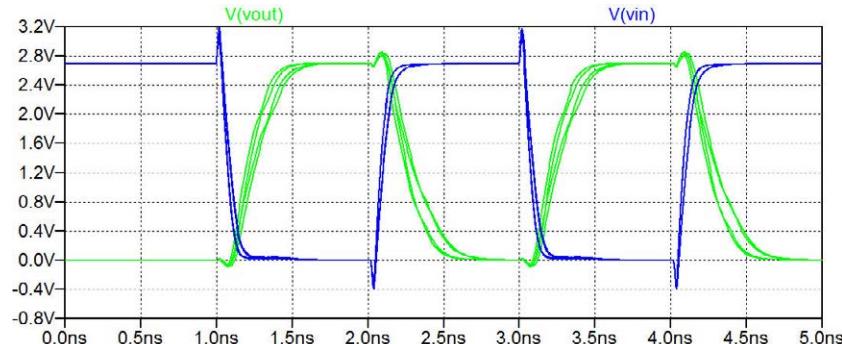
Don't just pick a place - pick a future.
>studyinsweden.se



```
.global VDD
.param VDD=2.7
.param SP=-1 SN=-1
.param Lmin=0.35u
.include BSIM3_035PVT.lib
.temp 85

.tran 5n
.step param SN -1 1 2
.step param SP -1 1 2

.meas tdelayr trig V(vin)={VDD/2} fall=1 targ V(vout)={VDD/2} rise=1
.meas tdelayf trig V(vin)={VDD/2} rise=1 targ V(vout)={VDD/2} fall=1
.meas trise trig V(vout)={VDD*0.1} rise=1 targ V(vout)={VDD*0.9} rise=1
.meas tfall trig V(vout)={VDD*0.9} fall=1 targ V(vout)={VDD*0.1} fall=1
```



Direct Newton iteration for .op point succeeded.

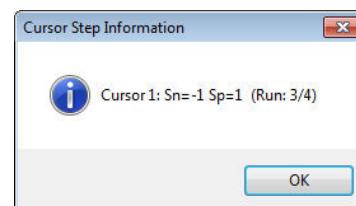
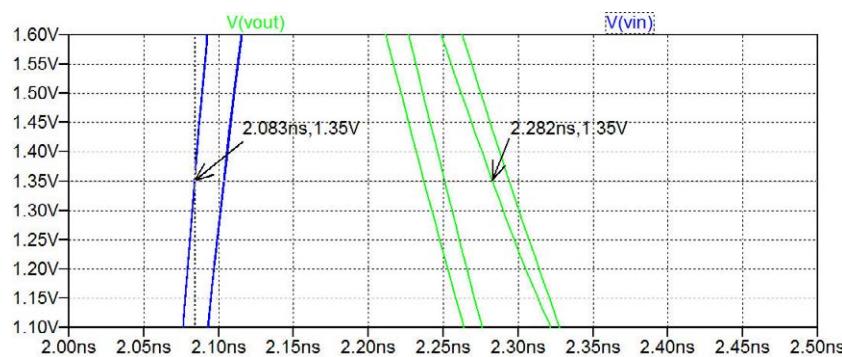
```
.step sn=-1 sp=-1
.step sn=1 sp=-1
.step sn=-1 sp=1
.step sn=1 sp=1
```

Measurement: tdelayr

step	tdelayr	FROM	TO
1	1.76492e-010	1.0868e-009	1.26329e-009
2	1.75295e-010	1.06988e-009	1.24517e-009
3	1.32493e-010	1.08991e-009	1.2224e-009
4	1.30468e-010	1.07231e-009	1.20278e-009

Measurement: tdelayf

step	tdelayf	FROM	TO
1	1.90873e-010	2.1032e-009	2.29407e-009
2	1.47291e-010	2.10361e-009	2.2509e-009
3	1.99271e-010	2.08364e-009	2.28291e-009
4	1.53242e-010	2.08384e-009	2.23708e-009



6.5

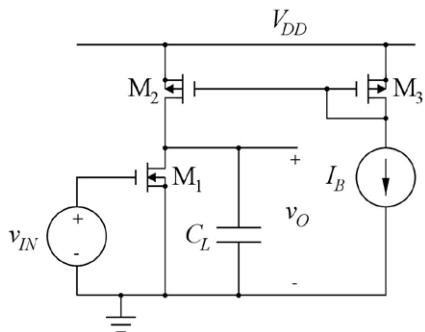


Figure P6.5

For the common-source stage shown in Fig. P6.5, find the worst-case corner for unity-gain bandwidth (lowest unity-gain bandwidth) for temperature variations and supply voltage variations. Assume $C_L = 1.5 \text{ pF}$, $L_1 = L_2 = L_3 = 1 \mu\text{m}$, $W_1 = 22 \mu\text{m}$, $W_2 = W_3 = 20 \mu\text{m}$, $V_{DD} = 3 \text{ V}$ and $I_B = (V_{DD} - 0.9 \text{ V})/(15 \text{ k}\Omega)$.

Assume the BSIM3 models shown in Fig. 6.2 on page 193 with typical process parameters, temperature variations from -40°C to 85°C and supply voltage variations from 2.7 V to 3.3 V. Run a Monte Carlo simulation for the worst-case combination of temperature and supply voltage with stochastic variations of the process parameters for the transistors and the capacitor C_L . Assume a standard deviation of 0.4 for the process speed parameters and a capacitor tolerance of $\pm 5\%$. Estimate mean value and standard deviation of the unity-gain frequency for the worst-case combination of temperature and supply voltage.

Solution:

For simulating the unity-gain frequency, we need a ‘.ac’ simulation. In order to ensure a correct dc bias point for the ‘.ac’ simulation in all process corners, we apply a dc feedback as shown in Fig. 6.15(a) (also shown on page 99 in this book). For finding corners for supply voltage variation and temperature variation, we step the supply voltage VDD and the temperature using the ‘.step’ directive and the ‘.temp’ directive shown in the schematic on the next page. We may find the unity-gain frequency from the plots resulting from a ‘.ac’ simulation but it is easier to use a ‘.measure’ directive to calculate the process corner values of the unity-gain frequency. The ‘.measure’ directive is shown in the schematic on the next page.

**TAKE THE
RIGHT TRACK**

**Click here
to learn more**

**Give your career a head start
by studying with us. Experience the advantages
of our collaboration with major companies like
ABB, Volvo and Ericsson!**

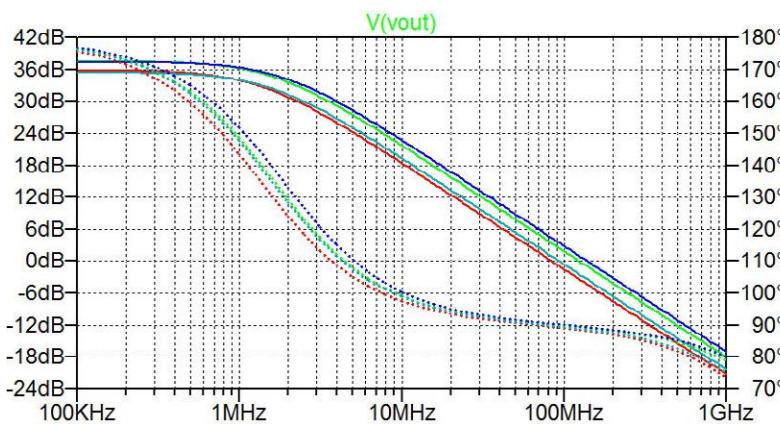
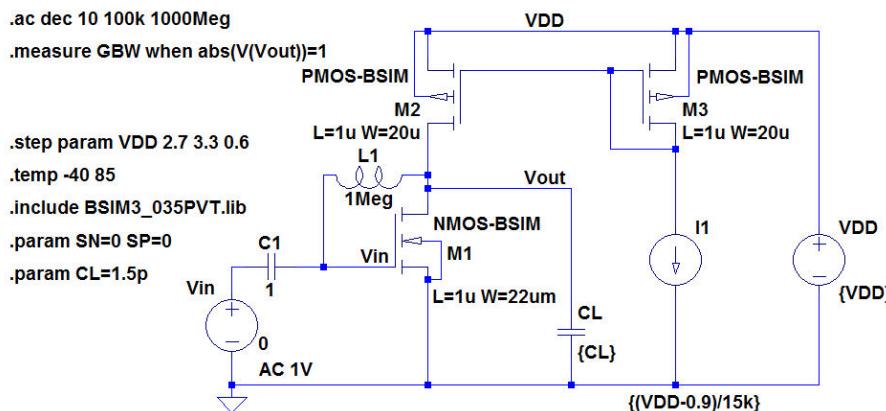
**Apply by
15 January**

**World class
research**

www.mdh.se

**MÄLARDALEN UNIVERSITY
SWEDEN**





The results from the ‘.measure’ directive are found in the error log file shown below, and we find that the worst-case corner is the combination of a low supply voltage and a high temperature.

The process corners can also be shown graphically by right-clicking in the error log file and selecting ‘Plot .step’ed .meas data’. The figure below shows the resulting plot.

```

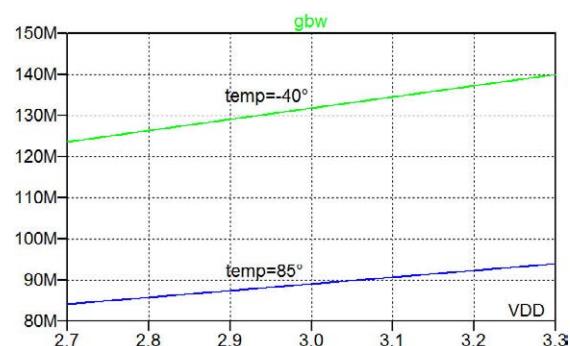
Direct Newton iteration for .op point succeeded.
.step vdd=2.7 temp=-40°C
.step vdd=3.3 temp=-40°C
.step vdd=2.7 temp=85°C
.step vdd=3.3 temp=85°C

```

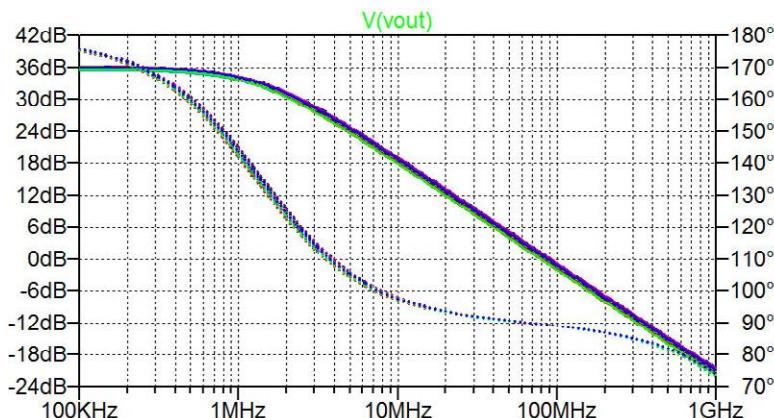
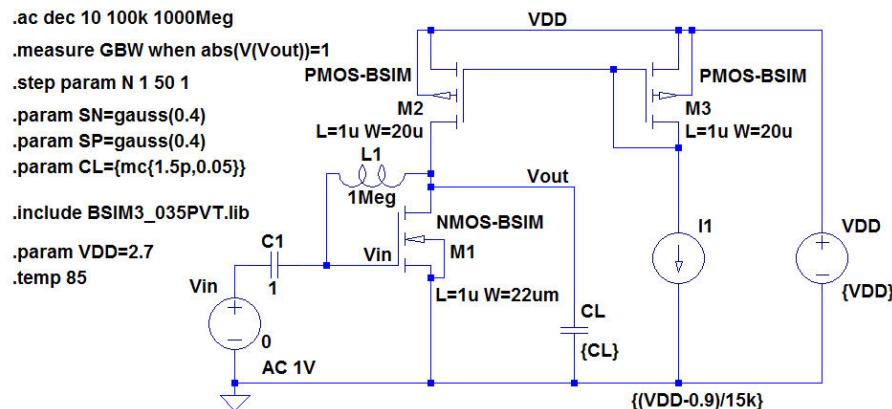
```

Measurement: gbw
step      abs (v(vout))=1
1        1.23642e+008
2        1.39998e+008
3        8.42695e+007
4        9.40421e+007

```



For running a Monte Carlo simulation with a supply voltage of 2.7 V and a temperature of 85°C, we define VDD and temp to have these values. Also, we define SN, SP and CL to have stochastic variations using the functions ‘gauss(x)’ and ‘mc(x,y)’. For a Monte Carlo simulation with 50 simulations, a step count parameter N must be defined as shown in the schematic below. Also a plot of the output voltage resulting from the simulation is shown.



The error log file from the simulation gives the calculated values of the unity-gain bandwidth for each of the 50 steps in the Monte Carlo simulation. The results are shown on the next page. By right-clicking in the error log file and selecting ‘Plot .step’ed .meas data’, the results can also be plotted graphically as also shown on the next page.

The results from the error log file may be copied into an Excel spreadsheet, and from this, we find a mean value of 85 MHz and a standard deviation of 4 MHz.

```
Measurement: gbw
step      abs(v(vout))=1
1          8.17271e+007
2          7.92561e+007
3          8.97408e+007
4          8.67015e+007
5          8.50062e+007
6          8.82216e+007
7          8.74819e+007
8          8.38107e+007
9          8.57428e+007
10         8.34513e+007
11         8.11149e+007
12         9.0147e+007
13         7.982e+007
14         7.90185e+007
15         9.11583e+007
16         8.71882e+007
17         8.1665e+007
18         8.76643e+007
19         8.4134e+007
20         9.25686e+007
21         9.00365e+007
22         8.22461e+007
23         8.85673e+007
24         8.5306e+007
25         8.32077e+007
26         8.09493e+007
27         8.22352e+007
28         7.99386e+007
29         8.83158e+007
30         8.22246e+007
31         9.11552e+007
32         8.30066e+007
33         7.83127e+007
34         8.09654e+007
35         8.51145e+007
36         8.50773e+007
37         8.60746e+007
38         8.83669e+007
39         7.90209e+007
40         7.94301e+007
41         9.22594e+007
42         8.69342e+007
43         8.88345e+007
44         8.85208e+007
45         8.13371e+007
46         9.11521e+007
47         8.43626e+007
48         8.66154e+007
49         7.90699e+007
50         8.74e+007
```



Tutorial 7 – Importing and Exporting Files

7.1

*Differential NMOS pair with
*resistive load and differential output

*Noninverting input: Node 3
*Inverting input: Node 2
*Noninverting output: Node 4
*Inverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground

*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W=16u
M2 5 3 6 0 NMOS-BSIM L=0.7u W=16u

Figure P7.1

Figure 3.10 is shown on page 82 in this book.

Figure P7.1 shows a netlist for a differential NMOS pair with differential output. Create a netlist file for LTspice for simulating the circuit with a supply voltage of 3 V, a bias current of 250 μ A and a common-mode input voltage of 1.5 V. Use the BSIM3 transistor model from Fig. 3.10 on page 86. Find the bias values of the output voltages and the small-signal differential gain.



ADVANCE YOUR CAREER IN UMEÅ!

- modern campus • world class research • 32 000 students
- top class teachers • ranked nr 1 in Sweden by international students

Master's programmes:

- Architecture • Industrial Design • Science • Engineering

Download brochure here!

UMEÅ UNIVERSITY
FACULTY OF SCIENCE & TECHNOLOGY

Solution:

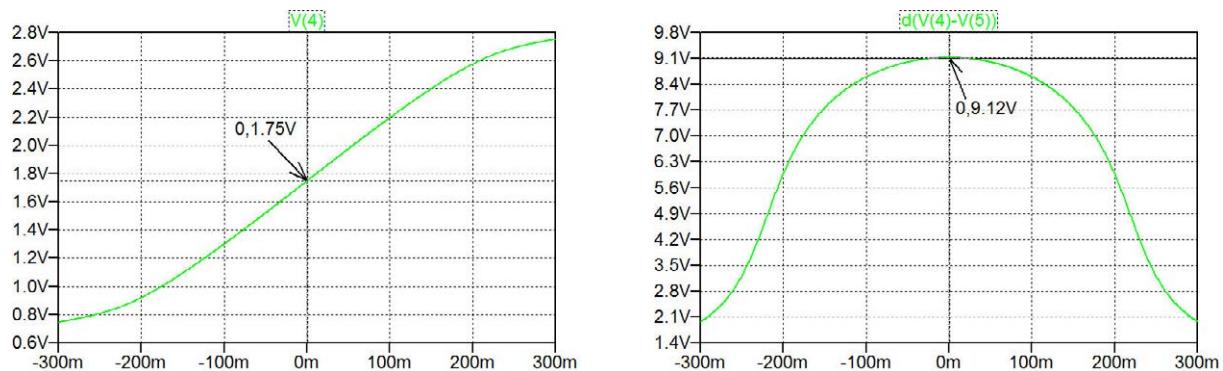
For the netlist file for LTspice, we need to add the supply voltage, the bias current, and the input voltages (common-mode and differential-mode). Also, a simulation directive must be specified. In the file shown below, the input voltages are added using the scheme from Problem 4.6, and the differential input voltage is varied using a ‘.step’ directive in combination with a ‘.op’ simulation.

```

*Differential NMOS pair with
*resistive load and differential output
*NNoninverting input: Node 3
*IInverting input: Node 2
*NNoninverting output: Node 4
*IInverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground
*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W=16u
M2 5 3 6 0 NMOS-BSIM L=0.7u W=16u
*Transistor models
.include BSIM3_035.lib
*Supply voltage and bias current
VDD 1 0 3
IB 6 0 250u
*input voltages
vcm 11 0 1.5
vdp 3 11 {vid/2}
vdn 2 11 {-vid/2}
.step param vid -0.3 0.3 0.001
.op
.end

```

The simulation is run directly from the netlist file in LTspice using the ‘Simulate → Run’ command (or ‘Ctrl-R’), and in the plot window which opens, the traces to plot are selected using ‘Plot Setting → Add trace’ (or ‘Ctrl-A’). For finding the common-mode output voltage, we plot the noninverting output ($V(4)$) and read the value for an input voltage of 0 V. For finding the differential gain, we plot the derivative of the differential output voltage, i.e. $d(V(4)-V(5))$ and find the value for an input voltage of 0 V. From the plots below, we find a common-mode output voltage of 1.75 V and a differential gain of 9.12 V/V.



7.2

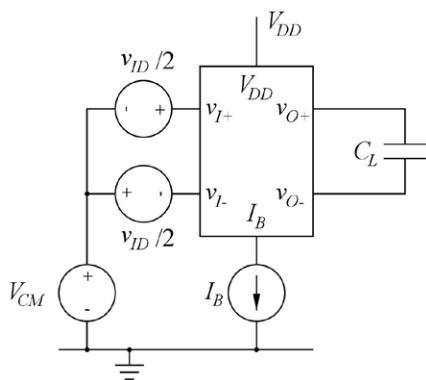


Figure P7.2

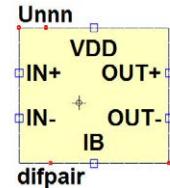
Use the netlist from Fig. P7.1 to design a subcircuit and a subcircuit symbol for the differential pair. Use the BSIM3 transistor model from Fig. 3.10 on page 86. Design the subcircuit to have separate terminals for the supply voltage and the bias current. Insert the differential pair in a test bench as shown in Fig. P7.2 and find the -3 dB frequency for the differential gain. Use $V_{DD} = 3$ V, $I_B = 250$ μ A, $V_{CM} = 1.5$ V and $C_L = 3$ pF.

Figure 3.10 is shown on page 82 in this book.

Solution:

The netlist from Fig. P7.1 is modified by including a ‘.subckt’ directive and a ‘.ends’ directive as shown below. By placing the cursor in the ‘.subckt’ line and right-clicking, a symbol is generated, and using the graphic symbol editor, this may be modified into the symbol shown below.

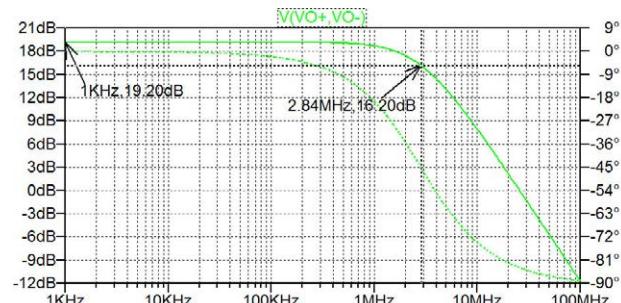
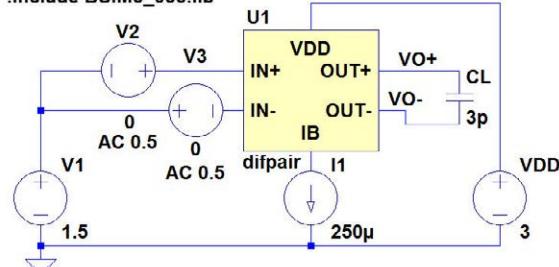
```
*Differential NMOS pair with
*resistive load and differential output
*Noninverting input: Node 3
*Inverting input: Node 2
*Noninverting output: Node 4
*Inverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground
.subckt difpair 1 2 3 4 5 6
*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W=16u
M2 5 3 6 0 NMOS-BSIM L=0.7u W=16u
.ends
```



The figure below shows a testbench corresponding to Fig. P7.2 and a plot of the differential output voltage. From the plot, we find a -3 dB frequency of 2.84 MHz.

.ac oct 5 1k 100Meg

.include BSIM3_035.lib





We ask you
**WHERE DO YOU
WANT TO BE?**

TomTom 

TomTom is a place for people who see solutions when faced with problems, who have the energy to drive our technology, innovation, growth along with goal achievement. We make it easy for people to make smarter decisions to keep moving towards their goals. If you share our passion - this could be the place for you.

Founded in 1991 and headquartered in Amsterdam, we have 3,600 employees worldwide and sell our products in over 35 countries.

For further information, please visit tomtom.jobs

7.3

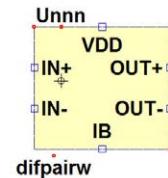
Redefine the subcircuit from Problem 7.2 to have the transistor channel width as a parameter which can be defined at top level.

Use the testbench from Fig. P7.2 to find the low-frequency gain as a function of the channel width for $5 \mu\text{m} \leq W \leq 30 \mu\text{m}$. What is the value of the low-frequency gain for $W = 5 \mu\text{m}$ and $W = 30 \mu\text{m}$?

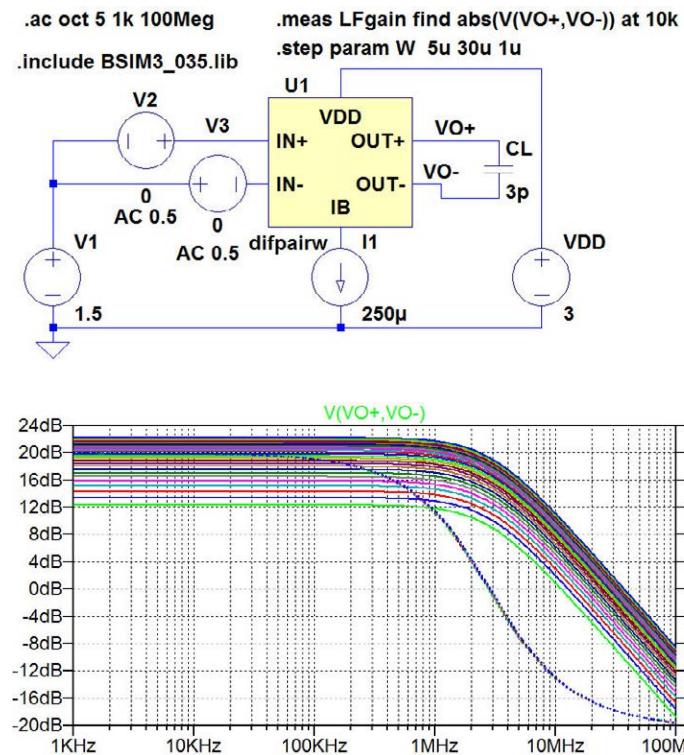
Solution:

The netlist from Problem 7.2 is modified by specifying the channel width as a parameter. Also, the subcircuit is renamed to ‘difpairw’ with a corresponding symbol as shown below.

```
*Differential NMOS pair with
*resistive load and differential output
*Noninverting input: Node 3
*Inverting input: Node 2
*Noninverting output: Node 4
*Inverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground
.subckt difpairw 1 2 3 4 5 6
*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W={W}
M2 5 3 6 0 NMOS-BSIM L=0.7u W={W}
.ends
```



The testbench from Problem 7.2 is modified by replacing the subcircuit ‘difpair’ with ‘difpairw’ and including a ‘.step’ directive to sweep the channel width. Also, a ‘.measure’ directive for finding the low-frequency gain is inserted as shown below. The resulting ‘.ac’ simulation has many traces, see below.



In order to find the low-frequency gain versus channel width, we open the error log file and right-click to ‘Plot .step’ed .meas data’. The plot is shown below, and from the plot, we find a gain of 4.15 V/V for $W = 5 \mu\text{m}$ and 12.9 V/V for $W = 30 \mu\text{m}$.

