Zichen Fan
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Education

- **University of Michigan** — Ann Arbor, MI
  PhD Candidate in Electrical Computer Engineering — *Aug. 2019 – Present*
- **University of Michigan** — Ann Arbor, MI
  Master of Engineering in Electrical Computer Engineering, GPA: 4.0/4.0 — *Aug. 2019 – Apr. 2022*
- **Tsinghua University** — Beijing, China
  Bachelor of Engineering in Electronics Engineering, GPA: 3.7/4.0 — *Aug. 2015 – July. 2019*

Publication

- **Zichen Fan**, et al. "Audio and Image Cross-Modal Intelligence via a 10TOPS/W 22nm SoC with Back-Propagation and Dynamic Power Gating." *2022 IEEE Symposium on VLSI Circuits (VLSI-Symp)*. IEEE, 2022.
- Qirui Zhang, Hyochan An, **Zichen Fan**, et al. "A 22nm 3.5TOPS/W Flexible Micro-Robotic Vision SoC with 2MB eMRAM for Fully-on-Chip Intelligence." *2022 IEEE Symposium on VLSI Circuits (VLSI-Symp)*. IEEE, 2022.
- Ziru Li, Bing Li, **Zichen Fan**, et al. "RED: A ReRAM-based Efficient Accelerator for Deconvolutional Computation." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. 2020.
- **Zichen Fan**, et al. "ASP-SIFT: Using Analog Signal Processing Architecture to Accelerate Keypoint Detection of SIFT Algorithm." *IEEE Transactions on Very Large Scale Integration (T-VLSI) Systems*. 2019.
- Zheyu Liu, **Zichen Fan**, et al. "Design of Switched-Current Based Low-Power PIM Vision System for IoT Applications." *2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE, 2019.
- **Zichen Fan**, et al. "RED: A ReRAM-based Deconvolution Accelerator." *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2019.
- Sergei Alyamkin, et al. "Low-Power Computer Vision: Status, Challenges, Opportunities." *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*. 2019.

Research Experience

- **Michigan Integrated Circuit Lab (MICL),** University of Michigan — Ann Arbor, MI
  Co-advisors: Professor Dennis Sylvester and Professor David Blaauw — *Aug 2019 - Present*
  - **Total 1 real silicon is taped out and tested successfully**:
  - **Multi-modal Signal Processing SoC**: Designed an ultra-low-power multi-modal signal processor (MMSP) SoC in 22nm technology that integrates a versatile deep neural network (DNN) engine with audio and image signal processing accelerators for cross-modal IoT intelligence. The SoC achieves up to 3-10 TOPS/W peak energy efficiency and consumes only 0.25-3.84 mW. Being the first to demonstrate CNN, GAN, and back-propagation (BP) on a single accelerator SoC for cross-modal fusion, it outperforms state-of-the-art DNN processors by 1.4 - 4.5× in energy efficiency.
  - **MRAM**: Used TSMC 22nm 2MB MRAM macro on two different real-silicon tape-outs and tested correctly.
  - **CPF Flow**: First time using Cadence Innovus CPF Flow to handle multiple power domains in the group. The chip is tested correctly and the scripts have been used on another 2 real silicon tape-outs in the group.
  - **Back-propagation GAN for Audio Compression**: Worked on the GAN-based audio compression algorithms, which result in low data rate (less than 1kbps) for audio. Used BPGAN to compress audio and reduced the complexity of the network to be compatible with the computation ability of the hardware.
- **Nanoscale Integrated Circuits and Systems Lab (NICS),** Tsinghua University — Beijing, China
  Advisor: Professor Fei Qiao — *Aug 2017 - Jun 2019*

- **Current-based PIM**: Worked on the switched-current based low-power processing-in-memory (PIM) vision system. Designed current mode APS and current mode PIM architecture. The designed system outperformed the state-of-the-art designs in terms of power consumption (1.45mW) and achieves energy efficiency up to 28.25TOPS/W.
- **Analog Signal Processing SIFT Accelerator**: Worked on the SIFT acceleration system using analog signal processing architecture. Proposed an analog circuit network that realized the keypoint detection part of SIFT. Results showed that the system can process 2.3k VGA frames per second, which is at least 3.26 times faster than the state-of-art digital hardware accelerators.

- **Computational Evolutionary Intelligence Lab (CEI),** Duke University — Durham, NC
  Co-advisor: Professor Yiran Chen and Professor Hai Li — *Jul 2018 - Sept 2018*
  - **ReRAM-based Deconvolution accelerator**: Worked on ReRAM-based deconvolution accelerator design, which aims to accelerate the deconvolution operation in Generative Adversarial Networks and Fully Convolutional Networks using ReRAM. Proposed the pixel-wise mapping scheme for reducing redundancy and zero-skipping data flow for increasing the computation parallelism which could accelerate the deconvolution operation by $3.69\times \sim 31.15\times$.

Skills

- **Languages**: C, C++, Python, MATLAB, Verilog, System Verilog, LaTex
- **Tools**: Synopsys & Cadence Design Tools, Pytorch, Vivado, Spice

Awards

- 3^{rd} Place in Low-Power Image Recognition Challenge (LPIRC 2018), Track2 — 2018
- 2^{nd} Prize in Tsinghua Excellent Student Research Training (SRT) Project **(top 10%)** — 2018
- 3^{rd} Prize in 35^{th} Challenge cup of Tsinghua University **(top 15%)** — 2017
- Meritorious Winner in Mathematical Contest in Modeling, COMAP — 2017
- 1^{st} Prize for the 32rd National Undergraduate Physics Olympic — 2016
- 2^{nd} Prize in Tsinghua Maker Challenge, Tsinghua University — 2016
- Scholarship for Scientific and Technological Innovation — 2016-18
- Scholarship for Academic Excellence — 2015-16