Zichen Fan

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Education

- **University of Michigan** — Ann Arbor, MI
  PhD pre-candidate of Electrical Computer Engineering — *Aug. 2019 – Present*
- **Tsinghua University** — Beijing, China
  Bachelor of Engineering in Electronics Engineering, GPA: 3.7/4.0 — *Aug. 2015 – July. 2019*

Publication

- **Fan, Zichen**, et al. "RED: A ReRAM-based Deconvolution Accelerator." *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2019.
- **Fan, Zichen**, et al. "ASP-SIFT: Using Analog Signal Processing Architecture to Accelerate Keypoint Detection of SIFT Algorithm." *IEEE Transactions on Very Large Scale Integration (T-VLSI) Systems*. 2019.
- Liu, Zheyu, **Fan, Zichen**, et al. "Design of Switched-Current Based Low-Power PIM Vision System for IoT Applications." *2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE, 2019.
- Alyamkin, Sergei, et al. "Low-Power Computer Vision: Status, Challenges, Opportunities." *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*. 2019.

Research Experience

- **Michigan Integrated Circuit Lab (MICL),** University of Michigan — Ann Arbor, MI
  Co-advisors: Professor Dennis Sylvester and Professor David Blaauw — *Aug 2019 - Present*
- **Nanoscale Integrated Circuits and Systems Lab (NICS),** Tsinghua University — Beijing, China
  Advisor: Professor Fei Qiao — *Aug 2017 - Jun 2019*
  - **Current-based PIM**: Worked on the switched-current based low-power processing-in-memory (PIM) vision system. Designed current mode APS and current mode PIM architecture. The designed system outperformed the state-of-the-art designs in terms of power consumption (1.45mW) and achieves energy efficiency up to 28.25TOPS/W.
  - **ASP-SIFT**: Worked on the SIFT acceleration system using analog signal processing architecture. Proposed an analog circuit network that realized the keypoint detection part of SIFT. Results showed that the system can process 2.3k VGA frames per second, which is at least 3.26 times faster than the state-of-art digital hardware accelerators.
- **Computational Evolutionary Intelligence Lab (CEI),** Duke University — Durham, NC
  Co-advisor: Professor Yiran Chen and Professor Hai Li — *Jul 2018 - Sept 2018*
  - **RED**: Worked on ReRAM-based deconvolution accelerator design, which aims to accelerate the deconvolution operation in Generative Adversarial Networks and Fully Convolutional Networks using ReRAM. Proposed the pixel-wise mapping scheme for reducing redundancy and zero-skipping data flow for increasing the computation parallelism which could accelerate the deconvolution operation by $3.69\times \sim 31.15\times$.

Course Projects

- **Fully Differential OTA**: Led a team of three and successfully designed a fully differential OTA which meet the requirements given by the guidance, responsible for 90% of the work, proposed the circuit structure and do simulations. The result can be seen in github.
- **Convolution Accelerator**: Led a team of two and successfully accelerated convolution operation using ZYNQ-7000 FPGA board controlled by embedded Linux system "Xillinux". Used convolution IP core to accelerate CNN network (convolution layer) on FPGA and got top 1 grade in the class.

Skills

- **Languages**:C, C++, Python, MATLAB, Verilog, LaTex **Tools**:Cadence, Pytorch, Caffe, Vivado, HSpice