3.3V\_NUM\_\_\_ VSS\_26 J10 VSS\_27 J11 VDD\_9 J14 PK0 J15 PK1 J15 PK1 J16 PK1 J16 PK1 J17 VSS\_28 J17 VSS\_29 J17 VSS\_29 J17 VSS\_30 K1 PF6 K2 PF7 K4 PF8 K4 VSS\_31 K7 VSS\_31 K9 VSS\_32 K10 VSS\_33 K11 VSS\_33 K11 VSS\_33 K11 A1 VSS\_1
A2 P16
A3 P16
A3 P15
A4 P15
A5 P14
A6 P85
A6 P85
A7 VDD\_LDO\_1
A8 VCAP\_1
A8 VCAP\_1
A8 VCAP\_1
A8 PC10
A11 P09
A12 P05
A12 P05
A13 P04
A13 PC10
A15 PA15
A16 P11
A17 P10
A17 P10
A17 P10
A17 P10
A18 VSS\_2
B1 VSS\_2
B1 VSS\_3
B1 VSS\_3
B1 VSS\_3
B1 VSS\_3
B1 VSS\_1
B1 P11
B1 P15
B1 P16
B1 P1 D28 1 VVV FMC\_NBL3 33 FMC\_NBL2 ULPI\_D7 LTDC\_G5 LTDC\_G6 RESET# GND VCC-1 1 2 LTDC B6 GPIO\_IN\_3 SPI\_CLK SPI\_CLK UART7\_TX/TDI LTDC\_G4 3.3V\_NUM SPI\_MISO I2C\_SCL 3.3V\_ANA TRST GPIO\_OUT\_4 C57 LTDC\_B5

ETH\_TX\_EN

LTDC\_B3 UART5\_RX GPIO\_ ETH\_TXD0 FMC\_NWAIT UART5 TX ETH\_TXD1 GPIO\_OUT\_3
SPI\_MISO
TCK/SWCLK UART4\_TX UART4\_RX GPIO\_IN\_6 I2C\_SDA I2C\_SCL LTDC\_G3 UART7\_RX/SWO GPIO\_IN\_2 GPIO\_IN\_5 3.3V\_ANA FMC NBLO 3.3V ANA I2C\_SDA UART7\_RX/SWO LTDC\_B7 LTDC\_B4 ETH\_TXD1 ETH\_MDC ADC\_3
ADC\_6  $\triangle$ USBUP\_DP1 —

□LTDC G2 FMC\_NE1 UART5\_TX R26 GPIO\_OUT\_5

ETH\_MDIO

ETH\_REF\_CLK TMS/SWDIO R44 520 LTDC\_R1 1 SDNCAS LTDC\_DE R45 520 LTDC\_G1 LTDC\_G0 LTDC\_R7 ETH\_TXD0 R106 LTDC\_B2 LTDC\_B0 L 3.3V\_NUM

RCC\_MCO\_1

USART6\_TX

KEYBOARD\_INT D\_IN\_5 R158 ULPI\_NXT SDNWE | LTDC\_R0 | ؇57 | LTDC\_R2 | RTDC\_R2 | 2.2µ C82 R₹₹2 LTDC\_R0
LTDC\_R2
LTDC\_R4
LTDC\_R5
LTDC\_G1
LTDC\_G6 LTDC\_R6 \_1\_\_\_\_\_2 LTDC\_R3

LTDC\_R7

LTDC\_G0

LTDC\_G2 GPIO\_IN\_6 LTDC\_G6
LTDC\_G3
LTDC\_G5
LTDC\_B6
LTDC\_B7
LTDC\_B2
LTDC\_B4 PH10 | r13 | PH10 | P14 | PH11 | P14 | PH15 | P15 | PH16 | PH16 | PH17 | LTDC B3
LTDC B3
LTDC B5
ETH REF CLK
ETH RXXXXIII
LTDC CLK
SPI\_MOSI
ETH MDC
3.3V\_NUM 1 33 D3 \_\_\_\_ LTDC\_B4
ETH\_CRS\_DV
LTDC\_HSYNC
ETH\_RXD1
GPTO\_OUT\_1
LTDC\_DE
LCD\_BL\_CTRL KEYBOARD INT RCC\_MCO\_1
VBUS\_FS\_DP
VBUS\_FS\_DM ETH\_MDIO

3.3V\_NUM SDCLK USART6\_RX USART6\_TX  $\begin{array}{c|c} A2 & \begin{array}{c} & 1 \\ \hline \\ A1 & \\ \end{array} \\ \begin{array}{c} R118 & 1 \\ \hline \\ \end{array} \\ \begin{array}{c} 2 \\ \hline \\ \end{array} \\ \begin{array}{c} 33 \\ \end{array} \\ \begin{array}{c} 2 \\ \hline \\ \end{array}$ ETH\_RXD0 ULPI\_D2 R139 A15 33 0 100n C38 GPIO\_OUT\_6 USART1\_RX R132 1 2 2 1 1 2 33 D14 C47 GPIO\_OUT\_1

ETH\_RXD1

ULPI\_D1 J1-1 LTDC\_RQ R131

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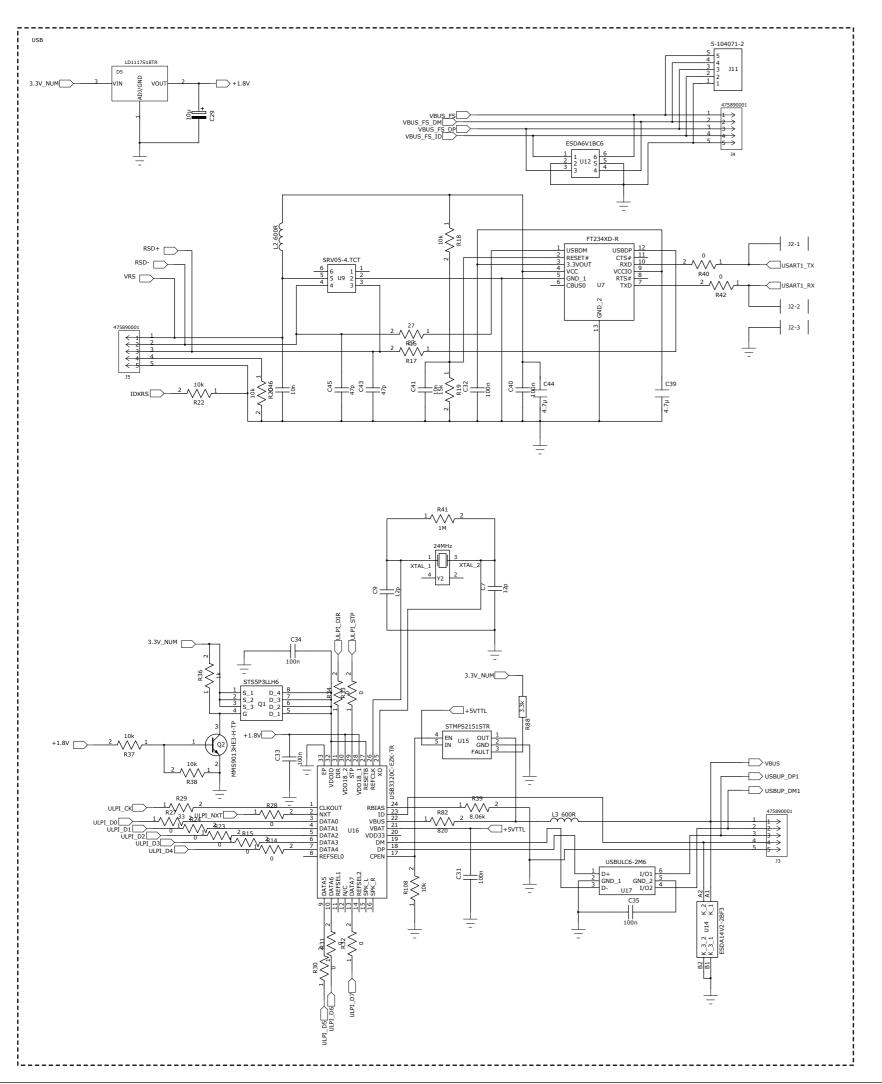
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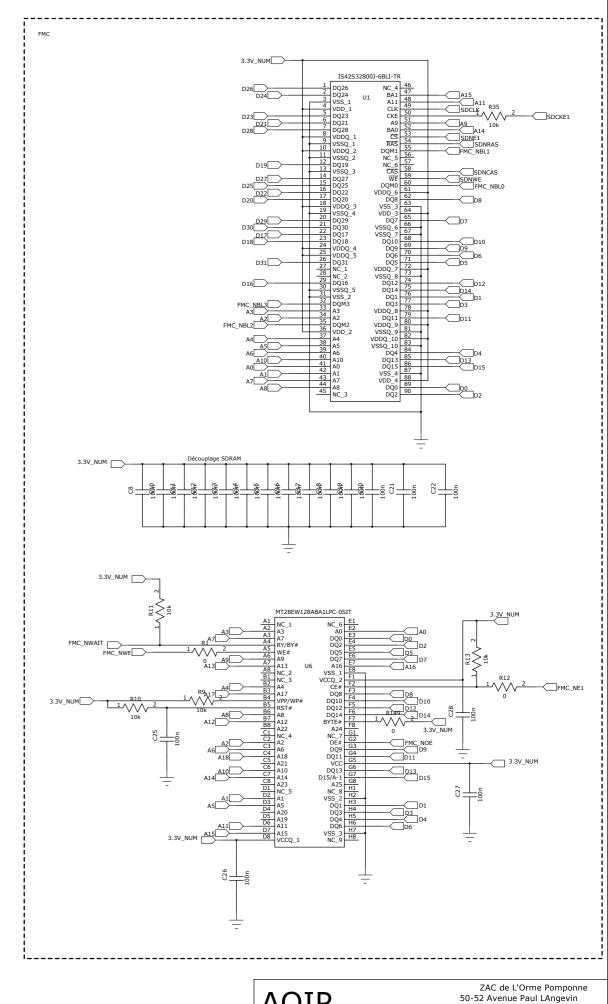
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38 J1-2 TCK/SWCLK A14 R121 R122 R122 A13 R123 32 33 J1-3 R126 Дер 11 2.2µ С81 J1-4 LTDC\_G7 UART7\_TX/TDI TMS/SWDIO  $\begin{array}{c|c}
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& & \\$ J1-5 RESET# UART7\_RX/SWO J7-1 J1-6 UART7 RX/SWO 中 ZAC de L'Orme Pomponne AOIP La Mesure Certifiée 50-52 Avenue Paul LAngevin 91130 RIS ORANGIS REVISION TYPE: uc IHM N PLAN: SPCA 50042-PID N C.I. : Ind. DESCRIPTION MODIF. DATE Designation: DGA Appareil: Rack polyvalent DGA

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 $AOIP_{\ {\scriptscriptstyle La\ Mesure\ Certifiée}}$ 91130 RIS ORANGIS REVISION N PLAN: SPCA 50042-PID N C.I. : DESCRIPTION MODIF

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