Arm China Zhouyi Compass Software

Version: 3.3

Technical Overview

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Arm China Zhouyi Compass Software

Technical Overview

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Contents
Arm China Zhouyi Compass Software Technical Overview

Preface

This preface introduces the *Arm China Zhouyi Compass Software Technical Overview*.

It contains the following sections:

- *About this book* on page 7.
- *Feedback* on page 10.

About this book

This Technical Overview is intended to provide an overview of the Zhouyi Compass Software for developers writing programs for Zhouyi *Neural Processing Units* (NPUs), bringing together information from a wide variety of sources useful to C and assembly language programmers. This document also introduces all the necessary tools to compile a neural network and run it on Zhouyi NPU devices. Hardware concepts such as scalar and *Direct Memory Access* (DMA) modules are covered where knowledge of the architecture is necessary to understand the principles of application programming. We will also look at ways to take full advantage of the capabilities of Arm China processors.

This is not an introductory level book. It assumes some knowledge of the C, OpenCL and assembly programming language and microprocessors, but not of any Arm China-specific background. We cannot hope to cover every topic in detail. In some chapters, we suggest additional reading (referring either to books or websites) that can give a deeper level of background to the topic in hand, but in this book we focus on the Arm China-specific detail. We will mention both GNU and Arm China tools in the course of the book. We hope that the book is suitable for programmers who have a desktop PC or x86 background and are taking their first steps into the Arm China NPU based world.

The book is meant to complement rather than replace other Arm China documentation available for Zhouyi series processors, such as the Arm China *Technical Reference Manual*s (TRMs) for the processors themselves, and documentation for integration and implementation.

Intended audience

This guide is for developers and programmers writing programs for Zhouyi NPUs.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter provides the basic features and architecture of Zhouyi NPUs.

Chapter 2 Memory operation
This chapter describes the operation of memory.

Chapter 3 NPU toolchain
This chapter describes the toolchain of Zhouyi NPUs.

Chapter 4 NPU NN compiler
This chapter describes the NPU *Neural Network* (NN) compiler.

Chapter 5 NPU driver
This chapter describes the driver of Zhouyi NPUs.

Chapter 6 NPU runtime
This chapter describes the runtime of Zhouyi NPUs.

Chapter 7 NPU simulator
This chapter describes the simulator of Zhouyi NPUs.

Chapter 8 Apache TVM
This chapter describes the Zhouyi Compass Apache TVM.

Chapter 9 CompassStudio
This chapter describes the Zhouyi NPU integrated development platform.

Appendix A NPU general-purpose registers summary
This appendix provides a summary of the general-purpose registers of Zhouyi NPUs.

Glossary

The Arm® Glossary is a list of terms used in Arm China documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm China meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`monospace`

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`

Denotes language keywords when used outside example code.

`<and>`

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

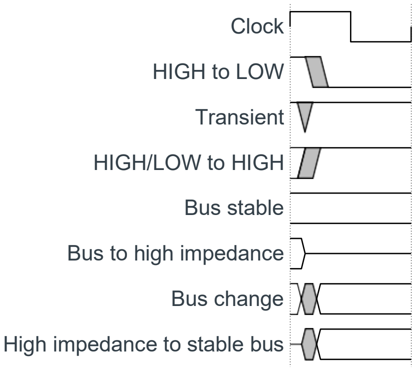

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.

Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm China publications

The following confidential documents are only available to licensees:

- *Arm China Zhouyi Z2 AIPU Technical Reference Manual*.
- *Arm China Zhouyi Z3 AIPU Technical Reference Manual*.
- *Arm China Zhouyi NPU X1 Technical Reference Manual*.
- *Arm China Zhouyi NPU X2 Technical Reference Manual*.
- *Arm China Zhouyi Compass Assembly Programming Guide*.
- *Arm China Zhouyi Compass C Programming Guide*.
- *Arm China Zhouyi Compass Debugger User Guide*.
- *Arm China Zhouyi Compass Getting Started Guide*.
- *Arm China Zhouyi Compass Apache TVM User Guide*.
- *Arm China Zhouyi CompassStudio User Guide*.
- *Arm China Zhouyi Compass NN Compiler User Guide*.
- *Arm China Zhouyi Compass Driver and Runtime User Guide*.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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- The number 61010011_0303_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm China also welcomes general suggestions for additions and improvements.

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Chapter 1
Introduction

This chapter introduces the basic features and architecture of Zhouyi NPUs.

It contains the following sections:

1.1 About Zhouyi NPUs

Zhouyi *Neural Processing Units* (NPUs) are domain flexible and highly power efficient processors that are dedicated to *Artificial Intelligence* (AI), deep learning and various machine learning processing. Zhouyi NPUs provide scalable performance for a wide range of end markets including surveillance, smartphones, drones, smart homes, automotive, robotics, medical and industrial applications.

Zhouyi NPUs have several notable features on the architecture and *Software Development Kit* (SDK). Zhouyi NPUs adopt a unified instruction set architecture that supports various standard and specific granularity of operations for AI and machine/deep learning needs. The architecture also provides easy support for customer-supplied fixed functions. For easy use of the NPUs, a comprehensive SDK that can support popular AI frameworks is available. Based on the innovative architecture and SDK, Zhouyi NPUs are versatile and can be easily integrated into the existing Arm ecosystem.

Zhouyi NPUs have an optional Security Extension, which enables the state-of-the-art security technology to redefine AI security levels.

There are different generations of processors based on the Zhouyi architecture:

- AIPUv1 processors, including the following products:
  - Z1_0701_P
  - Z1_0701
  - Z1_0904

Note

Zhouyi Compass does not support AIPUv1 processors anymore.

- AIPUv2 processors, including the following products:
  - Z2_0901
  - Z2_1002
  - Z2_1104
  - Z3_0901
  - Z3_1104
  - X1_1204
- AIPUv3 processors, including the following products:
  - X2_1204
  - X2_1204MP3

The features of AIPUv2 and AIPUv3 processors are described in *1.2 AIPUv2 NPUs* and *1.3 AIPUv3 NPU*. For more information, see the TRMs for these processors.

In this document, the *Artificial Intelligence Processing Unit* (AIPU) has the same meaning as the NPU.

The following figure shows the processors in a typical system.

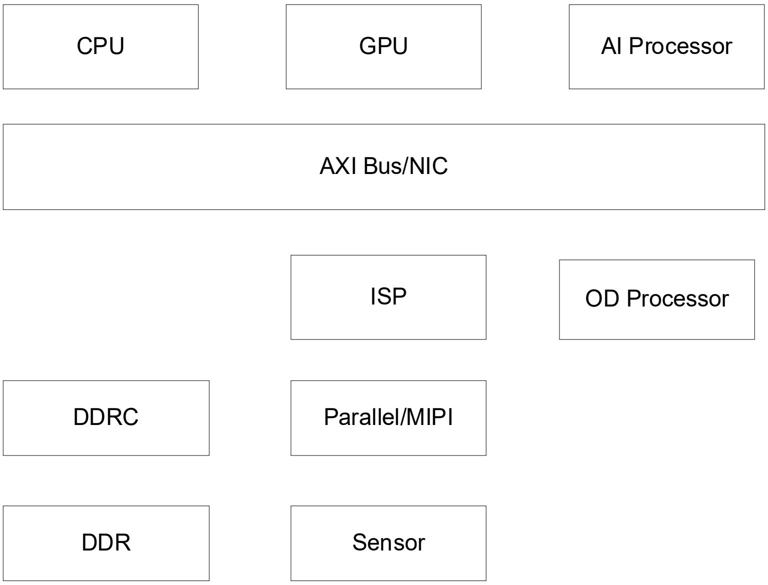


Figure 1-1 Example processor system

1.2 AIPUv2 NPUs

An AIPUv2 architecture based NPU works as an independent processor to apply AI calculation. It provides both general-purpose computing ability and AI-specific processing ability through different units:

- General purpose.
  - —Scalar
  - —Vector/Tensor
- *AI Fixed Function* (AIFF) accelerator.

All the compute units have register files and local SRAM wherever necessary. The whole pipeline also has various memories such as instruction and data caches, and *Tightly-Coupled Memory* (TCM).

The following figure shows the components of a typical Zhouyi NPU.

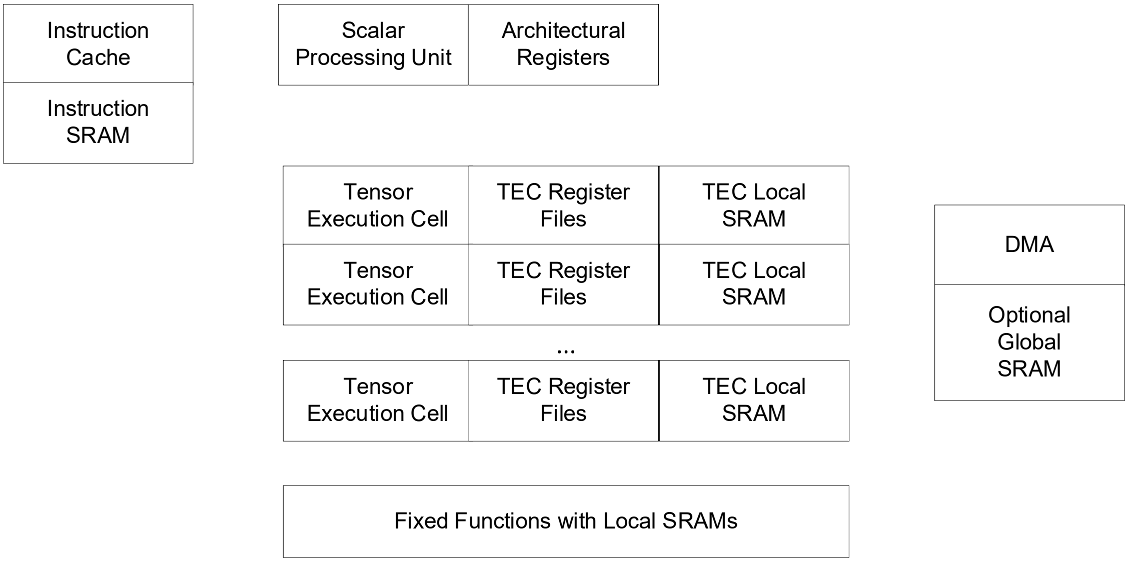


Figure 1-2 Components of an AIPUv2 NPU

The NPUs include the following features:

- A *Reduced Instruction Set Computer* (RISC) based *Very Long Instruction Word* (VLIW) architecture with four instruction slots, containing both scalar and vector/tensor processing instructions.
  - — Slot 0: Scalar instructions or vector arithmetic instructions other than *Tensor Processing Cluster* (TPC) *Multiply-Accumulate* (MAC).
  - — Slot 1: TPC MACs.
  - — Slot 2: TPC load/store instructions to local SRAM.
  - — Slot 3: Scalar arithmetic instructions or TPC load/store instructions to global SRAM.
- An in-order issue pipeline for both scalar and the TPC.
- One or more *Tensor Execution Cell* (TECs) in the TPC to form super wide vectors.
- Suitable TEC numbers in different scenarios.
- 32 x 32-bit scalar register (Rn, Rm, Rd, Rc).
- Each TEC contains:
  - — 32/16 x 256-bit tensor vector register (Tn, Tm, Td).
  - — 4 x 256-bit tensor accumulation register (Acc).
  - — 8 x 32-bit predication register (Pg, Pn, Pd).

- 8 x 32-bit address register (2 read-only and 6 read/write via control) (An, Ad).

- Scalar:
  - Support for zero-overhead loops.
  - Support for misaligned load/store.
  - Non-blocking load/store.
  - Support for Contiguous/Stride load/store in global SRAM.
  - Unified instruction cache.
  - Dedicated scalar data cache (not supported in Zhouyi Z3_0901/Z2-0901).
  - Instruction scratch pad RAM (not supported in Zhouyi Z3_0901/Z2-0901/Z2-1002).
  - Integer DIV/Mod instruction.
  - Additional compare instruction.
  - Support for data cache write-through mode.
- TPC:
  - Support for int8 and int16 vector operations, with extended accumulation precision up to int32 and additional support for int32 vector operation.
  - Additional copy instruction to move TEC register values to scalar registers.
  - Load/Store operation access to local SRAM and global SRAM.
  - Support for misaligned load/store.
  - Non-blocking load/store.
  - Support for Contiguous/Stride load/store in both local and global SRAM.
  - Support for Gather-load/Scatter-store in local SRAM.
  - Support for predication vector operations.
- AIFF/HWA:
  - PE array of convolution and fully connected layer.
  - Max/Min and average pooling.
  - Support for RGB/NC’HWC32 (8-bit data)/NC’HWC16 (16-bit data) input format (not supported in Zhouyi Z2).
  - Flexible LUT table for nonlinear functions like ReLU, Sigmoid, and TanH.
  - *Batch Normalization* (BN).
  - Bias.
  - Elementwise.
  - Relu/PRelu.
  - Depthwise convolution.
  - Dilated convolution with fixed dilated factors (not supported in Zhouyi Z3/Z2).
  - Max/Min/Average Pooling with regular NN size and configurations.
  - Deconvolution zero skipping (not supported in Zhouyi Z3/Z2).
  - Support for bilinear/nearest interpolation (not supported in Zhouyi Z3/Z2).
  - Weight compression format.
  - Configurable Winograd F(2,3) for int8*int8 (not supported in Zhouyi Z3-0901/Z2).
  - ROI pooling (not supported in Zhouyi Z2).
  - Output Activation Inflight Compression (not supported in Zhouyi Z3-0901/Z2).
  - Input Activation Inflight Decompression (not supported in Zhouyi Z3-0901/Z2).

- — Sparse zero-skipping (not supported in Zhouyi Z2).
- Interlock unit:
  - — Key deposit/key deposit support for each major unit.
  - — Key box units to support FIFO mode.
- DMA:
  - — 2D and 3D data movement operation.
  - — Data format transformation among NHWC/NCHW/NC’HWC$_{32}$ (8-bit data format)/NC’HWC$_{16}$ (16-bit data).
  - — Support for transpose.
  - — Data upsampling.
  - — Immediate Mode.
- TrustZone:
  - — Support for TrustZone Secure/Non-secure configuration.
- *Performance Counter* (PFC):
  - — Performance counters can be configured to monitor several event metrics.
- Debug function.
- Support for *Data Tightly Coupled Memory* (DTCM) access (not supported in Zhouyi Z3-0901/Z2).
- Support for NPU IP soft reset (not supported in Zhouyi Z3-0901/Z2).

1.3 AIPUv3 NPU

An AIPUv3 NPU introduces an extensible multi-cluster and multi-core architecture. When an NPU has only one core and one cluster, it can act as a single-core NPU. Each core provides both general-purpose computing capability and AI-specific processing capability with different processing units.

- General purpose
  - — *Scalar Processing Unit* (SPU)
  - — *Vector/Tensor Processing Engine* (VPE)
  - — Optional *Floating-point Processing Unit* (FPU)
- *AI Fixed Function* (AIFF) accelerator

Zhouyi NPU X2 can be configured as a single core, multiple cores, or multiple clusters. By default, it includes all hierarchy levels and may simplify some levels to match the configuration.

The following figure shows the overall hierarchy of Zhouyi AIPUv3 NPU (Zhouyi X2).

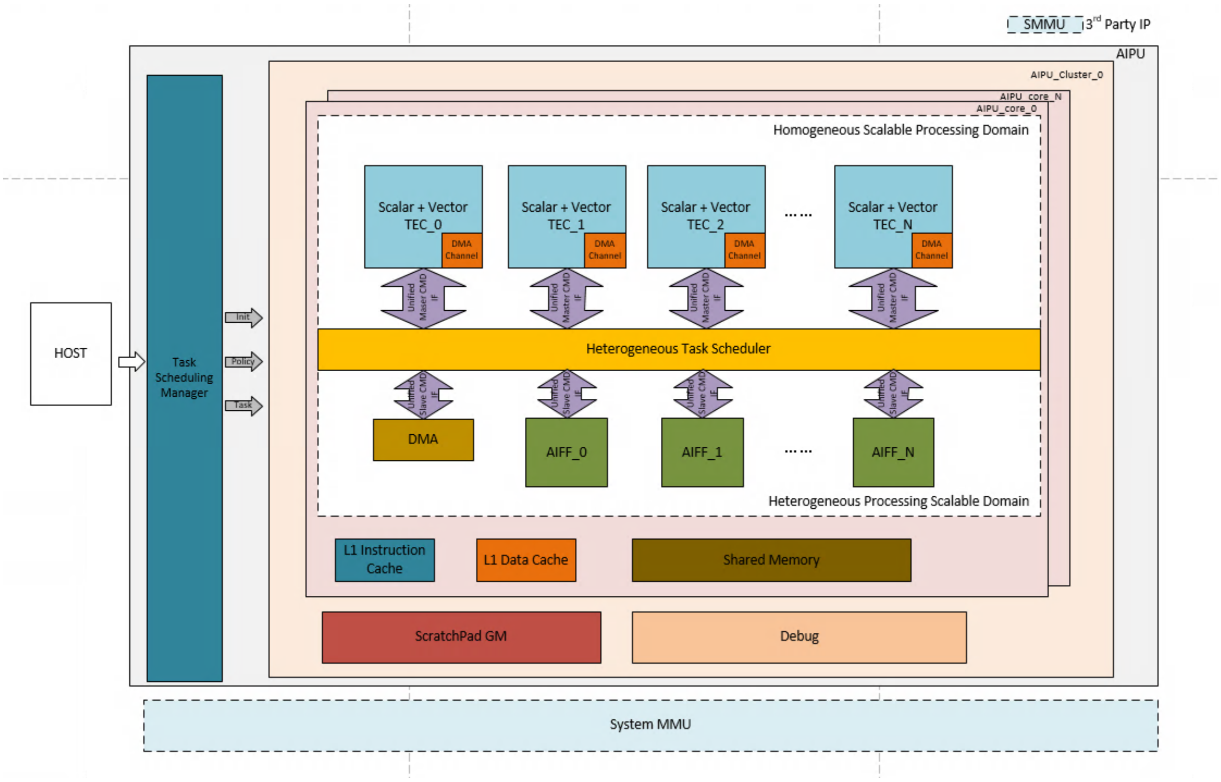


Figure 1-3 Components of an AIPUv3 NPU

The NPU includes the following features:

Multi-Cluster (MC) and *Multi-Core* (MP)

- An NPU chip can contain multiple clusters.
  - — For the Zhouyi NPU X2_1204MP3/X2_1204, the number of clusters is 1.
- Each cluster consists of multiple cores.
  - — For the Zhouyi NPU X2_1204MP3, the number of cores is 3. For the Zhouyi NPU X2_1204, the number of cores is 1.
- Each core consists of multiple *Tensor Execution Cells* (TECs).
  - — For the Zhouyi NPU X2_1204MP3/X2_1204, the number of TECs is 4.
- Common host interface to serve task control and scheduling.

Memory hierarchy

- Unified memory addressing except local memory.
- Independent instruction buffer and shared L1 instruction cache across multiple TECs.
- Independent data buffer and shared L1 data cache across multiple TECs.
- *Local Memory* (LM) for each TEC. LM is accessible by AIFF tasks. No cross-TEC LM access is allowed.
- *Shared Memory* (SM) for TECs within the same core.
- Scratchpad *Global Memory* (GM).
- All function units have direct access to external memory.
- *Task Configuration Block* (TCB) access is independent memory access and non-cacheable.

TEC overall functionality

- A *Reduced Instruction Set Computer* (RISC) based *Very Long Instruction Word* (VLIW) architecture with four instruction slots, containing both scalar and vector/tensor processing instructions.
- 4-slot 128b/2-slot 64b/1-slot 64b variant instruction packet length
- In-order issue pipeline
- 256-bit SIMD lane data width
- Independent instruction fetching in multiple TECs through unified L1 instruction cache
- 2x ALU throughput and VLIW slots combination
- Unified DMA and AIFF command channel
- Unified *Load Store Unit* (LSU) for both scalar and vector, all memory hierarchy
- No coherence across TECs within the same core
- Register files per TEC:
  - 32 x 32-bit scalar register (Rn, Rm, Rd, Rdn)
  - 32 x 256-bit tensor vector register (Tn, Tm, Td, Tdn).
  - 8 x 32-bit predication register (Pg, Pn, Pm, Pd, Pdn).
  - 32 x 32-bit floating-point register (Fn, Fm, Fd, Fdn) integrated with vector register's low 32-bit.

TEC general-purpose functions

- *Scalar Processing Unit* (SPU)
  - Support for 32-bit scalar operations
  - Support for control flow instructions
- *Vector Processing Engine* (VPE)
  - Support for signed/unsigned int8/int16/int32 vector operations
  - Vector engine to support merge mode predication by default
  - Additional copy instruction to move TEC register values to scalar registers
  - Support for predication vector operations
- *Load Store Unit* (LSU)
  - Load/Store operation access to all memory hierarchy
  - Support for misaligned load/store
  - Support for non-blocking load/store
  - Support for Contiguous/Stride load/store
  - Support for Gather-load/Scatter-store
- *Floating-point Processing Unit* (FPU)
  - Scalar/Vector floating-point pipeline integrated into the vector pipeline
  - Support for FP32/FP16/BF16 operations
  - Support for mix-precision operations
  - Support for *Matrix Multiply Accumulation* (MMA) with 4:2 weight sparse support in FP16/BF16
- *Segmented MMU* (SegMMU)
  - 4-segment remapping
  - Fixed ASID 0

- Segment read/write privilege

AI Fixed Functions

- *Matrix-to-Tensor Processing* (MTP)
  - Two MTPs available for independent tasks, batch tasks, or partitioned tasks
  - New PE array structure that consists of PE
  - Each PE supports 8 * int8 * int8 / 2 * int16 * int16 MAC
  - Winograd F(2,3) for int8*int8
  - Each MTP with 4096 MAC addresses
  - Support for NC'HWC32 (8-bit data)/NC'HWC16 (16-bit data) input format
  - Support for HWC/CHW RGB input format
  - Direct convolution
  - Support for FC
  - Dilated convolution with fixed dilated factors
  - Bypass function
  - Average Pooling with wide configuration options
  - Deconvolution zero skipping
  - Activation zero skipping for convolution or FC
- *Intra-Tensor and Inter-Tensor Processing* (ITP)
  - M0/M1/E/LUT/OCVT function pipeline
  - Three different configurations for MTP_0/MTP_1/ITP result loopback
  - Support for bilinear/nearest interpolation
  - Intra-Tensor Operation:
    - Batch Normalization
    - Bias Addition and Subtraction
    - Elementwise Addition and Subtraction
    - Relu/PRelu
    - Programmable LUT function
    - Input and intermediate signed 32-bit integer
    - Output 32-bit, 16-bit, or 8-bit data
  - Inter-Tensor Operation:
    - Input tensor merging with addition and multiplication
    - Input tenor concatenation
- *Planar-to-Tenor Processing* (PTP)
  - Depthwise convolution
  - Max/Min/Average Pooling with regular NN size and configurations
  - ROI pooling
  - Fixed dilated factor for depthwise convolution
  - FC
  - Support for 8-bit and 16-bit integer data formats
  - Dedicated pDMA channel
- *Unified Buffer* (UnB)
  - Support for consumer prefetch, read, and write
  - Direct request to external memory
  - Dedicated uDMA to support prefetch or direct write-out for context switch
- *Write Buffer* (WrB)
  - Two write result collections
  - Dedicated wDMA for output activation output and inflight compression
  - Data format transformation
- *Segmented MMU* (SegMMU)
  - 4-segment remapping
  - ASIDs remapping

  - Segment read/write privilege
- Sparse
  - Weight Sparse Inflight Decompression
  - Output Activation Inflight Compression
  - Input Activation Inflight Decompression

DMA

- 2D and 3D data movement operation
- Data format transformation among NHWC/NCHW/NC'HWC$_{32}$ (8-bit data format)/NC'HWC$_{16}$ (16-bit data)
- Support for transpose
- Data upsampling
- Immediate mode
- *Segmented MMU* (SegMMU)
  - 4-segment remapping
  - ASIDs remapping
  - Segment read/write privilege

Interconnect

- Multiple virtual channels on each master node
- By-directional compressed physical channel
- Double bandwidth on hotspot
- Mesh network for easy layout

Synchronization

- Host synchronization control
- Cross-TEC synchronization
- Sync Flag within a TEC

MBIST

- Optional support for single shared MBIST access interface
- Separate MBIST block for TEC, AIFF, Scalar, DMA, LM, SM, and GM

TrustZone

- Support for TrustZone Secure/Non-secure configuration

Power aware

- Q channel power interface protocol
- AIPU core-level power domain, no register/memory retention

Debug and other features

- Debug function
- Support for NPU IP soft reset

1.4 Registers

This section provides information about system registers with implementation defined bit fields and implementation defined registers associated with the core.

Arm China classifies the NPU registers into six types based on the access ways:

- General-purpose registers used as operand or destination directly.
- Architecture control registers accessed by data move instructions such as mtctrl0/mfctrl0.
- Architecture control registers accessed by data move instructions such as mtctrl1/mfctrl1.
- Architecture control registers accessed by data move instructions such as mtctrl2/mfctrl2.
- Memory-mapped registers accessed by load/store instructions.
- Memory-mapped registers accessed by external bus slave interface.

For more information about the NPU general-purpose registers summary, see *Appendix A NPU general-purpose registers summary*.

1.5 Software architecture

The Zhouyi software development kit includes the following components:

- Toolchain. For more information, see *Chapter 3 NPU toolchain*.
- NN compiler. For more information, see *Chapter 4 NPU NN compiler*.
- Driver and runtime. For more information, see *Chapter 5 NPU driver and runtime*.
- Simulator. For more information, see *Chapter 6 NPU simulator*.
- Apache TVM. For more information, see *Chapter 7 Apache TVM*.
- CompassStudio. For more information, see *Chapter 8 CompassStudio*.

Chapter 2
Memory operation

This chapter describes the operation of memory.

It contains the following sections:

2.1 AIPUv2 NPU memory hierarchy

2.1.1 Overview

This section describes different memory units of AIPUv2 NPUs. For more information about programming with assembly or C compiler, see the *Arm China Zhouyi Compass Assembly Programming Guide* and *Arm China Zhouyi Compass C Programming Guide*.

The following figure shows the memory hierarchy of AIPUv2 NPUs.

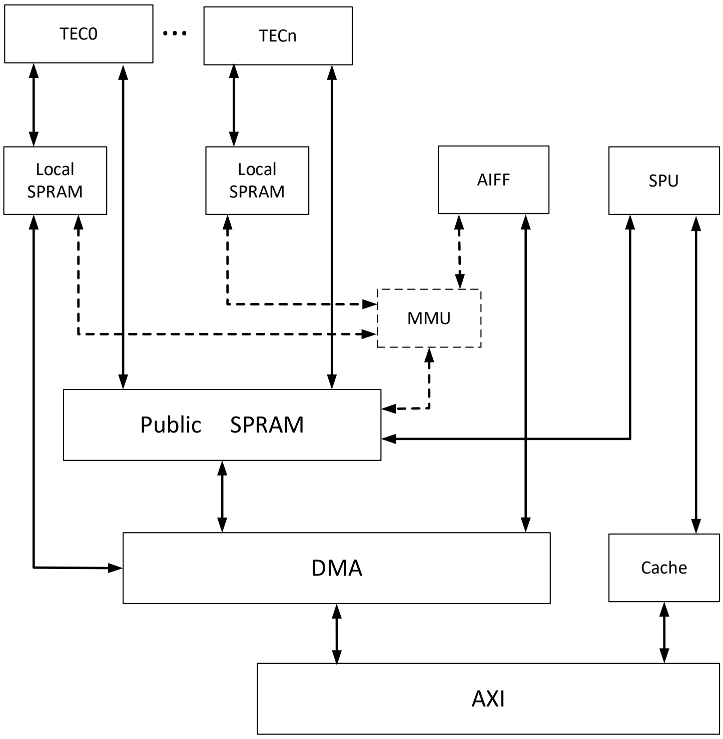


Figure 2-1 AIPUv2 NPU memory hierarchy

2.1.2 Memory space

The following figure shows an overview of the memory space of Zhouyi AIPUv2 NPUs.

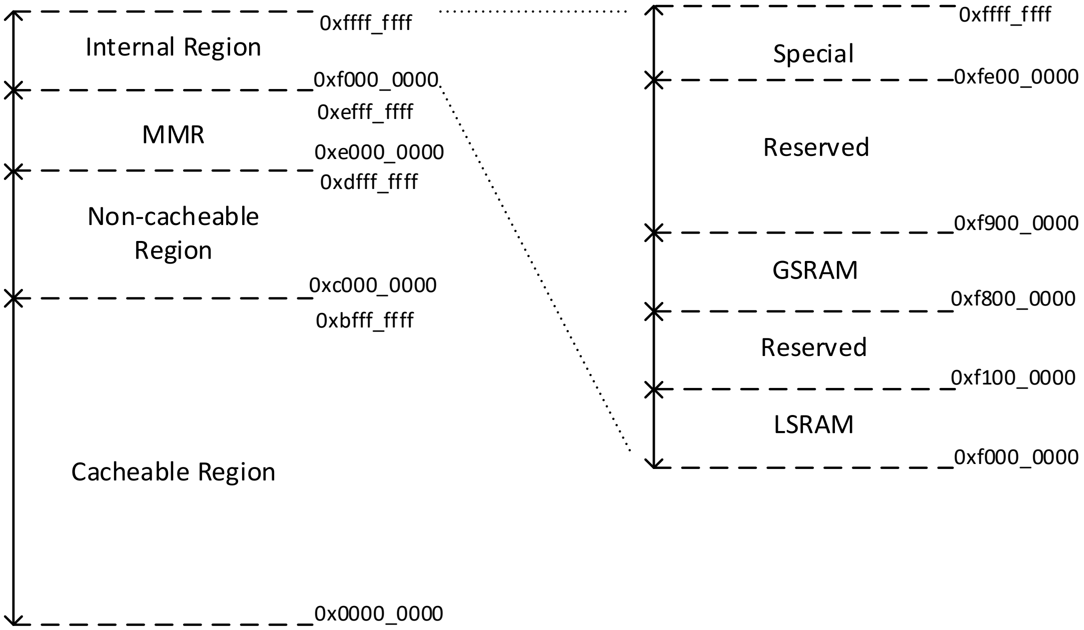


Figure 2-2 AIPUv2 NPU memory space

2.1.3 TEC local SRAM

Each TEC of an AIPUv2 NPU has its local SRAM that is divided into two halves for ping-pong buffer. Each TEC accesses its local SRAM by tensor load/store instructions with the base address in address registers and the offset.

Only the instructions in slot 2 can access the local SRAM by TECs.

Each half of the local SRAM can be accessed either by TPC load/store instructions or DMA. The order between the two requests shall be maintained by software. That is, if both request sources try to access the same half of memory, the data order can be unpredictable and might result in data inconsistency.

Therefore, it is strongly recommended that the TPC and DMA operate in different half of the local SRAM.

2.1.4 Global SRAM

AIPUv2 NPUs have global SRAM for the access of the TPC and scalar core. TECs access the global SRAM by tensor load/store instructions with the base address in address registers and the offset.

Unlike parallel access to TEC local SRAM, the global SRAM is accessed by TECs one by one, so only the data shared by TECs shall be stored in the global SRAM for higher efficiency. Software uses **mfctrl** to read address registers and uses **mtctrl** to write address registers.

Note that only the instructions in slot 3 can access the global SRAM by TECs.

The scalar core accesses the global SRAM by scalar load/store instructions with the corresponding addresses.

The order between the TPC and scalar load/store instructions within the same VLIW instruction packet will be considered as parallel processing. That is, the data order is unpredictable when the TPC and scalar load/store instructions are accessing the same global SRAM address.

The data order is strictly guaranteed between different VLIW instruction packets in the global SRAM.

Each half of the global SRAM can be accessed either by TPC/scalar load/store instructions or DMA. The order between the two requests shall be maintained by software. That is, if both request sources try to access the same half of memory, the data order can be unpredictable and might result in data inconsistency.

Therefore, it is strongly recommended that the TPC and DMA operate in different half of the global SRAM.

2.1.5 DMA operation

The DMA of an AIPUv2 NPU is software controlled to perform data movement between the internal memory and external memory space. Similar to the AIFF operation, there are two modes supported—MMR configuration mode and descriptor mode. These two modes cannot work at the same time. When software needs to change the mode, it needs to ensure that the DMA is idle.

There are two types of registers—global register and channel register. For global registers, software should be programmed correctly before enabling any channel to work.

Register configuration mode

To work in the register configuration mode, software shall perform the following configuration:

- Set Control_mode to `1'b0` in the Common Control Register.
- Choose the channel to perform the data movement. Set the corresponding CHn registers to configure the movement. Ensure that all the registers of the specified channel are configured, and set the START bit in the CHn Control register.

Note

- Always choose the idle channel to perform the data movement. If the chosen channel is not in idle state, all the registers cannot be written.
- Before configuring a channel, read the START bit of that channel to check whether it is working. START=0 means that it is idle.

For more information about DMA channel N, see the *Arm China Zhouyi NPU X1 Technical Reference Manual*. Each channel works independently.

Channel N can be set up using the following programming flow:

1. Program the external memory (AXI) side start address.
2. Program the external memory (AXI) side width and stride.
3. Program the external memory (AXI) side trans number and trans size.
4. Program the external memory (AXI) side address gap between two trans.
5. Program the internal memory (RBUS) side start address.
6. Program the internal memory (RBUS) side width and stride.
7. Program the internal memory (RBUS) side trans number and trans size.
8. Program the internal memory (RBUS) side address gap between two trans.
9. Program the channel control register including ASID/OP_MODE/DATA_UNIT/DIRECTION and then start the DMA channel.

Note

If two channels target to the same write address space, software shall ensure that one channel is finished before another one starts or use KB to ensure the sequence. The DMA does not guarantee the write order.

Configuration error report

The following rules will be checked by the hardware. If any of these rules is not followed, the DMA of an AIPUv2 NPU will report a configuration error in the corresponding channel status register.

- The width, stride, num_trans, and trans_size shall be all larger than 0.
- The width should be no larger than stride.
- The whole size of data movement should not cross the 4GB boundary.
- The total size of data movement shall be equal between the internal and external sides.
- The data unit shall not be a reserved value.
- For upsampling, it only supports the direction from internal to external.
- For transpose, it only supports the direction from external to internal.
- The internal address shall be a valid address range in the TEC.

DMA registers

The DMA of an AIPUv2 NPU is controlled by registers. For more information, see the *Technical Reference Manuals* (TRMs) delivered with the Arm China Zhouyi products.

2.2 AIPUv3 NPU memory hierarchy

2.2.1 Overview

This section describes different memory units of an AIPUv3 NPU. For more information about programming with assembly or C compiler, see the *Arm China Zhouyi Compass AIPUv3 Assembly Programming Guide* and *Arm China Zhouyi Compass OpenCL Programming Guide*.

The following figure shows the memory model of an AIPUv3 NPU.

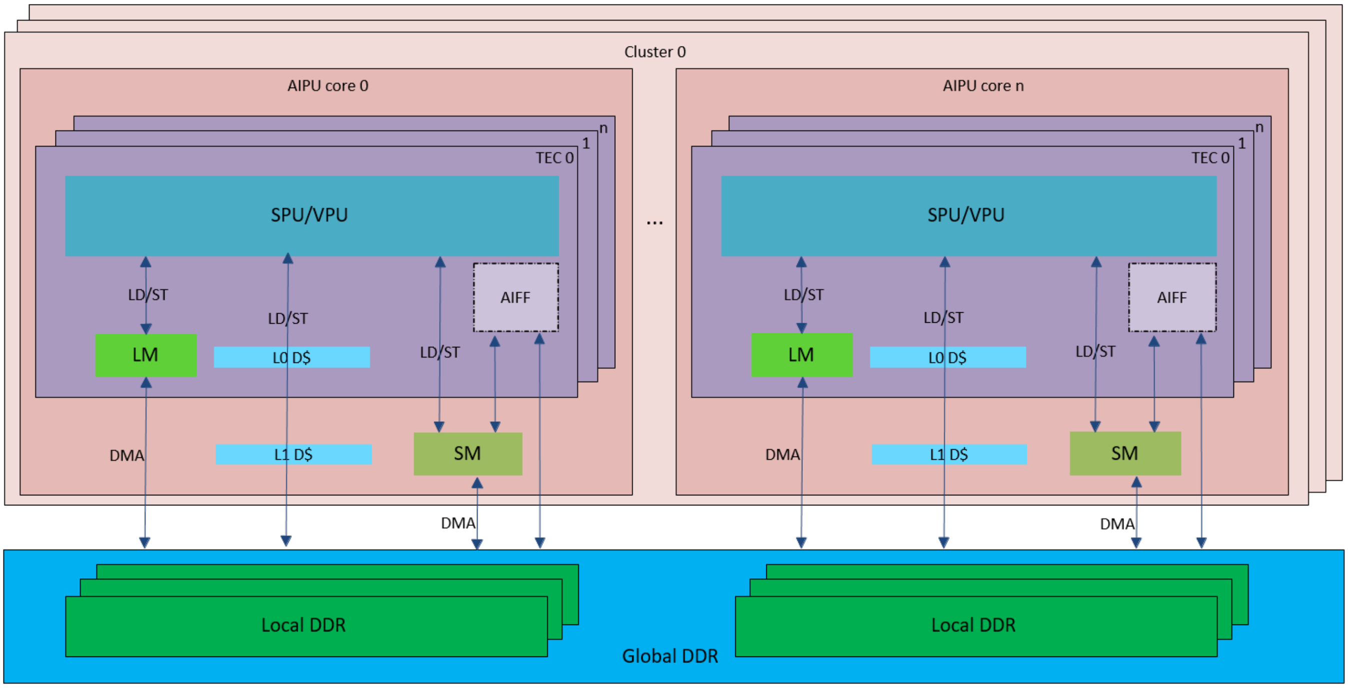


Figure 2-3 AIPUv3 NPU memory model

2.2.2 Memory space

The following figure shows an overview of the memory space of a Zhouyi AIPUv3 NPU.

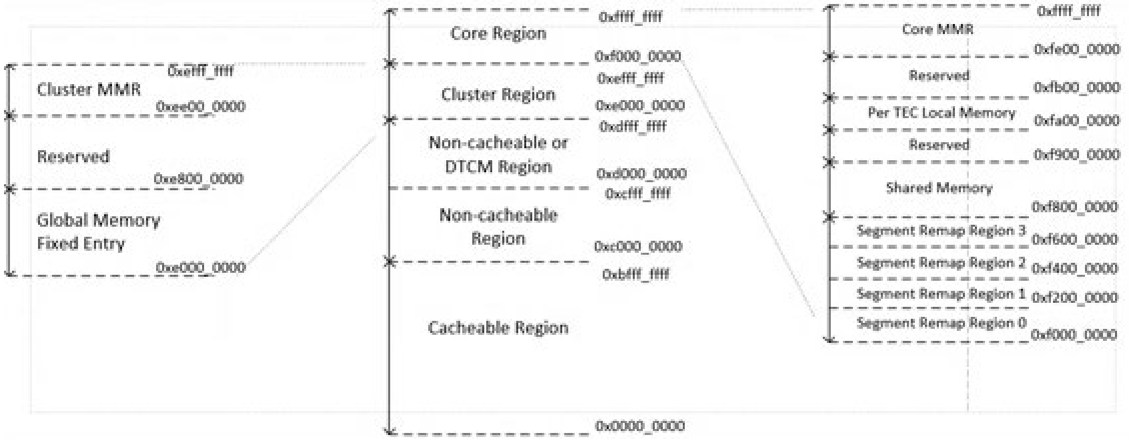


Figure 2-4 AIPUv3 NPU memory space

2.2.3 Local Memory and Global Memory

Local Memory (LM) is TEC local SRAM, while the local DDR stores TEC private variable data. *Shared Memory* (SM) is shared SRAM which is shared by all TECs in a core, while the global DDR stores kernel global data.

The SPU/VPU can access its local SRAM, shared SRAM or DDR by load/store instructions with addresses.

Because of the asynchronous functionality of the DMA module, Arm China recommends that you do not use the load/store instructions to access the same memory location before the DMA transmission completes. For more information about the DMA operation, see the relevant *Technical Reference Manuals* (TRMs) delivered with the Arm China Zhouyi products.

2.2.4 DMA operation

In an AIPUv3 NPU, DMA is a virtual hardware resource for all TECs to use in a core.

Different from the AIPUv2 NPUs, there is a distributed DMA system to execute DMA instructions. There is a local DMA in LM/SM respectively to execute LM/SM related direct move transfer, while all other operations and other transfer targets are executed by a dedicated DMA.

For more information about DMA instructions, see the *Arm China Zhouyi Compass AIPUv3 Assembly Programming Guide*.

Chapter 3
NPU toolchain

This chapter describes the NPU toolchain.

It contains the following sections:

3.1 About the NPU toolchain

To facilitate the programming for the NPU and take full advantage of hardware features, Arm China provides a basic toolchain for all level programmers. The NPU toolchain includes compiler, assembler, and linker. With these tools, programmers can develop their own AI operations on the NPU.

- For AIPUv2 NPUs, Arm China provides the NPU C toolchain. For more information, see *3.2 NPU C toolchain*.
- For an AIPUv3 NPU, Arm China provides the NPU OpenCL toolchain, see *3.3 NPU OpenCL toolchain*.

3.2 NPU C toolchain

3.2.1 NPU C toolchain compilation process

After completing the coding of an operator, you need to compile the code and generate the final binary file that can be run on the NPU. The compilation process is similar to the traditional compilation process, including compilation, assembly and linking.

The following figure shows the compilation process.

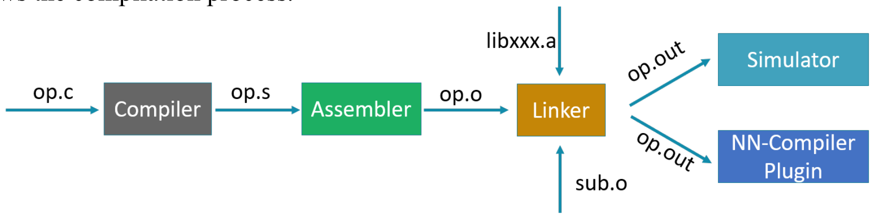


Figure 3-1 Compilation process

In the compilation stage, the `.c` source file is compiled through NPU C compiler `aipucc` to generate a `.s` assembly file. In the assembly stage, the `.s` file is turned into a `.o` object file by assembler `aipuas`. In the final stage, linker `aipuld` links one or more `.o` files and the dependent `.a` static library file and generates the final `.out` binary file.

For some special functions (like `printf`), the driver support is also needed. For more information, see *Chapter 4 NPU NN compiler* and *Chapter 5 NPU driver*.

The final compiled `.out` binary files can run on the NPU simulator directly, or are integrated in the NN compiler by plugins. For more information, see *Chapter 4 NPU NN compiler* and *Chapter 7 NPU simulator*.

3.2.2 NPU C toolchain C compiler

For high level programming, Arm China provides NPU C which is based on C programming language with some extensions, and also provides an NPU C compiler named `aipucc`.

Like the traditional C programming language, NPU C supports scalar data type and scalar operators. In addition, NPU C has the following major extensions:

- Function qualifier `__entry` to specify an entry function. An entry function defines the entry point of an NPU C program. This function is similar to the main function in C.
- Address space qualifiers to distinguish three different memory regions of the NPU. Qualifier `__gsram0`/`__gsram1` is for the global SRAM, and `__lsram0`/`lsram1` is for the local SRAM.
- Vector data types for TPC programming. The vector data types include tensor vector types that are used to place data and predicate vector types that are used to set computing masks.
- Vector built-in functions to simplify TPC programming.
- High level DMA functions to simplify DMA operations.
- `printf` for debugging.

The NPU C compiler supports all the Zhouyi AIPUv2 series platforms. The compiler provides the `-mcpu` option to specify the process that you want the program to run on. This compiler option is the most important option that you need to know.

The NPU C compiler supports multi-level optimization. Arm China recommends that you use `-O0` for development and use `-O2` for release that requires higher performance.

Note the options in the following compilation commands for `aipucc`:

- To generate the assembly code file for Zhouyi Z2-1104 with the `-S` option, use optimization level `O0`:

```
$aipucc -O0 -mcpu=Z2_1104 -S test.c
```

- To generate the object file for Zhouyi Z2-1002 with the `-c` option, use optimization level `O2`:

  ```
  $aipucc -O2 -mcpu=Z2_1002 -c test.c
  ```

- To generate the executable object file for the NN compiler or simulator, link with `libcommon.a`:

  ```
  $aipucc -O2 -mcpu=Z2_1104 test.c -Lpath_to_libcommon.a -lcommon -o test.out
  ```

For more information about the NPU C programming and NPU C compiler, see the *Arm China Zhouyi Compass C Programming Guide*.

3.2.3 NPU C toolchain assembler

As shown in the compilation process, the NPU C toolchain assembler `aipuas` translates the assembly language code into the objective machine code. If you are familiar with the NPU assembly language, you can program for the NPU with the assembly language directly.

The NPU C toolchain assembly language syntax is the same as the normal assembly language syntax, except for some small differences. The NPU assembler supports instructions, directives, and user-defined macros.

The key features of `aipuas` are:

- Zhouyi NPU unified assembly language.
- Zhouyi NPU scalar and TPC instructions.
- Zhouyi NPU function module operation instructions.
- Directives in assembly source code.
- Processing of user-defined macros.

The following shows a simple example of using `aipuas`:

```
$aipuas input.S -mcpu=Z2_1104 -o output.o
```

The only thing that you need to know is the `-mcpu` option. This option supports all the Zhouyi series platforms.

For more information about the NPU C programming and NPU C compiler, see the *Arm China Zhouyi Compass Assembly Programming Guide*.

3.2.4 NPU C toolchain linker

The NPU C toolchain linker `aipuld` is used to link objective files to an executable file.

The following shows the simple usage of the NPU C toolchain linker:

- To generate an executable object file with linker `aipuld` for a single file, link with `libcommon.a`:

  ```
  $aipuld -static test.o -Lpath_to_libcommon.a -lcommon -o test.out
  ```

- To generate an executable object file with linker `aipuld` for multiple files, run the following:

  ```
  $aipuld -static test1.o test2.o -o test.out
  ```

3.2.5 NPU C toolchain debugger

Arm China also provides a debugger named `aipudbg` for debugging NPU applications on the NPU simulator or actual hardware. `aipudbg` allows you to set breakpoints and single-stepping, and to inspect and modify memories and variables. Currently, the NPU debugger can support Linux platform and Android platform.

Debugging on the simulator platform enables you to debug applications without actual hardware.

Debugging on the hardware platform requires actual extra peripherals to communicate between the client and actual hardware.

In multi-instance mode, only hardware targets are supported for debugging. The core should be specified before an application is launched in the debugger.

To debug an application, add the `-g` option when performing compilation with `aipucc`. In addition, '`-O0`' is highly recommended because the higher optimization level and the bundle strategy will mess up debugging information. For example:

```
$ aipucc -O0 -g -mcpu=Z2_1104 test.c -o test.out
```

The following table describes the common debug commands. For more information about the NPU debugger, see the *Arm China Zhouyi Compass Debugger User Guide*.

Table 3-1 Common debug commands of `aipudbg`

Command	Description
`platform select <platform-name>`	Create a platform and select it as the current platform.
`platform connect <connect-url>`	Select the current platform by providing a connection URL.
`target create <target-file>`	Create a target using the argument as the main application.
`settings set target.run-args <configuration-file> [core-id=Number]`	Set the run arguments with the configuration file and the core ID for multi-instance mode. The core ID is 0 by default. `core-id` is only used for hardware targets.
`breakpoint set <cmd-options>`	Set a breakpoint or a set of breakpoints in the executable using the options.
`breakpoint delete <cmd-options>`	Delete the specified breakpoint(s). If no breakpoints are specified, delete them all.
`watchpoint set expression|variable <cmd-options>`	Commands for setting a watchpoint.
`watchpoint delete <cmd-options>`	Delete the specified watchpoint(s). If no watchpoints are specified, delete them all.
`process launch`	Launch the NPU application in the debugger.
`thread step-in`	Source level single step, stepping into calls.
`thread step-over`	Source level single step, stepping over calls.
`thread continue`	Commands for operating on one or more threads in the current process.
`thread backtrace`	Show thread call stacks.
`memory read <cmd-options> <address-expression>`	Read from the memory of the current target process.
`memory write <cmd-options> <address> <value> [<value> [...]]`	Write to the memory of the current target process.
`register read <cmd-options> [<register-name> [...]]`	Dump the contents of one or more register values from the current frame. If no register is specified, dumps all general-purpose registers.
`register write <register-name> <value>`	Modify a single register value.

3.3 NPU OpenCL toolchain

3.3.1 NPU OpenCL toolchain compilation process

After completing the coding of an operator with OpenCL, you need to compile the code and generate the final binary file that can be run on the NPU. The compilation process is similar to the traditional compilation process, including compilation, assembly and linking.

The following figure shows the compilation process.

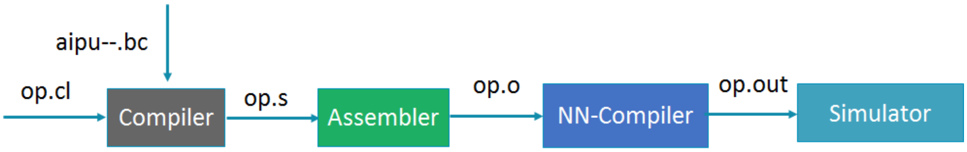


Figure 3-2 NPU OpenCL toolchain compilation process

In the compilation stage, the `.cl` source file is compiled through NPU OpenCL C compiler `aipuocc` to generate a `.s` assembly file. In this stage, the NPU OpenCL C compiler will link the OpenCL C built-in function library name `aipu--.bc`. In the assembly stage, the `.s` file is turned into a `.o` object file by assembler `aipuoas`. In the final stage, the NN-Compiler will call linker `aipuold` to link one or more `.o` files and the dependent `.a` static library file and generates the final `.out` binary file.

The final compiled `.out` binary files can run on the NPU simulator directly. For more information, see *Chapter 4 NPU NN compiler* and *Chapter 7 NPU simulator*.

3.3.2 NPU OpenCL toolchain C compiler

For high level programming, Arm China provides NPU OpenCL C language which is based on OpenCL C programming language with some extensions, and also provides an NPU OpenCL C compiler named `aipuocc`.

Like the OpenCL C programming language, NPU OpenCL C supports scalar data types and vector data types, as well as most OpenCL 2.0 built-in functions. In addition, NPU OpenCL C has the following major extensions:

- Extended address space qualifier. `__lsram` is for the TEC local SRAM.
- Extended vector data type char32 with the boolean vector data type support.
- Target specific built-in functions for low-level programming.

The NPU OpenCL C compiler supports all the Zhouyi AIPUv3 series platforms. The compiler provides the `-mcpu` option to specify the process that you want the program to run on. This compiler option is the most important option that you need to know.

The NPU OpenCL C compiler supports multi-level optimization. Arm China recommends that you use `-O0` for development and use `-O2` for a release that requires higher performance.

Note the options in the following compilation commands for `aipuocc`:

- To generate the assembly code file for Zhouyi X2-1204 with the `-S` option, use optimization level `O0`:

```
$aipuocc -target aipu -O0 -mcpu=X2_1204 -S test.cl
```

- To generate the object file for Zhouyi X2-1204 with the `-c` option, use optimization level `O2`:

```
$aipuocc -target aipu -O2 -mcpu=X2_1204 -c test.cl
```

- To generate the executable object file for the NN compiler or simulator, link with `libcommon.a`:

```
$aipuocc –target aipu -O2 -mcpu=X2_1204 test.c -Lpath_to_libcommon.a -lcommon
-o test.out
```

Different from the NPU C toolchain and the OpenCL toolchain assembler and linker, the NPU OpenCL C compiler must have the `–target aipu` option.

For more information about the NPU OpenCL C programming and NPU OpenCL C compiler, see the *Arm China Zhouyi Compass OpenCL Programming Guide*.

3.3.3 NPU OpenCL toolchain assembler

As shown in the compilation process, the NPU OpenCL toolchain assembler `aipuoas` translates the assembly language code into the objective machine code. If you are familiar with the assembly language, you can program for the NPU with the assembly language directly.

The NPU OpenCL toolchain assembly language syntax is the same as the normal assembly language syntax, except for some small differences. The NPU assembler supports instructions, directives, and user-defined macros.

The key features of `aipuoas` are:

- Zhouyi NPU unified assembly language.
- Zhouyi NPU scalar and TPC instructions.
- Zhouyi NPU fixed function accelerated instructions.
- Directives in assembly source code.
- Processing of user-defined macros.

The following shows a simple example of using `aipuoas`:

```
$aipuoas input.S -mcpu=X2_1204 -o output.o
```

The only thing that you need to know is the `-mcpu` option. This option supports all the Zhouyi AIPUv3 series platforms.

For more information about the NPU OpenCL toolchain assembly programming and the NPU OpenCL toolchain assembler, see the *Arm China Zhouyi Compass AIPUV3 Assembly Programming Guide*.

3.3.4 NPU OpenCL toolchain linker

The NPU OpenCL toolchain linker `aipuold` is used to link objective files to an executable file.

The following shows the simple usage of the NPU OpenCL toolchain linker:

- To generate an executable object file with linker `aipuld` for a single file, link with `libcommon.a`:

```
$aipuold –static test.o -Lpath_to_libcommon.a -lcommon -o test.out
```

- To generate an executable object file with linker `aipuld` for multiple files, run the following:

```
$aipuold –static test1.o test2.o -o test.out
```

Note

It is not recommended to use the linker directly.

3.3.5 NPU OpenCL toolchain debugger

Arm China also provides an OpenCL debugger named `aipuodb` for debugging NPU OpenCL applications on the NPU simulator or actual hardware. `aipuodb` allows you to set breakpoints and single-stepping, and to inspect and modify memories and variables.

- Debugging on the simulator platform enables you to debug applications without actual hardware.
- Debugging on the hardware platform requires actual extra peripherals to communicate between the client and actual hardware.

To debug an application, add the `-g` option when performing compilation with `aipuocc`. In addition, '`-O0`' is highly recommended because the higher optimization level and the bundle strategy will mess up debugging information. For example:

```
$ aipuocc -O0 -g –target aipu -mcpu=X2_1204 –c –x cl test.cl -o test.out
```

Note

For either the X2_1204 NPU or the X2_1204MP3 NPU, `mcpu` is X2_1204.

The following table describes the common debug commands. For more information about the NPU debugger, see the *Arm China Zhouyi Compass OpenCL Debugger User Guide*.

Table 3-1 Common debug commands of aipuodb

Command	Description
`platform select <platform-name>`	Create a platform and select it as the current platform.
`platform connect <connect-url>`	Select the current platform by providing a connection URL.
`target create <target-file>`	Create a target using the argument as the main application.
`settings set target.run-args <configuration-file> [core-id=Number]`	Set the run arguments with the configuration file and the core ID for multi-instance mode. The core ID is 0 by default. `core-id` is only used for hardware targets.
`aipu work-item list`	Show a summary of each work-item in the current target process.
`aipu work-item select <work-item-id>`	Change the currently selected work-item.
aipu tec list	Show a summary of each TEC in the current target process.
`aipu tec select <tec-id>`	Change the currently selected TEC.
`breakpoint set <cmd-options>`	Set a breakpoint or a set of breakpoints in the executable using the options.
`breakpoint delete <cmd-options>`	Delete the specified breakpoint(s). If no breakpoints are specified, delete them all.
`process launch`	Launch the NPU application in the debugger.
`thread step-in`	Source level single step, stepping into calls.
`thread step-over`	Source level single step, stepping over calls.
`thread continue`	Commands for operating on one or more threads in the current process.
`memory read <cmd-options> <address-expression>`	Read from the memory of the current target process.
`memory write <cmd-options> <address> <value> [<value> [...]]`	Write to the memory of the current target process.
`register read <cmd-options> [<register-name> [...]]`	Dump the contents of one or more register values from the current frame. If no register is specified, dumps all general-purpose registers.
`register write <register-name> <value>`	Modify a single register value.

Chapter 4
NPU NN compiler

This chapter describes the NPU *Neural Network* (NN) compiler.

It contains the following sections:

4.1 About the NPU NN compiler

The NPU NN compiler converts a neural network model into graph that can be run on the NPU.

The following figure shows the workflow of the NPU NN compiler.

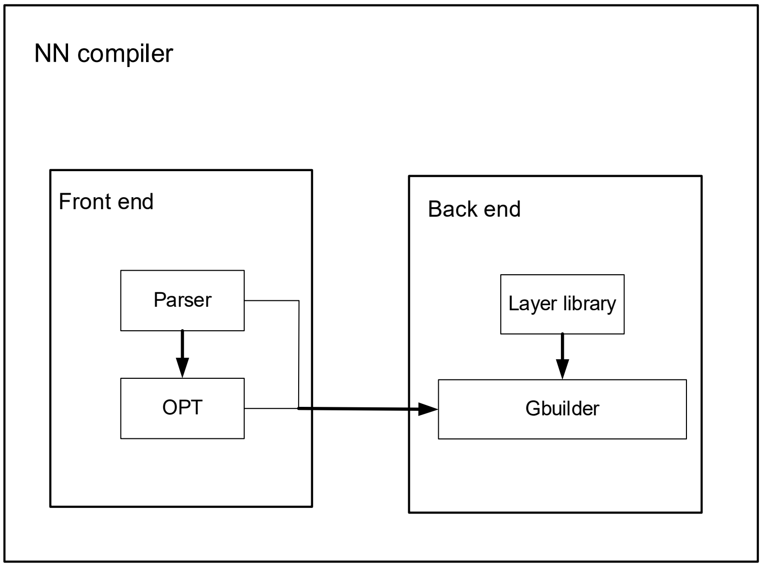


Figure 4-1 Workflow of the NN compiler

4.2 Workflows

The NN compiler is a serial tool for compiling a neural network model to an NPU executable file.

The running of the NN compiler mainly includes three steps:

1. Convert a pretrained model to an *Intermediate Representation* (IR).
   The IR can be a float IR or quantized IR (if the input model is a *Quantization Aware Training* (QAT) model. For more information, see the *Arm China Zhouyi Compass IR Definition Application Note*.
2. Convert a float IR to a quantized IR if needed.
3. Generate an executable file for the NPU with the IR.

There are the following corresponding three modules for the three steps:

- Model parse module—The model parse module (also called the Parser) will parse a third-party model and convert to an NPU internal IR.
- Quantization module—The quantization module (also called the OPT, short for Optimizer) will quantize the model into the quantized model if needed, reorganize the quantized data, and then transfer the quantized model to the generation module.
- Generation module—The generation module (also called the GBuilder) will optimize the execute path and lower the model to fit NPU instructions, and then build the model to an executable file.

In addition to these modules, there is an IR-to-IR optimization module, called GSim. The GSim module works after the parse module and quantization module to optimize the float IR and quantized IR.

For more information about the usage of the NN compiler, see the *Zhouyi Compass NN Compiler User Guide*.

Chapter 5
NPU driver

This chapter describes the driver of the Zhouyi NPU.

It contains the following section:

5.1 About the NPU driver

The Zhouyi NPU driver is responsible for parsing middleware generated by an offline NN compiler and scheduling corresponding AI acceleration tasks to the NPU accelerator. Currently, the driver can support NPU controlling on Arm Linux, bare-metal, QNX and RTOS host platforms.

The following figure shows the components of a typical NPU driver.

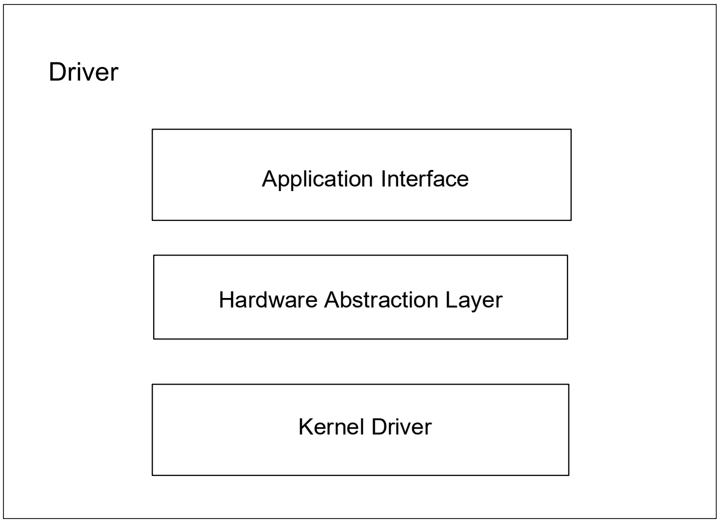


Figure 5-1 Components of a typical NPU driver

For more information about using the Zhouyi Compass driver, see Chapter 1 of the *Arm China Zhouyi Compass Driver and Runtime User Guide.*

Chapter 6
NPU runtime

This chapter describes the runtime of the Zhouyi NPU.

It contains the following section:

6.1 About the NPU runtime

The Zhouyi NPU runtime is a program that provides a runtime system for the *Neural Network* (NN). It sets up the running environment, with the handle of the NPU and maybe some other hardware, along with their drivers. In the NPU runtime, it has a hardware abstraction for the NPU and other hardware, to treat different hardware with the same interfaces as the NPU.

The NPU runtime also provides a set of application interfaces, with which engineers can build their neural network applications.

The Zhouyi Compass NPU runtime includes:

- Runtime developed based on the Arm NN interference engine.
- Runtime based on Android NNAPI.
- Runtime based on TFLite delegate.

The following figure shows the components of a typical NPU runtime.

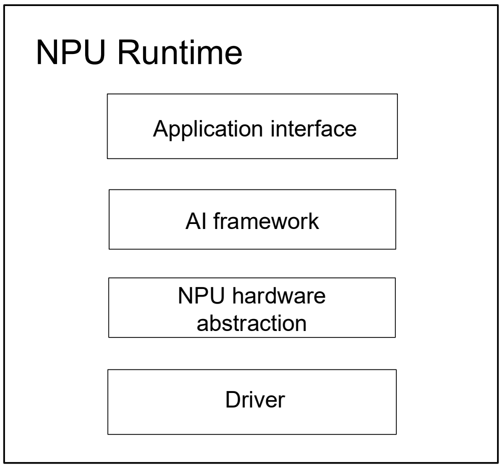


Figure 6-1 NPU runtime architecture

For more information about using the Zhouyi Compass runtime, see Chapter 2 of the *Arm China Zhouyi Compass Driver and Runtime User Guide.*

Chapter 7
NPU simulator

This chapter describes the simulator of the Zhouyi NPU.

It contains the following sections:

7.1 About the NPU simulator

The Zhouyi NPU simulator is a functional instruction set simulator. It is used to verify the correct functionality of a program written for a new target hardware before the hardware is put into use.

The Zhouyi NPU simulator monitors the execution of all the instructions of the Zhouyi NPU core, DMA device and AIFF.

Arm China provides a simulator called `aipu_simulator` (along with `libaipu_simulator_xx.so`, supports all the Zhouyi series platforms). You need to provide a configuration file (`runtime.cfg`) to run the simulator.

Before running the simulator, add the path where `libaipu_simulator_xx.so` is located into environment variable `LD_LIBRARY_PATH` (the following takes Zhouyi Z2 for example):

```
$setenv LD_LIBRARY_PATH PATH_OF_AIPU_SIMULATOR_Z2_SO:$LD_LIBRARY_PATH
```

Run the following command to start the simulator:

```
$./aipu_simulator_z2 runtime.cfg
```

The following table describes the items that need to be set in `runtime.cfg`.

Table 6-1 Items to be set in runtime.cfg (for Zhouyi Z2/Z3/X1)

Items	Description
LOG_FILE	Sets the log file name. If the name is set to `log_default`, all messages will be written to the `log_default` file, meanwhile all errors will be written to `log_default.errlog`.
CONFIG	Configuration for Zhouyi platforms, for example, Z2_1104.
INPUT_INST_CNT	Instruction bin number. If it is set to a number greater than 1, the corresponding items INPUT_INST_FILEx, INPUT_INST_BASEx and INPUT_INST_STARTPCx need to be set accordingly.
INPUT_INST_FILE0	Instruction bin 0.
INPUT_INST_BASE0	Base address of instruction bin 0.
INPUT_INST_STARTPC0	Start PC of instruction bin 0. It should be greater than or equal to the instruction base address.
INPUT_DATA_CNT	Input data number. If it is set to a number greater than 1, the corresponding items INPUT_DATA_FILEx and INPUT_DATA_BASEx need to be set accordingly.
INPUT_DATA_FILE0	Input data 0.
INPUT_DATA_BASE0	Base address of input data 0.
INPUT_DATA_FILE1	Input data 1.
INPUT_DATA_BASE1	Base address of input data 1.
OUTPUT_DATA_CNT	Output data number. If it is set to a number greater than 1, the corresponding items OUTPUT_DATA_FILEx, OUTPUT_DATA_BASEx and OUTPUT_DATA_SIZEx need to be set accordingly.
OUTPUT_DATA_FILE0	Output data 0.
OUTPUT_DATA_BASE0	Base address of output data 0.
OUTPUT_DATA_SIZE0	Size (bytes) of output data 0.
EN_PRINTF_BUF	Enables the printf buf function for the compiler.
SET_PRT_BUF_ADDR	Enables/disables the setting of the printf buf address. [0/1]
PRINTF_BUF_ADDR	Printf buf address. It is valid when SET_PRT_BUF_ADDR=1.
EN_EVAL	0: Disables profiling. 1: Enables profiling.

Table 6-2 Items to be set in runtime.cfg (for Zhouyi X2)

Group	Items	Description
COMMON	CONFIG	Configuration for Zhouyi X2 platforms, for example, X2_1204 or X2_1204MP3.
	LOG_FILEPATH	Specifies where the log output is stored.
	LOG_LEVEL	Determines the importance of messages. The levels are in the order of decreasing importance: `0` ERROR `1` WARN `2` INFO `3` DEBUG
	LOG_VERBOSE	If LOG_VERBOSE is true, then prints the log to the console, otherwise the log is not printed to the console.
	DDR_SIZE	Specifies the DDR size, for example, 64GiB. By default, it is 16GiB.
	GM_SIZE	Specifies the Global Memory size. It only supports 512KiB, 1MiB, 2MiB, 4MiB, 8MiB, 16MiB, 32MiB and 64MiB. By default, it is 4MiB for X2-1204.
INPUT	COUNT	Indicates how many files need to write to the DDR.
	FILE0	Indicates where the first input file is, for example, `./input_file0`.
	BASE0	Writes the first input file to this address.
	FILE1	Indicates where the second input file is, for example, `./input_file1`.
	BASE1	Writes the second input file to this address.
HOST	TCBP_HI	The command pool reads the high address of the TCB chain.
	TCBP_LO	The command pool reads the low address of the TCB chain.
OUTPUT	COUNT	Dump data files from the DDR.
	FILE0	The first dump data is stored to this file path.
	BASE0	Dump data address.
	SIZE0	Dump data size.
PROFILE	EN_EVAL	`0` Disables profiling. `1` Enables profiling.

7.2 Examples of runtime.cfg

For Zhouyi Z2/Z3/X1:

Note

Lines that start with # are comment lines.

```
#-----------------------------------------------------------------
# GENERAL CONFIG
#-----------------------------------------------------------------
CONFIG=Z2_1104
LOG_FILE=log_default
#-----------------------------------------------------------------
# INST CONFIG
#-----------------------------------------------------------------
INPUT_INST_CNT=1
INPUT_INST_FILE0=temp.text
INPUT_INST_BASE0=0x0
INPUT_INST_STARTPC0=0x0
#-----------------------------------------------------------------
# INPUT DATA CONFIG
#-----------------------------------------------------------------
INPUT_DATA_CNT=2
INPUT_DATA_FILE0=temp.ro
INPUT_DATA_BASE0=0x10000000
INPUT_DATA_FILE1=temp.data
INPUT_DATA_BASE1=0x20000000
#----------------------------------------------------------------
-
# OUTPUT DATA CONFIG
#-----------------------------------------------------------------
OUTPUT_DATA_CNT=1
OUTPUT_DATA_FILE0=output.bin
OUTPUT_DATA_BASE0=0x20474200
OUTPUT_DATA_SIZE0=0xc400
#-----------------------------------------------------------------
# PRINTF BUF
#-----------------------------------------------------------------
EN_PRINTF_BUF=0
SET_PRT_BUF_ADDR=0
PRINTF_BUF_ADDR=0x0
#-----------------------------------------------------------------
# PROFILE
```

```
#-----------------------------------------------------------------
EN_EVAL=0
```

For Zhouyi X2:

```
[COMMON]
CONFIG=X2_1204MP3
LOG_LEVEL=2

[INPUT]
COUNT=6
FILE0=temp.text
BASE0=0x00000000
FILE1=temp.ro
BASE1=0x10000000
FILE2=temp.input
BASE2=0x20000000
FILE3=temp.weight
BASE3=0x30000000
FILE4=temp.tcbinit
BASE4=0x40000000
FILE5=temp.tcbtask
BASE5=0x50000000

[HOST]
TCBP_HI=0
TCBP_LO=0x20

[OUTPUT]
COUNT=1
FILE0=aipu_dump.bin
BASE0=0x20000000
SIZE0=0x800

[PROFILE]
EN_EVAL=0
```

7.3 Using the aipu_simulator_profiler

The aipu_simulator_profiler is used to profile the performance data generated by the aipu_simulator.

Before running the aipu_simulator_profiler, you must run the aipu_simulator with configuration "EN_EVAL=1" in `runtime.cfg`.

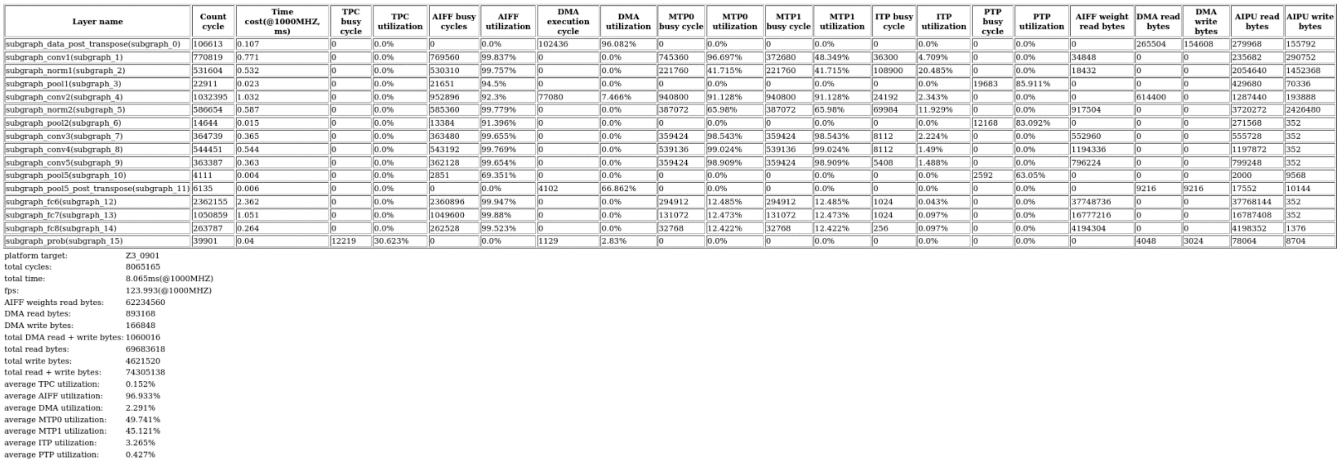
7.3.1 Command options

The following shows the command options of the aipu_simulator_profiler:

```
$./aipu_simulator_profiler -h:

  -h, --help

              show this help message and exit

  -v, --version

              show version

  -c, --case_path CASE_PATH

              specific case path

  -g GRAPH_JSON, --graph_json GRAPH_JSON

              graph.json path generated by NN-Compiler,
          default={case_path}/graph.json

  -f FREQUENCY, --frequency

              Current frequency(MHZ), default=1000(MHZ)

  --ddr_rd_delay {0, 100, 150, 200, 300}

              DDR read delay, default=0(cycles)

  --ddr_wr_delay {0, 40, 50, 100}

              DDR_write_delay, default=0(cycles)

  -o OUTPUT, --output

              Output path, default output=./sim_perf.html

  -m {html, xlsx}, --method {html, xlsx}

              The output file format, only support html or xlsx
```

7.3.2 Report format

The following figure shows an example of the profiler report, which includes the profiling data for every layer (subgraph) and the summary which indicates the total network performance.



Layer name	Count cycle	Time cost(@1000MHZ, ms)	TPC busy cycle	TPC utilization	AIFF busy cycles	AIFF utilization	DMA execution cycle	DMA utilization	MTP0 busy cycle	MTP0 utilization	MTP1 busy cycle	MTP1 utilization	ITP busy cycle	ITP utilization	PTP busy cycle	PTP utilization	AIFF weight read bytes	DMA read bytes	DMA write bytes	AIPU read bytes	AIPU write bytes
subgraph_data_post_transpose(subgraph_0)	106613	0.107	0	0.0%	0	0.0%	102436	96.082%	0	0.0%	0	0.0%	0	0.0%	0	0.0%	0	265504	154608	279968	155792
subgraph_conv1(subgraph_1)	770819	0.771	0	0.0%	769560	99.837%	0	0.0%	745360	96.697%	372680	48.349%	36300	4.709%	0	0.0%	34848	0	0	235682	290752
subgraph_norm1(subgraph_2)	531604	0.532	0	0.0%	530310	99.757%	0	0.0%	221760	41.715%	221760	41.715%	108900	20.485%	0	0.0%	18432	0	0	2054640	1452368
subgraph_pool1(subgraph_3)	22911	0.023	0	0.0%	21651	94.5%	0	0.0%	0	0.0%	0	0.0%	0	0.0%	19683	85.911%	0	0	0	429680	70336
subgraph_conv2(subgraph_4)	1032395	1.032	0	0.0%	952896	92.3%	77080	7.466%	940800	91.128%	940800	91.128%	24192	2.343%	0	0.0%	0	614400	0	1287440	193888
subgraph_norm2(subgraph_5)	586654	0.587	0	0.0%	585360	99.779%	0	0.0%	387072	65.98%	387072	65.98%	69984	11.929%	0	0.0%	917504	0	0	3720272	2426480
subgraph_pool2(subgraph_6)	14644	0.015	0	0.0%	13384	91.396%	0	0.0%	0	0.0%	0	0.0%	0	0.0%	12168	83.092%	0	0	0	271568	352
subgraph_conv3(subgraph_7)	364739	0.365	0	0.0%	363480	99.655%	0	0.0%	359424	98.543%	359424	98.543%	8112	2.224%	0	0.0%	552960	0	0	555728	352
subgraph_conv4(subgraph_8)	544451	0.544	0	0.0%	543192	99.769%	0	0.0%	539136	99.024%	539136	99.024%	8112	1.49%	0	0.0%	1194336	0	0	1197872	352
subgraph_conv5(subgraph_9)	363387	0.363	0	0.0%	362128	99.654%	0	0.0%	359424	98.909%	359424	98.909%	5408	1.488%	0	0.0%	796224	0	0	799248	352
subgraph_pool5(subgraph_10)	4111	0.004	0	0.0%	2851	69.351%	0	0.0%	0	0.0%	0	0.0%	0	0.0%	2592	63.05%	0	0	0	2000	9568
subgraph_pool5_post_transpose(subgraph_11)	6135	0.006	0	0.0%	0	0.0%	4102	66.862%	0	0.0%	0	0.0%	0	0.0%	0	0.0%	0	9216	9216	17552	10144
subgraph_fc6(subgraph_12)	2362155	2.362	0	0.0%	2360896	99.947%	0	0.0%	294912	12.485%	294912	12.485%	1024	0.043%	0	0.0%	37748736	0	0	37768144	352
subgraph_fc7(subgraph_13)	1050859	1.051	0	0.0%	1049600	99.88%	0	0.0%	131072	12.473%	131072	12.473%	1024	0.097%	0	0.0%	16777216	0	0	16787408	352
subgraph_fc8(subgraph_14)	263787	0.264	0	0.0%	262528	99.523%	0	0.0%	32768	12.422%	32768	12.422%	256	0.097%	0	0.0%	4194304	0	0	4198352	1376
subgraph_prob(subgraph_15)	39901	0.04	12219	30.623%	0	0.0%	1129	2.83%	0	0.0%	0	0.0%	0	0.0%	0	0.0%	0	4048	3024	78064	8704

platform target:	Z3_0901
total cycles:	8065165
total time:	8.065ms(@1000MHZ)
fps:	123.993(@1000MHZ)
AIFF weights read bytes:	62234560
DMA read bytes:	893168
DMA write bytes:	166848
total DMA read + write bytes:	1060016
total read bytes:	69683618
total write bytes:	4621520
total read + write bytes:	74305138
average TPC utilization:	0.152%
average AIFF utilization:	96.933%
average DMA utilization:	2.291%
average MTP0 utilization:	49.741%
average MTP1 utilization:	45.121%
average ITP utilization:	3.265%
average PTP utilization:	0.427%

Figure 6-1 Format of the profiler report

7.3.3 DTCM usage

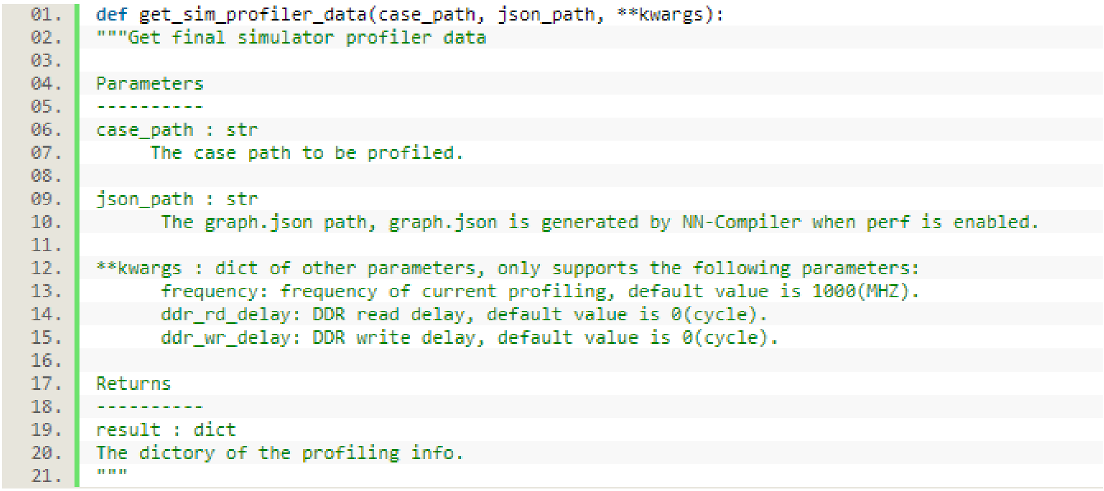
The simulator also supports DTCM case evaluation. There is no additional configuration for the simulator. Such case is generated by the NN compiler. For more information, see the DTCM usage introduction for the NN compiler.

7.3.4 Simulator profiler API

The simulator profiler now provides an API to get the performance data instead of generating an HTML report.

API overview

The following code shows an overview of the simulator profiler API.

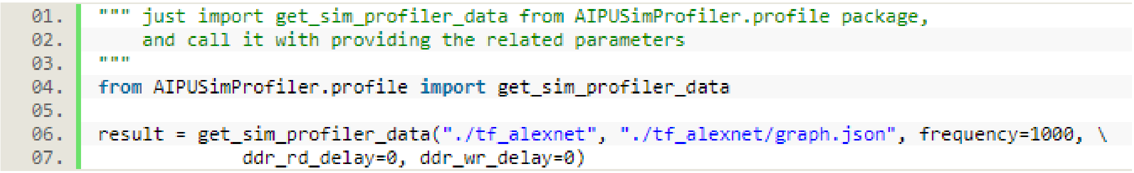


```
def get_sim_profiler_data(case_path, json_path, **kwargs):
"""Get final simulator profiler data

Parameters
----------
case_path : str
     The case path to be profiled.

json_path : str
      The graph.json path, graph.json is generated by NN-Compiler when perf is enabled.

**kwargs : dict of other parameters, only supports the following parameters:
      frequency: frequency of current profiling, default value is 1000(MHZ).
      ddr_rd_delay: DDR read delay, default value is 0(cycle).
      ddr_wr_delay: DDR write delay, default value is 0(cycle).

Returns
----------
result : dict
The dictory of the profiling info.
"""
```

Code 1. Simulator profiler API

Example usage of the API

Code 2 shows an example usage of the simulator profiler API.



```
""" just import get_sim_profiler_data from AIPUSimProfiler.profile package,
    and call it with providing the related parameters
"""
from AIPUSimProfiler.profile import get_sim_profiler_data

result = get_sim_profiler_data("./tf_alexnet", "./tf_alexnet/graph.json", frequency=1000, \
            ddr_rd_delay=0, ddr_wr_delay=0)
```

Code 2. Example usage of the API

The following section describes the return value of the API and provides a detailed example.

Profiling data arrangement

The return value of the API is a Python dictionary, which contains the performance information. Using the result of code 2 as an example, the dictionary has the following five keys:

`"target"`

> `result["target"]` is a string which shows the hardware target of the current model.

`"graph_name"`

> `result["graph_name"]` is a string which shows the model name.

`"frequency"`

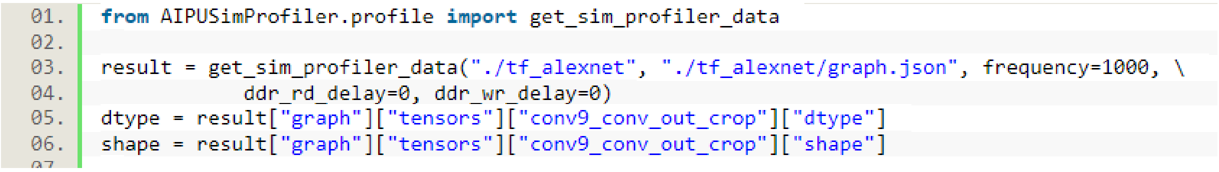
> `result["frequency"]` is an int value. Usually time (ms) is preferred instead of cycles count. This value helps to convert between time and cycle count. You can set it by passing the frequency parameter in the `get_sim_profiler_data` call as shown in the preceding example, or just use the default value (1000, which means the frequency is 1000MHz).

`"graph"`

> `result["graph"]` is a dictionary, which is organized by the topological structure of the current model. You can get node information and tensors information in this dictionary. This dictionary also has the following two keys:

- `"tensors"`

  `result["graph"]["tensors"]` is a dictionary which contains all the tensors information. The key is the tensor name, and the value is the dictionary which contains the tensor dtype and its shape. Code 3 shows how to get the dtype and shape if the tensor name is `"conv9_conv_out_crop"`.



```
from AIPUSimProfiler.profile import get_sim_profiler_data

result = get_sim_profiler_data("./tf_alexnet", "./tf_alexnet/graph.json", frequency=1000, \
            ddr_rd_delay=0, ddr_wr_delay=0)
dtype = result["graph"]["tensors"]["conv9_conv_out_crop"]["dtype"]
shape = result["graph"]["tensors"]["conv9_conv_out_crop"]["shape"]
```

Code 3. Example of getting node information

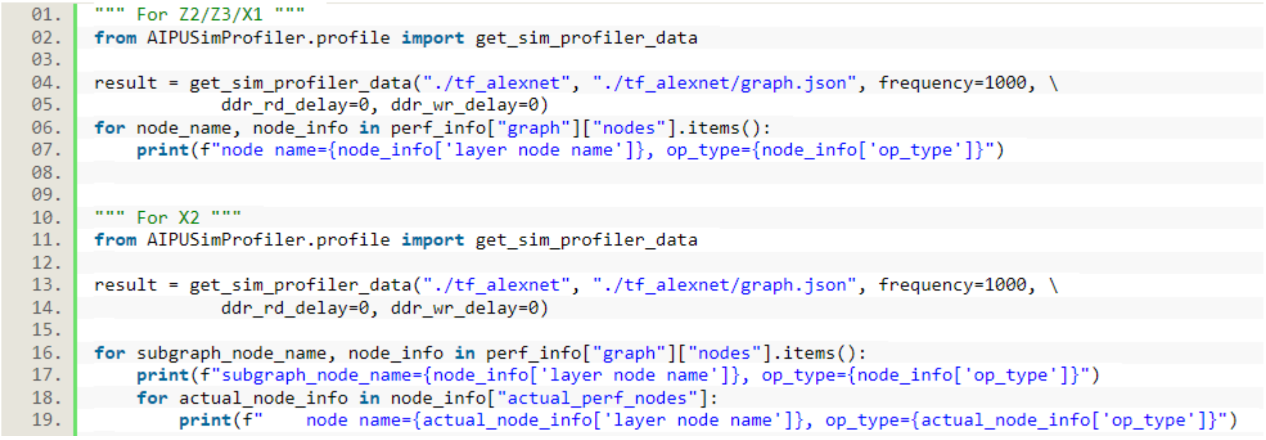
- `"nodes"`

  `result["graph"]["nodes"]` is a dictionary which contains all the nodes information (for Zhouyi X2, it is a two-level dictionary indicating nodes of each subgraph). The key is the node name, and the value is the dictionary which contains the node information collected by the NN compiler, including `"layer node name"`, `"op_type"`, `"plugin"`, `"perf_node"`, `"ops_count"`, `"operator_id"`, `"inputs"`, and `"outputs"`. If `"op_type"` is `"SubGraph"`, which means that this node is a fusion operator, `"internal_nodes"` is also provided. The following table shows the details of the node information.

Table 6-3 Node information

Item	Description
`"layer node name"`	The node name, which is the same as the key of this node.
`"op_type"`	The node operator type.
`"plugin"`	The plugin name when GBuilder selects to run this node.
`"perf_node"`	Indicates whether the node is profiled, true or false. Actually not all nodes are profiled. Some nodes such as reshape/input which do not generate any instructions to run, are not profiled.
`"ops_count"`	Specifies how many operators should be performed when running this node. This value is calculated at build time, not collected during runtime.
`"inputs"`	Input tensor name of this node.
`"outputs"`	Output tensor name of this node.
`"internal_nodes"`	A dictionary to show information on internal nodes of the fusion node.

Code 4 shows how to print the name and op_type of each node of a model.



```
""" For Z2/Z3/X1 """
from AIPUSimProfiler.profile import get_sim_profiler_data

result = get_sim_profiler_data("./tf_alexnet", "./tf_alexnet/graph.json", frequency=1000, \
            ddr_rd_delay=0, ddr_wr_delay=0)
for node_name, node_info in perf_info["graph"]["nodes"].items():
    print(f"node name={node_info['layer node name']}, op_type={node_info['op_type']}")


""" For X2 """
from AIPUSimProfiler.profile import get_sim_profiler_data

result = get_sim_profiler_data("./tf_alexnet", "./tf_alexnet/graph.json", frequency=1000, \
            ddr_rd_delay=0, ddr_wr_delay=0)

for subgraph_node_name, node_info in perf_info["graph"]["nodes"].items():
    print(f"subgraph_node_name={node_info['layer node name']}, op_type={node_info['op_type']}")
    for actual_node_info in node_info["actual_perf_nodes"]:
        print(f"    node name={actual_node_info['layer node name']}, op_type={actual_node_info['op_type']}")
```

Code 4. Printing the name and op_type of each node

`"profile_data"`

For Zhouyi Z2/Z3/X1:

`result["profile_data"]` is a list. The element in list order is the runtime order of each node, and the last element of which is the total performance data of the current model. The element in this list is a dictionary, which contains the following two keys:

- `"names"`

  A string of the current node name.

- `"runtime_information"`

  A dictionary of the performance data of the current node.

For Zhouyi X2:

`result["profile_data"]` is a list. The element in list order is the runtime order of each subgraph, and the last element of which is the total performance data of the current model. The element in this list is a dictionary, which contains the following three keys:

- `"names"`

  A string of the current subgraph name.

- `"runtime_information"`

  A dictionary of the performance data of the current node or subgraph, which contains the following information:

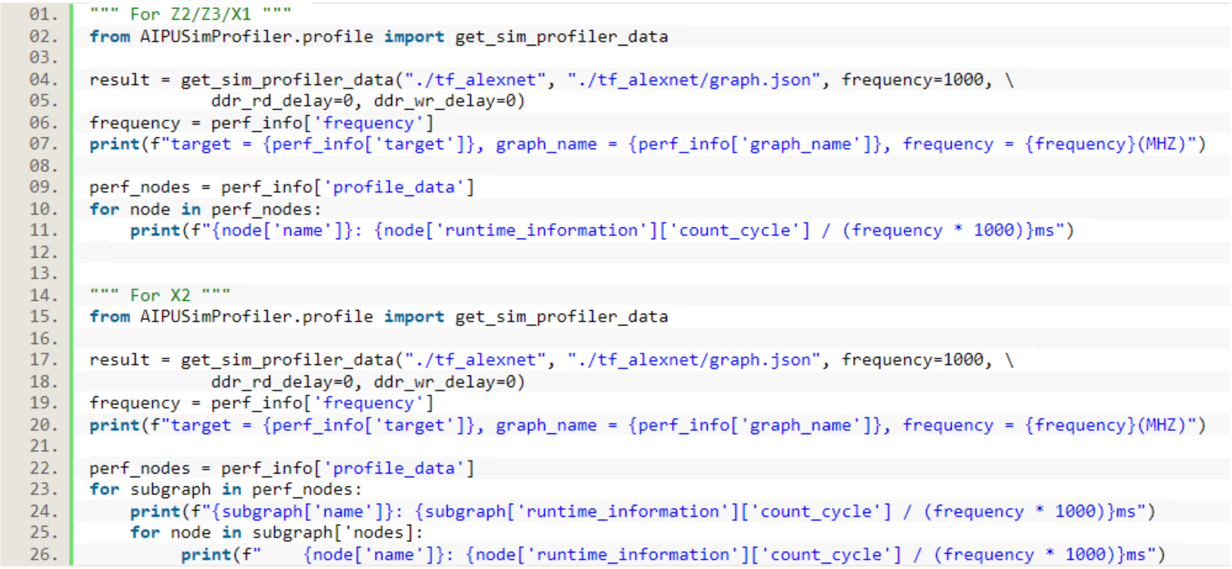
Table 6-4 Runtime information

Item	Description
"count_cycle"	Indicates how many cycles this node or subgraph costs.
"TPC_credit_cycle"	The TPC credit cycles of the node. The IFU fetches instructions and emits to the TPC. If the TPC receives and does not wait, the credit cycle will not be added. However, if the TPC is not ready and must wait, this counter will add one for each cycle. Therefore, the real TPC busy cycle is this value plus the VLIW package number which contains TPC instructions. This information is excluded in Zhouyi X2.
"AIFF_busy_cycle"	AIFF execution cycles in this node.
"DMA_busy_cycle"	DMA execution cycles in this node. AIFF internal RDMA and WDMA are not included.
"DMA_read_bytes"	Number of DMA read bytes, regardless of the direction. AIFF internal RDMA and WDMA are not included.
"DMA_write_bytes"	Number of DMA write bytes, regardless of the direction. AIFF internal RDMA and WDMA are not included.
"AIPU_read_bytes"	Number of AIPU read bytes of this node. When the AIPU (including the scalar processor, TEC processor, DMA and AIFF) accesses external DDR or external system SRAM, this value will be added. However, the value will not be added if the AIPU accesses internal local SRAM or global SRAM.
"AIPU_write_bytes"	Number of AIPU write bytes of this node. When the AIPU (including the scalar processor, TEC processor, DMA and AIFF) accesses external DDR or external system SRAM, this value will be added. However, the value will not be added if the AIPU accesses internal local SRAM/global SRAM.
"MTP0_busy_cycle"	MTP0 execution cycles in this node.
"MTP1_busy_cycle"	MTP1 execution cycles in this node.
"ITP_busy_cycle"	ITP execution cycles in this node.
"PTP_busy_cycle"	PTP execution cycles in this node.
"RDMA_WT_RD_bytes"	Number of read bytes of AIFF internal RDMA and WDMA. This information is excluded in Zhouyi X1 and X2.

- "nodes"

  A list of nodes that the current subgraph contains. The element of this list is a dictionary, which has two keys, that is, "names" and "runtime_information" of each node.

Code 5 shows an example of printing the cost time of each node of a model.



```python
""" For Z2/Z3/X1 """
from AIPUSimProfiler.profile import get_sim_profiler_data

result = get_sim_profiler_data("./tf_alexnet", "./tf_alexnet/graph.json", frequency=1000, \
            ddr_rd_delay=0, ddr_wr_delay=0)
frequency = perf_info['frequency']
print(f"target = {perf_info['target']}, graph_name = {perf_info['graph_name']}, frequency = {frequency}(MHZ)")

perf_nodes = perf_info['profile_data']
for node in perf_nodes:
    print(f"{node['name']}: {node['runtime_information']['count_cycle'] / (frequency * 1000)}ms")


""" For X2 """
from AIPUSimProfiler.profile import get_sim_profiler_data

result = get_sim_profiler_data("./tf_alexnet", "./tf_alexnet/graph.json", frequency=1000, \
            ddr_rd_delay=0, ddr_wr_delay=0)
frequency = perf_info['frequency']
print(f"target = {perf_info['target']}, graph_name = {perf_info['graph_name']}, frequency = {frequency}(MHZ)")

perf_nodes = perf_info['profile_data']
for subgraph in perf_nodes:
    print(f"{subgraph['name']}: {subgraph['runtime_information']['count_cycle'] / (frequency * 1000)}ms")
    for node in subgraph['nodes']:
        print(f"    {node['name']}: {node['runtime_information']['count_cycle'] / (frequency * 1000)}ms")
```

Code 5. Printing the cost time of each node

7.4 Simulator plugin

The simulator plugin is a way to monitor the status of various internal components in real time. It is convenient for debugging, for example, monitoring GPRs, CSRs, MMRs, memories, and even more complex heterogeneous devices such as DMA and AIFF.

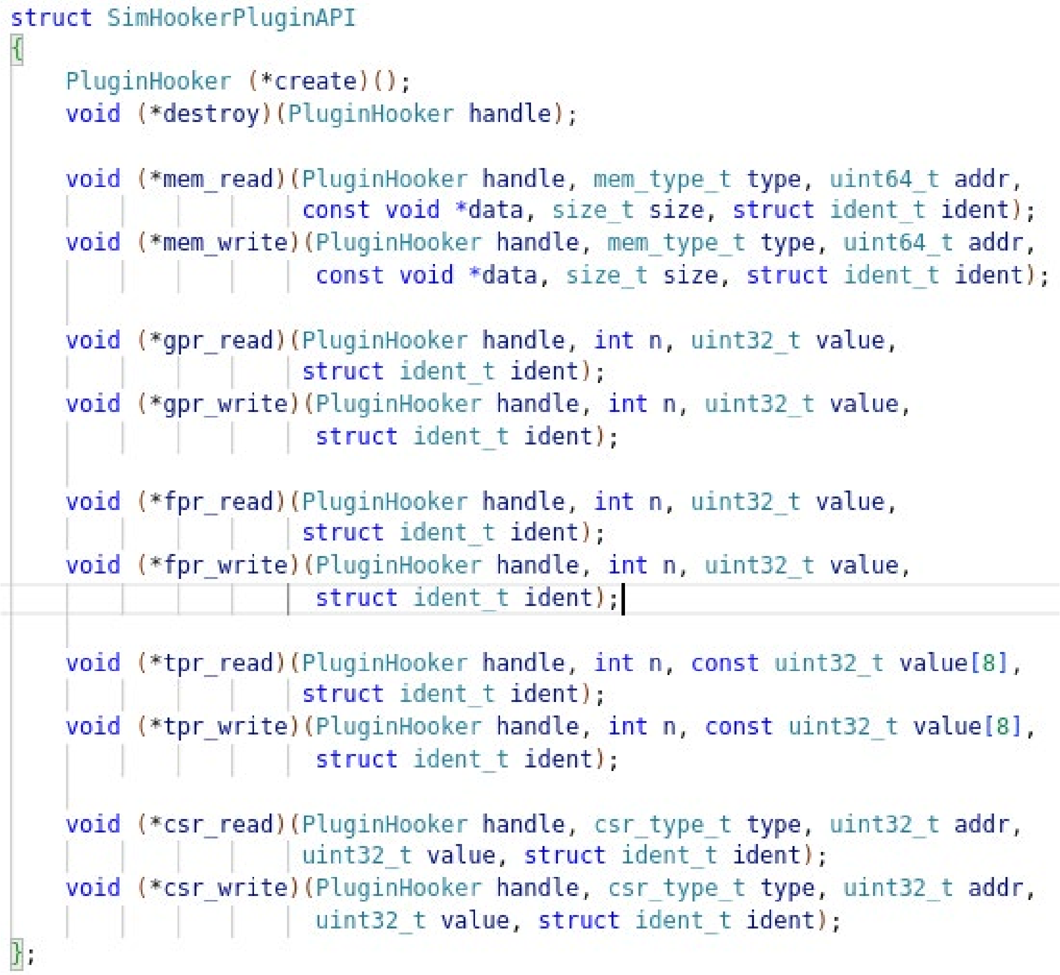
7.4.1 Interfaces

Arm China provides two sets of APIs:

- C APIs
- C++ APIs

Overview of C APIs

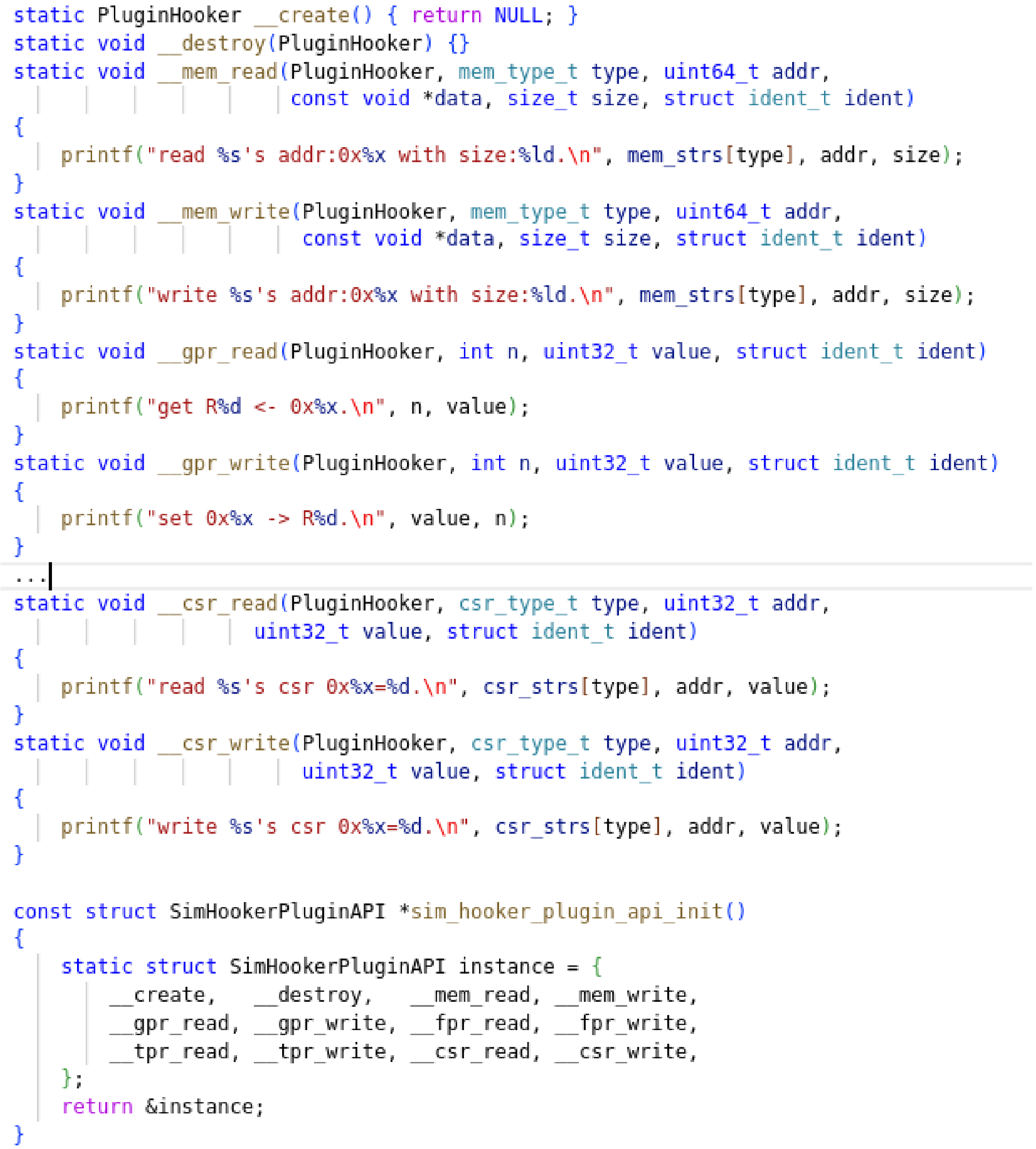
The C APIs are defined in header `<plugin_hooker_api.h>`.



```
struct SimHookerPluginAPI
{
    PluginHooker (*create)();
    void (*destroy)(PluginHooker handle);

    void (*mem_read)(PluginHooker handle, mem_type_t type, uint64_t addr,
                     const void *data, size_t size, struct ident_t ident);
    void (*mem_write)(PluginHooker handle, mem_type_t type, uint64_t addr,
                      const void *data, size_t size, struct ident_t ident);

    void (*gpr_read)(PluginHooker handle, int n, uint32_t value,
                     struct ident_t ident);
    void (*gpr_write)(PluginHooker handle, int n, uint32_t value,
                      struct ident_t ident);

    void (*fpr_read)(PluginHooker handle, int n, uint32_t value,
                     struct ident_t ident);
    void (*fpr_write)(PluginHooker handle, int n, uint32_t value,
                      struct ident_t ident);

    void (*tpr_read)(PluginHooker handle, int n, const uint32_t value[8],
                     struct ident_t ident);
    void (*tpr_write)(PluginHooker handle, int n, const uint32_t value[8],
                      struct ident_t ident);

    void (*csr_read)(PluginHooker handle, csr_type_t type, uint32_t addr,
                     uint32_t value, struct ident_t ident);
    void (*csr_write)(PluginHooker handle, csr_type_t type, uint32_t addr,
                      uint32_t value, struct ident_t ident);
};
```

C example:

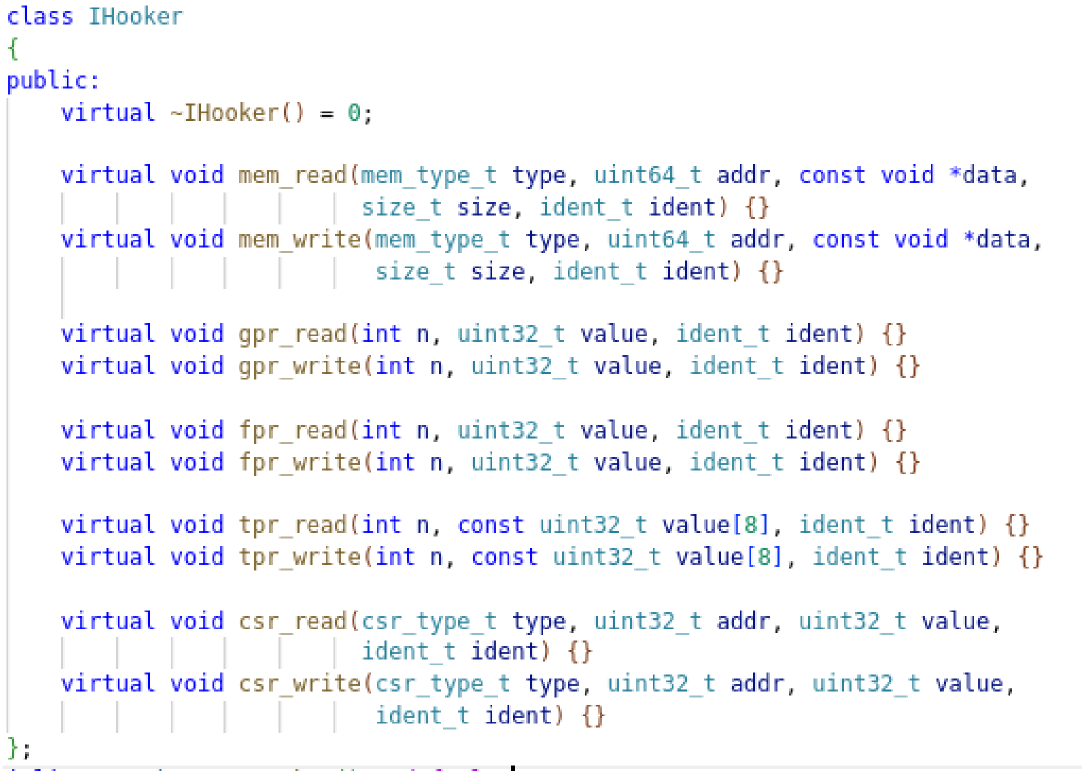
Implement all functions declared in the SimHookerPluginAPI structure and the plugin interface of sim_hooker_plugin_api_int.



```
static PluginHooker __create() { return NULL; }
static void __destroy(PluginHooker) {}
static void __mem_read(PluginHooker, mem_type_t type, uint64_t addr,
                       const void *data, size_t size, struct ident_t ident)
{
    printf("read %s's addr:0x%x with size:%ld.\n", mem_strs[type], addr, size);
}
static void __mem_write(PluginHooker, mem_type_t type, uint64_t addr,
                        const void *data, size_t size, struct ident_t ident)
{
    printf("write %s's addr:0x%x with size:%ld.\n", mem_strs[type], addr, size);
}
static void __gpr_read(PluginHooker, int n, uint32_t value, struct ident_t ident)
{
    printf("get R%d <- 0x%x.\n", n, value);
}
static void __gpr_write(PluginHooker, int n, uint32_t value, struct ident_t ident)
{
    printf("set 0x%x -> R%d.\n", value, n);
}
...
static void __csr_read(PluginHooker, csr_type_t type, uint32_t addr,
                    uint32_t value, struct ident_t ident)
{
    printf("read %s's csr 0x%x=%d.\n", csr_strs[type], addr, value);
}
static void __csr_write(PluginHooker, csr_type_t type, uint32_t addr,
                        uint32_t value, struct ident_t ident)
{
    printf("write %s's csr 0x%x=%d.\n", csr_strs[type], addr, value);
}

const struct SimHookerPluginAPI *sim_hooker_plugin_api_init()
{
    static struct SimHookerPluginAPI instance = {
        __create,   __destroy,   __mem_read, __mem_write,
        __gpr_read, __gpr_write, __fpr_read, __fpr_write,
        __tpr_read, __tpr_write, __csr_read, __csr_write,
    };
    return &instance;
}
```

Overview of C++ APIs

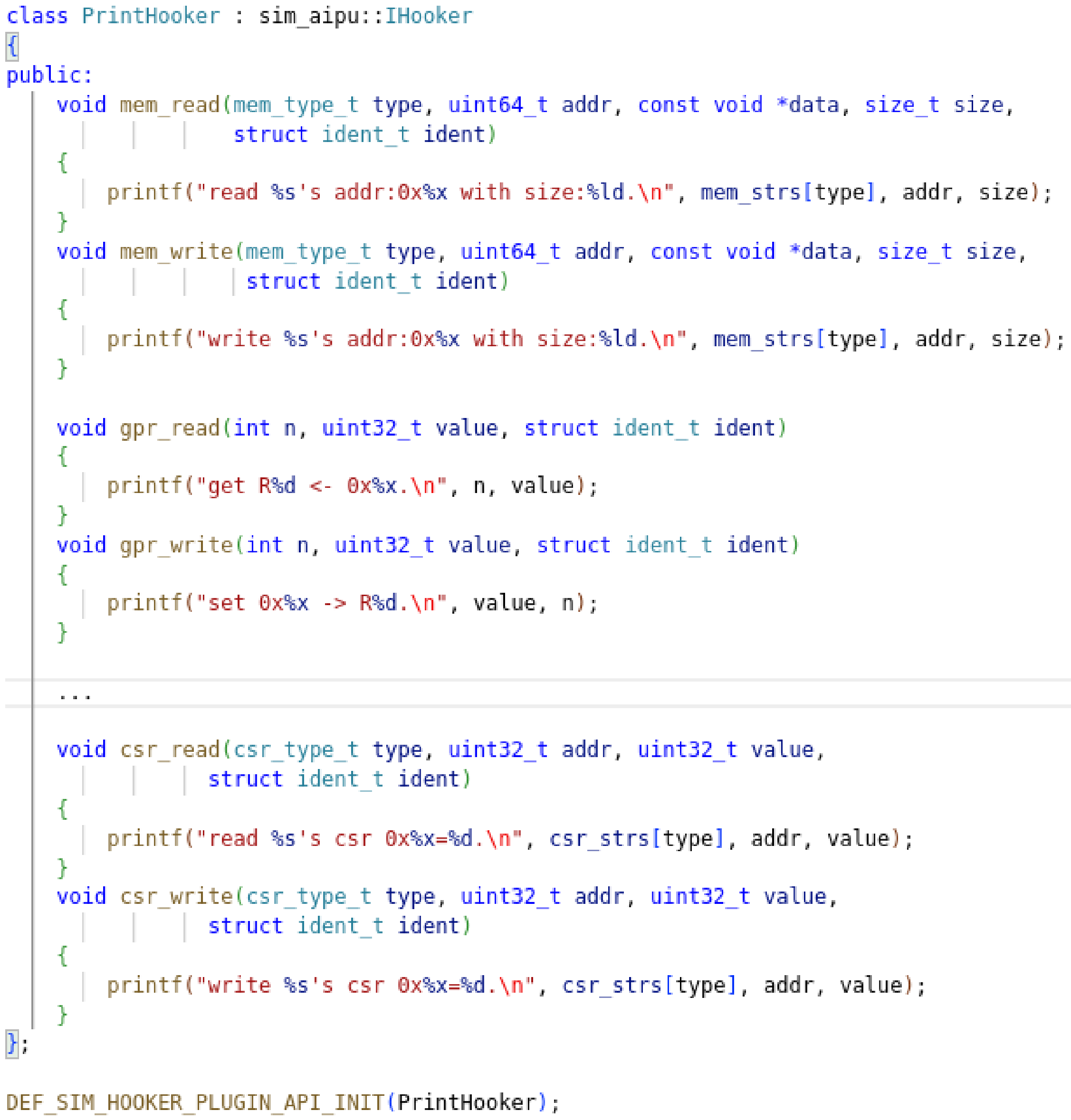
The C++ APIs are defined in header `<plugin_interface.h>`.



```
class IHooker
{
public:
    virtual ~IHooker() = 0;

    virtual void mem_read(mem_type_t type, uint64_t addr, const void *data,
                          size_t size, ident_t ident) {}
    virtual void mem_write(mem_type_t type, uint64_t addr, const void *data,
                           size_t size, ident_t ident) {}

    virtual void gpr_read(int n, uint32_t value, ident_t ident) {}
    virtual void gpr_write(int n, uint32_t value, ident_t ident) {}

    virtual void fpr_read(int n, uint32_t value, ident_t ident) {}
    virtual void fpr_write(int n, uint32_t value, ident_t ident) {}

    virtual void tpr_read(int n, const uint32_t value[8], ident_t ident) {}
    virtual void tpr_write(int n, const uint32_t value[8], ident_t ident) {}

    virtual void csr_read(csr_type_t type, uint32_t addr, uint32_t value,
                          ident_t ident) {}
    virtual void csr_write(csr_type_t type, uint32_t addr, uint32_t value,
                           ident_t ident) {}
};
```

C++ example:

Inherit the IHooker class provided by the simulator and implement the desired interface. Use the DEF_SIM_HOOKER_PLUGIN_API_INIT macro to help quickly implement the plugin interface of sim_hooker_plugin_api_init.



```
class PrintHooker : sim_aipu::IHooker
{
public:
    void mem_read(mem_type_t type, uint64_t addr, const void *data, size_t size,
                  struct ident_t ident)
    {
        printf("read %s's addr:0x%x with size:%ld.\n", mem_strs[type], addr, size);
    }
    void mem_write(mem_type_t type, uint64_t addr, const void *data, size_t size,
                   struct ident_t ident)
    {
        printf("write %s's addr:0x%x with size:%ld.\n", mem_strs[type], addr, size);
    }

    void gpr_read(int n, uint32_t value, struct ident_t ident)
    {
        printf("get R%d <- 0x%x.\n", n, value);
    }
    void gpr_write(int n, uint32_t value, struct ident_t ident)
    {
        printf("set 0x%x -> R%d.\n", value, n);
    }

    ...

    void csr_read(csr_type_t type, uint32_t addr, uint32_t value,
                struct ident_t ident)
    {
        printf("read %s's csr 0x%x=%d.\n", csr_strs[type], addr, value);
    }
    void csr_write(csr_type_t type, uint32_t addr, uint32_t value,
                struct ident_t ident)
    {
        printf("write %s's csr 0x%x=%d.\n", csr_strs[type], addr, value);
    }
};

DEF_SIM_HOOKER_PLUGIN_API_INIT(PrintHooker);
```

7.4.2 Using the simulator plugin

1. Compile your program as a dynamic linking library.

   ```
   $gcc -fPIC -shared -c srcs.c -o your_plugin.so
   ```

1. Add `PLUGIN_FILENAME=your_plugin.so` into the `runtime.cfg` file.

   ```
   $vim runtime.cfg
   …
   [COMMON] #z2, z3, x1 does not have this section label
   PLUGIN_FILENAME=your_plugin.so
   …
   ```

2. Run the simulator.

   ```
   $./aipu_simulator_x2 runtime.cfg
   ```

Chapter 8
Apache TVM

This chapter describes the Zhouyi Compass Apache TVM.

It contains the following section:

8.1 About the Apache TVM

The Apache TVM is an open-source machine learning compiler framework for CPUs, GPUs, and accelerators. It aims to enable machine learning engineers to optimize and run computations efficiently on any hardware backend.

The Zhouyi Compass is integrated with the Apache TVM for *Neural Network* (NN) model quick support and heterogeneous execution.

Currently, the Apache TVM only supports Zhouyi Z2, Zhouyi Z3, Zhouyi X1 and Zhouyi X2.

The Apache TVM parser supports extensive *Machine Learning* (ML) frameworks, including TensorFlow, PyTorch, ONNX, Keras, TensorFlow Lite, TensorFlow 2, Caffe, MxNet, PaddlePaddle, and Darknet. Through the Zhouyi Compass integration with the Apache TVM, your NN model can be supported quickly even though the NN compiler of the Zhouyi Compass does not support the ML framework of the NN model yet.

The Apache TVM provides the solution for graph partition and heterogeneous execution, through the Zhouyi Compass integration with the Apache TVM. The NN operators supported by Zhouyi NPU are split to Zhouyi NPU sub graph automatically, and you can continue to place the remaining NN operators to other devices (for example, CPU and GPU). After building the Apache TVM, the runtime will execute the NN model heterogeneously and automatically. So, your NN model can be supported even though some of its NN operators are not supported by the Zhouyi Compass.

For more information on using the Zhouyi Compass Apache TVM, see the *Arm China Zhouyi Compass Apache TVM User Guide*.

Chapter 9
CompassStudio

This chapter describes the Zhouyi NPU integrated development platform.

It contains the following section:

9.1 About the CompassStudio

Arm China Zhouyi CompassStudio is a development platform for Zhouyi NPU SDK and Toolchain integration. The CompassStudio is an easy-to-use tool with an intuitive *Graphical User Interface* (GUI) that enables you to program the Zhouyi NPU quickly, conveniently, and safely.

The CompassStudio has the following basic and advanced features and components.

Basic features and components

- Project management
- NN Model Configuration Visual Editor
- NN Compiler
- NN Model Run on Simulator and Hardware
- Profiler
- QuantTuning Visualizer
- CompassIR Visualizer
- NpyFile Visualizer
- Log management
- Device management
- Compass C/OpenCL Compiler
- Compass C/OpenCL Debugger
- Operator Deployment

Advanced components

- CompassIR Visual Editor
- QuantTuning Visualizer

The following figure shows the architecture of the CompassStudio.

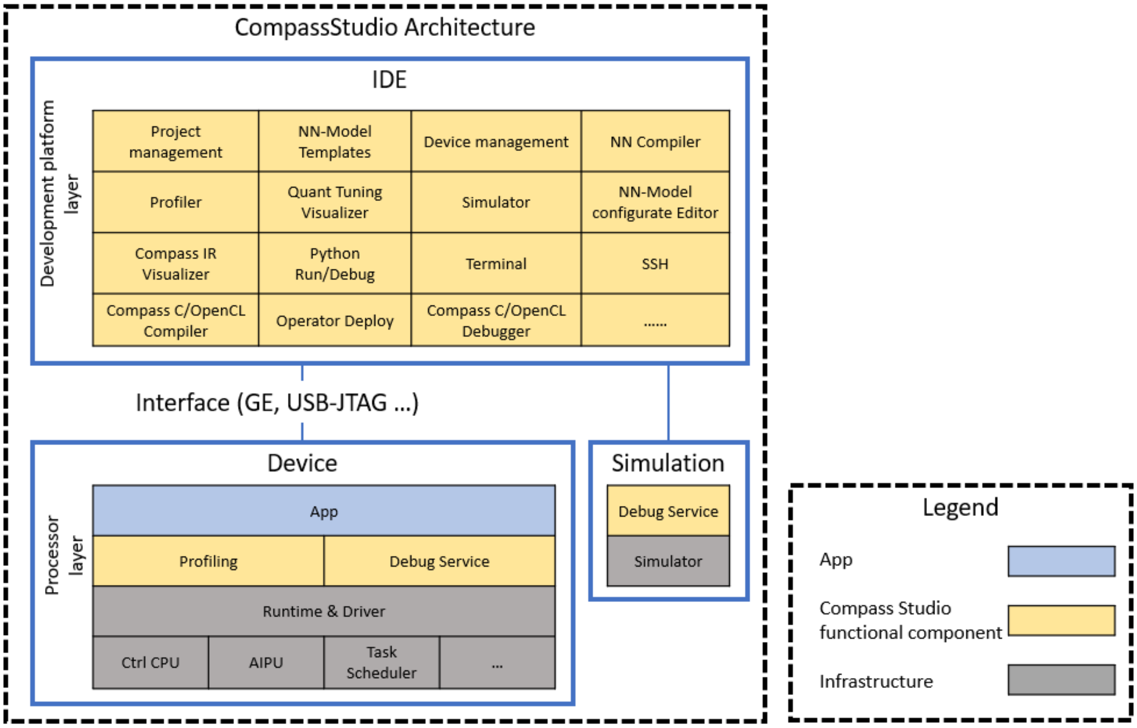


Figure 8-1 Architecture of the CompassStudio

For more information on using CompassStudio, see the *Arm China Zhouyi CompassStudio User Guide*.

Appendix A
NPU general-purpose registers summary

This appendix provides a summary of the general-purpose registers of the Zhouyi NPUs.

It contains the following sections:

A.1 Zhouyi Z2 AIPU general-purpose registers summary

The following table lists all the general-purpose registers of the Zhouyi Z2 AIPU.

Table A-1 General-purpose registers

Name	Description
R31	Constant zero. Can be accessed as a source or destination register.
R0-R30	31 32-bit general-purpose registers. • All can be accessed by scalar instructions with bit fields Rd, Rn, and Rm. • R0-R6 can be accessed by scalar instructions with the bit field Rc. • R30 is implicit as Ra for sub routine calling instructions BL and BRL. • R29 is implicit as SP for stack push and pop instruction. • R0-R31 can be accessed by vector instructions as source registers with the bit field Rn. • R0-R31 can be accessed by vector instructions as destination registers with the bit field Rd.
PC	Program counter. An implicit register. It can be accessed by GPC instructions.
Ra	Return address. It is an alias of GPR R30.
SP	Stack pointer. It is an alias of GPR R29. It will decrease by 4 when pushing a word into stack, and increase by 4 when popping a word from stack.
Rc0-Rc6	Condition registers. The condition registers are aliases of the LSB of GPR R0-R6.
Rc7	Constant true.
T0-T31	32 256-bit tensor registers per TEC. All can be accessed by vector instructions with bit fields Tn, Tm, Td, and Tdn.
P0-P7	8 32-bit predication governing registers per TEC. • All can be accessed by vector instructions with bit fields Pg, Pn, Pm, Pd, and Pdn. • All can be accessed by scalar instructions with the bit field Pd.
ACC	4 256-bit accumulation registers per SIMD. Can be accessed by tensor MOV or arithmetic instructions with bit fields ACC, ACCn, and ACCd.

AIPU architectural system register summary

This section identifies the architectural system registers implemented in the AIPU core.

Table A-2 AIPU Control Register Group 0

Address	Name	Reset value	Description
0x1E0	ISA version	0x00000001	ISA Version Register
0x1E1	TPC Feature	Z2-1104: 0x00000004 Z2-1002: 0x00000002 Z2-0901: 0x00000001	TPC Feature Register
0x1E2	SPU Feature	0x00000000	SPU Feature Register
0x1E3	AIFF Feature	Z2-1104: 0x00030103 Z2-1002: 0x00030002 Z2-0901: 0x00000001	AIFF Feature Register
0x1E4	Revision ID	0x00000100	Revision ID Register
0x1E5	Memory Architecture Feature	Z2-1104: 0x00000370 Z2-1002: 0x00000360 Z2-0901: 0x00000160	Memory Architecture Feature Register
0x1E6	Instruction RAM Feature	Z2-1104: 0x00000001 Z2-1002: 0x00000000 Z2-0901: 0x00000000	Instruction RAM Feature Register
0x1E7	TEC Local SRAM Feature	0x00000312	TEC Local SRAM Feature Register
0x1E8	Global SRAM Feature	Z2-1104: 0x00000115 Z2-1002: 0x00000115 Z2-0901: 0x00000114	Global SRAM Feature Register
0x1E9	Instruction Cache Feature	0x00000234	Instruction Cache Feature Register
0x1EA	Data Cache Feature	Z2-1104: 0x000F0134 Z2-1002: 0x000F0134 Z2-0901: 0x000F0030	Data Cache Feature Register
0x007	AIPU Fault Status	0x00000000	AIPU Fault Status Register
0x008	AIPU Debug	-	AIPU Debug Register
0x020	TPC Control Enable	0x00000000	TPC control Enable Register
0x021	TPC Control Status	0x00000000	TPC Control Status Register
0x022	TPC Fault/Exception Status	0x00000000	TPC Fault/Exception Status Register
0x040	Interrupt Mask	0x80000000	Interrupt Mask Register
0x041	Interrupt Cause	0x00000000	Interrupt Cause Register
0x042	Interrupt Status	0x00000000	Interrupt Status Register
0x043	Interrupt Priority	0x00000000	Interrupt Priority Register
0x044	Interrupt Back-up Mask	0x00000000	Interrupt Back-up Mask Register
0x045	Interrupt Back-up PC	0x00000000	Interrupt Back-up PC Register

Address	Name	Reset value	Description
0x046	Interrupt Back-up Status	0x00000000	Interrupt Back-up Status Register
0x050	Cache Control	Z2-1104: 0x00000007 Z2-1002: 0x00000007 Z2-0901: 0x00000003	Cache Control Register
0x051	IRAM Configuration	0x00000000	IRAM Configuration Register
0x060	Performance Counter 0 Control	0x00000000	Performance Counter 0 Control Register
0x061	Performance Counter 1 Control	0x00000000	Performance Counter 1 Control Register
0x062	Performance Counter 2 Control	0x00000000	Performance Counter 2 Control Register
0x063	Performance Counter 3 Control	0x00000000	Performance Counter 3 Control Register
0x064	Performance Counter 0 Low 32-bit	-	Performance Counter 0 Control Low 32-bit Register
0x065	Performance Counter 0 High 32-bit	-	Performance Counter 0 Control High 32-bit Register
0x066	Performance Counter 1 Low 32-bit	-	Performance Counter 1 Control Low 32-bit Register
0x067	Performance Counter 1 High 32-bit	-	Performance Counter 1 Control High 32-bit Register
0x068	Performance Counter 2 Low 32-bit	-	Performance Counter 2 Control Low 32-bit Register
0x069	Performance Counter 2 High 32-bit	-	Performance Counter 2 Control High 32-bit Register
0x06A	Performance Counter 3 Low 32-bit	-	Performance Counter 3 Control Low 32-bit Register
0x06B	Performance Counter 3 High 32-bit	-	Performance Counter 3 Control High 32-bit Register

Table A-3 AIPU Control Register Group 1

Address	Name	Reset value	Description
0x000	TEC0_A0	0xF0000000	Fixed address pointer to point to the start of LSRAM 0 for TEC 0.
0x001	TEC0_A1	0xF0080000	Fixed address pointer to point to the start of LSRAM 1 for TEC 0.
0x002	TEC0_A2	0xF0000000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 0.
0x003	TEC0_A3	0xF0080000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 0.
0x004	TEC0_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 0, shared by all TECs.
0x005	TEC0_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 0, shared by all TECs.
0x006	TEC0_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 0.
0x007	TEC0_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 0.
0x010	TEC0_MFSR	0x00000000	Memory Fault Status Register for TEC0.
0x011	TEC0_MFFCR	0x00000000	Memory First-Fault Control Register for TEC0.
0x020	TEC1_A0	0xF0100000	Fixed address pointer to point to the start of LSRAM 0 for TEC 1. Reserved in Z2-0901.
0x021	TEC1_A1	0xF0180000	Fixed address pointer to point to the start of LSRAM 1 for TEC 1. Reserved in Z2-0901.
0x022	TEC1_A2	0xF0100000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 1. Reserved in Z2-0901.

Address	Name	Reset value	Description
0x023	TEC1_A3	0xF0180000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 1. Reserved in Z2-0901.
0x024	TEC1_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 1, shared by all TECs. Reserved in Z2-0901.
0x025	TEC1_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 1, shared by all TECs. Reserved in Z2-0901.
0x026	TEC1_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 1. Reserved in Z2-0901.
0x027	TEC1_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 1. Reserved in Z2-0901.
0x030	TEC1_MFSR	0x00000000	Memory Fault Status Register for TEC1. Reserved in Z2-0901.
0x031	TEC1_MFFCR	0x00000000	Memory First-Fault Control Register for TEC1. Reserved in Z2-0901.
0x040	TEC2_A0	0xF0200000	Fixed address pointer to point to the start of LSRAM 0 for TEC 2. Reserved in Z2-0901 and Z2-1002.
0x041	TEC2_A1	0xF0280000	Fixed address pointer to point to the start of LSRAM 1 for TEC 2. Reserved in Z2-0901 and Z2-1002.
0x042	TEC2_A2	0xF0200000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 2. Reserved in Z2-0901 and Z2-1002.
0x043	TEC2_A3	0xF0280000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 2. Reserved in Z2-0901 and Z2-1002.
0x044	TEC2_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 2, shared by all TECs. Reserved in Z2-0901 and Z2-1002.
0x045	TEC2_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 2, shared by all TECs. Reserved in Z2-0901 and Z2-1002.
0x046	TEC2_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 2. Reserved in Z2-0901 and Z2-1002.
0x047	TEC2_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 2. Reserved in Z2-0901 and Z2-1002.
0x050	TEC2_MFSR	0x00000000	Memory Fault Status Register for TEC2. Reserved in Z2-0901 and Z2-1002.
0x051	TEC2_MFFCR	0x00000000	Memory First-Fault Control Register for TEC2. Reserved in Z2-0901 and Z2-1002.
0x060	TEC3_A0	0xF0300000	Fixed address pointer to point to the start of LSRAM 0 for TEC 3. Reserved in Z2-0901 and Z2-1002.
0x061	TEC3_A1	0xF0380000	Fixed address pointer to point to the start of LSRAM 1 for TEC 3. Reserved in Z2-0901 and Z2-1002.
0x062	TEC3_A2	0xF0300000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 3. Reserved in Z2-0901 and Z2-1002.
0x063	TEC3_A3	0xF0380000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 3. Reserved in Z2-0901 and Z2-1002.
0x064	TEC3_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 3, Reserved in Z2-0901 and Z2-1002.shared by all TECs.
0x065	TEC3_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 3, Reserved in Z2-0901 and Z2-1002.shared by all TECs.
0x066	TEC3_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 3. Reserved in Z2-0901 and Z2-1002.

Address	Name	Reset value	Description
0x067	TEC3_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 3. Reserved in Z2-0901 and Z2-1002.
0x070	TEC3_MFSR	0x00000000	Memory Fault Status Register for TEC3. Reserved in Z2-0901 and Z2-1002.
0x071	TEC3_MFFCR	0x00000000	Memory First-Fault Control Register for TEC3. Reserved in Z2-0901 and Z2-1002.

Table A-4 AIPU control register group 2

Address	Name	Reset value	Description
0x000	AIFF_CTRL	0x00000000	AIFF Configuration Control Register
0x001	AIFF_DESP_ADDR	0x00000000	AIFF Descriptor Address Register
0x002	AIFF_DESP_LENGTH	0x00000000	AIFF Descriptor Length Register
0x003	AIFF_STATUS	0x00000000	AIFF Status Register
0x004	AIFF_INTR_CTRL	0x00000000	AIFF Interrupt Control Register
0x005	AIFF_SYNC_CTRL	0x00000000	AIFF Descriptor Synchronization Control Register
0x006	AIFF_SYNC_KEY	0x00000000	AIFF Synchronization Key Register
0x007	AIFF_SYNC_BAD_KEY	0x00000000	AIFF Synchronization BAD Key Register
0x010	AIFF_UTIL_CNT_CTRL	0x00000000	AIFF Utilization Counter Control
0x011	MTP0_PE_A_UTIL_CNT	-	MTP0 PE Array Utilization Counter
0x012	MTP1_PE_A_UTIL_CNT	-	MTP1 PE Array Utilization Counter
0x013	ITP_PIPE_UTIL_CNT	-	ITP Pipeline Utilization Counter
0x014	PTP_PIPE_UTIL_CNT	-	PTP Pipeline Utilization Counter
0x015	WRB_UTIL_CNT	-	WRB Utilization Counter
0x020	UNB_MTP0_BASE_ADDR	0x00000000	MTP0 Base Address in Unified Buffer Register
0x021	UNB_MTP1_BASE_ADDR	0x00000000	MTP1 Base Address in Unified Buffer Register
0x022	UNB_ITP_BASE_ADDR	0x00000000	ITP Base Address in Unified Buffer Register
0x023	UNB_PTP_BASE_ADDR	0x00000000	PTP Base Address in Unified Buffer Register
0x030	WRB_MODE CTRL	0x30000003	WRB Mode Control Register
0x031	WRB_Region0_OACT_CTRL	0x00000000	WRB Region 0 Output Activation Control Register
0x032	WRB_Region0_CBLI_CTRL	0x00000000	WRB Region 0 Output Activation Compression Block length Info Register
0x033	WRB_Region0_CTAG_CTRL	0x00000000	WRB Region 0 Output Activation Compression Tag Register
0x034	WRB_Region0_OACT_L_STRIDE	0x00000000	WRB Region 0 Output Activation Line Stride Register
0x035	WRB_Region0_OACT_S_STRIDE	0x00000000	WRB Region 0 Output activation Surface Stride Register
0x036	WRB_Region0_INT_LS_STRIDE	0x00000000	WRB Region 0 Internal Buffer Line/Surface Stride Register
0x037	WRB_Region1_OACT_CTRL	0x00000000	WRB Region 1 Output Activation Control Register
0x038	WRB_Region1_CBLI_CTRL	0x00000000	WRB Region 1 Output Activation Compression Block length Info Register
0x039	WRB_Region1_CTAG_CTRL	0x00000000	WRB Region 1 Output Activation Compression Tag Register

Address	Name	Reset value	Description
0x03A	WRB_Region1_OACT_L_STRIDE	0x00000000	WRB Region 1 Output Activation Line Stride Register
0x03B	WRB_Region1_OACT_S_STRIDE	0x00000000	WRB Region 1 Output activation Surface Stride Register
0x03C	WRB_Region1_INT_LS_STRIDE	0x00000000	WRB Region 1 Internal Buffer Line/Surface Stride Register
0x040	AIFF_MMU_CTRL	0x00000000	AIFF MMU Control Register
0x041	AIFF_SEG_CTRL	0x00000000	AIFF Segment Control Register
0x042	AIFF_SEGMMU_STAT	0x00000000	AIFF MMU Status Register
0x048	AIFF_SEG0_CTRL0	0x00000000	AIFF MMU Segment 0 Control 0 Register
0x049	AIFF_SEG0_CTRL1	0x00000000	AIFF MMU Segment 0 Control 1 Register
0x04A	AIFF_SEG1_CTRL0	0x00000000	AIFF MMU Segment 1 Control 0 Register
0x04B	AIFF_SEG1_CTRL1	0x00000000	AIFF MMU Segment 1 Control 1 Register
0x04C	AIFF_SEG2_CTRL0	0x00000000	AIFF MMU Segment 2 Control 0 Register
0x04D	AIFF_SEG2_CTRL1	0x00000000	AIFF MMU Segment 2 Control 1 Register
0x04E	AIFF_SEG3_CTRL0	0x00000000	AIFF MMU Segment 3 Control 0 Register
0x04F	AIFF_SEG3_CTRL1	0x00000000	AIFF MMU Segment 3 Control 1 Register
0x080	MTP_Twin_CTRL	0x00000000	MTP Twin Control register
0x088	MTP_INDEX_CTRL	0x00000000	MTP Index Control Register
0x090	MTP_CTRL	0x00000000	MTP Mode Control register
0x091	MTP_BACK_END_CTRL	0x00000000	MTP Back End Control register
0x092	MTP_UnB_CTRL	0x0000000C	MTP UnB Control register
0x093	MTP_KERNEL_CTRL	0x00000000	MTP Kernel Control Register
0x094	MTP_WEIGHT_ADDR	0x00000000	MTP Weight Address Register
0x095	MTP_WEIGHT_SPARSE	0x00000000	MTP Weight Sparse Register
0x096	MTP_WEIGHT_SIZE	0x00000000	MTP Weight Size Register
0x097	MTP_W_STEP	0x00000000	MTP Width Step Register
0x098	MTP_H_STEP	0x00000000	MTP Height Step Register
0x0A0	MTP_IACT_CTRL	0x00000000	Input Activation Control Register
0x0A1	MTP_IACT_SPARSE _R0	0x00000000	Input Activation Sparse Information Register0
0x0A2	MTP_IACT_SPARSE _R1	0x00000000	Input Activation Sparse Information Register1
0x0A3	MTP_PAD_CTRL	0x00000000	MTP padding Control Register
0x0A4	MTP_PAD_ADDR	0x00000000	MTP padding Address Register
0x0A5	MTP_IACT_W_STRIDE	0x00000000	Input Activation Width Stride Register
0x0A6	MTP_IACT_S_STRIDE	0x00000000	Input activation Surface Stride Register
0x0A7	MTP_ACT_C_CTRL	0x00000000	Activation Channel Axis Control Register
0x0A8	MTP_ACT_W_CTRL	0x00000000	Activation Width Axis Control Register
0x0A9	MTP_ACT_ H_CTRL	0x00000000	Activation Height Axis Control Register
0x100	ITP_MODE_CCFG	0x00000000	ITP WORK MODE Configuration Register
0x101	ITP_UNB_ADDR_MCFG	0x00000000	ITP UNB Address Configuration Register

Address	Name	Reset value	Description
0x102	ITP_LUT_MCFG	0x00000000	ITP LUT Base Address Configuration Register
0x108	ITP_INDEX_CCFG	0x00000000	ITP INDEX Configuration Register
0x109	ITP_LUT_DCFG0	-	ITP LUT Data Configuration Register 0. The register will not be updated by descriptor
0x10A	ITP_LUT_DCFG1	0x00000000	ITP LUT Data Configuration Register 1. The register will not be updated by descriptor
0x110	ITP_ACT_CCFG0	0x00000000	ITP ACT Configuration Register 0
0x111	ITP_ACT_CCFG1	0x00000000	ITP ACT Configuration Register 1
0x112	ITP_ACT_STEP_CCFG	0x00000000	ITP ACT STEP Configuration Register
0x113	ITP_M0_CCFG	0x00000000	ITP M0 Execution Pipe Configuration Register
0x114	ITP_M0_ALU_MCFG	0x00000000	ITP M0 ALU Parameter Base Address Register
0x115	ITP_M0_MUL_MCFG	0x00000000	ITP M0 MUL Parameter Base Address Register
0x116	ITP_M0_PCFG	0x00000000	ITP M0 Per Layer Parameter Value Register
0x117	ITP_N_M1_CCFG	0x00000000	ITP M1 Execution Pipe Configuration Register
0x118	ITP_N_M1_ALU_MCFG	0x00000000	ITP M1 ALU Parameter Base Address Register
0x119	ITP_N_M1_MUL_MCFG	0x00000000	ITP M1 MUL Parameter Base Address Register
0x11A	ITP_N_M1_PCFG	0x00000000	ITP M1 Per Layer Parameter Value Register
0x11B	ITP_E_CCFG	0x00000000	ITP E Execution Pipe Configuration Register
0x11C	ITP_E_MUL_MCFG	0x00000000	ITP E MUL Parameter Base Address Register
0x11D	ITP_E_ALU_MCFG	0x00000000	ITP E ALU Parameter Base Address Register
0x11E	ITP_EMUL_SURF_STRIDE	0x00000000	E MUL PARAMETER Surface Stride Register
0x11F	ITP_EALU_SURF_STRIDE	0x00000000	E ALU PARAMETER Surface Stride Register
0x120	ITP_OCVT_SUB_CFG	0x00000000	ITP Output Data Format Conversion Subtract Configuration Register
0x121	ITP_OCVT_MUL_CFG	0x00000000	ITP Output Data Format Conversion Multiply Configuration Register
0x122	ITP_OCVT_CFG	0x00000000	ITP Output Data Format Conversion Truncate Configuration Register
0x123	ITP_E_MUL_PCFG	0x00000000	ITP E MUL Per Layer Parameter Value Register
0x124	ITP_E_ALU_PCFG	0x00000000	ITP E ALU Per Layer Parameter Value Register
0x125	ITP_E_ALU_CLAMP_PCFG0	0x00000000	ITP E ALU Clamp High Value Register
0x126	ITP_E_ALU_CLAMP_PCFG1	0x00000000	ITP E ALU Clamp Low Value Register
0x127	ITP_E_MUL_PCVT_CCFG	0x00000000	ITP E MUL Parameter Data Format Conversion Configuration Register 0
0x128	ITP_E_MUL_PCVT_PCFG	0x00000000	ITP E MUL Parameter Format Conversion Configuration Register 1
0x129	ITP_E_ALU_PCVT_CCFG	0x00000000	ITP E ALU Parameter Data Format Conversion Configuration Register 0
0x12A	ITP_E_ALU_PCVT_PCFG	0x00000000	TP E ALU Parameter Format Conversion Configuration Register 1

Address	Name	Reset value	Description
0x12B	ITP_LUT_PCFG0	0x00000000	ITP LUT Pre Processing Configuration Register 0
0x12C	ITP_LUT_PCFG1	0x00000000	ITP LUT Pre Processing Configuration Register 1
0x12D	ITP_LUT_OCFG	0x00000000	ITP LUT Output Configuration Register
0x180	PTP_MODE	0x00000000	PTP Mode Control Register
0x181	PTP_KERNEL	0x00000000	PTP Kernel Control Register
0x182	PTP_PAD	0x00000000	PTP Padding Register
0x183	PTP_BIAS_CTRL	0x00000000	PTP Bias Control Register
0x184	PTP_SCALE_CTRL	0x00000000	PTP Scale Control Register
0x185	PTP_W_STEP	0x00000000	PTP Width Step Register
0x186	PTP_H_STEP	0x00000000	PTP Height Step Register
0x187	PTP_STEP_OUT	0x00000000	PTP Step Out Register
0x188	PTP_C_STEP	0x00000000	PTP Channel Step Register
0x190	PTP_IACT_ADDR	0x00000000	PTP Input Activation Control Register
0x191	PTP_IACT_SPARSE	0x00000000	PTP Input Activation Sparse Register
0x192	PTP_CTAG_ADDR	0x00000000	PTP Input Activation Compression TAG address
0x193	PTP_PAD_ADDR	0x00000000	PTP Pad Memory Address Register
0x194	PTP_WEIGHT_ADDR	0x00000000	PTP Weight Memory Address Register
0x195	PTP_BIAS_ADDR	0x00000000	PTP BIAS Memory Address Register
0x196	PTP_SCALE_ADDR	0x00000000	PTP Scale Memory Address Register
0x197	PTP_PAD_UnB_ADDR	0x00000000	PTP Pad UnB Address Register
0x198	PTP_WEIGHT_UnB_ADDR	0x00000000	PTP Weight UnB Address Register
0x199	PTP_BIAS_UnB_ADDR	0x00000000	PTP Bias UnB Address Register
0x19A	PTP_SCALE_UnB_ADDR	0x00000000	PTP Scale UnB Address Register
0x19B	PTP_IACT_W_STRIDE	0x00000000	PTP Input Activation Width Stride Register
0x19C	PTP_IACT_SURF_STRIDE	0x00000000	PTP Input Activation Surface Stride Register
0x19D	PTP_ACT_C_CTRL	0x00000000	PTP Activation Channel Control Register
0x19E	PTP_ACT_W_CTRL	0x00000000	PTP Activation Width Control Register
0x19F	PTP_ACT_H_CTRL	0x00000000	PTP Activation Height Control Register

Table A-5 MMR (Memory-Mapped Register) group

Address	Name	Reset value	Description
CR registers			
0xE0000000	AIPU_DATA_ADDR0	-	AIPU Data Address Register 0
0xE0000004	AIPU_DATA_ADDR1	-	AIPU Data Address Register 1
0xE0000008	AIPU_DATA_ADDR2	-	AIPU Data Address Register 2
0xE000000C	AIPU_DATA_ADDR3	-	AIPU Data Address Register 3
DMA registers			

Address	Name	Reset value	Description
0xE0000400	CMCR	0x00000000	Common Control Register
0xE0000404	CMSR	0x00000000	Common Status Register
0xE0000408	DMA_DESP_CTRL	0x00000000	Description Control Register
0xE000040C	ERR_BLOCK_CTRL	0x00000000	ERROR Block Control Register
0xE0000410	DMA_ALL_CHAN_STS	0x00000000	One bit represents one channel. It indicates the status of each channel—working or idle. Read only.
0xE0000414	BAD_Descriptor_addr	0x00000000	The descriptor address when transfer encounters an error. Descriptor mode only.
0xE0000418	SYNC_BAD_KEY	0x00000000	BAD KEY received
0xE0000440	CH0CR	0x00000000	CH0 Control Register
0xE0000444	CH0SR	0x00000000	CH0 Status Register
0xE0000448	CH0_INT_ADDR	0x00000000	CH0 internal memory address
0xE000044C	CH0_INT_TRANS_SIZE	0x00000000	CH0 internal memory data transfer size
0xE0000450	CH0_INT_WIDTH_STRIDE	0x00000000	CH0 internal memory data width and stride control
0xE0000454	CH0_INT_ADDR_GAP	0x00000000	CH0 internal memory address gap
0xE0000458	CH0_EXT_ADDR	0x00000000	CH0 external memory address
0xE000045C	CH0_EXT_TRANS_SIZE	0x00000000	CH0 external memory data transfer size
0xE0000460	CH0_EXT_WIDTH_STRIDE	0x00000000	CH0 external memory data width and stride control
0xE0000464	CH0_EXT_ADDR_GAP	0x00000000	CH0 external memory address gap
0xE0000468	CH0_IMM_DATA	0x00000000	CH0 IMM DATA
0xE000046C	CH0_SYNC_CTRL	0x00000000	CH0 key board load/deposit control
0xE0000470	CH0_SYNC_KEY	0x00000000	The expect key value of key fetch
0xE0000480	CH1CR	0x00000000	CH1 Control Register
0xE0000484	CH1SR	0x00000000	CH1 Status Register
0xE0000488	CH1_INT_ADDR	0x00000000	CH1 internal memory address
0xE000048C	CH1_INT_TRANS_SIZE	0x00000000	CH1 internal memory data transfer size
0xE0000490	CH1_INT_WIDTH_STRIDE	0x00000000	CH1 internal memory data width and stride control
0xE0000494	CH1_INT_ADDR_GAP	0x00000000	CH1 internal memory address gap
0xE0000498	CH1_EXT_ADDR	0x00000000	CH1 external memory address
0xE000049C	CH1_EXT_TRANS_SIZE	0x00000000	CH1 external memory data transfer size
0xE00004A0	CH1_EXT_WIDTH_STRIDE	0x00000000	CH1 external memory data width and stride control
0xE00004A4	CH1_EXT_ADDR_GAP	0x00000000	CH1 external memory address gap
0xE00004A8	CH1_IMM_DATA	0x00000000	CH1 IMM DATA
0xE00004AC	CH1_SYNC_CTRL	0x00000000	CH1 Key Board Load/Deposit control
0xE00004B0	CH1_SYNC_KEY	0x00000000	The expect key value of key fetch
0xE00004C0	CH2CR	0x00000000	CH2 Control Register
0xE00004C4	CH2SR	0x00000000	CH2 Status Register

Address	Name	Reset value	Description
0xE00004C8	CH2_INT_ADDR	0x00000000	CH2 internal memory address
0xE00004CC	CH2_INT_TRANS_SIZE	0x00000000	CH2 internal memory data transfer size
0xE00004D0	CH2_INT_WIDTH_STRIDE	0x00000000	CH2 internal memory data width and stride control
0xE00004D4	CH2_INT_ADDR_GAP	0x00000000	CH2 internal memory address gap
0xE00004D8	CH2_EXT_ADDR	0x00000000	CH2 external memory address
0xE00004DC	CH2_EXT_TRANS_SIZE	0x00000000	CH2 external memory data transfer size
0xE00004E0	CH2_EXT_WIDTH_STRIDE	0x00000000	CH2 external memory data width and stride control
0xE00004E4	CH2_EXT_ADDR_GAP	0x00000000	CH2 external memory address gap
0xE00004E8	CH2_IMM_DATA	0x00000000	CH2 IMM DATA
0xE00004EC	CH2_SYNC_CTRL	0x00000000	CH2 key board load/deposit control
0xE00004F0	CH2_SYNC_KEY	0x00000000	The expect key value of key fetch
0xE0000500	CH3CR	0x00000000	CH3 Control Register
0xE0000504	CH3SR	0x00000000	CH3 Status Register
0xE0000508	CH3_INT_ADDR	0x00000000	CH3 internal memory address
0xE000050C	CH3_INT_TRANS_SIZE	0x00000000	CH3 internal memory data transfer size
0xE0000510	CH3_INT_WIDTH_STRIDE	0x00000000	CH3 internal memory data width and stride control
0xE0000514	CH3_INT_ADDR_GAP	0x00000000	CH3 internal memory address gap
0xE0000518	CH3_EXT_ADDR	0x00000000	CH3 external memory address
0xE000051C	CH3_EXT_TRANS_SIZE	0x00000000	CH3 external memory data transfer size
0xE0000520	CH3_EXT_WIDTH_STRIDE	0x00000000	CH3 external memory data width and stride control
0xE0000524	CH3_EXT_ADDR_GAP	0x00000000	CH3 external memory address gap
0xE0000528	CH3_IMM_DATA	0x00000000	CH3 IMM DATA
0xE000052C	CH3_SYNC_CTRL	0x00000000	CH3 key board load/deposit control
0xE0000530	CH3_SYNC_KEY	0x00000000	The expect key value of key fetch
0xE0000540	CH4CR	0x00000000	CH4 Control Register. Reserved in Z2-0901.
0xE0000544	CH4SR	0x00000000	CH4 Status Register. Reserved in Z2-0901.
0xE0000548	CH4_INT_ADDR	0x00000000	CH4 internal memory address. Reserved in Z2-0901.
0xE000054C	CH4_INT_TRANS_SIZE	0x00000000	CH4 internal memory data transfer size. Reserved in Z2-0901.
0xE0000550	CH4_INT_WIDTH_STRIDE	0x00000000	CH4 internal memory data width and stride control. Reserved in Z2-0901.
0xE0000554	CH4_INT_ADDR_GAP	0x00000000	CH4 internal memory address gap. Reserved in Z2-0901.
0xE0000558	CH4_EXT_ADDR	0x00000000	CH4 external memory address. Reserved in Z2-0901.
0xE000055C	CH4_EXT_TRANS_SIZE	0x00000000	CH4 external memory data transfer size. Reserved in Z2-0901.
0xE0000560	CH4_EXT_WIDTH_STRIDE	0x00000000	CH4 external memory data width and stride control. Reserved in Z2-0901.
0xE0000564	CH4_EXT_ADDR_GAP	0x00000000	CH4 external memory address gap. Reserved in Z2-0901.
0xE0000568	CH4_IMM_DATA	0x00000000	CH4 IMM DATA. Reserved in Z2-0901.
0xE000056C	CH4_SYNC_CTRL	0x00000000	CH4 key board load/deposit control. Reserved in Z2-0901.

Address	Name	Reset value	Description
0xE0000570	CH4_SYNC_KEY	0x00000000	The expect key value of key fetch. Reserved in Z2-0901.
0xE0000580	CH5CR	0x00000000	CH5 Control Register. Reserved in Z2-0901.
0xE0000584	CH5SR	0x00000000	CH5 Status Register. Reserved in Z2-0901.
0xE0000588	CH5_INT_ADDR	0x00000000	CH5 internal memory address. Reserved in Z2-0901.
0xE000058C	CH5_INT_TRANS_SIZE	0x00000000	CH5 internal memory data transfer size. Reserved in Z2-0901.
0xE0000590	CH5_INT_WIDTH_STRIDE	0x00000000	CH5 internal memory data width and stride control. Reserved in Z2-0901.
0xE0000594	CH5_INT_ADDR_GAP	0x00000000	CH5 internal memory address gap. Reserved in Z2-0901.
0xE0000598	CH5_EXT_ADDR	0x00000000	CH5 external memory address. Reserved in Z2-0901.
0xE000059C	CH5_EXT_TRANS_SIZE	0x00000000	CH5 external memory data transfer size. Reserved in Z2-0901.
0xE00005A0	CH5_EXT_WIDTH_STRIDE	0x00000000	CH5 external memory data width and stride control. Reserved in Z2-0901.
0xE00005A4	CH5_EXT_ADDR_GAP	0x00000000	CH5 external memory address gap. Reserved in Z2-0901.
0xE00005A8	CH5_IMM_DATA	0x00000000	CH5 IMM DATA. Reserved in Z2-0901.
0xE00005AC	CH5_SYNC_CTRL	0x00000000	CH5 key board load/deposit control. Reserved in Z2-0901.
0xE00005B0	CH5_SYNC_KEY	0x00000000	The expect key value of key fetch. Reserved in Z2-0901.
0xE00005C0	CH6CR	0x00000000	CH6 Control Register. Reserved in Z2-0901.
0xE00005C4	CH6SR	0x00000000	CH6 Status Register. Reserved in Z2-0901.
0xE00005C8	CH6_INT_ADDR	0x00000000	CH6 internal memory address. Reserved in Z2-0901.
0xE00005CC	CH6_INT_TRANS_SIZE	0x00000000	CH6 internal memory data transfer size. Reserved in Z2-0901.
0xE00005D0	CH6_INT_WIDTH_STRIDE	0x00000000	CH6 internal memory data width and stride control. Reserved in Z2-0901.
0xE00005D4	CH6_INT_ADDR_GAP	0x00000000	CH6 internal memory address gap. Reserved in Z2-0901.
0xE00005D8	CH6_EXT_ADDR	0x00000000	CH6 external memory address. Reserved in Z2-0901.
0xE00005DC	CH6_EXT_TRANS_SIZE	0x00000000	CH6 external memory data transfer size. Reserved in Z2-0901.
0xE00005E0	CH6_EXT_WIDTH_STRIDE	0x00000000	CH6 external memory data width and stride control. Reserved in Z2-0901.
0xE00005E4	CH6_EXT_ADDR_GAP	0x00000000	CH6 external memory address gap. Reserved in Z2-0901.
0xE00005E8	CH6_IMM_DATA	0x00000000	CH6 IMM DATA. Reserved in Z2-0901.
0xE00005EC	CH6_SYNC_CTRL	0x00000000	CH6 key board load/deposit control. Reserved in Z2-0901.
0xE00005F0	CH6_SYNC_KEY	0x00000000	The expect key value of key fetch. Reserved in Z2-0901.
0xE0000600	CH7CR	0x00000000	CH7 Control Register. Reserved in Z2-0901.
0xE0000604	CH7SR	0x00000000	CH7 Status Register. Reserved in Z2-0901.
0xE0000608	CH7_INT_ADDR	0x00000000	CH7 internal memory address. Reserved in Z2-0901.
0xE000060C	CH7_INT_TRANS_SIZE	0x00000000	CH7 internal memory data transfer size. Reserved in Z2-0901.
0xE0000610	CH7_INT_WIDTH_STRIDE	0x00000000	CH7 internal memory data width and stride control. Reserved in Z2-0901.
0xE0000614	CH7_INT_ADDR_GAP	0x00000000	CH7 internal memory address gap. Reserved in Z2-0901.
0xE0000618	CH7_EXT_ADDR	0x00000000	CH7 external memory address. Reserved in Z2-0901.

Address	Name	Reset value	Description
0xE000061C	CH7_EXT_TRANS_SIZE	0x00000000	CH7 external memory data transfer size. Reserved in Z2-0901.
0xE0000620	CH7_EXT_WIDTH_STRIDE	0x00000000	CH7 external memory data width and stride control. Reserved in Z2-0901.
0xE0000624	CH7_EXT_ADDR_GAP	0x00000000	CH7 external memory address gap. Reserved in Z2-0901.
0xE0000628	CH7_IMM_DATA	0x00000000	CH7 IMM DATA. Reserved in Z2-0901.
0xE000062C	CH7_SYNC_CTRL	0x00000000	CH7 key board load/deposit control. Reserved in Z2-0901.
0xE0000630	CH7_SYNC_KEY	0x00000000	The expect key value of key fetch. Reserved in Z2-0901.
KeyBox registers			
0xE0001000	Keybox0_config	0x00000000	KeyBox0 Control Register
0xE0001004	Keybox1_config	0x00000000	KeyBox1 Control Register
0xE0001008	Keybox2_config	0x00000000	KeyBox2 Control Register
0xE000100C	Keybox3_config	0x00000000	KeyBox3 Control Register
0xE0001010	Keybox4_config	0x00000000	KeyBox4 Control Register
0xE0001014	Keybox5_config	0x00000000	KeyBox5 Control Register
0xE0001018	Keybox6_config	0x00000000	KeyBox6 Control Register
0xE000101C	Keybox7_config	0x00000000	KeyBox7 Control Register
0xE0001020	Keybox8_config	0x00000000	KeyBox8 Control Register
0xE0001024	Keybox9_config	0x00000000	KeyBox9 Control Register
0xE0001028	Keybox10_config	0x00000000	KeyBox10 Control Register
0xE000102C	Keybox11_config	0x00000000	KeyBox11 Control Register
0xE0001030	Keybox12_config	0x00000000	KeyBox12 Control Register
0xE0001034	Keybox13_config	0x00000000	KeyBox13 Control Register
0xE0001038	Keybox14_config	0x00000000	KeyBox14 Control Register
0xE000103C	Keybox15_config	0x00000000	KeyBox15 Control Register
0xE0001040	Keybox0_status	0x00000000	KeyBox0 Status Register
0xE0001044	Keybox1_Status	0x00000000	KeyBox1 Status Register
0xE0001048	Keybox2_Status	0x00000000	KeyBox2 Status Register
0xE000104C	Keybox3_Status	0x00000000	KeyBox3 Status Register
0xE0001050	Keybox4_Status	0x00000000	KeyBox4 Status Register
0xE0001054	Keybox5_Status	0x00000000	KeyBox5 Status Register
0xE0001058	Keybox6_Status	0x00000000	KeyBox6 Status Register
0xE000105C	Keybox7_Status	0x00000000	KeyBox7 Status Register
0xE0001060	Keybox8_Status	0x00000000	KeyBox8 Status Register
0xE0001064	Keybox9_Status	0x00000000	KeyBox9 Status Register
0xE0001068	Keybox10_Status	0x00000000	KeyBox10 Status Register
0xE000106C	Keybox11_Status	0x00000000	KeyBox11 Status Register
0xE0001070	Keybox12_Status	0x00000000	KeyBox12 Status Register

Address	Name	Reset value	Description
0xE0001074	Keybox13_Status	0x00000000	KeyBox13 Status Register
0xE0001078	Keybox14_Status	0x00000000	KeyBox14 Status Register
0xE000107C	Keybox15_Status	0x00000000	KeyBox15 Status Register
Debug registers			
0xE0000C00	DEBUG_COM_DATA	0x00000000	Debug Communication Data Register.
XBU registers			
0xE0001400	TOCR	0x00000100	XBU Timeout Control Register
0xE0001404	WR_TRANS_CR	0x00000000	XBU Transaction Counter Control
0xE0001408	WRCNT_Status	0x00000000	Read/Write Request/Data Counter Status Register
0xE000140C	RREQ_CNT	-	Read Request Counter
0xE0001410	RDATA_CNT	-	Read Data Counter Register
0xE0001414	WREQ_CNT	-	Write Request Counter
0xE0001418	WDATA_CNT	-	Write Data Counter Register

Table A-6 AIPU Debug Register group (base address is due to SoC)

Offset address	Name	Reset value	Description
0x0	DEBUG_STATUS	0x00000000	Debug Status Register
0x4	DEBUG_SAVED_ADDR	0x00000000	Debug Saved Address Register
0x8	DEBUG_SAVED_PC	0x00000000	Debug Saved PC Register
0xC	DEBUG_SAVED_SIZE	0x00000000	Debug Saved Size Register
0x10	DEBUG_DATA_COM	0x00000000	Debug Data Communication Register
0x14	DEBUG_CMD	0x00000000	Debug Command Register
0x18	DEBUG_INST_TRANS	0x00000000	Debug Instruction Transfer Register
0x1C	DEBUG_BP0_CTRL	0x00000000	Debug Breakpoint0 Ctrl Register
0x20	DEBUG_BP1_CTRL	0x00000000	Debug Breakpoint1 Ctrl Register
0x24	DEBUG_WP0_CTRL	0x00000000	Debug Watchpoint0 Ctrl Register
0x28	DEBUG_WP1_CTRL	0x00000000	Debug Watchpoint1 Ctrl Register
0x2c	DEBUG_BP0_ADDR	0x00000000	Debug Breakpoint 0 Address Register
0x30	DEBUG_BP1_ADDR	0x00000000	Debug Breakpoint 1 Address Register
0x34	DEBUG_WP0_ADDR	0x00000000	Debug Watchpoint 0 Address Register
0x38	DEBUG_WP1_ADDR	0x00000000	Debug Watchpoint 1 Address Register
0xfa8	DEV_AFF0	0x00000000	Device Affinity register 0
0xfac	DEV_AFF1	0x00000000	Device Affinity register 1
0xfb8	AUTH_STATUS	0x00000003	Authentication status register.
0xfbc	DEV_ARCH	0x00000000	Device Architecture register.
0xfc0	DEV_ID2	0x00000000	Device configuration register 2

Offset address	Name	Reset value	Description
0xfc4	DEV_ID1	0x00000000	Device configuration register
0xfc8	DEV_ID	0x00000000	Device configuration register
0xfcc	DEV_TYPE	0x00000035	Device type identifier register
0xfd0	PIDR4	0x00000000	Peripheral identifier register 4
0xfe0	PIDR0	0x00000000	Peripheral identifier register 0
0xfe4	PIDR1	0x00000000	Peripheral identifier register 1
0xfe8	PIDR2	0x00000000	Peripheral identifier register 2
0xfec	PIDR3	0x00000000	Peripheral identifier register 3
0xff0	CIDR0	0x0000000d	Component identifier register 0
0xff4	CIDR1	0x00000090	Component identifier register 1
0xff8	CIDR2	0x00000005	Component identifier register 2
0xffc	CIDR3	0x000000b1	Component identifier register 3

Table A-7 AIPU External Control Register group (base address is due to SoC)

Offset address	Name	Reset value	Description
0x0	AIPU Control	0x00000000	AIPU Control Register
0x4	AIPU Status	0x00050000	AIPU Status Register
0x8	AIPU Start PC	0x00000000	AIPU Start PC Register
0xC	AIPU Interrupt PC	0x00000010	AIPU Interrupt PC Register
0x10	AIPU IPI Control	0x00000000	AIPU IPI Control Register
0x14	AIPU Data Address 0	-	AIPU Data Address 0 Register
0x18	AIPU Data Address 1	-	AIPU Data Address 1 Register
0x1C	AIPU Data Address 2	-	AIPU Data Address 2 Register
0x20	AIPU Data Address 3	-	AIPU Data Address 3 Register
0x30	AIPU Secure Configuration	0x00000001	AIPU Secure Configuration Register
0x38	AIPU Power Control	0x00000001	AIPU Power Control Register
0x3C	AIPU Clock Control	0x00000000	AIPU Clock Control Register
0xC0	AIPU Address Space Extension 0 Control	0xC0000000	AIPU Address Space Extension 0 Control Register
0xC4	AIPU Address Space Extension 0 High Base Address	0x00000000	AIPU Address Space Extension 0 High Base Address Register
0xC8	AIPU Address Space Extension 0 Low Base Address	0x00000000	AIPU Address Space Extension 0 Low Base Address Register
0xCC	AIPU Address Space Extension 1 Control	0x00000000	AIPU Address Space Extension 1 Control Register
0xD0	AIPU Address Space Extension 1 High Base Address	-	AIPU Address Space Extension 1 High Base Address Register

Offset address	Name	Reset value	Description
0xD4	AIPU Address Space Extension 1 Low Base Address	-	AIPU Address Space Extension 1 Low Base Address Register
0xD8	AIPU Address Space Extension 2 Control	0x00000000	AIPU Address Space Extension 2 Control Register
0xDC	AIPU Address Space Extension 2 High Base Address	-	AIPU Address Space Extension 2 High Base Address Register
0xE0	AIPU Address Space Extension 2 Low Base Address	-	AIPU Address Space Extension 2 Low Base Address Register
0xE4	AIPU Address Space Extension 3 Control	0x00000000	AIPU Address Space Extension 3 Control Register
0xE8	AIPU Address Space Extension 3 High Base Address	-	AIPU Address Space Extension 3 High Base Address Register
0xEC	AIPU Address Space Extension 3 Low Base Address	-	AIPU Address Space Extension 3 Low Base Address Register
0x40	AIPU ISA version	0x00000001	AIPU ISA Version Register
0x44	AIPU TPC Feature	Z2-1104: 0x00000004 Z2-1002: 0x00000002 Z2-0901: 0x00000001	AIPU TPC Feature Register
0x48	AIPU SPU Feature	0x00000000	AIPU SPU Feature Register
0x4C	AIPU AIFF Feature	Z2-1104: 0x00030103 Z2-1002: 0x00030002 Z2-0901: 0x00000001	AIPU AIFF Feature Register
0x50	AIPU Revision ID	0x00000100	AIPU Revision ID Register
0x54	AIPU Memory Architecture Feature	Z2-1104: 0x00000370 Z2-1002: 0x00000360 Z2-0901: 0x00000160	AIPU Memory Architecture Feature Register
0x58	AIPU Instruction RAM Feature	Z2-1104: 0x00000001 Z2-1002: 0x00000000 Z2-0901: 0x00000000	AIPU Instruction RAM Feature Register
0x5C	AIPU TEC Local SRAM Feature	0x00000312	AIPU TEC Local SRAM Feature Register
0x60	AIPU Global SRAM Feature	Z2-1104: 0x00000115 Z2-1002: 0x00000115 Z2-0901: 0x00000114	AIPU Global SRAM Feature Register
0x64	AIPU Instruction Cache Feature	0x00000234	AIPU Instruction Cache Feature Register
0x68	AIPU Data Cache Feature	Z2-1104: 0x000F0134 Z2-1002: 0x000F0134 Z2-0901: 0x000F0030	AIPU Data Cache Feature Register

A.2 Zhouyi Z3 AIPU general-purpose registers summary

The following table lists all the general-purpose registers of the Zhouyi Z3 AIPU.

Table A-8 General-purpose registers

Name	Description
R31	Constant zero. Can be accessed as a source or destination register.
R0-R30	31 32-bit general-purpose registers. • All can be accessed by scalar instructions with bit fields Rd, Rn, and Rm. • R0-R6 can be accessed by scalar instructions with the bit field Rc. • R30 is implicit as Ra for sub routine calling instructions BL and BRL. • R29 is implicit as SP for stack push and pop instruction. • R0-R31 can be accessed by vector instructions as source registers with the bit field Rn. • R0-R31 can be accessed by vector instructions as destination registers with the bit field Rd.
PC	Program counter. An implicit register. It can be accessed by GPC instructions.
Ra	Return address. It is an alias of GPR R30.
SP	Stack pointer. It is an alias of GPR R29. It will decrease by 4 when pushing a word into stack, and increase by 4 when popping a word from stack.
Rc0-Rc6	Condition registers. The condition registers are aliases of the LSB of GPR R0-R6.
Rc7	Constant true.
T0-T31	32 256-bit tensor registers per TEC. All can be accessed by vector instructions with bit fields Tn, Tm, Td, and Tdn.
P0-P7	8 32-bit predication governing registers per TEC. • All can be accessed by vector instructions with bit fields Pg, Pn, Pm, Pd, and Pdn. • All can be accessed by scalar instructions with the bit field Pd.
ACC	4 256-bit accumulation registers per SIMD. Can be accessed by tensor MOV or arithmetic instructions with bit fields ACC, ACCn, and ACCd.

AIPU architectural system register summary

This section identifies the architectural system registers implemented in the AIPU core.

Table A-9 AIPU Control Register Group 0

Address	Name	Reset value	Description
0x1E0	ISA version	0x00000001	ISA Version Register
0x1E1	TPC Feature	Z3-1204: 0x00000004 Z3-1104: 0x00000004 Z3-0901: 0x00000001	TPC Feature Register
0x1E2	SPU Feature	0x00000000	SPU Feature Register
0x1E3	AIFF Feature	Z3-1204: 0x00030104 Z3-1104: 0x00030103 Z3-0901: 0x00000001	AIFF Feature Register
0x1E4	Revision ID	0x00000200	Revision ID Register
0x1E5	Memory Architecture Feature	Z3-1204: 0x00000370 Z3-1104: 0x00000370 Z3-0901: 0x00000160	Memory Architecture Feature Register
0x1E6	Instruction RAM Feature	Z3-1204: 0x00000001 Z3-1104: 0x00000001 Z3-0901: 0x00000000	Instruction RAM Feature Register
0x1E7	TEC Local SRAM Feature	0x00000312	TEC Local SRAM Feature Register
0x1E8	Global SRAM Feature	Z3-1204: 0x00000116 Z3-1104: 0x00000115 Z3-0901: 0x00000114	Global SRAM Feature Register
0x1E9	Instruction Cache Feature	0x00000234	Instruction Cache Feature Register
0x1EA	Data Cache Feature	Z3-1204: 0x000F0134 Z3-1104: 0x000F0134 Z3-0901: 0x000F0030	Data Cache Feature Register
0x007	AIPU Fault Status	0x00000000	AIPU Fault Status Register
0x008	AIPU Debug	-	AIPU Debug Register
0x020	TPC Control Enable	0x00000000	TPC control Enable Register
0x021	TPC Control Status	0x00000000	TPC Control Status Register
0x022	TPC Fault/Exception Status	0x00000000	TPC Fault/Exception Status Register
0x040	Interrupt Mask	0x80000000	Interrupt Mask Register
0x041	Interrupt Cause	0x00000000	Interrupt Cause Register
0x042	Interrupt Status	0x00000000	Interrupt Status Register
0x043	Interrupt Priority	0x00000000	Interrupt Priority Register
0x044	Interrupt Back-up Mask	0x00000000	Interrupt Back-up Mask Register
0x045	Interrupt Back-up PC	0x00000000	Interrupt Back-up PC Register
0x046	Interrupt Back-up Status	0x00000000	Interrupt Back-up Status Register

Address	Name	Reset value	Description
0x050	Cache Control	Z3-1204: 0x00000007 Z3-1104: 0x00000007 Z3-0901: 0x00000003	Cache Control Register
0x051	IRAM Configuration	0x00000000	IRAM Configuration Register
0x060	Performance Counter 0 Control	0x00000000	Performance Counter 0 Control Register
0x061	Performance Counter 1 Control	0x00000000	Performance Counter 1 Control Register
0x062	Performance Counter 2 Control	0x00000000	Performance Counter 2 Control Register
0x063	Performance Counter 3 Control	0x00000000	Performance Counter 3 Control Register
0x064	Performance Counter 0 Low 32-bit	-	Performance Counter 0 Control Low 32-bit Register
0x065	Performance Counter 0 High 32-bit	-	Performance Counter 0 Control High 32-bit Register
0x066	Performance Counter 1 Low 32-bit	-	Performance Counter 1 Control Low 32-bit Register
0x067	Performance Counter 1 High 32-bit	-	Performance Counter 1 Control High 32-bit Register
0x068	Performance Counter 2 Low 32-bit	-	Performance Counter 2 Control Low 32-bit Register
0x069	Performance Counter 2 High 32-bit	-	Performance Counter 2 Control High 32-bit Register
0x06A	Performance Counter 3 Low 32-bit	-	Performance Counter 3 Control Low 32-bit Register
0x06B	Performance Counter 3 High 32-bit	-	Performance Counter 3 Control High 32-bit Register

Table A-10 AIPU Control Register Group 1

Address	Name	Reset value	Description
0x000	TEC0_A0	0xF0000000	Fixed address pointer to point to the start of LSRAM 0 for TEC 0.
0x001	TEC0_A1	0xF0080000	Fixed address pointer to point to the start of LSRAM 1 for TEC 0.
0x002	TEC0_A2	0xF0000000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 0.
0x003	TEC0_A3	0xF0080000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 0.
0x004	TEC0_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 0, shared by all TECs.
0x005	TEC0_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 0, shared by all TECs.
0x006	TEC0_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 0.
0x007	TEC0_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 0.
0x010	TEC0_MFSR	0x00000000	Memory Fault Status Register for TEC0.
0x011	TEC0_MFFCR	0x00000000	Memory First-Fault Control Register for TEC0.
0x020	TEC1_A0	0xF0100000	Fixed address pointer to point to the start of LSRAM 0 for TEC 1. Reserved in Z3-0901.
0x021	TEC1_A1	0xF0180000	Fixed address pointer to point to the start of LSRAM 1 for TEC 1. Reserved in Z3-0901.
0x022	TEC1_A2	0xF0100000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 1. Reserved in Z3-0901.

Address	Name	Reset value	Description
0x023	TEC1_A3	0xF0180000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 1. Reserved in Z3-0901.
0x024	TEC1_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 1, shared by all TECs. Reserved in Z3-0901.
0x025	TEC1_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 1, shared by all TECs. Reserved in Z3-0901.
0x026	TEC1_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 1. Reserved in Z3-0901.
0x027	TEC1_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 1. Reserved in Z3-0901.
0x030	TEC1_MFSR	0x00000000	Memory Fault Status Register for TEC1. Reserved in Z3-0901.
0x031	TEC1_MFFCR	0x00000000	Memory First-Fault Control Register for TEC1. Reserved in Z3-0901.
0x040	TEC2_A0	0xF0200000	Fixed address pointer to point to the start of LSRAM 0 for TEC 2. Reserved in Z3-0901.
0x041	TEC2_A1	0xF0280000	Fixed address pointer to point to the start of LSRAM 1 for TEC 2. Reserved in Z3-0901.
0x042	TEC2_A2	0xF0200000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 2. Reserved in Z3-0901.
0x043	TEC2_A3	0xF0280000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 2. Reserved in Z3-0901.
0x044	TEC2_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 2, shared by all TECs. Reserved in Z3-0901.
0x045	TEC2_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 2, shared by all TECs. Reserved in Z3-0901.
0x046	TEC2_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 2. Reserved in Z3-0901.
0x047	TEC2_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 2. Reserved in Z3-0901.
0x050	TEC2_MFSR	0x00000000	Memory Fault Status Register for TEC2. Reserved in Z3-0901.
0x051	TEC2_MFFCR	0x00000000	Memory First-Fault Control Register for TEC2. Reserved in Z3-0901.
0x060	TEC3_A0	0xF0300000	Fixed address pointer to point to the start of LSRAM 0 for TEC 3. Reserved in Z3-0901.
0x061	TEC3_A1	0xF0380000	Fixed address pointer to point to the start of LSRAM 1 for TEC 3. Reserved in Z3-0901.
0x062	TEC3_A2	0xF0300000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 3. Reserved in Z3-0901.
0x063	TEC3_A3	0xF0380000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 3. Reserved in Z3-0901.
0x064	TEC3_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 3, shared by all TECs. Reserved in Z3-0901.
0x065	TEC3_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 3, shared by all TECs. Reserved in Z3-0901.
0x066	TEC3_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 3. Reserved in Z3-0901.

Address	Name	Reset value	Description
0x067	TEC3_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 3. Reserved in Z3-0901.
0x070	TEC3_MFSR	0x00000000	Memory Fault Status Register for TEC3. Reserved in Z3-0901.
0x071	TEC3_MFFCR	0x00000000	Memory First-Fault Control Register for TEC3. Reserved in Z3-0901.

Table A-11 AIPU control register group 2

Address	Name	Reset value	Description
0x000	AIFF_CTRL	0x00000000	AIFF Configuration Control Register
0x001	AIFF_DESP_ADDR	0x00000000	AIFF Descriptor Address Register
0x002	AIFF_DESP_LENGTH	0x00000000	AIFF Descriptor Length Register
0x003	AIFF_STATUS	0x00000000	AIFF Status Register
0x004	AIFF_INTR_CTRL	0x00000000	AIFF Interrupt Control Register
0x005	AIFF_SYNC_CTRL	0x00000000	AIFF Descriptor Synchronization Control Register
0x006	AIFF_SYNC_KEY	0x00000000	AIFF Synchronization Key Register
0x007	AIFF_SYNC_BAD_KEY	0x00000000	AIFF Synchronization BAD Key Register
0x010	AIFF_UTIL_CNT_CTRL	0x00000000	AIFF Utilization Counter Control
0x011	MTP0_PE_A_UTIL_CNT	-	MTP0 PE Array Utilization Counter
0x012	MTP1_PE_A_UTIL_CNT	-	MTP1 PE Array Utilization Counter
0x013	ITP_PIPE_UTIL_CNT	-	ITP Pipeline Utilization Counter
0x014	PTP_PIPE_UTIL_CNT	-	PTP Pipeline Utilization Counter
0x015	WRB_UTIL_CNT	-	WRB Utilization Counter
0x020	UNB_MTP0_BASE_ADDR	0x00000000	MTP0 Base Address in Unified Buffer Register
0x021	UNB_MTP1_BASE_ADDR	0x00000000	MTP1 Base Address in Unified Buffer Register
0x022	UNB_ITP_BASE_ADDR	0x00000000	ITP Base Address in Unified Buffer Register
0x023	UNB_PTP_BASE_ADDR	0x00000000	PTP Base Address in Unified Buffer Register
0x030	WRB_MODE CTRL	0x30000003	WRB Mode Control Register
0x031	WRB_Region0_OACT_CTRL	0x00000000	WRB Region 0 Output Activation Control Register
0x032	WRB_Region0_CBLI_CTRL	0x00000000	WRB Region 0 Output Activation Compression Block Length Info Register
0x033	WRB_Region0_CTAG_CTRL	0x00000000	WRB Region 0 Output Activation Compression Tag Register
0x034	WRB_Region0_OACT_L_STRIDE	0x00000000	WRB Region 0 Output Activation Line Stride Register
0x035	WRB_Region0_OACT_S_STRIDE	0x00000000	WRB Region 0 Output activation Surface Stride Register
0x036	WRB_Region0_INT_LS_STRIDE	0x00000000	WRB Region 0 Internal Buffer Line/Surface Stride Register
0x037	WRB_Region1_OACT_CTRL	0x00000000	WRB Region 1 Output Activation Control Register
0x038	WRB_Region1_CBLI_CTRL	0x00000000	WRB Region 1 Output Activation Compression Block Length Info Register

Address	Name	Reset value	Description
0x039	WRB_Region1_CTAG_CTRL	0x00000000	WRB Region 1 Output Activation Compression Tag Register
0x03A	WRB_Region1_OACT_L_STRIDE	0x00000000	WRB Region 1 Output Activation Line Stride Register
0x03B	WRB_Region1_OACT_S_STRIDE	0x00000000	WRB Region 1 Output Activation Surface Stride Register
0x03C	WRB_Region1_INT_LS_STRIDE	0x00000000	WRB Region 1 Internal Buffer Line/Surface Stride Register
0x060	WRB_Region0_OCTAG_S_STRIDE	0x00000000	WRB Region 0 Output Activation Compression TAG Surface Stride Register
0x061	WRB_Region0_OACT_BATCH_STRIDE	0x00000000	WRB Region 0 Output Activation Batch Stride Register
0x062	WRB_Region0_OCTAG_BATCH_STRIDE	0x00000000	WRB Region 0 Output Activation Compression TAG Batch Stride Register
0x063	WRB_Region1_OCTAG_S_STRIDE	0x00000000	WRB Region 1 Output Activation Compression TAG Surface Stride Register
0x064	WRB_Region1_OACT_BATCH_STRIDE	0x00000000	WRB Region 1 Output Activation Batch Stride Register
0x065	WRB_Region1_OCTAG_BATCH_STRIDE	0x00000000	WRB Region 1 Output Activation Compression TAG Batch Stride Register
0x066	WRB_Region0_OACT_WH_OFFS	0x00000000	WRB Region 0 Output activation offset address in width/height
0x067	WRB_Region1_OACT_WH_OFFS	0x00000000	WRB Region 1 Output activation offset address in width/height
0x040	AIFF_MMU_CTRL	0x00000000	AIFF MMU Control Register
0x041	AIFF_SEG_CTRL	0x00000000	AIFF Segment Control Register
0x042	AIFF_SEGMMU_STAT	0x00000000	AIFF MMU Status Register
0x048	AIFF_SEG0_CTRL0	0x00000000	AIFF MMU Segment 0 Control 0 Register
0x049	AIFF_SEG0_CTRL1	0x00000000	AIFF MMU Segment 0 Control 1 Register
0x04A	AIFF_SEG1_CTRL0	0x00000000	AIFF MMU Segment 1 Control 0 Register
0x04B	AIFF_SEG1_CTRL1	0x00000000	AIFF MMU Segment 1 Control 1 Register
0x04C	AIFF_SEG2_CTRL0	0x00000000	AIFF MMU Segment 2 Control 0 Register
0x04D	AIFF_SEG2_CTRL1	0x00000000	AIFF MMU Segment 2 Control 1 Register
0x04E	AIFF_SEG3_CTRL0	0x00000000	AIFF MMU Segment 3 Control 0 Register
0x04F	AIFF_SEG3_CTRL1	0x00000000	AIFF MMU Segment 3 Control 1 Register
0x080	MTP_Twin_CTRL	0x00000004	MTP Twin Control Register
0x081	MTP_ACT_TOTAL_STRIDE	0x00000000	MTP Activation Total Stride Register
0x088	MTP_INDEX_CTRL	0x00000000	MTP Index Control Register
0x090	MTP_CTRL	0x00000000	MTP Mode Control Register
0x091	MTP_BACK_END_CTRL	0x00000000	MTP Back End Control Register
0x092	MTP_UnB_CTRL	0x0000000C	MTP UnB Control Register
0x093	MTP_KERNEL_CTRL	0x00000000	MTP Kernel Control Register

Address	Name	Reset value	Description
0x094	MTP_WEIGHT_ADDR	0x00000000	MTP Weight Address Register
0x095	MTP_WEIGHT_SPARSE	0x00000000	MTP Weight Sparse Register
0x096	MTP_WEIGHT_SIZE	0x00000000	MTP Weight Size Register
0x097	MTP_W_STEP	0x00000000	MTP Width Step Register
0x098	MTP_H_STEP	0x00000000	MTP Height Step Register
0x099	MTP_BATCH_STRIDE	0x00000000	MTP BATCH STRIDE Register
0x09A	MTP_DECONV_PAD	0x00000000	MTP DECONV PAD Register
0x09B	MTP_IACT_CTAG_SURF_STRIDE	0x00000000	MTP Input Activation Compression TAG Surface Stride Register
0x09C	MTP_IACT_CTAG_BATCH_STRIDE	0x00000000	MTP Input Activation Compression TAG BATCH Stride Register
0x0A0	MTP_IACT_CTRL	0x00000000	Input Activation Control Register
0x0A1	MTP_IACT_SPARSE _R0	0x00000000	Input Activation Sparse Information Register0
0x0A2	MTP_IACT_SPARSE _R1	0x00000000	Input Activation Sparse Information Register1
0x0A3	MTP_PAD_CTRL	0x00000000	MTP padding Control Register
0x0A4	MTP_PAD_ADDR	0x00000000	MTP padding Address Register
0x0A5	MTP_IACT_W_STRIDE	0x00000000	Input Activation Width Stride Register
0x0A6	MTP_IACT_S_STRIDE	0x00000000	Input activation Surface Stride Register
0x0A7	MTP_ACT_C_CTRL	0x00000000	Activation Channel Axis Control Register
0x0A8	MTP_ACT_W_CTRL	0x00000000	Activation Width Axis Control Register
0x0A9	MTP_ACT_ H_CTRL	0x00000000	Activation Height Axis Control Register
0x0AA	MTP_FE_UNB_OFFSET	0x00000000	Deformable and Sparse UnB Offset
0x0AB	MTP_WT_COMPRESS	0x00000000	Weight Compress Format Control Register
0x0B2	MTP_BATCH_MATMUL0	0x00000000	Batch Matmul Control Register 0
0x0B3	MTP_BATCH_MATMUL1	0x00000000	Batch Matmul Control Register 1
0x0B4	MTP_BATCH_MATMUL2	0x00000000	Batch Matmul Control Register 2
0x100	ITP_MODE_CCFG	0x00000000	ITP Work Mode Configuration Register
0x101	ITP_UNB_ADDR_MCFG	0x00000000	ITP UNB Address Configuration Register
0x102	ITP_LUT_MCFG	0x00000000	ITP LUT Base Address Configuration Register
0x103	ITP_ACC_INT_DST_MCFG0	0x00000000	ITP Accumulation/Interpolation Register
0x104	ITP_ACC_DST_MCFG1	0x00000000	ITP Accumulation Register
0x108	ITP_INDEX_CCFG	0x00000000	ITP INDEX Configuration Register
0x109	ITP_LUT_DCFG0	-	ITP LUT Data Configuration Register 0
0x10A	ITP_LUT_DCFG1	0x00000000	ITP LUT Data Configuration Register 1
0x110	ITP_ACT_CCFG0	0x00000000	ITP ACT Configuration Register 0
0x111	ITP_ACT_CCFG1	0x00000000	ITP ACT Configuration Register 1

Address	Name	Reset value	Description
0x112	ITP_ACT_STEP_CCFG	0x00000000	ITP ACT STEP Configuration Register
0x113	ITP_M0_CCFG	0x00000000	ITP M0 Execution Pipe Configuration Register
0x114	ITP_M0_ALU_MCFG	0x00000000	ITP M0 ALU Parameter Base Address Register
0x115	ITP_M0_MUL_MCFG	0x00000000	ITP M0 MUL Parameter Base Address Register
0x116	ITP_M0_PCFG	0x00000000	ITP M0 Per Layer Parameter Value Register
0x117	ITP_N_M1_CCFG	0x00000000	ITP M1 Execution Pipe Configuration Register
0x118	ITP_N_M1_ALU_MCFG	0x00000000	ITP M1 ALU Parameter Base Address Register
0x119	ITP_N_M1_MUL_MCFG	0x00000000	ITP M1 MUL Parameter Base Address Register
0x11A	ITP_N_M1_PCFG	0x00000000	ITP M1 Per Layer Parameter Value Register
0x11B	ITP_E_CCFG	0x00000000	ITP E Execution Pipe Configuration Register
0x11C	ITP_E_MUL_MCFG	0x00000000	ITP E MUL Parameter Base Address Register
0x11D	ITP_E_ALU_MCFG	0x00000000	ITP E ALU Parameter Base Address Register
0x11E	ITP_EMUL_SURF_STRIDE	0x00000000	E MUL PARAMETER Surface Stride Register
0x11F	ITP_EALU_SURF_STRIDE	0x00000000	E ALU PARAMETER Surface Stride Register
0x120	ITP_OCVT_SUB_CFG	0x00000000	ITP Output Data Format Conversion Subtract Configuration Register
0x121	ITP_OCVT_MUL_CFG	0x00000000	ITP Output Data Format Conversion Multiply Configuration Register
0x122	ITP_OCVT_CFG	0x00000000	ITP Output Data Format Conversion Truncate Configuration Register
0x123	ITP_E_MUL_PCFG	0x00000000	ITP E MUL Per Layer Parameter Value Register
0x124	ITP_E_ALU_PCFG	0x00000000	ITP E ALU Per Layer Parameter Value Register
0x125	ITP_E_ALU_CLAMP_PCFG0	0x00000000	ITP E ALU Clamp High Value Register
0x126	ITP_E_ALU_CLAMP_PCFG1	0x00000000	ITP E ALU Clamp Low Value Register
0x127	ITP_E_MUL_PCVT_CCFG	0x00000000	ITP E MUL Parameter Data Format Conversion Configuration Register 0
0x128	ITP_E_MUL_PCVT_PCFG	0x00000000	ITP E MUL Parameter Format Conversion Configuration Register 1
0x129	ITP_E_ALU_PCVT_CCFG	0x00000000	ITP E ALU Parameter Data Format Conversion Configuration Register 0
0x12A	ITP_E_ALU_PCVT_PCFG	0x00000000	TP E ALU Parameter Format Conversion Configuration Register 1
0x12B	ITP_LUT_PCFG0	0x00000000	ITP LUT Pre Processing Configuration Register 0
0x12C	ITP_LUT_PCFG1	0x00000000	ITP LUT Pre Processing Configuration Register 1
0x12D	ITP_LUT_OCFG	0x00000000	ITP LUT Output Configuration Register
0x12E	ITP_OCVT_MCFG	0x00000000	ITP Output Data Format Right Shift Number Base Address Register
0x12F	ITP_E_MUL_BATCH_STRIDE	0x00000000	ITP E MUL Batch Stride Register
0x130	ITP_E_ALU_BATCH_STRIDE	0x00000000	ITP E ALU Batch Stride Register

Address	Name	Reset value	Description
0x131	ITP_ E_MUL_TOTAL_STRIDE	0x00000000	ITP E MUL Total Stride Register
0x132	ITP_E_ALU_TOTAL_STRIDE	0x00000000	ITP E ALU Total Stride Register
0x133	ITP_E_MUL_WIDTH_STRIDE	0x00000000	ITP E MUL Width Stride Register
0x134	ITP_E_ALU_WIDTH_STRIDE	0x00000000	ITP E ALU Width Stride Register
0x180	PTP_MODE	0x00000000	PTP Mode Control Register
0x181	PTP_KERNEL	0x00000000	PTP Kernel Control Register
0x182	PTP_PAD	0x00000000	PTP Padding Register
0x183	PTP_BIAS_CTRL	0x00000000	PTP Bias Control Register
0x184	PTP_SCALE_CTRL	0x00000000	PTP Scale Control Register
0x185	PTP_W_STEP	0x00000000	PTP Width Step Register
0x186	PTP_H_STEP	0x00000000	PTP Height Step Register
0x187	PTP_STEP_OUT	0x00000000	PTP Step Out Register
0x188	PTP_C_STEP	0x00000000	PTP Channel Step Register
0x190	PTP_IACT_ADDR	0x00000000	PTP Input Activation Control Register
0x191	PTP_IACT_SPARSE	0x00000000	PTP Input Activation Sparse Register
0x192	PTP_CTAG_ADDR	0x00000000	PTP Input Activation Compression TAG address
0x193	PTP_PAD_ADDR	0x00000000	PTP Pad Memory Address Register
0x194	PTP_WEIGHT_ADDR	0x00000000	PTP Weight Memory Address Register
0x195	PTP_BIAS_ADDR	0x00000000	PTP BIAS Memory Address Register
0x196	PTP_SCALE_ADDR	0x00000000	PTP Scale Memory Address Register
0x197	PTP_PAD_UnB_ADDR	0x00000000	PTP Pad UnB Address Register
0x198	PTP_WEIGHT_UnB_ADDR	0x00000000	PTP Weight UnB Address Register
0x199	PTP_BIAS_UnB_ADDR	0x00000000	PTP Bias UnB Address Register
0x19A	PTP_SCALE_UnB_ADDR	0x00000000	PTP Scale UnB Address Register
0x19B	PTP_IACT_W_STRIDE	0x00000000	PTP Input Activation Width Stride Register
0x19C	PTP_IACT_SURF_STRIDE	0x00000000	PTP Input Activation Surface Stride Register
0x19D	PTP_ACT_C_CTRL	0x00000000	PTP Activation Channel Control Register
0x19E	PTP_ACT_W_CTRL	0x00000000	PTP Activation Width Control Register
0x19F	PTP_ACT_H_CTRL	0x00000000	PTP Activation Height Control Register
0x1A0	PTP_IACT_BATCH_STRIDE	0x00000000	PTP Input Activation Batch Stride Register
0x1A1	PTP_WEIGHT_SPARSE	0x00000000	PTP Weight Sparse Register
0x1A2	PTP_ROIP_DESP_ADDR	0x00000000	PTP ROI Pooling Descriptor Address Register
0x1A3	PTP_ROIP_UnB_ADDR	0x00000000	PTP ROI Pooling Descriptor UnB Address Register
0x1A4	PTP_IACT_CTAG_SURF_STRIDE	0x00000000	PTP Input Activation Compression TAG Surface Stride Register

Address	Name	Reset value	Description
0x1A5	PTP_IACT_CTAG_BATCH_STRIDE	0x00000000	PTP Input Activation Compression TAG Batch Stride Register
0x1A6	PTP_IACT_TOTAL_STRIDE	0x00000000	PTP Input Activation Total Stride Register

Table A-12 MMR (Memory-Mapped Register) group

Address	Name	Reset value	Description
CR registers			
0xE0000000	AIPU_DATA_ADDR0	-	AIPU Data Address Register 0
0xE0000004	AIPU_DATA_ADDR1	-	AIPU Data Address Register 1
0xE0000008	AIPU_DATA_ADDR2	-	AIPU Data Address Register 2
0xE000000C	AIPU_DATA_ADDR3	-	AIPU Data Address Register 3
DMA registers			
0xE0000400	CMCR	0x00000000	Common Control Register
0xE0000404	CMSR	0x00000000	Common Status Register
0xE0000408	DMA_DESP_CTRL	0x00000000	Description Control Register
0xE000040C	ERR_BLOCK_CTRL	0x00000000	ERROR Block Control Register
0xE0000410	DMA_ALL_CHAN_STS	0x00000000	One bit represents one channel. It indicates the status of each channel—working or idle. Read only.
0xE0000414	BAD_Descriptor_addr	0x00000000	The descriptor address when transfer encounters an error. Descriptor mode only.
0xE0000418	SYNC_BAD_KEY	0x00000000	BAD KEY received
0xE0000440	CH0CR	0x00000000	CH0 Control Register
0xE0000444	CH0SR	0x00000000	CH0 Status Register
0xE0000448	CH0_INT_ADDR	0x00000000	CH0 internal memory address
0xE000044C	CH0_INT_TRANS_SIZE	0x00000000	CH0 internal memory data transfer size
0xE0000450	CH0_INT_WIDTH_STRIDE	0x00000000	CH0 internal memory data width and stride control
0xE0000454	CH0_INT_ADDR_GAP	0x00000000	CH0 internal memory address gap
0xE0000458	CH0_EXT_ADDR	0x00000000	CH0 external memory address
0xE000045C	CH0_EXT_TRANS_SIZE	0x00000000	CH0 external memory data transfer size
0xE0000460	CH0_EXT_WIDTH_STRIDE	0x00000000	CH0 external memory data width and stride control
0xE0000464	CH0_EXT_ADDR_GAP	0x00000000	CH0 external memory address gap
0xE0000468	CH0_IMM_DATA	0x00000000	CH0 IMM DATA
0xE000046C	CH0_SYNC_CTRL	0x00000000	CH0 key board load/deposit control
0xE0000470	CH0_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE0000480	CH1CR	0x00000000	CH1 Control Register

Address	Name	Reset value	Description
0xE0000484	CH1SR	0x00000000	CH1 Status Register
0xE0000488	CH1_INT_ADDR	0x00000000	CH1 internal memory address
0xE000048C	CH1_INT_TRANS_SIZE	0x00000000	CH1 internal memory data transfer size
0xE0000490	CH1_INT_WIDTH_STRIDE	0x00000000	CH1 internal memory data width and stride control
0xE0000494	CH1_INT_ADDR_GAP	0x00000000	CH1 internal memory address gap
0xE0000498	CH1_EXT_ADDR	0x00000000	CH1 external memory address
0xE000049C	CH1_EXT_TRANS_SIZE	0x00000000	CH1 external memory data transfer size
0xE00004A0	CH1_EXT_WIDTH_STRIDE	0x00000000	CH1 external memory data width and stride control
0xE00004A4	CH1_EXT_ADDR_GAP	0x00000000	CH1 external memory address gap
0xE00004A8	CH1_IMM_DATA	0x00000000	CH1 IMM DATA
0xE00004AC	CH1_SYNC_CTRL	0x00000000	CH1 key board load/deposit control
0xE00004B0	CH1_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE00004C0	CH2CR	0x00000000	CH2 Control Register
0xE00004C4	CH2SR	0x00000000	CH2 Status Register
0xE00004C8	CH2_INT_ADDR	0x00000000	CH2 internal memory address
0xE00004CC	CH2_INT_TRANS_SIZE	0x00000000	CH2 internal memory data transfer size
0xE00004D0	CH2_INT_WIDTH_STRIDE	0x00000000	CH2 internal memory data width and stride control
0xE00004D4	CH2_INT_ADDR_GAP	0x00000000	CH2 internal memory address gap
0xE00004D8	CH2_EXT_ADDR	0x00000000	CH2 external memory address
0xE00004DC	CH2_EXT_TRANS_SIZE	0x00000000	CH2 external memory data transfer size
0xE00004E0	CH2_EXT_WIDTH_STRIDE	0x00000000	CH2 external memory data width and stride control
0xE00004E4	CH2_EXT_ADDR_GAP	0x00000000	CH2 external memory address gap
0xE00004E8	CH2_IMM_DATA	0x00000000	CH2 IMM DATA
0xE00004EC	CH2_SYNC_CTRL	0x00000000	CH2 key board load/deposit control
0xE00004F0	CH2_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE0000500	CH3CR	0x00000000	CH3 Control Register
0xE0000504	CH3SR	0x00000000	CH3 Status Register
0xE0000508	CH3_INT_ADDR	0x00000000	CH3 internal memory address
0xE000050C	CH3_INT_TRANS_SIZE	0x00000000	CH3 internal memory data transfer size
0xE0000510	CH3_INT_WIDTH_STRIDE	0x00000000	CH3 internal memory data width and stride control
0xE0000514	CH3_INT_ADDR_GAP	0x00000000	CH3 internal memory address gap
0xE0000518	CH3_EXT_ADDR	0x00000000	CH3 external memory address
0xE000051C	CH3_EXT_TRANS_SIZE	0x00000000	CH3 external memory data transfer size
0xE0000520	CH3_EXT_WIDTH_STRIDE	0x00000000	CH3 external memory data width and stride control
0xE0000524	CH3_EXT_ADDR_GAP	0x00000000	CH3 external memory address gap

Address	Name	Reset value	Description
0xE0000528	CH3_IMM_DATA	0x00000000	CH3 IMM DATA
0xE000052C	CH3_SYNC_CTRL	0x00000000	CH3 key board load/deposit control
0xE0000530	CH3_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE0000540	CH4CR	0x00000000	CH4 Control Register. Reserved in Z3-0901.
0xE0000544	CH4SR	0x00000000	CH4 Status Register. Reserved in Z3-0901.
0xE0000548	CH4_INT_ADDR	0x00000000	CH4 internal memory address. Reserved in Z3-0901.
0xE000054C	CH4_INT_TRANS_SIZE	0x00000000	CH4 internal memory data transfer size. Reserved in Z3-0901.
0xE0000550	CH4_INT_WIDTH_STRIDE	0x00000000	CH4 internal memory data width and stride control. Reserved in Z3-0901.
0xE0000554	CH4_INT_ADDR_GAP	0x00000000	CH4 internal memory address gap. Reserved in Z3-0901.
0xE0000558	CH4_EXT_ADDR	0x00000000	CH4 external memory address. Reserved in Z3-0901.
0xE000055C	CH4_EXT_TRANS_SIZE	0x00000000	CH4 external memory data transfer size. Reserved in Z3-0901.
0xE0000560	CH4_EXT_WIDTH_STRIDE	0x00000000	CH4 external memory data width and stride control. Reserved in Z3-0901.
0xE0000564	CH4_EXT_ADDR_GAP	0x00000000	CH4 external memory address gap. Reserved in Z3-0901.
0xE0000568	CH4_IMM_DATA	0x00000000	CH4 IMM DATA. Reserved in Z3-0901.
0xE000056C	CH4_SYNC_CTRL	0x00000000	CH4 key board load/deposit control. Reserved in Z3-0901.
0xE0000570	CH4_SYNC_KEY	0x00000000	The expected key value of key fetch. Reserved in Z3-0901.
0xE0000580	CH5CR	0x00000000	CH5 Control Register. Reserved in Z3-0901.
0xE0000584	CH5SR	0x00000000	CH5 Status Register. Reserved in Z3-0901.
0xE0000588	CH5_INT_ADDR	0x00000000	CH5 internal memory address. Reserved in Z3-0901.
0xE000058C	CH5_INT_TRANS_SIZE	0x00000000	CH5 internal memory data transfer size. Reserved in Z3-0901.
0xE0000590	CH5_INT_WIDTH_STRIDE	0x00000000	CH5 internal memory data width and stride control. Reserved in Z3-0901.
0xE0000594	CH5_INT_ADDR_GAP	0x00000000	CH5 internal memory address gap. Reserved in Z3-0901.
0xE0000598	CH5_EXT_ADDR	0x00000000	CH5 external memory address. Reserved in Z3-0901.
0xE000059C	CH5_EXT_TRANS_SIZE	0x00000000	CH5 external memory data transfer size. Reserved in Z3-0901.
0xE00005A0	CH5_EXT_WIDTH_STRIDE	0x00000000	CH5 external memory data width and stride control. Reserved in Z3-0901.
0xE00005A4	CH5_EXT_ADDR_GAP	0x00000000	CH5 external memory address gap. Reserved in Z3-0901.
0xE00005A8	CH5_IMM_DATA	0x00000000	CH5 IMM DATA. Reserved in Z3-0901.
0xE00005AC	CH5_SYNC_CTRL	0x00000000	CH5 key board load/deposit control. Reserved in Z3-0901.
0xE00005B0	CH5_SYNC_KEY	0x00000000	The expected key value of key fetch. Reserved in Z3-0901.
0xE00005C0	CH6CR	0x00000000	CH6 Control Register. Reserved in Z3-0901.
0xE00005C4	CH6SR	0x00000000	CH6 Status Register. Reserved in Z3-0901.
0xE00005C8	CH6_INT_ADDR	0x00000000	CH6 internal memory address. Reserved in Z3-0901.
0xE00005CC	CH6_INT_TRANS_SIZE	0x00000000	CH6 internal memory data transfer size. Reserved in Z3-0901.

Address	Name	Reset value	Description
0xE00005D0	CH6_INT_WIDTH_STRIDE	0x00000000	CH6 internal memory data width and stride control. Reserved in Z3-0901.
0xE00005D4	CH6_INT_ADDR_GAP	0x00000000	CH6 internal memory address gap. Reserved in Z3-0901.
0xE00005D8	CH6_EXT_ADDR	0x00000000	CH6 external memory address. Reserved in Z3-0901.
0xE00005DC	CH6_EXT_TRANS_SIZE	0x00000000	CH6 external memory data transfer size. Reserved in Z3-0901.
0xE00005E0	CH6_EXT_WIDTH_STRIDE	0x00000000	CH6 external memory data width and stride control. Reserved in Z3-0901.
0xE00005E4	CH6_EXT_ADDR_GAP	0x00000000	CH6 external memory address gap. Reserved in Z3-0901.
0xE00005E8	CH6_IMM_DATA	0x00000000	CH6 IMM DATA. Reserved in Z3-0901.
0xE00005EC	CH6_SYNC_CTRL	0x00000000	CH6 key board load/deposit control. Reserved in Z3-0901.
0xE00005F0	CH6_SYNC_KEY	0x00000000	The expected key value of key fetch. Reserved in Z3-0901.
0xE0000600	CH7CR	0x00000000	CH7 Control Register. Reserved in Z3-0901.
0xE0000604	CH7SR	0x00000000	CH7 Status Register. Reserved in Z3-0901.
0xE0000608	CH7_INT_ADDR	0x00000000	CH7 internal memory address. Reserved in Z3-0901.
0xE000060C	CH7_INT_TRANS_SIZE	0x00000000	CH7 internal memory data transfer size. Reserved in Z3-0901.
0xE0000610	CH7_INT_WIDTH_STRIDE	0x00000000	CH7 internal memory data width and stride control. Reserved in Z3-0901.
0xE0000614	CH7_INT_ADDR_GAP	0x00000000	CH7 internal memory address gap. Reserved in Z3-0901.
0xE0000618	CH7_EXT_ADDR	0x00000000	CH7 external memory address. Reserved in Z3-0901.
0xE000061C	CH7_EXT_TRANS_SIZE	0x00000000	CH7 external memory data transfer size. Reserved in Z3-0901.
0xE0000620	CH7_EXT_WIDTH_STRIDE	0x00000000	CH7 external memory data width and stride control. Reserved in Z3-0901.
0xE0000624	CH7_EXT_ADDR_GAP	0x00000000	CH7 external memory address gap. Reserved in Z3-0901.
0xE0000628	CH7_IMM_DATA	0x00000000	CH7 IMM DATA. Reserved in Z3-0901.
0xE000062C	CH7_SYNC_CTRL	0x00000000	CH7 key board load/deposit control. Reserved in Z3-0901.
0xE0000630	CH7_SYNC_KEY	0x00000000	The expected key value of key fetch. Reserved in Z3-0901.
KeyBox registers			
0xE0001000	Keybox0_config	0x00000000	KeyBox0 Control Register
0xE0001004	Keybox1_config	0x00000000	KeyBox1 Control Register
0xE0001008	Keybox2_config	0x00000000	KeyBox2 Control Register
0xE000100C	Keybox3_config	0x00000000	KeyBox3 Control Register
0xE0001010	Keybox4_config	0x00000000	KeyBox4 Control Register
0xE0001014	Keybox5_config	0x00000000	KeyBox5 Control Register
0xE0001018	Keybox6_config	0x00000000	KeyBox6 Control Register
0xE000101C	Keybox7_config	0x00000000	KeyBox7 Control Register
0xE0001020	Keybox8_config	0x00000000	KeyBox8 Control Register
0xE0001024	Keybox9_config	0x00000000	KeyBox9 Control Register

Address	Name	Reset value	Description
0xE0001028	Keybox10_config	0x00000000	KeyBox10 Control Register
0xE000102C	Keybox11_config	0x00000000	KeyBox11 Control Register
0xE0001030	Keybox12_config	0x00000000	KeyBox12 Control Register
0xE0001034	Keybox13_config	0x00000000	KeyBox13 Control Register
0xE0001038	Keybox14_config	0x00000000	KeyBox14 Control Register
0xE000103C	Keybox15_config	0x00000000	KeyBox15 Control Register
0xE0001040	Keybox0_status	0x00000000	KeyBox0 Status Register
0xE0001044	Keybox1_Status	0x00000000	KeyBox1 Status Register
0xE0001048	Keybox2_Status	0x00000000	KeyBox2 Status Register
0xE000104C	Keybox3_Status	0x00000000	KeyBox3 Status Register
0xE0001050	Keybox4_Status	0x00000000	KeyBox4 Status Register
0xE0001054	Keybox5_Status	0x00000000	KeyBox5 Status Register
0xE0001058	Keybox6_Status	0x00000000	KeyBox6 Status Register
0xE000105C	Keybox7_Status	0x00000000	KeyBox7 Status Register
0xE0001060	Keybox8_Status	0x00000000	KeyBox8 Status Register
0xE0001064	Keybox9_Status	0x00000000	KeyBox9 Status Register
0xE0001068	Keybox10_Status	0x00000000	KeyBox10 Status Register
0xE000106C	Keybox11_Status	0x00000000	KeyBox11 Status Register
0xE0001070	Keybox12_Status	0x00000000	KeyBox12 Status Register
0xE0001074	Keybox13_Status	0x00000000	KeyBox13 Status Register
0xE0001078	Keybox14_Status	0x00000000	KeyBox14 Status Register
0xE000107C	Keybox15_Status	0x00000000	KeyBox15 Status Register
Debug registers			
0xE0000C00	DEBUG_COM_DATA	0x00000000	Debug Communication Data Register.
XBU registers			
0xE0001400	TOCR	0x00000100	XBU Timeout Control Register
0xE0001404	WR_TRANS_CR	0x00000000	XBU Transaction Counter Control
0xE0001408	WRCNT_Status	0x00000000	Read/Write Request/Data Counter Status Register
0xE000140C	RREQ_CNT	-	Read Request Counter
0xE0001410	RDATA_CNT	-	Read Data Counter Register
0xE0001414	WREQ_CNT	-	Write Request Counter
0xE0001418	WDATA_CNT	-	Write Data Counter Register

Table A-13 AIPU Debug Register group (base address is due to SoC)

Offset address	Name	Reset value	Description
0x0	DEBUG_STATUS	0x00000000	Debug Status Register
0x4	DEBUG_SAVED_ADDR	0x00000000	Debug Saved Address Register
0x8	DEBUG_SAVED_PC	0x00000000	Debug Saved PC Register
0xC	DEBUG_SAVED_SIZE	0x00000000	Debug Saved Size Register
0x10	DEBUG_DATA_COM	0x00000000	Debug Data Communication Register
0x14	DEBUG_CMD	0x00000000	Debug Command Register
0x18	DEBUG_INST_TRANS	0x00000000	Debug Instruction Transfer Register
0x1C	DEBUG_BP0_CTRL	0x00000000	Debug Breakpoint0 Ctrl Register
0x20	DEBUG_BP1_CTRL	0x00000000	Debug Breakpoint1 Ctrl Register
0x24	DEBUG_WP0_CTRL	0x00000000	Debug Watchpoint0 Ctrl Register
0x28	DEBUG_WP1_CTRL	0x00000000	Debug Watchpoint1 Ctrl Register
0x2c	DEBUG_BP0_ADDR	0x00000000	Debug Breakpoint 0 Address Register
0x30	DEBUG_BP1_ADDR	0x00000000	Debug Breakpoint 1 Address Register
0x34	DEBUG_WP0_ADDR	0x00000000	Debug Watchpoint 0 Address Register
0x38	DEBUG_WP1_ADDR	0x00000000	Debug Watchpoint 1 Address Register
0xfa8	DEV_AFF0	0x00000000	Device Affinity Register 0
0xfac	DEV_AFF1	0x00000000	Device Affinity Register 1
0xfb8	AUTH_STATUS	0x00000003	Authentication Status Register.
0xfbc	DEV_ARCH	0x00000000	Device Architecture Register.
0xfc0	DEV_ID2	0x00000000	Device Configuration Register 2
0xfc4	DEV_ID1	0x00000000	Device Configuration Register
0xfc8	DEV_ID	0x00000000	Device Configuration Register
0xfcc	DEV_TYPE	0x00000035	Device Type Identifier Register
0xfd0	PIDR4	0x00000000	Peripheral Identifier Register 4
0xfe0	PIDR0	0x00000002	Peripheral Identifier Register 0
0xfe4	PIDR1	0x0000005a	Peripheral Identifier Register 1
0xfe8	PIDR2	0x00000002	Peripheral Identifier Register 2
0xfec	PIDR3	0x00000000	Peripheral Identifier Register 3
0xff0	CIDR0	0x0000000d	Component Identifier Register 0
0xff4	CIDR1	0x00000090	Component Identifier Register 1
0xff8	CIDR2	0x00000005	Component Identifier Register 2
0xffc	CIDR3	0x000000b1	Component Identifier Register 3

Table A-14 AIPU External Control Register group (base address is due to SoC)

Offset address	Name	Reset value	Description
0x0	AIPU Control	0x00000000	AIPU Control Register
0x4	AIPU Status	0x00050000	AIPU Status Register
0x8	AIPU Start PC	0x00000000	AIPU Start PC Register
0xC	AIPU Interrupt PC	0x00000010	AIPU Interrupt PC Register
0x10	AIPU IPI Control	0x00000000	AIPU IPI Control Register
0x14	AIPU Data Address 0	-	AIPU Data Address 0 Register
0x18	AIPU Data Address 1	-	AIPU Data Address 1 Register
0x1C	AIPU Data Address 2	-	AIPU Data Address 2 Register
0x20	AIPU Data Address 3	-	AIPU Data Address 3 Register
0x30	AIPU Secure Configuration	0x00000001	AIPU Secure Configuration Register
0x38	AIPU Power Control	0x00000001	AIPU Power Control Register
0x3C	AIPU Clock Control	0x00000000	AIPU Clock Control Register
0xC0	AIPU Address Space Extension 0 Control	0xC0000000	AIPU Address Space Extension 0 Control Register
0xC4	AIPU Address Space Extension 0 High Base Address	0x00000000	AIPU Address Space Extension 0 High Base Address Register
0xC8	AIPU Address Space Extension 0 Low Base Address	0x00000000	AIPU Address Space Extension 0 Low Base Address Register
0xCC	AIPU Address Space Extension 1 Control	0x00000000	AIPU Address Space Extension 1 Control Register
0xD0	AIPU Address Space Extension 1 High Base Address	-	AIPU Address Space Extension 1 High Base Address Register
0xD4	AIPU Address Space Extension 1 Low Base Address	-	AIPU Address Space Extension 1 Low Base Address Register
0xD8	AIPU Address Space Extension 2 Control	0x00000000	AIPU Address Space Extension 2 Control Register
0xDC	AIPU Address Space Extension 2 High Base Address	-	AIPU Address Space Extension 2 High Base Address Register
0xE0	AIPU Address Space Extension 2 Low Base Address	-	AIPU Address Space Extension 2 Low Base Address Register
0xE4	AIPU Address Space Extension 3 Control	0x00000000	AIPU Address Space Extension 3 Control Register
0xE8	AIPU Address Space Extension 3 High Base Address	-	AIPU Address Space Extension 3 High Base Address Register
0xEC	AIPU Address Space Extension 3 Low Base Address	-	AIPU Address Space Extension 3 Low Base Address Register
0x40	AIPU ISA version	0x00000001	AIPU ISA Version Register
0x44	AIPU TPC Feature	Z3-1204: 0x00000004 Z3-1104: 0x00000004 Z3-0901: 0x00000001	AIPU TPC Feature Register

Offset address	Name	Reset value	Description
0x48	AIPU SPU Feature	0x00000000	AIPU SPU Feature Register
0x4C	AIPU AIFF Feature	Z3-1204: 0x00030104 Z3-1104: 0x00030103 Z3-0901: 0x00000001	AIPU AIFF Feature Register
0x50	AIPU Revision ID	0x00000200	AIPU Revision ID Register
0x54	AIPU Memory Architecture Feature	Z3-1204: 0x00000370 Z3-1104: 0x00000370 Z3-0901: 0x00000160	AIPU Memory Architecture Feature Register
0x58	AIPU Instruction RAM Feature	Z3-1204: 0x00000001 Z3-1104: 0x00000001 Z3-0901: 0x00000000	AIPU Instruction RAM Feature Register
0x5C	AIPU TEC Local SRAM Feature	0x00000312	AIPU TEC Local SRAM Feature Register
0x60	AIPU Global SRAM Feature	Z3-1204: 0x00000116 Z3-1104: 0x00000115 Z3-0901: 0x00000114	AIPU Global SRAM Feature Register
0x64	AIPU Instruction Cache Feature	0x00000234	AIPU Instruction Cache Feature Register
0x68	AIPU Data Cache Feature	Z3-1204: 0x000F0134 Z3-1104: 0x000F0134 Z3-0901: 0x000F0030	AIPU Data Cache Feature Register

A.3 Zhouyi NPU X1 general-purpose registers summary

The following table lists all the general-purpose registers of the Zhouyi NPU X1.

Table A-15 General-purpose register

Name	Description
R31	Constant zero. Can be accessed as a source or destination register.
R0-R30	31 32-bit general-purpose registers. • All can be accessed by scalar instructions with bit fields Rd, Rn, and Rm. • R0-R6 can be accessed by scalar instructions with the bit field Rc. • R30 is implicit as Ra for sub routine calling instructions BL and BRL. • R29 is implicit as SP for stack push and pop instruction. • R0-R31 can be accessed by vector instructions as source registers with the bit field Rn. • R0-R31 can be accessed by vector instructions as destination registers with the bit field Rd.
PC	Program counter. An implicit register. It can be accessed by GPC instructions.
Ra	Return address. It is an alias of GPR R30.
SP	Stack pointer. It is an alias of GPR R29. It will decrease by 4 when pushing a word into stack, and increase by 4 when popping a word from stack.
Rc0-Rc6	Condition registers. The condition registers are aliases of the LSB of GPR R0-R6.
Rc7	Constant true.
T0-T31	32 256-bit tensor registers per TEC. All can be accessed by vector instructions with bit fields Tn, Tm, Td, and Tdn.
P0-P7	8 32-bit predication governing registers per TEC. • All can be accessed by vector instructions with bit fields Pg, Pn, Pm, Pd, and Pdn. • All can be accessed by scalar instructions with the bit field Pd.
ACC	4 256-bit accumulation registers per SIMD. Can be accessed by tensor MOV or arithmetic instructions with bit fields ACC, ACCn, and ACCd.

AIPU architectural system register summary

This section identifies the architectural system registers implemented in the AIPU core.

Table A-16 AIPU Control Register Group 0

Address	Name	Reset value	Description
0x1E0	ISA version	0x00000001	ISA Version Register
0x1E1	TPC Feature	0x00000004	TPC Feature Register
0x1E2	SPU Feature	0x00000000	SPU Feature Register
0x1E3	AIFF Feature	0x00030104	AIFF Feature Register
0x1E4	Revision ID	0x00000300	Revision ID Register
0x1E5	Memory Architecture Feature	0x00000370	Memory Architecture Feature Register
0x1E6	Instruction RAM Feature	0x00000001	Instruction RAM Feature Register
0x1E7	TEC Local SRAM Feature	0x00000312	TEC Local SRAM Feature Register
0x1E8	Global SRAM Feature	0x00000116	Global SRAM Feature Register
0x1E9	Instruction Cache Feature	0x00000234	Instruction Cache Feature Register
0x1EA	Data Cache Feature	0x000F0134	Data Cache Feature Register
0x007	AIPU Fault Status	0x00000000	AIPU Fault Status Register
0x008	AIPU Debug	-	AIPU Debug Register
0x020	TPC Control Enable	0x00000000	TPC control Enable Register
0x021	TPC Control Status	0x00000000	TPC Control Status Register
0x022	TPC Fault/Exception Status	0x00000000	TPC Fault/Exception Status Register
0x040	Interrupt Mask	0x80000000	Interrupt Mask Register
0x041	Interrupt Cause	0x00000000	Interrupt Cause Register
0x042	Interrupt Status	0x00000000	Interrupt Status Register
0x043	Interrupt Priority	0x00000000	Interrupt Priority Register
0x044	Interrupt Back-up Mask	0x00000000	Interrupt Back-up Mask Register
0x045	Interrupt Back-up PC	0x00000000	Interrupt Back-up PC Register
0x046	Interrupt Back-up Status	0x00000000	Interrupt Back-up Status Register
0x050	Cache Control	0x00000007	Cache Control Register
0x051	IRAM Configuration	0x00000000	IRAM Configuration Register
0x060	Performance Counter 0 Control	0x00000000	Performance Counter 0 Control Register
0x061	Performance Counter 1 Control	0x00000000	Performance Counter 1 Control Register
0x062	Performance Counter 2 Control	0x00000000	Performance Counter 2 Control Register
0x063	Performance Counter 3 Control	0x00000000	Performance Counter 3 Control Register
0x064	Performance Counter 0 Low 32-bit	-	Performance Counter 0 Control Low 32-bit Register
0x065	Performance Counter 0 High 32-bit	-	Performance Counter 0 Control High 32-bit Register
0x066	Performance Counter 1 Low 32-bit	-	Performance Counter 1 Control Low 32-bit Register

Address	Name	Reset value	Description
0x067	Performance Counter 1 High 32-bit	-	Performance Counter 1 Control High 32-bit Register
0x068	Performance Counter 2 Low 32-bit	-	Performance Counter 2 Control Low 32-bit Register
0x069	Performance Counter 2 High 32-bit	-	Performance Counter 2 Control High 32-bit Register
0x06A	Performance Counter 3 Low 32-bit	-	Performance Counter 3 Control Low 32-bit Register
0x06B	Performance Counter 3 High 32-bit	-	Performance Counter 3 Control High 32-bit Register
0x070	Performance Counter 4 Control	0x00000000	Performance Counter 4 Control Register
0x071	Performance Counter 5 Control	0x00000000	Performance Counter 5 Control Register
0x072	Performance Counter 6 Control	0x00000000	Performance Counter 6 Control Register
0x073	Performance Counter 7 Control	0x00000000	Performance Counter 7 Control Register
0x074	Performance Counter 4 Low 32-bit	-	Performance Counter 4 Control Low 32-bit Register
0x075	Performance Counter 4 High 32-bit	-	Performance Counter 4 Control High 32-bit Register
0x076	Performance Counter 5 Low 32-bit	-	Performance Counter 5 Control Low 32-bit Register
0x077	Performance Counter 5 High 32-bit	-	Performance Counter 5 Control High 32-bit Register
0x078	Performance Counter 6 Low 32-bit	-	Performance Counter 6 Control Low 32-bit Register
0x079	Performance Counter 6 High 32-bit	-	Performance Counter 6 Control High 32-bit Register
0x07A	Performance Counter 7 Low 32-bit	-	Performance Counter 7 Control Low 32-bit Register
0x07B	Performance Counter 7 High 32-bit	-	Performance Counter 7 Control High 32-bit Register

Table A-17 AIPU Control Register Group 1

Address	Name	Reset value	Description
0x000	TEC0_A0	0xF0000000	Fixed address pointer to point to the start of LSRAM 0 for TEC 0.
0x001	TEC0_A1	0xF0080000	Fixed address pointer to point to the start of LSRAM 1 for TEC 0.
0x002	TEC0_A2	0xF0000000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 0.
0x003	TEC0_A3	0xF0080000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 0.
0x004	TEC0_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 0, shared by all TECs.
0x005	TEC0_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 0, shared by all TECs.
0x006	TEC0_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 0.
0x007	TEC0_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 0.
0x010	TEC0_MFSR	0x00000000	Memory Fault Status Register for TEC0.
0x011	TEC0_MFFCR	0x00000000	Memory First-Fault Control Register for TEC0.
0x020	TEC1_A0	0xF0100000	Fixed address pointer to point to the start of LSRAM 0 for TEC 1.
0x021	TEC1_A1	0xF0180000	Fixed address pointer to point to the start of LSRAM 1 for TEC 1.
0x022	TEC1_A2	0xF0100000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 1.
0x023	TEC1_A3	0xF0180000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 1.

Address	Name	Reset value	Description
0x024	TEC1_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 1, shared by all TECs.
0x025	TEC1_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 1, shared by all TECs.
0x026	TEC1_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 1.
0x027	TEC1_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 1.
0x030	TEC1_MFSR	0x00000000	Memory Fault Status Register for TEC1.
0x031	TEC1_MFFCR	0x00000000	Memory First-Fault Control Register for TEC1.
0x040	TEC2_A0	0xF0200000	Fixed address pointer to point to the start of LSRAM 0 for TEC 2.
0x041	TEC2_A1	0xF0280000	Fixed address pointer to point to the start of LSRAM 1 for TEC 2.
0x042	TEC2_A2	0xF0200000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 2.
0x043	TEC2_A3	0xF0280000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 2.
0x044	TEC2_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 2, shared by all TECs.
0x045	TEC2_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 2, shared by all TECs..
0x046	TEC2_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 2.
0x047	TEC2_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 2.
0x050	TEC2_MFSR	0x00000000	Memory Fault Status Register for TEC2.
0x051	TEC2_MFFCR	0x00000000	Memory First-Fault Control Register for TEC2.
0x060	TEC3_A0	0xF0300000	Fixed address pointer to point to the start of LSRAM 0 for TEC 3.
0x061	TEC3_A1	0xF0380000	Fixed address pointer to point to the start of LSRAM 1 for TEC 3.
0x062	TEC3_A2	0xF0300000	Variable address pointer to point to byte aligned position of LSRAM 0/1 for TEC 3.
0x063	TEC3_A3	0xF0380000	Variable address pointer to point to byte aligned position of LSRAM 1/0 for TEC 3.
0x064	TEC3_A4	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 3, shared by all TECs.
0x065	TEC3_A5	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 3, shared by all TECs.
0x066	TEC3_A6	0xF8000000	Variable address pointer to point to byte aligned position of GSRAM 0 for TEC 3.
0x067	TEC3_A7	0xF8800000	Variable address pointer to point to byte aligned position of GSRAM 1 for TEC 3.
0x070	TEC3_MFSR	0x00000000	Memory Fault Status Register for TEC3.
0x071	TEC3_MFFCR	0x00000000	Memory First-Fault Control Register for TEC3.

Table A-18 AIPU control register group 2

Address	Name	Reset value	Description
0x000	AIFF_CTRL	0x00000000	AIFF Configuration Control Register
0x001	AIFF_DESP_ADDR	0x00000000	AIFF Descriptor Address Register
0x002	AIFF_DESP_LENGTH	0x00000000	AIFF Descriptor Length Register

Address	Name	Reset value	Description
0x003	AIFF_STATUS	0x00000000	AIFF Status Register
0x004	AIFF_INTR_CTRL	0x00000000	AIFF Interrupt Control Register
0x005	AIFF_SYNC_CTRL	0x00000000	AIFF Descriptor Synchronization Control Register
0x006	AIFF_SYNC_KEY	0x00000000	AIFF Synchronization Key Register
0x007	AIFF_SYNC_BAD_KEY	0x00000000	AIFF Synchronization BAD Key Register
0x010	AIFF_UTIL_CNT_CTRL	0x00000000	AIFF Utilization Counter Control
0x011	MTP0_PE_A_UTIL_CNT	-	MTP0 PE Array Utilization Counter
0x012	MTP1_PE_A_UTIL_CNT	-	MTP1 PE Array Utilization Counter
0x013	ITP_PIPE_UTIL_CNT	-	ITP Pipeline Utilization Counter
0x014	PTP_PIPE_UTIL_CNT	-	PTP Pipeline Utilization Counter
0x015	WRB_UTIL_CNT	-	WRB Utilization Counter
0x016	RDMA_WT_RD_CNT	-	RDMA Weight Read Counter
0x017	RDMA_ACT_RD_CNT	-	RDMA Activation Read Counter
0x018	UDMA_PARAM_RD_CNT	-	UDMA Parameter Read Counter
0x019	UDMA_ACT_WR_CNT	-	UDMA Activation Write Counter
0x01a	WDMA_ACT_WT_CNT	-	WDMA Activation Write Counter
0x01b	BIF_RD_CNT	-	BIF Read Counter
0x01c	BIF_WR_CNT	-	BIF Write Counter
0x020	UNB_MTP0_BASE_ADDR	0x00000000	MTP0 Base Address in Unified Buffer Register
0x021	UNB_MTP1_BASE_ADDR	0x00000000	MTP1 Base Address in Unified Buffer Register
0x022	UNB_ITP_BASE_ADDR	0x00000000	ITP Base Address in Unified Buffer Register
0x023	UNB_PTP_BASE_ADDR	0x00000000	PTP Base Address in Unified Buffer Register
0x030	WRB_MODE CTRL	0x30000003	WRB Mode Control Register
0x031	WRB_Region0_OACT_CTRL	0x00000000	WRB Region 0 Output Activation Control Register
0x032	WRB_Region0_CBLI_CTRL	0x00000000	WRB Region 0 Output Activation Compression Block length Info Register
0x033	WRB_Region0_CTAG_CTRL	0x00000000	WRB Region 0 Output Activation Compression Tag Register
0x034	WRB_Region0_OACT_L_STRIDE	0x00000000	WRB Region 0 Output Activation Line Stride Register
0x035	WRB_Region0_OACT_S_STRIDE	0x00000000	WRB Region 0 Output activation Surface Stride Register
0x036	WRB_Region0_INT_LS_STRIDE	0x00000000	WRB Region 0 Internal Buffer Line/Surface Stride Register
0x037	WRB_Region1_OACT_CTRL	0x00000000	WRB Region 1 Output Activation Control Register
0x038	WRB_Region1_CBLI_CTRL	0x00000000	WRB Region 1 Output Activation Compression Block length Info Register
0x039	WRB_Region1_CTAG_CTRL	0x00000000	WRB Region 1 Output Activation Compression Tag Register
0x03A	WRB_Region1_OACT_L_STRIDE	0x00000000	WRB Region 1 Output Activation Line Stride Register
0x03B	WRB_Region1_OACT_S_STRIDE	0x00000000	WRB Region 1 Output Activation Surface Stride Register

Address	Name	Reset value	Description
0x03C	WRB_Region1_INT_LS_STRIDE	0x00000000	WRB Region 1 Internal Buffer Line/Surface Stride Register
0x060	WRB_Region0_OCTAG_S_STRIDE	0x00000000	WRB Region 0 Output Activation Compression TAG Surface Stride Register
0x061	WRB_Region0_OACT_BATCH_STRIDE	0x00000000	WRB Region 0 Output Activation Batch Stride Register
0x062	WRB_Region0_OCTAG_BATCH_STRIDE	0x00000000	WRB Region 0 Output Activation Compression TAG Batch Stride Register
0x063	WRB_Region1_OCTAG_S_STRIDE	0x00000000	WRB Region 1 Output Activation Compression TAG Surface Stride Register
0x064	WRB_Region1_OACT_BATCH_STRIDE	0x00000000	WRB Region 1 Output Activation Batch Stride Register
0x065	WRB_Region1_OCTAG_BATCH_STRIDE	0x00000000	WRB Region 1 Output Activation Compression TAG Batch Stride Register
0x066	WRB_Region0_OACT_WH_OFFS	0x00000000	WRB Region 0 Output Activation Offset Address in Width/Height
0x067	WRB_Region1_OACT_WH_OFFS	0x00000000	WRB Region 1 Output Activation Offset Address in Width/Height
0x040	AIFF_MMU_CTRL	0x00000000	AIFF MMU Control Register
0x041	AIFF_SEG_CTRL	0x00000000	AIFF Segment Control Register
0x042	AIFF_SEGMMU_STAT	0x00000000	AIFF MMU Status Register
0x048	AIFF_SEG0_CTRL0	0x00000000	AIFF MMU Segment 0 Control 0 Register
0x049	AIFF_SEG0_CTRL1	0x00000000	AIFF MMU Segment 0 Control 1 Register
0x04A	AIFF_SEG1_CTRL0	0x00000000	AIFF MMU Segment 1 Control 0 Register
0x04B	AIFF_SEG1_CTRL1	0x00000000	AIFF MMU Segment 1 Control 1 Register
0x04C	AIFF_SEG2_CTRL0	0x00000000	AIFF MMU Segment 2 Control 0 Register
0x04D	AIFF_SEG2_CTRL1	0x00000000	AIFF MMU Segment 2 Control 1 Register
0x04E	AIFF_SEG3_CTRL0	0x00000000	AIFF MMU Segment 3 Control 0 Register
0x04F	AIFF_SEG3_CTRL1	0x00000000	AIFF MMU Segment 3 Control 1 Register
0x080	MTP_Twin_CTRL	0x00000004	MTP Twin Control Register
0x081	MTP_ACT_TOTAL_STRIDE	0x00000000	MTP Activation Total Stride Register
0x088	MTP_INDEX_CTRL	0x00000000	MTP Index Control Register
0x090	MTP_CTRL	0x00000000	MTP Mode Control Register
0x091	MTP_BACK_END_CTRL	0x00000000	MTP Back End Control Register
0x092	MTP_UnB_CTRL	0x0000000C	MTP UnB Control Register
0x093	MTP_KERNEL_CTRL	0x00000000	MTP Kernel Control Register
0x094	MTP_WEIGHT_ADDR	0x00000000	MTP Weight Address Register
0x095	MTP_WEIGHT_SPARSE	0x00000000	MTP Weight Sparse Register
0x096	MTP_WEIGHT_SIZE	0x00000000	MTP Weight Size Register
0x097	MTP_W_STEP	0x00000000	MTP Width Step Register

Address	Name	Reset value	Description
0x098	MTP_H_STEP	0x00000000	MTP Height Step Register
0x099	MTP_BATCH_STRIDE	0x00000000	MTP BATCH STRIDE Register
0x09A	MTP_DECONV_PAD	0x00000000	MTP DECONV PAD Register
0x09B	MTP_IACT_CTAG_SURF_STRIDE	0x00000000	MTP Input Activation Compression TAG Surface Stride Register
0x09C	MTP_IACT_CTAG_BATCH_STRIDE	0x00000000	MTP Input Activation Compression TAG BATCH Stride Register
0x0A0	MTP_IACT_CTRL	0x00000000	Input Activation Control Register
0x0A1	MTP_IACT_SPARSE _R0	0x00000000	Input Activation Sparse Information Register0
0x0A2	MTP_IACT_SPARSE _R1	0x00000000	Input Activation Sparse Information Register1
0x0A3	MTP_PAD_CTRL	0x00000000	MTP padding Control Register
0x0A4	MTP_PAD_ADDR	0x00000000	MTP padding Address Register
0x0A5	MTP_IACT_W_STRIDE	0x00000000	Input Activation Width Stride Register
0x0A6	MTP_IACT_S_STRIDE	0x00000000	Input activation Surface Stride Register
0x0A7	MTP_ACT_C_CTRL	0x00000000	Activation Channel Axis Control Register
0x0A8	MTP_ACT_W_CTRL	0x00000000	Activation Width Axis Control Register
0x0A9	MTP_ACT_ H_CTRL	0x00000000	Activation Height Axis Control Register
0x0AA	MTP_FE_UNB_OFFSET	0x00000000	Deformable and Sparse UnB Offset
0x0AB	MTP_WT_COMPRESS	0x00000000	Weight Compress Format Control Register
0x0B2	MTP_BATCH_MATMUL0	0x00000000	Batch Matmul Control Register 0
0x0B3	MTP_BATCH_MATMUL1	0x00000000	Batch Matmul Control Register 1
0x0B4	MTP_BATCH_MATMUL2	0x00000000	Batch Matmul Control Register 2
0x100	ITP_MODE_CCFG	0x00000000	ITP Work Mode Configuration Register
0x101	ITP_UNB_ADDR_MCFG	0x00000000	ITP UNB Address Configuration Register
0x102	ITP_LUT_MCFG	0x00000000	ITP LUT Base Address Configuration Register
0x103	ITP_ACC_INT_DST_MCFG0	0x00000000	ITP Accumulation/Interpolation Register
0x104	ITP_ACC_DST_MCFG1	0x00000000	ITP Accumulation Register
0x108	ITP_INDEX_CCFG	0x00000000	ITP INDEX Configuration Register
0x109	ITP_LUT_DCFG0	-	ITP LUT Data Configuration Register 0
0x10A	ITP_LUT_DCFG1	0x00000000	ITP LUT Data Configuration Register 1
0x10B	ITP_LIN_INT_OCFG	0x00000000	ITP Linear Interpolation Output Configuration Register
0x10C	ITP_LIN_INT_CCFG0	0x00000000	ITP Linear Interpolation Control Configuration Register 0
0x10D	ITP_LIN_INT_CCFG1	0x00000000	ITP Linear Interpolation Control Configuration Register 1
0x10E	ITP_LIN_INT_START_OFFSET0	0x00000000	ITP Linear Interpolation Start Offset Configuration Register 0
0x10F	ITP_LIN_INT_START_OFFSET1	0x00000000	ITP Linear Interpolation Start Offset Configuration Register 1
0x110	ITP_ACT_CCFG0	0x00000000	ITP ACT Configuration Register 0

Address	Name	Reset value	Description
0x111	ITP_ACT_CCFG1	0x00000000	ITP ACT Configuration Register 1
0x112	ITP_ACT_STEP_CCFG	0x00000000	ITP ACT STEP Configuration Register
0x113	ITP_M0_CCFG	0x00000000	ITP M0 Execution Pipe Configuration Register
0x114	ITP_M0_ALU_MCFG	0x00000000	ITP M0 ALU Parameter Base Address Register
0x115	ITP_M0_MUL_MCFG	0x00000000	ITP M0 MUL Parameter Base Address Register
0x116	ITP_M0_PCFG	0x00000000	ITP M0 Per Layer Parameter Value Register
0x117	ITP_N_M1_CCFG	0x00000000	ITP M1 Execution Pipe Configuration Register
0x118	ITP_N_M1_ALU_MCFG	0x00000000	ITP M1 ALU Parameter Base Address Register
0x119	ITP_N_M1_MUL_MCFG	0x00000000	ITP M1 MUL Parameter Base Address Register
0x11A	ITP_N_M1_PCFG	0x00000000	ITP M1 Per Layer Parameter Value Register
0x11B	ITP_E_CCFG	0x00000000	ITP E Execution Pipe Configuration Register
0x11C	ITP_E_MUL_MCFG	0x00000000	ITP E MUL Parameter Base Address Register
0x11D	ITP_E_ALU_MCFG	0x00000000	ITP E ALU Parameter Base Address Register
0x11E	ITP_EMUL_SURF_STRIDE	0x00000000	E MUL PARAMETER Surface Stride Register
0x11F	ITP_EALU_SURF_STRIDE	0x00000000	E ALU PARAMETER Surface Stride Register
0x120	ITP_OCVT_SUB_CFG	0x00000000	ITP Output Data Format Conversion Subtract Configuration Register
0x121	ITP_OCVT_MUL_CFG	0x00000000	ITP Output Data Format Conversion Multiply Configuration Register
0x122	ITP_OCVT_CFG	0x00000000	ITP Output Data Format Conversion Truncate Configuration Register
0x123	ITP_E_MUL_PCFG	0x00000000	ITP E MUL Per Layer Parameter Value Register
0x124	ITP_E_ALU_PCFG	0x00000000	ITP E ALU Per Layer Parameter Value Register
0x125	ITP_E_ALU_CLAMP_PCFG0	0x00000000	ITP E ALU Clamp High Value Register
0x126	ITP_E_ALU_CLAMP_PCFG1	0x00000000	ITP E ALU Clamp Low Value Register
0x127	ITP_E_MUL_PCVT_CCFG	0x00000000	ITP E MUL Parameter Data Format Conversion Configuration Register 0
0x128	ITP_E_MUL_PCVT_PCFG	0x00000000	ITP E MUL Parameter Format Conversion Configuration Register 1
0x129	ITP_E_ALU_PCVT_CCFG	0x00000000	ITP E ALU Parameter Data Format Conversion Configuration Register 0
0x12A	ITP_E_ALU_PCVT_PCFG	0x00000000	TP E ALU Parameter Format Conversion Configuration Register 1
0x12B	ITP_LUT_PCFG0	0x00000000	ITP LUT Pre Processing Configuration Register 0
0x12C	ITP_LUT_PCFG1	0x00000000	ITP LUT Pre Processing Configuration Register 1
0x12D	ITP_LUT_OCFG	0x00000000	ITP LUT Output Configuration Register
0x12E	ITP_OCVT_MCFG	0x00000000	ITP Output Data Format Right Shift Number Base Address Register
0x12F	ITP_E_MUL_BATCH_STRIDE	0x00000000	ITP E MUL Batch Stride Register

Address	Name	Reset value	Description
0x130	ITP_E_ALU_BATCH_STRIDE	0x00000000	ITP E ALU Batch Stride Register
0x131	ITP_ E_MUL_TOTAL_STRIDE	0x00000000	ITP E MUL Total Stride Register
0x132	ITP_E_ALU_TOTAL_STRIDE	0x00000000	ITP E ALU Total Stride Register
0x133	ITP_E_MUL_WIDTH_STRIDE	0x00000000	ITP E MUL Width Stride Register
0x134	ITP_E_ALU_WIDTH_STRIDE	0x00000000	ITP E ALU Width Stride Register
0x180	PTP_MODE	0x00000000	PTP Mode Control Register
0x181	PTP_KERNEL	0x00000000	PTP Kernel Control Register
0x182	PTP_PAD	0x00000000	PTP Padding Register
0x183	PTP_BIAS_CTRL	0x00000000	PTP Bias Control Register
0x184	PTP_SCALE_CTRL	0x00000000	PTP Scale Control Register
0x185	PTP_W_STEP	0x00000000	PTP Width Step Register
0x186	PTP_H_STEP	0x00000000	PTP Height Step Register
0x187	PTP_STEP_OUT	0x00000000	PTP Step Out Register
0x188	PTP_C_STEP	0x00000000	PTP Channel Step Register
0x190	PTP_IACT_ADDR	0x00000000	PTP Input Activation Control Register
0x191	PTP_IACT_SPARSE	0x00000000	PTP Input Activation Sparse Register
0x192	PTP_CTAG_ADDR	0x00000000	PTP Input Activation Compression TAG address
0x193	PTP_PAD_ADDR	0x00000000	PTP Pad Memory Address Register
0x194	PTP_WEIGHT_ADDR	0x00000000	PTP Weight Memory Address Register
0x195	PTP_BIAS_ADDR	0x00000000	PTP BIAS Memory Address Register
0x196	PTP_SCALE_ADDR	0x00000000	PTP Scale Memory Address Register
0x197	PTP_PAD_UnB_ADDR	0x00000000	PTP Pad UnB Address Register
0x198	PTP_WEIGHT_UnB_ADDR	0x00000000	PTP Weight UnB Address Register
0x199	PTP_BIAS_UnB_ADDR	0x00000000	PTP Bias UnB Address Register
0x19A	PTP_SCALE_UnB_ADDR	0x00000000	PTP Scale UnB Address Register
0x19B	PTP_IACT_W_STRIDE	0x00000000	PTP Input Activation Width Stride Register
0x19C	PTP_IACT_SURF_STRIDE	0x00000000	PTP Input Activation Surface Stride Register
0x19D	PTP_ACT_C_CTRL	0x00000000	PTP Activation Channel Control Register
0x19E	PTP_ACT_W_CTRL	0x00000000	PTP Activation Width Control Register
0x19F	PTP_ACT_H_CTRL	0x00000000	PTP Activation Height Control Register
0x1A0	PTP_IACT_BATCH_STRIDE	0x00000000	PTP Input Activation Batch Stride Register
0x1A1	PTP_WEIGHT_SPARSE	0x00000000	PTP Weight Sparse Register
0x1A2	PTP_ROIP_DESP_ADDR	0x00000000	PTP ROI Pooling Descriptor Address Register
0x1A3	PTP_ROIP_UnB_ADDR	0x00000000	PTP ROI Pooling Descriptor UnB Address Register
0x1A4	PTP_IACT_CTAG_SURF_STRIDE	0x00000000	PTP Input Activation Compression TAG Surface Stride Register

Address	Name	Reset value	Description
0x1A5	PTP_IACT_CTAG_BATCH_STRIDE	0x00000000	PTP Input Activation Compression TAG Batch Stride Register
0x1A6	PTP_IACT_TOTAL_STRIDE	0x00000000	PTP Input Activation Total Stride Register

Table A-19 MMR (Memory-Mapped Register) group

Address	Name	Reset value	Description
CR registers			
0xE0000000	AIPU_DATA_ADDR0	-	AIPU Data Address Register 0
0xE0000004	AIPU_DATA_ADDR1	-	AIPU Data Address Register 1
0xE0000008	AIPU_DATA_ADDR2	-	AIPU Data Address Register 2
0xE000000C	AIPU_DATA_ADDR3	-	AIPU Data Address Register 3
DMA registers			
0xE0000400	CMCR	0x00000000	Common Control Register
0xE0000404	CMSR	0x00000000	Common Status Register
0xE0000408	DMA_DESP_CTRL	0x00000000	Description Control Register
0xE000040C	ERR_BLOCK_CTRL	0x00000000	ERROR Block Control Register
0xE0000410	DMA_ALL_CHAN_STS	0x00000000	One bit represents one channel. It indicates the status of each channel—working or idle. Read only.
0xE0000414	BAD_Descriptor_addr	0x00000000	The descriptor address when transfer encounters an error. Descriptor mode only.
0xE0000418	SYNC_BAD_KEY	0x00000000	BAD KEY received
0xE0000440	CH0CR	0x00000000	CH0 Control Register
0xE0000444	CH0SR	0x00000000	CH0 Status Register
0xE0000448	CH0_INT_ADDR	0x00000000	CH0 internal memory address
0xE000044C	CH0_INT_TRANS_SIZE	0x00000000	CH0 internal memory data transfer size
0xE0000450	CH0_INT_WIDTH_STRIDE	0x00000000	CH0 internal memory data width and stride control
0xE0000454	CH0_INT_ADDR_GAP	0x00000000	CH0 internal memory address gap
0xE0000458	CH0_EXT_ADDR	0x00000000	CH0 external memory address
0xE000045C	CH0_EXT_TRANS_SIZE	0x00000000	CH0 external memory data transfer size
0xE0000460	CH0_EXT_WIDTH_STRIDE	0x00000000	CH0 external memory data width and stride control
0xE0000464	CH0_EXT_ADDR_GAP	0x00000000	CH0 external memory address gap
0xE0000468	CH0_IMM_DATA	0x00000000	CH0 IMM DATA
0xE000046C	CH0_SYNC_CTRL	0x00000000	CH0 key board load/deposit control
0xE0000470	CH0_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE0000480	CH1CR	0x00000000	CH1 Control Register
0xE0000484	CH1SR	0x00000000	CH1 Status Register

Address	Name	Reset value	Description
0xE0000488	CH1_INT_ADDR	0x00000000	CH1 internal memory address
0xE000048C	CH1_INT_TRANS_SIZE	0x00000000	CH1 internal memory data transfer size
0xE0000490	CH1_INT_WIDTH_STRIDE	0x00000000	CH1 internal memory data width and stride control
0xE0000494	CH1_INT_ADDR_GAP	0x00000000	CH1 internal memory address gap
0xE0000498	CH1_EXT_ADDR	0x00000000	CH1 external memory address
0xE000049C	CH1_EXT_TRANS_SIZE	0x00000000	CH1 external memory data transfer size
0xE00004A0	CH1_EXT_WIDTH_STRIDE	0x00000000	CH1 external memory data width and stride control
0xE00004A4	CH1_EXT_ADDR_GAP	0x00000000	CH1 external memory address gap
0xE00004A8	CH1_IMM_DATA	0x00000000	CH1 IMM DATA
0xE00004AC	CH1_SYNC_CTRL	0x00000000	CH1 key board load/deposit control
0xE00004B0	CH1_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE00004C0	CH2CR	0x00000000	CH2 Control Register
0xE00004C4	CH2SR	0x00000000	CH2 Status Register
0xE00004C8	CH2_INT_ADDR	0x00000000	CH2 internal memory address
0xE00004CC	CH2_INT_TRANS_SIZE	0x00000000	CH2 internal memory data transfer size
0xE00004D0	CH2_INT_WIDTH_STRIDE	0x00000000	CH2 internal memory data width and stride control
0xE00004D4	CH2_INT_ADDR_GAP	0x00000000	CH2 internal memory address gap
0xE00004D8	CH2_EXT_ADDR	0x00000000	CH2 external memory address
0xE00004DC	CH2_EXT_TRANS_SIZE	0x00000000	CH2 external memory data transfer size
0xE00004E0	CH2_EXT_WIDTH_STRIDE	0x00000000	CH2 external memory data width and stride control
0xE00004E4	CH2_EXT_ADDR_GAP	0x00000000	CH2 external memory address gap
0xE00004E8	CH2_IMM_DATA	0x00000000	CH2 IMM DATA
0xE00004EC	CH2_SYNC_CTRL	0x00000000	CH2 key board load/deposit control
0xE00004F0	CH2_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE0000500	CH3CR	0x00000000	CH3 Control Register
0xE0000504	CH3SR	0x00000000	CH3 Status Register
0xE0000508	CH3_INT_ADDR	0x00000000	CH3 internal memory address
0xE000050C	CH3_INT_TRANS_SIZE	0x00000000	CH3 internal memory data transfer size
0xE0000510	CH3_INT_WIDTH_STRIDE	0x00000000	CH3 internal memory data width and stride control
0xE0000514	CH3_INT_ADDR_GAP	0x00000000	CH3 internal memory address gap
0xE0000518	CH3_EXT_ADDR	0x00000000	CH3 external memory address
0xE000051C	CH3_EXT_TRANS_SIZE	0x00000000	CH3 external memory data transfer size
0xE0000520	CH3_EXT_WIDTH_STRIDE	0x00000000	CH3 external memory data width and stride control
0xE0000524	CH3_EXT_ADDR_GAP	0x00000000	CH3 external memory address gap
0xE0000528	CH3_IMM_DATA	0x00000000	CH3 IMM DATA

Address	Name	Reset value	Description
0xE000052C	CH3_SYNC_CTRL	0x00000000	CH3 key board load/deposit control
0xE0000530	CH3_SYNC_KEY	0x00000000	The expected key value of key fetch
0xE0000540	CH4CR	0x00000000	CH4 Control Register.
0xE0000544	CH4SR	0x00000000	CH4 Status Register.
0xE0000548	CH4_INT_ADDR	0x00000000	CH4 internal memory address.
0xE000054C	CH4_INT_TRANS_SIZE	0x00000000	CH4 internal memory data transfer size.
0xE0000550	CH4_INT_WIDTH_STRIDE	0x00000000	CH4 internal memory data width and stride control.
0xE0000554	CH4_INT_ADDR_GAP	0x00000000	CH4 internal memory address gap.
0xE0000558	CH4_EXT_ADDR	0x00000000	CH4 external memory address.
0xE000055C	CH4_EXT_TRANS_SIZE	0x00000000	CH4 external memory data transfer size.
0xE0000560	CH4_EXT_WIDTH_STRIDE	0x00000000	CH4 external memory data width and stride control.
0xE0000564	CH4_EXT_ADDR_GAP	0x00000000	CH4 external memory address gap.
0xE0000568	CH4_IMM_DATA	0x00000000	CH4 IMM DATA.
0xE000056C	CH4_SYNC_CTRL	0x00000000	CH4 key board load/deposit control.
0xE0000570	CH4_SYNC_KEY	0x00000000	The expected key value of key fetch.
0xE0000580	CH5CR	0x00000000	CH5 Control Register.
0xE0000584	CH5SR	0x00000000	CH5 Status Register.
0xE0000588	CH5_INT_ADDR	0x00000000	CH5 internal memory address.
0xE000058C	CH5_INT_TRANS_SIZE	0x00000000	CH5 internal memory data transfer size.
0xE0000590	CH5_INT_WIDTH_STRIDE	0x00000000	CH5 internal memory data width and stride control.
0xE0000594	CH5_INT_ADDR_GAP	0x00000000	CH5 internal memory address gap.
0xE0000598	CH5_EXT_ADDR	0x00000000	CH5 external memory address.
0xE000059C	CH5_EXT_TRANS_SIZE	0x00000000	CH5 external memory data transfer size.
0xE00005A0	CH5_EXT_WIDTH_STRIDE	0x00000000	CH5 external memory data width and stride control.
0xE00005A4	CH5_EXT_ADDR_GAP	0x00000000	CH5 external memory address gap.
0xE00005A8	CH5_IMM_DATA	0x00000000	CH5 IMM DATA.
0xE00005AC	CH5_SYNC_CTRL	0x00000000	CH5 key board load/deposit control.
0xE00005B0	CH5_SYNC_KEY	0x00000000	The expected key value of key fetch.
0xE00005C0	CH6CR	0x00000000	CH6 Control Register.
0xE00005C4	CH6SR	0x00000000	CH6 Status Register.
0xE00005C8	CH6_INT_ADDR	0x00000000	CH6 internal memory address.
0xE00005CC	CH6_INT_TRANS_SIZE	0x00000000	CH6 internal memory data transfer size.
0xE00005D0	CH6_INT_WIDTH_STRIDE	0x00000000	CH6 internal memory data width and stride control.
0xE00005D4	CH6_INT_ADDR_GAP	0x00000000	CH6 internal memory address gap.
0xE00005D8	CH6_EXT_ADDR	0x00000000	CH6 external memory address.

Address	Name	Reset value	Description
0xE00005DC	CH6_EXT_TRANS_SIZE	0x00000000	CH6 external memory data transfer size.
0xE00005E0	CH6_EXT_WIDTH_STRIDE	0x00000000	CH6 external memory data width and stride control.
0xE00005E4	CH6_EXT_ADDR_GAP	0x00000000	CH6 external memory address gap.
0xE00005E8	CH6_IMM_DATA	0x00000000	CH6 IMM DATA.
0xE00005EC	CH6_SYNC_CTRL	0x00000000	CH6 key board load/deposit control.
0xE00005F0	CH6_SYNC_KEY	0x00000000	The expected key value of key fetch.
0xE0000600	CH7CR	0x00000000	CH7 Control Register.
0xE0000604	CH7SR	0x00000000	CH7 Status Register.
0xE0000608	CH7_INT_ADDR	0x00000000	CH7 internal memory address.
0xE000060C	CH7_INT_TRANS_SIZE	0x00000000	CH7 internal memory data transfer size.
0xE0000610	CH7_INT_WIDTH_STRIDE	0x00000000	CH7 internal memory data width and stride control.
0xE0000614	CH7_INT_ADDR_GAP	0x00000000	CH7 internal memory address gap.
0xE0000618	CH7_EXT_ADDR	0x00000000	CH7 external memory address.
0xE000061C	CH7_EXT_TRANS_SIZE	0x00000000	CH7 external memory data transfer size.
0xE0000620	CH7_EXT_WIDTH_STRIDE	0x00000000	CH7 external memory data width and stride control.
0xE0000624	CH7_EXT_ADDR_GAP	0x00000000	CH7 external memory address gap.
0xE0000628	CH7_IMM_DATA	0x00000000	CH7 IMM DATA.
0xE000062C	CH7_SYNC_CTRL	0x00000000	CH7 key board load/deposit control.
0xE0000630	CH7_SYNC_KEY	0x00000000	The expected key value of key fetch.
KeyBox registers			
0xE0001000	Keybox0_config	0x00000000	KeyBox0 Control Register
0xE0001004	Keybox1_config	0x00000000	KeyBox1 Control Register
0xE0001008	Keybox2_config	0x00000000	KeyBox2 Control Register
0xE000100C	Keybox3_config	0x00000000	KeyBox3 Control Register
0xE0001010	Keybox4_config	0x00000000	KeyBox4 Control Register
0xE0001014	Keybox5_config	0x00000000	KeyBox5 Control Register
0xE0001018	Keybox6_config	0x00000000	KeyBox6 Control Register
0xE000101C	Keybox7_config	0x00000000	KeyBox7 Control Register
0xE0001020	Keybox8_config	0x00000000	KeyBox8 Control Register
0xE0001024	Keybox9_config	0x00000000	KeyBox9 Control Register
0xE0001028	Keybox10_config	0x00000000	KeyBox10 Control Register
0xE000102C	Keybox11_config	0x00000000	KeyBox11 Control Register
0xE0001030	Keybox12_config	0x00000000	KeyBox12 Control Register
0xE0001034	Keybox13_config	0x00000000	KeyBox13 Control Register
0xE0001038	Keybox14_config	0x00000000	KeyBox14 Control Register

Address	Name	Reset value	Description
0xE000103C	Keybox15_config	0x00000000	KeyBox15 Control Register
0xE0001040	Keybox0_status	0x00000000	KeyBox0 Status Register
0xE0001044	Keybox1_Status	0x00000000	KeyBox1 Status Register
0xE0001048	Keybox2_Status	0x00000000	KeyBox2 Status Register
0xE000104C	Keybox3_Status	0x00000000	KeyBox3 Status Register
0xE0001050	Keybox4_Status	0x00000000	KeyBox4 Status Register
0xE0001054	Keybox5_Status	0x00000000	KeyBox5 Status Register
0xE0001058	Keybox6_Status	0x00000000	KeyBox6 Status Register
0xE000105C	Keybox7_Status	0x00000000	KeyBox7 Status Register
0xE0001060	Keybox8_Status	0x00000000	KeyBox8 Status Register
0xE0001064	Keybox9_Status	0x00000000	KeyBox9 Status Register
0xE0001068	Keybox10_Status	0x00000000	KeyBox10 Status Register
0xE000106C	Keybox11_Status	0x00000000	KeyBox11 Status Register
0xE0001070	Keybox12_Status	0x00000000	KeyBox12 Status Register
0xE0001074	Keybox13_Status	0x00000000	KeyBox13 Status Register
0xE0001078	Keybox14_Status	0x00000000	KeyBox14 Status Register
0xE000107C	Keybox15_Status	0x00000000	KeyBox15 Status Register
Debug registers			
0xE0000C00	DEBUG_COM_DATA	0x00000000	Debug Communication Data Register.
XBU registers			
0xE0001400	TOCR	0x00000100	XBU Timeout Control Register
0xE0001404	WR_TRANS_CR	0x00000000	XBU Transaction Counter Control
0xE0001408	WRCNT_Status	0x00000000	Read/Write Request/Data Counter Status Register
0xE000140C	RREQ_CNT	-	Read Request Counter
0xE0001410	RDATA_CNT	-	Read Data Counter Register
0xE0001414	WREQ_CNT	-	Write Request Counter
0xE0001418	WDATA_CNT	-	Write Data Counter Register

Table A-20 AIPU Debug Register group (base address is due to SoC)

Offset address	Name	Reset value	Description
0x0	DEBUG_STATUS	0x00000000	Debug Status Register
0x4	DEBUG_SAVED_ADDR	0x00000000	Debug Saved Address Register
0x8	DEBUG_SAVED_PC	0x00000000	Debug Saved PC Register
0xC	DEBUG_SAVED_SIZE	0x00000000	Debug Saved Size Register
0x10	DEBUG_DATA_COM	0x00000000	Debug Data Communication Register

Offset address	Name	Reset value	Description
0x14	DEBUG_CMD	0x00000000	Debug Command Register
0x18	DEBUG_INST_TRANS	0x00000000	Debug Instruction Transfer Register
0x1C	DEBUG_BP0_CTRL	0x00000000	Debug Breakpoint0 Ctrl Register
0x20	DEBUG_BP1_CTRL	0x00000000	Debug Breakpoint1 Ctrl Register
0x24	DEBUG_WP0_CTRL	0x00000000	Debug Watchpoint0 Ctrl Register
0x28	DEBUG_WP1_CTRL	0x00000000	Debug Watchpoint1 Ctrl Register
0x2c	DEBUG_BP0_ADDR	0x00000000	Debug Breakpoint 0 Address Register
0x30	DEBUG_BP1_ADDR	0x00000000	Debug Breakpoint 1 Address Register
0x34	DEBUG_WP0_ADDR	0x00000000	Debug Watchpoint 0 Address Register
0x38	DEBUG_WP1_ADDR	0x00000000	Debug Watchpoint 1 Address Register
0xfa8	DEV_AFF0	0x00000000	Device Affinity Register 0
0xfac	DEV_AFF1	0x00000000	Device Affinity Register 1
0xfb8	AUTH_STATUS	0x00000003	Authentication Status Register.
0xfbc	DEV_ARCH	0x00000000	Device Architecture Register.
0xfc0	DEV_ID2	0x00000000	Device Configuration Register 2
0xfc4	DEV_ID1	0x00000000	Device Configuration Register
0xfc8	DEV_ID	0x00000000	Device Configuration Register
0xfcc	DEV_TYPE	0x00000035	Device Type Identifier Register
0xfd0	PIDR4	0x00000000	Peripheral Identifier Register 4
0xfe0	PIDR0	0x00000003	Peripheral Identifier Register 0
0xfe4	PIDR1	0x0000005a	Peripheral Identifier Register 1
0xfe8	PIDR2	0x00000002	Peripheral Identifier Register 2
0xfec	PIDR3	0x00000000	Peripheral Identifier Register 3
0xff0	CIDR0	0x0000000d	Component Identifier Register 0
0xff4	CIDR1	0x00000090	Component Identifier Register 1
0xff8	CIDR2	0x00000005	Component Identifier Register 2
0xffc	CIDR3	0x000000b1	Component Identifier Register 3

Table A-21 AIPU External Control Register group (base address is due to SoC)

Offset address	Name	Reset value	Description
0x0	AIPU Control	0x00000000	AIPU Control Register
0x4	AIPU Status	0x00050000	AIPU Status Register
0x8	AIPU Start PC	0x00000000	AIPU Start PC Register
0xC	AIPU Interrupt PC	0x00000010	AIPU Interrupt PC Register
0x10	AIPU IPI Control	0x00000000	AIPU IPI Control Register

Offset address	Name	Reset value	Description
0x14	AIPU Data Address 0	-	AIPU Data Address 0 Register
0x18	AIPU Data Address 1	-	AIPU Data Address 1 Register
0x1C	AIPU Data Address 2	-	AIPU Data Address 2 Register
0x20	AIPU Data Address 3	-	AIPU Data Address 3 Register
0x30	AIPU Secure Configuration	0x00000001	AIPU Secure Configuration Register
0x38	AIPU Power Control	0x00000001	AIPU Power Control Register
0x3C	AIPU Clock Control	0x00000000	AIPU Clock Control Register
0xC0	AIPU Address Space Extension 0 Control	0xC0000000	AIPU Address Space Extension 0 Control Register
0xC4	AIPU Address Space Extension 0 High Base Address	0x00000000	AIPU Address Space Extension 0 High Base Address Register
0xC8	AIPU Address Space Extension 0 Low Base Address	0x00000000	AIPU Address Space Extension 0 Low Base Address Register
0xCC	AIPU Address Space Extension 1 Control	0x00000000	AIPU Address Space Extension 1 Control Register
0xD0	AIPU Address Space Extension 1 High Base Address	-	AIPU Address Space Extension 1 High Base Address Register
0xD4	AIPU Address Space Extension 1 Low Base Address	-	AIPU Address Space Extension 1 Low Base Address Register
0xD8	AIPU Address Space Extension 2 Control	0x00000000	AIPU Address Space Extension 2 Control Register
0xDC	AIPU Address Space Extension 2 High Base Address	-	AIPU Address Space Extension 2 High Base Address Register
0xE0	AIPU Address Space Extension 2 Low Base Address	-	AIPU Address Space Extension 2 Low Base Address Register
0xE4	AIPU Address Space Extension 3 Control	0x00000000	AIPU Address Space Extension 3 Control Register
0xE8	AIPU Address Space Extension 3 High Base Address	-	AIPU Address Space Extension 3 High Base Address Register
0xEC	AIPU Address Space Extension 3 Low Base Address	-	AIPU Address Space Extension 3 Low Base Address Register
0x40	AIPU ISA version	0x00000001	AIPU ISA Version Register
0x44	AIPU TPC Feature	0x00000004	AIPU TPC Feature Register
0x48	AIPU SPU Feature	0x00000000	AIPU SPU Feature Register
0x4C	AIPU AIFF Feature	0x00030104	AIPU AIFF Feature Register
0x50	AIPU Revision ID	0x00000300	AIPU Revision ID Register
0x54	AIPU Memory Architecture Feature	0x00000370	AIPU Memory Architecture Feature Register
0x58	AIPU Instruction RAM Feature	0x00000001	AIPU Instruction RAM Feature Register
0x5C	AIPU TEC Local SRAM Feature	0x00000312	AIPU TEC Local SRAM Feature Register
0x60	AIPU Global SRAM Feature	0x00000116	AIPU Global SRAM Feature Register
0x64	AIPU Instruction Cache Feature	0x00000234	AIPU Instruction Cache Feature Register

Offset address	Name	Reset value	Description
0x68	AIPU Data Cache Feature	0x000F0134	AIPU Data Cache Feature Register
0x180	AIPU Data Tightly Coupled Memory Control	0x00000000	AIPU Data Tightly Coupled Memory Control Register
0x184	AIPU Data Tightly Coupled Memory High Base Address	0x00000000	AIPU Data Tightly Coupled Memory High Base Address Register
0x188	AIPU Data Tightly Coupled Memory Low Base Address	0x00000000	AIPU Data Tightly Coupled Memory Low Base Address Register
0x200	AIPU Soft Reset	0x00000000	AIPU Soft Reset Register

A.4 Zhouyi NPU X2 general-purpose registers summary

The following table lists all the general-purpose registers of the Zhouyi NPU X2.

Table A-22 General-purpose register

Name	Description
R31	Constant zero. Can be accessed as a source or destination register.
R0-R30	31 32-bit general-purpose registers. • All can be accessed by integer scalar instructions with bit fields Rd, Rn, and Rm. • R30 is implicit as Ra for sub routine calling instructions BL, BRL and BRRL. • R0-R31 can be accessed by integer vector instructions as source registers with the bit field Rn. • R0-R31 can be accessed by integer vector instructions as destination registers with the bit field Rd. • R0-R31 can be accessed by floating-point scalar instructions as source registers with the bit field Rn. • R0-R31 can be accessed by floating-point scalar instructions as destination registers with the bit field Rd.
PC	Program counter. An implicit register. It can be accessed by MFCTRL instructions.
Ra	Return address. It is an alias of GPR R30.
T0-T31	32 256-bit vector registers per TEC. • All can be accessed by integer vector instructions with bit fields Tn, Tm, Td, and Tdn. • All can be accessed by floating-point vector instructions with bit fields Tn, Tm, Td, and Tdn.
P0-P7	8 32-bit predication governing registers per TEC. • All can be accessed by integer vector instructions with bit fields Pg, Pn, Pm, Pd, and Pdn. • All can be accessed by floating-point vector instructions with bit fields Pg, Pd.
F0-F31	They are alias of LSB 32-bit of T0-T31. All can be accessed by floating-point scalar instructions with bit fields Fn, Fm, Fd, Fdn.

AIPU architectural system register summary

This section identifies the architectural system registers implemented in the AIPU core.

Table A-23 Host-TSM Registers

Address	Name	Reset value	Description
0x00000c00	Cluster 0 Configuration	X2-1204MP3: 0x00001314 X2-1204: 0x00001114	Cluster 0 Configuration Register
0x00000c04	Cluster 0 Control	0x00000000	Cluster 0 Control Register
0x00000000	TSM Command Schedule Control Handle	0x00000000	TSM Command Schedule Control Handle Register
0x00000004	TSM Command Schedule Control Info	0x00000000	TSM Command Schedule Control Info Register
0x00000008	TSM Command Schedule Address High	0x00000000	TSM Command Schedule Address High Register
0x0000000c	TSM Command Schedule Address Low	0x00000000	TSM Command Schedule Address Low Register
0x00000010	TSM Configuration	0x00000000	TSM Configuration Register
0x00000014	TSM Build Info	0x00010000	TSM Build Info Register
0x00000018	TSM Status	0x00000000	TSM Status Register
0x00000020	TSM Soft Reset	0x00000000	TSM Soft Reset Register
0x00000050	TSM Revision ID	X2-1204MP3: 0x00010003 X2-1204: 0x00010000	TSM Revision ID Register
0x00000060	Tick Counter Low	0x00000000	Tick Counter Low Register
0x00000064	Tick Counter High	0x00000000	Tick Counter High Register
0x00000068	Tick Counter Control Status	0x00000000	Tick Counter Control Status Register
0x00000800	TSM Command Pool 0 Configuration	0x00000000	TSM Command Pool 0 Configuration Register
0x00000804	TSM Command Pool 0 Status	0x00000040	TSM Command Pool 0 Status Register
0x00000808	TSM Command Pool 0 Interrupt Control	0x00000000	TSM Command Pool 0 Interrupt Control Register
0x0000080c	TSM Command Pool 0 Interrupt Status	0x00000000	TSM Command Pool 0 Interrupt Status Register
0x00000810	TSM Command Pool 0 IRQ Signal	0x00000000	TSM Command Pool 0 IRQ Signal Register
0x00000814	TSM Command Pool 0 First Bad Command Info	0x00000000	TSM Command Pool 0 First Bad Command Info Register
0x00000818	TSM Command Pool 0 Executing Command Info	0x00000000	TSM Command Pool 0 Executing Command Info Register
0x0000081c	TSM Command Pool 0 Secure Configuration	0x00000001	TSM Command Pool 0 Secure Configuration Register
0x00000820	TSM Command Pool 0 IRQ Signal Flag	0x00000000	TSM Command Pool 0 IRQ Signal Flag Register
0x00000824	TSM Command Pool 0 Interrupt TCB Pointer	0x00000000	TSM Command Pool 0 Interrupt TCB Pointer Register

Address	Name	Reset value	Description
0x00001f00	Debug Page Selection Control	0x00000000	Debug Page Selection Control Register
0x00002000	Cluster Identification	0x00000000	Cluster Identification Register
0x00002004	Cluster Status	0x00000060	Cluster Status Register
0x00002008	Cluster Idle Status	0x00000001	Cluster Idle Status Register
0x00002020	Cluster Core Control	X2-1204MP3: 0x00000007 X2-1204: 0x00000001	Cluster Core Control Register
0x00002030	Cluster Interrupt Control	0x00000000	Cluster Interrupt Control Register
0x00002034	Cluster Interrupt Status	0x00000000	Cluster Interrupt Status Register
0x00002038	Cluster IRQ Signal	0x00000000	Cluster IRQ Signal
0x0000203c	Cluster IRQ Signal Flag	0x00000000	Cluster IRQ Signal Flag Register
0x00002040	Cluster Secure Control	0x00000001	Cluster Secure Control Register
0x00002044	Cluster Clock & Power Control	0x00000003	Cluster Clock & Power Control Register
0x00002064	Cluster Start Control ID	0x00000000	Cluster Start Control ID Register
0x00002070	Global Memory Control	X2-1204MP3: 0x00030000 X2-1204: 0x00010000	Global Memory Control Register
0x00002074	Global Memory Status	0x00000000	Global Memory Status Register
0x00002078	Global Memory Region 0 Control	0x00000000	Global Memory Region 0 Control Register
0x0000207c	Global Memory Region 1 Control	0x00000000	Global Memory Region 1 Control Register
0x00002084	Global Memory Region 0 Remap Address High	0x00000000	Global Memory Region 0 Remap Address High Register
0x00002080	Global Memory Region 0 Remap Address Low	0x00000000	Global Memory Region 0 Remap Address Low Register
0x0000208c	Global Memory Region 1 Remap Address High	0x00000000	Global Memory Region 1 Remap Address High Register
0x00002088	Global Memory Region 1 Remap Address Low	0x00000000	Global Memory Region 1 Remap Address Low Register
0x00002094	Cluster Address Space Extension 0 High Base Address	0x00000000	Cluster Address Space Extension 0 High Base Address Register
0x00002090	Cluster Address Space Extension 0 Low Base Address	0x00000060	Cluster Address Space Extension 0 Low Base Address Register
0x0000209c	Cluster Address Space Extension 1 High Base Address	0x00000000	Cluster Address Space Extension 1 High Base Address Register
0x00002098	Cluster Address Space Extension 1 Low Base Address	0x00000060	Cluster Address Space Extension 1 Low Base Address Register
0x000020a4	Cluster Address Space Extension 2 High Base Address	0x00000000	Cluster Address Space Extension 2 High Base Address Register
0x000020a0	Cluster Address Space Extension 2 Low Base Address	0x00000060	Cluster Address Space Extension 2 Low Base Address Register
0x000020ac	Cluster Address Space Extension 3 High Base Address	0x00000000	Cluster Address Space Extension 3 High Base Address Register

Address	Name	Reset value	Description
0x000020a8	Cluster Address Space Extension 3 Low Base Address	0x00000060	Cluster Address Space Extension 3 Low Base Address Register
0x000020b0	Cluster Data Tightly Coupled Memory Low Base Address	0x00000000	Cluster Data Tightly Coupled Memory Low Base Address
0x000020b4	Cluster Data Tightly Coupled Memory High Base Address	0x00000000	Cluster Data Tightly Coupled Memory High Base Address
0x000020d8	Core Memory Segment Control	0x00000000	Core Memory Segment Control
0x000020dc	Core Segment Remap Control	0x00000000	Core Segment Remap Control
0x000020d0	Core Segment Remap Status	0x00000000	Core Segment Remap Status
0x000020e0	Core Segment 0 Control 0	0x00000000	Core Segment 0 Control 0
0x000020e4	Core Segment 0 Control 1	0x00000000	Core Segment 0 Control 1
0x000020e8	Core Segment 1 Control 0	0x00000000	Core Segment 1 Control 0
0x000020ec	Core Segment 1 Control 1	0x00000000	Core Segment 1 Control 1
0x000020f0	Core Segment 2 Control 0	0x00000000	Core Segment 2 Control 0
0x000020f4	Core Segment 2 Control 1	0x00000000	Core Segment 2 Control 1
0x000020f8	Core Segment 3 Control 0	0x00000000	Core Segment 3 Control 0
0x000020fc	Core Segment 3 Control 1	0x00000000	Core Segment 3 Control 1
0x00002800	ISA Version	0x00000003	ISA Version Register
0x00002804	TEC Feature 0	0x00000000	TEC Feature 0 Register
0x00002808	TEC Feature 1	0x00000000	TEC Feature 1 Register
0x0000280c	TEC Feature 2	0x00020ef1	TEC Feature 2 Register
0x00002810	DMA Feature	0x00000000	DMA Feature Register
0x00002814	AIFF Feature	0x0c570104	AIFF Feature Register
0x00002818	Customization Feature	0x00000000	Customization Feature Register
0x00002820	Revision ID	X2-1204MP3: 0x00010003 X2-1204: 0x00010000	Revision ID Register
0x00002840	Memory Hierarchy Feature	0x00000371	Memory Hierarchy Feature Register
0x00002844	TEC Internal Buffer Feature	0x00002243	TEC Internal Buffer Feature Register
0x00002848	TEC Local Memory Feature	0x00001411	TEC Local Memory Feature Register
0x0000284c	Core Share Memory Feature	0x00000314	Core Share Memory Feature Register
0x00002850	Core Instruction Cache Feature	0x00000235	Core Instruction Cache Feature Register
0x00002854	Core Data Cache Feature	0x00070235	Core Data Cache Feature Register
0x00002858	Cluster Global Memory Feature	X2-1204MP3: 0x00000415 X2-1204: 0x00000313	Cluster Global Memory Feature Register
0x00003000	Core Identification	0x00000000	Core Identification Register
0x00003004	Core Status Registers	0x00000030	Core Status Registers
0x00003008	Core Idle Status	0x000000ff	Core Idle Status Register
0x00003020	Core Configuration 0	0x0000000f	Core Configuration 0 Register

Address	Name	Reset value	Description
0x00003024	Core Configuration 1	0x00000001	Core Configuration 1 Register
0x00003050	Core Instruction Cache Config	0x00000000	Core Instruction Cache Config Register
0x00003054	Core Data Cache Config	0x00000000	Core Data Cache Config Register
0x00003080	Core Start Control	0x00000000	Core Start Control Register
0x00003084	Core Start PC	0x00000000	Core Start PC Register
0x00003088	Core Start Control Batch ID	0x00000000	Core Start Control Batch ID Register
0x00003090	Core Interrupt Control	0x00000000	Core Interrupt Control Register
0x00003094	Core Interrupt Status	0x00000000	Core Interrupt Status Register
0x00003098	Core IRQ Signal	0x00000000	Core IRQ Signal Register
0x0000309c	Core IRQ Signal Flag	0x00000000	Core IRQ Signal Flag Register
0x000030c0	Core HTS Control	0x00000000	Core HTS Control Register
0x000030c4	Core HTS Status	0x00000000	Core HTS Status Register
0x000030d8	Core Memory Segment Control	0x00000000	Core Memory Segment Control Register
0x000030dc	Core Segment Remap Control	0x00000000	Core Segment Remap Control Register
0x000030d0	Core Segment Remap Status	0x00000000	Core Segment Remap Status Register
0x000030e0	Core Segment 0 Control 0	0x00000000	Core Segment 0 Control 0 Register
0x000030e4	Core Segment 0 Control 1	0x00000000	Core Segment 0 Control 1 Register
0x000030e8	Core Segment 1 Control 0	0x00000000	Core Segment 1 Control 0 Register
0x000030ec	Core Segment 1 Control 1	0x00000000	Core Segment 1 Control 1 Register
0x000030f0	Core Segment 2 Control 0	0x00000000	Core Segment 2 Control 0 Register
0x000030f4	Core Segment 2 Control 1	0x00000000	Core Segment 2 Control 1 Register
0x000030f8	Core Segment 3 Control 0	0x00000000	Core Segment 3 Control 0 Register
0x000030fc	Core Segment 3 Control 1	0x00000000	Core Segment 3 Control 1 Register
0x00003100	Core Start Control ID TEC0	0x00000000	Core Start Control ID TEC0 Register
0x00003140	Core Interrupt Control TEC0	0x00000000	Core Interrupt Control TEC0 Register
0x00003180	Core Start Task Configuration Block Pointer TEC0	0x00000000	Core Start Task Configuration Block Pointer TEC0 Register
0x000031c0	Core Interrupt Status TEC0	0x00000000	Core Interrupt Status TEC0 Register
0x00003104	Core Start Control ID TEC1	0x00000000	Core Start Control ID TEC1 Register
0x00003144	Core Interrupt Control TEC1	0x00000000	Core Interrupt Control TEC1 Register
0x00003184	Core Start Task Configuration Block Pointer TEC1	0x00000000	Core Start Task Configuration Block Pointer TEC1 Register
0x000031c4	Core Interrupt Status TEC1	0x00000000	Core Interrupt Status TEC1 Register
0x00003108	Core Start Control ID TEC2	0x00000000	Core Start Control ID TEC2 Register
0x00003148	Core Interrupt Control TEC2	0x00000000	Core Interrupt Control TEC2 Register
0x00003188	Core Start Task Configuration Block Pointer TEC2	0x00000000	Core Start Task Configuration Block Pointer TEC2 Register
0x000031c8	Core Interrupt Status TEC2	0x00000000	Core Interrupt Status TEC2 Register

Address	Name	Reset value	Description
0x0000310c	Core Start Control ID TEC3	0x00000000	Core Start Control ID TEC3 Register
0x0000314c	Core Interrupt Control TEC3	0x00000000	Core Interrupt Control TEC3 Register
0x0000318c	Core Start Task Configuration Block Pointer TEC3	0x00000000	Core Start Task Configuration Block Pointer TEC3 Register
0x000031cc	Core Interrupt Status TEC3	0x00000000	Core Interrupt Status TEC3 Register

Table A-24 TEC Registers

Address	Name	Reset value	Description
0x000	TEC Identification	0x00000000	TEC Identification Register
0x001	TEC Batch ID	0x00000000	TEC Batch ID Register
0x010	TEC Program Counter	0x00000000	TEC Program Counter Register
0x014	TEC Task Configuration Block Pointer	0x00000000	TEC Task Configuration Block Pointer Register
0x030	TEC Synchronization Flag	0x00000000	TEC Synchronization Flag Register
0x031	TEC WFE Control	0x00000000	TEC WFE Control Register
0x032	TEC IRQ Signal	0x00010000	TEC IRQ Signal Register
0x033	TEC IRQ Signal Flag	0x00000000	TEC IRQ Signal Flag Register
0x040	TEC Interrupt Mask	0x80000000	TEC Interrupt Mask Register
0x041	TEC Interrupt Priority	0x00000000	TEC Interrupt Priority Register
0x044	TEC Interrupt Back-up Mask	0x80000000	TEC Interrupt Back-up Mask Register
0x045	TEC Interrupt Back-up PC	0x00000000	TEC Interrupt Back-up PC Register
0x080	TEC Control	0x00000000	TEC Control Register
0x081	TEC IFU Control	0x00000001	TEC IFU Control Register
0x082	TEC LSU Control	0x00000001	TEC LSU Control Register
0x090	TEC Status	0x0000007f	TEC Status Register
0x091	TEC LSU Status	0x00000000	TEC LSU Status Register
0x092	TEC Local Memory Fault Status	0x00000000	TEC Local Memory Fault Status Register
0x093	TEC Local Memory First Fault Address	0x00000000	TEC Local Memory First Fault Address Register
0x0d0	TEC Tick Counter High	0x00000000	TEC Tick Counter High Register
0x0d1	TEC Tick Counter Low	0x00000000	TEC Tick Counter Low Register
0x0e0	TEC Performance Counter 0 Control	0x00000000	TEC Performance Counter 0 Control Register
0x0e1	TEC Performance Counter 1 Control	0x00000000	TEC Performance Counter 1 Control Register
0x0e2	TEC Performance Counter 2 Control	0x00000000	TEC Performance Counter 2 Control Register
0x0e3	TEC Performance Counter 3 Control	0x00000000	TEC Performance Counter 3 Control Register

Address	Name	Reset value	Description
0x0e8	TEC Performance Counter 0	0x00000000	TEC Performance Counter 0 Register
0x0e9	TEC Performance Counter 1	0x00000000	TEC Performance Counter 1 Register
0x0ea	TEC Performance Counter 2	0x00000000	TEC Performance Counter 2 Register
0x0eb	TEC Performance Counter 3	0x00000000	TEC Performance Counter 3 Register
0x0f0	TEC Debug Data	0x00000000	TEC Debug Data Register
0x000	TEC VPE Control	0x00000000	TEC VPE Control Register
0x001	TEC VPE Status	0x00000000	TEC VPE Status Register
0x002	TEC Vector Floating-Point Control	0x00000080	TEC Vector Floating-Point Control Register
0x003	TEC Vector Floating Point Status	0x00000000	TEC Vector Floating Point Status Register
0x010	TEC Scalar Floating-Point Control	0x00000080	TEC Scalar Floating-Point Control Register
0x011	TEC Scalar Floating-Point Status	0x00000000	TEC Scalar Floating-Point Status Register
0x080	TEC VFP LS Stride 0	0x00000000	TEC VFP LS Stride 0 Register
0x081	TEC VFP LS Stride 1	0x00000000	TEC VFP LS Stride 1 Register
0x082	TEC VFP LS Stride 2	0x00000000	TEC VFP LS Stride 2 Register
0x083	TEC VFP LS Stride 3	0x00000000	TEC VFP LS Stride 3 Register
0x000	TEC AIFF Execution Status	0x00000000	TEC AIFF Execution Status Register
0x002	TEC AIFF First Bad Instruction PC	0x00000000	TEC AIFF First Bad Instruction PC
0x003	TEC AIFF Last Executed Instruction PC	0x00000000	TEC AIFF Last Executed Instruction PC
0x004	TEC AIFF Memory Access Control	0x00000123	TEC AIFF Memory Access Control
0x030	AIFF Performance Counter Control	0x00000000	AIFF Performance Counter Control
0x031	AIFF Performance Counter Config	0x1f000000	AIFF Performance Counter Config
0x040	TEC DMA Execution Status	0x00000000	TEC DMA Execution Status Register
0x042	TEC DMA First Bad PC	0x00000000	TEC DMA First Bad PC Register
0x043	TEC DMA Last Executed Instruction PC	0x00000000	TEC DMA Last Executed Instruction PC
0x044	TEC DMA Memory Access Control	0x00000000	TEC DMA Memory Access Control
0x070	TEC DMA Performance Counter Control	0x00000000	TEC DMA Performance Counter Control
0x071	TEC DMA Performance Counter Config	0x07000000	TEC DMA Performance Counter Config
0x1e0	ISA Version	0x00000003	ISA Version Register
0x1e4	DMA Feature	0x00000000	DMA Feature Register
0x1e5	AIFF Feature	0x0c570104	AIFF Feature Register
0x1e6	Customization Feature	0x00000000	Customization Feature Register
0x1e1	TEC Feature 0	0x00000000	TEC Feature 0 Register
0x1e2	TEC Feature 1	0x00000000	TEC Feature 1 Register
0x1e3	TEC Feature 2	0x00020ef1	TEC Feature 2 Register

Address	Name	Reset value	Description
0x1e8	Revision ID	X2-1204MP3: 0x00010003 X2-1204: 0x00010000	Revision ID Register
0x1e9	Memory Hierarchy Feature	0x00000371	Memory Hierarchy Feature Register
0x1eb	TEC Local Memory Feature	0x00001411	TEC Local Memory Feature Register
0x1ec	Core Share Memory Feature	0x00000314	Core Share Memory Feature Register
0x1ed	Core Instruction Cache Feature	0x00000235	Core Instruction Cache Feature Register
0x1ee	Core Data Cache Feature	0x00070235	Core Data Cache Feature Register
0x1ef	Cluster Global Memory Feature	X2-1204MP3: 0x00000415 X2-1204: 0x00000313	Cluster Global Memory Feature Register
0x1ea	TEC Internal Buffer Feature	0x00002243	TEC Internal Buffer Feature Register

Table A-25 DMA Registers

Address	Name	Reset value	Description
0x000	CH0 EXT Width Stride	0x00000000	CH0 EXT Width Stride Register
0x004	CH0 EXT Trans Size	0x00000000	CH0 EXT Trans Size Register
0x008	CH0 EXT Gap	0x00000000	CH0 EXT Gap Register
0x00c	CH0 INT GAP	0x00000000	CH0 INT GAP Register
0x010	CH0 INT Width Stride	0x00000000	CH0 INT Width Stride Register
0x014	CH0 INT Trans Size	0x00000000	CH0 INT Trans Size Register
0x020	CH0 record PC	0x00000000	CH0 record PC Register
0x024	CH0 DMA inst0 Control	0x00000000	CH0 DMA inst0 Control Register
0x028	CH0 DMA inst1 Control	0x00000000	CH0 DMA inst1 Control Register
0x02c	CH0 INT ADDR	0x00000000	CH0 INT ADDR Register
0x030	CH0 EXT ADDR	0x00000000	CH0 EXT ADDR Register
0x034	CH0 Performance Counter Control	0x00000000	CH0 Performance Counter Control Register
0x038	CH0 Performance Counter Config	0x07000000	CH0 Performance Counter Config Register
0x03c	CH0 Memory Access Control	0x00000000	CH0 Memory Access Control Register
0x040	CH0 DMA Busy Counter	0x00000000	CH0 DMA Busy Counter Register
0x044	CH0 DMA ARNUM Counter	0x00000000	CH0 DMA ARNUM Counter Register
0x048	CH0 DMA RNUM Counter	0x00000000	CH0 DMA RNUM Counter Register
0x04c	CH0 DMA AWNUM Counter	0x00000000	CH0 DMA AWNUM Counter Register
0x050	CH0 DMA WNUM Counter	0x00000000	CH0 DMA WNUM Counter Register
0x400	CH1 EXT Width Stride	0x00000000	CH1 EXT Width Stride Register
0x404	CH1 EXT Trans Size	0x00000000	CH1 EXT Trans Size Register
0x408	CH1 EXT Gap	0x00000000	CH1 EXT Gap Register
0x40c	CH1 INT GAP	0x00000000	CH1 INT GAP Register
0x410	CH1 INT Width Stride	0x00000000	CH1 INT Width Stride Register

Address	Name	Reset value	Description
0x414	CH1 INT Trans Size	0x00000000	CH1 INT Trans Size Register
0x420	CH1 record PC	0x00000000	CH1 record PC Register
0x424	CH1 DMA inst0 Control	0x00000000	CH1 DMA inst0 Control Register
0x428	CH1 DMA inst1 Control	0x00000000	CH1 DMA inst1 Control Register
0x42c	CH1 INT ADDR	0x00000000	CH1 INT ADDR Register
0x430	CH1 EXT ADDR	0x00000000	CH1 EXT ADDR Register
0x434	CH1 Performance Counter Control	0x00000000	CH1 Performance Counter Control Register
0x438	CH1 Performance Counter Config	0x07000000	CH1 Performance Counter Config Register
0x43c	CH1 Memory Access Control	0x00000000	CH1 Memory Access Control Register
0x440	CH1 DMA Busy Counter	0x00000000	CH1 DMA Busy Counter Register
0x444	CH1 DMA ARNUM Counter	0x00000000	CH1 DMA ARNUM Counter Register
0x448	CH1 DMA RNUM Counter	0x00000000	CH1 DMA RNUM Counter Register
0x44c	CH1 DMA AWNUM Counter	0x00000000	CH1 DMA AWNUM Counter Register
0x450	CH1 DMA WNUM Counter	0x00000000	CH1 DMA WNUM Counter Register
Address	**Name**	**Reset value**	**Description**
0x000	CH0 EXT Width Stride	0x00000000	CH0 EXT Width Stride Register
0x004	CH0 EXT Trans Size	0x00000000	CH0 EXT Trans Size Register
0x008	CH0 EXT Gap	0x00000000	CH0 EXT Gap Register
0x00c	CH0 INT GAP	0x00000000	CH0 INT GAP Register
0x010	CH0 INT Width Stride	0x00000000	CH0 INT Width Stride Register
0x014	CH0 INT Trans Size	0x00000000	CH0 INT Trans Size Register
0x020	CH0 record PC	0x00000000	CH0 record PC Register
0x024	CH0 DMA inst0 Control	0x00000000	CH0 DMA inst0 Control Register
0x028	CH0 DMA inst1 Control	0x00000000	CH0 DMA inst1 Control Register
0x02c	CH0 INT ADDR	0x00000000	CH0 INT ADDR Register
0x030	CH0 EXT ADDR	0x00000000	CH0 EXT ADDR Register
0x034	CH0 Performance Counter Control	0x00000000	CH0 Performance Counter Control Register
0x038	CH0 Performance Counter Config	0x07000000	CH0 Performance Counter Config Register
0x03c	CH0 Memory Access Control	0x00000000	CH0 Memory Access Control Register
0x040	CH0 DMA Busy Counter	0x00000000	CH0 DMA Busy Counter Register
0x044	CH0 DMA ARNUM Counter	0x00000000	CH0 DMA ARNUM Counter Register
0x048	CH0 DMA RNUM Counter	0x00000000	CH0 DMA RNUM Counter Register
0x04c	CH0 DMA AWNUM Counter	0x00000000	CH0 DMA AWNUM Counter Register
0x050	CH0 DMA WNUM Counter	0x00000000	CH0 DMA WNUM Counter Register
0x400	CH1 EXT Width Stride	0x00000000	CH1 EXT Width Stride Register
0x404	CH1 EXT Trans Size	0x00000000	CH1 EXT Trans Size Register
0x408	CH1 EXT Gap	0x00000000	CH1 EXT Gap Register

Address	Name	Reset value	Description
0x40c	CH1 INT GAP	0x00000000	CH1 INT GAP Register
0x410	CH1 INT Width Stride	0x00000000	CH1 INT Width Stride Register
0x414	CH1 INT Trans Size	0x00000000	CH1 INT Trans Size Register
0x420	CH1 record PC	0x00000000	CH1 record PC Register
0x424	CH1 DMA inst0 Control	0x00000000	CH1 DMA inst0 Control Register
0x428	CH1 DMA inst1 Control	0x00000000	CH1 DMA inst1 Control Register
0x42c	CH1 INT ADDR	0x00000000	CH1 INT ADDR Register
0x430	CH1 EXT ADDR	0x00000000	CH1 EXT ADDR Register
0x434	CH1 Performance Counter Control	0x00000000	CH1 Performance Counter Control Register
0x438	CH1 Performance Counter Config	0x07000000	CH1 Performance Counter Config Register
0x43c	CH1 Memory Access Control	0x00000000	CH1 Memory Access Control Register
0x440	CH1 DMA Busy Counter	0x00000000	CH1 DMA Busy Counter Register
0x444	CH1 DMA ARNUM Counter	0x00000000	CH1 DMA ARNUM Counter Register
0x448	CH1 DMA RNUM Counter	0x00000000	CH1 DMA RNUM Counter Register
0x44c	CH1 DMA AWNUM Counter	0x00000000	CH1 DMA AWNUM Counter Register
0x450	CH1 DMA WNUM Counter	0x00000000	CH1 DMA WNUM Counter Register

Table A-26 AIFF Registers

Address	Name	Reset value	Description
0x00000000	AIFF_CTRL (AIFF Status Register)	0x00000000	AIFF_CTRL (AIFF Status Register)
0x00000004	AIFF_STATUS (AIFF Status Register)	0x00000000	AIFF_STATUS (AIFF Status Register)
0x00000040	AIFF_BUSY_CYCLE_CNT (AIFF Busy Cycle Counter)	0x00000000	AIFF_BUSY_CYCLE_CNT (AIFF Busy Cycle Counter)
0x00000044	MTP0_PE_A_UTIL_CNT (MTP0 PE Array Utilization Counter)	0x00000000	MTP0_PE_A_UTIL_CNT (MTP0 PE Array Utilization Counter)
0x00000048	MTP1_PE_A_UTIL_CNT (MTP1 PE Array Utilization Counter)	0x00000000	MTP1_PE_A_UTIL_CNT (MTP1 PE Array Utilization Counter)
0x0000004c	ITP_PIPE_UTIL_CNT (ITP PIPELINE Utilization Counter)	0x00000000	ITP_PIPE_UTIL_CNT (ITP PIPELINE Utilization Counter)
0x00000050	PTP_PIPE_UTIL_CNT (PTP PIPELINE Utilization Counter)	0x00000000	PTP_PIPE_UTIL_CNT (PTP PIPELINE Utilization Counter)
0x00000054	WRB_UTIL_CNT (WRB Utilization Counter)	0x00000000	WRB_UTIL_CNT (WRB Utilization Counter)
0x00000058	RDMA_WT_RD_CNT (RDMA Weight Read Counter)	0x00000000	RDMA_WT_RD_CNT (RDMA Weight Read Counter)
0x0000005c	RDMA_ACT_RD_CNT (RDMA Activation Read Counter)	0x00000000	RDMA_ACT_RD_CNT (RDMA Activation Read Counter)
0x00000060	UDMA_PARAM_RD_CNT (UDMA Parameter Read Counter)	0x00000000	UDMA_PARAM_RD_CNT (UDMA Parameter Read Counter)

Address	Name	Reset value	Description
0x00000064	UDMA_ACT_WR_CNT (UDMA Activation Write Counter)	0x00000000	UDMA_ACT_WR_CNT (UDMA Activation Write Counter)
0x00000068	WDMA_ACT_WR_CNT (WDMA Activation Write Counter)	0x00000000	WDMA_ACT_WR_CNT (WDMA Activation Write Counter)
0x0000006c	BIF_RD_CNT (BIF Read Counter)	0x00000000	BIF_RD_CNT (BIF Read Counter)
0x00000070	BIF_WR_CNT (BIF Write Counter)	0x00000000	BIF_WR_CNT (BIF Write Counter)
0x00000074	AIFF_COM0_CNT (AIF Common 0 Counter)	0x00000000	AIFF_COM0_CNT (AIF Common 0 Counter)
0x00000078	AIFF_COM1_CNT (AIF Common 1 Counter)	0x00000000	AIFF_COM1_CNT (AIF Common 1 Counter)
0x00000080	UNB_MTP0_BASE_ADDR	0x00000000	UNB_MTP0_BASE_ADDR
0x00000084	UNB_MTP1_BASE_ADDR	0x00000000	UNB_MTP1_BASE_ADDR
0x00000088	UNB_ITP_BASE_ADDR	0x00000000	UNB_ITP_BASE_ADDR
0x0000008c	UNB_PTP_BASE_ADDR	0x00000000	UNB_PTP_BASE_ADDR
0x000000c0	WRB_Region0_OACT_ADDR	0x00000000	WRB_Region0_OACT_ADDR
0x000000c4	WRB_Region0_OACT_CTAG_ADDR	0x00000000	WRB_Region0_OACT_CTAG_ADDR
0x000000c8	WRB_Region1_OACT_ADDR	0x00000000	WRB_Region1_OACT_ADDR
0x000000cc	WRB_Region1_OACT_CTAG_ADDR	0x00000000	WRB_Region1_OACT_CTAG_ADDR
0x00000100	WRB_MODE_CTRL	0x30000003	WRB_MODE_CTRL
0x00000104	WRB_Region0_OACT_CTRL	0x00000000	WRB_Region0_OACT_CTRL
0x00000108	WRB_Region0_OACT_L_STRIDE	0x00000000	WRB_Region0_OACT_L_STRIDE
0x0000010c	WRB_Region0_OACT_S_STRIDE	0x00000000	WRB_Region0_OACT_S_STRIDE
0x00000110	WRB_Region0_INT_LS_STRIDE	0x00000000	WRB_Region0_INT_LS_STRIDE
0x00000114	WRB_Region0_OCTAG_S_STRIDE	0x00000000	WRB_Region0_OCTAG_S_STRIDE
0x00000118	WRB_Region0_OACT_BATCH_STRIDE	0x00000000	WRB_Region0_OACT_BATCH_STRIDE
0x0000011c	WRB_Region0_OCTAG_BATCH_STRIDE	0x00000000	WRB_Region0_OCTAG_BATCH_STRIDE
0x00000120	WRB_Region0_OACT_WH_OFFS	0x00000000	WRB_Region0_OACT_WH_OFFS
0x00000144	WRB_Region1_OACT_CTRL	0x00000000	WRB_Region1_OACT_CTRL
0x00000148	WRB_Region1_OACT_L_STRIDE	0x00000000	WRB_Region1_OACT_L_STRIDE
0x0000014c	WRB_Region1_OACT_S_STRIDE	0x00000000	WRB_Region1_OACT_S_STRIDE
0x00000150	WRB_Region1_INT_LS_STRIDE	0x00000000	WRB_Region1_INT_LS_STRIDE
0x00000154	WRB_Region1_OCTAG_S_STRIDE	0x00000000	WRB_Region1_OCTAG_S_STRIDE
0x00000158	WRB_Region1_OACT_BATCH_STRIDE	0x00000000	WRB_Region1_OACT_BATCH_STRIDE
0x0000015c	WRB_Region1_OCTAG_BATCH_STRIDE	0x00000000	WRB_Region1_OCTAG_BATCH_STRIDE
0x00000160	WRB_Region1_OACT_WH_OFFS	0x00000000	WRB_Region1_OACT_WH_OFFS
0x000005c0	MTP_Twin_CTRL	0x00000000	MTP_Twin_CTRL
0x00000400	MTP0_IACT_ADDR	0x00000000	MTP0_IACT_ADDR
0x00000404	MTP0_BATCH_MATMUL_IACT_ADDR	0x00000000	MTP0_BATCH_MATMUL_IACT_ADDR

Address	Name	Reset value	Description
0x00000408	MTP0_IACT_CTAG_ADDR	0x00000000	MTP0_IACT_CTAG_ADDR
0x0000040c	MTP0_Unb_ADDR	0x00000000	MTP0_Unb_ADDR
0x00000440	MTP0_WEIGHT_ADDR	0x00000000	MTP0_WEIGHT_ADDR
0x00000444	MTP0_PAD_ADDR	0x00000000	MTP0_PAD_ADDR
0x00000448	MTP0_IACT_FP_PARAM_ADDR0	0x00000000	MTP0_IACT_FP_PARAM_ADDR0
0x0000044c	MTP0_IACT_FP_PARAM_ADDR1	0x00000000	MTP0_IACT_FP_PARAM_ADDR1
0x00000480	MTP0_CTRL	0x00000000	MTP0_CTRL
0x00000484	MTP0_BE_CTRL	0x00000000	MTP0_BE_CTRL
0x00000488	MTP0_UNB_CTRL	0x00000000	MTP0_UNB_CTRL
0x0000048c	MTP0_KERNEL_CTRL	0x00000000	MTP0_KERNEL_CTRL
0x00000490	MTP0_WEIGHT_SPARSE	0x00000000	MTP0_WEIGHT_SPARSE
0x00000494	MTP0_WEIGHT_SIZE	0x00000000	MTP0_WEIGHT_SIZE
0x00000498	MTP0_W_STEP	0x00000000	MTP0_W_STEP
0x0000049c	MTP0_H_STEP	0x00000000	MTP0_H_STEP
0x000004a0	MTP0_BATCH_STRIDE	0x00000000	MTP0_BATCH_STRIDE
0x000004a4	MTP0_DECONV_PAD	0x00000000	MTP0_DECONV_PAD
0x000004a8	MTP0_IACT_CTAG_SURF_STRIDE	0x00000000	MTP0_IACT_CTAG_SURF_STRIDE
0x000004ac	MTP0_IACT_CTAG_BATCH_STRIDE	0x00000000	MTP0_IACT_CTAG_BATCH_STRIDE
0x000004b0	MTP0_IACT_CTRL	0x00000000	MTP0_IACT_CTRL
0x000004b4	MTP0_PAD_SIZE	0x00000000	MTP0_PAD_SIZE
0x000004b8	MTP0_PAD_VALUE	0x00000000	MTP0_PAD_VALUE
0x000004bc	MTP0_FP_PARAM	0x00000000	MTP0_FP_PARAM
0x000004c0	MTP0_IACT_W_STRIDE	0x00000000	MTP0_IACT_W_STRIDE
0x000004c4	MTP0_IACT_S_STRIDE	0x00000000	MTP0_IACT_S_STRIDE
0x000004c8	MTP0_IACT_TOTAL_STRIDE	0x00000000	MTP0_IACT_TOTAL_STRIDE
0x000004cc	MTP0_ACT_C_CTRL	0x00000000	MTP0_ACT_C_CTRL
0x000004d0	MTP0_ACT_W_CTRL	0x00000000	MTP0_ACT_W_CTRL
0x000004d4	MTP0_ACT_H_CTRL	0x00000000	MTP0_ACT_H_CTRL
0x000004d8	MTP0_WT_COMPRESS	0x00000000	MTP0_WT_COMPRESS
0x000004dc	MTP0_BATCH_MATMUL0	0x00000000	MTP0_BATCH_MATMUL0
0x000004e0	MTP0_BATCH_MATMUL1	0x00000000	MTP0_BATCH_MATMUL1
0x000004e4	MTP0_BATCH_MATMUL2	0x00000000	MTP0_BATCH_MATMUL2
0x000004e8	MTP0_CONV3D_CTRL	0x00000000	MTP0_CONV3D_CTRL
0x000004ec	MTP0_CONV3D_WT_STRIDE	0x00000000	MTP0_CONV3D_WT_STRIDE
0x00000600	MTP1_IACT_ADDR	0x00000000	MTP1_IACT_ADDR
0x00000604	MTP1_BATCH_MATMUL_IACT_ADDR	0x00000000	MTP1_BATCH_MATMUL_IACT_ADDR
0x00000608	MTP1_IACT_CTAG_ADDR	0x00000000	MTP1_IACT_CTAG_ADDR

Address	Name	Reset value	Description
0x0000060c	MTP1_Unb_ADDR	0x00000000	MTP1_Unb_ADDR
0x00000640	MTP1_WEIGHT_ADDR	0x00000000	MTP1_WEIGHT_ADDR
0x00000644	MTP1_PAD_ADDR	0x00000000	MTP1_PAD_ADDR
0x00000648	MTP1_IACT_FP_PARAM_ADDR0	0x00000000	MTP1_IACT_FP_PARAM_ADDR0
0x0000064c	MTP1_IACT_FP_PARAM_ADDR1	0x00000000	MTP1_IACT_FP_PARAM_ADDR1
0x00000680	MTP1_CTRL	0x00000000	MTP1_CTRL
0x00000684	MTP1_BE_CTRL	0x00000000	MTP1_BE_CTRL
0x00000688	MTP1_UNB_CTRL	0x00000000	MTP1_UNB_CTRL
0x0000068c	MTP1_KERNEL_CTRL	0x00000000	MTP1_KERNEL_CTRL
0x00000690	MTP1_WEIGHT_SPARSE	0x00000000	MTP1_WEIGHT_SPARSE
0x00000694	MTP1_WEIGHT_SIZE	0x00000000	MTP1_WEIGHT_SIZE
0x00000698	MTP1_W_STEP	0x00000000	MTP1_W_STEP
0x0000069c	MTP1_H_STEP	0x00000000	MTP1_H_STEP
0x000006a0	MTP1_BATCH_STRIDE	0x00000000	MTP1_BATCH_STRIDE
0x000006a4	MTP1_DECONV_PAD	0x00000000	MTP1_DECONV_PAD
0x000006a8	MTP1_IACT_CTAG_SURF_STRIDE	0x00000000	MTP1_IACT_CTAG_SURF_STRIDE
0x000006ac	MTP1_IACT_CTAG_BATCH_STRIDE	0x00000000	MTP1_IACT_CTAG_BATCH_STRIDE
0x000006b0	MTP1_IACT_CTRL	0x00000000	MTP1_IACT_CTRL
0x000006b4	MTP1_PAD_SIZE	0x00000000	MTP1_PAD_SIZE
0x000006b8	MTP1_PAD_VALUE	0x00000000	MTP1_PAD_VALUE
0x000006bc	MTP1_FP_PARAM	0x00000000	MTP1_FP_PARAM
0x000006c0	MTP1_IACT_W_STRIDE	0x00000000	MTP1_IACT_W_STRIDE
0x000006c4	MTP1_IACT_S_STRIDE	0x00000000	MTP1_IACT_S_STRIDE
0x000006c8	MTP1_IACT_TOTAL_STRIDE	0x00000000	MTP1_IACT_TOTAL_STRIDE
0x000006cc	MTP1_ACT_C_CTRL	0x00000000	MTP1_ACT_C_CTRL
0x000006d0	MTP1_ACT_W_CTRL	0x00000000	MTP1_ACT_W_CTRL
0x000006d4	MTP1_ACT_H_CTRL	0x00000000	MTP1_ACT_H_CTRL
0x000006d8	MTP1_WT_COMPRESS	0x00000000	MTP1_WT_COMPRESS
0x000006dc	MTP1_BATCH_MATMUL0	0x00000000	MTP1_BATCH_MATMUL0
0x000006e0	MTP1_BATCH_MATMUL1	0x00000000	MTP1_BATCH_MATMUL1
0x000006e4	MTP1_BATCH_MATMUL2	0x00000000	MTP1_BATCH_MATMUL2
0x000006e8	MTP1_CONV3D_CTRL	0x00000000	MTP1_CONV3D_CTRL
0x000006ec	MTP1_CONV3D_WT_STRIDE	0x00000000	MTP1_CONV3D_WT_STRIDE
0x00000800	ITP_ACC_INT_DST_MCFG0	0x00000000	ITP_ACC_INT_DST_MCFG0
0x00000804	ITP_ACC_DST_MCFG1	0x00000000	ITP_ACC_DST_MCFG1
0x00000808	ITP_INTP_MCFG	0x00000000	ITP_INTP_MCFG
0x00000840	ITP_LUT_MCFG	0x00000000	ITP_LUT_MCFG

Address	Name	Reset value	Description
0x00000880	ITP_MODE_CCFG	0x00000000	ITP_MODE_CCFG
0x00000884	ITP_UNB_ADDR_MCFG	0x00000000	ITP_UNB_ADDR_MCFG
0x00000888	ITP_LIN_INT_OCFG	0x00000000	ITP_LIN_INT_OCFG
0x0000088c	ITP_LIN_INT_CCFG0	0x00000000	ITP_LIN_INT_CCFG0
0x00000890	ITP_LIN_INT_CCFG1	0x00000000	ITP_LIN_INT_CCFG1
0x00000894	ITP_LIN_INT_START_OFFSET0	0x00000000	ITP_LIN_INT_START_OFFSET0
0x00000898	ITP_LIN_INT_START_OFFSET1	0x00000000	ITP_LIN_INT_START_OFFSET1
0x000008c0	ITP_LUT_DCFG0	0x00000000	ITP_LUT_DCFG0
0x000008c4	ITP_LUT_DCFG1	0x00000000	ITP_LUT_DCFG1
0x00000c00	ITPA_E_MUL_ACT_MCFG	0x00000000	ITPA_E_MUL_ACT_MCFG
0x00000c04	ITPA_E_ALU_ACT_MCFG	0x00000000	ITPA_E_ALU_ACT_MCFG
0x00000c40	ITPA_M0_ALU_MCFG	0x00000000	ITPA_M0_ALU_MCFG
0x00000c44	ITPA_M0_MUL_MCFG	0x00000000	ITPA_M0_MUL_MCFG
0x00000c48	ITPA_M1_ALU_MCFG	0x00000000	ITPA_M1_ALU_MCFG
0x00000c4c	ITPA_M1_MUL_MCFG	0x00000000	ITPA_M1_MUL_MCFG
0x00000c50	ITPA_E_MUL_PRM_MCFG	0x00000000	ITPA_E_MUL_PRM_MCFG
0x00000c54	ITPA_E_ALU_PRM_MCFG	0x00000000	ITPA_E_ALU_PRM_MCFG
0x00000c58	ITPA_E_MUL_FPOP_MCFG	0x00000000	ITPA_E_MUL_FPOP_MCFG
0x00000c5c	ITPA_E_ALU_FPOP_MCFG	0x00000000	ITPA_E_ALU_FPOP_MCFG
0x00000c60	ITPA_OCVT_BIAS_MCFG	0x00000000	ITPA_OCVT_BIAS_MCFG
0x00000c64	ITPA_OCVT_SCALE_MCFG	0x00000000	ITPA_OCVT_SCALE_MCFG
0x00000c68	ITPA_OCVT_TRSH_MCFG	0x00000000	ITPA_OCVT_TRSH_MCFG
0x00000c6c	ITPA_OFPSH_MCFG	0x00000000	ITPA_OFPSH_MCFG
0x00000c80	ITPA_M0_CCFG	0x00000000	ITPA_M0_CCFG
0x00000c84	ITPA_M0_ALU_PCFG	0x00000000	ITPA_M0_ALU_PCFG
0x00000c88	ITPA_M0_MUL_PCFG	0x00000000	ITPA_M0_MUL_PCFG
0x00000c8c	ITPA_M1_CCFG	0x00000000	ITPA_M1_CCFG
0x00000c90	ITPA_M1_ALU_PCFG	0x00000000	ITPA_M1_ALU_PCFG
0x00000c94	ITPA_M1_MUL_PCFG	0x00000000	ITPA_M1_MUL_PCFG
0x00000c98	ITPA_E_CCFG	0x00000000	ITPA_E_CCFG
0x00000c9c	ITPA_E_MUL_PCFG	0x00000000	ITPA_E_MUL_PCFG
0x00000ca0	ITPA_E_ALU_PCFG	0x00000000	ITPA_E_ALU_PCFG
0x00000ca4	ITPA_E_ALU_CLAMP_PCFG0	0x00000000	ITPA_E_ALU_CLAMP_PCFG0
0x00000ca8	ITPA_E_ALU_CLAMP_PCFG1	0x00000000	ITPA_E_ALU_CLAMP_PCFG1
0x00000cac	ITPA_E_MUL_PCVT_CCFG	0x0000000b	ITPA_E_MUL_PCVT_CCFG
0x00000cb0	ITPA_E_MUL_PCVT_PCFG	0x00000000	ITPA_E_MUL_PCVT_PCFG
0x00000cb4	ITPA_E_ALU_PCVT_CCFG	0x00000000	ITPA_E_ALU_PCVT_CCFG

Address	Name	Reset value	Description
0x00000cb8	ITPA_E_ALU_PCVT_PCFG	0x00000000	ITPA_E_ALU_PCVT_PCFG
0x00000cbc	ITPA_E_MUL_FP_PCFG	0x00000000	ITPA_E_MUL_FP_PCFG
0x00000cc0	ITPA_E_ALU_FP_PCFG	0x00000000	ITPA_E_ALU_FP_PCFG
0x00000cc4	ITPA_LUT_PCFG0	0x00000000	ITPA_LUT_PCFG0
0x00000cc8	ITPA_LUT_PCFG1	0x00000000	ITPA_LUT_PCFG1
0x00000ccc	ITPA_LUT_OCFG	0x00000000	ITPA_LUT_OCFG
0x00000cd0	ITPA_OCVT_ CFG	0x00000000	ITPA_OCVT_ CFG
0x00000cd4	ITPA_OCVT_SUB_CFG	0x00000000	ITPA_OCVT_SUB_CFG
0x00000cd8	ITPA_OCVT_MUL_CFG	0x00000000	ITPA_OCVT_MUL_CFG
0x00000cdc	ITPA_OCVT_ASYM_CFG	0x00000000	ITPA_OCVT_ASYM_CFG
0x00000ce0	ITPA_ACT_CCFG0	0x00000000	ITPA_ACT_CCFG0
0x00000ce4	ITPA_ACT_CCFG1	0x00000000	ITPA_ACT_CCFG1
0x00000ce8	ITPA_ACT_STEP_CCFG	0x00000000	ITPA_ACT_STEP_CCFG
0x00000cec	ITPA_E_MUL_SURF_STRIDE	0x00000000	ITPA_E_MUL_SURF_STRIDE
0x00000cf0	ITPA_E_MUL_TOTAL_STRIDE	0x00000000	ITPA_E_MUL_TOTAL_STRIDE
0x00000cf4	ITPA_E_MUL_WIDTH_STRIDE	0x00000000	ITPA_E_MUL_WIDTH_STRIDE
0x00000cf8	ITPA_E_MUL_BATCH_STRIDE	0x00000000	ITPA_E_MUL_BATCH_STRIDE
0x00000cfc	ITPA_E_ALU_SURF_STRIDE	0x00000000	ITPA_E_ALU_SURF_STRIDE
0x00000d00	ITPA_E_ALU_TOTAL_STRIDE	0x00000000	ITPA_E_ALU_TOTAL_STRIDE
0x00000d04	ITPA_E_ALU_WIDTH_STRIDE	0x00000000	ITPA_E_ALU_WIDTH_STRIDE
0x00000d08	ITPA_E_ALU_BATCH_STRIDE	0x00000000	ITPA_E_ALU_BATCH_STRIDE
0x00001000	ITPB_E_MUL_ACT_MCFG	0x00000000	ITPB_E_MUL_ACT_MCFG
0x00001004	ITPB_E_ALU_ACT_MCFG	0x00000000	ITPB_E_ALU_ACT_MCFG
0x00001040	ITPB_M0_ALU_MCFG	0x00000000	ITPB_M0_ALU_MCFG
0x00001044	ITPB_M0_MUL_MCFG	0x00000000	ITPB_M0_MUL_MCFG
0x00001048	ITPB_M1_ALU_MCFG	0x00000000	ITPB_M1_ALU_MCFG
0x0000104c	ITPB_M1_MUL_MCFG	0x00000000	ITPB_M1_MUL_MCFG
0x00001050	ITPB_E_MUL_PRM_MCFG	0x00000000	ITPB_E_MUL_PRM_MCFG
0x00001054	ITPB_E_ALU_PRM_MCFG	0x00000000	ITPB_E_ALU_PRM_MCFG
0x00001058	ITPB_E_MUL_FPOP_MCFG	0x00000000	ITPB_E_MUL_FPOP_MCFG
0x0000105c	ITPB_E_ALU_FPOP_MCFG	0x00000000	ITPB_E_ALU_FPOP_MCFG
0x00001060	ITPB_OCVT_BIAS_MCFG	0x00000000	ITPB_OCVT_BIAS_MCFG
0x00001064	ITPB_OCVT_SCALE_MCFG	0x00000000	ITPB_OCVT_SCALE_MCFG
0x00001068	ITPB_OCVT_TRSH_MCFG	0x00000000	ITPB_OCVT_TRSH_MCFG
0x0000106c	ITPB_OFPSH_MCFG	0x00000000	ITPB_OFPSH_MCFG
0x00001080	ITPB_M0_CCFG	0x00000000	ITPB_M0_CCFG
0x00001084	ITPB_M0_ALU_PCFG	0x00000000	ITPB_M0_ALU_PCFG

Address	Name	Reset value	Description
0x00001088	ITPB_M0_MUL_PCFG	0x00000000	ITPB_M0_MUL_PCFG
0x0000108c	ITPB_M1_CCFG	0x00000000	ITPB_M1_CCFG
0x00001090	ITPB_M1_ALU_PCFG	0x00000000	ITPB_M1_ALU_PCFG
0x00001094	ITPB_M1_MUL_PCFG	0x00000000	ITPB_M1_MUL_PCFG
0x00001098	ITPB_E_CCFG	0x00000000	ITPB_E_CCFG
0x0000109c	ITPB_E_MUL_PCFG	0x00000000	ITPB_E_MUL_PCFG
0x000010a0	ITPB_E_ALU_PCFG	0x00000000	ITPB_E_ALU_PCFG
0x000010a4	ITPB_E_ALU_CLAMP_PCFG0	0x00000000	ITPB_E_ALU_CLAMP_PCFG0
0x000010a8	ITPB_E_ALU_CLAMP_PCFG1	0x00000000	ITPB_E_ALU_CLAMP_PCFG1
0x000010ac	ITPB_E_MUL_PCVT_CCFG	0x0000000b	ITPB_E_MUL_PCVT_CCFG
0x000010b0	ITPB_E_MUL_PCVT_PCFG	0x00000000	ITPB_E_MUL_PCVT_PCFG
0x000010b4	ITPB_E_ALU_PCVT_CCFG	0x00000000	ITPB_E_ALU_PCVT_CCFG
0x000010b8	ITPB_E_ALU_PCVT_PCFG	0x00000000	ITPB_E_ALU_PCVT_PCFG
0x000010bc	ITPB_E_MUL_FP_PCFG	0x00000000	ITPB_E_MUL_FP_PCFG
0x000010c0	ITPB_E_ALU_FP_PCFG	0x00000000	ITPB_E_ALU_FP_PCFG
0x000010c4	ITPB_LUT_PCFG0	0x00000000	ITPB_LUT_PCFG0
0x000010c8	ITPB_LUT_PCFG1	0x00000000	ITPB_LUT_PCFG1
0x000010cc	ITPB_LUT_OCFG	0x00000000	ITPB_LUT_OCFG
0x000010d0	ITPB_OCVT_ CFG	0x00000000	ITPB_OCVT_ CFG
0x000010d4	ITPB_OCVT_SUB_CFG	0x00000000	ITPB_OCVT_SUB_CFG
0x000010d8	ITPB_OCVT_MUL_CFG	0x00000000	ITPB_OCVT_MUL_CFG
0x000010dc	ITPB_OCVT_ASYM_CFG	0x00000000	ITPB_OCVT_ASYM_CFG
0x000010e0	ITPB_ACT_CCFG0	0x00000000	ITPB_ACT_CCFG0
0x000010e4	ITPB_ACT_CCFG1	0x00000000	ITPB_ACT_CCFG1
0x000010e8	ITPB_ACT_STEP_CCFG	0x00000000	ITPB_ACT_STEP_CCFG
0x000010ec	ITPB_E_MUL_SURF_STRIDE	0x00000000	ITPB_E_MUL_SURF_STRIDE
0x000010f0	ITPB_E_MUL_TOTAL_STRIDE	0x00000000	ITPB_E_MUL_TOTAL_STRIDE
0x000010f4	ITPB_E_MUL_WIDTH_STRIDE	0x00000000	ITPB_E_MUL_WIDTH_STRIDE
0x000010f8	ITPB_E_MUL_BATCH_STRIDE	0x00000000	ITPB_E_MUL_BATCH_STRIDE
0x000010fc	ITPB_E_ALU_SURF_STRIDE	0x00000000	ITPB_E_ALU_SURF_STRIDE
0x00001100	ITPB_E_ALU_TOTAL_STRIDE	0x00000000	ITPB_E_ALU_TOTAL_STRIDE
0x00001104	ITPB_E_ALU_WIDTH_STRIDE	0x00000000	ITPB_E_ALU_WIDTH_STRIDE
0x00001108	ITPB_E_ALU_BATCH_STRIDE	0x00000000	ITPB_E_ALU_BATCH_STRIDE
0x00001400	ITPC_E_MUL_ACT_MCFG	0x00000000	ITPC_E_MUL_ACT_MCFG
0x00001404	ITPC_E_ALU_ACT_MCFG	0x00000000	ITPC_E_ALU_ACT_MCFG
0x00001440	ITPC_M0_ALU_MCFG	0x00000000	ITPC_M0_ALU_MCFG
0x00001444	ITPC_M0_MUL_MCFG	0x00000000	ITPC_M0_MUL_MCFG

Address	Name	Reset value	Description
0x00001448	ITPC_M1_ALU_MCFG	0x00000000	ITPC_M1_ALU_MCFG
0x0000144c	ITPC_M1_MUL_MCFG	0x00000000	ITPC_M1_MUL_MCFG
0x00001450	ITPC_E_MUL_PRM_MCFG	0x00000000	ITPC_E_MUL_PRM_MCFG
0x00001454	ITPC_E_ALU_PRM_MCFG	0x00000000	ITPC_E_ALU_PRM_MCFG
0x00001458	ITPC_E_MUL_FPOP_MCFG	0x00000000	ITPC_E_MUL_FPOP_MCFG
0x0000145c	ITPC_E_ALU_FPOP_MCFG	0x00000000	ITPC_E_ALU_FPOP_MCFG
0x00001460	ITPC_OCVT_BIAS_MCFG	0x00000000	ITPC_OCVT_BIAS_MCFG
0x00001464	ITPC_OCVT_SCALE_MCFG	0x00000000	ITPC_OCVT_SCALE_MCFG
0x00001468	ITPC_OCVT_TRSH_MCFG	0x00000000	ITPC_OCVT_TRSH_MCFG
0x0000146c	ITPC_OFPSH_MCFG	0x00000000	ITPC_OFPSH_MCFG
0x00001480	ITPC_M0_CCFG	0x00000000	ITPC_M0_CCFG
0x00001484	ITPC_M0_ALU_PCFG	0x00000000	ITPC_M0_ALU_PCFG
0x00001488	ITPC_M0_MUL_PCFG	0x00000000	ITPC_M0_MUL_PCFG
0x0000148c	ITPC_M1_CCFG	0x00000000	ITPC_M1_CCFG
0x00001490	ITPC_M1_ALU_PCFG	0x00000000	ITPC_M1_ALU_PCFG
0x00001494	ITPC_M1_MUL_PCFG	0x00000000	ITPC_M1_MUL_PCFG
0x00001498	ITPC_E_CCFG	0x00000000	ITPC_E_CCFG
0x0000149c	ITPC_E_MUL_PCFG	0x00000000	ITPC_E_MUL_PCFG
0x000014a0	ITPC_E_ALU_PCFG	0x00000000	ITPC_E_ALU_PCFG
0x000014a4	ITPC_E_ALU_CLAMP_PCFG0	0x00000000	ITPC_E_ALU_CLAMP_PCFG0
0x000014a8	ITPC_E_ALU_CLAMP_PCFG1	0x00000000	ITPC_E_ALU_CLAMP_PCFG1
0x000014ac	ITPC_E_MUL_PCVT_CCFG	0x0000000b	ITPC_E_MUL_PCVT_CCFG
0x000014b0	ITPC_E_MUL_PCVT_PCFG	0x00000000	ITPC_E_MUL_PCVT_PCFG
0x000014b4	ITPC_E_ALU_PCVT_CCFG	0x00000000	ITPC_E_ALU_PCVT_CCFG
0x000014b8	ITPC_E_ALU_PCVT_PCFG	0x00000000	ITPC_E_ALU_PCVT_PCFG
0x000014bc	ITPC_E_MUL_FP_PCFG	0x00000000	ITPC_E_MUL_FP_PCFG
0x000014c0	ITPC_E_ALU_FP_PCFG	0x00000000	ITPC_E_ALU_FP_PCFG
0x000014c4	ITPC_LUT_PCFG0	0x00000000	ITPC_LUT_PCFG0
0x000014c8	ITPC_LUT_PCFG1	0x00000000	ITPC_LUT_PCFG1
0x000014cc	ITPC_LUT_OCFG	0x00000000	ITPC_LUT_OCFG
0x000014d0	ITPC_OCVT_ CFG	0x00000000	ITPC_OCVT_ CFG
0x000014d4	ITPC_OCVT_SUB_CFG	0x00000000	ITPC_OCVT_SUB_CFG
0x000014d8	ITPC_OCVT_MUL_CFG	0x00000000	ITPC_OCVT_MUL_CFG
0x000014dc	ITPC_OCVT_ASYM_CFG	0x00000000	ITPC_OCVT_ASYM_CFG
0x000014e0	ITPC_ACT_CCFG0	0x00000000	ITPC_ACT_CCFG0
0x000014e4	ITPC_ACT_CCFG1	0x00000000	ITPC_ACT_CCFG1
0x000014e8	ITPC_ACT_STEP_CCFG	0x00000000	ITPC_ACT_STEP_CCFG

Address	Name	Reset value	Description
0x000014ec	ITPC_E_MUL_SURF_STRIDE	0x00000000	ITPC_E_MUL_SURF_STRIDE
0x000014f0	ITPC_E_MUL_TOTAL_STRIDE	0x00000000	ITPC_E_MUL_TOTAL_STRIDE
0x000014f4	ITPC_E_MUL_WIDTH_STRIDE	0x00000000	ITPC_E_MUL_WIDTH_STRIDE
0x000014f8	ITPC_E_MUL_BATCH_STRIDE	0x00000000	ITPC_E_MUL_BATCH_STRIDE
0x000014fc	ITPC_E_ALU_SURF_STRIDE	0x00000000	ITPC_E_ALU_SURF_STRIDE
0x00001500	ITPC_E_ALU_TOTAL_STRIDE	0x00000000	ITPC_E_ALU_TOTAL_STRIDE
0x00001504	ITPC_E_ALU_WIDTH_STRIDE	0x00000000	ITPC_E_ALU_WIDTH_STRIDE
0x00001508	ITPC_E_ALU_BATCH_STRIDE	0x00000000	ITPC_E_ALU_BATCH_STRIDE
0x00001800	PTP_IACT_ADDR(PTP Input Activation Address Register)	0x00000000	PTP_IACT_ADDR(PTP Input Activation Address Register)
0x00001804	PTP_CTAG_ADDR(PTP Input Activation Compression TAG Register)	0x00000000	PTP_CTAG_ADDR(PTP Input Activation Compression TAG Register)
0x00001808	PTP_ROIP_DESP_ADDR (PTP ROI Pooling Descriptor Address Register)	0x00000000	PTP_ROIP_DESP_ADDR (PTP ROI Pooling Descriptor Address Register)
0x00001840	PTP_PAD_ADDR (PTP Pad Memory Address Register)	0x00000000	PTP_PAD_ADDR (PTP Pad Memory Address Register)
0x00001844	PTP_WEIGHT_ADDR (PTP Weight Memory Address Register)	0x00000000	PTP_WEIGHT_ADDR (PTP Weight Memory Address Register)
0x00001848	PTP_BIAS_ADDR (PTP BIAS Memory Address Register)	0x00000000	PTP_BIAS_ADDR (PTP BIAS Memory Address Register)
0x0000184c	PTP_SCALE_ADDR (PTP Scale Memory Address Register)	0x00000000	PTP_SCALE_ADDR (PTP Scale Memory Address Register)
0x00001850	PTP_SHIFT_ADDR (PTP Shift Memory Address Register)	0x00000000	PTP_SHIFT_ADDR (PTP Shift Memory Address Register)
0x00001854	PTP_IACT_FP_PARAM_ADDR (PTP Input Activation Float Point Conversion Parameter Address Register)	0x00000000	PTP_IACT_FP_PARAM_ADDR (PTP Input Activation Float Point Conversion Parameter Address Register)
0x00001858	PTP_OACT_FP_PARAM_ADDR (PTP Output Activation Float Point Conversion Parameter Address Register)	0x00000000	PTP_OACT_FP_PARAM_ADDR (PTP Output Activation Float Point Conversion Parameter Address Register)
0x00001880	PTP_MODE (PTP Mode Control Register)	0x00000000	PTP_MODE (PTP Mode Control Register)
0x00001884	PTP_KERNEL (PTP Kernel Control Register)	0x00000000	PTP_KERNEL (PTP Kernel Control Register)
0x00001888	PTP_PAD_SIZE (PTP Padding Size Register)	0x00000000	PTP_PAD_SIZE (PTP Padding Size Register)
0x0000188c	PTP_PAD_VALUE (PTP Padding Value Register)	0x00000000	PTP_PAD_VALUE (PTP Padding Value Register)
0x00001890	PTP_BIAS_CTRL (PTP Bias Control Register)	0x00000000	PTP_BIAS_CTRL (PTP Bias Control Register)
0x00001894	PTP_BIAS_VALUE (PTP Bias VALUE Register)	0x00000000	PTP_BIAS_VALUE (PTP Bias VALUE Register)
0x00001898	PTP_SCALE_CTRL (PTP Scale Control Register)	0x00000000	PTP_SCALE_CTRL (PTP Scale Control Register)

Address	Name	Reset value	Description
0x0000189c	PTP_ASYM_VALUE(PTP Asymmetric Value Register)	0x00000000	PTP_ASYM_VALUE(PTP Asymmetric Value Register)
0x000018a0	PTP_FP_PARAM(PTP Float Point Parameter Register)	0x00000000	PTP_FP_PARAM(PTP Float Point Parameter Register)
0x000018a4	PTP_W_STEP (PTP Width Step Register)	0x00000000	PTP_W_STEP (PTP Width Step Register)
0x000018a8	PTP_H_STEP (PTP Height Step Register)	0x00000000	PTP_H_STEP (PTP Height Step Register)
0x000018ac	PTP_STEP_OUT (PTP Step Out Register)	0x00000000	PTP_STEP_OUT (PTP Step Out Register)
0x000018b0	PTP_C_STEP (PTP Channel Step Register)	0x00000000	PTP_C_STEP (PTP Channel Step Register)
0x000018b4	PTP_IACT_CTRL(PTP Input Activation Control Register)	0x00000000	PTP_IACT_CTRL(PTP Input Activation Control Register)
0x000018b8	PTP_WEIGHT_SPARSE (PTP Weight Sparse Register)	0x00000000	PTP_WEIGHT_SPARSE (PTP Weight Sparse Register)
0x000018bc	PTP_ACT_C_CTRL (PTP Activation Channel Control Register)	0x00000000	PTP_ACT_C_CTRL (PTP Activation Channel Control Register)
0x000018c0	PTP_ACT_W_CTRL (PTP Activation Width Control Register)	0x00000000	PTP_ACT_W_CTRL (PTP Activation Width Control Register)
0x000018c4	PTP_ACT_H_CTRL (PTP Activation Height Control Register)	0x00000000	PTP_ACT_H_CTRL (PTP Activation Height Control Register)
0x000018c8	PTP_PAD_UnB_ADDR (PTP Pad Unb Address Register)	0x00000000	PTP_PAD_UnB_ADDR (PTP Pad Unb Address Register)
0x000018cc	PTP_WEIGHT_UnB_ADDR (PTP Weight UnB Address Register)	0x00000000	PTP_WEIGHT_UnB_ADDR (PTP Weight UnB Address Register)
0x000018d0	PTP_BIAS_UnB_ADDR (PTP Bias UnB Address Register)	0x00000000	PTP_BIAS_UnB_ADDR (PTP Bias UnB Address Register)
0x000018d4	PTP_SCALE_UnB_ADDR (PTP Scale UnB Address Register)	0x00000000	PTP_SCALE_UnB_ADDR (PTP Scale UnB Address Register)
0x000018d8	PTP_FP_PARAM_UnB_ADDR(PTP Float Point Parameter UnB Address Register)	0x00000000	PTP_FP_PARAM_UnB_ADDR(PTP Float Point Parameter UnB Address Register)
0x000018dc	PTP_ROIP_UnB_ADDR (PTP ROI Pooling Descriptor UnB Address Register)	0x00000000	PTP_ROIP_UnB_ADDR (PTP ROI Pooling Descriptor UnB Address Register)
0x000018e0	PTP_IACT_W_STRIDE (PTP Input Activation Width Stride Register)	0x00000000	PTP_IACT_W_STRIDE (PTP Input Activation Width Stride Register)
0x000018e4	PTP_IACT_SURF_STRIDE (PTP Input Activation Surface Stride Register)	0x00000000	PTP_IACT_SURF_STRIDE (PTP Input Activation Surface Stride Register)
0x000018e8	PTP_IACT_TOTAL_STRIDE (PTP Input Activation Total Stride Register)	0x00000000	PTP_IACT_TOTAL_STRIDE (PTP Input Activation Total Stride Register)
0x000018ec	PTP_IACT_BATCH_STRIDE (PTP Input Activation Batch Stride Register)	0x00000000	PTP_IACT_BATCH_STRIDE (PTP Input Activation Batch Stride Register)
0x000018f0	PTP_IACT_CTAG_SURF_STRIDE (PTP Input Activation Compression TAG Surface Stride Register)	0x00000000	PTP_IACT_CTAG_SURF_STRIDE (PTP Input Activation Compression TAG Surface Stride Register)
0x000018f4	PTP_IACT_CTAG_BATCH_STRIDE (PTP Input Activation Compression TAG Batch Stride Register)	0x00000000	PTP_IACT_CTAG_BATCH_STRIDE (PTP Input Activation Compression TAG Batch Stride Register)

Table A-27 MMR Registers

Address	Name	Reset value	Description
0xee000000	Cluster MIF Timeout Control	0x00000100	Cluster MIF Timeout Control Register
0xfe006000	Core MIF Transaction Counter Control	0x00000000	Core MIF Transaction Counter Control Register
0xfe006004	WRCNT_Status	0x00000000	WRCNT_Status
0xfe006010	RREQ_CNT	0x00000000	RREQ_CNT
0xfe006014	RDATA_CNT	0x00000000	RDATA_CNT
0xfe006018	WREQ_CNT	0x00000000	WREQ_CNT
0xfe00601c	WDATA_CNT	0x00000000	WDATA_CNT
0xfe004000	DEBUG_COM_DATA	0x00000000	DEBUG_COM_DATA Register
0xfe004400	Core IFU Fault Status	0x00000000	Core IFU Fault Status Register
0xfe004404	Core IFU First Fault Address	0x00000000	Core IFU First Fault Address Register
0xfe004800	Core Data Cache Fault Status	0x00000000	Core Data Cache Fault Status Register
0xfe004804	Core Data Cache First Fault Status	0x00000000	Core Data Cache First Fault Status Register
0xfe004c00	Core Share Memory Fault Status	0x00000000	Core Share Memory Fault Status Register
0xfe004c04	Core Share Memory First Fault Address	0x00000000	Core Share Memory First Fault Address Register