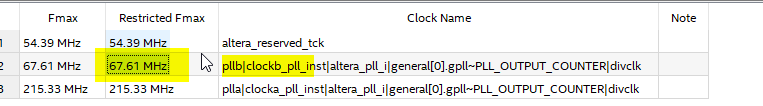
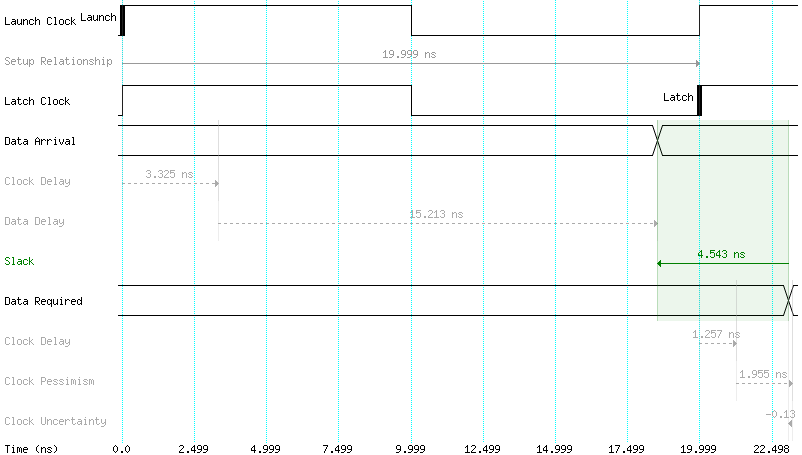
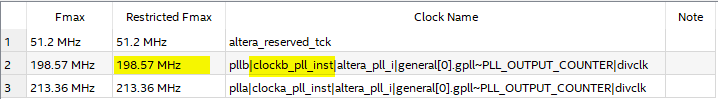
# Block Diagram:

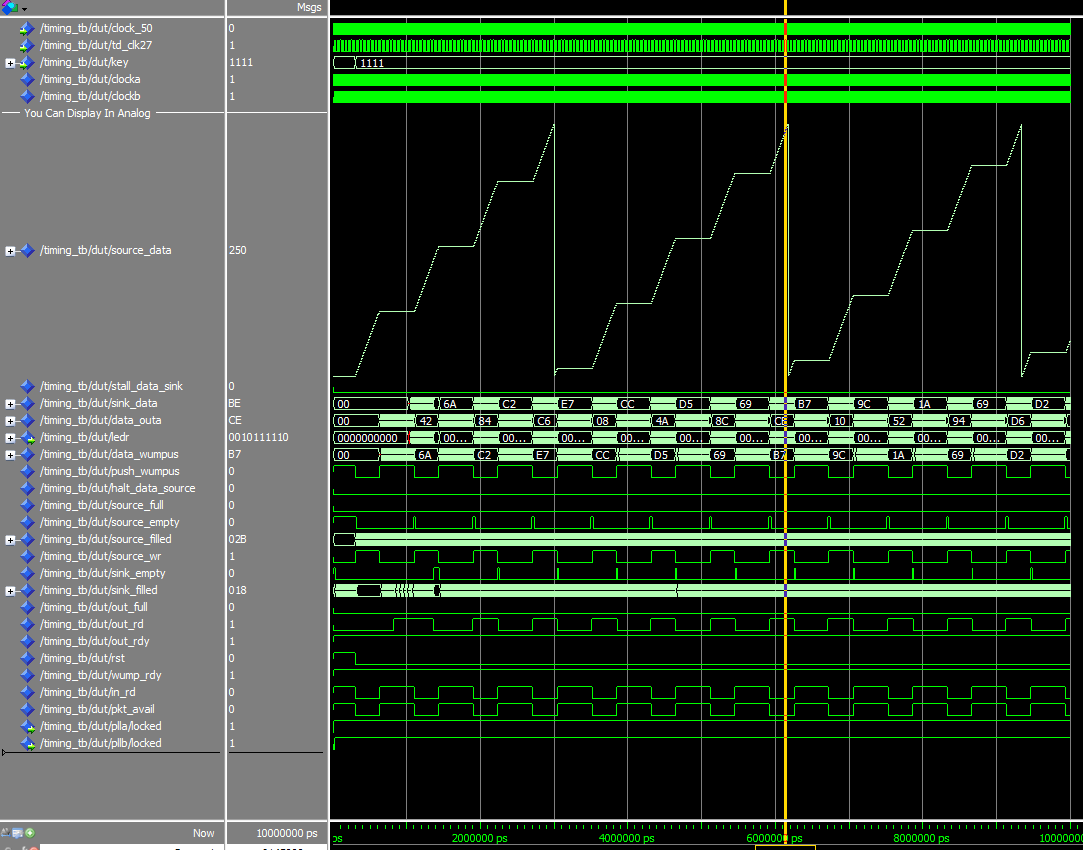
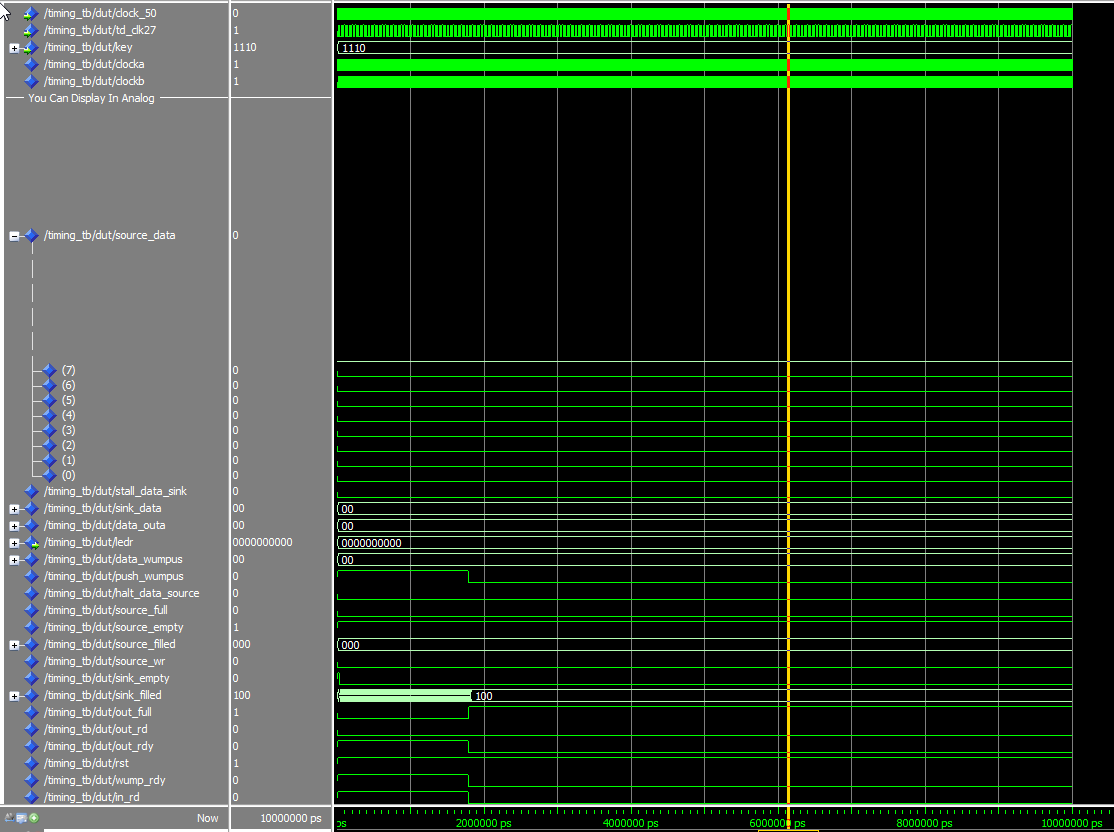
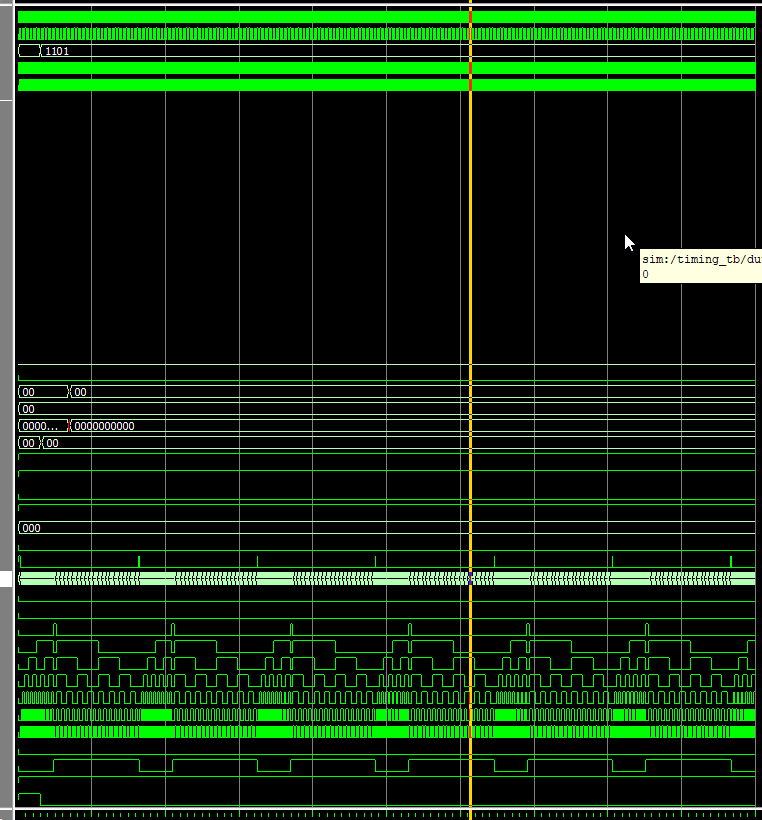
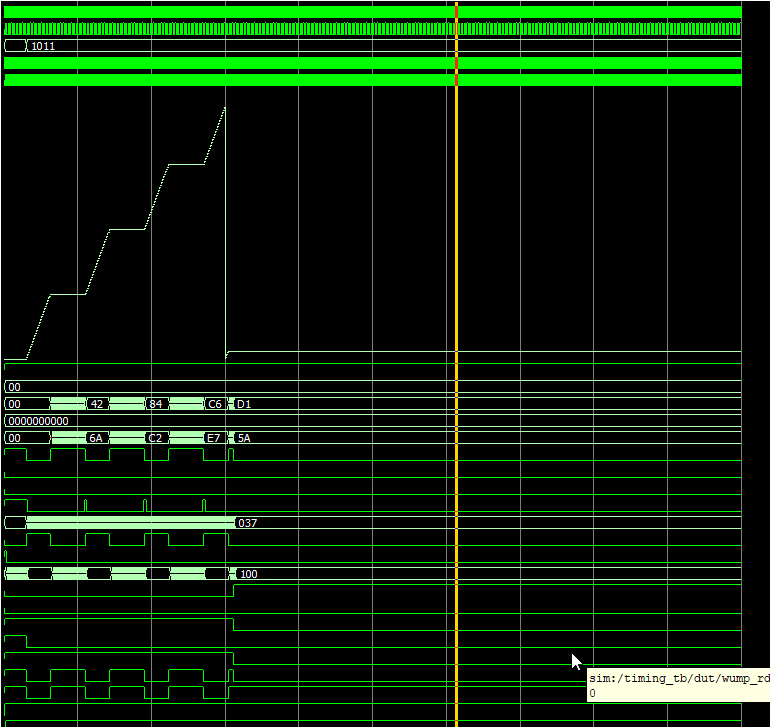
# Observe the timing analysis in Quartus/Timequest.

* 1. What is the Fmax that will fix the clock B violations: 67.61 MHz



* 1. Changing clock B output frequency to 50kHz leaves 4.543ns between the retrieval and the required latch. Timing is OK.  
     
  2. Timing after adding pipeline shifters: New Restricted Fmax: 198.57Hz  
     

# ModelSim Analysis

1. The following diagrams show the simulated timing behavior.
   1. Unhalted key(0)  
      
   2. Halted key(0)  
        
      Above: When key(0) is halted the data sink fills but the clock is off so the data doesn’t move through any of the frazzles.
   3. Halt key(1)  
        
      Here the clock runs but the data source is halted, resulting in a 0 output.
   4. Halt key(2)  
        
      Here, we see the sink fills but it does not clear resulting in 1 cycle of clear output after which the system halts.