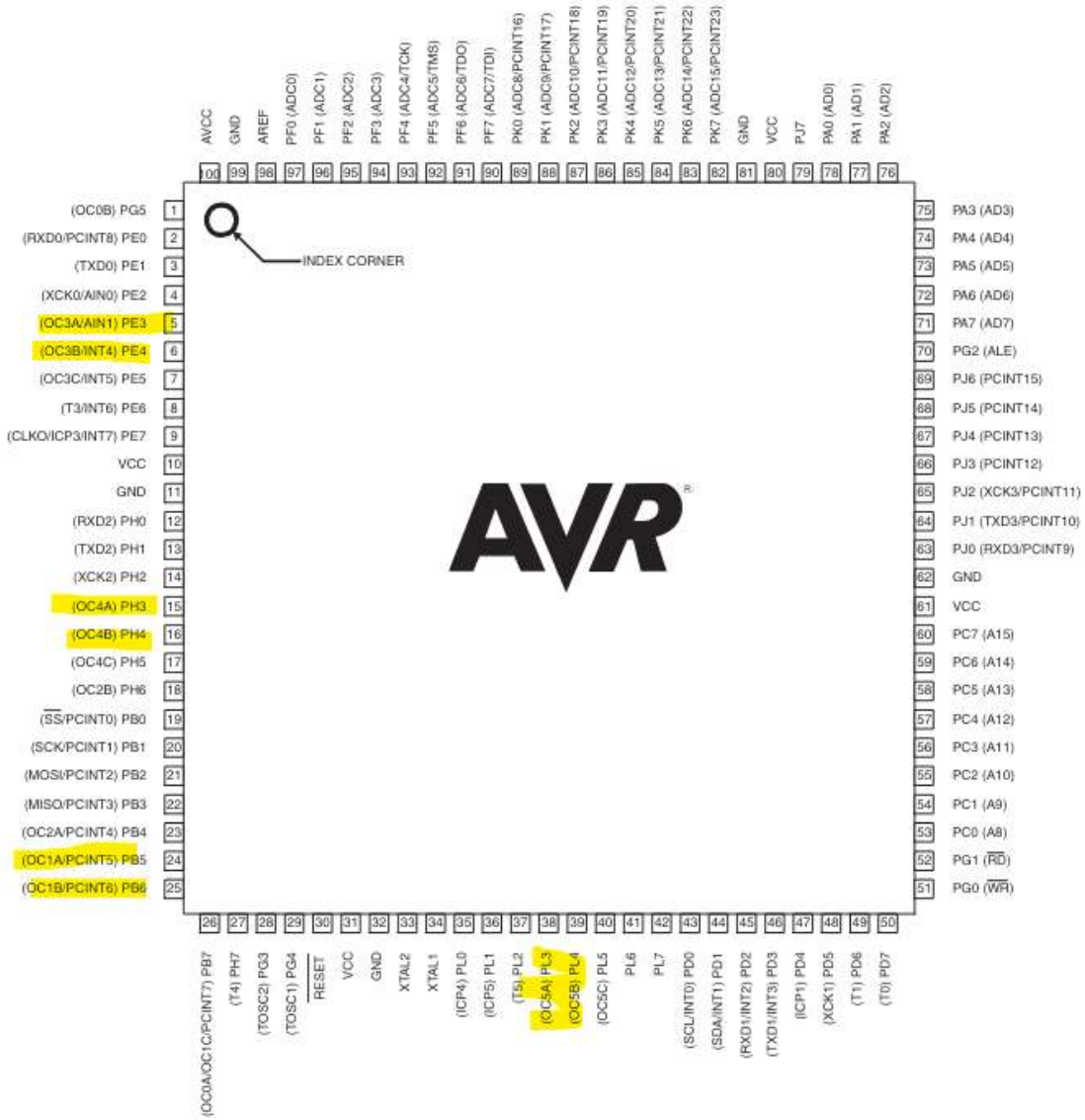
핀번호 탐색



clock

16MHz (62.5ns)

Flash(보조기억)

256K

EEPROM 크기(비휘발)

4K

SRAM 크기(메모리)

8K

Waveform Generation Mode Bit

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation	TOP	Update of OCRnx at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICRn	BOTTOM	BOTTOM
9	1	0	0	1	PWM,Phase and Frequency Correct	OCRnA	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICRn	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCRnA	TOP	BOTTOM
12	1	1	0	0	CTC	ICRn	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICRn	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

Timer/Counter Mode of Operation

어떤 종류의 PWM 사용할 것인지

TOP (MAX)

clock을 어디까지 오르게 할 것인지

Update of OCRnX at (synchronize)

OCRnx의 갱신 시기

(p.118)(p.142)

OCR 레지스터에서 주의할 점은 이중 버퍼 구조로 되어 있어서 사용자가 동작 중에 값을 수정한다 하더라도 바로 바뀌지 않고 TOP혹은 BOTTOM에 도달했을 때 변경된다.

OCRnA=100;

이 문장이 실행될 때 OCR0가 100으로 바뀌는 것이 아니라, 잠시 임시레지스터에 저장된 후 TCNT0이 255->0으로 바뀔 때 100을 넣어준다.

TOVn Flag Set on

인터럽트 발생 시기

TIMSK (p.161)

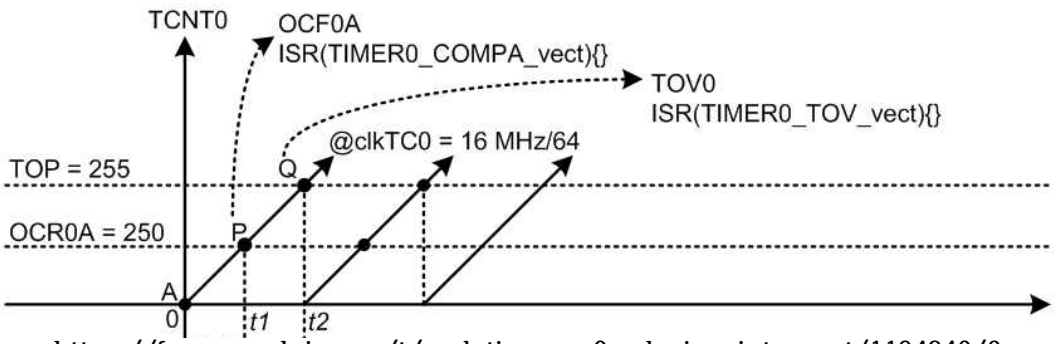
Timer/Counter 1 Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0	
(0x6F)	–	–	ICIE1	–	OCIE1C	OCIE1B	OCIE1A	TOIE1	TIMSK1
Read/Write	R	R	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Timer/Countern, Input Capture Interrupt Enable
(입력 핀 따로 있음)

Timer/Countern, Output Compare (N) Match Interrupt Enable
(사용하기에 힘들 듯)

Timer/Countern, Overflow Interrupt Enable



https://forum.arduino.cc/t/updating-ocr0a-during-interrupt/1194846/6

TCCRnA (p.154)

(Timer/Counter Control Register)

Bit	7	6	5	4	3	2	1	0	
(0x80)	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

COMnA1 COMnB1 COMnC1	COMnA0 COMnB0 COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected
0	1	WGM13:0 =9 or 11: Toggle OC1A on Compare Match, OC1B and OC1C disconnected (normal port operation). For all other WGM1 settings, normal port operation, OC1A/OC1B/OC1C disconnected
1	0	Clear OCnA/OCnB/OCnC on compare match when up-counting Set OCnA/OCnB/OCnC on compare match when downcounting
1	1	Set OCnA/OCnB/OCnC on compare match when up-counting Clear OCnA/OCnB/OCnC on compare match when downcounting

COMnA: 1 0 ->
삼각파 상승시 사인파와 만나면 ON
삼각파 하강시 사인파와 만나면 OFF

COMnA: 1 1->
삼각파 상승시 사인파와 만나면 OFF
삼각파 하강시 사인파와 만나면 ON

OCnA, OCnB, OCnC로 서로 다른 펄스 출력 가능

Waveform Generation Mode

TCCRnB (p.156)

(Timer/Counter Control Register

Bit	7	6	5	4	3	2	1	0	
(0x81)	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Input Capture Noise Canceler

Input Capture Edge Select

Waveform Generation Mode

Clock Select Bit Description(p.178)

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/1 (No prescaling
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

$$f_{OCnxPCPWM} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot TOP}$$

TCCR1C 생략

p.134

16-bit Timer/Counter Block Diagram

전체 동작은 이렇게 동작한다.

Register Description for I/O-Ports

DDRN(p.96)

Data Direction Register (A)

Bit	7	6	5	4	3	2	1	0	
0x01 (0x21)	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

출력 핀 설정

p.101

Reset and Interrupt Vectors Handling

ISR(...)

TCCR2x는 다름(p.182)

ctc는 double buffer disable임

double buffer disable 불가능하면 힘들 것으로 보임.