Data Formatter Firmware Design Note

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Abstract

1 Introduction

This describes the design of the Data Formatter Firmware. The documentation is for GitHub revision of `data_formatter_firmware-00-00-03`. This version of firmware is developed from `data_formatter_firmware-00-00-02` branch. All the needed details can be found in the `DF_Design_V00-00-03-branch.xlsx`, too.

2 Changes of this version of FW

This version of FW includes the following significant changes:

1. Implementation of IM-DF block transfer
2. Implementation of automatic FMC delay value setting
3. Bug fix for SPY buffer inconsistent readout
4. Bug fix for AUX-DF slink communication (AUX idle words as pad words, partially done)
5. Addition of registers to read out fmc fifo fullness, fmc fifo number of words writte, FW version and etc.
6. Addition of SLINK output for SSB and implementation of QSFP link for inter-crate DF communication and DF-SSB communication
7. Addition of the functionality to change IP address for FW through IPBus

3 32 board allocation and numbering

Table 1, 2, 3 and 4 show DF boards allocation and numbering in USA 15.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination	
		Shelf	Slot	Tower ID	Position	Tower ID	Position	Link 1	Link 2
0	0x00000001	1	3	2	C E phi1	3	C E phi2	Shelf 4 - Slot 7	Shelf 2 - Slot 7
4	0x00000010	1	4	18	C B phi1	19	C B phi2	Shelf 4 - Slot 8	Shelf 2 - Slot 8
8	0x00000100	1	5	34	A B phi1	35	A B phi2	Shelf 4 - Slot 9	Shelf 2 - Slot 9
12	0x00001000	1	6	50	A E phi1	51	A E phi2	Shelf 4 - Slot 10	Shelf 2 - Slot 10
16	0x00010000	1	7	4	C E phi3	5	C E phi4	Shelf 4 - Slot 3	Shelf 2 - Slot 3
20	0x00100000	1	8	20	C B phi3	21	C B phi4	Shelf 4 - Slot 4	Shelf 2 - Slot 4
24	0x01000000	1	9	36	A B phi3	37	A B phi4	Shelf 4 - Slot 5	Shelf 2 - Slot 5
28	0x10000000	1	10	52	A E phi3	53	A E phi4	Shelf 4 - Slot 6	Shelf 2 - Slot 6

Table 1: Shelf 1.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination	
		Shelf	Slot	Tower ID	Position	Tower ID	Position	Link 1	Link 2
1	0x00000002	2	3	6	C E phi5	7	C E phi6	Shelf 1 - Slot 7	Shelf 3 - Slot 7
5	0x00000020	2	4	22	C B phi5	23	C B phi6	Shelf 1 - Slot 8	Shelf 3 - Slot 8
9	0x00000200	2	5	38	A B phi5	39	A B phi6	Shelf 1 - Slot 9	Shelf 3 - Slot 9
13	0x00002000	2	6	54	A E phi5	55	A E phi6	Shelf 1 - Slot 10	Shelf 3 - Slot 10
17	0x00020000	2	7	8	C E phi7	9	C E phi8	Shelf 1 - Slot 3	Shelf 3 - Slot 3
21	0x00200000	2	8	24	C B phi7	25	C B phi8	Shelf 1 - Slot 4	Shelf 3 - Slot 4
25	0x02000000	2	9	40	A B phi7	41	A B phi8	Shelf 1 - Slot 5	Shelf 3 - Slot 5
29	0x20000000	2	10	53	A E phi7	54	A E phi8	Shelf 1 - Slot 6	Shelf 3 - Slot 6

Table 2: Shelf 2.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination	
		Shelf	Slot	Tower ID	Position	Tower ID	Position	Link 1	Link 2
2	0x00000004	3	3	10	C E phi9	11	C E phi10	Shelf 2 - Slot 7	Shelf 4 - Slot 7
6	0x00000040	3	4	26	C B phi9	27	C B phi10	Shelf 2 - Slot 8	Shelf 4 - Slot 8
10	0x00000400	3	5	42	A B phi9	43	A B phi10	Shelf 2 - Slot 9	Shelf 4 - Slot 9
14	0x00004000	3	6	58	A E phi9	59	A E phi10	Shelf 2 - Slot 10	Shelf 4 - Slot 10
18	0x00040000	3	7	12	C E phi11	13	C E phi12	Shelf 2 - Slot 3	Shelf 4 - Slot 3
22	0x00400000	3	8	28	C B phi11	29	C B phi12	Shelf 2 - Slot 4	Shelf 4 - Slot 4
26	0x04000000	3	9	44	A B phi11	45	A B phi12	Shelf 2 - Slot 5	Shelf 4 - Slot 5
30	0x40000000	3	10	60	A E phi11	61	A E phi12	Shelf 2 - Slot 6	Shelf 4 - Slot 6

Table 3: Shelf 3.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination	
		Shelf	Slot	Tower ID	Position	Tower ID	Position	Link 1	Link 2
3	0x00000008	4	3	14	C E phi13	15	C E phi14	Shelf 3 - Slot 7	Shelf 1 - Slot 7
7	0x00000080	4	4	30	C B phi13	31	C B phi14	Shelf 3 - Slot 8	Shelf 1 - Slot 8
11	0x00000800	4	5	46	A B phi13	47	A B phi14	Shelf 3 - Slot 9	Shelf 1 - Slot 9
15	0x00008000	4	6	62	A E phi13	63	A E phi14	Shelf 3 - Slot 10	Shelf 1 - Slot 10
20	0x00080000	4	7	0	C E phi15	1	C E phi0	Shelf 3 - Slot 3	Shelf 1 - Slot 3
24	0x00800000	4	8	16	C B phi15	17	C B phi0	Shelf 3 - Slot 4	Shelf 1 - Slot 4
27	0x08000000	4	9	32	A B phi15	33	A B phi0	Shelf 3 - Slot 5	Shelf 1 - Slot 5
31	0x80000000	4	10	48	A E phi15	49	A E phi0	Shelf 3 - Slot 6	Shelf 1 - Slot 6

Table 4: Shelf 4.

4 Overview of the firmware

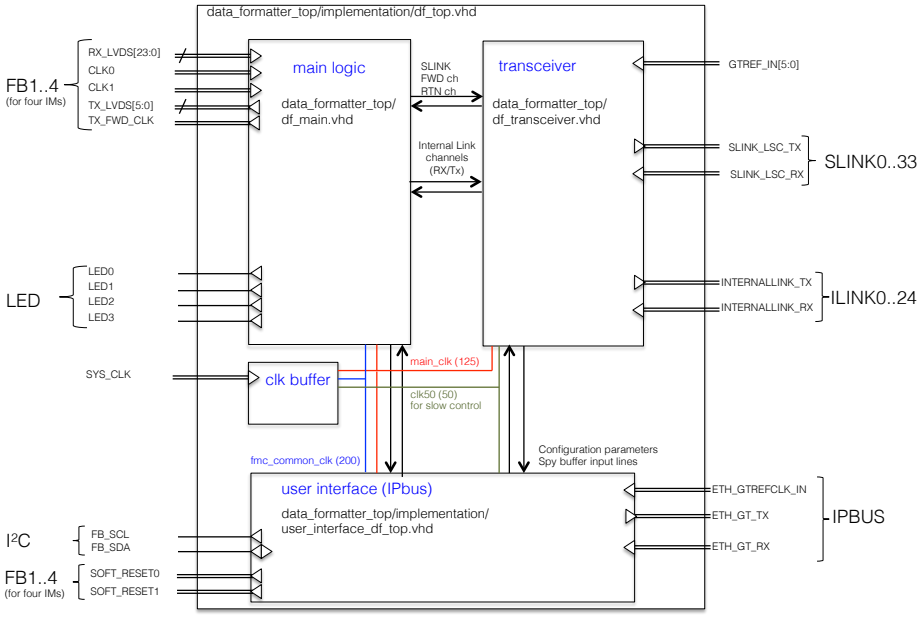

Figure 1: Firmware overview.

5 Main logic

- FMC interface : `data_formatter_top/df_fmc_interface.vhd`
- Input data operator : `data_formatter_top/df_input_data_operator.vhd`
- Output data operator : `data_formatter_top/df_output_data_operator_v2.vhd`
- Internal Link input : `data_formatter_top/df_internallink_input.vhd`
- Internal Link input : `data_formatter_top/df_internallink_output.vhd`

5.1 FMC interface

- Input mapper : `pulsar2_fmc_interface/fmc_rx_mapper_fmc_to_fpga.vhd`
- Front : `pulsar2_fmc_interface/fmc_rx_front.vhd`
- Mapper : `pulsar2_fmc_interface/fmc_rx_mapper_fpga_to_detword.vhd`
- Parity checker : `pulsar2_fmc_interface/fmc_rx_parity.vhd`
- Frame : `pulsar2_fmc_interface/fmc_rx_frame.vhd`
- Pattern checker : `pulsar2_fmc_interface/fmc_rx_data_checker_v3.vhd`
- Elasitc buffer : `fmc_input_buffer/fmc_input_buffer.vhd`

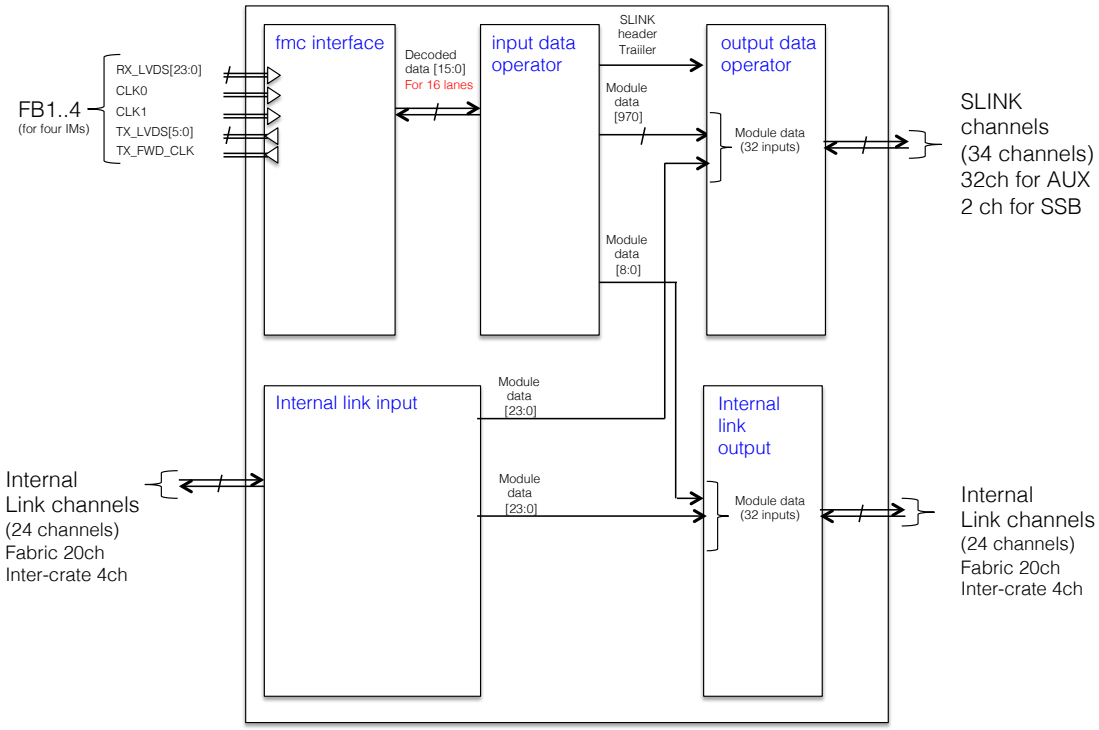

Figure 2: Main logic overview.

- FMC TX interface : `pulsar2_fmc_interface/fmc_tx_interface.vhd`

5.2 Input data operator

- Input lane handler : `pulsar2_df_internal_decoder/df_input_handler.vhd`
- Internal frame adder : `pulsar2_df_internal_decoder/add_df_internalframe.vhd`
- SWITCH : `pulsar2_df_switch/df_switch_element_v3.vhd`

5.3 Output data operator

- DF output preparation : `pulsar2_df_internal_decoder/df_output_preparation_v2.vhd`
- Switch 32 x 32 : `pulsar2_df_switch/df_switch_matrix_32x32.vhd`
- Duplicator : `pulsar2_df_internal_decoder/df_output_duplicator.vhd`
- SLINK Packer : `pulsar2_df_internal_decoder/df_output_slink_packer_v2.vhd`

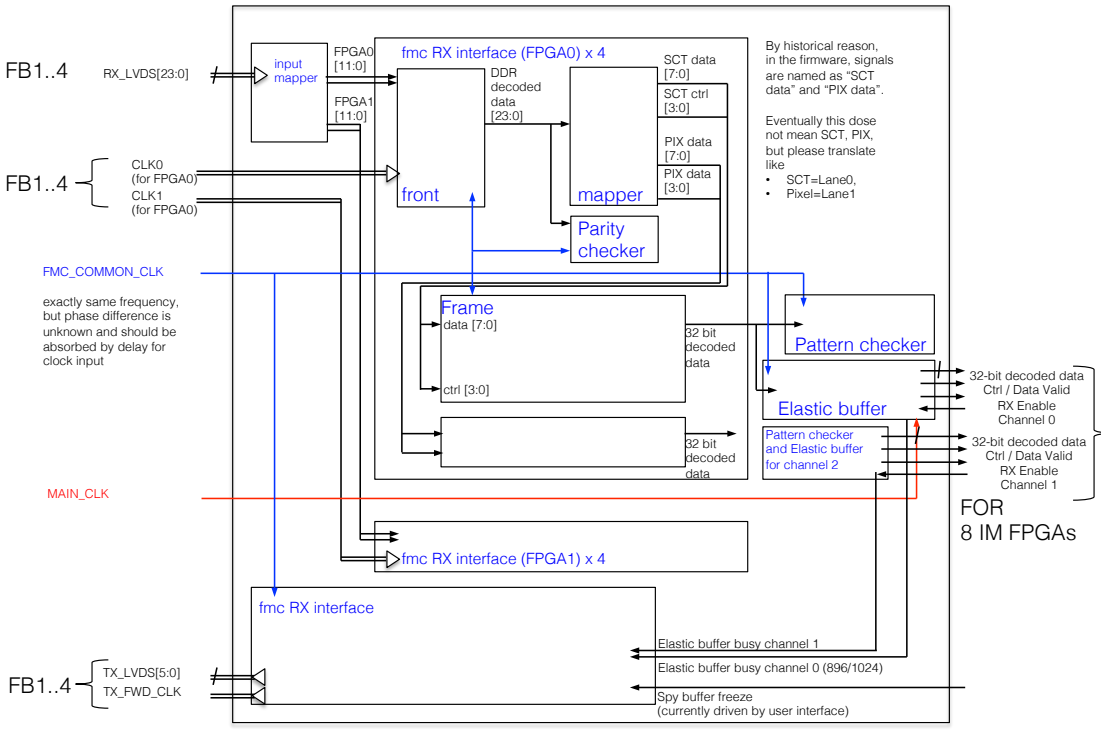

Figure 3: FMC interface firmware overview.

5.4 Internal link input / output

- Internal link interface : `pulsar2_df_internal_link/ilink_interface.vhd`
- Bit Error Rate Test (BERT) pattern generator : `pulsar2_df_internal_link/pattern_gen.vhd`
- Bit Error Rate Test (BERT) pattern checker : `pulsar2_df_internal_link/pattern_chk.vhd`

5.4.1 Internal link

- idle word (at least every 128 cycle) - `D5_`
-

A ATCA fabric interface

B GT channel assignment

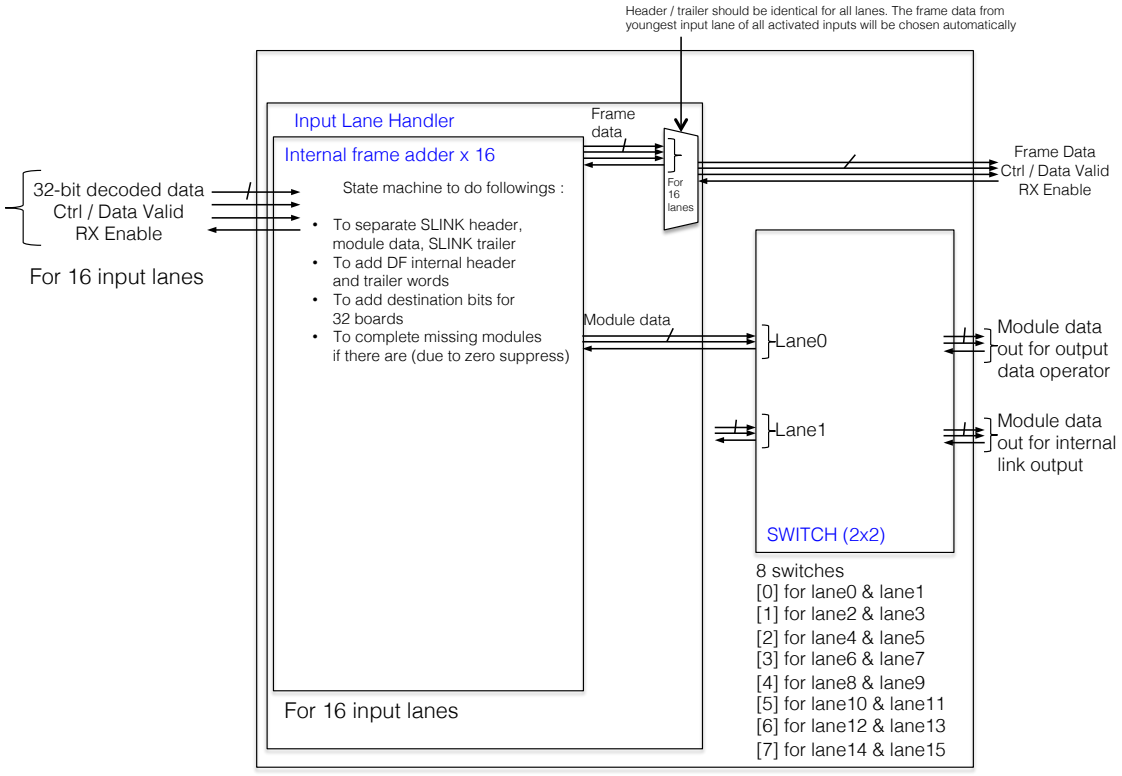

Figure 4: Internal data operator. One modules have three additional words, header, destination words and trailer.

lane	description	
	type	channel
0	IM	ch0 and ch1
1	Fabric	ch3 p0
2	Fabric	ch4 p0
3	Fabric	ch5 p0
4	IM	ch2 and ch3
5	Fabric	ch6 p0
6	Fabric	ch7 p0
7	Fabric	ch8 p0
8	IM	ch4 and ch5
9	Fabric	ch9 po0
10	Fabric	ch10 p0
11	Fabric	ch11 p0
12	IM	ch6 and ch7
13	Fabric	ch12 p0
14	Inter-crate	ch0 p0
15	Inter-crate	ch1 p0

lane	description	
	type	channel
16	IM	ch8 and ch9
17	Fabric	ch3 p1
18	Fabric	ch4 p1
19	Fabric	ch5 p1
20	IM	ch10 and ch11
21	Fabric	ch6 p1
22	Fabric	ch7 p1
23	Fabric	ch8 p1
24	IM	ch12 and ch13
25	Fabric	ch9 p1
26	Fabric	ch10 p1
27	Fabric	ch11 p1
28	IM	ch14 and ch15
29	Fabric	ch12 p1
30	Inter-crate	ch0 p1
31	Inter-crate	ch1 p1

Table 5: Input channel assignment for output data operator module. Defined in "MAPPING_CONF_IDO2ODO" and "MAPPING_CONF_ILI2ODO" in data_formatter_top/data_formatter_constants.vhd.

Original module data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
1	**0**	**0**	**0**	Reserved				Reserved				Reserved				**0**	Reserved			R	Pixel module number (10..0)											Pixel Module Header
0	Column width			Column coordinate (27..16)												S	Row width			Row coordinate (11..0)												Pixel Cluster
1	**0**	**0**	**0**	Reserved				Reserved				Reserved				**1**	Reserved			SCT module number (12..0)												SCT Module Header
0	Hit 2 Width			hit2 empty	Hit 2 coordinate (26..16)											R	Hit1 width			R	Hit 1 coordinate (10..0)											SCT Cluster

Note

* If the second SCT hit is empty, the empty= '1'
* "R" means Reserved
* "S" means Split Cluster Bit

Data formatter internal data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	F/T	Reserved								Random Counter				DF internal Event Counter (from 0 - 255)															
Global destination bits for 32 slots																															
Module DATA																															
1	1	1	0	Reserved																											

NOTE: F/T shows the modules data is fake data only inside of the DF for event synchronization (this is case of "F'='1') or not ("T'='0'). Fake data will be removed in output data
NOTE: Random 4 bit counter is reserved to randamize the switching destination in CENTRAL SWITCH so that the efficiency of switching resource use will be maximized

Special format adding internal link output lanes

(the "global destination bit" is treated as part of "module data" in switch firmware)

3) Local Switching data format (inside internal link switch)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	F/T	Reserved								Random Counter				DF internal Event Counter (from 0 - 255)															
Local output port information (should be single destination packet)																															
Global destination bit for 32 slots (SHOULD BE A SINGLE DESTINATION PACKET DATA)																															
Module DATA																															
1	1	1	0	Reserved																											

NOTE: This DF firmware will miss channel #13 of fabric on purpose to form the input lane number to be 32

Output with 16-bit is determined with the following equation:

- Reference index = (32 + Lane ID – Random Counter) mod 32
- For random counter = 0 case

The original global destination bit is treated as one of normal module words. Note switch firmware only will category, (1) DF header (fragment ID="110X"), (2) Destination bit (following DF header), and (3) DF trailer (fragment ID="1110")

Figure 5: Input data operator firmware overview.

lane	description	
	type	channel
0	AUX0 Tower 0	ch0
1	AUX0 Tower 0	ch1
2	AUX0 Tower 0	ch2
3	AUX0 Tower 0	ch3
4	AUX1 Tower 0	ch4
5	AUX1 Tower 0	ch5
6	AUX1 Tower 0	ch6
7	AUX1 Tower 0	ch7
8	AUX2 Tower 0	ch0
9	AUX2 Tower 0	ch1
10	AUX2 Tower 0	ch2
11	AUX2 Tower 0	ch3
12	AUX3 Tower 0	ch4
13	AUX3 Tower 0	ch5
14	AUX3 Tower 0	ch6
15	AUX3 Tower 0	ch7
16	SSB Tower 0	

lane	description	
	type	channel
17	AUX0 Tower 1	ch0
18	AUX0 Tower 1	ch1
19	AUX0 Tower 1	ch2
20	AUX0 Tower 1	ch3
21	AUX1 Tower 1	ch4
22	AUX1 Tower 1	ch5
23	AUX1 Tower 1	ch6
24	AUX1 Tower 1	ch7
25	AUX2 Tower 1	ch0
26	AUX2 Tower 1	ch1
27	AUX2 Tower 1	ch2
28	AUX2 Tower1	ch3
29	AUX3 Tower1	ch4
30	AUX3 Tower1	ch5
31	AUX3 Tower1	ch6
32	AUX3 Tower 1	ch7
33	SSB Tower 1	

Table 6: SLINK output channel assignment (34 channel). "MAPPING_CONF_SLINKOUT2GTLOC" and "MAPPING_CONF_SLINKOUT2GTLOC" in data_formatter_top/data_formatter_constants.vhd.

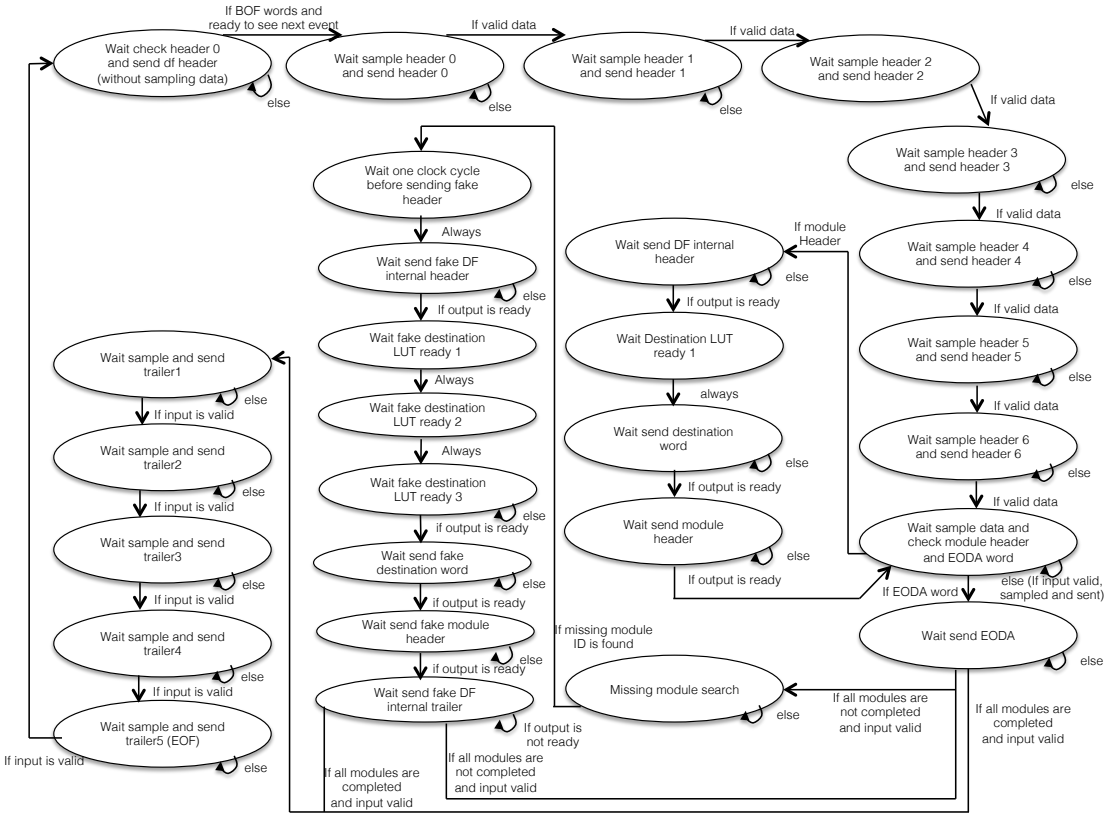

Figure 6: State machine in Internal frame adder.

lane	description		lane	description	
	type	channel		type	channel
0	IM	ch0 and ch1	16	IM	ch8 and ch9
1	Fabric	ch3 p0	17	Fabric	ch3 p1
2	Fabric	ch4 p0	18	Fabric	ch4 p1
3	Fabric	ch5 p0	19	Fabric	ch5 p1
4	IM	ch2 and ch3	20	IM	ch10 and ch11
5	Fabric	ch6 p0	21	Fabric	ch6 p1
6	Fabric	ch7 p0	22	Fabric	ch7 p1
7	Fabric	ch8 p0	23	Fabric	ch8 p1
8	IM	ch4 and ch5	24	IM	ch12 and ch13
9	Fabric	ch9 po0	25	Fabric	ch9 p1
10	Fabric	ch10 p0	26	Fabric	ch10 p1
11	Fabric	ch11 p0	27	Fabric	ch11 p1
12	IM	ch6 and ch7	28	IM	ch14 and ch15
13	Fabric	ch12 p0	29	Fabric	ch12 p1
14	Inter-crate	ch0 p0	30	Inter-crate	ch0 p1
15	Inter-crate	ch1 p0	31	Inter-crate	ch1 p1

Table 7: Input channel assignment for internal data output module (i.e. input of Central Switch.). Defined in "MAPPING_CONF_IDO2ILO" and "MAPPING_CONF_ILI2ILO" in data_formatter_top/data_formatter_constants.vhd.

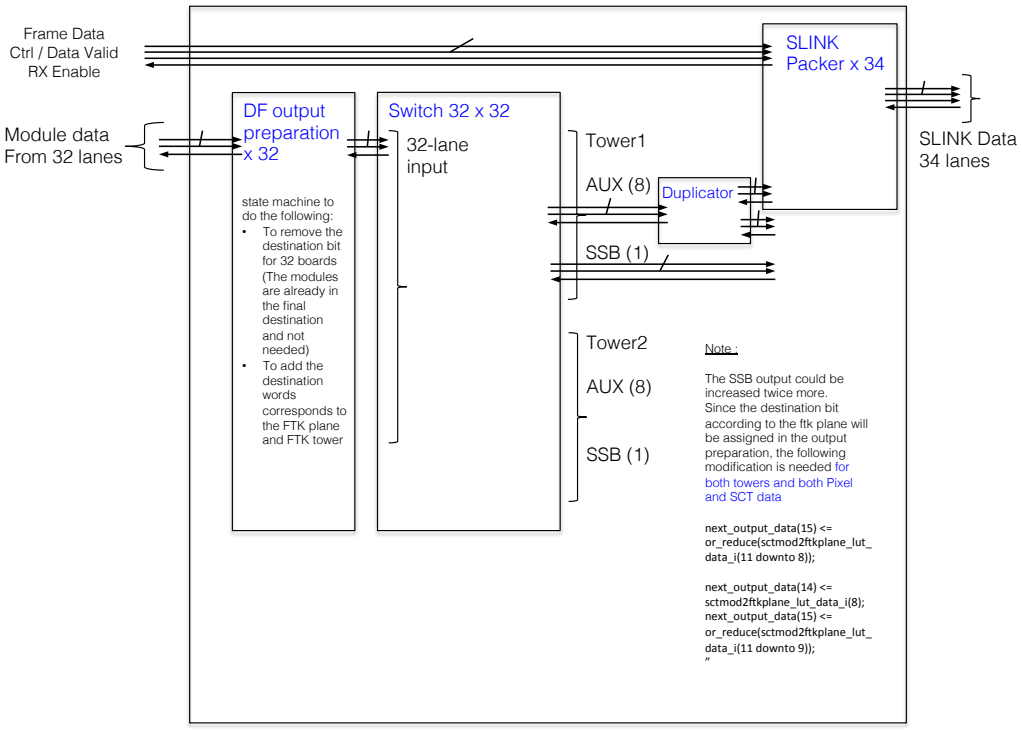

Figure 7: Output data operator firmware overview.

lane	description	
	type	channel
0	Fabric	ch3 p0
1	Fabric	ch4 p0
2	Fabric	ch5 p0
3	Fabric	ch6 p0
4	Fabric	ch7 p0
5	Fabric	ch8 p0
6	Fabric	ch9 p0
7	Fabric	ch10 p0
8	Fabric	ch11 p0
9	Fabric	ch12 p0
10	Internal link	ch0 p0
11	Internal link	ch1 p0

lane	description	
	type	channel
12	Fabric	ch3 p1
13	Fabric	ch4 p1
14	Fabric	ch5 p1
15	Fabric	ch6 p1
16	Fabric	ch7 p1
17	Fabric	ch8 p1
18	Fabric	ch9 p1
19	Fabric	ch10 p1
20	Fabric	ch11 p1
21	Fabric	ch12 p1
22	Internal link	ch0 p1
23	Internal link	ch1 p1

Table 8: Internal link channel assignment. Defined in “MAPPING_CONF_INTERNALLINK2GTCHANNEL” and “MAPPING_CONF_INTERNALLINK2GTLOC” in data_formatter_top/data_formatter_constants.vhd.

31:0
$K23.7\&K23.7\&K23.7\&K23.7$

Table 9: Pad-word definition. It will be inserted in the interface (TX side) every 128-word cycle, and removed in the interface (RX side) in The isKCharctor word is 1111. This is for RX clock correction functionality.

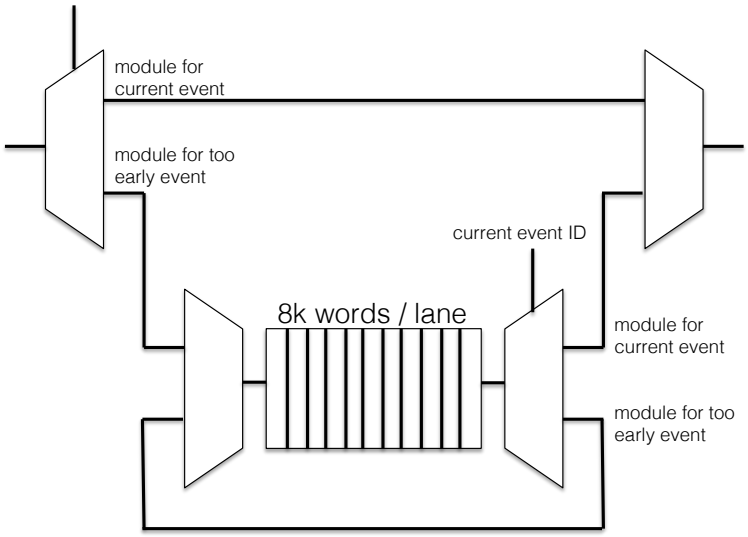

Figure 8: Schematics of event sorting buffer in the SLINK packer.

31:16	15:13	12	11:8	7:0
$D5.6\&D5.6$	Reserved	XOFF	Return Channel 4 bit	$K28.5$

Table 10: idle word definition. At least it will be inserted in the interface every 128-word cycle. The isKCharctor word is 0001.

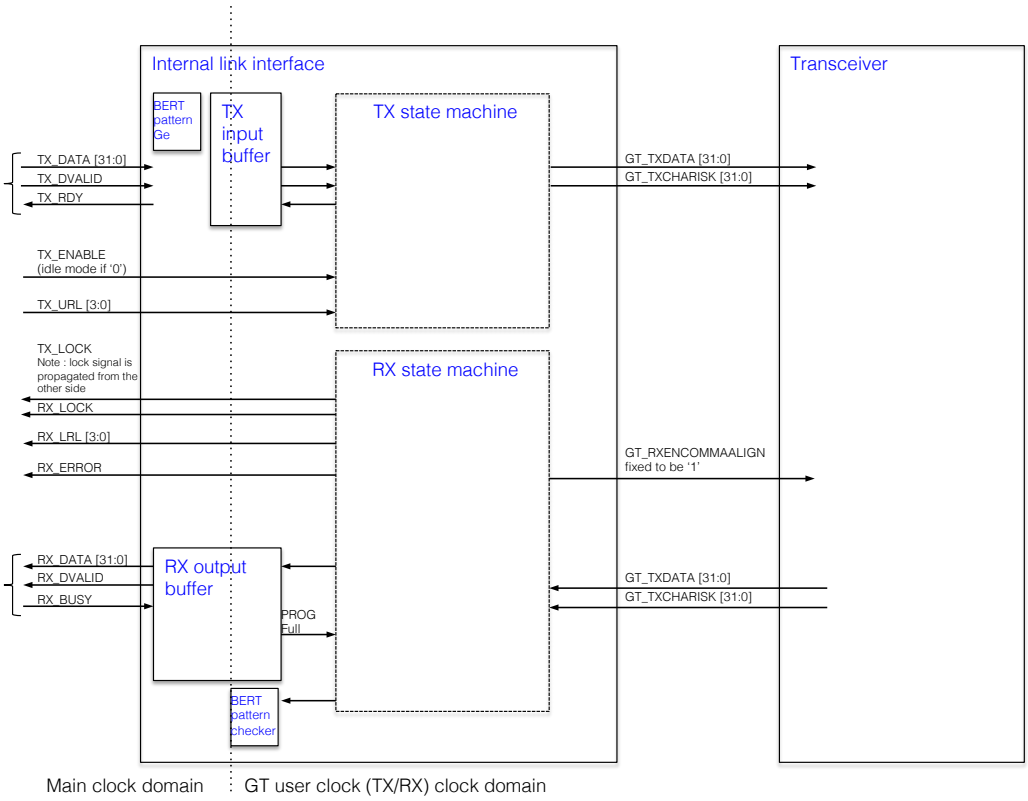

Figure 9: Internal link interface. This includes clock domain crossing (CDC) buffer between GT user clocks and main logic clock.

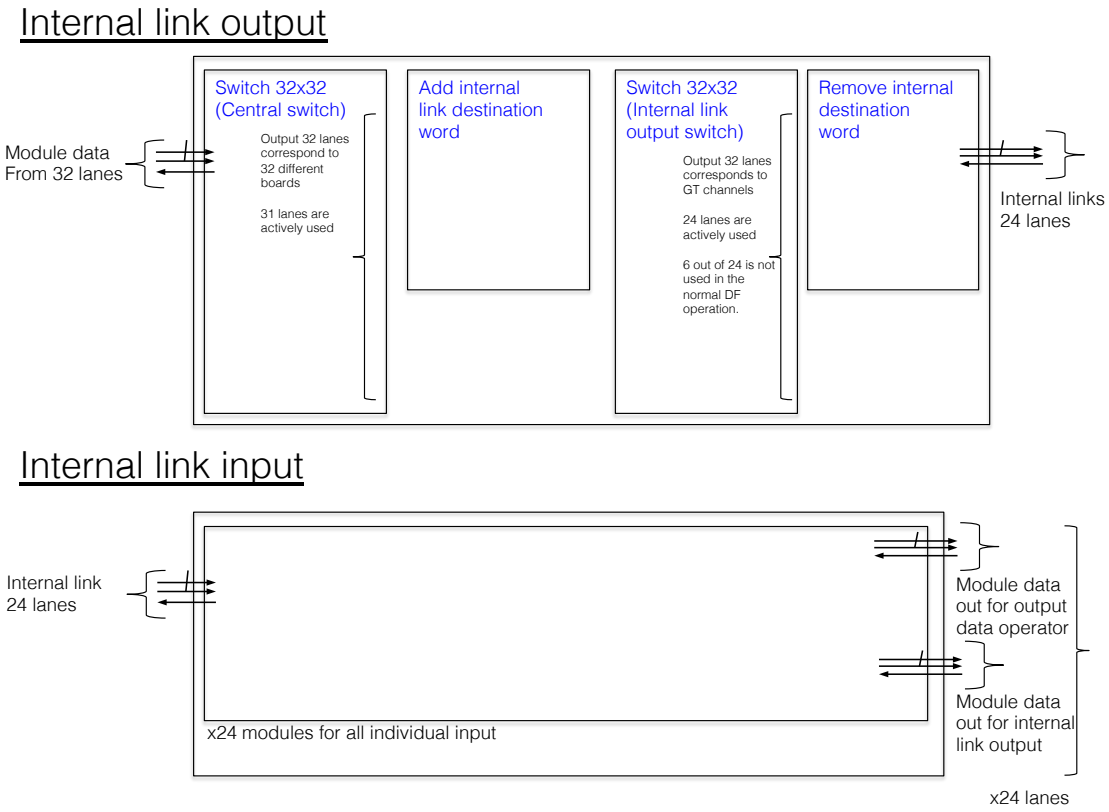

Figure 10: Schematics of input and output internal link.

Routing table description

¶ 89 Each column in the routing table depict Logical Slot positions. There are fifteen Fabric Channels per Slot each represented by a cell in the table. Each cell within the table represents a Fabric Channel and the numbers within the cell represent the destination end-point to which that Channel is routed. For example, the cell representing Channel 1 of Slot 9 contains the value (1–8) to indicate it is connected to Slot 1, Channel 8. This method to describe routing destinations per Channel is used for all routing assignment tables in this specification.

Table 6-11 Full Mesh Backplane routing assignments

	Logical Slot #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Connector	Channel #																
P20	15	16-1	16-2	16-3	16-4	16-5	16-6	16-7	16-8	16-9	16-10	16-11	16-12	16-13	16-14	16-15	15-15
P20	14	15-1	15-2	15-3	15-4	15-5	15-6	15-7	15-8	15-9	15-10	15-11	15-12	15-13	15-14	14-14	14-15
P20	13	14-1	14-2	14-3	14-4	14-5	14-6	14-7	14-8	14-9	14-10	14-11	14-12	14-13	13-13	13-14	13-15
P21	12	13-1	13-2	13-3	13-4	13-5	13-6	13-7	13-8	13-9	13-10	13-11	13-12	12-12	12-13	12-14	12-15
P21	11	12-1	12-2	12-3	12-4	12-5	12-6	12-7	12-8	12-9	12-10	12-11	11-11	11-12	11-13	11-14	11-15
P21	10	11-1	11-2	11-3	11-4	11-5	11-6	11-7	11-8	11-9	11-10	10-10	10-11	10-12	10-13	10-14	10-15
P21	9	10-1	10-2	10-3	10-4	10-5	10-6	10-7	10-8	10-9	9-9	9-10	9-11	9-12	9-13	9-14	9-15
P21	8	9-1	9-2	9-3	9-4	9-5	9-6	9-7	9-8	8-8	8-9	8-10	8-11	8-12	8-13	8-14	8-15
P22	7	8-1	8-2	8-3	8-4	8-5	8-6	8-7	7-7	7-8	7-9	7-10	7-11	7-12	7-13	7-14	7-15
P22	6	7-1	7-2	7-3	7-4	7-5	7-6	6-6	6-7	6-8	6-9	6-10	6-11	6-12	6-13	6-14	6-15
P22	5	6-1	6-2	6-3	6-4	6-5	5-5	5-6	5-7	5-8	5-9	5-10	5-11	5-12	5-13	5-14	5-15
P22	4	5-1	5-2	5-3	5-4	4-4	4-5	4-6	4-7	4-8	4-9	4-10	4-11	4-12	4-13	4-14	4-15
P22	3	4-1	4-2	4-3	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	3-12	3-13	3-14	3-15
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13	1-14	1-15

NOTE: The shading used in Table 6-11, "Full Mesh Backplane routing assignments," shows discontinuity of the routing sequence across rows and columns in the table.

Figure 11: ATCA fabric connection table.

ATCA ch	Type	ID	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	NOTE 2	Categoly	GT ID	GT ch	LSC ch	Internal Link	RX FLIP	TX FLIP
J32P19	QSFP+	T1	Ch0	218	1	0	33	217				RTM LEFT	gt33	0	0			
J32P18	QSFP+	T1	Ch1	218	0	0	32	217		AUX T0		RTM LEFT	gt32	1	1			
J32P17	QSFP+	T1	Ch2	217	3	0	31	217				RTM LEFT	gt31	2	2			
J32P16	QSFP+	T1	Ch3	217	2	0	30	217				RTM LEFT	gt30	3	3			
J32P15	QSFP+	T2	Ch0	217	1	0	29	217				RTM LEFT	gt29	4	4			
J32P14	QSFP+	T2	Ch1	217	0	0	28	217		AUX T1		RTM LEFT	gt28	5	5			
J32P13	QSFP+	T2	Ch2	216	3	0	27	217				RTM LEFT	gt27	6	6			
J32P12	QSFP+	T2	Ch3	216	2	0	26	217				RTM LEFT	gt26	7	7			
J32P11	QSFP+	T3	Ch0	216	1	0	25	217			SLINK	RTM LEFT	gt25	8	8			
J32P10	QSFP+	T3	Ch1	216	0	0	24	217		AUX T2		RTM LEFT	**gt24**	9	9			
J32P9	QSFP+	T3	Ch2	215	3	0	23	214	U27			RTM LEFT	gt23	10	10			
J32P8	QSFP+	T3	Ch3	215	2	0	22	214				RTM LEFT	gt22	11	11			
J32P7	QSFP+	T4	Ch0	215	1	0	21	214				RTM LEFT	gt21	12	12			
J32P6	QSFP+	T4	Ch1	215	0	0	20	214		AUX T3		RTM LEFT	gt20	13	13			
J32P5	QSFP+	T4	Ch2	214	3	0	19	214				RTM LEFT	gt19	14	14			
J32P4	QSFP+	T4	Ch3	214	2	0	18	214				RTM LEFT	gt18	15	15			
J32P3	SFP+	T5		214	1	0	17	214		SSB T		RTM LEFT	gt17	16	16			
J32P2	SFP+	T6		214	0	0	16	214		Internal Link Ch0 P0		RTM LEFT	gt16	41		7	**RX**	
J32P1	SFP+	T7		213	3	0	15	214		Internal Link Ch0 P1		RTM LEFT	gt15	50		16		
J32P0	N/A			213	2	0	14	214		-	-	-	gt14					

ATCA ch	Type	ID	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	NOTE 2	Categoly	GT ID				RX FLIP	TX FLIP
J33P19	QSFP+	T1	Ch0	213	1	0	13	214				RTM LEFT	gt13	17	17			
J33P18	QSFP+	T1	Ch1	213	0	0	12	214		AUX B0		RTM LEFT	**gt12**	18	18			
J33P17	QSFP+	T1	Ch2	212	3	0	11	211				RTM LEFT	gt11	19	19			**TX**
J33P16	QSFP+	T1	Ch3	212	2	0	10	211				RTM LEFT	gt10	20	20		**RX**	
J33P15	QSFP+	T2	Ch0	212	1	0	9	211				RTM LEFT	gt9	21	21			
J33P14	QSFP+	T2	Ch1	212	0	0	8	211		AUX B1		RTM LEFT	gt8	22	22			
J33P13	QSFP+	T2	Ch2	211	3	0	7	211				RTM LEFT	gt7	23	23			
J33P12	QSFP+	T2	Ch3	211	2	0	6	211				RTM LEFT	gt6	24	24			**TX**
J33P11	QSFP+	T3	Ch0	211	1	0	5	211			SLINK	RTM LEFT	gt5	25	25			
J33P10	QSFP+	T3	Ch1	211	0	0	4	211		AUX B2		RTM LEFT	gt4	26	26			
J33P9	QSFP+	T3	Ch2	210	3	0	3	211	U27			RTM LEFT	gt3	27	27			
J33P8	QSFP+	T3	Ch3	210	2	0	2	211				RTM LEFT	gt2	28	28			
J33P7	QSFP+	T4	Ch0	210	1	0	1	211				RTM LEFT	gt1	29	29			
J33P6	QSFP+	T4	Ch1	210	0	0	0	211		AUX B3		RTM LEFT	**gt0**	30	30			
J33P5	QSFP+	T4	Ch2	110	0	1	0	110				RTM RIGHT	gt0	31	31		**RX**	**TX**
J33P4	QSFP+	T4	Ch3	110	1	1	1	110				RTM RIGHT	gt1	32	32		**RX**	**TX**
J33P3	SFP+	T5		110	2	1	2	110		SSB B		RTM RIGHT	gt2	33	33		**RX**	**TX**
J33P2	SFP+	T6		110	3	1	3	110		Internal Link Ch1 P0		RTM RIGHT	gt3	42		8	**RX**	**TX**
J33P1	SFP+	T7		111	0	1	4	110		Internal Link Ch1 P1		RTM RIGHT	gt4	51		17		**TX**
J33P0	N/A			111	1	1	5	110		-	-	-	gt5					

Figure 12: Transceiver channel assignment summary (1). For RTM channels.

Fabric	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	Categoly	GT ID	GT ch	Internal Link	RX FLIP	TX FLIP
C13	P1	111	2	1	6	110	U27	-	NOT USED					**TX**
C13	P0	111	3	1	7	110		-	NOT USED					
C12	P1	112	0	1	8	112	U11	Internal link	Fabric	**gt0**				
C12	P0	112	1	1	9	112			Fabric	gt1				
C11	P1	112	2	1	10	112			Fabric	gt2				
C11	P0	112	3	1	11	112			Fabric	gt3				
C10	P1	113	0	1	12	112			Fabric	gt4				
C10	P0	113	1	1	13	112			Fabric	gt5				
C9	P1	113	2	1	14	112			Fabric	gt6	49	15		
C9	P0	113	3	1	15	112			Fabric	gt7	40	6		
C8	P1	114	0	1	16	115			Fabric	**gt8**	48	14		
C8	P0	114	1	1	17	115			Fabric	gt9	39	5		
C7	P1	114	2	1	18	115			Fabric	gt10	47	13		
C7	P0	114	3	1	19	115			Fabric	gt11	38	4	**RX**	
C6	P1	115	0	1	20	115			Fabric	gt12	46	12		
C6	P0	115	1	1	21	115			Fabric	gt13	37	3		
C5	P1	115	2	1	22	115			Fabric	gt14	45	11		
C5	P0	115	3	1	23	115			Fabric	gt15	36	2		
C4	P1	116	0	1	24	115			Fabric	gt16	44	10		
C4	P0	116	1	1	25	115			Fabric	gt17	35	1		
C3	P1	116	2	1	26	115			Fabric	gt18	43	9		
C3	P0	116	3	1	27	115			Fabric	gt19	34	0		
C2	P1	117	**1**	1	**29**	118		HUB						
C2	P0	117	**0**	1	**28**	118		HUB						
C1	P3	117	2	1	30	118		HUB						
C1	P2	117	3	1	31	118		HUB						
C1	P1	118	0	1	32	118		HUB						
C1	P0	118	1	1	33	118		IP Bus	1000BASE-T	gt0				

FMC	GP	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE	FTK IM	Channel			RX FLP	TX FLP
3	0	118	2	1	34	118	U11	Shared with IPBus	3	0			**RX**	
3	1	118	3	1	35	118		Shared with IPBus	3	1				
3	2	119	0	1	36	118				N/C				
4	0	119	1	1	37	118			4	0			**RX**	**TX**
4	1	119	2	1	38	118			4	1			**TX**	
4	2	119	3	1	39	118				N/C				**TX**
2	2	218	2	0	34	217	U11	Shared with RTM		N/C				
2	1	218	3	0	35	217		Shared with RTM	2	1				**TX**
2	0	219	0	0	36	219			2	0				
1	2	219	1	0	37	219				N/C			**RX**	
1	1	219	2	0	38	219			1	1			**RX**	
1	0	219	3	0	39	219			1	1			**RX**	**TX**

Figure 13: Transceiver channel assignment summary (2). For Fabric and DF-IM channels.

C IP Bus registers

See `https://okumura.web.cern.ch/okumura/tmp/address_df.xml`.

C.1 IP Address

Address	Bit Postion	R/W	Name	Description
0X00000000	31:0	R	ipaddress	IP address (IPv4 32 bit)

C.2 Reset

Address	Bit Postion	R/W	Name	Description
0X00000001			reset	
	0	R/W	reset_delay	
	1	R/W	disable_fmc_input	
	2	R/W	reset_parity_checker	
	3	R/W	fmcin_logic_reset	
	4	R/W	main_state_machine_reset	
	5	R/W	i2c_state_machine_reset	
	6	R/W	configurable_parameter_reset	
	7	R/W	counter_parameter_reset	
	8	R/W	counter_parameter_reset	
	31:9	-		Reserved

C.3 Front FIFO error

Address	Bit Postion	R/W	Name	Description
0X00000002		R	fmcin_front_fifo_error	

.... to be summarized, including the details of use case for all the parameters.