DF firmware design specification figures

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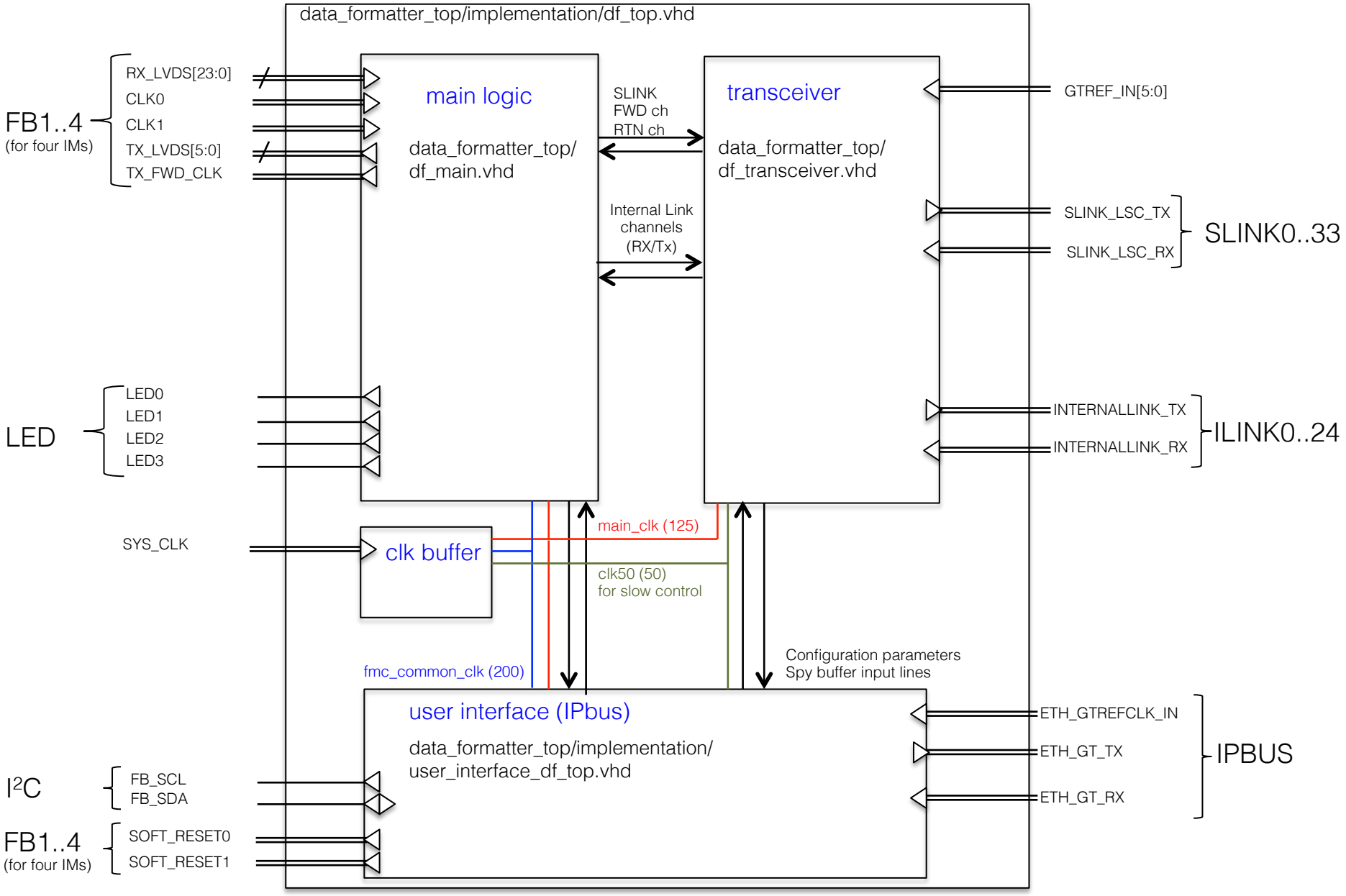
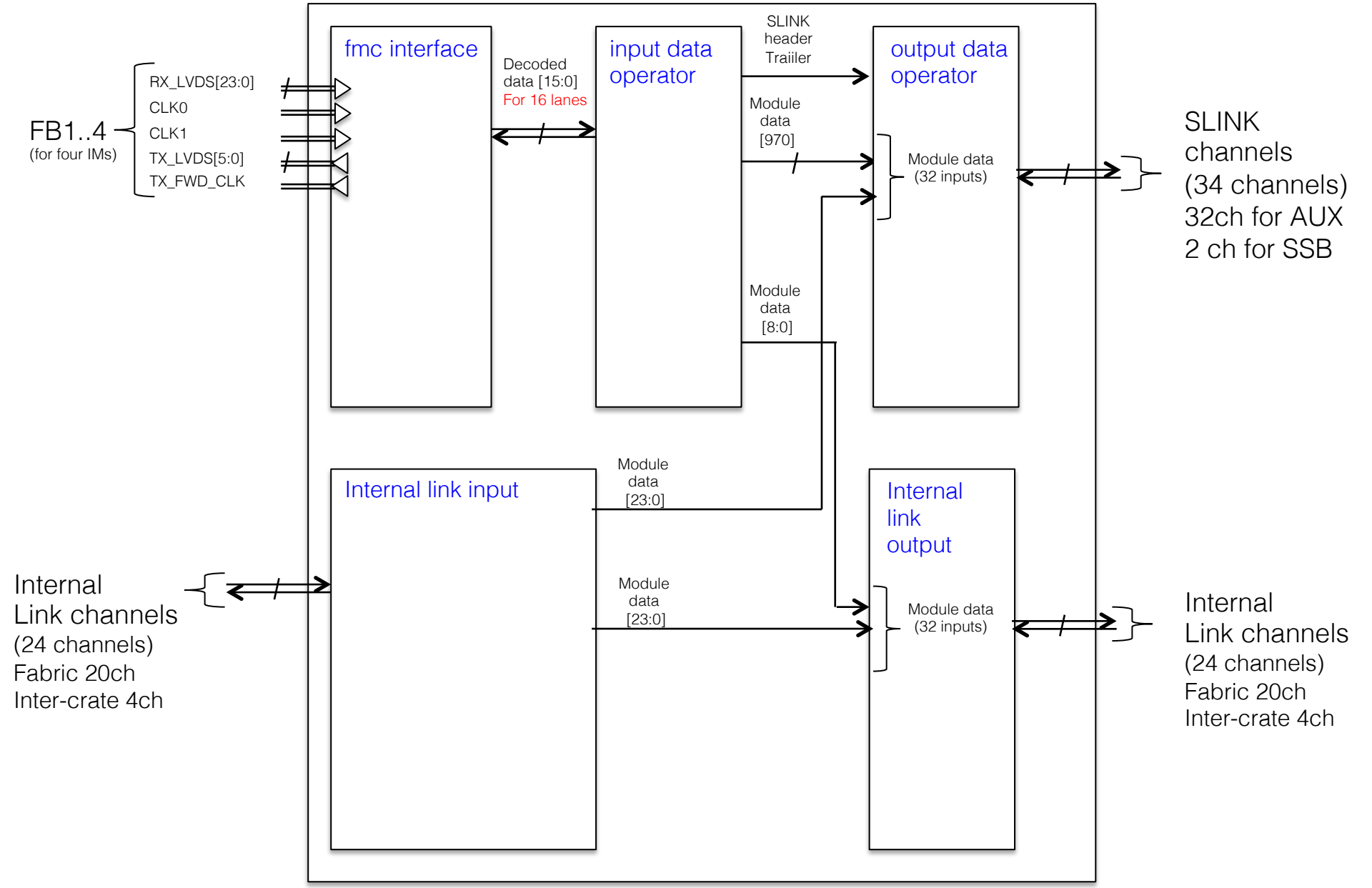
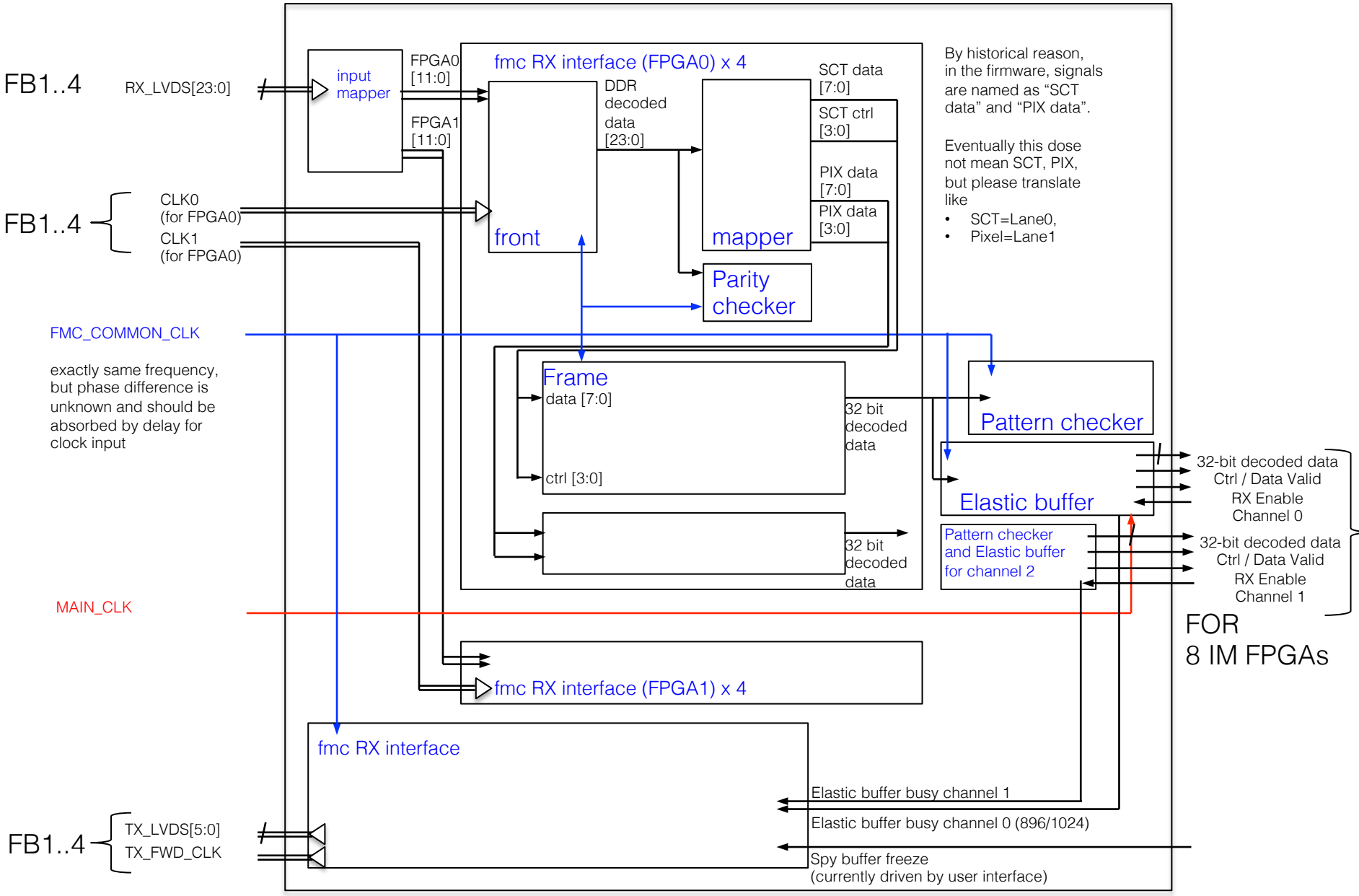
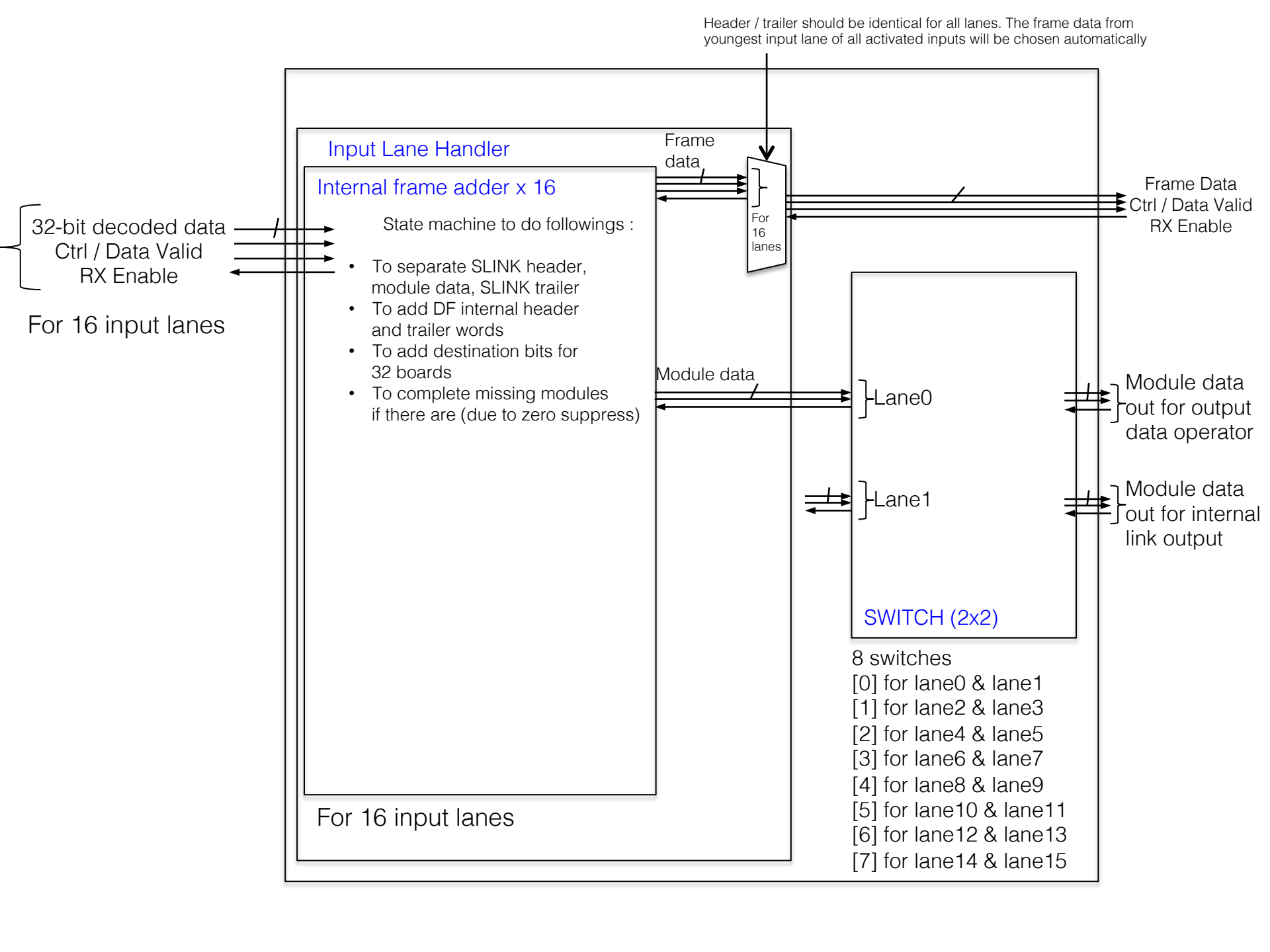
TO BE UPDATED


data_formatter_top/implementation/df_top.vhd
FB1..4
(for four IMs)
RX_LVDS[23:0]
CLK0
CLK1
TX_LVDS[5:0]
TX_FWD_CLK
main logic
data_formatter_top/
df_main.vhd
SLINK
FWD ch
RTN ch
transceiver
data_formatter_top/
df_transceiver.vhd
GTREF_IN[5:0]
Internal Link
channels
(RX/Tx)
SLINK_LSC_TX
SLINK_LSC_RX
SLINK0..33
LED
LED0
LED1
LED2
LED3
INTERNALLINK_TX
INTERNALLINK_RX
ILINK0..24
SYS_CLK
clk buffer
main_clk (125)
clk50 (50)
for slow control
fmc_common_clk (200)
Configuration parameters
Spy buffer input lines
user interface (IPbus)
data_formatter_top/implementation/
user_interface_df_top.vhd
ETH_GTREFCLK_IN
ETH_GT_TX
ETH_GT_RX
IPBUS
I2C
FB_SCL
FB_SDA
FB1..4
(for four IMs)
SOFT_RESET0
SOFT_RESET1


FB1..4
(for four IMs)
RX_LVDS[23:0]
CLK0
CLK1
TX_LVDS[5:0]
TX_FWD_CLK
fmc interface
Decoded
data [15:0]
For 16 lanes
input data
operator
SLINK
header
Trailler
Module
data
[970]
Module
data
[8:0]
output data
operator
Module data
(32 inputs)
SLINK
channels
(34 channels)
32ch for AUX
2 ch for SSB
Internal link input
Module
data
[23:0]
Module
data
[23:0]
Internal
link
output
Module data
(32 inputs)
Internal
Link channels
(24 channels)
Fabric 20ch
Inter-crate 4ch
Internal
Link channels
(24 channels)
Fabric 20ch
Inter-crate 4ch


FB1..4
RX_LVDS[23:0]
input mapper
FPGA0 [11:0]
FPGA1 [11:0]
fmc RX interface (FPGA0) x 4
DDR decoded data [23:0]
front
mapper
SCT data [7:0]
SCT ctrl [3:0]
PIX data [7:0]
PIX data [3:0]
Parity checker
By historical reason, in the firmware, signals are named as "SCT data" and "PIX data".
Eventually this dose not mean SCT, PIX, but please translate like
• SCT=Lane0,
• Pixel=Lane1
FB1..4
CLK0 (for FPGA0)
CLK1 (for FPGA0)
FMC_COMMON_CLK
exactly same frequency, but phase difference is unknown and should be absorbed by delay for clock input
Frame
data [7:0]
ctrl [3:0]
32 bit decoded data
Pattern checker
Elastic buffer
32-bit decoded data
Ctrl / Data Valid
RX Enable
Channel 0
Pattern checker and Elastic buffer for channel 2
32-bit decoded data
Ctrl / Data Valid
RX Enable
Channel 1
MAIN_CLK
FOR 8 IM FPGAs
fmc RX interface (FPGA1) x 4
fmc RX interface
Elastic buffer busy channel 1
Elastic buffer busy channel 0 (896/1024)
Spy buffer freeze (currently driven by user interface)
FB1..4
TX_LVDS[5:0]
TX_FWD_CLK


Header / trailer should be identical for all lanes. The frame data from youngest input lane of all activated inputs will be chosen automatically
Input Lane Handler
Internal frame adder x 16
State machine to do followings :
To separate SLINK header, module data, SLINK trailer
To add DF internal header and trailer words
To add destination bits for 32 boards
To complete missing modules if there are (due to zero suppress)
32-bit decoded data
Ctrl / Data Valid
RX Enable
For 16 input lanes
Frame data
For 16 lanes
Frame Data
Ctrl / Data Valid
RX Enable
Module data
Lane0
Lane1
Module data out for output data operator
Module data out for internal link output
SWITCH (2x2)
8 switches
[0] for lane0 & lane1
[1] for lane2 & lane3
[2] for lane4 & lane5
[3] for lane6 & lane7
[4] for lane8 & lane9
[5] for lane10 & lane11
[6] for lane12 & lane13
[7] for lane14 & lane15
For 16 input lanes

Original module data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
1	**0**	**0**	**0**	Reserved				Reserved				Reserved				**0**	Reserved			R	Pixel module number (10..0)											Pixel Module Header
0	Column width			Column coordinate (27..16)												S	Row width			Row coordinate (11..0)												Pixel Cluster
1	**0**	**0**	**0**	Reserved				Reserved				Reserved				**1**	Reserved			SCT module number (12..0)												SCT Module Header
0	Hit 2 Width			hit2 empty	Hit 2 coordinate (26..16)											R	Hit1 width			R	Hit 1 coordinate (10..0)											SCT Cluster

Note

* If the second SCT hit is empty, the empty= '1'
* "R" means Reserved
* "S" means Split Cluster Bit

Data formatter internal data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	F/T	Reserved							Random Counter					DF internal Event Counter (from 0 - 255)															
Global destination bits for 32 slots																															
Module DATA																															
1	1	1	0	Reserved																											

NOTE: F/T shows the modules data is fake data only inside of the DF for event synchronization (this is case of "F"='1') or not ("T"='0'). Fake data will be removed in output data

NOTE: Random 4 bit counter is reserved to randamize the switching destination in CENTRAL SWITCH so that the efficiency of switching resource use will be maximized

Special format adding internal link output lanes

(the “global destination bit” is treated as part of “module data” in switch firmware)

3) Local Switching data format (inside internal link switch)

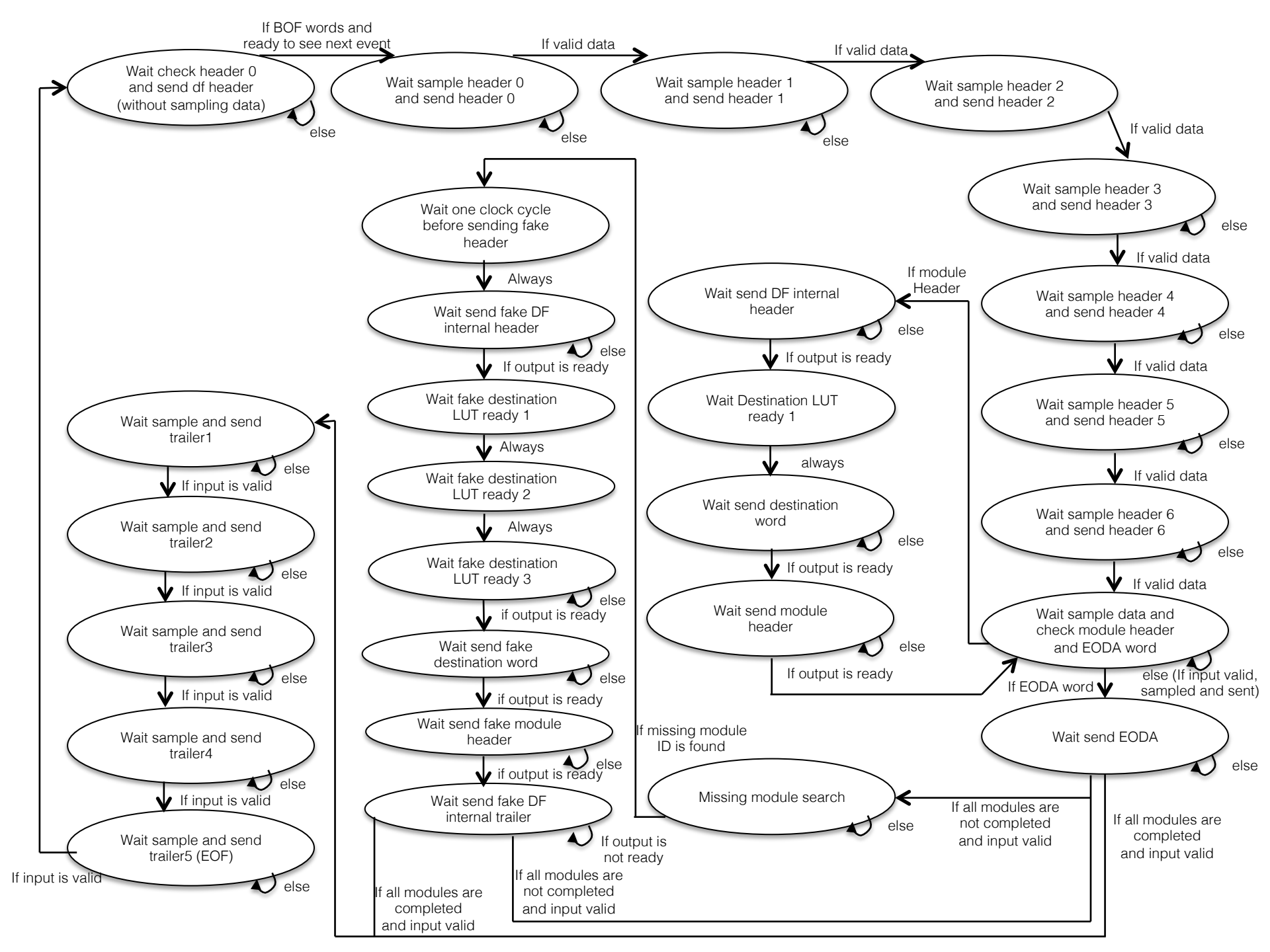
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	F/T	Reserved							Random Counter					DF internal Event Counter (from 0 - 255)															
Local output port information (should be single destination packet)																															
Global destination bit for 32 slots (SHOULD BE A SINGLE DESTINATION PACKET DATA)																															
Module DATA																															
1	1	1	0	Reserved																											

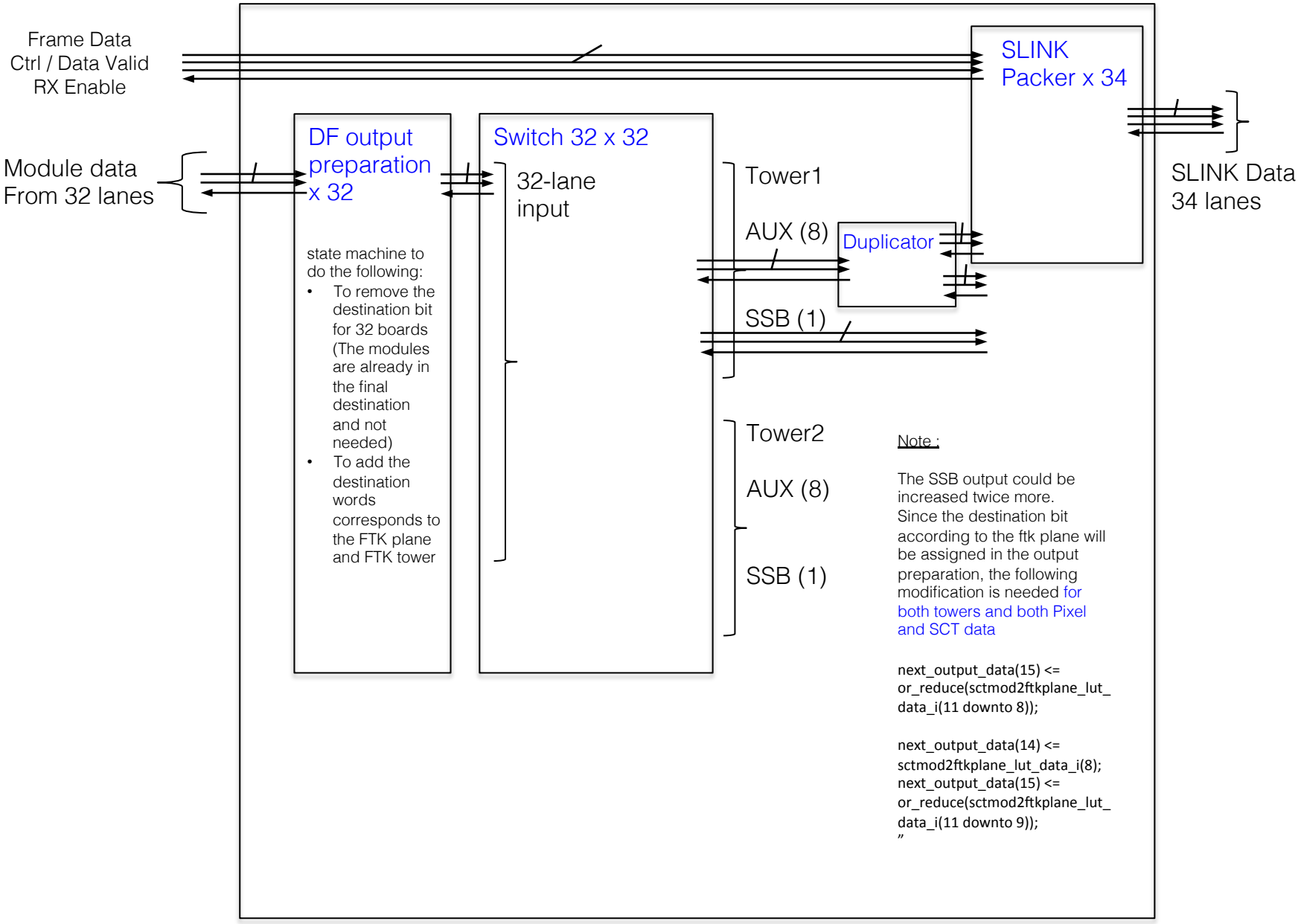
NOTE: This DF firmware will miss channel #13 of fabric on purpose to form the input lane number to be 32

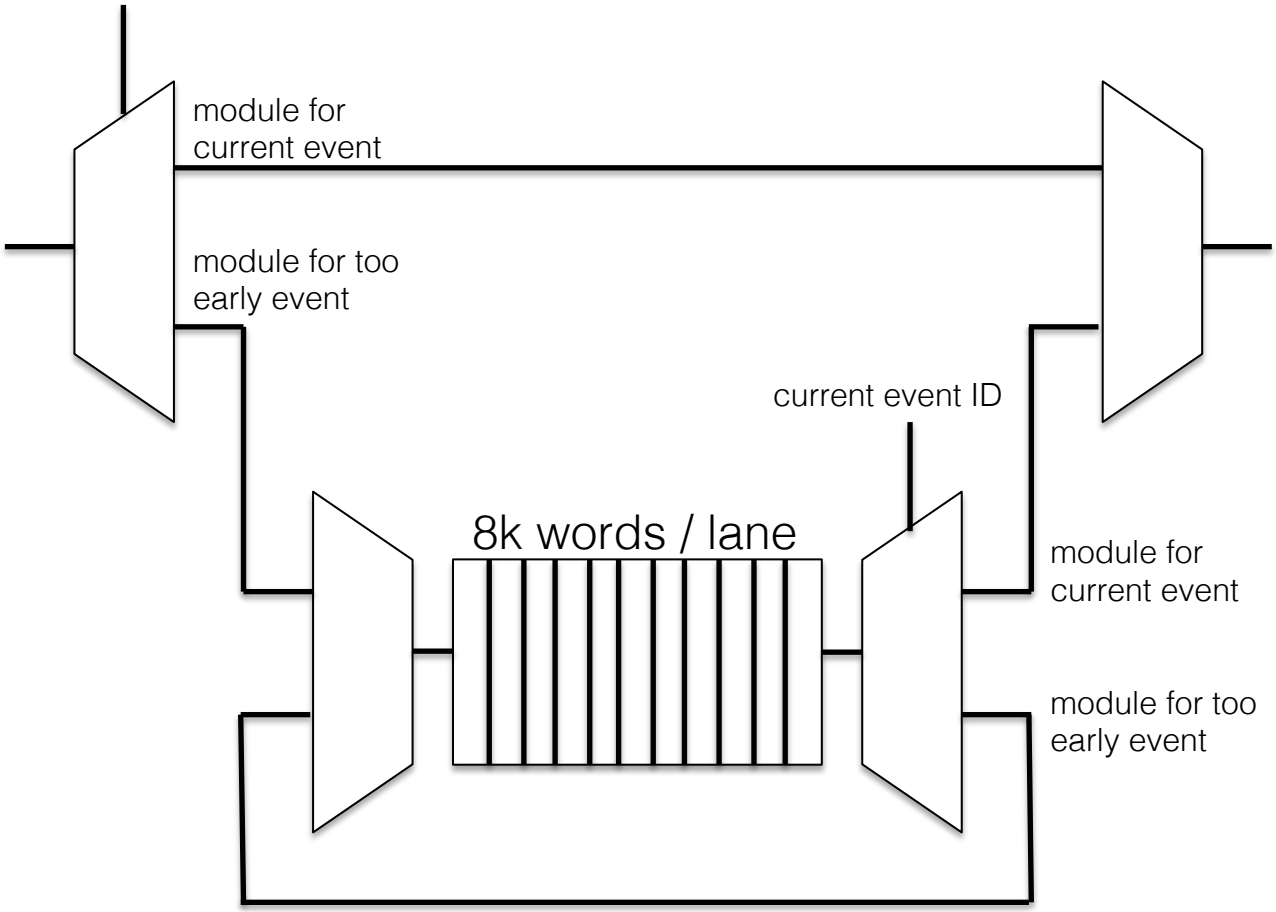
Output with 16-bit is determined with the following equation:

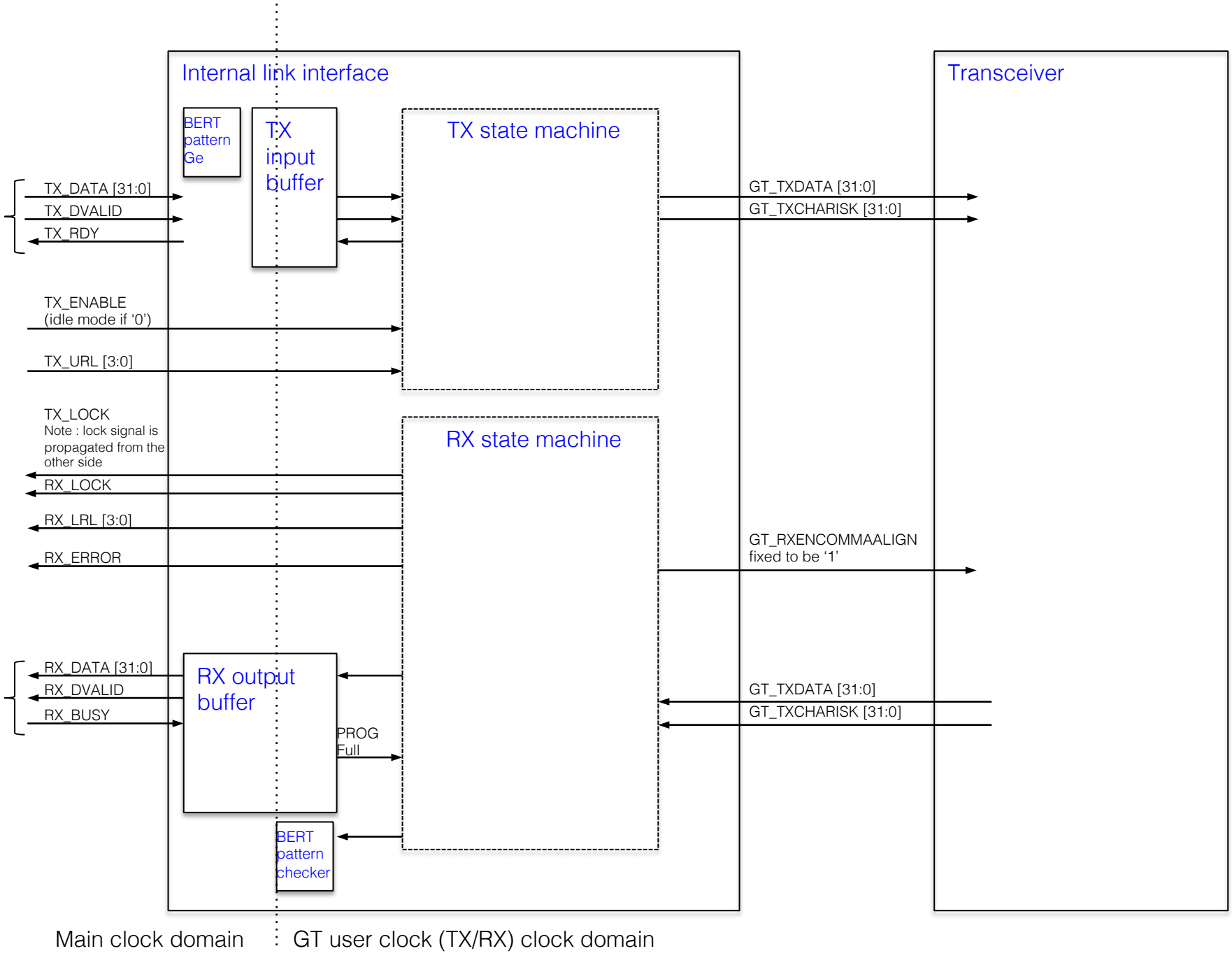
- Reference index = (32 + Lane ID – Random Counter) mod 32
- For random counter = 0 case

The original global destination bit is treated as one of normal module words. Note switch firmware only will category, (1) DF header (fragment ID=“110X”), (2) Destination bit (following DF header), and (3) DF trailer (fragment ID=“1110”)

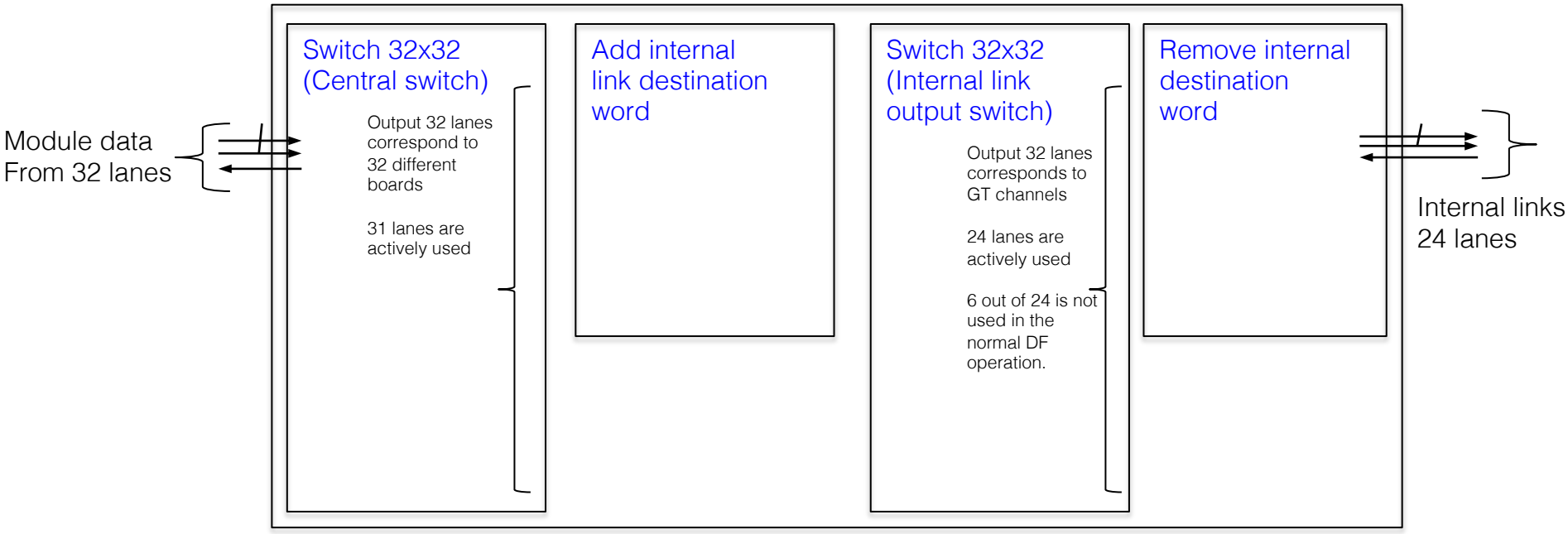

If BOF words and ready to see next event
If valid data
If valid data
If valid data
If valid data
If valid data
If valid data
If valid data
If valid data
If valid data
If valid data
Always
Always
Always
if output is ready
if output is ready
if output is ready
if output is ready
If output is ready
If output is ready
If output is ready
always
If input is valid
If input is valid
If input is valid
If input is valid
If input is valid
If input is valid
If module Header
If missing module ID is found
If EODA word
else (If input valid, sampled and sent)
If output is not ready
If all modules are not completed and input valid
If all modules are completed and input valid
If all modules are not completed and input valid
If all modules are completed and input valid
Wait check header 0 and send df header (without sampling data)
Wait sample header 0 and send header 0
Wait sample header 1 and send header 1
Wait sample header 2 and send header 2
Wait sample header 3 and send header 3
Wait sample header 4 and send header 4
Wait sample header 5 and send header 5
Wait sample header 6 and send header 6
Wait sample data and check module header and EODA word
Wait send EODA
Wait one clock cycle before sending fake header
Wait send fake DF internal header
Wait fake destination LUT ready 1
Wait fake destination LUT ready 2
Wait fake destination LUT ready 3
Wait send fake destination word
Wait send fake module header
Wait send fake DF internal trailer
Wait send DF internal header
Wait Destination LUT ready 1
Wait send destination word
Wait send module header
Missing module search
Wait sample and send trailer1
Wait sample and send trailer2
Wait sample and send trailer3
Wait sample and send trailer4
Wait sample and send trailer5 (EOF)
else


Frame Data
Ctrl / Data Valid
RX Enable
SLINK
Packer x 34
SLINK Data
34 lanes
Module data
From 32 lanes
DF output
preparation
x 32
state machine to
do the following:
• To remove the destination bit for 32 boards (The modules are already in the final destination and not needed)
• To add the destination words corresponds to the FTK plane and FTK tower
Switch 32 x 32
32-lane
input
Tower1
AUX (8)
Duplicator
SSB (1)
Tower2
AUX (8)
SSB (1)
Note :
The SSB output could be increased twice more.
Since the destination bit according to the ftk plane will be assigned in the output preparation, the following modification is needed for both towers and both Pixel and SCT data
next_output_data(15) <= or_reduce(sctmod2ftkplane_lut_data_i(11 downto 8));
next_output_data(14) <= sctmod2ftkplane_lut_data_i(8);
next_output_data(15) <= or_reduce(sctmod2ftkplane_lut_data_i(11 downto 9));
”

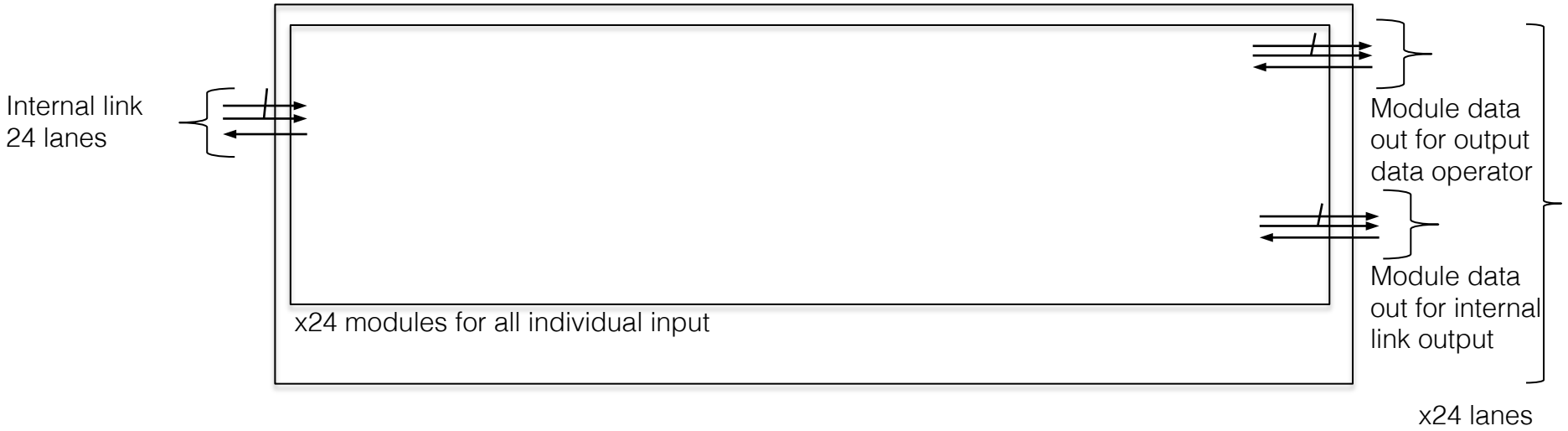

module for
current event
module for too
early event
current event ID
8k words / lane
module for
current event
module for too
early event


Internal link interface
Transceiver
BERT pattern Ge
TX input buffer
TX state machine
TX_DATA [31:0]
TX_DVALID
TX_RDY
GT_TXDATA [31:0]
GT_TXCHARISK [31:0]
TX_ENABLE (idle mode if '0')
TX_URL [3:0]
TX_LOCK
Note : lock signal is propagated from the other side
RX state machine
RX_LOCK
RX_LRL [3:0]
RX_ERROR
GT_RXENCOMMAALIGN fixed to be '1'
RX_DATA [31:0]
RX_DVALID
RX_BUSY
RX output buffer
PROG Full
GT_TXDATA [31:0]
GT_TXCHARISK [31:0]
BERT pattern checker
Main clock domain
GT user clock (TX/RX) clock domain

Internal link output



Internal link input



Routing table description

¶ 89 Each column in the routing table depict Logical Slot positions. There are fifteen Fabric Channels per Slot each represented by a cell in the table. Each cell within the table represents a Fabric Channel and the numbers within the cell represent the destination end-point to which that Channel is routed. For example, the cell representing Channel 1 of Slot 9 contains the value (1–8) to indicate it is connected to Slot 1, Channel 8. This method to describe routing destinations per Channel is used for all routing assignment tables in this specification.

Table 6-11 Full Mesh Backplane routing assignments

	Logical Slot #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Connector	Channel #																
P20	15	16-1	16-2	16-3	16-4	16-5	16-6	16-7	16-8	16-9	16-10	16-11	16-12	16-13	16-14	16-15	15-15
P20	14	15-1	15-2	15-3	15-4	15-5	15-6	15-7	15-8	15-9	15-10	15-11	15-12	15-13	15-14	14-14	14-15
P20	13	14-1	14-2	14-3	14-4	14-5	14-6	14-7	14-8	14-9	14-10	14-11	14-12	14-13	13-13	13-14	13-15
P21	12	13-1	13-2	13-3	13-4	13-5	13-6	13-7	13-8	13-9	13-10	13-11	13-12	12-12	12-13	12-14	12-15
P21	11	12-1	12-2	12-3	12-4	12-5	12-6	12-7	12-8	12-9	12-10	12-11	11-11	11-12	11-13	11-14	11-15
P21	10	11-1	11-2	11-3	11-4	11-5	11-6	11-7	11-8	11-9	11-10	10-10	10-11	10-12	10-13	10-14	10-15
P21	9	10-1	10-2	10-3	10-4	10-5	10-6	10-7	10-8	10-9	9-9	9-10	9-11	9-12	9-13	9-14	9-15
P21	8	9-1	9-2	9-3	9-4	9-5	9-6	9-7	9-8	8-8	8-9	8-10	8-11	8-12	8-13	8-14	8-15
P22	7	8-1	8-2	8-3	8-4	8-5	8-6	8-7	7-7	7-8	7-9	7-10	7-11	7-12	7-13	7-14	7-15
P22	6	7-1	7-2	7-3	7-4	7-5	7-6	6-6	6-7	6-8	6-9	6-10	6-11	6-12	6-13	6-14	6-15
P22	5	6-1	6-2	6-3	6-4	6-5	5-5	5-6	5-7	5-8	5-9	5-10	5-11	5-12	5-13	5-14	5-15
P22	4	5-1	5-2	5-3	5-4	4-4	4-5	4-6	4-7	4-8	4-9	4-10	4-11	4-12	4-13	4-14	4-15
P22	3	4-1	4-2	4-3	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	3-12	3-13	3-14	3-15
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13	1-14	1-15

NOTE: The shading used in Table 6-11, “Full Mesh Backplane routing assignments,” shows discontinuity of the routing sequence across rows and columns in the table.

ATCA ch	Type	ID	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	NOTE 2	Categoly	GT ID	GT ch	LSC ch	Internal Link	RX FLIP	TX FLIP
J32P19	QSFP+	T1	Ch0	218	1	0	33	217	U27	AUX T0	SLINK	RTM LEFT	gt33	0	0			
J32P18	QSFP+	T1	Ch1	218	0	0	32	217				RTM LEFT	gt32	1	1			
J32P17	QSFP+	T1	Ch2	217	3	0	31	217				RTM LEFT	gt31	2	2			
J32P16	QSFP+	T1	Ch3	217	2	0	30	217				RTM LEFT	gt30	3	3			
J32P15	QSFP+	T2	Ch0	217	1	0	29	217		AUX T1		RTM LEFT	gt29	4	4			
J32P14	QSFP+	T2	Ch1	217	0	0	28	217				RTM LEFT	gt28	5	5			
J32P13	QSFP+	T2	Ch2	216	3	0	27	217				RTM LEFT	gt27	6	6			
J32P12	QSFP+	T2	Ch3	216	2	0	26	217				RTM LEFT	gt26	7	7			
J32P11	QSFP+	T3	Ch0	216	1	0	25	217		AUX T2		RTM LEFT	gt25	8	8			
J32P10	QSFP+	T3	Ch1	216	0	0	24	217				RTM LEFT	**gt24**	9	9			
J32P9	QSFP+	T3	Ch2	215	3	0	23	214				RTM LEFT	gt23	10	10			
J32P8	QSFP+	T3	Ch3	215	2	0	22	214				RTM LEFT	gt22	11	11			
J32P7	QSFP+	T4	Ch0	215	1	0	21	214		AUX T3		RTM LEFT	gt21	12	12			
J32P6	QSFP+	T4	Ch1	215	0	0	20	214				RTM LEFT	gt20	13	13			
J32P5	QSFP+	T4	Ch2	214	3	0	19	214				RTM LEFT	gt19	14	14			
J32P4	QSFP+	T4	Ch3	214	2	0	18	214				RTM LEFT	gt18	15	15			
J32P3	SFP+	T5		214	1	0	17	214		SSB T		RTM LEFT	gt17	16	16			
J32P2	SFP+	T6		214	0	0	16	214		Internal Link Ch0 P0		RTM LEFT	gt16	41		7	**RX**	
J32P1	SFP+	T7		213	3	0	15	214		Internal Link Ch0 P1		RTM LEFT	gt15	50		16		
J32P0	N/A			213	2	0	14	214		-	-	-	gt14					

ATCA ch	Type	ID	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	NOTE 2	Categoly	GT ID				RX FLIP	TX FLIP
J33P19	QSFP+	T1	Ch0	213	1	0	13	214	U27	AUX B0	SLINK	RTM LEFT	gt13	17	17			
J33P18	QSFP+	T1	Ch1	213	0	0	12	214				RTM LEFT	**gt12**	18	18			
J33P17	QSFP+	T1	Ch2	212	3	0	11	211				RTM LEFT	gt11	19	19			**TX**
J33P16	QSFP+	T1	Ch3	212	2	0	10	211				RTM LEFT	gt10	20	20		**RX**	
J33P15	QSFP+	T2	Ch0	212	1	0	9	211		AUX B1		RTM LEFT	gt9	21	21			
J33P14	QSFP+	T2	Ch1	212	0	0	8	211				RTM LEFT	gt8	22	22			
J33P13	QSFP+	T2	Ch2	211	3	0	7	211				RTM LEFT	gt7	23	23			
J33P12	QSFP+	T2	Ch3	211	2	0	6	211				RTM LEFT	gt6	24	24			**TX**
J33P11	QSFP+	T3	Ch0	211	1	0	5	211		AUX B2		RTM LEFT	gt5	25	25			
J33P10	QSFP+	T3	Ch1	211	0	0	4	211				RTM LEFT	gt4	26	26			
J33P9	QSFP+	T3	Ch2	210	3	0	3	211				RTM LEFT	gt3	27	27			
J33P8	QSFP+	T3	Ch3	210	2	0	2	211				RTM LEFT	gt2	28	28			
J33P7	QSFP+	T4	Ch0	210	1	0	1	211		AUX B3		RTM LEFT	gt1	29	29			
J33P6	QSFP+	T4	Ch1	210	0	0	0	211				RTM LEFT	**gt0**	30	30			
J33P5	QSFP+	T4	Ch2	110	0	1	0	110				RTM RIGHT	gt0	31	31		**RX**	**TX**
J33P4	QSFP+	T4	Ch3	110	1	1	1	110				RTM RIGHT	gt1	32	32		**RX**	**TX**
J33P3	SFP+	T5		110	2	1	2	110		SSB B		RTM RIGHT	gt2	33	33		**RX**	**TX**
J33P2	SFP+	T6		110	3	1	3	110		Internal Link Ch1 P0		RTM RIGHT	gt3	42		8	**RX**	**TX**
J33P1	SFP+	T7		111	0	1	4	110		Internal Link Ch1 P1		RTM RIGHT	gt4	51		17		**TX**
J33P0	N/A			111	1	1	5	110		-	-	-	gt5					

Fabric	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	Categoly	GT ID	GT ch	Internal Link	RX FLIP	TX FLIP
C13	P1	111	2	1	6	110	U27	-	NOT USED					**TX**
C13	P0	111	3	1	7	110		-	NOT USED					
C12	P1	112	0	1	8	112	U11	Internal link	Fabric	**gt0**				
C12	P0	112	1	1	9	112			Fabric	gt1				
C11	P1	112	2	1	10	112			Fabric	gt2				
C11	P0	112	3	1	11	112			Fabric	gt3				
C10	P1	113	0	1	12	112			Fabric	gt4				
C10	P0	113	1	1	13	112			Fabric	gt5				
C9	P1	113	2	1	14	112			Fabric	gt6	49	15		
C9	P0	113	3	1	15	112			Fabric	gt7	40	6		
C8	P1	114	0	1	16	115			Fabric	**gt8**	48	14		
C8	P0	114	1	1	17	115			Fabric	gt9	39	5		
C7	P1	114	2	1	18	115			Fabric	gt10	47	13		
C7	P0	114	3	1	19	115			Fabric	gt11	38	4	**RX**	
C6	P1	115	0	1	20	115			Fabric	gt12	46	12		
C6	P0	115	1	1	21	115			Fabric	gt13	37	3		
C5	P1	115	2	1	22	115			Fabric	gt14	45	11		
C5	P0	115	3	1	23	115			Fabric	gt15	36	2		
C4	P1	116	0	1	24	115			Fabric	gt16	44	10		
C4	P0	116	1	1	25	115			Fabric	gt17	35	1		
C3	P1	116	2	1	26	115			Fabric	gt18	43	9		
C3	P0	116	3	1	27	115			Fabric	gt19	34	0		
C2	P1	117	**1**	1	**29**	118		HUB						
C2	P0	117	**0**	1	**28**	118		HUB						
C1	P3	117	2	1	30	118		HUB						
C1	P2	117	3	1	31	118		HUB						
C1	P1	118	0	1	32	118		HUB						
C1	P0	118	1	1	33	118		IP Bus	1000BASE-T	gt0				

FMC	GP	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE	FTK IM	Channel			RX FLP	TX FLP
3	0	118	2	1	34	118	U11	Shared with IPBus	3	0			**RX**	
3	1	118	3	1	35	118		Shared with IPBus	3	1				
3	2	119	0	1	36	118				N/C				
4	0	119	1	1	37	118			4	0			**RX**	**TX**
4	1	119	2	1	38	118			4	1			**TX**	
4	2	119	3	1	39	118				N/C				**TX**

2	2	218	2	0	34	217	U11	Shared with RTM		N/C				
2	1	218	3	0	35	217		Shared with RTM	2	1				**TX**
2	0	219	0	0	36	219			2	0				
1	2	219	1	0	37	219				N/C			**RX**	
1	1	219	2	0	38	219			1	1			**RX**	
1	0	219	3	0	39	219			1	1			**RX**	**TX**