Data Formatter Firmware Design Note

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Abstract

1 Introduction

This documentation describes the design of the Data Formatter Firmware. The development log of DF FW is stored in: `https://its.cern.ch/jira/browse/FTKHWD-119`. This version of documentation also summarizes the change of DF FW version change from 18000 to 18022.

2 Changes included in this version of note

1. Re-assignment of tower to DF boards to satisfy the requirement from SSB-FLIC so that each DF board outputs two adjacent η towers.
2. Increase of FW speed from 150 MHz to 200 MHz
3. Implementation of automatic FMC delay value setting
4. Automatic retrieval of IP and MAC address using EFUSE USR register
5. Addition of SLINK output for SSB and implementation of QSFP link for inter-crate DF communication and DF-SSB communication
6. Dual SLINK output packer structure to improve data formatter speed
7. SLINK module completion time-out in case of packets loss/corruption in incoming module data or inter-board communication without affecting dataflow
8. FMC input b0f time-out in case the ID goes busy for a short period of time to disable certain IM input channels without affecting dataflow
9. Majority L1ID out-of-sync monitoring
10. FMC input re-sync functionality (to be validated in data) designed to re-enable input channels b0f timed-out

3 32 board allocation and numbering

Table 1, 2, 3 and 4 show DF boards allocation and numbering in USA 15.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination
		Shelf	Slot	Tower ID	Position	Tower ID	Position	
0	0x00000001	1	3	2	C E phi1	18	C B phi1	Shelf 3 - Slot 6
4	0x00000010	1	4	3	C E phi2	19	C B phi2	Shelf 4 - Slot 8
8	0x00000100	1	5	34	A B phi1	50	A E phi1	Shelf 4 - Slot 9
12	0x00001000	1	6	35	A B phi2	51	A E phi2	Shelf 4 - Slot 10
16	0x00010000	1	7	4	C E phi3	20	C B phi3	Shelf 2 - Slot 3
20	0x00100000	1	8	5	C E phi4	21	C B phi4	Shelf 2 - Slot 4
24	0x01000000	1	9	36	A B phi3	52	A E phi3	Shelf 2 - Slot 5
28	0x10000000	1	10	37	A B phi4	53	A E phi4	Shelf 2 - Slot 6

Table 1: Shelf 1.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination
		Shelf	Slot	Tower ID	Position	Tower ID	Position	
1	0x00000002	2	3	6	C E phi5	22	C B phi5	Shelf 1 - Slot 7
5	0x00000020	2	4	7	C B phi5	23	C B phi6	Shelf 1 - Slot 8
9	0x00000200	2	5	38	A B phi5	54	A E phi5	Shelf 1 - Slot 9
13	0x00002000	2	6	39	A B phi6	55	A E phi6	Shelf 1 - Slot 10
17	0x00020000	2	7	8	C E phi7	24	C B phi7	Shelf 3 - Slot 3
21	0x00200000	2	8	9	C B phi7	25	C B phi8	Shelf 3 - Slot 4
25	0x02000000	2	9	40	A B phi7	56	A E phi7	Shelf 3 - Slot 5
29	0x20000000	2	10	41	A B phi8	57	A E phi8	Shelf 4 - Slot 7

Table 2: Shelf 2.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination
		Shelf	Slot	Tower ID	Position	Tower ID	Position	Link 1
2	0x00000004	3	3	10	C E phi9	26	C B phi9	Shelf 2 - Slot 7
6	0x00000040	3	4	11	C E phi10	27	C B phi10	Shelf 2 - Slot 8
10	0x00000400	3	5	42	A B phi9	58	A E phi9	Shelf 2 - Slot 9
14	0x00004000	3	6	43	A B phi10	59	A E phi10	Shelf 1 - Slot 6
18	0x00040000	3	7	12	C E phi11	28	C B phi11	Shelf 4 - Slot 3
22	0x00400000	3	8	13	C E phi12	29	C B phi12	Shelf 4 - Slot 4
26	0x04000000	3	9	44	A B phi11	60	A E phi11	Shelf 4 - Slot 5
30	0x40000000	3	10	45	A B phi12	61	A E phi12	Shelf 4 - Slot 6

Table 3: Shelf 3.

Table 4: Shelf 4.

Board ID	bit mask	location		destination 1		destination 2		inter-crate link destination
		Shelf	Slot	Tower ID	Position	Tower ID	Position	Link 1
3	0x00000008	4	3	14	C E phi13	30	C E phi14	Shelf 3 - Slot 7
7	0x00000080	4	4	15	C E phi14	31	C B phi14	Shelf 3 - Slot 8
11	0x00000800	4	5	46	A B phi13	62	A B phi14	Shelf 3 - Slot 9
15	0x00008000	4	6	47	A B phi14	63	A E phi14	Shelf 3 - Slot 10
20	0x00080000	4	7	0	C E phi15	16	C B phi15	Shelf 2 - Slot 10
24	0x00800000	4	8	1	C E phi0	17	C B phi0	Shelf 1 - Slot 4
27	0x08000000	4	9	32	A B phi15	48	A E phi15	Shelf 1 - Slot 5
31	0x80000000	4	10	33	A B phi0	49	A E phi0	Shelf 3 - Slot 6

4 Overview of the firmware

The DF FW has three main blocks: the main logic, the transceiver and the user interface. The main logic is where the input packets get their destination defined and routed properly. The transceiver is the block that handels the SLINK connections to downstream boards as well as the internal link connections among DFs. The user interfaces defines the logic DF communicating to PC through IPBus and includes the monitoring/config registers. The FW diagram is shown in Fig. 1

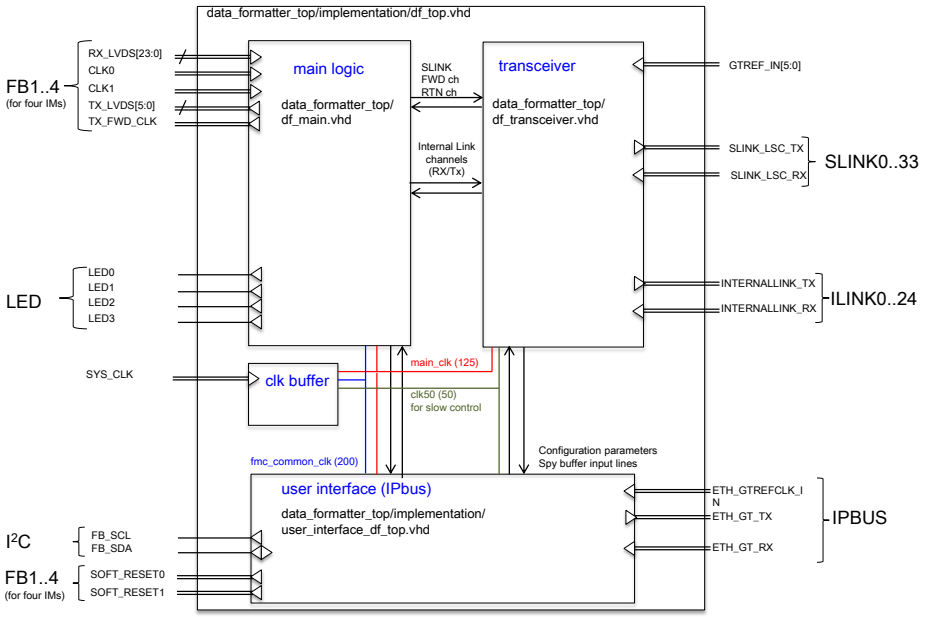

Figure 1: Firmware overview.

5 Main logic

The main logic reads the input data from IM boards through FMC interface and stripps of the event headers and trailers and determines the module destination through Input Data Operater (IDO). The headers and trailers are then sent directly to Output Data Operator (ODO), while the modules depending on their destination goes directly to ODO or through Internal Link Input (ILI) and Internal Link Output (ILO) to another DF board. The FW diagram is shown in Fig. 2. Detailed description of each module is presented in the subsections of this section.

- FMC interface : `data_formatter_top/df_fmc_interface.vhd`
- Input Data Operator : `data_formatter_top/df_input_data_operator.vhd`
- Output Data Operator : `data_formatter_top/df_output_data_operator_v2.vhd`
- Internal Link Input : `data_formatter_top/df_internallink_input.vhd`
- Internal Link Output : `data_formatter_top/df_internallink_output.vhd`

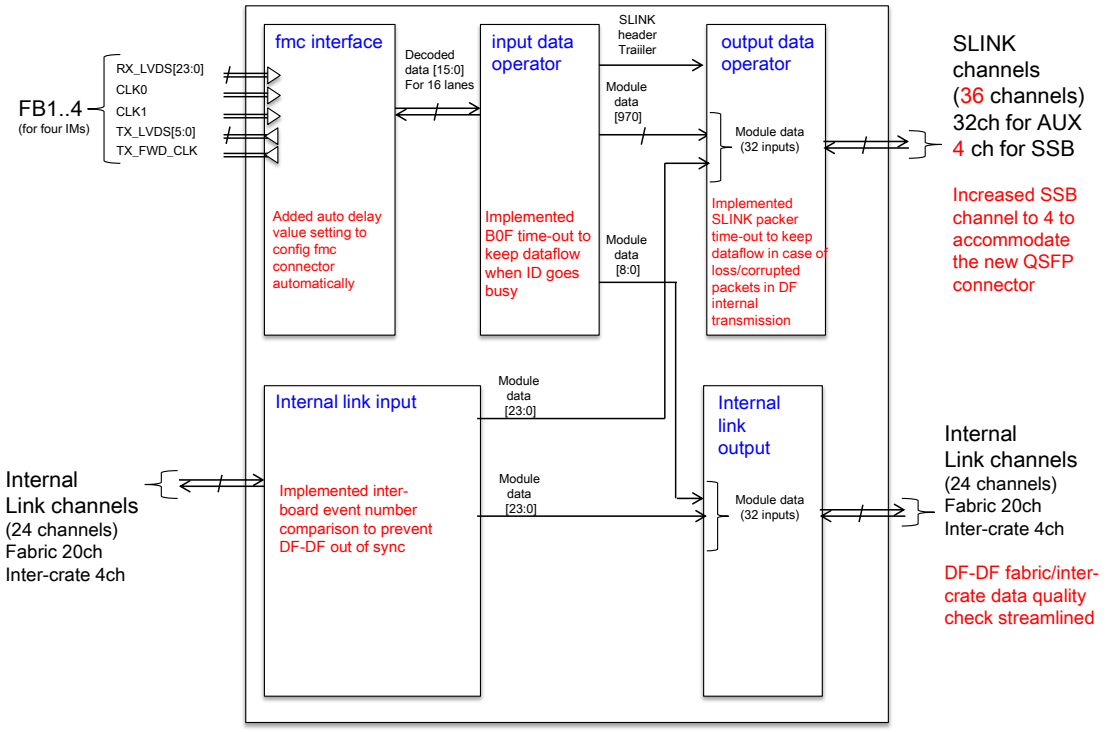

Figure 2: Main logic overview.

5.1 FMC interface

The FMC interface has two maps Input Mapper and Mapper which map the data from FMC links to pre-defined DF input channels splitted into IBL/PIX/SCT lanes. The Front logic then decodes the serial data to form 32 bits data words. FMC TX Interface sends back "HOLD", "RESET" and "FREEZE" signal to IM.

To establish good phase value for FMC connecter, the Pattern Checker checks on incoming idle words in DF config stage to make sure on the correct idle words (4 different kinds) are reconstructed correctly over a period of 0.1s per channel corresponding to BER=$10e-8$.

The FMC interface diagram is shown in Fig. 3

- Input mapper : `pulsar2_fmc_interface/fmc_rx_mapper_fmc_to_fpga.vhd`
- Front : `pulsar2_fmc_interface/fmc_rx_front.vhd`
- Mapper : `pulsar2_fmc_interface/fmc_rx_mapper_fpga_to_detword.vhd`
- Frame : `pulsar2_fmc_interface/fmc_rx_frame.vhd`
- Pattern Checker : `pulsar2_fmc_interface/fmc_rx_data_checker_v3.vhd`
- Elasitc Buffer : `fmc_input_buffer/fmc_input_buffer.vhd`
- FMC TX Interface : `pulsar2_fmc_interface/fmc_tx_interface.vhd`

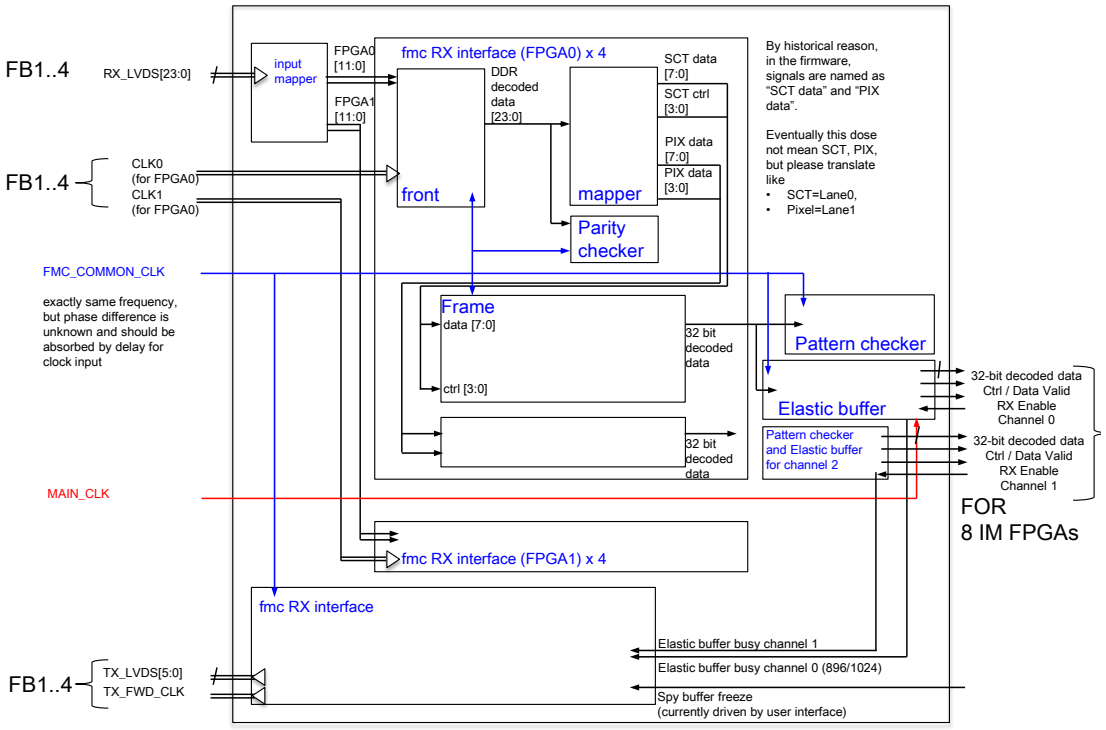

Figure 3: FMC interface firmware overview.

5.2 Input data operator

The IDO (logic shown in Fig. 5) connects to ODO and ILO. This FW block strips off the headers and trailers of incoming data (of the first enabled IM channel) sending them through express lane to ODO. The module data goes through a state machine diagrammed in Fig. 6 for the FW to add on DF internal processing data words (Fig. 4) and to determine its proper destination. Depending on the destination board of the module would either go directly to the ODO of the current DF board, or will be sent through ILO to another DF.

A number of special functionalities are implemented to stablize the dataflow in extreme conditions of ID.

- **L1ID out of sync monitoring:** DF implements a seeded majority check of L1ID across all input channels. The seed L1ID is initialized as the first L1ID we receive from the first enabled channel. Then for the subsequent events, we first compare L1ID from all channels to the seed. If we see at least one channel has L1ID that is +1 of the seed, then the seed is incremented. Else if we see at least one channel that sees an ECR then the seed would be set to the ECR. After the seed is determined by all channels, we compare the seed against all L1IDs received and determine which lanes are out of sync. Note the L1ID out of sync monitoring is only for monitoring purpose. We do not disable input channels because of L1ID out of sync. The code is implemented in `pulsar2_df_internal_decoder/df_input_handler.vhd`

- **b0f time-out:** As shown in Fig. 6, all input channels are required to be synced at the state "WAIT CHECK HEADER 0 AND SEND DF HEADER". If one of the enabled channels do not finish the previous event, the signal "ready_to_see_next_event" stays

at 0 and hecne all channels are stalled. This design ensures the DF is synced at the input level, while it is not robust against the scenario that a few ID channels going busy and not sending FTK data. Therefore, we inplement a b0f time-out scheme such that we maintain a counter that counts the number of clock cycles since the first channel receivng the "b0f". If the counter surpasses a threshold, the channels which have not yet received the "b0f" word would be disabled and the ones do will proceed on with the next event. The code is implemented in `pulsar2_df_internal_decoder/add_df_internalframe.vhd`

- **b0f resync:** If a particular input channel is timed-out, we make an attempt to resync it. Once we see a "b0f" word again from the disabled channel, we enter a "loop" mode re-enabling and spying on the channel without sending the input data downstream. We start re-processing the channel once we see an ECR that is synchronized with other input channels. The code is implemented in `pulsar2_df_internal_decoder/add_df_internalframe.vhd`. NOTE: THIS FUNCTIONALITY HASN'T BEEN FULLY TESTED YET.

- Input lane handler : `pulsar2_df_internal_decoder/df_input_handler.vhd`
- Internal frame adder : `pulsar2_df_internal_decoder/add_df_internalframe.vhd`
- SWITCH : `pulsar2_df_switch/df_switch_element_v3.vhd`

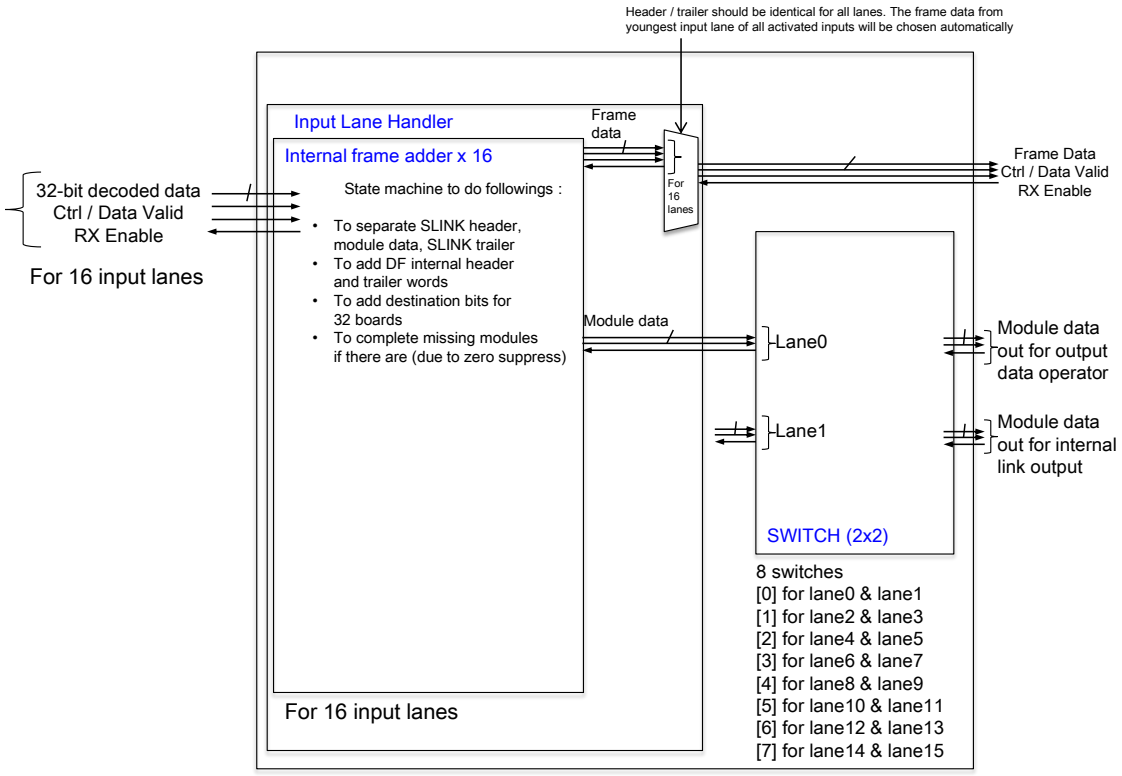

Figure 4: Internal data operator. One modules have three additional words, header, destination words and trailer.

Original module data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
1	**0**	**0**	**0**	Reserved				Reserved				Reserved				**0**	Reserved			R	Pixel module number (10..0)											Pixel Module Header
0	Column width			Column coordinate (27..16)												S	Row width			Row coordinate (11..0)												Pixel Cluster
1	**0**	**0**	**0**	Reserved				Reserved				Reserved				**1**	Reserved			SCT module number (12..0)												SCT Module Header
0	Hit 2 Width			hit2 empty	Hit 2 coordinate (26..16)											R	Hit1 width			R	Hit 1 coordinate (10..0)											SCT Cluster

Note

* If the second SCT hit is empty, the empty= '1'
* "R" means
Reserved
* "S" means Split Cluster Bit

Data formatter internal data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	F/T	Reserved							Random Counter					DF internal Event Counter (from 0 - 255)															
Global destination bits for 32 slots																															
Module DATA																															
1	1	1	0	Reserved																											

NOTE: F/T shows the modules data is fake data only inside of the DF for event synchronization (this is case of "F"='1') or not ("T"='0'). Fake data will be removed in output data
NOTE: Random 4 bit counter is reserved to randamize the switching destination in CENTRAL SWITCH so that the efficiency of switching resource use will be maximized

Special format adding internal link output lanes

(the “global destination bit” is treated as part of “module data” in switch firmware)

3) Local Switching data format (inside internal link switch)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	F/T	Reserved							Random Counter					DF internal Event Counter (from 0 - 255)															
Local output port information (should be single destination packet)																															
Global destination bit for 32 slots (SHOULD BE A SINGLE DESTINATION PACKET DATA)																															
Module DATA																															
1	1	1	0	Reserved																											

NOTE: This DF firmware will miss channel #13 of fabric on purpose to form the input lane number to be 32

Output with 16-bit is determined with the following equation:

- Reference index = (32 + Lane ID – Random Counter) mod 32
- For random counter = 0 case

The original global destination bit is treated as one of normal module words. Note switch firmware only will category,
(1) DF header (fragment ID=“110X”), (2) Destination bit (following DF header), and (3) DF trailer (fragment ID=“1110”)

Figure 5: Input data operator firmware overview.

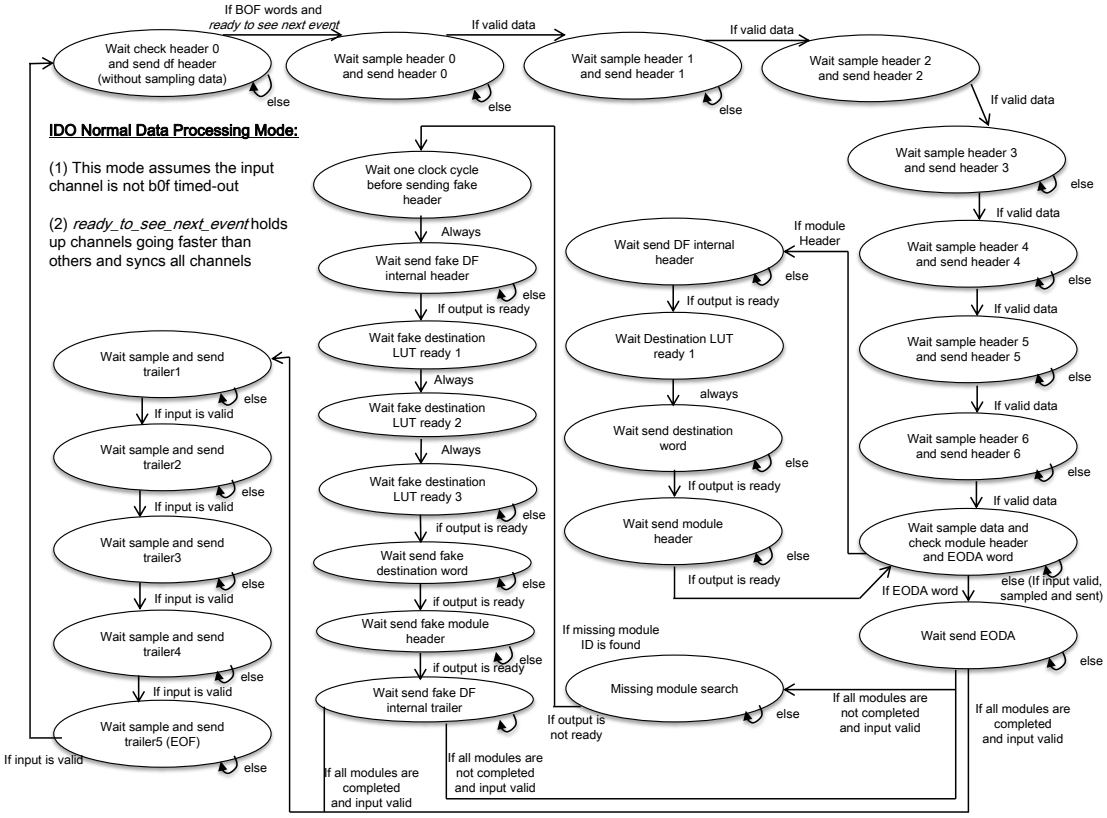

Figure 6: State machine in Internal frame adder for normal processing modes.

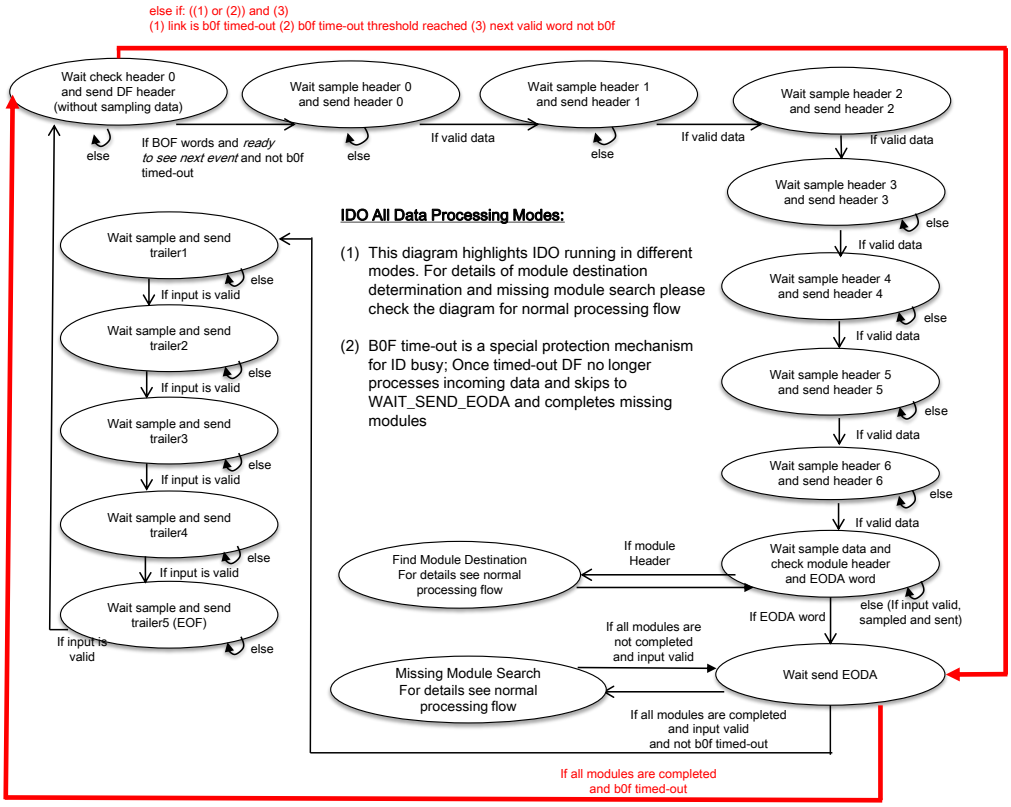

Figure 7: State machine in Internal frame adder for different processing modes.

5.3 Output data operator

The ODO (logic shown in Fig. 8) connects to ILI and IDO. This FW block gathers module data from all DFs should be routed to one of the destination towers the board is associated with. The DF Output Preparation (has switch in it) block will route the module based on the layer number to the proper SLINK channel. SLINK Packer shown in Fig. 9 and 10 holds the module data in circular buffers. If the module is too early for the current event, it is looped in the circular buffer.

- DF Output Preparation : `pulsar2_df_internal_decoder/df_output_preparation_v2.vhd`
- Switch 32 x 32 : `pulsar2_df_switch/df_switch_matrix_32x32.vhd`
- SLINK Packer : `pulsar2_df_internal_decoder/df_output_slink_packer_v2.vhd`

lane	description	
	type	channel
0	IM	ch0 and ch1
1	Fabric	ch3 p0
2	Fabric	ch4 p0
3	Fabric	ch5 p0
4	IM	ch2 and ch3
5	Fabric	ch6 p0
6	Fabric	ch7 p0
7	Fabric	ch8 p0
8	IM	ch4 and ch5
9	Fabric	ch9 po0
10	Fabric	ch10 p0
11	Fabric	ch11 p0
12	IM	ch6 and ch7
13	Fabric	ch12 p0
14	Inter-crate	ch0 p0
15	Inter-crate	ch1 p0

lane	description	
	type	channel
16	IM	ch8 and ch9
17	Fabric	ch3 p1
18	Fabric	ch4 p1
19	Fabric	ch5 p1
20	IM	ch10 and ch11
21	Fabric	ch6 p1
22	Fabric	ch7 p1
23	Fabric	ch8 p1
24	IM	ch12 and ch13
25	Fabric	ch9 p1
26	Fabric	ch10 p1
27	Fabric	ch11 p1
28	IM	ch14 and ch15
29	Fabric	ch12 p1
30	Inter-crate	ch0 p1
31	Inter-crate	ch1 p1

Table 5: Input channel assignment for output data operator module. Defined in "MAPPING_CONF_IDO2ODO" and "MAPPING_CONF_ILI2ODO" in data_formatter_top/data_formatter_constants.vhd.

lane	description	
	type	channel
0	AUX0 Tower 0	ch0
1	AUX0 Tower 0	ch1
2	AUX0 Tower 0	ch2
3	AUX0 Tower 0	ch3
4	AUX1 Tower 0	ch4
5	AUX1 Tower 0	ch5
6	AUX1 Tower 0	ch6
7	AUX1 Tower 0	ch7
8	AUX2 Tower 0	ch0
9	AUX2 Tower 0	ch1
10	AUX2 Tower 0	ch2
11	AUX2 Tower 0	ch3
12	AUX3 Tower 0	ch4
13	AUX3 Tower 0	ch5
14	AUX3 Tower 0	ch6
15	AUX3 Tower 0	ch7
16	SSB Tower 0	

lane	description	
	type	channel
17	AUX0 Tower 1	ch0
18	AUX0 Tower 1	ch1
19	AUX0 Tower 1	ch2
20	AUX0 Tower 1	ch3
21	AUX1 Tower 1	ch4
22	AUX1 Tower 1	ch5
23	AUX1 Tower 1	ch6
24	AUX1 Tower 1	ch7
25	AUX2 Tower 1	ch0
26	AUX2 Tower 1	ch1
27	AUX2 Tower 1	ch2
28	AUX2 Tower1	ch3
29	AUX3 Tower1	ch4
30	AUX3 Tower1	ch5
31	AUX3 Tower1	ch6
32	AUX3 Tower 1	ch7
33	SSB Tower 1	

Table 6: SLINK output channel assignment (34 channel). "MAPPING_CONF_SLINKOUT2GTLOC" and "MAPPING_CONF_SLINKOUT2GTLOC" in data_formatter_top/data_formatter_constants.vhd.

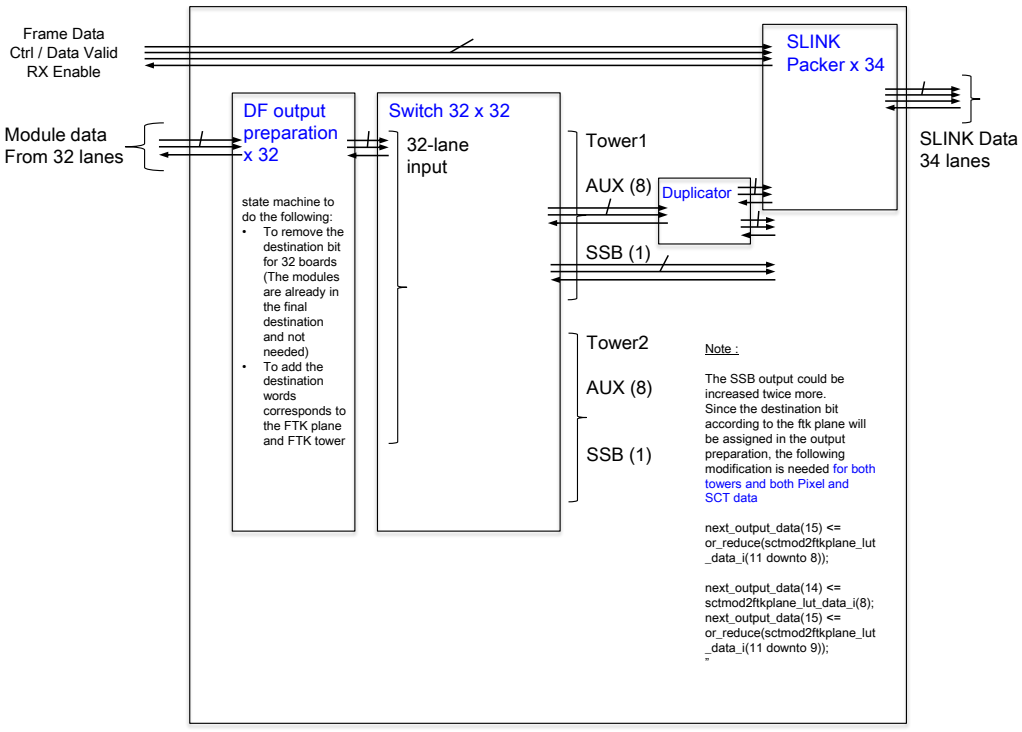

Figure 8: Output data operator firmware overview.

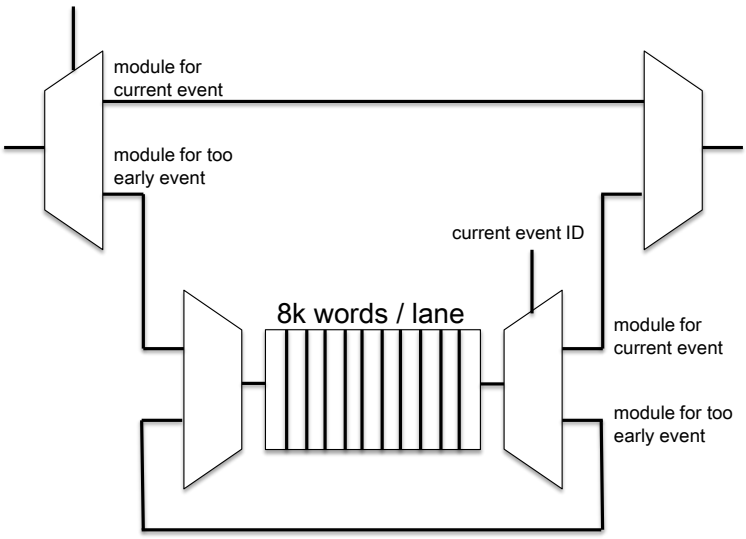

Figure 9: Schematics of the early design of individual event sorting buffer in the SLINK packer. In the current design of DF FW, we have two event sorting buffers for each of the output lane for sorting odd and even numbered events separetely to increase the processing speed. Each sorting buffer is of 4K word size.

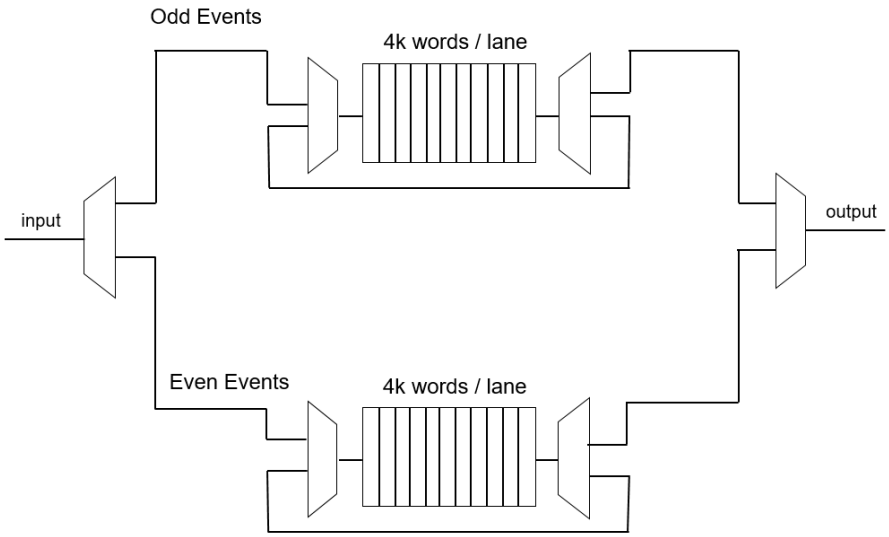

Figure 10: Schematics of the current design of individual event sorting buffer in the SLINK packer. The current design strips off the express lane for modules of the current to save FW resources.

5.4 Internal link input / output

The ILI and ILO (12) are blocks for DF-DF communication. The ILO has two 32x32 switches. The first one is CW (central switch) which spreads out the traffic by randomly routing the modules based on the random counter they receive in IDO. The second switch then routes the module to the proper trasceiver. ILI connected to another board's ILO will determine if the module goes out from the current board or needs to be routed again. Hence the ILI connects ODO as well as ILO.

It is a good exercise for the reader given the information of the DF-DF connection in Tab. 1,2,3,4 to reach the same conclusion as the authors that the there are three different data sharing patterns as show in Fig.13. In practice, the bottle-neck of DF processing is coming from the ODO circular buffer, which origninates from the fact that modules from old and new events need to be cycled through the buffer before an event can be completed. To minimize the overlapping of old and new events, we need to minimize amount of module data being shared in between DFs. A good heruistic is to optimizatize the DF cabling reduce the total path cost of all modules being routed in the DF system. As of how this is done in code level is beyond the scope of this note, please contact Zihao directly for more information.

The internal link interface (Fig. 11) implements a DF-DF sync scheme. By checking the DF internal event numbers of the incoming events, the destination board determines if it is processing ahead more than 2 events the source board does. The scheme is enforced by the idle words which contain the DF internal current event ID counter sent every 128 cycles (Table. 5.4).

- Internal link interface : `pulsar2_df_internal_link/ilink_interface_v2.vhd`
- Bit Error Rate Test (BERT) pattern generator : `pulsar2_df_internal_link/pattern_gen.vhd`
- Bit Error Rate Test (BERT) pattern checker : `pulsar2_df_internal_link/pattern_chk.vhd`

lane	description	
	type	channel
0	IM	ch0 and ch1
1	Fabric	ch3 p0
2	Fabric	ch4 p0
3	Fabric	ch5 p0
4	IM	ch2 and ch3
5	Fabric	ch6 p0
6	Fabric	ch7 p0
7	Fabric	ch8 p0
8	IM	ch4 and ch5
9	Fabric	ch9 po0
10	Fabric	ch10 p0
11	Fabric	ch11 p0
12	IM	ch6 and ch7
13	Fabric	ch12 p0
14	Inter-crate	ch0 p0
15	Inter-crate	ch1 p0

lane	description	
	type	channel
16	IM	ch8 and ch9
17	Fabric	ch3 p1
18	Fabric	ch4 p1
19	Fabric	ch5 p1
20	IM	ch10 and ch11
21	Fabric	ch6 p1
22	Fabric	ch7 p1
23	Fabric	ch8 p1
24	IM	ch12 and ch13
25	Fabric	ch9 p1
26	Fabric	ch10 p1
27	Fabric	ch11 p1
28	IM	ch14 and ch15
29	Fabric	ch12 p1
30	Inter-crate	ch0 p1
31	Inter-crate	ch1 p1

Table 7: Input channel assignment for internal data output module (i.e. input of Central Switch.). Defined in "MAPPING_CONF_IDO2ILO" and "MAPPING_CONF_ILI2ILO" in data_formatter_top/data_formatter_constants.vhd.

lane	description	
	type	channel
0	Fabric	ch3 p0
1	Fabric	ch4 p0
2	Fabric	ch5 p0
3	Fabric	ch6 p0
4	Fabric	ch7 p0
5	Fabric	ch8 p0
6	Fabric	ch9 p0
7	Fabric	ch10 p0
8	Fabric	ch11 p0
9	Fabric	ch12 p0
10	Internal link	ch0 p0
11	Internal link	ch1 p0

lane	description	
	type	channel
12	Fabric	ch3 p1
13	Fabric	ch4 p1
14	Fabric	ch5 p1
15	Fabric	ch6 p1
16	Fabric	ch7 p1
17	Fabric	ch8 p1
18	Fabric	ch9 p1
19	Fabric	ch10 p1
20	Fabric	ch11 p1
21	Fabric	ch12 p1
22	Internal link	ch0 p1
23	Internal link	ch1 p1

Table 8: Internal link channel assignment. Defined in "MAPPING_CONF_INTERNALLINK2GTCHANNEL" and "MAPPING_CONF_INTERNALLINK2GTLOC" in data_formatter_top/data_formatter_constants.vhd.

31:0
$K23.7\&K23.7\&K23.7\&K23.7$

Table 9: Pad-word definition. It will be inserted in the interface (TX side) every 128-word cycle, and removed in the interface (RX side) in The isKCharctor word is 1111. This is for RX clock correction functionality.

31:24	23:16	15:13	12	11:8	7:0
$D5.6$	00 Current Event ID	Reserved	XOFF	Return Channel 4 bit	$K28.5$

Table 10: idle word definition. At least it will be inserted in the interface every 128-word cycle. The isKCharctor word is 0001.

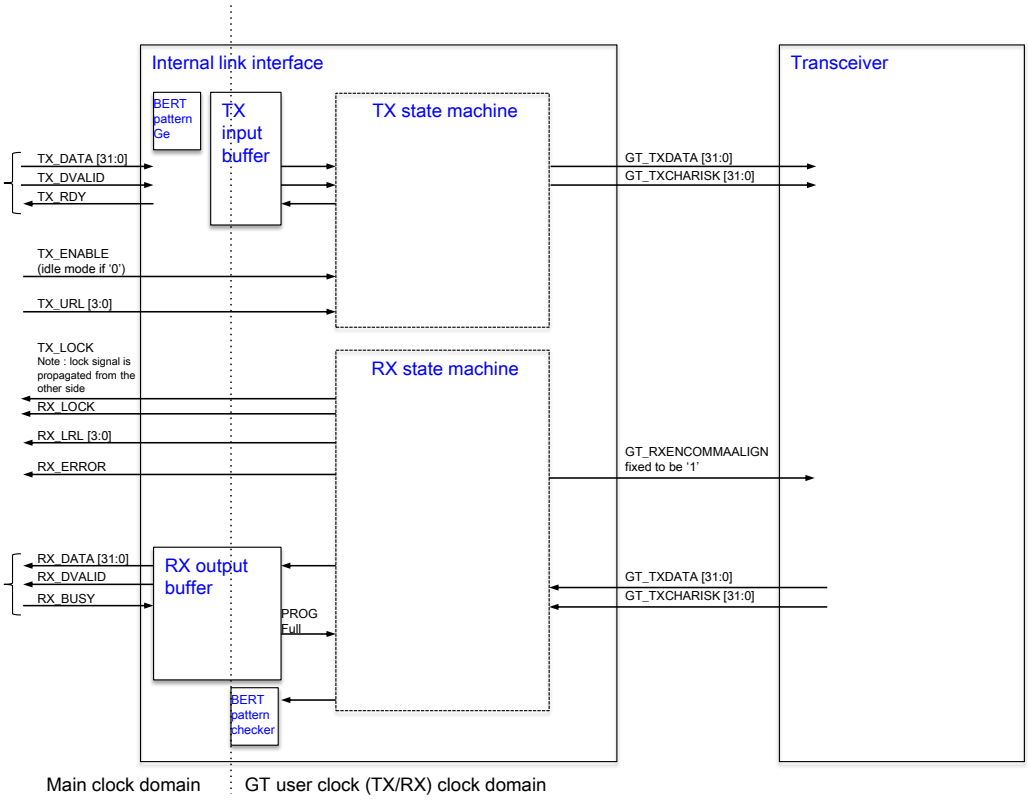

Figure 11: Internal link interface. This includes clock domain crossing (CDC) buffer between GT user clocks and main logic clock.

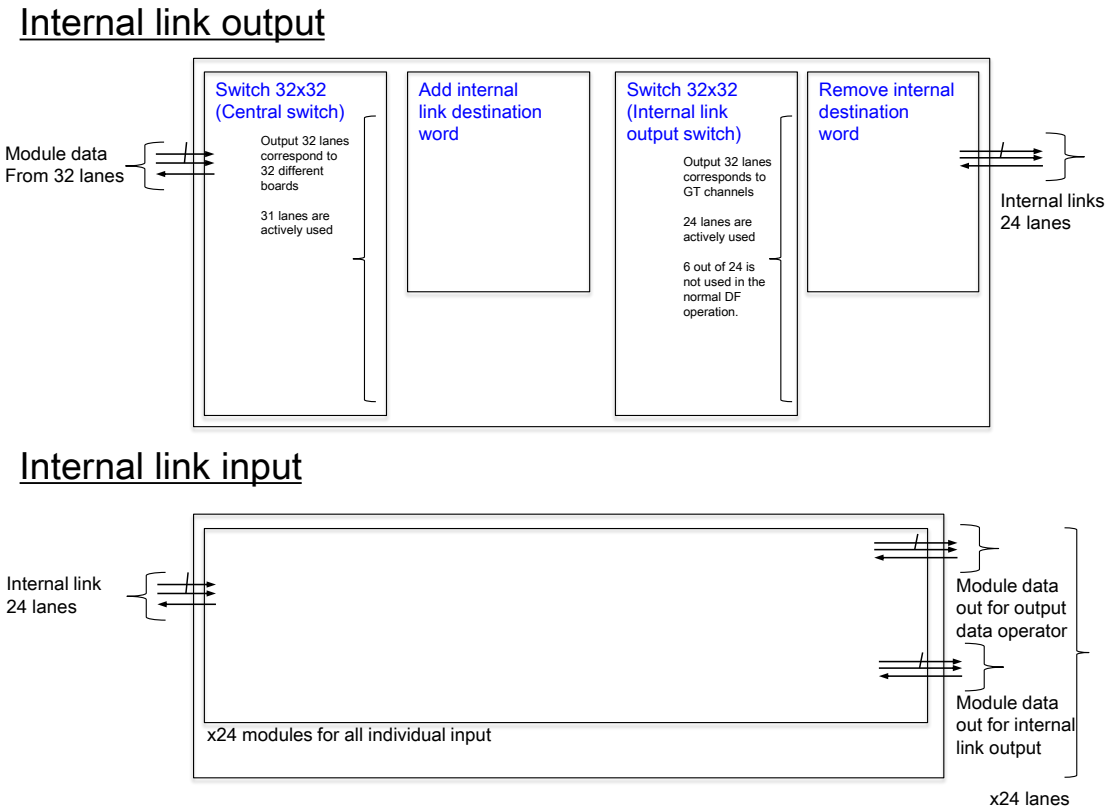

Figure 12: Schematics of input and output internal link.

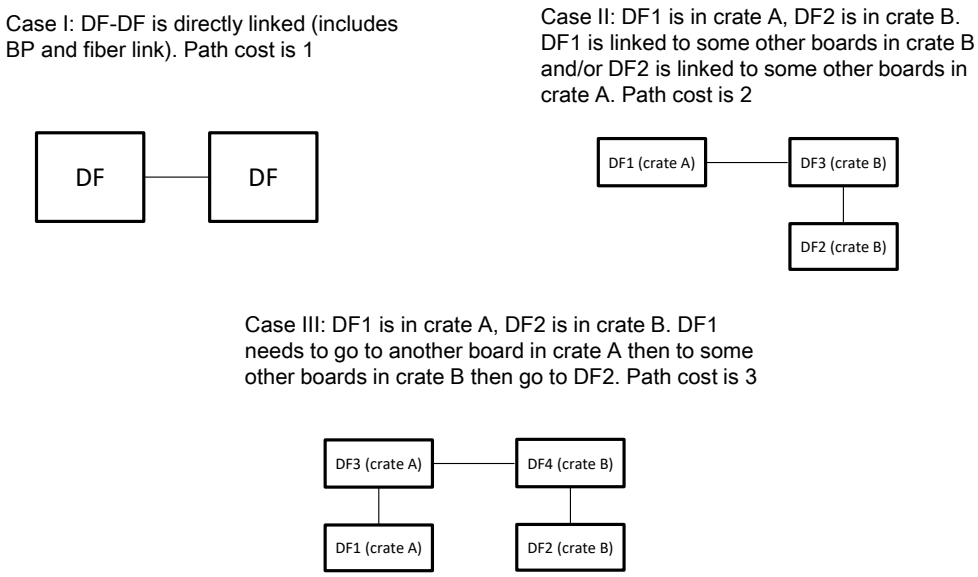

Figure 13: DF sharing pattern.

A ATCA fabric interface

Routing table description

¶ 89 Each column in the routing table depict Logical Slot positions. There are fifteen Fabric Channels per Slot each represented by a cell in the table. Each cell within the table represents a Fabric Channel and the numbers within the cell represent the destination end-point to which that Channel is routed. For example, the cell representing Channel 1 of Slot 9 contains the value (1–8) to indicate it is connected to Slot 1, Channel 8. This method to describe routing destinations per Channel is used for all routing assignment tables in this specification.

Table 6-11 Full Mesh Backplane routing assignments

	Logical Slot #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Connector	Channel #																
P20	15	16-1	16-2	16-3	16-4	16-5	16-6	16-7	16-8	16-9	16-10	16-11	16-12	16-13	16-14	16-15	15-15
P20	14	15-1	15-2	15-3	15-4	15-5	15-6	15-7	15-8	15-9	15-10	15-11	15-12	15-13	15-14	14-14	14-15
P20	13	14-1	14-2	14-3	14-4	14-5	14-6	14-7	14-8	14-9	14-10	14-11	14-12	14-13	13-13	13-14	13-15
P21	12	13-1	13-2	13-3	13-4	13-5	13-6	13-7	13-8	13-9	13-10	13-11	13-12	12-12	12-13	12-14	12-15
P21	11	12-1	12-2	12-3	12-4	12-5	12-6	12-7	12-8	12-9	12-10	12-11	11-11	11-12	11-13	11-14	11-15
P21	10	11-1	11-2	11-3	11-4	11-5	11-6	11-7	11-8	11-9	11-10	10-10	10-11	10-12	10-13	10-14	10-15
P21	9	10-1	10-2	10-3	10-4	10-5	10-6	10-7	10-8	10-9	9-9	9-10	9-11	9-12	9-13	9-14	9-15
P21	8	9-1	9-2	9-3	9-4	9-5	9-6	9-7	9-8	8-8	8-9	8-10	8-11	8-12	8-13	8-14	8-15
P22	7	8-1	8-2	8-3	8-4	8-5	8-6	8-7	7-7	7-8	7-9	7-10	7-11	7-12	7-13	7-14	7-15
P22	6	7-1	7-2	7-3	7-4	7-5	7-6	6-6	6-7	6-8	6-9	6-10	6-11	6-12	6-13	6-14	6-15
P22	5	6-1	6-2	6-3	6-4	6-5	5-5	5-6	5-7	5-8	5-9	5-10	5-11	5-12	5-13	5-14	5-15
P22	4	5-1	5-2	5-3	5-4	4-4	4-5	4-6	4-7	4-8	4-9	4-10	4-11	4-12	4-13	4-14	4-15
P22	3	4-1	4-2	4-3	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	3-12	3-13	3-14	3-15
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13	1-14	1-15

NOTE: The shading used in Table 6-11, "Full Mesh Backplane routing assignments," shows discontinuity of the routing sequence across rows and columns in the table.

Figure 14: ATCA fabric connection table.

B GT channel assignment

ATCA ch	Type	ID	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	NOTE 2	Categoly	GT ID	GT ch	LSC ch	Internal Link	RX FLIP	TX FLIP
J32P19	QSFP+	T1	Ch0	218	1	0	33	217		AUX T0		RTM LEFT	gt33	0	0			
J32P18	QSFP+	T1	Ch1	218	0	0	32	217				RTM LEFT	gt32	1	1			
J32P17	QSFP+	T1	Ch2	217	3	0	31	217				RTM LEFT	gt31	2	2			
J32P16	QSFP+	T1	Ch3	217	2	0	30	217				RTM LEFT	gt30	3	3			
J32P15	QSFP+	T2	Ch0	217	1	0	29	217		AUX T1		RTM LEFT	gt29	4	4			
J32P14	QSFP+	T2	Ch1	217	0	0	28	217				RTM LEFT	gt28	5	5			
J32P13	QSFP+	T2	Ch2	216	3	0	27	217				RTM LEFT	gt27	6	6			
J32P12	QSFP+	T2	Ch3	216	2	0	26	217				RTM LEFT	gt26	7	7			
J32P11	QSFP+	T3	Ch0	216	1	0	25	217		AUX T2	SLINK	RTM LEFT	gt25	8	8			
J32P10	QSFP+	T3	Ch1	216	0	0	24	217				RTM LEFT	**gt24**	9	9			
J32P9	QSFP+	T3	Ch2	215	3	0	23	214	U27			RTM LEFT	gt23	10	10			
J32P8	QSFP+	T3	Ch3	215	2	0	22	214				RTM LEFT	gt22	11	11			
J32P7	QSFP+	T4	Ch0	215	1	0	21	214		AUX T3		RTM LEFT	gt21	12	12			
J32P6	QSFP+	T4	Ch1	215	0	0	20	214				RTM LEFT	gt20	13	13			
J32P5	QSFP+	T4	Ch2	214	3	0	19	214				RTM LEFT	gt19	14	14			
J32P4	QSFP+	T4	Ch3	214	2	0	18	214				RTM LEFT	gt18	15	15			
J32P3	SFP+	T5		214	1	0	17	214		SSB T		RTM LEFT	gt17	16	16			
J32P2	SFP+	T6		214	0	0	16	214		Internal Link Ch0 P0		RTM LEFT	gt16	41		7	**RX**	
J32P1	SFP+	T7		213	3	0	15	214		Internal Link Ch0 P1		RTM LEFT	gt15	50		16		
J32P0	N/A			213	2	0	14	214		–	–	–	gt14					

ATCA ch	Type	ID	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	NOTE 2	Categoly	GT ID				RX FLIP	TX FLIP
J33P19	QSFP+	T1	Ch0	213	1	0	13	214		AUX B0		RTM LEFT	gt13	17	17			
J33P18	QSFP+	T1	Ch1	213	0	0	12	214				RTM LEFT	**gt12**	18	18			
J33P17	QSFP+	T1	Ch2	212	3	0	11	211				RTM LEFT	gt11	19	19			**TX**
J33P16	QSFP+	T1	Ch3	212	2	0	10	211				RTM LEFT	gt10	20	20		**RX**	
J33P15	QSFP+	T2	Ch0	212	1	0	9	211		AUX B1		RTM LEFT	gt9	21	21			
J33P14	QSFP+	T2	Ch1	212	0	0	8	211				RTM LEFT	gt8	22	22			
J33P13	QSFP+	T2	Ch2	211	3	0	7	211				RTM LEFT	gt7	23	23			
J33P12	QSFP+	T2	Ch3	211	2	0	6	211				RTM LEFT	gt6	24	24			**TX**
J33P11	QSFP+	T3	Ch0	211	1	0	5	211		AUX B2	SLINK	RTM LEFT	gt5	25	25			
J33P10	QSFP+	T3	Ch1	211	0	0	4	211				RTM LEFT	gt4	26	26			
J33P9	QSFP+	T3	Ch2	210	3	0	3	211	U27			RTM LEFT	gt3	27	27			
J33P8	QSFP+	T3	Ch3	210	2	0	2	211				RTM LEFT	gt2	28	28			
J33P7	QSFP+	T4	Ch0	210	1	0	1	211		AUX B3		RTM LEFT	gt1	29	29			
J33P6	QSFP+	T4	Ch1	210	0	0	0	211				RTM LEFT	**gt0**	30	30			
J33P5	QSFP+	T4	Ch2	110	0	1	0	110				RTM RIGHT	gt0	31	31		**RX**	**TX**
J33P4	QSFP+	T4	Ch3	110	1	1	1	110				RTM RIGHT	gt1	32	32		**RX**	**TX**
J33P3	SFP+	T5		110	2	1	2	110		SSB B		RTM RIGHT	gt2	33	33		**RX**	**TX**
J33P2	SFP+	T6		110	3	1	3	110		Internal Link Ch1 P0		RTM RIGHT	gt3	42		8	**RX**	**TX**
J33P1	SFP+	T7		111	0	1	4	110		Internal Link Ch1 P1		RTM RIGHT	gt4	51		17		**TX**
J33P0	N/A			111	1	1	5	110		–	–	–	gt5					

Figure 15: Transceiver channel assignment summary (1). For RTM channels.

Fabric	Ch	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE 1	Categoly	GT ID	GT ch	Internal Link	RX FLIP	TX FLIP
C13	P1	111	2	1	6	110	U27	–	NOT USED					**TX**
C13	P0	111	3	1	7	110		–	NOT USED					
C12	P1	112	0	1	8	112			Fabric	**gt0**				
C12	P0	112	1	1	9	112			Fabric	gt1				
C11	P1	112	2	1	10	112			Fabric	gt2				
C11	P0	112	3	1	11	112			Fabric	gt3				
C10	P1	113	0	1	12	112			Fabric	gt4				
C10	P0	113	1	1	13	112			Fabric	gt5				
C9	P1	113	2	1	14	112			Fabric	gt6	49	15		
C9	P0	113	3	1	15	112			Fabric	gt7	40	6		
C8	P1	114	0	1	16	115			Fabric	**gt8**	48	14		
C8	P0	114	1	1	17	115		Internal link	Fabric	gt9	39	5		
C7	P1	114	2	1	18	115			Fabric	gt10	47	13		
C7	P0	114	3	1	19	115			Fabric	gt11	38	4	**RX**	
C6	P1	115	0	1	20	115			Fabric	gt12	46	12		
C6	P0	115	1	1	21	115	U11		Fabric	gt13	37	3		
C5	P1	115	2	1	22	115			Fabric	gt14	45	11		
C5	P0	115	3	1	23	115			Fabric	gt15	36	2		
C4	P1	116	0	1	24	115			Fabric	gt16	44	10		
C4	P0	116	1	1	25	115			Fabric	gt17	35	1		
C3	P1	116	2	1	26	115			Fabric	gt18	43	9		
C3	P0	116	3	1	27	115			Fabric	gt19	34	0		
C2	P1	117	**1**	1	**29**	118		HUB						
C2	P0	117	**0**	1	**28**	118		HUB						
C1	P3	117	2	1	30	118		HUB						
C1	P2	117	3	1	31	118		HUB						
C1	P1	118	0	1	32	118		HUB						
C1	P0	118	1	1	33	118		IP Bus	1000BASE-T	gt0				

FMC	GP	GT Bank	Line	X	Y	REF CLK	clk gen	NOTE	FTK IM	Channel			RX FLP	TX FLP
3	0	118	2	1	34	118		Shared with IPBus	3	0			**RX**	
3	1	118	3	1	35	118		Shared with IPBus	3	1				
3	2	119	0	1	36	118	U11			N/C				
4	0	119	1	1	37	118			4	0			**RX**	**TX**
4	1	119	2	1	38	118			4	1			**TX**	
4	2	119	3	1	39	118				N/C				**TX**

2	2	218	2	0	34	217		Shared with RTM		N/C				
2	1	218	3	0	35	217		Shared with RTM	2	1				**TX**
2	0	219	0	0	36	219	U11		2	0				
1	2	219	1	0	37	219				N/C			**RX**	
1	1	219	2	0	38	219			1	1			**RX**	
1	0	219	3	0	39	219			1	1			**RX**	**TX**

Figure 16: Transceiver channel assignment summary (2). For Fabric and DF-IM channels.

C IP Bus registers

See `https://okumura.web.cern.ch/okumura/tmp/address_df.xml`.

C.1 IP Address

Address	Bit Postion	R/W	Name	Description
0X00000000	31:0	R	ipaddress	IP address (IPv4 32 bit)

C.2 Reset

Address	Bit Postion	R/W	Name	Description
0X00000001			reset	
	0	R/W	reset_delay	
	1	R/W	disable_fmc_input	
	2	R/W	reset_parity_checker	
	3	R/W	fmcin_logic_reset	
	4	R/W	main_state_machine_reset	
	5	R/W	i2c_state_machine_reset	
	6	R/W	configurable_parameter_reset	
	7	R/W	counter_parameter_reset	
	8	R/W	counter_parameter_reset	
	31:9	-		Reserved

C.3 Front FIFO error

Address	Bit Postion	R/W	Name	Description
0X00000002		R	fmcin_front_fifo_error	

.... to be summarized, including the details of use case for all the parameters.