1. (1) 1 nop

(2) modify the hazard detection unit so that:

when branch is detected,

1. select mux of ID-control to give all zeros.

2. stall IF/ID register for one clock cycle.

(3) IF stage

no stalls

the clock cycle would increase significantly because we are moving lots of components in ID stage to IF stage.

2.

instruction/clock cycle	1	2	3	4	5											
lw x10, 0(x13)	IF	ID	EX	MEM	WB											
lw x11, 8(x13)		IF	ID	EX	MEM	WB										
add x12, x10, x11			IF	ID	STALL	EX	MEM	WB								
addi x13, x13, 16				IF	STALL	ID	EX	MEM	WB							
bne x12, x0, LOOP					STALL	IF	ID	EX	MEM	WB						
lw x10, 0(x13)							IF	ID	EX	MEM	WB					
lw x11, 8(x13)								IF	ID	EX	MEM	WB				
add x12, x10, x11									IF	ID	STALL	EX	MEM	WB		
addi x13, x13, 16										IF	STALL	ID	EX	MEM	WB	
bne x12, x0, LOOP											STALL	IF	ID	EX	MEM	WB

3. (1) Assume X instructions

least CPI: $\frac{X+4}{X}$

CPI with jal: $\frac{X+4+X\cdot 5\%}{X}$

Δ CPI: 5%

CPI with mispredicted always taken: $\frac{X+4+X\cdot 3.1\%\cdot(1-5\%)}{X} = \frac{X+4+X\cdot 13.5\%}{X}$

Δ CPI: 13.5%

(2) CPI of jal doesn't change, still 5%

CPI with mispredicted 2 bit: $\frac{X+4+X\cdot 3.1\%\cdot(1-8.1\%)}{X} = \frac{X+4+X\cdot 6\%}{X}$

Δ CPI: 6%

4. (1) always NT : 33.33%.

always T : 66.67%.

(2) start rounds may give different accuracy depending on the initial value, but will eventually stabilize, i.e.

T	T	NT	T	NT	T	T	T	NT	T	NT	T
00	01	10	01	10	01	10	11	11	10	11	10	11
							✓	✓	✗	✓	✗	✓

Finally, accuracy goes to 66.67%.

(3) a shift register with initial values of 11 0 10 presents the first value as output in each cycle.