JOINT INSTITUTE
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ECE3700J Introduction to Computer Organization

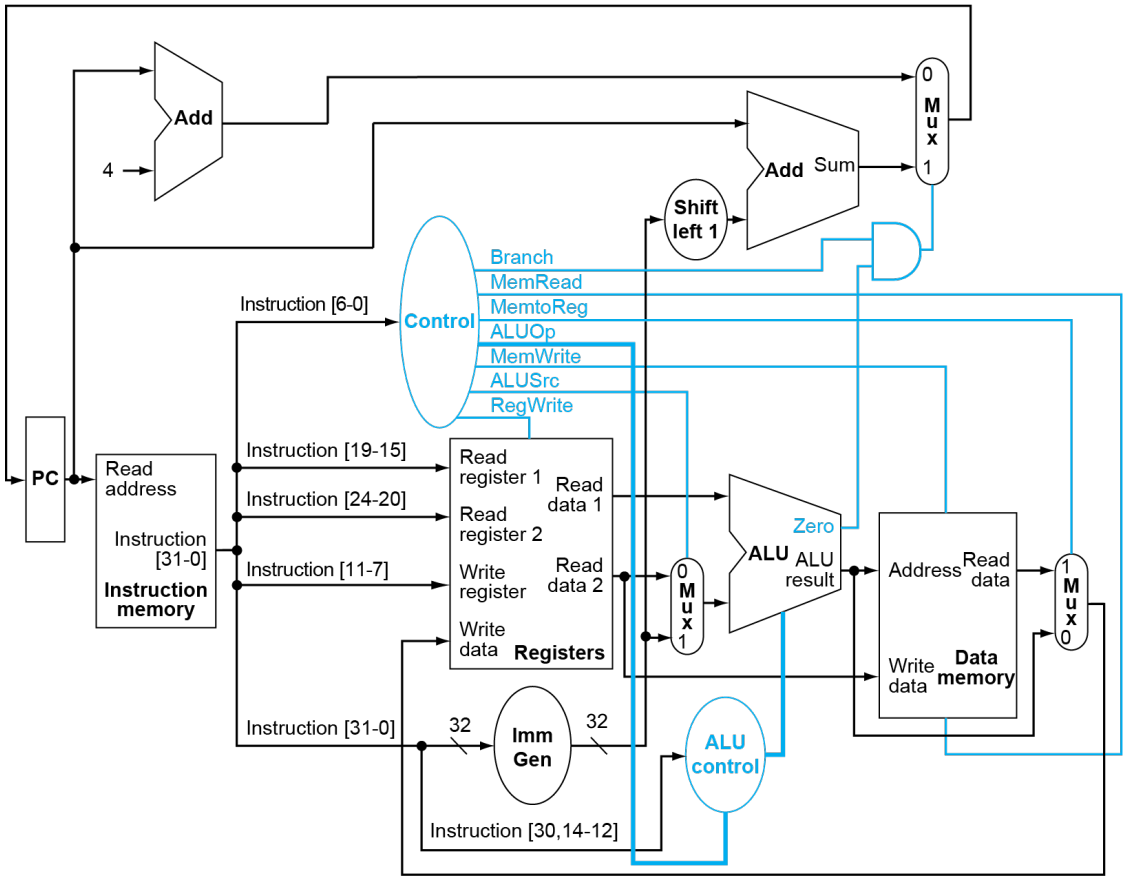
Homework 3

Assigned: October 13, 2022

Due: 2:00pm on October 20, 2022

Submit a PDF file on Canvas

All questions refer to the following figure.



1. (30 points) Given RISC-V assembly instruction sequence:

```
        bne x22, x23, Else
        add x19, x20, x21
        beq x0,x0,Exit
Else:   lw x19, 0(x20)
Exit:   …
```

Assuming the memory location of the first instruction (`bne`) is 0x1000F400, what are the values of the following control signals for each of the instructions?

Ctrl Signals / Instruction	Branch	MemRead	MemtoReg	ALUOp	MemWrite	ALUSrc	RegWrite	Zero	ImmGen Output
`add`	**0**	**0**	**0**	**10**	**0**	**0**	**1**	**0**	**x**
`beq`	**1**	**0**	**x**	**01**	**0**	**0**	**0**	**1**	**4**
`lw`	**0**	**1**	**1**	**00**	**0**	**1**	**1**	**0**	**0**

2. (10 points) Given following assembly instruction:
`sw rs2, imm12(rs1)`

(1) Which resources (blocks) perform a useful function for this instruction? (3 points)

Answer:
Instruction memory, register file, Imm Gen, ALUsrc mux, ALU, data memory, PCsrc mux

(2) Which resources (blocks) produce no output for this instruction? Which resources produce output that is not used? (7 points)

Answer:
All blocks produce some output (including data memory).
The outputs of Data Memory and PC + imm12*2 are not used.

3. (10 points) Consider the following instruction mix:

R-type	I-type (non-lw)	Load	Store	Branch	Jump
20%	28%	25%	10%	15%	2%

(1) What fraction of all instructions use data memory? (3 points)

Answer:
25 + 10 = 35%. Only Load and Store use Data memory.

(2) What fraction of all instructions use instruction memory? (2 points)

Answer:
100% Every instruction must be fetched from instruction memory before it can be executed.

(3) What fraction of all instructions use the sign extend? (5 points)

Answer:
28 + 25 + 10 + 15 + 2 = 80%. Only R-type instructions do not use the Sign extender.

4. (10 points) When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always read a logical 0. This is often called a "stuck-at-0" fault.
   (1) Which instructions fail to operate correctly if the MemToReg wire is stuck at 0? (5 points)

   Answer:
   Only loads are broken. MemToReg is either 1 or "don't care" for all other instructions.

   (2) Which instructions fail to operate correctly if the ALUSrc wire is stuck at 0? (5 points)

   Answer:
   I-type, loads, stores are all broken.

5. (30 points) Problems in this exercise assume that the logic blocks used to implement a processor's datapath have the following latencies:

I-Mem / D-Mem	Register File	Mux	ALU	Adder	Single gate	Register Read	Register Setup	Sign extend	Control
250 ps	150 ps	25 ps	200 ps	150 ps	5 ps	30 ps	20 ps	30 ps	100 ps

In above table, "Register Read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register Setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

(1) What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)? (5 points)

R-type:
Latency = Register Read (PC) + I-Mem + Register File (read & write) + Mux (ALUSrc) + ALU + Mux (MemtoReg) + Register Setup
= 30 + 250 + 150 + 25 + 200 + 25 + 20 = 700ps

(2) What is the latency of lw? (5 points)

lw:
Latency = Register Read (PC) + I-Mem + Register File (read & write, overlaps with ImmGen) + Mux (ALUSrc) + ALU + D-Mem + Mux (MemtoReg) + Register Setup
= 30 + 250 + 150 + 25 + 200 + 250 + 25 + 20 = 950ps

(3) What is the latency of sw? (5 points)

sw:

Latency = Register Read (PC) + I-Mem + Register File (read, overlaps with ImmGen) + Mux (ALUSrc) + ALU + D-Mem + Register Setup
= 30 + 250 + 150 + 25 + 200 + 250 + 20 = 925

(4) What is the latency of beq? (5 points)

beq:
Latency = Register Read (PC) + I-Mem + Register File (read, overlaps with ImmGen) + Mux (ALUSrc) + ALU (overlaps with Adder) + gate + Mux (PCSrc) + Register Setup
= 30 + 250 + 150 + 25 + 200 + 5 + 25 + 20 = 705

(5) What is the latency of an arithmetic, logical, or shift I-type (non-load) instruction? (5 points)

I-type:
Latency = Register Read (PC) + I-Mem + Register File (read & write, overlaps with ImmGen) + Mux (ALUSrc) + ALU + Mux (MemtoReg) + Register Setup
= 30 + 250 + 150 + 25 + 200 + 25 + 20 = 700

(6) What is the minimum clock period for this CPU? (5 points)

Answer: 950ps

6. (10 points) Modify the single-cycle processor datapath to support the `jal` instruction:

Answer:

jal rd, Target involves two operations:

1). R[rd] <= PC+4.
To load PC + 4 into register file, a new MUX is needed to select between PC + 4 and MemtoReg MUX output for the Write Data input to the register file. The new MUX should be controlled by a new control signal generated by the Control unit for jal.

2). PC <= PC + imm20 << 2
To load the Target into PC, a new MUX is needed to select between PCSur MUX output and the calculated Target. The new MUX should be controlled by a new control signal generated by the Control unit for jal.