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ECE3700J Introduction to Computer Organization

Homework 8

Assigned: October November 29, 2022

Due: 2:00pm on December 6, 2022

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1. (20 points) Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows parameters for a two-level cache memory.

	Size	Miss Rate	Hit Time
L1	16 KB	7.3%	1.18 ns
L2	1 MB	1.5%	5.34 ns

   (1) What is the AMAT for the computer? (10 points)

   (2) Assuming the L1 hit time determines the cycle times and a base CPI is 1.0 without any memory stalls, what is the total CPI? (10 points)

2. (30 points) In this exercise, we will examine how replacement policies impact miss rate. Assume a 2-way set associative cache with 4 blocks. Following table gives addresses for memory access.

   (1) Assuming an LRU replacement policy, how many hits does this address sequence exhibit? (10 points)

   (2) Assuming an MRU (most recently used) replacement policy, how many hits does this address sequence exhibit? (10 points)

   (3) Simulate a random replacement policy by flipping a coin. For example, “heads” means to evict the first block in a set and “tails” means to evict the second block in a set. How many hits does this address sequence exhibit? Note: you should flip the coin yourself, not by computer. (10 points)

   You may find following table is useful：

Block Address of memory	Hit/Miss	Evicted Block	Contents of Cache			
			Set 0		Set 1	
1						
3						
5						
1						
3						
1						

3						
5						
3						

3. (50 points) Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. The following is a stream of virtual byte addresses used to access memory.
Virtual addresses (in decimal): 12648, 45419, 46824, 16975, 40004, 12707, 52236
Assume 4 KB pages, a 4-entry fully associative TLB, and LRU replacement. If pages must be brought in from disk, increment to the next largest page number.

TLB:

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page Table:

Valid	Physical Page Number
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

(1) Given the virtual address stream, and the initial TLB and page table states shown above, show the final state of the system. Also list for each reference if it is a hit in the TLB, a hit in the page table, or a page fault. (15 points)

(2) Repeat question (1), but this time use 16 KB pages instead of 4 KB pages. (15 points)

(3) What would be some of the advantages and disadvantages of having a larger page size? (5 points)

(4) Show the final contents of the TLB if it is 2-way set associative. (15 points)

1(1) AMAT = 1.18 + 7.3% × (5.34 + 1.5% × 70) = 1.6467 ns

(2) L2 miss penalty = $\frac{70}{1.18}$ = 59.32 = 60 cycles

L1 miss penalty = $\frac{5.34}{1.18}$ = 4.53 = 5 cycles

CPI = 1 + 36% (7.3% × 5 + 7.3% × 1.5% × 60) = 1.641

2. (1) LRU: 3 Hits

Block Address of memory	Hit/Miss	Evicted Block	Contents of Cache			
			Set 0		Set 1	
1	M	None			1	
3	M	None			1	3
5	M	1			5	3
1	M	3			5	1
3	M	5			3	1
1	H	None			3	1
3	H	None			3	1
5	M	1			3	5
3	H	None			3	5

(2) MRU: 3 Hits

Block Address of memory	Hit/Miss	Evicted Block	Contents of Cache			
			Set 0		Set 1	
1	M	None			1	
3	M	None			1	3
5	M	3			1	5
1	H	None			1	5
3	M	1			3	5
1	M	3			1	5
3	M	1			3	5
5	H	None			3	5
3	H	None			3	5

(3) Random replace 4 hits

Block Address of memory	Hit/Miss	Evicted Block	Contents of Cache			
			Set 0		Set 1	
1	M	None			1	
3	M	None			1	3
5	M	3			1	5
1	H	None			1	5
3	M	5			1	3
1	H	None			1	3
3	H	None			1	3
5	M	1			5	3
3	H	None			5	3

3. (1) final stage

TLB:

Valid	Tag	Physical Page Number
1	~~12~~ 14	~~14~~
1	~~9~~ 13	~~13~~
1	3	6
~~1~~	4	9

Page Table:

Valid	Physical Page Number
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
~~1~~	~~Disk~~ 13
1	3
1	12

1 14

12648 = 0011 0001 0110 1000

45419 = 1011 0001 0110 1011

46824 = 1011 0110 1110 1000

16975 = 0100 0010 0100 1111

40004 = 1001 1100 0100 0100

12707 = 0011 0001 1010 0011

52236 = 1100 1100 0000 1100

4KB pages → 12 bits page offset.

	VPN:	TLB	page table	page fault
12648:	0011 = 3	hit	hit	no
45419:	1011 = 11	hit	hit	no
46824	1011 = 11	hit	hit	no
16975	0100 = 4	hit	miss	no
40004	1001 = 9	miss	miss	yes

12707	0011=3	hit	hit	no
52236	1100=12	miss	miss	yes

(2) final stage

TLB:

Valid	Tag	Physical Page Number
1	~~11~~ 2	~~12~~ 13
1	~~2~~ 1	~~3~~ 14
1	3	6
~~0~~ 1	~~1~~ 0	~~7~~ 5

Page Table:

Valid	Physical Page Number
1	5
~~0~~ 1	~~Disk~~ 14
~~0~~ 1	~~Disk~~ 13
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

12648 = 0011 0001 0110 1000

45419 = 1011 0001 0110 1011

46824 = 1011 0110 1110 1000

16975 = 0100 0010 0100 1111

40004 = 1001 1100 0100 0100

12707 = 0011 0001 1010 0011

52236 = 1100 1100 0000 1100

16 KB pages → 14 bits page offset.

	VPN:	TLB	page table	page fault
12648:	00 = 0	miss	hit	no
45419:	10 = 2	miss	miss	yes
46824	10 = 2	hit	hit	no
16975	01 = 1	miss	miss	yes
40004	10 = 2	hit	hit	no
12707	00 = 0	hit	hit	no
52236	11 = 3	hit	hit	no

(3) advantages: decreased page fault rate

disadvantages: slower speed, larger page fault penalty

(4) final stage

TLB:

	Valid	Tag	Physical Page Number
0	1	~~2~~ 4	~~2~~ 9
	1	~~2~~ 12	~~4~~ 14
1	1	~~2~~ 9	~~0~~ 13
	~~0~~ 1	4 3	9 6

Page Table:

Valid	Physical Page Number
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
~~2~~ 1	~~Disk~~ 13
1	3
1	12

1 14

12648 = 0011 0001 0110 1000

45419 = 1011 0001 0110 1011

46824 = 1011 0110 1110 1000

16975 = 0100 0010 0100 1111

40004 = 1001 1100 0000 0100

12707 = 0011 0001 1010 0011

52256 = 1100 1100 0000 1100

4KB pages → 12 bits page offset.

	VPN:	TLB	index	page table	page fault
12648:	0011 = 3	hit	1	hit	no
45419:	1011 = 11	miss	1	hit	no
46824	1011 = 11	hit	1	hit	no
16975	0100 = 4	miss	0	miss	no
40004	1001 = 9	miss	1	miss	yes
12707	0011 = 3	miss	1	hit	no
52256	1100 = 12	miss	0	miss	yes