Course Introduction

Instructional Support

- **Instructor:** Gang Zheng, Ph.D.
- **Office:** JI New Building 400E
- **Contact:** (021) 3420-6765 x4005, gzheng@sjtu.edu.cn
- **Classroom:** DZY 2-106
- **Office Hours:** W 4:00 – 6:00pm / Th 10:00am – noon, in office and on Feishu, or by appointment
- **TAs:** Ms. TANG Yuxuan, tyx-forgetful@sjtu.edu.cn
  Mr. GU Jiajun, jay_04@sjtu.edu.cn
  Mr. XU Liyang, xuleeyoung@sjtu.edu.cn
- **Recitation:** on schedule
- **TA Office Hours:** TBD

What will be taught?

- Assembly language
- How computers execute programs?
- What's the correspondence between different levels of languages: C/C++, assembly, and machine language?
- How to design a processor as a digital system?
- What are the difficulties and tricks in the design of a CPU? How to resolve? How to improve?
- How memory works as part of a computer, and how is it organized?
- How processor, memory, and I/O devices work together as a computer?

What Are You Expected to Do?

- Write an assembly language program, translate the program into binary code, and trace execution of the program.
- Model a processor using hardware description languages (HDLs).
- Be able to identify and resolve potential data and control hazards in the Instruction Set Architecture (ISA)
- Understand memory hierarchy including cache, main memory, hard disk, and how data is stored, understand memory hits and misses
- Understand the memory mapped I/O concept and how I/O devices interface to the CPU
- Be able to use library and internet resources for literature search to learn contemporary issues, technologies, and future development trends in computing

Textbook

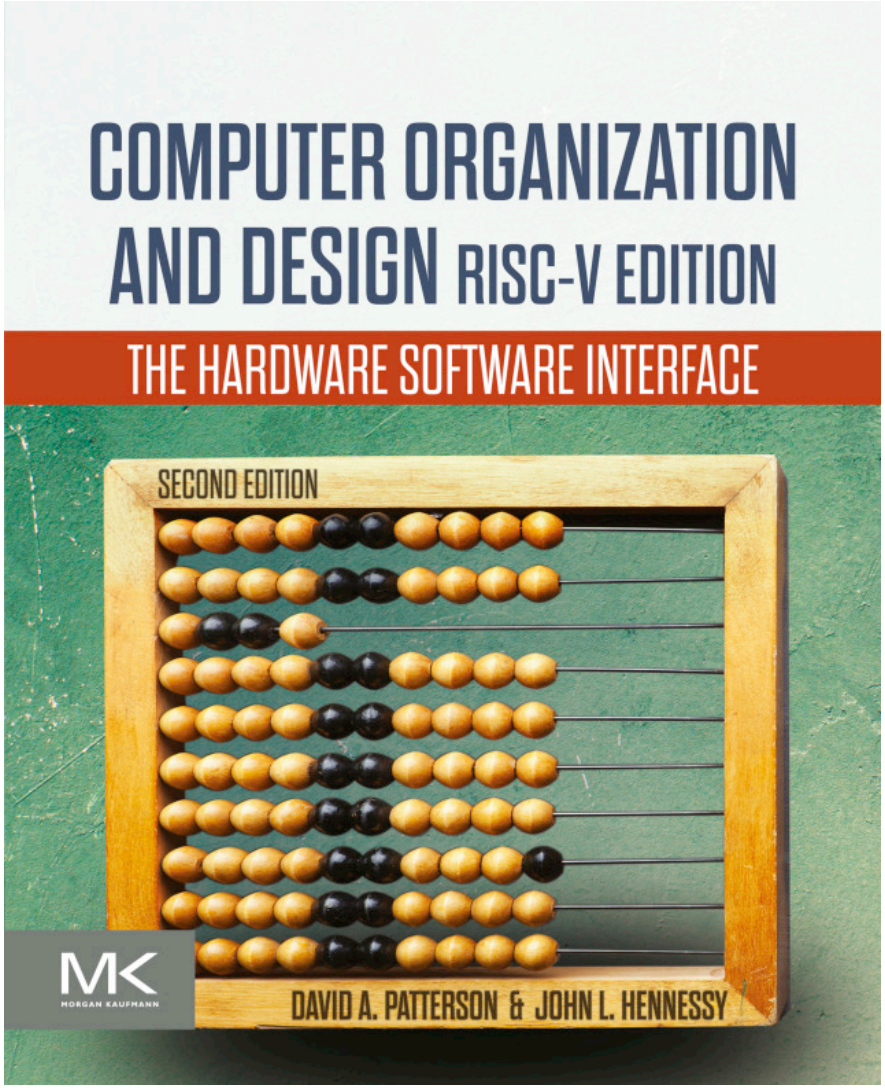
David Patterson and John Hennessy

Computer Organization and Design RISC-V Edition, 2nd edition

Morgan Kaufmann, 2020,

ISBN-10: 0128203315

ISBN-13: 978-0128203316



Tentative Schedule

Week	Date	Topics	Labs
1	9/13	Course Introduction, introduction to computer	
	9/15	RISC-V assembly: operations and operands	
2	9/20	RISC-V assembly: operations and operands	Lab 1. RISC-V Assembly
	9/22	RISC-V assembly: function and function call	
3	9/27	RISC-V assembly: function and function call	Lab 2. Assembly Programming
	9/29	RISC-V assembly: instruction encoding	
4	10/4	**No Class (National Holiday)**	
	10/6	**No Class (National Holiday)**	
5	10/11	CPU: single cycle processor	Lab 3. Single Cycle Processor
	10/13	CPU: pipelined processor	
6	10/18	CPU: pipelined processor	
	10/20	CPU: data hazards	
7	10/25	CPU: data hazards	
	10/27	CPU: data hazards	
8	11/1	CPU: control hazards	Lab 4. Pipelined Processor
	11/3	**Midterm Exam**	
9	11/8	CPU: control hazards	
	11/10	Memory: cache	
10	11/15	Memory: cache	Lab 5. Resolving Hazards
	11/17	Memory: cache	
11	11/22	Memory: cache	Lab 6. Cache Memory
	11/24	Memory: virtual memory	
12	11/29	Memory: virtual memory	Lab 7. Virtual Memory
	12/1	Memory: virtual memory	
13	12/6	I/Os and interfaces	
	12/8	Discussion & Review	
14	TBD	**Final Exam**	

Course Policies

- **Honor Code:**
  - Honor Code of the Joint Institute
  - ***Addendum to the Honor Code for Online Teaching***.
- **Test:**
  - Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- **Attendance:**
  - Strongly encouraged for better understanding of difficult concepts and student engagement during class time
  - Randomly taken
  - Attendance to all labs are required

Course Policies

- **Individual Assignments:**
  - Homework, some labs, literature review report
  - OK to discuss lecture topics and help each other understand the project/homework requirements better
  - NOT OK for duplicated submission
- **Group Assignments:**
  - Teams of 3 students, grouped randomly
  - One submission, shared grade, except for peer evaluation part
- **Submission:**
  - Electronic submission on Canvas before deadline

Assessment Methods

- **Homework:**
  - About 8 homework assignments
- **Examination:**
  - Two online or paper-based examinations.
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.
- **Laboratories:**
  - 7 labs
  - Labs 1-3 are individual work, Labs 4-7 are team work

Assessment Methods

- **Literature Review:**
  - Choose an interesting topic related to **performance improvement**, search literatures to review, write a review report
- **Attendance, Participation and Etiquette:**
  - Classroom interaction with the instructor and other students
  - Effective visit to office hours of the instructor and TA
  - effective contribution on Piazza
  - active participation in team-based labs
  - Vandalism, spam messages, verbal and other forms of abuse, violation of English-only policies and disturbance of the learning experience of other students are not permitted

Grading Policy

Attendance, Participation & Etiquette	5%
Midterm Exam	20%
Final Exam	20%
Lab */**	40%
Literature Review Report *	5%
Homework *	10%
Total	**100%**

*Individual assignments

**Group assignments

Note: final letter grades may be curved