JOINT INSTITUTE
交大密西根学院

ECE3700J Introduction to Computer Organization

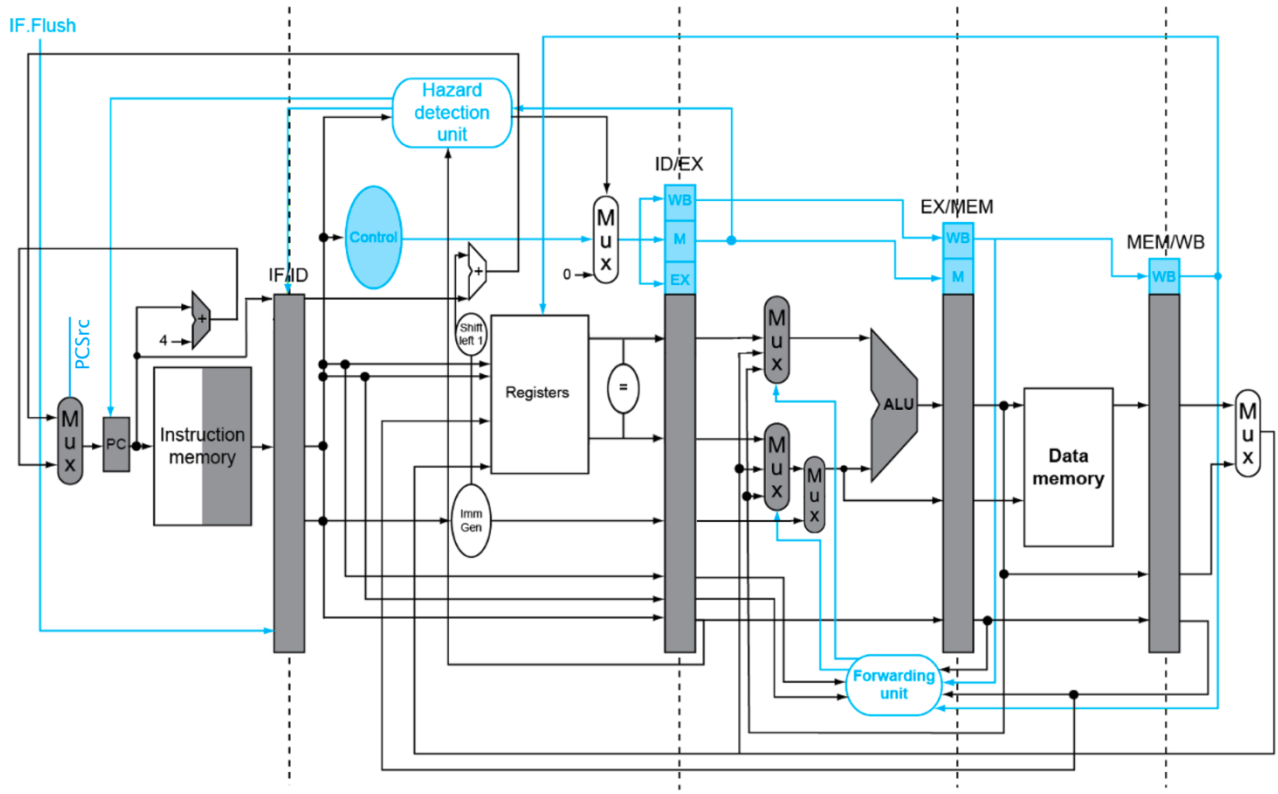
Homework 5

Assigned: October November 8, 2022

Due: 2:00pm on November 15, 2022

Submit a PDF file on Canvas

1. (30 points) One of the solutions to control hazard is to always stall the instruction following the branch or jump instruction by inserting nop instructions. Using the following diagram as a reference:



(1) How many nop should be inserted after each beq instruction? (5 points)

Answer: 1

(2) How can this stall be implemented in hardware rather than in software? (10 points)

Answer:

Possible Method 1: When beq is detected in the ID stage, provide a signal to affect the control of PCSrc in the IF stage, and make PC (in addition to PC+4 and branch target) an option of the mux for PC source. This is to make sure at the next clock cycle, PC can be loaded with either PC (address of the instruction immediately following beq) or branch target. At the same time, provide a signal to clear IF/ID pipeline register so that an all-zero instruction is inserted.

Possible Method 2: put nop (addi) instruction in a special address of the instruction memory, choose that address for PC input when beq is detected in the IF stage. This is simple but would involve extra time in the IF stage.

(3) If the above pipeline is modified to support jal instruction, which would be the earliest stage the jump instruction is identified and jump target is calculated? In that case, how many stalls would have to be inserted? How would the clock cycle time be affected? (15 points)

Answer:
Student answer could be any stage, but most likely:
IF stage: in that case, no stall need be inserted. But IF stage will be prolonged due to extra work for the jal instruction. This could make the IF stage the new critical stage. Thus the clock cycle time would be longer.

ID stage: in that case, 1 stall need be inserted. In other words, the instruction in the IF stage needs to be flushed. PC should be loaded with the target address of the jal instruction. In the ID stage, write data input of the register file need be selected between the normal data to be written into register file and PC+4, which might take a bit longer time. The clock cycle time might be longer if ID stage becomes the new critical stage.

2. (25 points) Consider the following loop.

```
LOOP: lw x10, 0(x13)
      lw x11, 8(x13)
```

```
add x12, x10, x11
addi x13, x13, 16
bne x12, x0, LOOP
```

Assume that perfect branch prediction is used (no stalls due to control hazards), that there are no delay slots, that the pipeline has full forwarding support, and that branches are resolved in the EX (as opposed to the ID) stage. Show a pipeline execution (multicycle) diagram for the first two iterations of this loop. Hint: unfold the loop first. Hint : you may use Excel to show the execution diagram.

Answer :

lw x10, 0(x13)	IF	ID	EX	MEM	WB											
lw x11, 8(x13)		IF	ID	EX	MEM	WB										
add x12, x10, x11			IF	ID	-	EX	MEM	WB								
addi x13, x13, 16				IF	-	ID	EX	MEM	WB							
bne x12, x0, LOOP					-	IF	ID	EX	MEM	WB						
lw x10, 0(x13)							IF	ID	EX	MEM	WB					
lw x11, 8(x13)								IF	ID	EX	MEM	WB				
add x12, x10, x11									IF	ID	-	EX	MEM	WB		
addi x13, x13, 16										IF	-	ID	EX	MEM	WB	
bne x12, x0, LOOP											-	IF	ID	EX	MEM	WB

3. (20 points) The importance of having a good branch predictor depends on how often conditional branches are executed. Together with branch predictor accuracy, this will determine how much time is spent flushing due to mispredicted branches. In this exercise, assume that the breakdown of dynamic instructions into various instruction categories is as follows:

R-type	branch	jal	lw	sw
40%	30%	5%	15%	10%

Also, assume the following branch predictor accuracies:

Always-Taken	Always-Not-Taken	2-Bit Dynamic
55%	45%	80%

(1) Stall cycles due to mispredicted branches and jumps increase the CPI. What is the extra CPI due to jumps? What is the extra CPI due to mispredicted branches with the always-taken predictor? Assume that branch outcomes are determined in the ID stage and that there are no data hazards, and that no delay slots are used. (10 points)

Answer :

Extra CPI by jump :

assume the number of instructions is X. The number of jump instructions is X * 5%. Assume jump instruction is determined in the ID stage, then each jump instruction adds 1 clock cycle.

Total CPI = (X+4+X*5%)/X

Ideal CPI without stalls = (X+4)/X

Extra CPI =Total CPI – Ideal CPI = 5%

Extra CPI by mispredicted branch :

Total CPI = (X+4+X*45%*30%)/X

Ideal CPI without stalls = (X+4)/X

Extra CPI = Total CPI – Ideal CPI = 45%*30% = 0.135

(2) Repeat (1) for the 2-bit predictor. (10 points)

Answer：Extra CPI = 20% * 30% = 0.06

4. (25 points) Given following repeating pattern of a branch instruction: T, T, NT, T, NT, T. (T: taken, NT: not taken)

(1) What is the steady-state accuracy of a 1-bit dynamic predictor if this pattern is repeated forever? (10 points)

Answer: (any initial predition is OK.)

Assuming 0 (NT) prediction initially, 2/6

Branch outcome	T	T	NT	T	NT	T
State	0	1	1	0	1	0
Prediction	NT	T	T	NT	T	NT
Correct?	N	Y	N	N	N	N

Branch outcome	T	T	NT	T	NT	T
State	1	1	1	0	1	0
Prediction	T	T	T	NT	T	NT
Correct?	Y	Y	N	N	N	N

Or

Assuming 1 (T) prediction initially, 2/6

Branch outcome	T	T	NT	T	NT	T
State	1	1	1	0	1	0
Prediction	T	T	T	NT	T	NT
Correct?	Y	Y	N	N	N	N

(2) What is the steady-state accuracy of a 2-bit dynamic predictor (as on Slide 28 of Topic 8) if this pattern is repeated forever? (10 points)

Answer: (any initial prediction is OK.)

Refer to the state diagram we discussed during the lecture, and assume we start off from 01 (weak not taken), assume the other states are 00 (strong not taken), 10 (weak taken), 11 (strong taken).

Branch outcome	T	T	NT	T	NT	T
State	01	10	11	10	11	10
Prediction	WNT	WT	ST	WT	ST	WT
Correct?	N	Y	N	Y	N	Y

Branch outcome	T	T	NT	T	NT	T
State	11	11	11	10	11	10
Prediction	ST	ST	ST	WT	ST	WT
Correct?	Y	Y	N	Y	N	Y

Steady state: 4/6 (20 points)

Assume we start off from 00

Branch outcome	T	T	NT	T	NT	T
State	00	01	10	01	10	01
Prediction	SNT	WNT	WT	WNT	WT	WNT
Correct?	N	N	N	N	N	N

Branch outcome	T	T	NT	T	NT	T
State	10	11	11	10	11	10
Prediction	WT	ST	ST	WT	ST	WT
Correct?	Y	Y	N	Y	N	Y

Branch outcome	T	T	NT	T	NT	T

State	11	11	11	10	11	10
Prediction	ST	ST	ST	WT	ST	WT
Correct?	Y	Y	N	Y	N	Y

Steady state: 4/6 (20 points)

Assume we start off from 10

Branch outcome	T	T	NT	T	NT	T
State	10	11	11	10	11	10
Prediction	WT	ST	ST	WT	ST	WT
Correct?	Y	Y	N	Y	N	Y

Branch outcome	T	T	NT	T	NT	T
State	11	11	11	10	11	10
Prediction	ST	ST	ST	WT	ST	WT
Correct?	Y	Y	N	Y	N	Y

Steady state: 4/6 (20 points)

Assume we start off from 11

Branch outcome	T	T	NT	T	NT	T
State	11	11	11	10	11	10
Prediction	ST	ST	ST	WT	ST	WT
Correct?	Y	Y	N	Y	N	Y

Steady state: 4/6 (20 points)

(3) Design a predictor that would achieve a perfect accuracy if this pattern is repeated forever. You predictor should be a sequential circuit with one output that provides a prediction (1 for taken, 0 for not taken) and no inputs other than the clock and the control signal that indicates that the instruction is a conditional branch. (5 points)

Answer : The predictor may be an N-bit rotate register, where N is the number of branch predictions in the repeating pattern. The register should be initialized with the repeating pattern itself (0 for NT, 1 for T, 110101 for this problem), and the prediction is always given by the value of the leftmost bit of the rotate register. The register should be shifted after each predicted branch.