Chen Zou

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INTRODUCTION

Chen Zou is a second-year PhD student in the Computer Science department of the University of Chicago. Chen Zou lays a broad interest in different layers of the computer systems, including computer architecture, OS, Database/ML system but with concentration in accelerators' architecture. Chen Zou is under instructions of Prof. Andrew A. Chien.

EDUCATION

- Ph.D. student, GPA 4.0, *Computer Science*, The University of Chicago — Sep 2016 – Now
- B.S. in Microelectronics, GPA 3.74, *Microelectronics*, Fudan University — Sep 2012 – June 2016

SKILLS

- Programming Languages: C++, Python, SystemVerilog, VHDL, JAVA, Perl, MATLAB
- EDA Tools: Modelsim, VCS, Design Compiler, IC Compiler, Vivado, Quartus

EMPLOYMENT

- Research Assistant, Large scale system group, University of Chicago, IL, USA — Sep 2016 – Now
- Software Engineering Intern, Cadence, Shanghai, China — Jan 2016 - Jun 2016
- Research Intern, University of Alberta, AB, Canada — July 2014 – Oct 2014

RESEARCH PROJECT

Memory hierarchy for accelerators

- Extended ZSim with trace replay feature for memory hierarchy study
- Analyzed similarities and differences between CPU and an vector accelerator traces.
- On the way to design accelerator specific memory architecture.

Unstructured data processor(UDP), published on MICRO 2017

- Implemented UDP in SystemVerilog as an ASIC and did performance tuning.
- Ported the ASIC design to the Intel Xeon-FPGA platform, closed the timing and did performance tuning.
- Implemented the software library that encapsulates the UDP on FPGA as data transformation services.

Data-driven routing congestion prediction at placement stage

- Performed data collection and cleaning from the placed design in Cadence design database.
- Designed an CNN architecture to predict routability using the resource maps during placement
- Did Hype-Parameter turning on the designed CNN architecture.

Approximate Logic Synthesis for two-level circuits, published on ASICON 2015

- Designed a dynamic programming based heuristic algorithm to perform approximate logic synthesis
- Employed multithreading to accelerate the implementation.

SELECTED PUBLICATIONS

- Yuanwei Fang, **Chen Zou**, Aaron J. Elmore, and Andrew A. Chien. **UDP: a programmable accelerator for extract-transform-load workloads and more.** In Proceedings of the 50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO '17).
- **Chen Zou**, Yajie Qin, Chenglu Sun, Wei Li, and Wei Chen. **Motion artifact removal based on periodical property for ECG monitoring with wearable systems.** Pervasive Mob. Comput. 40, C (Sep 2017), 267-278
- **Chen Zou**, Weikang Qian and Jie Han, **DPALS: A dynamic programming-based algorithm for two-level approximate logic synthesis.** In Proceedings of IEEE 11th International Conference on ASIC (ASICON '15)