數位系統導論實驗

Lab 11 Serial Multiplier in Verilog

Outline

- 課程目的
- 簡介 Sequential Circuit in Verilog
- 範例
- 作業說明及評分方式
- 附錄

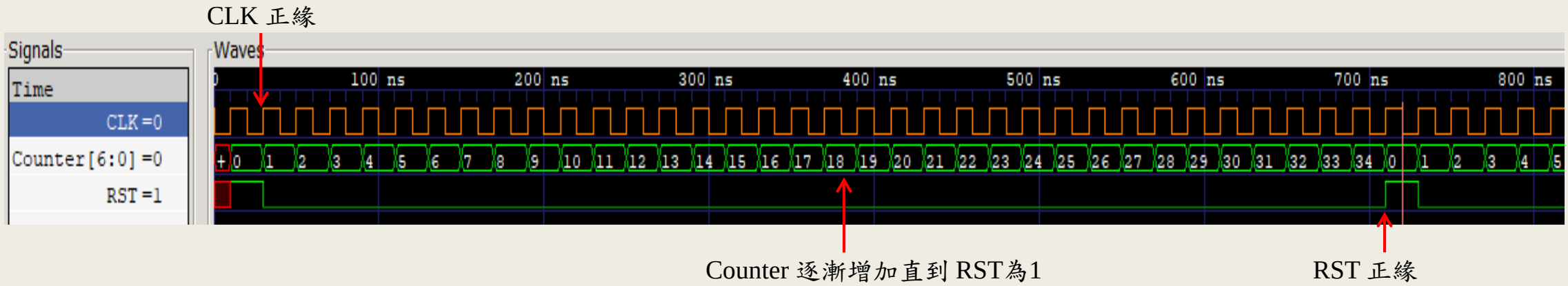
課程目的

- 學習以 Verilog 設計 32-bit serial multiplier
- 學習以 Verilog 設計 32-bit optimized serial multiplier
- 學習有號乘法與無號乘法在 serial multiplier 上的差異

簡介 Sequential Circuit in Verilog

- 右圖程式碼描述：觸發 CLK 或 RST 訊號正緣時會執行紅框內的程式碼

```
//Counter
always @(posedge CLK or posedge RST)
begin
  if(RST)
    Counter <=6'b0;
  else
    Counter <= Counter +6'b1;
end
```



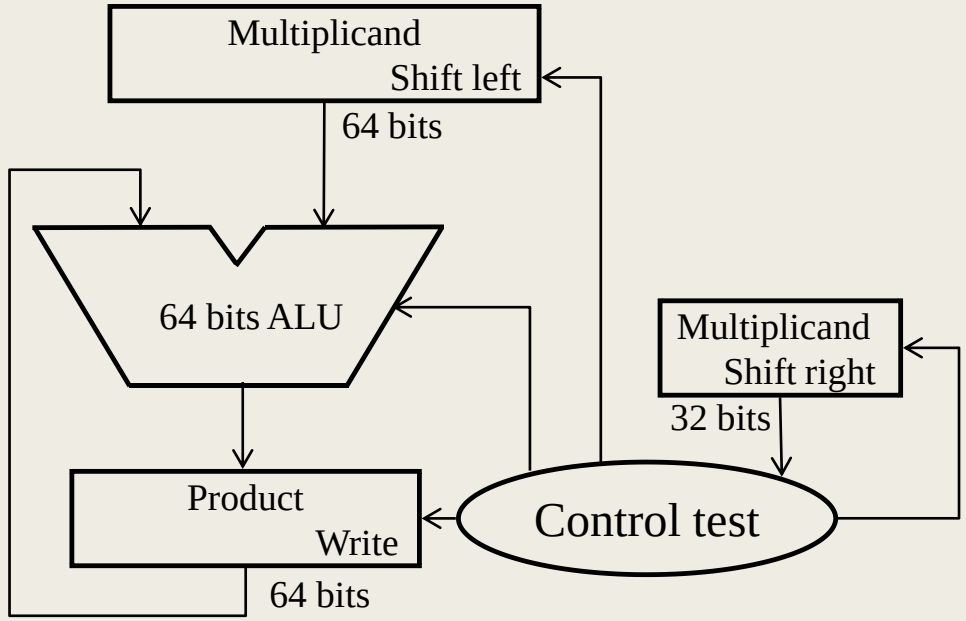
範例 – Unsigned 32-bit Serial Multiplier

- 本範例將以 Verilog 模擬 unsigned 32-bit serial multiplier，並以 testbench 產生如下圖的測試結果

```
// Successful //
//          30 *          90 = ?
//your answer is          2700,  correct answer is          2700


// Fail //
//          30 *         -90 = ?
//your answer is    128849016180, but correct answer is         -2700


// Fail //
//         -30 *          90 = ?
//your answer is    386547053940, but correct answer is         -2700


// Fail //
//         -30 *         -90 = ?
//your answer is 18446743558313478796, but correct answer is          2700


// Successful //
//    4294967295 *    4294967295 = ?
//your answer is 18446744065119617025,  correct answer is  18446744065119617025


// Fail //
//    4294967296 *           1 = ?
//your answer is          0, but correct answer is    4294967296


// Fail //
//    4294967297 *           1 = ?
//your answer is          1, but correct answer is    4294967297
```

Step1 – 修改範例程式

1. 開啟 example 資料夾內的 32mpy.v
2. 加入描述硬體行為的程式碼



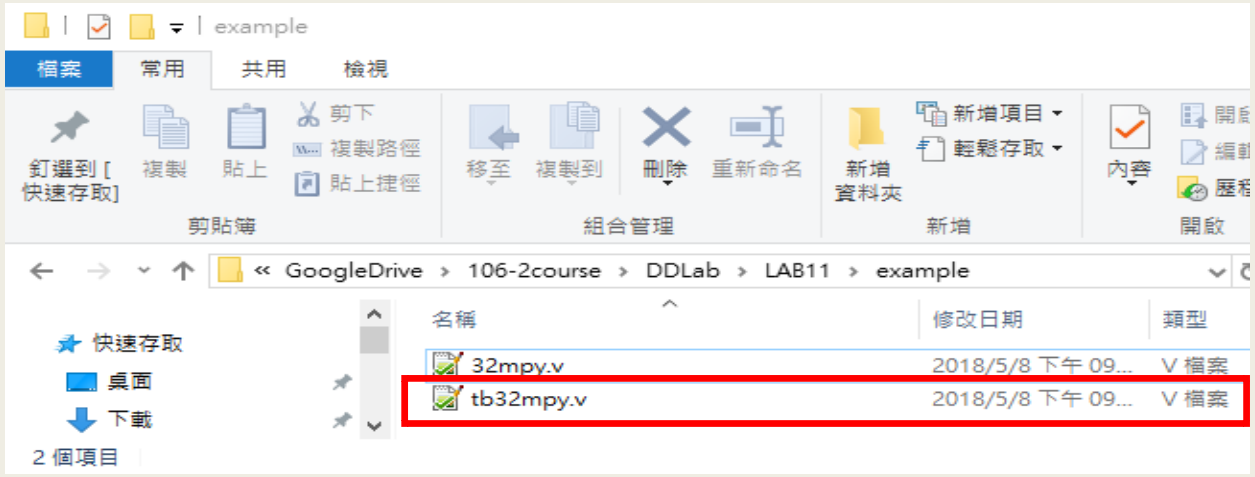

```
always @(posedge CLK or posedge RST)
begin
  //初始化數值
  if(RST) begin
    Product  <= 64'b0;
    Mplicand <= 64'b0;
    Mplier   <= 32'b0;
  end

  //輸入乘數與被乘數
  else if(Counter == 7'd0) begin
    Mplicand <= {32'b0,in_a};
    Mplier <= in_b;
  end

  //乘法與數值移位
  /* write down your design below */
  else if(Counter <=7'd32)
  begin
    if(Mplier[0] == 1'b1)
    Product <= Mplicand + Product;
    Mplicand <= Mplicand << 1'b1;
    Mplier <= Mplier >> 1'b1;
  end
  /* write down your design upon */
end
```

Step2 – 測試乘法器

1. 開啟 example 資料夾內的 tb32mpy.v
2. 在命令提示字元輸入指令

   “iverilog –o test tb32mby”

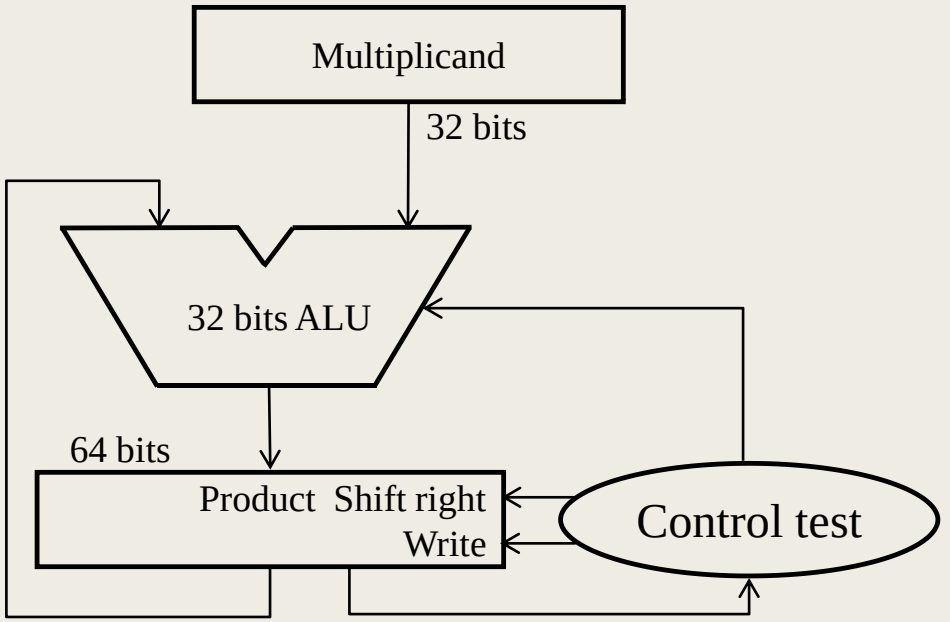
   “vvp test”
3. 確認 unsigned 32-bit serial multiplier 運算成功




```
// Successful //
//          30 *          90 = ?
//your answer is          2700,  correct answer is          2700


// Fail //
//          30 *         -90 = ?
//your answer is      128849016180, but correct answer is         -2700


// Fail //
//         -30 *          90 = ?
//your answer is      386547053940, but correct answer is         -2700


// Fail //
//         -30 *         -90 = ?
//your answer is 18446743558313478796, but correct answer is          2700


// Successful //
//  4294967295 *  4294967295 = ?
//your answer is 18446744065119617025,  correct answer is  18446744065119617025


// Fail //
//  4294967296 *           1 = ?
//your answer is          0, but correct answer is       4294967296


// Fail //
//  4294967297 *           1 = ?
//your answer is          1, but correct answer is       4294967297
```

作業說明及課程評分

- 作業Part1：按照範例操作並以 testbench 成功測試 unsigned 32-bit serial multiplier
- 作業Part2：參考範例與附錄，完成 unsigned 32-bit optimized serial multiplier，並設計 testbench 測試以下幾筆乘法
  1. 30×90
  2. 30×-90
  3. -30×90
  4. -30×-90
  5. $4294967295 \times 4294967295$
  6. 4294967296×1
  7. 4294967297×1



作業說明及課程評分

- 作業Part3：參考下表完成 32-bit booth multiplier，並設計 testbench 測試以下幾筆乘法
  1. 30×90
  2. 30×-90
  3. -30×90
  4. -30×-90

b_i	b_{i-1}	operation
0	0	0
0	1	+A
1	0	-A
1	1	0

作業說明及課程評分

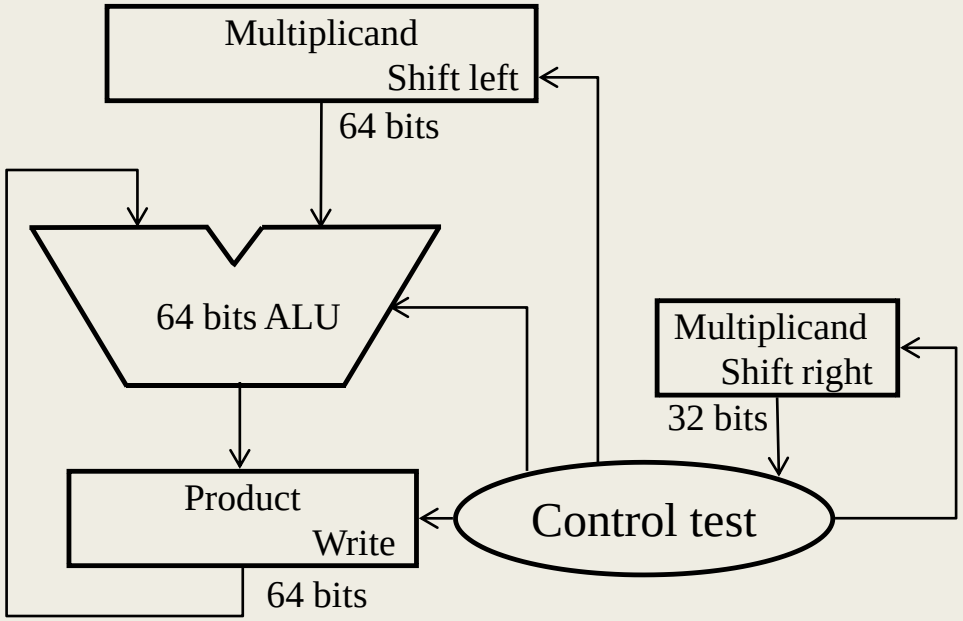
- 作業Part4：參考下表完成 32-bit modified booth multiplier，並設計 testbench 測試以下幾筆乘法
  1. 30×90
  2. 30×-90
  3. -30×90
  4. -30×-90

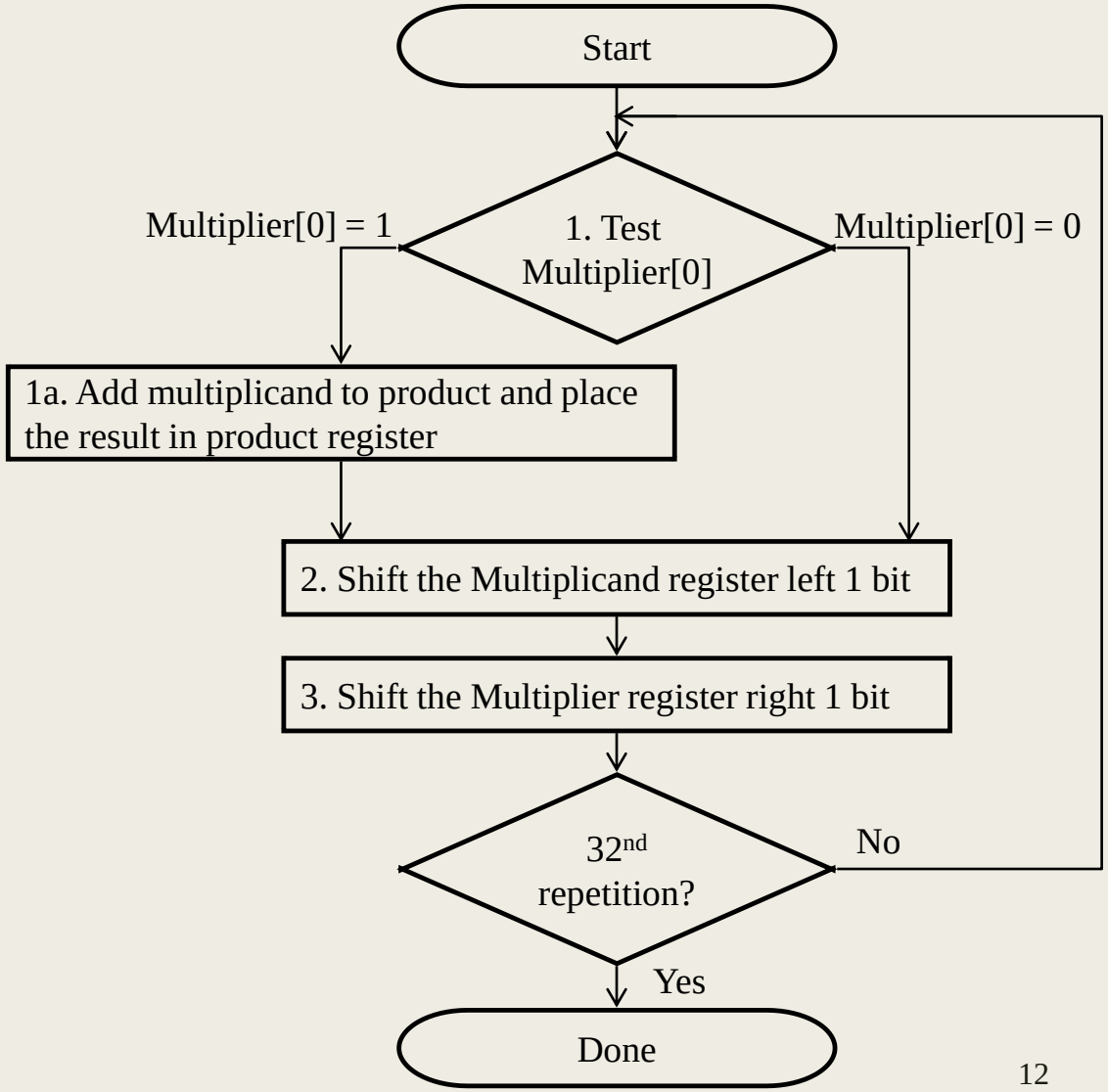
b_{i+1}	b_i	b_{i-1}	operation
0	0	0	0
0	0	1	+A
0	1	0	+A
0	1	1	+2A
1	0	0	-2A
1	0	1	-A
1	1	0	-A
1	1	1	0

作業說明及課程評分

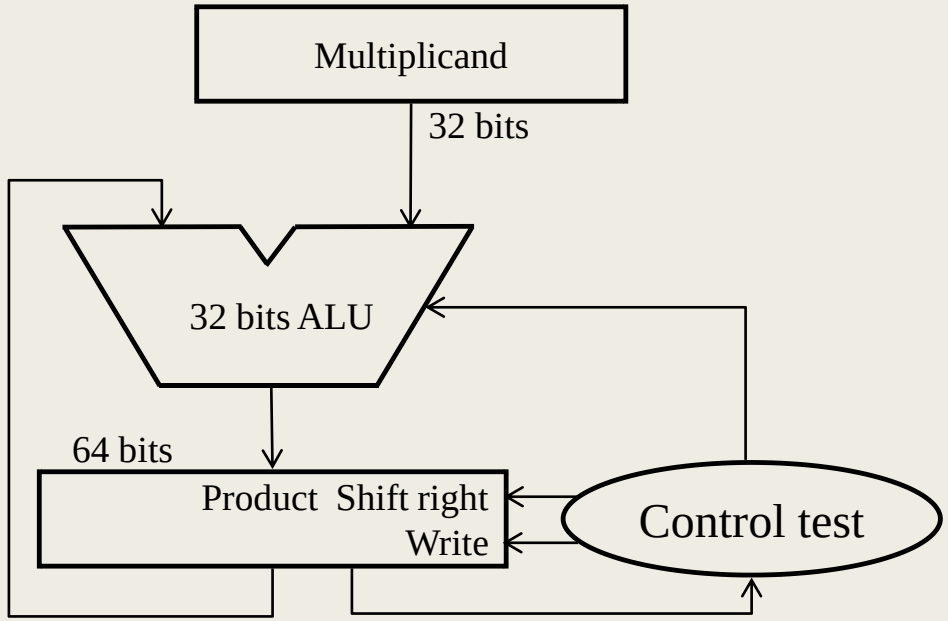
- Demo 方式： Demo 開始時助教會公布考題，請於時限內呈現作業並作答考題
- Demo 日期：5/28，5/30
- Demo 地點：工程一館105
- 梯次名單：與 Lab 1 相同
- 梯次時間： 19:10 ~ 19:30、19:40 ~ 20:00、20:10 ~ 20:30、20:40 ~ 21:00
- 評分方式：作業70 %，上機考30 %
- 作業配分：part1 30% ，part2 40% ，part3 30% ，part4 20%
- 注意事項：請同學於時限內完成作業呈現與考題作答，非該梯次之同學也請勿在現場逗留

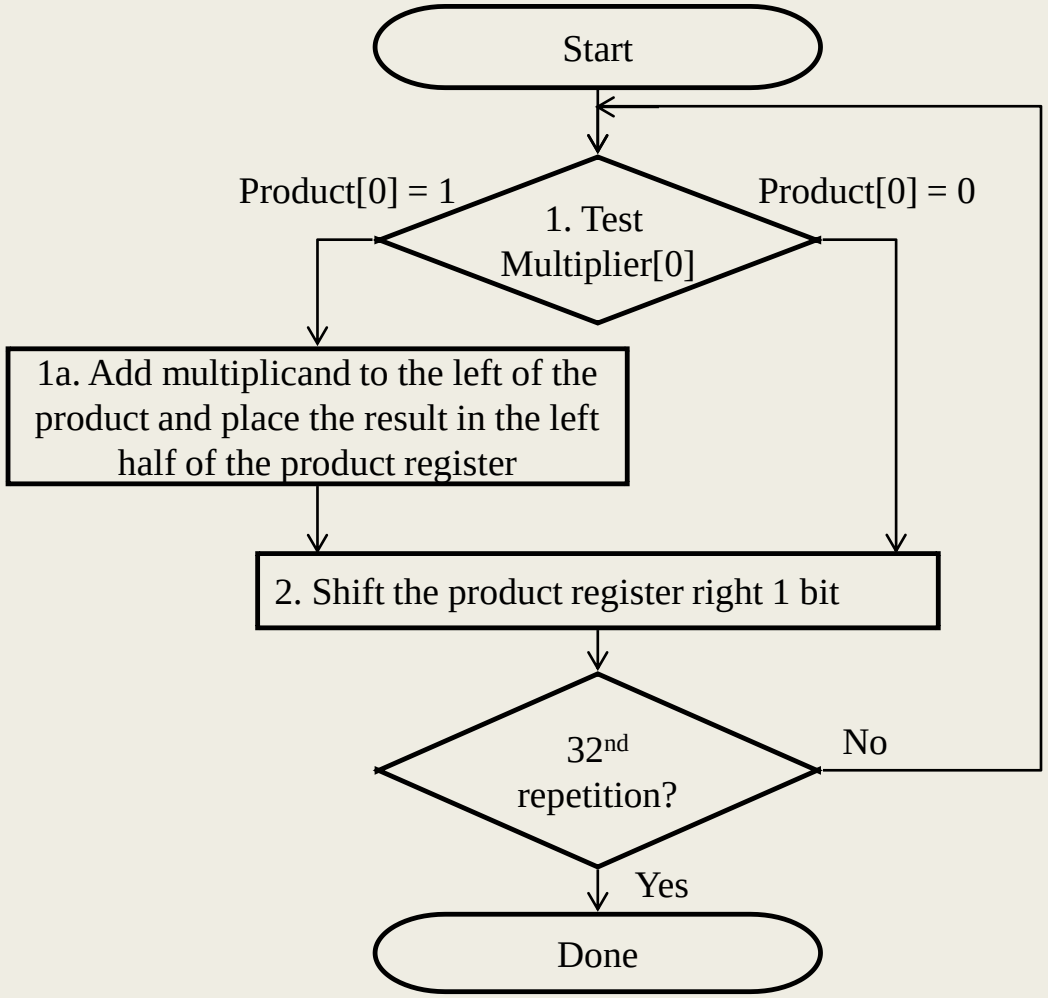
附錄 – Serial Multiplier





附錄 – Optimized Serial Multiplier





附錄 – Multiplier Comparison

Register	V1	V3
Mplicand	32 bits(shift left)	16 bits
ALU	32 bits	16 bits
Mplier	16 bits(shift right)	None
Product	32 bits	32 bits(shift right)