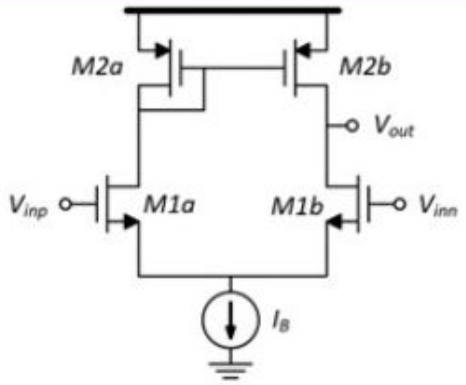
Consider the shown 5T OTA, and assume the square law is valid. Assume the OTA has a capacitive load (CL) that is much larger than the parasitics. If the designer halved the bias current (IB) (multiplied it by 0.5) and halved the width of every transistor as well, then:

1) The gm/ID of the input pair is multiplied by .....
2) The DC voltage gain is multiplied by .....
3) The bandwidth is multiplied by .....
4) The unity-gain frequency (UGF) is multiplied by .....
5) The input-referred noise density (in V^2/Hz) is multiplied by .....

Thursday Analog Quiz



if we halve I and W:

1) g_m/I_D:

$$\frac{g_m}{I_D} = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}}{I_D} \quad \left(I_D \times \frac{1}{2}\right)$$

$$= \frac{\frac{1}{2}}{\frac{1}{2}} \Rightarrow \times 1$$

2) A_v:

$$A_v = G_m \times \frac{1}{2} R_{out} \times 2$$

$A_v \times 1$

3) BW:

$$BW = \frac{1}{2\pi C_{out} R_{out}}$$

$BW \times \frac{1}{2}$

4) Unity-Gain Frequency:

$$UGF = GBW = A_v BW \Rightarrow UGF \times \frac{1}{2}$$

5) $\overline{v_n^2}$:

$$\overline{v_n^2} \propto \frac{1}{g_m} \Rightarrow \overline{v_n^2} \times 2$$

Conclusion:

As we halved the bias current and the width we preserved the inversion layer, so V_{OV} and g_m/I_D stays the same. As result, the gain also stays constant. What we decesively lose is the small-signal speed UGF. And we also pay Noise penalty.

So as design moral, scaling I and W down together save the power and keep us in the same operating region. But we make our amplifier slower and noisier.
So as solution we can reduce the capacitance, or move g_m/I_D to weak inversion or use compensation tweak.