Design #3

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1 Problem statement and Specifications

Design a low-voltage cascode current mirror with 1:2 input current to output current ratio. The low frequency output impedance should be greater than 2 MΩ. Assume a $50\mu A$ input current and V_{out} is $\frac{1}{2}V_{DD}$.

2 Theoretical Analysis

2.1 Sizing M1, M2:

Choose large channel length for M2 ($L_2 = 1\mu m$) to increase the transistor's output resistance, thereby increasing the output impedance. Additionally, we biased it in strong inversion ($gm/ID = 10$) for good trade-off between speed and accuracy.

- From the charts:
  - $W_2 = 21.4\,\mu$m
  - $W_1 = \frac{W_2}{2} = 10.7\,\mu$m
  - $r_{o2} = 88.5k\Omega$

2.2 Sizing of M3, M4:

Bias M3 and M4 in moderate inversion ($gm/ID = 15$). For the length $L_3, L_4 \geq 500nm$.

- From the charts:
  - $W_3 = 19.57\,\mu$m
  - $W_4 = \frac{W_3}{2} = 9.78\,\mu$m

2.3 Bias Generation (M5)

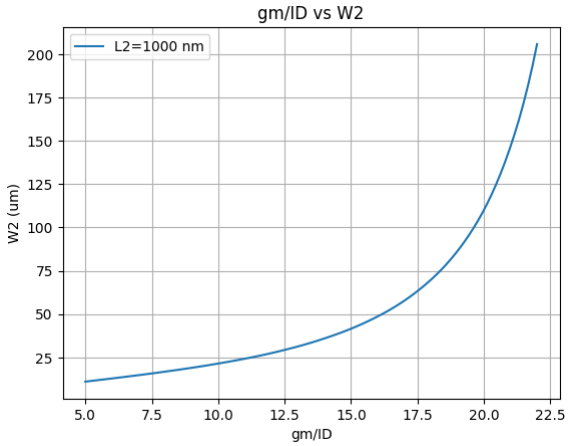
$V_{GS5} \geq V_{GS3} + V_2^*$, we assume $V_{th2} = V_{th3}$,

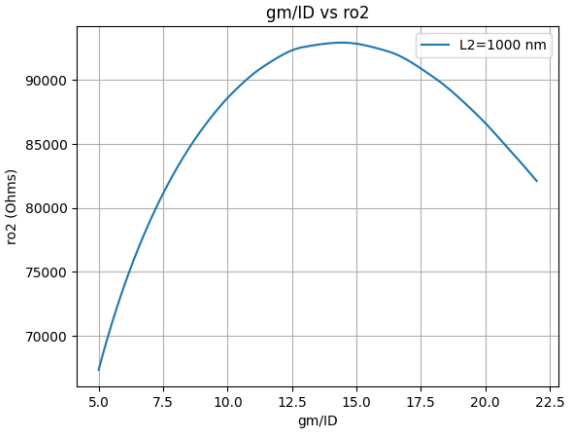
$$V_5^* = V_2^* + V_3^* = 0.333mV$$

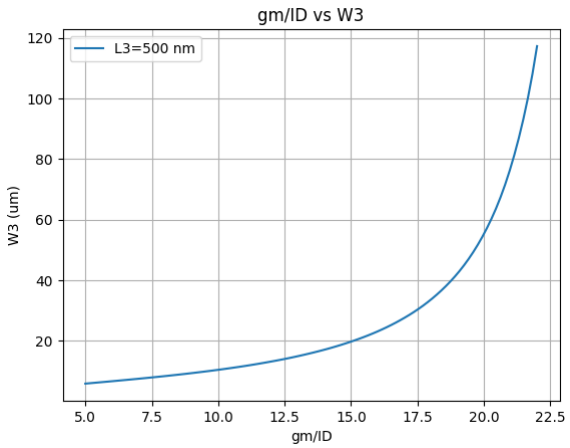
choosing $(gm/ID)_5 = 5$

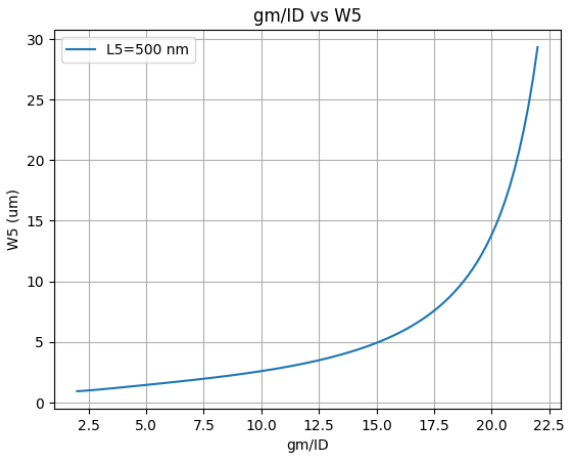
- From the charts:
  - $W_5 = 1.45\,\mu\text{m}$

3 gm/ID Charts



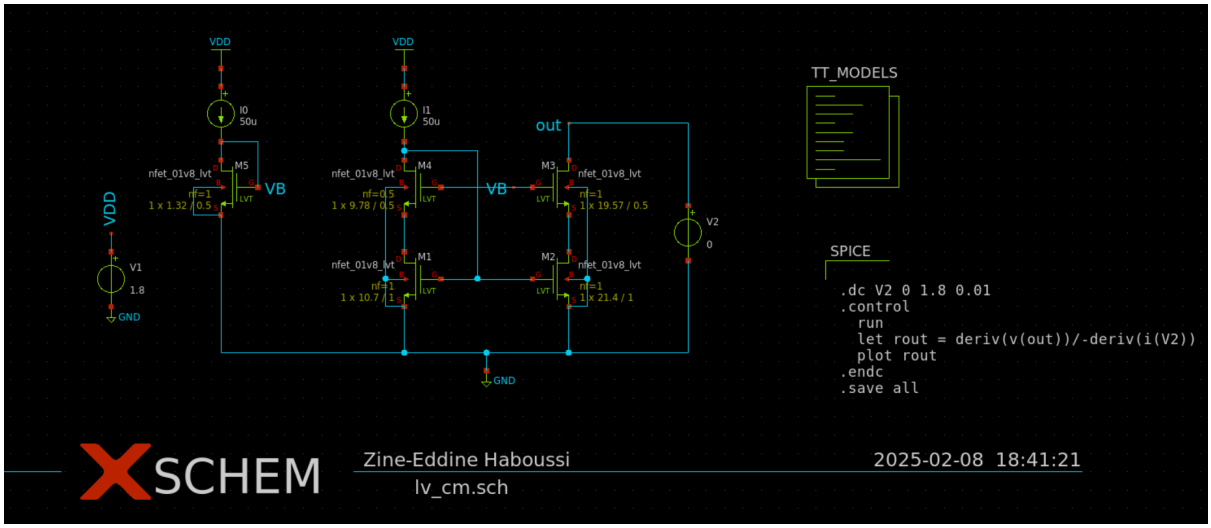






4 Simulation Results

4.1 Test bench



4.2 Simulation results

4.2.1 Output current

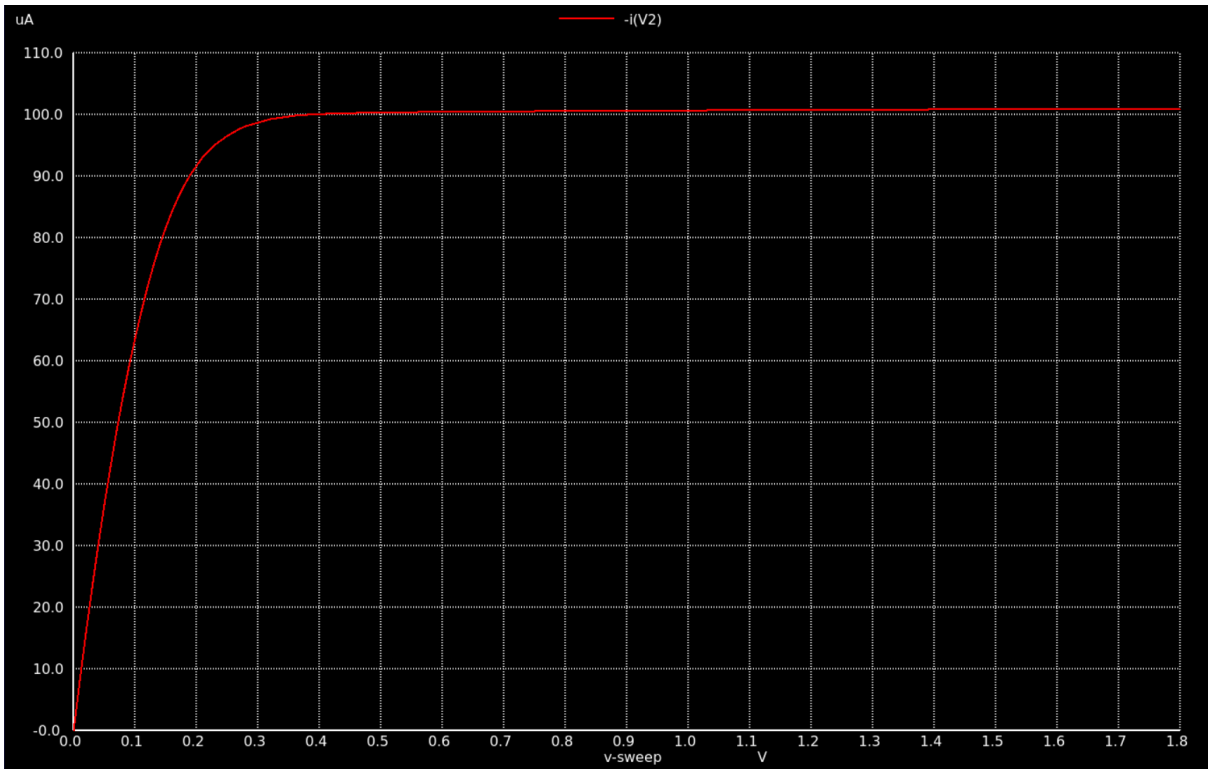


Figure 2: AC Analysis

4.2.2 AC Output Impedance