Design #2

Zine-Eddine Haboussi

January 23, 2025

1 Problem statement and Specifications

Design a single-ended amplifier using common-source configuration with a resistive load to meet the following specifications:

Specification	**Value**
DC Gain	20 dB
Bandwidth	$\geq 1\,\text{GHz}$
Power Consumption	$\leq 2\,\text{mW}$
Capacitive Load	50 fF

2 Theoretical Analysis

$$I_D \leq \frac{P_{cons}}{V_{DD}} \leq \frac{0.5 \cdot 10^{-3}}{1.8} \leq 277\mu A$$

$$GBW = \frac{g_m}{2\pi C_{out}} \geq 10 \cdot 10^9 \implies g_m \geq 3.14\text{mS}$$

We assume $V_{out} = 0.9V$, thus R_D can be derived:

$$R_D = \frac{V_{DD} - V_{out}}{I_D} = \frac{1.8 - 0.9}{260 \cdot 10^{-6}} = 3400\,\Omega$$

2.1 Design Choices

- **gm/ID Ratio**: Chosen as $20\,\text{V}^{-1}$ based on performance trade-offs.
- **Channel Length**: $L = 180\,\text{nm}$ for optimized intrinsic gain.

- **Transconductance**:

$$g_m = \frac{g_m}{I_D} \cdot I_D = 20 \cdot 260 \cdot 10^{-6} = 5.2\,\text{mS}$$

From charts:

- $g_m/g_{ds} = 25.22$ (intrinsic gain).
- $V_{GS} = 0.59V$
- $W = 98\,\mu\text{m}$.

2.2 Verification

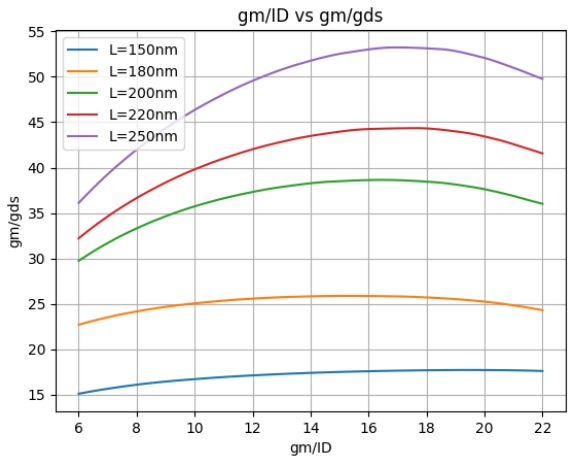
The output resistance (R_{out}) is calculated as:

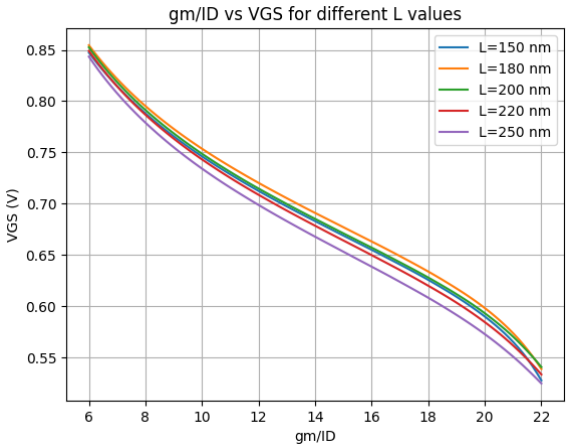
$$R_{\text{out}} = \frac{R_D \cdot r_o}{R_D + r_o} = \frac{3400 \cdot 4848}{3400 + 4848} = 1963\,\Omega$$

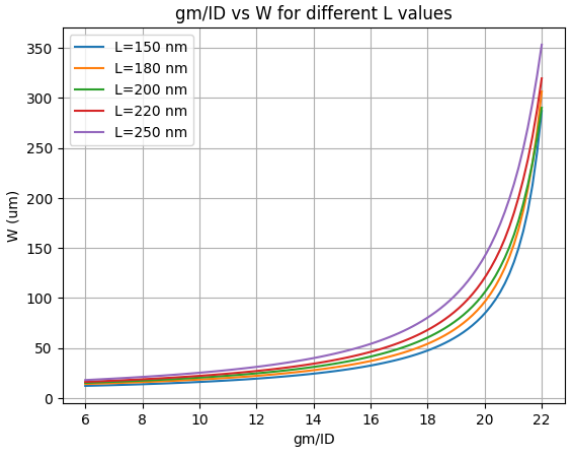
The voltage gain (A_v) is:

$$A_v = g_m \cdot R_{\text{out}} = 5.2 \cdot 10^{-3} \cdot 1963 = 10.20\,\text{V/V (or 20 dB)}$$

3 gm/ID Charts







4 Simulation Results

4.1 Test bench

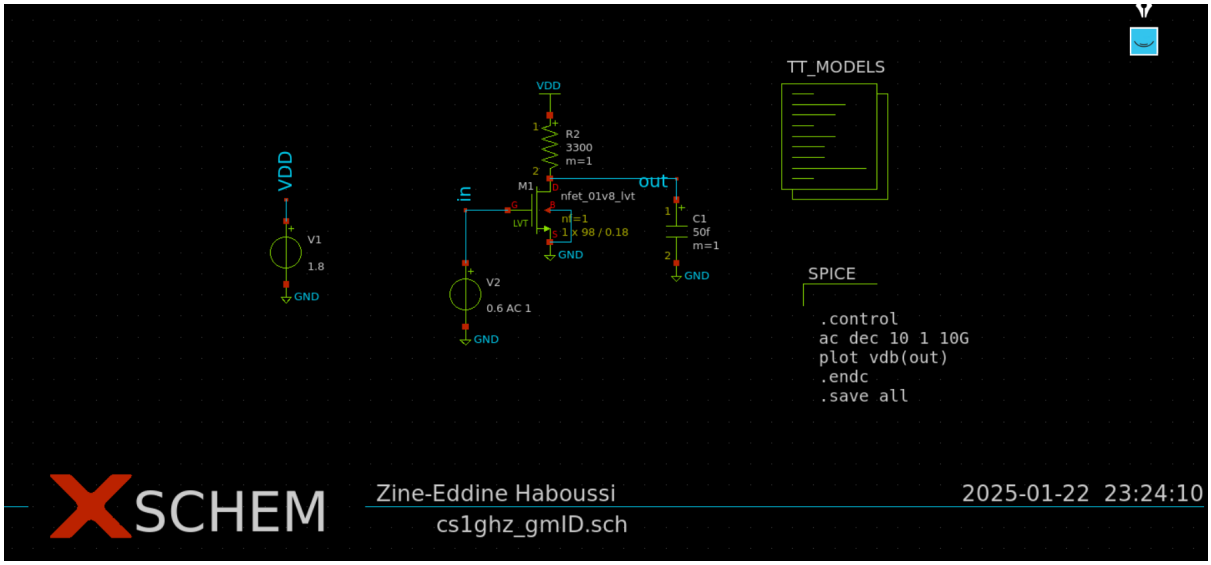


Figure 2: AC Analysis

4.2 AC Analysis

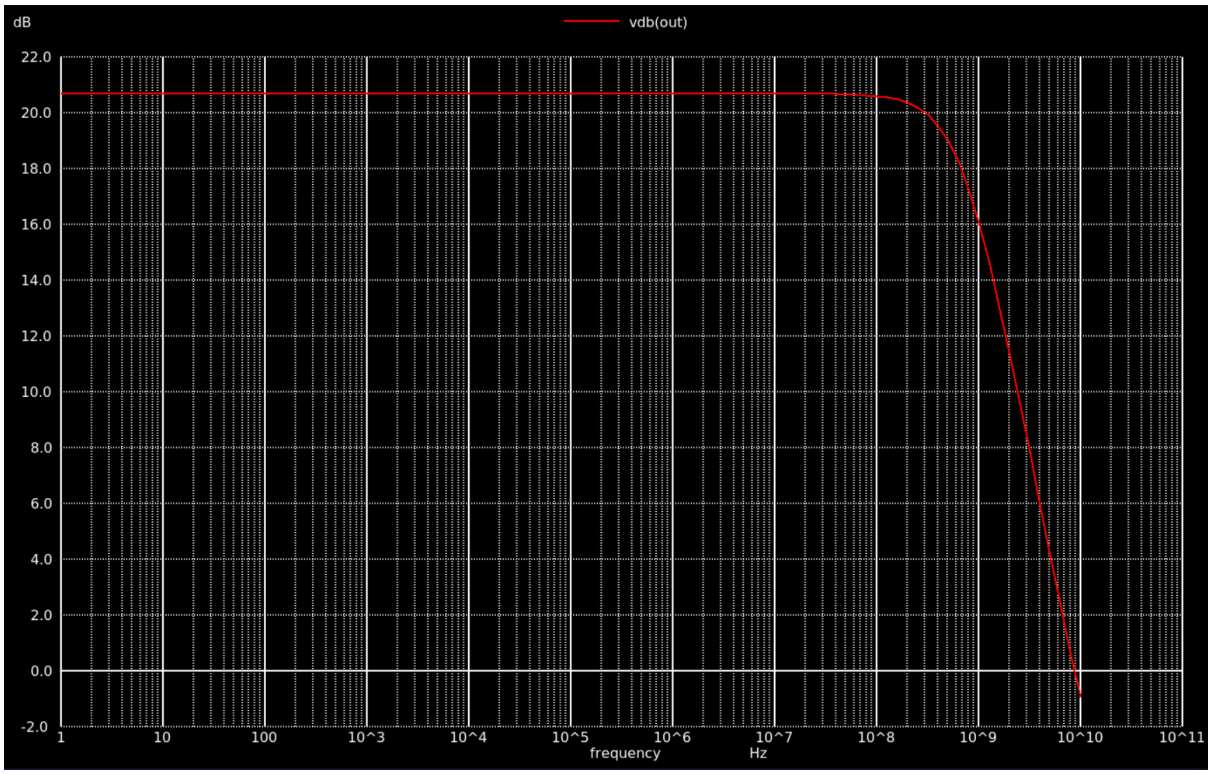


Figure 3: AC Analysis