

# Circuit and System Technologies for Energy-Efficient Edge Robotics

(Invited Paper)

Zishen Wan, Ashwin Sanjay Lele, Arijit Raychowdhury

School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA

[zishenwan@gatech.edu](mailto:zishenwan@gatech.edu), [alele9@gatech.edu](mailto:alele9@gatech.edu), [arijit.raychowdhury@ece.gatech.edu](mailto:arijit.raychowdhury@ece.gatech.edu)

**Abstract**—As we march towards the age of ubiquitous intelligence, we note that AI and intelligence are progressively moving from the cloud to the edge. The success of Edge-AI is pivoted on innovative circuits and hardware that can enable inference and limited learning in resource-constrained edge autonomous systems. This paper introduces a series of ultra-low-power accelerator and system designs on enabling the intelligence in edge robotic platforms, including reinforcement learning neuromorphic control, swarm intelligence, and simultaneous mapping and localization. We put an emphasis on the impact of the mixed-signal circuit, neuro-inspired computing system, benchmarking and software infrastructure, as well as algorithm-hardware co-design to realize the most energy-efficient Edge-AI ASICs for the next-generation intelligent and autonomous systems.

## I. INTRODUCTION

With intelligence marching from the cloud to the edge, autonomous robots are rising in real-world deployment. They require data to be processed from sensing to actuation in a closed-loop manner. The onboard circuits typically take power from the battery, limiting supported operational time. Recently, with neural networks being deployed at the edge, the demanding real-time performance and energy constraints are becoming increasingly difficult to achieve. Aerial platforms have an additional constraint of payload which limits the weight of the onboard sensors and compute. For tiny terrestrial robots, the form factor becomes a crucial requirement. Therefore, there is a strong need to develop energy-efficient compute platforms and processing frameworks to enable robotic edge intelligence.

Several hardware platforms have been used for robotic applications. CPUs and GPUs are designed to handle a wide range of robotic tasks and algorithms development. However, they usually consume 10-100 W of power, which are orders of magnitude higher than available resources on edge robotic systems. Edge processors like Jetson Nano and Google TPU have been used for programmability at a smaller form factor for faster system-level prototyping [1]. FPGAs are attracting attention due to its reconfigurability and hardware-efficiency, and have been presented for robotic perception [2], [3], localization [4], [5], and planning [6], [7]. The partial reconfiguration technique takes this flexibility one step further,

where part of FPGA resources can be reconfigured at runtime without compromising the other parts of applications [8], [9].

Edge-robotic specialized ASICs boost the energy-efficiency and customization even further. The constrained power budget on edge robots requires these chips to have a few mW of power consumption. For robotic perception, Jeon et al. [10] present a feature extraction accelerator at 2.7 mW power for micro aerial vehicles. For robotic autonomous navigation, Navion [11] accelerates the visual-inertial odometry of nano drones, Li et al. [12] speed up mutual information computation, and Li et al. [13] combine neural network with physical localization model with proposed specialized accelerators. For end-to-end learning-based robotic control, Kim et al. [14] develop a reinforcement learning accelerator for micro drones with 1.1 mW power consumption. For multi-robots scenarios, Honkote et al. [15] design a low-power SoC for distributed and collaborative swarm robot systems. Different techniques ranging from voltage-mode circuits [16], quantized neural networks [17]–[19] and sparse coding [20] have been utilized in restricting the power consumption. Several neural network accelerators have been proposed for general vision applications [21] which can be readily applied to robotic tasks.

Apart from energy consumption, memory bandwidth availability also becomes critical for high-speed edge robotic applications. A newer type of visual sensor called event cameras is being explored for such scenarios. Event cameras provide a stream of asynchronous events, and only part of frames are processed at every time instance, allowing high bandwidth, high speed, and high dynamic range [22]. System-level applications of this include a 3 ms latency robotic goalie [23] and looming obstacle avoiding drone [24]. The event-based processing modality of event cameras also lends itself naturally to processing bio-inspired spiking neural networks that benefit from data sparsity and low power. Tasks like lane detection and prey capturing [25] have been demonstrated using spiking neural networks and event camera pairs.

In this paper, we will show a series of our proposed ultra-low-power accelerators and system demonstrations for edge robotics, with an emphasis on circuit and system technologies. These demonstrations augment the large landscape of edge

robotic systems in reinforcement and swarm learning and neuro-inspired computing technologies. Section II presents a time-domain mixed-signal accelerator that supports embedded reinforcement learning control. Section IV introduces a hybrid-digital mixed-signal hardware design to enable edge swarm intelligence. Section IV presents an oscillator-based hardware platform for neuro-inspired mapping, localization, and control. Section V further provides benchmarking and simulation frameworks for cross-layer robotic workload evaluation. The paper concludes with challenges and opportunities for next-generation hardware-efficient robotic computing (Section VI).

## II. REINFORCEMENT LEARNING ON THE EDGE

This section presents our reinforcement learning neuromorphic accelerator for robotic autonomous navigation and exploration [26], [27]. We propose an energy-efficient time-domain mixed-signal computational framework to enable ultra-low-power operations.

### A. Reinforcement Learning Algorithm

Achieving true autonomy requires robots to perform continuous learning through frequently interacting with environments. Reinforcement learning (RL) is such a paradigm where robots take actions in environments to maximize the notion of cumulative reward. Among all RL algorithms, Q-learning is one of the well-studied techniques, which is implemented in this design. Q-learning seeks to find the optimal action policy ( $A_t$ ) given the current state ( $S_t$ ) to maximizes the reward ( $R_t$ ). It works on the principle of the action-value function [ $Q(S_t, A_t)$ ], where  $Q$  is iteratively updated from Bellman equation. For a detailed overview of RL algorithms and applications, interested readers are referred to [28].

### B. Circuit and System of RL Neuromorphic Accelerator

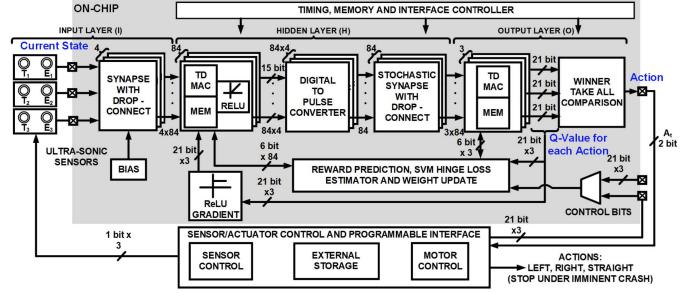
#### 1) Overview:

Fig. 1 shows the system diagram of our RL neuromorphic accelerator. It consists of ultrasonic sensors, an RL test chip, a Raspberry Pi-based micro-controller, and motor drivers.

The ultrasonic sensors feed depth information to the input layer of the neural network through an array of stochastic synapses. A three-layer neural network is implemented to process sensor data and generate actions that robots will follow. The micro-controller stores ( $S_t, A_t, R_t, S_{t+1}$ ) in a scratchpad memory during training and sends action commands from the chip to the motor controllers.

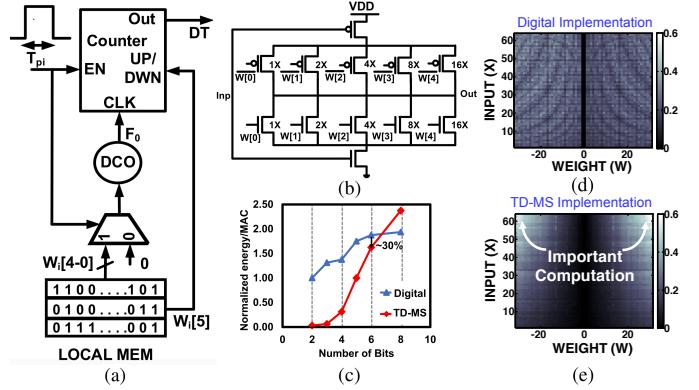
#### 2) Time-Domain Mixed-Signal Circuits:

To enable low-power edge intelligence on the robotic platform with low bit precision, we propose a time-domain mixed-signal (TD-MS) computational framework for energy-efficient and accurate operations. Fig. 2a illustrates the TD-MS multiply-and-accumulate (MAC) unit. A pulse input from sensor or hidden layers is used to enable the up-down counter that is triggered by a digitally controlled oscillator (DCO). The output of the counter is the product of weight  $W_i$  (digital) and pulse width  $T_{pi}$  of the gating signal (analog).



**Fig. 1:** The system architecture of our RL neuromorphic accelerator, including different circuit blocks and the interface to the external micro-controllers and motor drivers.

The proposed TD-MS design demonstrates unique advantages: 1) improved energy-efficiency at lower bit width compared to digital MAC operation (Fig. 2c); (2) the energy to compute is proportional to the significance of the computation - a feature in human brain but missing in digital logic (Fig. 2d-2e); (3) 45% lower system area, 47% lower interconnect power and 16% lower leakage power compared to digital design.



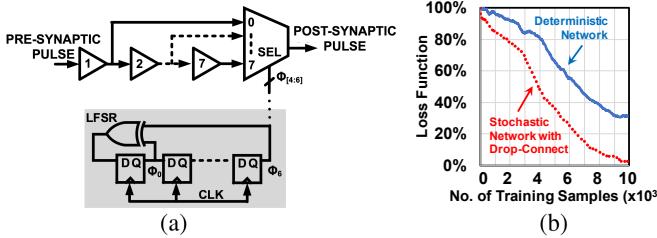
**Fig. 2:** (a) Proposed Time-Domain Mixed-Signal (TD-MS) MAC unit. (b) Digitally controlled oscillator (DCO) in TD-MS unit. (c) Computational energy per MAC for digital and TD-MS design with different bit precision at 0.6 V. (d)(e) 2-D energy per MAC surface for digital and TD-MS design with 6-bit inputs at 0.6 V.

#### 3) Enabling Regularization via Stochasticity:

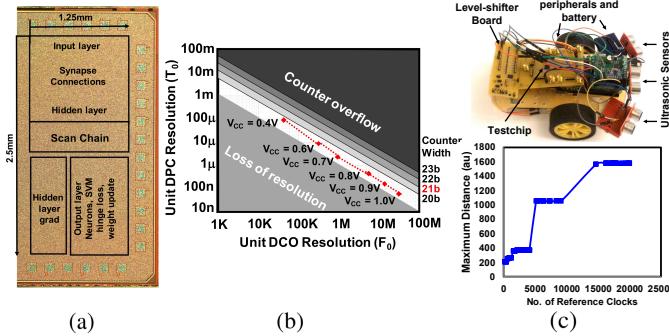
To help generalize the learned neural network model to unknown environments, we introduce stochasticity to synapses with drop-connect. As shown in Fig. 3a, the stochasticity is implemented with a buffer chain whose delays are randomly altered by a local high-speed linear-feedback-shift register (LFSR). Compared to the deterministic model, the stochastic network can achieve  $1.7\times$  speedup in convergence (Fig. 3b).

#### C. Evaluation

The RL neuromorphic test chip is implemented and taped-out in 55 nm CMOS process (Fig. 4a). By exploring design space of proposed TD-MS circuits, we show that the chip can ensure correct functionality and voltage scalability from 1.0 V down to 0.4 V (Fig. 4b). The chip is mounted on a tiny mobile robot for autonomous exploration and learning. Fig. 4c illustrates the increasing moved distance when robot continuously explores the space in the presence of obstacles.



**Fig. 3:** (a) Stochasticity is implemented by introducing varying delays between bit transitions using the linear-feedback-shift register (LFSR). (b) Stochasticity accelerates policy convergence.



**Fig. 4:** (a) RL neuromorphic chip die-photo. (b) Design space showing scalability till 0.4 V. (c) Mobile robot system and its covered distance as a function of the number of clock cycles or iterations.

### III. SWARM INTELLIGENCE ON THE EDGE

Going beyond single tasks, when facing a variety of tasks, swarms of robots usually collaborate with each other to solve problems. This section presents our energy-efficient hardware accelerator that enables swarm robotic applications [29], [30].

#### A. Swarm Intelligence Algorithms

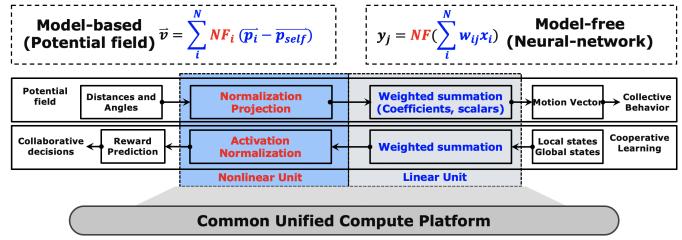
Swarm algorithms can be broadly classified into two categories, ones based on physical and mathematical models (model-based) and ones based on learning (model-free). Among model-based algorithms, artificial potential field (APF) is a commonly-used approach for collaborative path planning, where the motion force is obtained by aggregating the attractive and repulsive potential field. Model-free algorithms usually allow each robot to learn continuously to establish a model with real-world knowledge without human intervention. RL-based cooperative algorithms have shown great promise. Interested readers are directed to [31] for more details.

Interestingly, we observe that both model-based and model-free autonomy paradigms have similar mathematical structures (Fig. 5). Therefore, we identify the commonalities and develop a unified architecture to support real-time swarm intelligence.

#### B. Circuit and System of Swarm Intelligence Accelerator

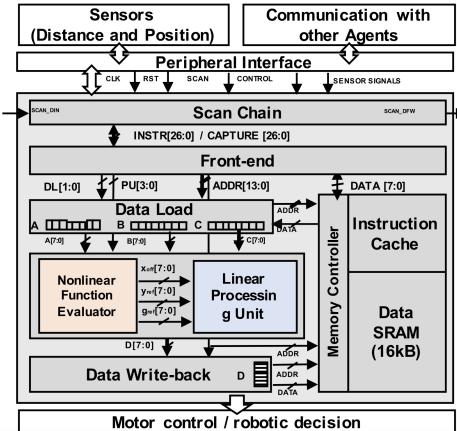
##### 1) Overview:

The system architecture of our swarm intelligence accelerator is shown in Fig. 6. Noticing that both model-based and model-free are combinations of nonlinear and linear operations, we design a nonlinear function evaluator (NFE)



**Fig. 5:** Common unified compute paradigm that supports both model-based and model-free swarm algorithms.

and linear processing unit (LPU). NFE supports nonlinear operations by using a piecewise linear approximation of nonlinear functions. LPU supports all addition and multiplication linear operations. Most operations are implemented in the digital domain except for MAC that leverages mixed-signal computing. The datapath of NFE and LPU is bi-directional, so data can move between each other seamlessly and preserve locality. We also observe that several required functions show symmetry and periodicity, which provides a further chance to reduce the number of computations and comparisons.



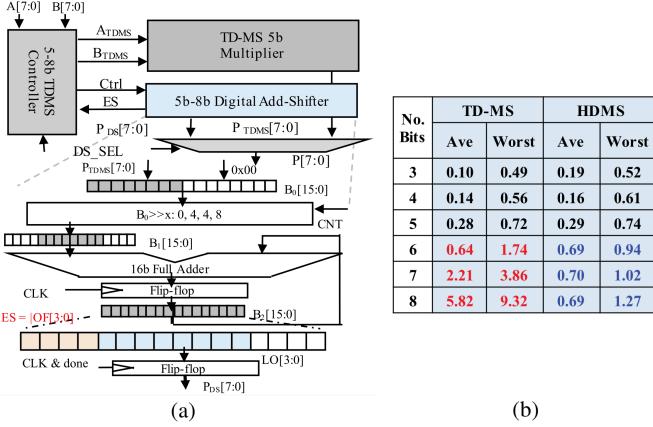
**Fig. 6:** The system architecture of our swarm intelligence accelerator, supporting both swarm-based and swarm-free autonomy paradigms with a nonlinear function evaluator and linear processing unit.

##### 2) Hybrid-Digital Mixed-Signal Circuits Architecture:

Swarm algorithms need to support various swarm sizes in dynamic environments. The required bit precision will increase from 3-bit to 8-bit, with swarm size increasing from 2 agents to 20 agents. TD-MS MACs show energy advantages over digital counterparts for low bit width, but exhibit higher energy with increasing operand size (Fig. 2c). To address this issue, we propose a hybrid-digital mixed-signal (HD-MS) MAC kernel, where computation is purely TD-MS for bit-width  $\leq 5$ , and hybrid of TD-MS and digital for  $6 \leq \text{bit-width} \leq 8$ .

Fig. 7a shows the circuit schematic of the HD-MS design. The HD-MS MAC kernel consists of a conventional TD-MS multiplier, a 5-8-bit TD-MS controller, and a 5-8-bit digital adder-shifter. The TD-MS multiplier computes  $\leq 5$ -bit operation. The TD-MS controller and digital adder-shifter reconfigure the multiplier to a higher bit width with seamless

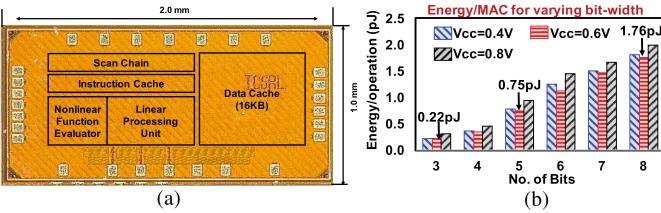
shift-and-add operations. Fig. 7b demonstrates that HD-MS have energy-benefits at higher precision compared with TD-MS. Compared with digital implementation, HD-MS exhibits 81% (for 3-bit) to 31% (for 8-bit) energy per MAC reduction.



**Fig. 7:** (a) Circuit schematic of the HD-MS design, including the 5-bit TD-MS kernel and the digital peripherals to enable efficient scaling to 8-bit. (b) Energy/MAC (normalized to a digital implementation) for TD-MS and HD-MS implementations. We observe that HD-MS outperforms TD-MS and digital for large swarm sizes.

### C. Evaluation

Our swarm intelligence accelerator is fabricated in 65 nm CMOS process (Fig. 8a). Fig. 8b demonstrates its scalability with bit precision, indicating a peak energy efficiency of 0.22 pJ/MAC (for 3-bit) and 1.76 pJ/MAC (for 8-bit). The average energy efficiency varies from 9.1 TOPS/W (for 3-bit) to 1.1 TOPS/W (for 8-bit). This bit precision scalability allows efficient computation for various swarm sizes.

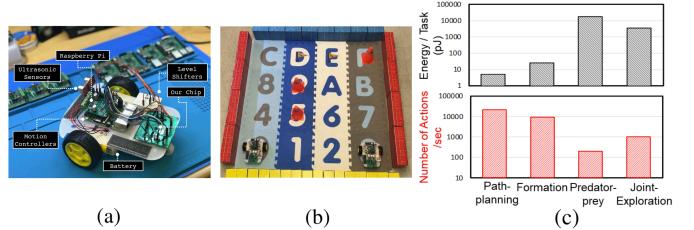


**Fig. 8:** (a) Swarm intelligence chip die-photo. (b) Measured energy per MAC across different bit widths at VCC = 0.4, 0.6, and 0.8 V.

We mounted the chip on a robotic car (Fig. 9a and Fig. 9b). The platform interfaces with a Raspberry Pi, sensors, motor controllers, and radios. We implement four exemplified swarm intelligence algorithms, namely path planning, pattern formation, predator-prey, and joint-exploration, where the first two are model-based and the last two are model-free. Fig. 9c shows large variations in energy consumption and the number of actions for each task, illustrating that future robotic platforms need to support a wide variety of algorithms, as the complexities of environments and task can dramatically change.

## IV. NEURO-INSPIRED COMPUTING ON THE EDGE

Recently, spiking neural networks (SNNs), with bio-inspired sparse spike-based temporally coded computing, offer an

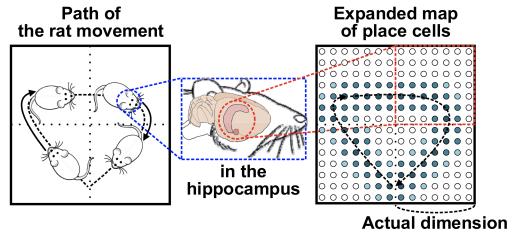


**Fig. 9:** (a) Our swarm intelligence accelerator is mounted on a robotic car with peripheral circuits. (b) Experimental setup. (c) Energy and performance for different template swarm algorithms.

energy-efficient alternative for edge robotic tasks. This section presents our proposed incorporation of SNNs for SLAM and prey tasks for ultra-low-power robotic applications [32], [33].

### A. Simultaneous Localization and Mapping Algorithms

Simultaneous localization and mapping (SLAM) forms an essential component of many autonomous navigation applications. SLAM algorithms can be broadly classified into two categories: visual-based and neuro-based. Visual-based SLAM requires the robot to identify its position from the beginning of motion and generate a map of the movement using only the images captured during motion. Previous approaches like probabilistic SLAM and keyframe-based SLAM remain inadequate due to the constrained power budget of edge systems. Neuro-based SLAM performs the computation in a more energy-efficient way and is applicable to ultra-low-power edge robotics. Neuroscientific exploration in rodent brains showed their phenomenal capacity to efficiently localize themselves (Fig. 10). Place cells and head direction cells are identified as neuronal circuits tuned to respond at a particular position and direction of motion, respectively. Our NeuroSLAM accelerator takes inspiration from RatSLAM [34] algorithm that mimics the neuromorphic connectivity and incorporates bio-inspired hardware to achieve ultra-low-power SLAM tasks.



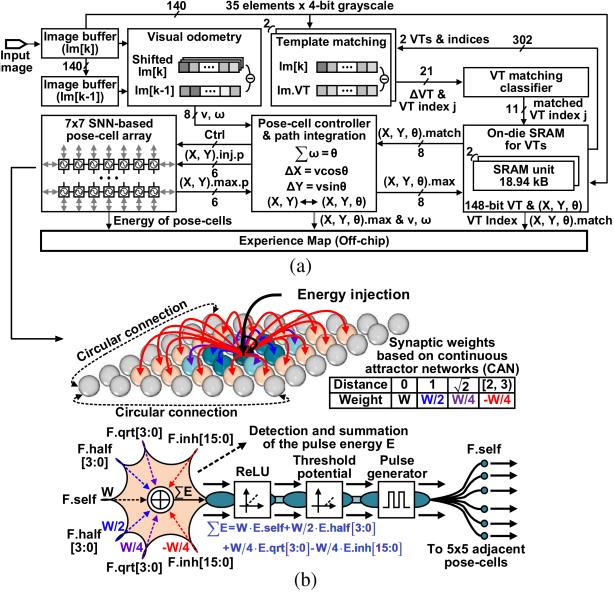
**Fig. 10:** Mapping between the position of rodent and the excited place cells in rodent's brain

### B. Circuit and System of NeuroSLAM Accelerator

#### 1) Architecture and Circuit Block:

The flow of data in the NeuroSLAM accelerator is shown in Fig. 11a, where the captured image is first compared with the previous image for visual odometry to estimate the displacement from previous image capture. This is followed by template matching with previous images to detect any possibility of loop closure. The translation is added with the previous position to find the current direction of motion with digital head direction cells, and the path integration is injected

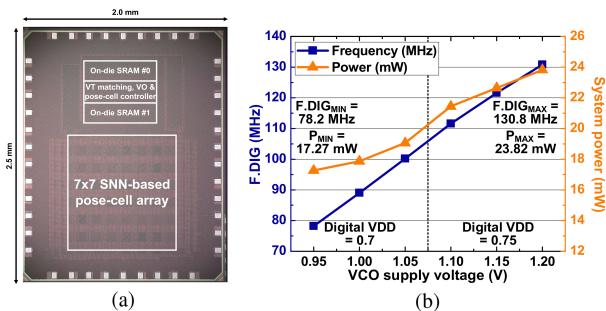
in the pose cell array. Pose cell array is made of oscillator-based continuous attractor network in spiking neural network fashion, as shown in Fig. 11b. The output is extracted to calculate the experience map.



**Fig. 11:** (a) Overview of our NeuroSLAM accelerator. (b) Spiking continuous attractor network mimicking rodent’s pose cell behavior.

## 2) Test Chip Measurement:

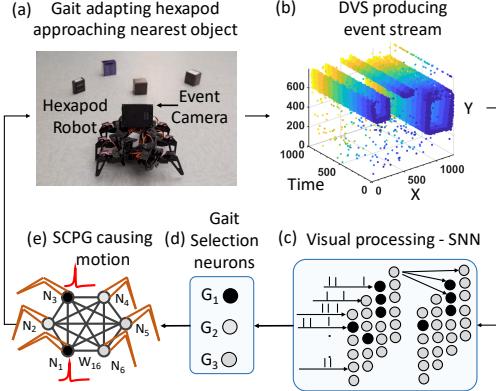
The NeuroSLAM test chip is fabricated in 65 nm technology (Fig. 12a). The template matching, odometry, and path integration are carried out in low-bit resolution with an efficient attractor network. The chip achieves SLAM with only 23.82 mW. The dependence of power consumption on input voltage is shown in Fig. 12b. The attractor network shows a high compute efficiency of 8.79 TOPS/W. Our NeuroSLAM accelerator demonstrates the incorporation of neuro-inspired analog hardware in the digital pipeline to enable edge intelligence in severe energy-constrained systems.



**Fig. 12:** (a) NeuroSLAM chip die-photo. (b) Measured operational frequency and power consumption of NeuroSLAM accelerator.

## C. Neuro-Inspired End-to-End Spike-Only Processing

Another neuro-inspired system exploration is the first autonomous sensing-to-actuation end-to-end spike-only processing pipeline for hexapod robots [35]. The goal is to demonstrate the functionality of spike-only processing and evaluate the potential of event-driven processing modalities. As shown



**Fig. 13:** Bio-inspired closed-loop end-to-end spike-only robot. (a) Event camera mounted on hexapod provides (b) input stream to (c) SNN for processing and (d) selecting gait to approach the nearest object. (e) Gait is executed by a spiking CPG causing leg movements.

in Fig. 13, event camera/dynamic vision sensor (DVS) is used as the sensory input to generate asynchronous event stream. The information is processed through SNN to activate one of the three gait selection neurons. The central pattern generator (CPG) is trained such that every gait selection neuron activates gait in a different direction to allow controlled movement. A task of identifying and approaching the nearest target is demonstrated using this platform. The ultra-low-power (2.55 mJ/step) consumption of this system with dedicated spiking hardware (e.g., Loihi) highlights the potential of neuro-inspired event-driven systems for edge applications.

## V. BENCHMARKING AND SOFTWARE INFRASTRUCTURE

Edge robotics is a cross-layer research field, spanning from environment modeling, autonomy algorithms, runtime systems to onboard compute architecture and circuits. The interaction between the layers impacts the efficacy and performance of the system [36], requiring software infrastructure for interdisciplinary research. Specially, we need a platform that can systematically benchmark each of these individual layers and also capture end-to-end cross-layer execution characteristics. Recently, some platforms for aerial robots have been proposed. MAVBench [37] is a platform for physical-model-based aerial robots evaluation. MAVBench involves a closed-loop simulator and a benchmark suite for several computational kernels involving perception, planning, and control. Airlearning [38] and PEDRA [39] are simulation suits and benchmarks for learning-based aerial edge robots. They provide a rich set of virtual worlds, including indoor and outdoor environments, to enable autonomy generalization. In addition, PEDRA supports swarm intelligence with different collaboration paradigms.

These benchmarking and software infrastructures inspire a proliferation of studies on edge robotic systems, such as reliability, system design methodology, and memory hierarchy optimization. Based on MAVBench, RoboRun [40] presents a robot runtime that leverages spatial-aware computing to dynamically improve performance and energy for heterogeneous operating environments. MAVFI [41] proposes a fault injection framework for end-to-end reliability characterization of robotic workload, which is portable to robot operating

system (ROS)-based applications. Based on AirLearning, Skyline [42], Autopilot [43], and AutoSoC [44] propose a visual performance model and automated design space exploration framework to design optimal onboard compute for aerial robots. Based on PEDRA, Anwar et al. [45] present a transfer learning-based approach to reduce the onboard computation required to train a neural network for autonomous navigation. Wan et al. [46] and FRL-FI [47] propose application-aware lightweight fault detection and mitigation techniques to enable reliable autonomy under hardware faults, for both learning-based and swarm-based intelligence. Zeng et al. [48] develop a mathematical framework for solving multi-task reinforcement learning problems based on policy gradient method. Anwar et al. [49] evaluate the robustness of swarm robotic systems under adversaries. Yoon et al. [50] present a novel hierarchically memory system with STT-MRAM and SRAM to support real-time learning-based robotic exploration. We believe a holistic benchmarking and simulator infrastructure will uncover more cross-layer research findings of various fields of edge robotics.

## VI. CHALLENGES AND OPPORTUNITIES

Robotic computing is a rising area and opens many research challenges and opportunities. At the device and circuit level, embedded non-volatile memory (e.g., RRAM, Ferroelectric memories) and monolithic 3D integration will provide opportunities for high-performance and energy-efficient robotic computing. At the architecture level, the robotic computing platform needs to be adaptive and reconfigurable to various scenarios and support a diverse set of applications, including both DNNs and SNNs. At the system level, a holistic benchmarking suite and a generic framework for mapping autonomy algorithms to heterogeneous hardware platforms will benefit the robotic computing development process. At the algorithm level, robots need to have the ability of lifelong learning and learning with sparse and limited data. The booming of swarm intelligence requires more effective and robust distributed learning across multiple agents.

## VII. CONCLUSION

This paper investigates circuit and system technologies for energy-efficient edge robotics. We present three robotic accelerators for edge reinforcement learning, swarm intelligence, and neuron-inspired mapping and localization, with an emphasis on novel mixed-signal circuit technologies. We summarize robotic benchmarking and simulation frameworks along with how they foster research efforts in cross-layer robotic systems. Finally, we discuss the challenges and opportunities for the next-generation energy-efficient robotic computing platforms.

## ACKNOWLEDGEMENTS

The authors would like to thank Anvesha Amaravati, Saad Bin Nasir, Insik Yoon, Ningyuan Cao, Muya Chang, Jong-Hyeok Yoon, Aqeel Anwar Malik, and Justin Ting for their technical support. This work was supported in part by C-BRIC, one of six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA.

## REFERENCES

- [1] S. Chinchali, A. Sharma, J. Harrison, A. Elhafsi, D. Kang, E. Pergament, E. Cidon, S. Katti, and M. Pavone, "Network offloading policies for cloud robotics: a learning-based approach," *Autonomous Robots*, vol. 45, no. 7, pp. 997–1012, 2021.
- [2] T. Gao, Z. Wan, Y. Zhang, B. Yu, Y. Zhang, S. Liu, and A. Raychowdhury, "Ielas: An elas-based energy-efficient accelerator for real-time stereo matching on fpga platform," in *2021 IEEE 3rd International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, pp. 1–4, IEEE, 2021.
- [3] Z. Wan, Y. Zhang, A. Raychowdhury, B. Yu, Y. Zhang, and S. Liu, "An energy-efficient quad-camera visual system for autonomous machines on fpga platform," in *2021 IEEE 3rd International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, pp. 1–4, IEEE, 2021.
- [4] W. Liu, B. Yu, Y. Gan, Q. Liu, J. Tang, S. Liu, and Y. Zhu, "Archytas: A framework for synthesizing and dynamically optimizing accelerators for robotic localization," in *MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture*, pp. 479–493, 2021.
- [5] Q. Liu, Z. Wan, B. Yu, W. Liu, S. Liu, and A. Raychowdhury, "An energy-efficient and runtime-reconfigurable fpga-based accelerator for robotic localization systems," *arXiv preprint arXiv:2202.08952*, 2022.
- [6] S. Murray, W. Floyd-Jones, Y. Qi, G. Konidaris, and D. J. Sorin, "The microarchitecture of a real-time robot motion planning accelerator," in *2016 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 1–12, IEEE, 2016.
- [7] S. M. Neuman, B. Plancher, T. Bourgeat, T. Tambe, S. Devadas, and V. J. Reddi, "Robomorphic computing: a design methodology for domain-specific accelerators parameterized by robot morphology," in *Proceedings of the 26th ACM International Conference on Architectural Support for Programming Languages and Operating Systems*, pp. 674–686, 2021.
- [8] Z. Wan, B. Yu, T. Y. Li, J. Tang, Y. Zhu, Y. Wang, A. Raychowdhury, and S. Liu, "A survey of fpga-based robotic computing," *IEEE Circuits and Systems Magazine*, vol. 21, no. 2, pp. 48–74, 2021.
- [9] S. Liu, Z. Wan, B. Yu, and Y. Wang, "Robotic computing on fpgas," *Synthesis Lectures on Computer Architecture*, vol. 16, no. 1, pp. 1–218, 2021.
- [10] D. Jeon, Y. Kim, I. Lee, Z. Zhang, D. Blaauw, and D. Sylvester, "A 470mv 2.7 mw feature extraction-accelerator for micro-autonomous vehicle navigation in 28nm cmos," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 166–167, IEEE, 2013.
- [11] A. Suleiman, Z. Zhang, L. Carlone, S. Karaman, and V. Sze, "Navion: A 2-mw fully integrated real-time visual-inertial odometry accelerator for autonomous navigation of nano drones," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 4, pp. 1106–1119, 2019.
- [12] P. Z. X. Li, *High-throughput computation of shannon mutual information on chip*, PhD thesis, Massachusetts Institute of Technology, 2020.
- [13] Z. Li, Y. Chen, L. Gong, L. Liu, D. Sylvester, D. Blaauw, and H.-S. Kim, "An 879gops 243mw 80fps vga fully visual cnn-slam processor for wide-range autonomous exploration," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 134–136, IEEE, 2019.
- [14] Y. Kim, D. Shin, J. Lee, Y. Lee, and H.-J. Yoo, "A 0.55 v 1.1 mw artificial intelligence processor with on-chip pvt compensation for autonomous mobile robots," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 2, pp. 567–580, 2017.
- [15] V. Honkote, D. Kurian, S. Muthukumar, D. Ghosh, S. Yada, K. Jain, B. Jackson, I. Klotchkov, M. R. Nimmagadda, S. Dattawadkar, et al., "2.4 a distributed autonomous and collaborative multi-robot system featuring a low-power robot soc in 22nm cmos for integrated battery-powered minibots," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 48–50, IEEE, 2019.
- [16] J. Zhang, Z. Wang, and N. Verma, "18.4 a matrix-multiplying adc implementing a machine-learning classifier directly with data conversion," in *2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers*, pp. 1–3, IEEE, 2015.
- [17] D. Bankman, L. Yang, B. Moons, M. Verhelst, and B. Murmann, "An always-on 3.8mu j/86% cifar-10 mixed-signal binary cnn processor with all memory on chip in 28-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 158–172, 2018.
- [18] M. Lam, S. Chitlangia, S. Krishnan, Z. Wan, G. Barth-Maron, A. Faust, and V. J. Reddi, "Quantized reinforcement learning (quarl)," *arXiv preprint arXiv:1910.01055*, 2019.

- [19] T. Tambe, E.-Y. Yang, Z. Wan, Y. Deng, V. J. Reddi, A. Rush, D. Brooks, and G.-Y. Wei, "Algorithm-hardware co-design of adaptive floating-point encodings for resilient deep learning inference," in *2020 57th ACM/IEEE Design Automation Conference (DAC)*, pp. 1–6, IEEE, 2020.
- [20] F. N. Buhler, P. Brown, J. Li, T. Chen, Z. Zhang, and M. P. Flynn, "A 3.43 tops/w 48.9 pj/pixel 50.1 nj/classification 512 analog neuron sparse coding neural network with on-chip learning and classification in 40nm cmos," in *2017 Symposium on VLSI Circuits*, pp. C30–C31, IEEE, 2017.
- [21] Y.-H. Chen, T. Krishna, J. S. Emer, and V. Sze, "Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks," *IEEE journal of solid-state circuits*, vol. 52, no. 1, pp. 127–138, 2016.
- [22] G. Gallego, T. Delbrück, G. Orchard, C. Bartolozzi, B. Taba, A. Censi, S. Leutenegger, A. J. Davison, J. Conradt, K. Daniilidis, et al., "Event-based vision: A survey," *IEEE transactions on pattern analysis and machine intelligence*, vol. 44, no. 1, pp. 154–180, 2020.
- [23] T. Delbrück and M. Lang, "Robotic goalie with 3 ms reaction time at 4% cpu load using event-based dynamic vision sensor," *Frontiers in neuroscience*, vol. 7, p. 223, 2013.
- [24] D. Falanga, K. Kleber, and D. Scaramuzza, "Dynamic obstacle avoidance for quadrotors with event cameras," *Science Robotics*, vol. 5, no. 40, p. eaaz9712, 2020.
- [25] L. Salt, G. Indiveri, and Y. Sandamirskaya, "Obstacle avoidance with lgmd neuron: towards a neuromorphic uav implementation," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, IEEE, 2017.
- [26] A. Amravati, S. B. Nasir, S. Thangadurai, I. Yoon, and A. Raychowdhury, "A 55nm time-domain mixed-signal neuromorphic accelerator with stochastic synapses and embedded reinforcement learning for autonomous micro-robots," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 124–126, IEEE, 2018.
- [27] A. Amravati, S. B. Nasir, J. Ting, I. Yoon, and A. Raychowdhury, "A 55-nm, 1.0–0.4 v, 1.25-pj/mac time-domain mixed-signal neuromorphic accelerator with stochastic synapses for reinforcement learning in autonomous mobile robots," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 75–87, 2018.
- [28] R. S. Sutton and A. G. Barto, *Reinforcement learning: An introduction*. MIT press, 2018.
- [29] N. Cao, M. Chang, and A. Raychowdhury, "14.1 a 65nm 1.1-to-9.1 tops/w hybrid-digital-mixed-signal computing platform for accelerating model-based and model-free swarm robotics," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 222–224, IEEE, 2019.
- [30] N. Cao, M. Chang, and A. Raychowdhury, "A 65-nm 8-to-3-b 1.0–0.36-v 9.1–1.1-tops/w hybrid-digital-mixed-signal computing platform for accelerating swarm robotics," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 1, pp. 49–59, 2019.
- [31] H. M. La, R. Lim, and W. Sheng, "Multirobot cooperative learning for predator avoidance," *IEEE Transactions on Control Systems Technology*, vol. 23, no. 1, pp. 52–63, 2014.
- [32] J.-H. Yoon and A. Raychowdhury, "31.1 a 65nm 8.79 tops/w 23.82 mw mixed-signal oscillator-based neuroslam accelerator for applications in edge robotics," in *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 478–480, IEEE, 2020.
- [33] J.-H. Yoon and A. Raychowdhury, "Neuroslam: A 65-nm 7.25-to-8.79-tops/w mixed-signal oscillator-based slam accelerator for edge robotics," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 1, pp. 66–78, 2020.
- [34] M. J. Milford and G. F. Wyeth, "Mapping a suburb with a single camera using a biologically inspired slam system," *IEEE Transactions on Robotics*, vol. 24, no. 5, pp. 1038–1053, 2008.
- [35] A. Lele, Y. Fang, J. Ting, and A. Raychowdhury, "An end-to-end spiking neural network platform for edge robotics: From event-cameras to central pattern generation," *IEEE Transactions on Cognitive and Developmental Systems*, 2021.
- [36] S. Krishnan, Z. Wan, K. Bhardwaj, P. Whatmough, A. Faust, G.-Y. Wei, D. Brooks, and V. J. Reddi, "The sky is not the limit: A visual performance model for cyber-physical co-design in autonomous machines," *IEEE Computer Architecture Letters*, vol. 19, no. 1, pp. 38–42, 2020.
- [37] B. Boroujerdian, H. Genc, S. Krishnan, W. Cui, A. Faust, and V. Reddi, "Mavbench: Micro aerial vehicle benchmarking," in *2018 51st annual IEEE/ACM international symposium on microarchitecture (MICRO)*, pp. 894–907, IEEE, 2018.
- [38] S. Krishnan, B. Boroujerdian, W. Fu, A. Faust, and V. J. Reddi, "Air learning: An ai research platform for algorithm-hardware benchmarking of autonomous aerial robots," *arXiv preprint arXiv:1906.00421*, 2019.
- [39] M. A. Anwar and A. Raychowdhury, "Navren-rl: Learning to fly in real environment via end-to-end deep reinforcement learning using monocular images," in *2018 25th International Conference on Mechatronics and Machine Vision in Practice (M2VIP)*, pp. 1–6, IEEE, 2018.
- [40] B. Boroujerdian, R. Ghosal, J. Cruz, B. Plancher, and V. J. Reddi, "Roborun: A robot runtime to exploit spatial heterogeneity," in *2021 58th ACM/IEEE Design Automation Conference (DAC)*, pp. 829–834, IEEE, 2021.
- [41] Y.-S. Hsiao, Z. Wan, T. Jia, R. Ghosal, A. Raychowdhury, D. Brooks, G.-Y. Wei, and V. J. Reddi, "Mavfi: An end-to-end fault analysis framework with anomaly detection and recovery for micro aerial vehicles," *arXiv preprint arXiv:2105.12882*, 2021.
- [42] S. K. Z. Wan, K. Bhardwaj, A. Faust, and V. J. Reddi, "Roofline model for uavs: A bottleneck analysis tool for designing compute systems for autonomous drones," *arXiv preprint arXiv:2111.03792*, 2021.
- [43] S. Krishnan, Z. Wan, K. Bharadwaj, P. Whatmough, A. Faust, S. Neuman, G.-Y. Wei, D. Brooks, and V. Janapa Reddi, "Machine learning-based automated design space exploration for autonomous aerial robots," *arXiv e-prints*, pp. arXiv–2102, 2021.
- [44] S. Krishnan, T. Tambe, Z. Wan, and V. J. Reddi, "Autosoc: Automating algorithm-soc co-design for aerial robots," *arXiv preprint arXiv:2109.05683*, 2021.
- [45] A. Anwar and A. Raychowdhury, "Autonomous navigation via deep reinforcement learning for resource constraint edge nodes using transfer learning," *IEEE Access*, vol. 8, pp. 26549–26560, 2020.
- [46] Z. Wan, A. Anwar, Y.-S. Hsiao, T. Jia, V. J. Reddi, and A. Raychowdhury, "Analyzing and improving fault tolerance of learning-based navigation systems," in *2021 58th ACM/IEEE Design Automation Conference (DAC)*, pp. 841–846, IEEE, 2021.
- [47] Z. Wan, A. Anwar, A. Mahmoud, T. Jia, Y.-S. Hsiao, V. J. Reddi, and A. Raychowdhury, "Frl-fi: Transient fault analysis for federated reinforcement learning-based navigation systems," in *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, IEEE, 2022.
- [48] S. Zeng, M. A. Anwar, T. T. Doan, A. Raychowdhury, and J. Romberg, "A decentralized policy gradient approach to multi-task reinforcement learning," in *Uncertainty in Artificial Intelligence*, pp. 1002–1012, PMLR, 2021.
- [49] A. Anwar and A. Raychowdhury, "Multi-task federated reinforcement learning with adversaries," *arXiv preprint arXiv:2103.06473*, 2021.
- [50] I. Yoon, M. A. Anwar, R. V. Joshi, T. Rakshit, and A. Raychowdhury, "Hierarchical memory system with stt-mram and sram to support transfer and real-time reinforcement learning in autonomous drones," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 9, no. 3, pp. 485–497, 2019.