CASE STUDY ON CENTRAL PROCESSING UNIT

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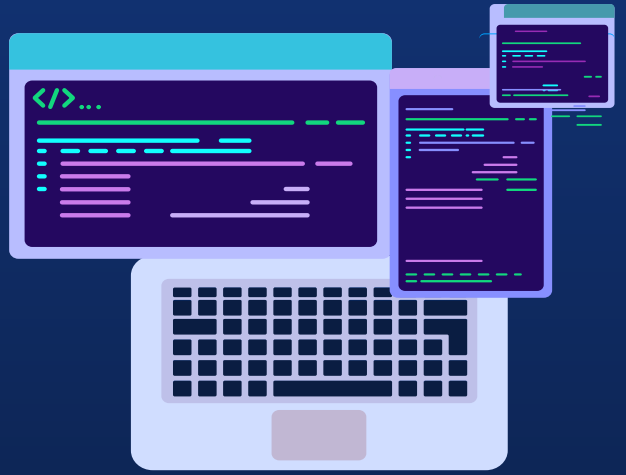

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COMPUTER ORGANIZATION AND ARCHITECTURE

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INTRODUCTION

A **central processing unit** (**CPU**) is the electronic circuitry within a computer that carries out the instructions of a computer program by performing the basic arithmetic, logical, control and input/output (I/O) operations specified by the instructions. It is the heart and brain of a computer, as it receives data input, executes instruction and processes information. It also communicates with I/O devices, which send and receive data to and from the CPU

The term has been used in the computer industry at least since the early 1960s. Traditionally, the term CPU refers to a processor, more specifically to its processing unit and control unit CU, distinguishing these core elements of a computer from external components such as main memory and IO circuitry. The central processing unit also completed all processing for any attached peripheral devices. Modern peripheral devices have a significant amount of processing power themselves and off load some processing tasks from CPU. We retain the term CPU today, but now it refers to the processor package on a typical motherboard.

Charles Babbage was considered to be the father of computing after his concept and later the invention of Analytical Engine. Again, many other is also considered many people as father of computer including Alan Turing, John Von Neumann etc.

HISTORY

1st generation	2nd generation	3rd generation	4th generation	5th generation
1946-1956 period	1956-1965 period	1965-1971 period	1971-1980 period	1980-today's period
Used vacuum tubes	Used transistors	Used IC (integrated circuit)	Used microprocessor	Based on artificial intelligence
Filled the whole building	Filled the entire room	Smallest than 2nd generation	small	Different sizes and unique features
Could calculate in milliseconds	Could calculate in microseconds	Could calculate in nanoseconds	Fastest in competition and size reduced	More reliable and works faster
Small amount of information for magnetic drums	Better portability than 1st generation	Fast and reliable and big storage	Microprocessor very complex with high level language	User friendly interfaces with multimedia features

HISTORY

1st generation	2nd generation	3rd generation	4th generation	5th generation
Large amount of energy	Less energy	Concepts of time sharing and multiprogramming	Heat generated is negligible	Low- level language
Large cooling system	Punch cards for inputs	Air conditioning is needed	Air conditioning is needed	UISI used ultra large scale integration tech
Example : ENIAC , EVDAC, UNIVAC , IBM-650	Example : Honeywell 400, IBM 7094 , CDC 1604 UNIVAC 1108	Example: PDP-8, PDP-2, ICI 2900, IBM- 360 , IBM 370	Example : IBM- 4341 , DFC 10, STAR 1000, PUP 11	Example : Desktop , laptop , notebook , ultrabook .

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BEGINNING OF THE EVOLUTION OF CPU

VACUUM TUBE

It was first relay and vacuum tube based computer .it's functionality was depend on how fast it's switches execute it's clock speed and it's clock signal frequency was 100 KHZ to 4 mega Hz . which to less on comparison of nowadays computer

TRANSISTOR

The first improvement of CPUs came with the advent of the transistor.

During 1950s and 1960s, Transistor based computers had several distinct advantages over their predecessors. Aside form facilitating increased reliability and lower power consumption, transistors also allowed cpu s to operate at much higher speeds because of the short switching time of a transistor in comparison to a tube or relay. CPU clock rates in the tens of megahertz were obtained during this period.

SMALL INTEGRATION

The IC allowed a large number of transistors to be manufactured on a single semiconductor based chip. At first only very basic non specialized digital circuits such as NOR gates were miniaturized into ICs. CPU based upon these building blocks or IC is known as "small-scale integration" devices.To build an entire CPU out of SSI ICs required thousands of individual chips, but still consumed much less space and power than earlier discrete transistor designs.

BEGINNING OF THE EVOLUTION OF CPU

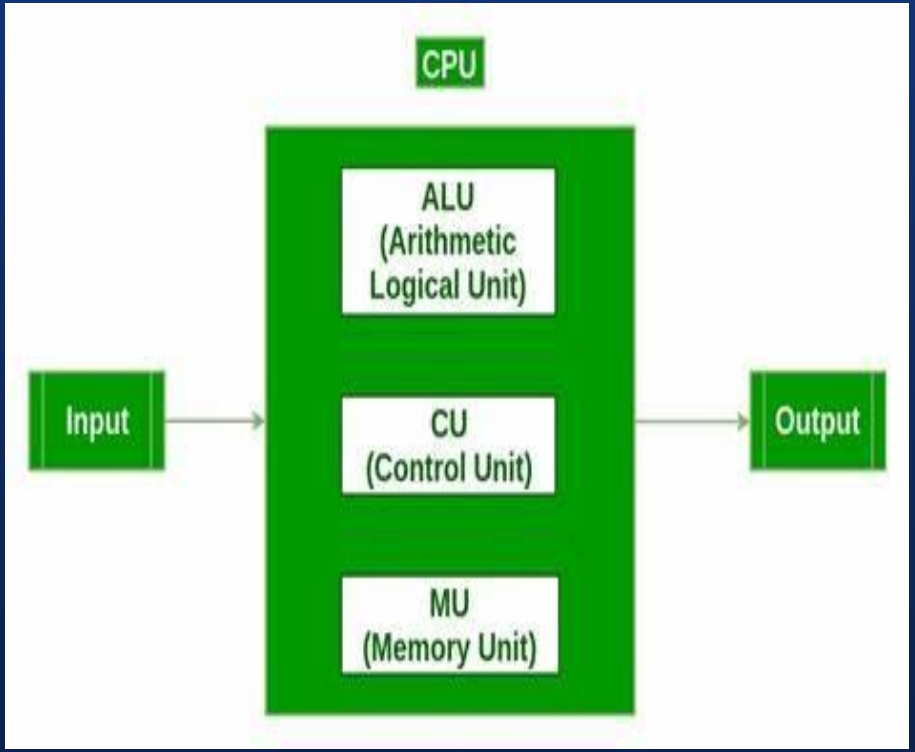
LARGE INTEGRATION

Large-scale integration (LSI) is the process of integrating or embedding thousands of transistors on a single silicon semiconductor microchip. LSI technology was conceived in the mid-1970s when computer processor microchips were under development. LSI is no longer in use.

LSI defines the technology used to build powerful microchips or integrated circuits (IC) in a very small form factor. It succeeded small-scale integration (SSI) and medium-scale integration (MSI), which included tens to hundreds of transistors per microchip. LSI consists of thousands of transistors that are closely embedded and integrated with a very small microchip . As the microelectronic technology advanced, an increasing number of transistors were placed on ICs, decreasing the quantity of individual ICs needed for a complete CPU. MSI and LSI ICs increased transistor counts to hundreds, and then thousands. By 1968, the number of ICs required to build a complete CPU had been reduced to 24 ICs of eight different types, with each IC containing roughly 1000 MOSFETs.

MICROPROCESSOR

A microprocessor is a computer processor where the data processing logic and control is included on a single integrated circuit, or a small number of integrated circuits. Microprocessor is a controlling unit fabricated on a small chip capable of performing ALU (Arithmetic Logical Unit) operations and communicating with the other devices connected to it. Microprocessor consists of an ALU, register array, and a control unit. ALU performs arithmetical and logical operations on the data received from the memory or an input device. Register array consists of registers and accumulator. The control unit controls the flow of data and instructions within the computer. There are some terms which are frequently used in a microprocessor . those are : instruction sets , bandwidth , clock rate , word length , data types . it has some advantages those are , it is cost-effective , lower power consumption , versatility , reliability and also small in size . the production of inexpensive microprocessors enabled computer engineers to develop microcomputers. Such computer systems are small but have enough computing power to perform many business, industrial, and scientific tasks.



STRUCTURE AND COMPONENTS OF CENTRAL PROCESSING UNIT

THE MAIN CPU MAINLY CONSIST OF THREE MAJOR PARTS:

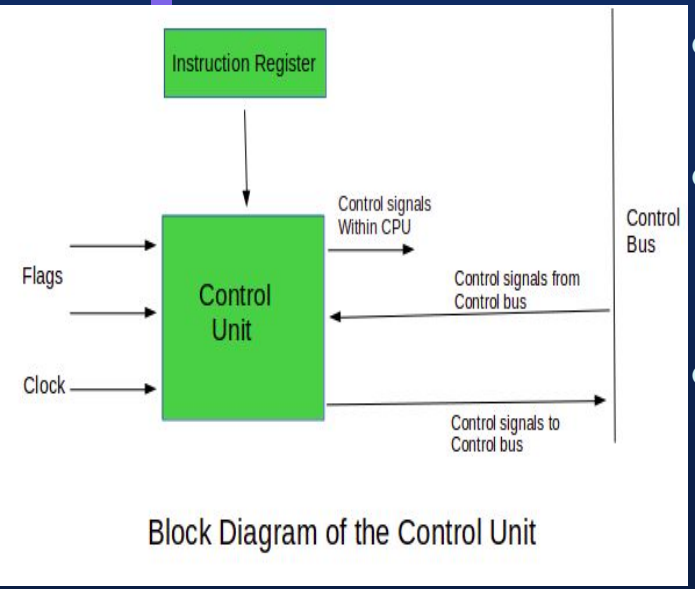
1. CONTROL UNIT
2. ARITHMETIC LOGIC UNIT
3. REGISTERS/ARRAY

01

MAJOR COMPONENTS OF CENTRAL PROCESSING UNIT

“CONTROL UNIT”

A **control unit** (CU) is an integrated circuit in a processor that controls the input and output. It receives instructions from a program, then passes them to the arithmetic logic **unit** (ALU).



Block Diagram of the Control Unit

- The control unit of CPU contains circuitry that uses electrical signals to direct the entire computer system to carry out the stored program instructions.
- The control unit does not execute program instructions; rather it directs other parts of the system to do so. The control unit communicates with both the ALU and memory.
- The control unit performs this function at a rate determined by the clock speed and is responsible for directing the operations of other units by using timing signals that extend throughout the CPU.

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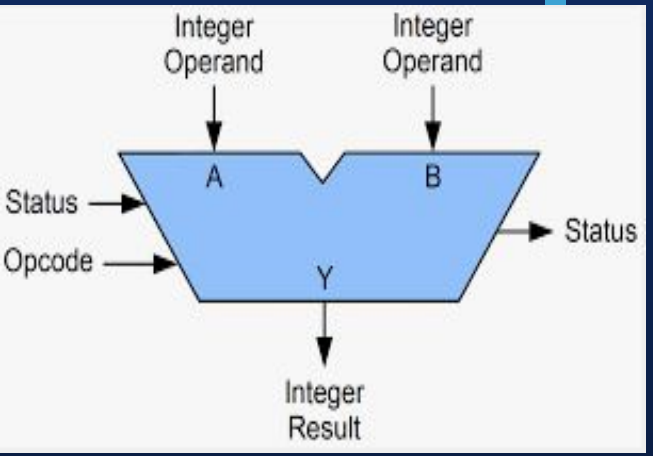
“ARITHMETIC LOGIC UNIT”



ALU means Arithmetic Logic Unit

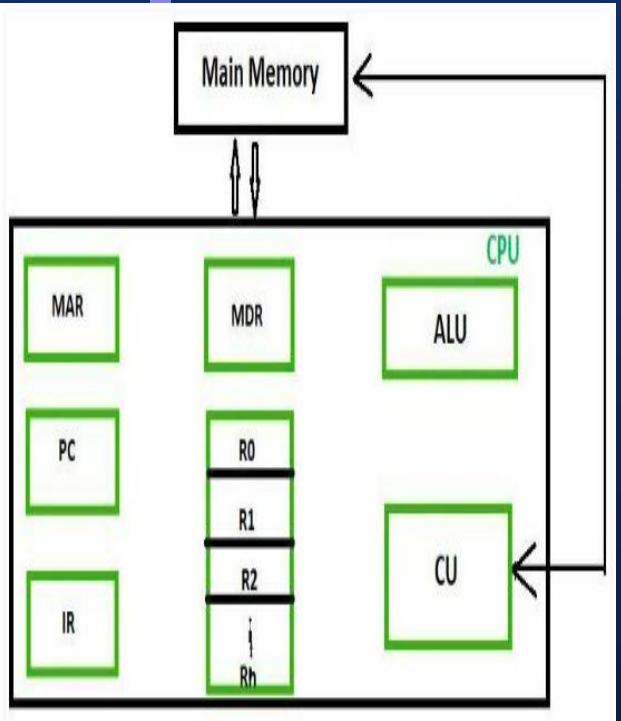
- It is a digital circuit within the processor that performs integer arithmetic and bitwise logic operations.
- It performs the arithmetic and logic functions that are the work of the computer.
- The inputs to the ALU are the data words to be operated on(called operands), status information from previous operations, and a code from the control unit indicating which operation to perform.
- Depending on the instruction being executed, the operands may come from internal CPU registers of external memory, or they may be constants generated by the ALU itself.
- The ALUs output consists of both data word, which may be stored in register or memory, and status information that is typically stored in a special, internal CPU register reserved for this purpose.

03

MAJOR COMPONENTS OF CENTRAL PROCESSING UNIT

“REGISTER/ ARRAY”

The registers used by the CPU are often termed as Processor registers.

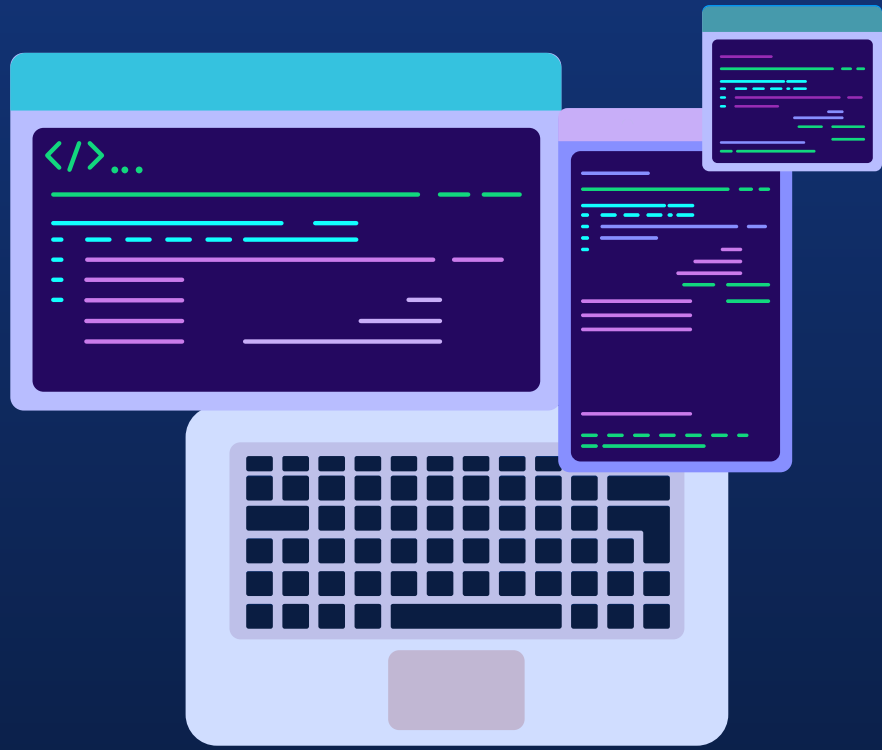


- Processor register is quickly accessible location available to digital processor CPU.
- Registers usually consist of a small amount of fast storage, although some registers have specific hardware functions, and may be read-only or write-only.
- A processor register may hold an instruction, a storage address, or any data(such as bit sequence or individual characters).
- The computer needs processor registers for manipulating data and a register for holding a memory address.
- Whether load store architecture or not, load data from a larger memory into registers where it is used for arithmetic operations and is manipulated or tested by machine instructions.
- Manipulated data is then often stored back to main memory, either by the same instruction or by a subsequent one.

TYPES OF CPU ORGANIZATION:

There are generally three types cpu organisations :

- Single Accumulator Organisation
- General Register
- Stack Organisations
  - ➔ Register Stack Organisations
  - ➔ Memory Stack Organisations



Single Accumulator Organisations :

The computers, present in the early days of computer history, had accumulator based CPUs. In this type of CPU organization, the accumulator register is used implicitly for processing all instructions of a program and store the results into the accumulator. The instruction format that is used by this CPU Organisation is **One address field**. Due to this the CPU is known as **One Address Machine**.

The format of instruction is:

Mode	Opcode	operand

The main points about Single Accumulator based CPU Organisation are:

1. In this CPU Organization, the first ALU operand is always stored into the Accumulator and the second operand is present either in Registers or in the Memory.
2. Accumulator is the default address thus after data manipulation the results are stored into the accumulator.
3. One address instruction is used in this type of organization.

Mainly two types of operation are performed in single accumulator based CPU organization:

1. **Data transfer operation –**
   In this type of operation, the data is transferred from a source to a destination.
   For ex: LOAD X, STORE Y
2. **ALU operation –**
   In this type of operation, arithmetic operations are performed on the data.
   For ex: MULT X

General Register Organisations :

When we are using multiple general-purpose registers, instead of a single accumulator register, in the CPU Organization then this type of organization is known as General register-based CPU Organization. In this type of organization, the computer uses two or three address fields in their instruction format. Each address field may specify a general register or a memory word. If many CPU registers are available for heavily used variables and intermediate results, we can avoid memory references much of the time, thus vastly increasing program execution speed, and reducing program size.

The format of instruction is:

Mode	Opcode	destination of operand	source operand	source operand

For example:

MULT R1, R2, R3

This is an instruction of an arithmetic multiplication written in assembly language. It uses three address fields R1, R2, and R3. The meaning of this instruction is:

R1 <-- R2 * R3

This instruction also can be written using only two address fields as:

MULT R1, R2

In this instruction, the destination register is the same as one of the source registers. This means the operation

R1 <-- R1 * R2

The use of large number of registers results in short program with limited instructions.

Some examples of General register based CPU Organization are IBM 360 and PDP- 11.

Stack Organisations :

The computers which use Stack-based CPU Organization are based on a data structure called **stack**. The stack is a list of data words. It uses **Last In First Out (LIFO)** access method which is the most popular access method in most of the CPU. A register is used to store the address of the topmost element of the stack which is known as **Stack pointer (SP)**. In this organisation, ALU operations are performed on stack data. It means both the operands are always required on the stack. After manipulation, the result is placed in the stack.

The main two operations that are performed on the operators of the stack are **Push** and **Pop**. These two operations are performed from one end only. (there Full and Empty two flags are used)

1.Push –This operation results in inserting one operand at the top of the stack and it increases the stack pointer register. The format of the PUSH instruction is "PUSH" .It inserts the data word at specified address to the top of the stack. It can be implemented as :

SP ← SP+1

M[SP] ← DR

if (SP=0) then (Full←1)

Empty ← 0

2.Pop – This operation results in deleting one operand from the top of the stack and it decrease the stack pointer register. The format of the POP instruction is "POP". It deletes the data word at the top of the stack to the specified address. It can be implemented as:

DR ← M[SP]

SP = SP – 1

if (SP=0) then (Empty ← 1)

Full← 0

There are usually two types of stack organisations : 1. Register Stack Organisation and 2. Memory Stack Organisation

OPERATION OF CPU

FETCH

The first step, fetch involves retrieving an instruction from program memory.

The instruction's location in program memory is determined by a Program Counter(PC), which stores a number that identifies the address of the next instruction to be fetched.

After an instruction is fetched, the PC is incremented by length of the instruction so that it will contain the address of the next instruction in the sequence.

DECODER

The instruction that the CPU fetches from memory determines what the CPU will do. In the decode step, performed by the circuitry know as **instruction decoder.**

The way in which the instruction is interpreted is defined by the CPU's instruction set architecture(ISA).

The operands may be specified as a constant value(called an immediate value), or as the location of value that may be a processor register or a memory address, as determined by some addressing mode. In some cases, the memory that stores the microprogram is rewritable, making it possible to change the way in which the CPU decodes instructions.

EXECUTE

After the fetch and decode steps, the execute step is performed. This may consist of a single action or sequence of actions. During each actions, various parts of the CPU are electrically connected so they can perform all or part of the desired operations and then the action is completed, typically in response to a clock pulse.

For example, if an addition instruction is to be executed, the arithmetic logic unit (ALU) inputs are connected to a pair of operand sources (numbers to be summed), the ALU is configured to perform an addition operation so that the sum of its operand inputs will appear at its output, and the ALU output is connected to storage (e.g., a register or memory) that will receive the sum. When the clock pulse occurs, the sum will be transferred to storage and, if the resulting sum is too large (i.e., it is larger than the ALU's output word size), an arithmetic overflow flag will be set.

IMPLEMENTATION

- Hardwired into CPUs circuitry is a set of basic operations it can perform, called an instruction set.
- The operations involved, adding or subtracting two numbers, comparing two numbers or jumping to a different part of a program.
- Each basic operation represented by particular combination of bits, known as the machine language opcode
- While executing instructions in a machine language program, the CPU decides which operation to perform by decoding the opcode.
- A complete machine language instruction consists of an opcode and, in many cases, additional bits that specify arguments for the operation.
- The actual mathematical operation for each instruction is performed by combinational logic circuit within the CPUs processor know **Arithmetic Logic Unit or ALU.**
- In general, a CPU executes an instruction by fetching it from memory, using is its ALU to perform an operation, and then storing the result to memory.

MEMORY MANAGEMENT UNIT

Memory is the location where data and program are stored which being processed by CPU.The *memory management unit* (MMU) manages the data flow between the main memory (RAM) and the CPU. It also provides memory protection required in multitasking environments and conversion between virtual memory addresses and physical addresses.

RAM

- RAM stands for Random access memory.
- It is not truly a part of the CPU.
- It is the main memory.
- Its function is to store programs and data so that they are ready for use when the CPU needs them.
- RAM is volatile and size is small and erased as soon as the power supply is cut off.

ROM

- It stands for Read only memory
- ROM is not volatile, so not erased by the cut of power supply, Example: HDD, SSD, compact disk, floppy disk.
- It must not be idle as it reduces the efficiency.
- Continuous data is processed.
- It is considered as the secondary memory which is used to store data.
- Data is stored permanently.
- Fetched data from the primary memory.
- Contains majority of data.

MEMORY MANAGEMENT UNIT

CACHE

Modern CPUs have one or more layers of cache. It is memory component that stores data so that future requests for the data can be served faster; the data stored in cache might be the results of an earlier computation or maybe a copy of data stored elsewhere

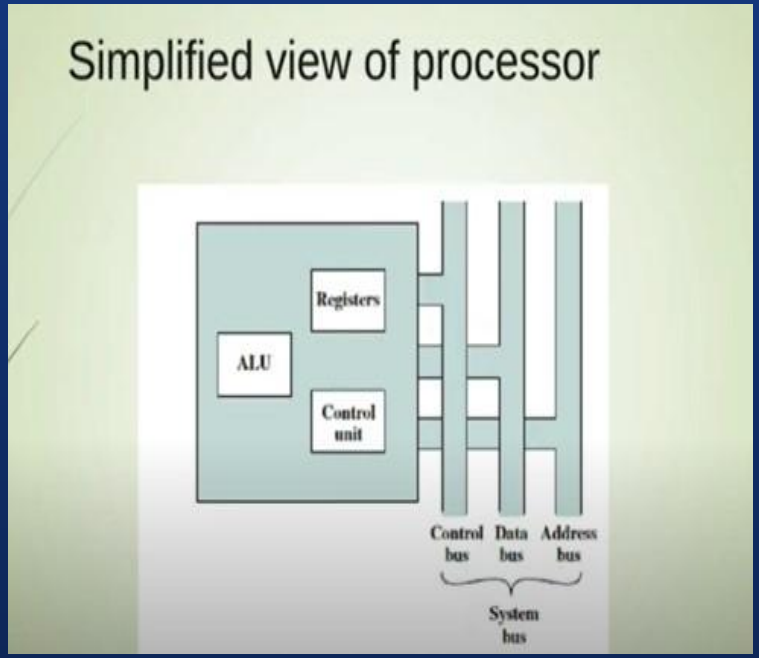
- Cache memory is faster than the system RAM, and it is closer to the CPU because it is on the processor chip.
- The cache provides data storage and instructions to prevent the CPU from waiting for data to be retrieved from RAM.
- The cache determines whether the data is already in residence and provides it to the CPU.
- Level 1 cache is closest to the CPU.
- These cache sizes typically range from 1MB to 32MB, depending upon the speed and intended use of the processor.

INSTRUCTION REGISTER AND POINTER

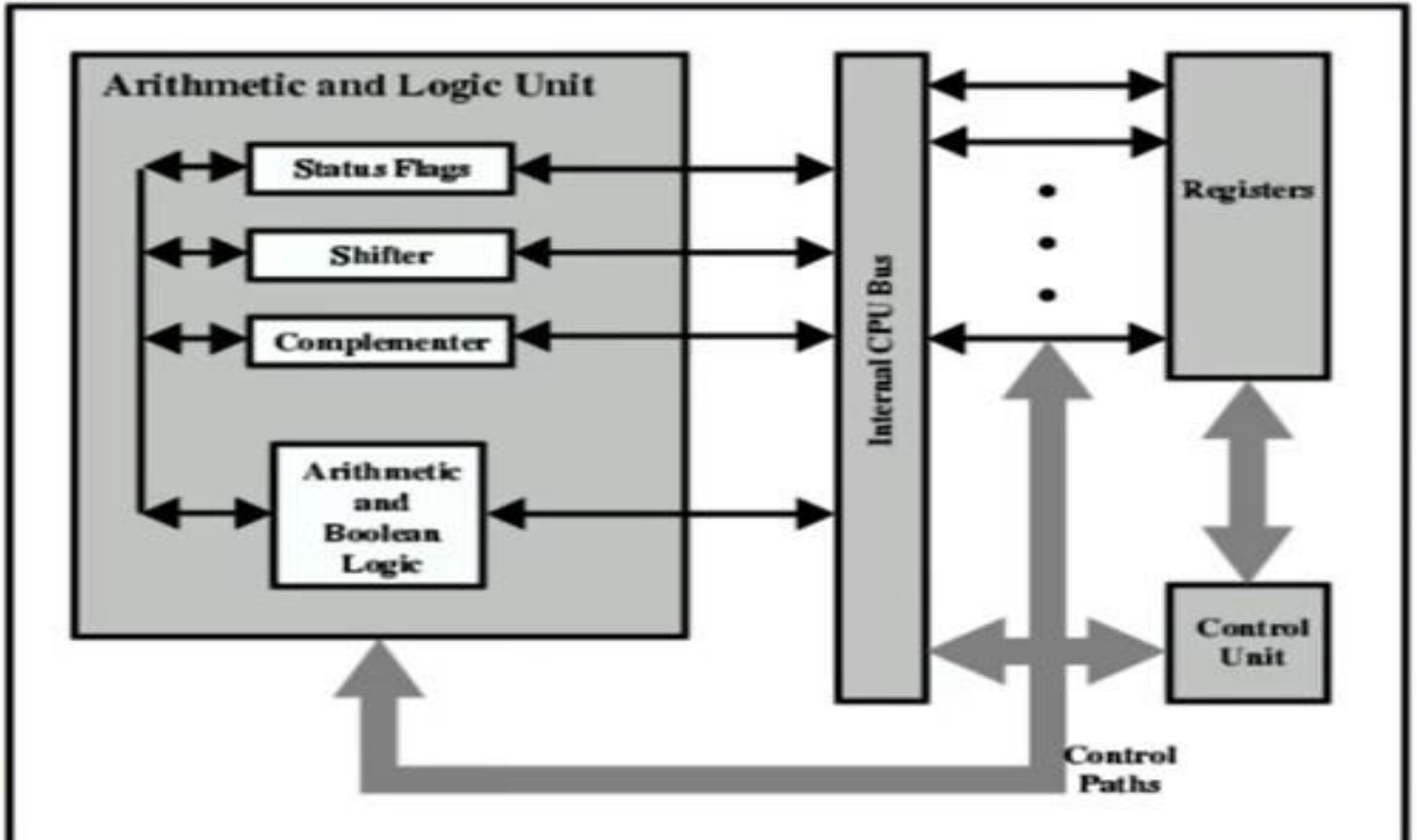
- The instruction pointer specifies the location in memory containing the next instruction to be executed by the CPU.
- When the CPU completes the execution of the current instruction, the next instruction is loaded into the instruction register from the memory location pointed to by the instruction pointer.
- After the instruction is loaded into the instruction register, the instruction register pointer is incremented by one instruction address. Incrementing allows it to be ready to move the next instruction into the instruction register.

PROCESSOR ORGANIZATION

The ALU does the actual computation or processing data. The control unit controls the movement of data and instructions in and out of the processor and controls the operation of the ALU. A minimal internal memory, consisting of a set of storage locations, called registers.



The data transfer and logic control paths are indicated, including an element labeled internal processor bus. This element is needed to transfer data between the various registers and the ALU because the ALU in fact operates only on data in the internal processor memory.


Arithmetic and Logic Unit
Status Flags
Shifter
Complementer
Arithmetic and Boolean Logic
Internal CPU Bus
Registers
Control Unit
Control Paths

Requirements placed on processor:

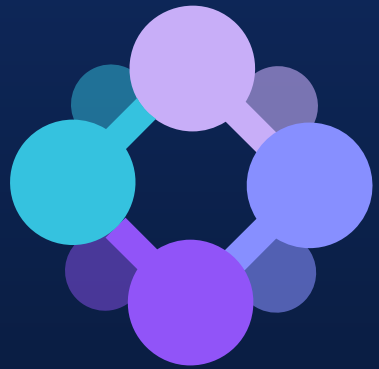
- **Fetch instruction:** The processor reads an instruction from memory

- **Interpret instruction:** The instruction is decoded to determine what action is required. Decoder circuit is used.

- **Fetch Data:** The execution of an instruction may require reading data from memory or an IO module.

- **Process Data:** The execution of an instruction may require performing some arithmetic or logical operation on data.

- **Write Data:** The results of an execution may require writing data to memory on IO module.



Fugaku

The A64FX was developed as a processor for the supercomputer Fugaku . For the semiconductor , the 7nm CMOS processor technology of TSMC[1] has been reached . For higher density , the TOFU interconnect D and the PCI express controllers have been implemented in the cpu chip and the high bandwidth 3D stack memory is integrated in the package . The A64FX employes the arm architecture to improve the software development environment while inheriting fujitsu’s proven high performance microarchitecture . Fugaku feature 158976 processor (432 racks) which has high performance microarchitecture to achieve high density packaging and lower power consumption desire

HARDWARE COMPONENT OF FUGAKU

Fujitsu A64FX

The A64FX is a 64-bit ARM architecture microprocessor design by fujitsu. The processor is replacing the SPARC64 V as fujitsu's processor for supercomputer application. It powers the fugaku supercomputer.the fastest supercomputer in the world . A64FX is the world's first processor to implement scalable vector extension (sve) which is a extension of the arm 8.2 -A instruction set . it has 4 NUMA nodes , with each with each NUMA node having 12 computer core, for a total of 48 crores processors each NUMA nodes also has its own level 2 cache, HBM2 memory and assistant cores for non-computational purpose . it has a theoretical peak performance of 3.3792 teraflops in double decision floating point calculation . It can perform both single and double precision floating point calculation , as well as 8 bit and 16 bit calculation with 512 bit wide SIMD and other cutting edge technology . A64FX has latest 7 nm process , 2.5 D packaging technology and microarchitecture which produces optimal power consumption from applications . It also has large scale parallel processing system , has approximately 128400 error check circuits , allowing it to offer mainframe class RAS .

ARM version 8.2A

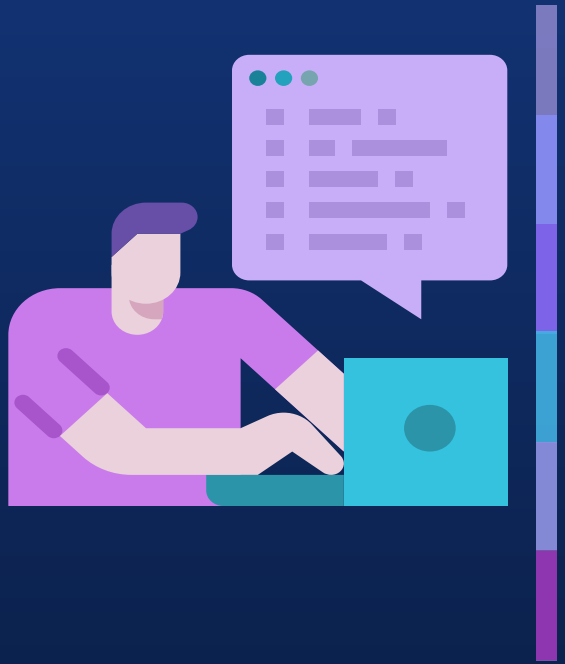
This CPU is based on ARM version 8.2A PROCESSOR Architecture.

- It's enhancement fell into four categories
    1. Optional half precision floating-point data processing(half precision was already supported, but not for processing, just as a storage format)
    2. (In computing, half precision is a binary floating-point computer number format that occupies 16 bits in computer memory)
    3. Memory model enhancement
    4. introduction of reliability, Availability and serviceability Extension (RAS Extension)
    5. introduction of statistical profiling.

Scalable Vector Extension (SVE)

- The Scalable Vector Extension (SVE) is "an optional extension to the ARMv8.2-A architecture and newer" developed specifically for vectorization of high-performance computing scientific workloads. The specification allows for variable vector lengths to be implemented from 128 to 2048 bits. The extension is complementary to, and does not replace, the NEON extensions.
- A 512-bit SVE variant has already been implemented on the Fugaku supercomputer using the Fujitsu A64FX ARM processor. It aims to be the world's highest-performing supercomputer with "the goal of beginning full operations around 2021
- SVE is supported by the GCC compiler, with GCC 8 supporting automatic vectorization and GCC 10 supporting C intrinsics. As of July 2020, LLVM and clang support C and IR intrinsics. ARM's own fork of LLVM supports auto-vectorization

CONCLUSION:



So, at the very end we want to conclude, Central processing unit (CPU) is a very important component in a computer because it process instructions of a computer program by performing the simple arithmetical, logical, and input/output (I/O) operations of the system. That is why CPU also known as the brain of the computer. The CPU has rich in history since the year 1945 before the CPU term had been use and the design and implementation of the CPU had improved tremendously over the years, thus, becoming more powerful and efficient. CPU had been used in various type of computers, from personal computer to supercomputer.

THANK YOU

WE THANK YOU FOR LISTENING

OUR TEAM

Zishnendu Sarker

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