Zsolt István

CONTACT
INFORMATION

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RESEARCH
PROFILE

My research interests lie in the intersection of distributed systems, databases and specialized hardware. I explore and combine ideas from these areas in order to overcome the compute/data gap that modern data centers face.

EDUCATION

Ph.D., Computer Science 2013 – 2018
    Systems Group, ETH Zürich, Switzerland
    Advisor: Prof. Gustavo Alonso

M.Sc., Computer Science (Distributed Systems) 2011 – 2013
    ETH Zürich, Switzerland

B.Sc., Computer Science 2007 – 2011
    UTCN Cluj-Napoca, Romania

PROFESSIONAL
EXPERIENCE

IMDEA Software Institute, Madrid, ES   September 2018 – Present
Assistant Research Professor
Working in the area of distributed systems and hardware acceleration for data processing.

IBM Research, Rüschlikon, CH   May 2018 – July 2018
Visiting Researcher
Topic: Exploring software and hardware acceleration opportunities for Blockchains.

Microsoft Research, Redmond, WA   June 2014 – August 2014
Research Intern
Supervisor: Ken Eguro
Topic: Adding support for B-tree indexes and a local cache to the FPGA in Cipherbase.

Xilinx Labs, Dublin, Ireland   September 2012 – March 2013
Research Intern (Master Thesis)
Supervisor: Michaela Blott
Topic: Design of a hash table for an FPGA-based key-value store optimized for caching scenarios. Helped in overall prototype implementation.

INRIA, Sophia-Antipolis, France   July 2011 – August 2011
Research Intern (OASIS Group)
Supervisors: Ludovic Henrio and Fabrice Huet
Topic: Annotation-based automatic parallelization of Active Objects in ProActive.

INRIA, Sophia-Antipolis, France   June 2010 – August 2010
Research Intern (OASIS Group)
Supervisor: Denis Caromel
Topic: Parallel programming and scheduling for multicores in the ProActive Framework

MaxIQ Computer, Oradea, Romania   2008 – 2009
Junior Software Engineer
Role: Backend (Java EE) and frontend (HTML, Javascript) developer.

CONFERENCE
PUBLICATIONS

A Flexible K-Means Operator for Hybrid Databases
Z. He, D. Sidler, Z. István, G. Alonso. *International Conference on Field Programmable Logic and Applications (FPL), 2018.*

Providing Multi-tenant Services with FPGAs: Case Study on a Key-Value Store. Z. István, G. Alonso, A. Singla. *International Conference on Field Programmable Logic and Applications (FPL), 2018.*

Accelerating Pattern Matching Queries in Hybrid CPU-FPGA Architectures.
D. Sidler, Z. István, M. Ewaida, G. Alonso. *ACM SIGMOD/PODS Conference (SIGMOD'17), 2017.*

Low-Latency TCP/IP Stack for Data Center Applications.
D. Sidler, Z. István, G. Alonso. *26th Int'l Conference on Field Programmable Logic and Applications (FPL'16), 2016.*

Runtime Parameterizable Regular Expression Operators for Databases.
Z. István, D. Sidler, G. Alonso. *24th IEEE Int'l Symposium on Field-Programmable Custom Computing Machines (FCCM'16), 2016*

Consensus in a Box: Inexpensive Coordination in Hardware
Z. István, D. Sidler, G. Alonso, M. Vukolic. *13th USENIX Symposium on Networked Systems Design and Implementation (NSDI '16), 2016.*

Histograms as a Side Effect of Data Movement for Big Data.
Z. István, L. Woods, G. Alonso. *ACM SIGMOD/PODS Conference (SIGMOD'14), 2014.*

A Flexible Hash Table Design For 10Gbps Key-value Stores on FPGAs.
Z. István, G. Alonso, M. Blott, K. Vissers. *23rd Int'l Conference on Field Programmable Logic and Applications (FPL'13), 2013.*

Achieving 10Gbps Line-rate Key-value Stores with FPGAs.
M. Blott, K. Karras, L. Liu, K. Vissers, Z. István, J. Bar. *5th USENIX Workshop on Hot Topics in Cloud Computing (HotCloud'13), 2013.*

Multi-threaded Active Objects. L. Henrio, F. Huet, Z. István. *15th Int'l Conference on Coordination models and Languages (COORDINATION), 2013.*

Adapting Active Objects to Multicore Architectures.
L. Henrio, F. Huet, Z. István, G. Sebestyen. *Int'l Symposium on Parallel and Distributed Computing (ISPDC 2011), 2011.*

JOURNAL
PUBLICATIONS

Active Pages 20 Years Later: Active Storage for the Cloud.
Z. István, D. Sidler, G. Alonso. *To appear in IEEE Internet Computing July/Aug 2018.*

Caribou: Intelligent Distributed Storage.
Z. István, D. Sidler, G. Alonso. *Proceedings of VLDB Endowment, Volume 10, No. 11 (VLDB'17), 2017.*

A Hash Table for Line Rate Data Processing.
Z. István, G. Alonso, M. Blott, K. Vissers. *ACM Transactions on Reconfigurable Technology and Systems (TRETS), March 2015.*

Ibex – An Intelligent Storage Engine with Support for Advanced SQL Off-loading.
L. Woods, Z. István, G. Alonso. *Proceedings of VLDB Endowment, Volume 7, No. 11 (VLDB'14), 2014.*

PATENTS

Systems and Methods for Providing Distributed Tree Traversal Using Hardware-Based Processing. K. Eguro, Z. István, A. Arasu, R. Ramamurthy, K. Shriraghav.
US 20160147779 A1, Patent application filed 11/26/2014

POSTERS AND DEMOS	**Enzian: a Research Computer for Datacenter and Rackscale Computing.** D. Cock, R. Achermann, M. Owaida, Z. Istvan, T. Grosser, Z. Wang, G. Alonso, T. Roscoe, D. Sidler, A. Turowski. *Poster at EuroSys'18.*
	Caribou: A Platform for Building Smart Storage Z. István, D. Sidler, G. Alonso. *Poster at EuroSys'17.*
	doppioDB: A Hardware Accelerated Database D. Sidler, M. Ewaida, Z. István, K. Kara, G. Alonso. *Demo for SIGMOD'17 and FPL'17.*
	Specialized Microservers for the Data Center Z. István, D. Sidler, G. Alonso. *Demo for FPL'15. Poster at EuroSys'15.*
	Hybrid FPGA-accelerated SQL Query Processing L. Woods, Z. István, G. Alonso. *Demo for FPL'13.*

TEACHING EXPERIENCE

Teaching Assistant at **ETH Zürich**

Advanced Systems Lab	Fall 2013, Fall 2014, Fall 2015, Fall 2016, Fall 2017
Data Modeling and Databases	Spring 2016, Spring 2017
Programmieren und Problemlösen	Spring 2014, Spring 2015

Student Supervision at **ETH Zürich**

Semester Project: Zhenhao He (co-advised with David Sidler) Title: A Flexible K-Means Operator for Hybrid Databases	Spring 2018
Bachelor Thesis: Mickey Vanska (co-advised with David Cock) Title: Program Trace Analysis on an FPGA	Spring 2017
Bachelor Thesis: Tim Taubner Title: Accelerating Statistical Methods using an FPGA	Spring 2015
Semester Project: Jakub Szymanek Title: Indexes and Caching in IBEX	Spring 2014

COMMUNITY SERVICE

Reviewer for IEEE Transactions on Knowledge and Data Engineering (TKDE) (09.2017), IEEE International Symposium on Circuits and Systems (ISCAS'18) (external), ACM Journal of Architecture and Code Optimization (TACO) (06.2017).

Shadow PC member for ASPLOS'18, EuroSys'18, EuroSys'17.

SCHOLARSHIPS AND AWARDS

ETH Zürich Excellence Scholarship 2011-2013: Full scholarship for M.Sc. studies

"Grigore Moisil" National Programming Competition (3rd Place), Romania, 2007

Debate – South-East European Youth Leadership Institute (SEEYLI) 2005: Finalist in Romania; Attendee of summer school at Wake Forest University, NC

SELECTED INVITED TALKS

Caribou – Intelligent Distributed Storage.
IMDEA Software Institute, Madrid, Spain. February 2018
KAUST, Thuwal, Saudi Arabia. October 2017

Packing a Punch: Building Intelligent Distributed Storage with Hardware.
TU Dresden, Germany. July 2017

Caribou: Intelligent Storage for the Datacenter.
Swiss Joint Research Center Workshop, MSR, Cambridge, UK. February 2017

Consensus in a Box: Inexpensive Coordination in Hardware.
IBM Research Rüschlikon, CH. October 2016

Accelerating String Matching Queries with Hybrid CPU-FPGA Multicores.
Oracle Labs, Belmont, CA. March 2016

Consensus in a box: can we build distributed systems with FPGAs?
Xilinx Labs, San Jose, CA. March 2016
IBM Research Almaden, San Jose, CA. March 2016

Time to Specialize! A Microserver for Key-value Stores.
University of Washington, Seattle, WA. June 2015

Towards Better Energy Efficiency in Datacenters using FPGAs.
Microsoft Research, Redmond, WA. June 2015

Application-specific Micro-servers.
Oracle Labs Zürich Kickoff Workshop, Zürich, CH. January 2015

Languages   Hungarian, Romanian, English – Proficient
German – Intermediate