CSC258 lab4

Part1:

3. Test vector does not work, because this is sequential circuit.
4. Should change the clk to 1, otherwise value of D will not be sent to the output.

Part2:

2. a. The output will be used as new input and the HE display keep changing.

b. When clock goes high, the output will keep changing.

c. 2n bit

d. The most significant bit will be ignored, it will not change the shift register.

3. a.

status	B	A	S
pass	1111	0000	0000 1111
pass	1101	0010	0011 0100
pass	1111	1000	0000 1111
pass	1000	1111	0000 0000

b.

status	B	A	S
pass	1111	0000	0000 1111
pass	1111	0001	0000 0111
pass	1100	1000	0000 1100
pass	1100	0010	0000 0011

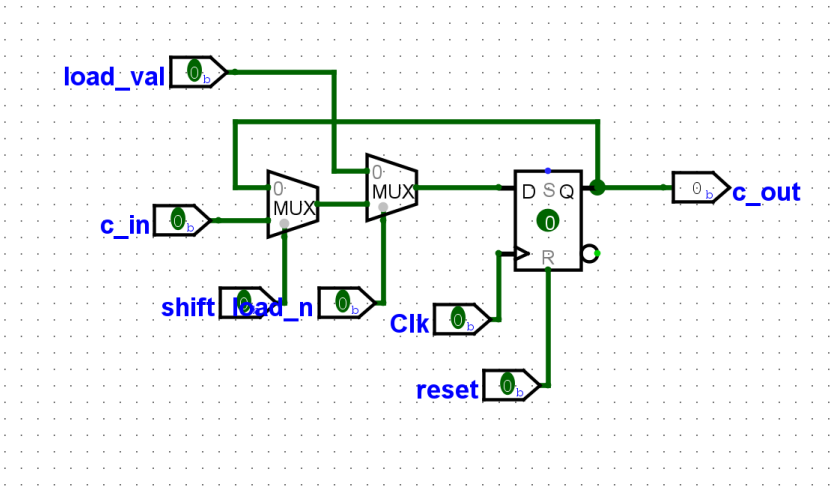
c.

status	A	B	S
pass	1101	0011	0000 0111
pass	1101	0001	0000 1101
pass	1101	0101	0000 0001

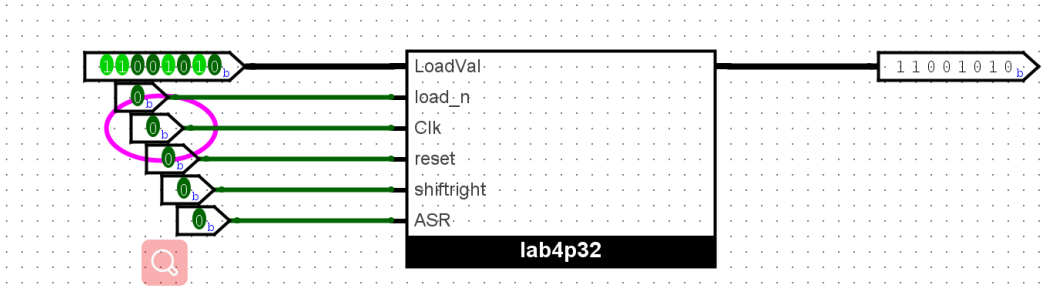
Part3

1. When load_n=0 and shift_right = 0, it will load the value.

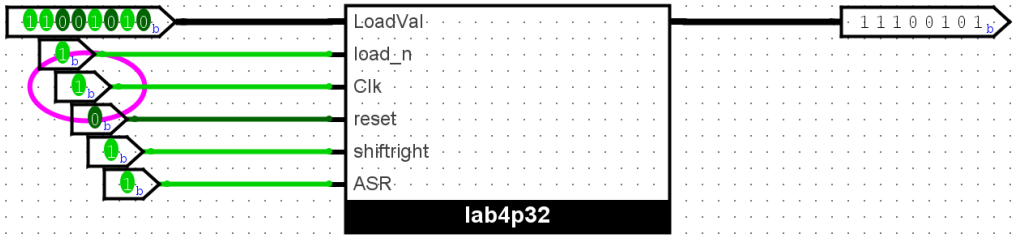
2.



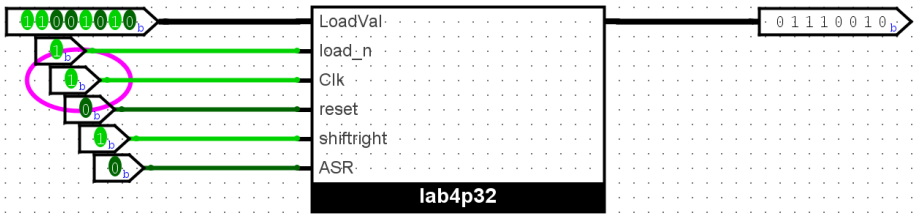
3. Load value:



Shift right = 1, ASR=1:



Shift right = 1, ASR = 0:



4. If we do not have reset, then we don't have output value in the D latch.