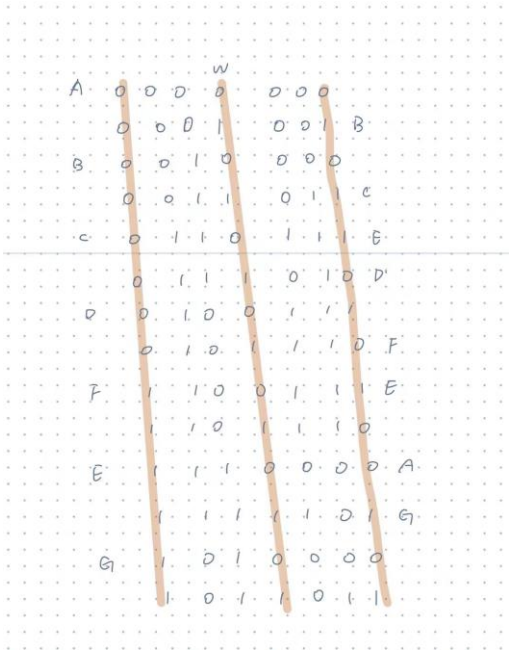
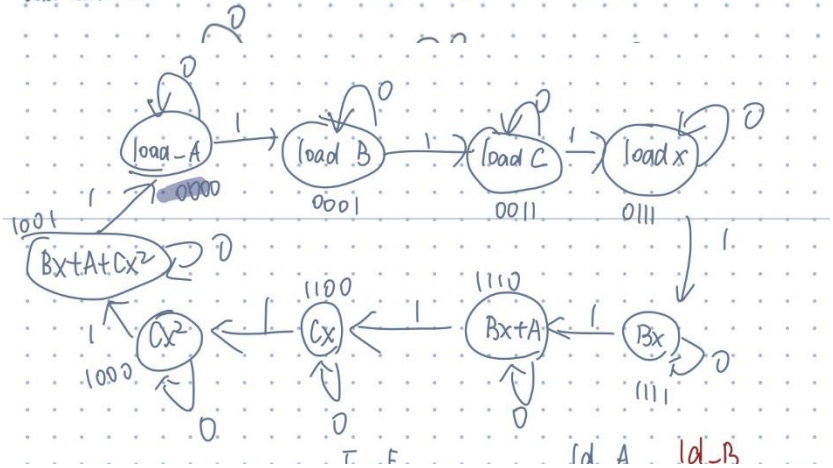
Part1

1. Reset signal is asynchronous.
   It is active high since the circuit is reset when the signal is 1.
   The reset signal should be … in the run.
2. 

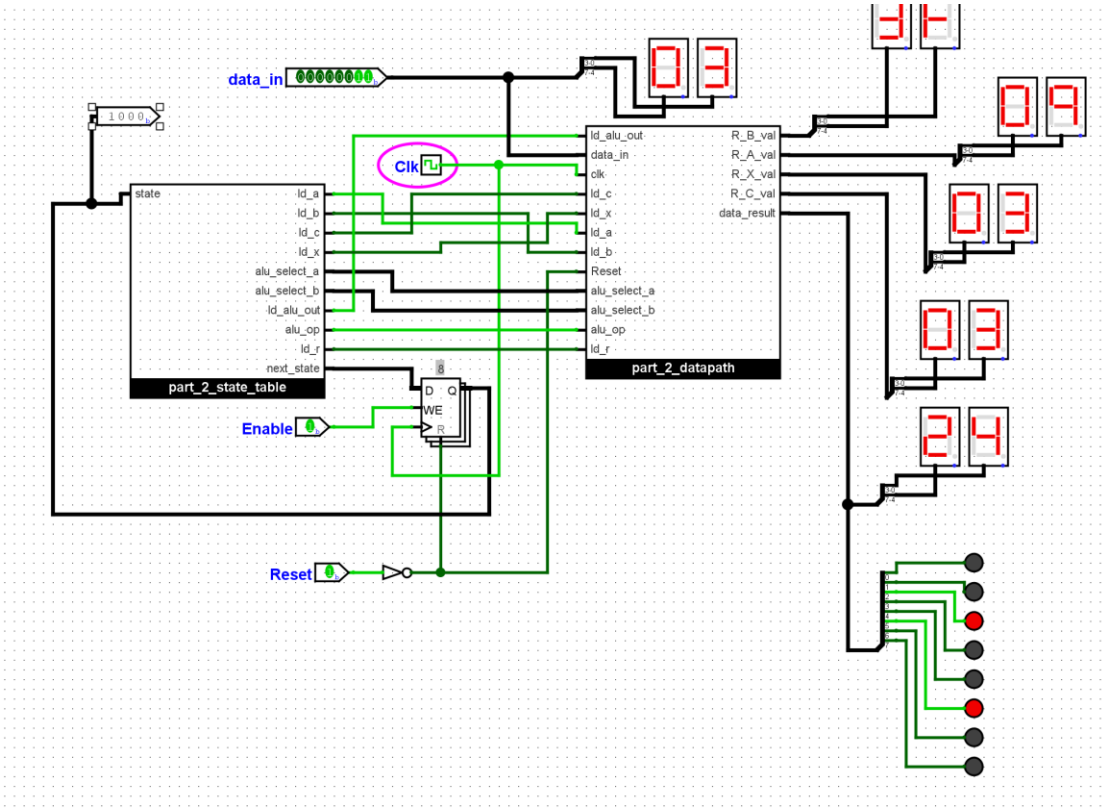
Part2

1.

	idc	idx	ida	idb	alusa	alusb	op	out	ldr	A	B
Mul Bx				1	01	11	1	1	0		
store in B											Bx
Add Bx+A				1	00	01	0	1	0		Bx+A
store in B											
Mul Cx			1		10	11	1	1	0	Cx	
store in A											
Mul Cx²			1		00	11	1	1	0	Cx²	
store in A											
add Bx+A+Cx²					00	01	0	0	1		

2. 

3.

4. 
data_in
1000
Clk
state
ld_a
ld_b
ld_c
ld_x
alu_select_a
alu_select_b
ld_alu_out
alu_op
ld_r
next_state
part_2_state_table
D
Q
WE
R
Enable
Reset
ld_alu_out
data_in
clk
ld_c
ld_x
ld_a
ld_b
Reset
alu_select_a
alu_select_b
alu_op
ld_r
part_2_datapath
R_B_val
R_A_val
R_X_val
R_C_val
data_result
0 3
0 9
0 3
0 3
2 4