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ELE 313

ELECTRONICS LABORATORY II

PROJECT REPORT

Two Input Schmitt TTL Nand Gate

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ABSTRACT

In this study, I generally evaluated my theoretically-based computations in both virtual and physical settings. My project is built around a unique TTL gate. Increased fan-out, improved transient responsiveness, and a need for less chip size are all features of TTL circuits. The 74XX series operates between 0 and 70 ^{o}C and is suitable for the majority of commercial applications. In particular, I tried to change the TTL gate to get the desired outcome. Totem-pole output architectures, level shifters, phase splitters, and basic emitter-coupled Schmitt triggers were some of the examples I utilized. In addition, I made an effort to get the laboratory experiences that an electronics engineer should have.

Introduction

First, let me explain the relationship between hysteresis and Schmitt triggers. For output high-to-low and low-to-high transitions, a type of logic circuit is typically defined that has a different voltage transfer characteristic. In contrast to the logic circuits previously discussed, the output low-to-high and high-to-low transitions take place at various input voltages. We call this hysteresis. Gates with inputs like those in figure 3 are frequently employed to eliminate these issues, especially at the input to a system where noise may be anticipated as signals arrive from an external source. This is among the circuit's most crucial goals.

As can be seen, the addition of an active pull-up sub-circuit is the primary enhancement of TTL design over DTL. As a result, the corresponding output capacitance charges more quickly, improving circuit performance.

By adding an ANDing diode section at the input and an emitter-follower level shifter section with Q_3 and D_4 followed by a typical inverting driver splitter connected to a totem-pole output section at the output, as shown in figure 1 below, we can convert the basic emitter-coupled Schmitt Trigger noninverter in figure 3 into a TTL compatible Schmitt Trigger NAND gate.

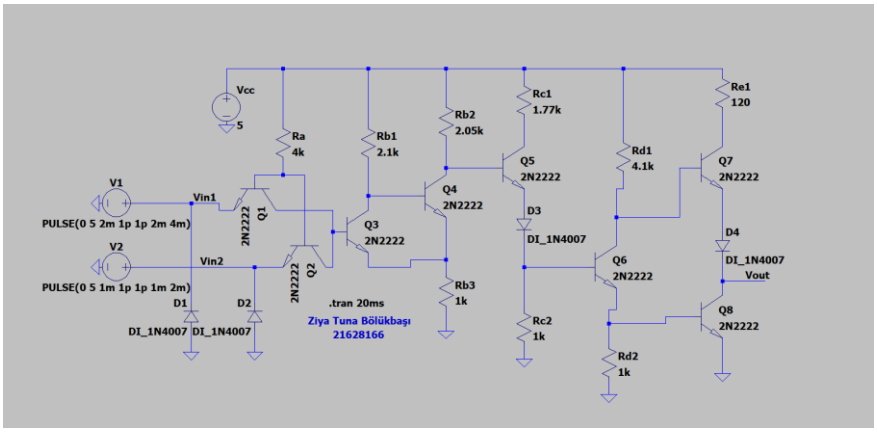

Figure 1: Generalized Schmitt TTL NAND Gate

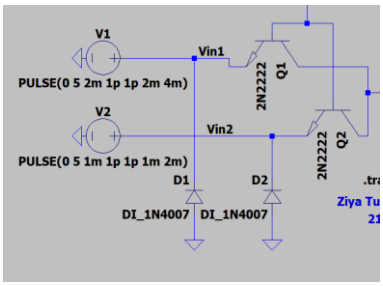

Figure 2:Input Stage

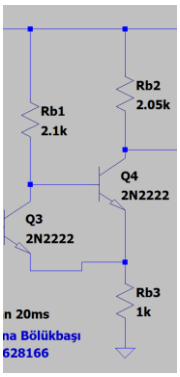

Figure 3: Schmitt Trigger

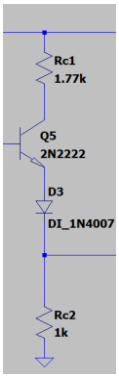

Figure 4:Level Shifter

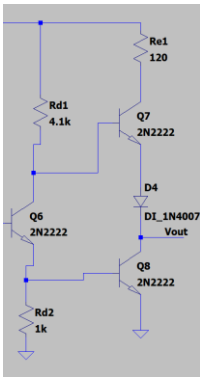

Figure 5:Output Stage

A totem pole output is created by stacking two BJTs, a resistor, and a diode in the output branch. Active pull-up is provided by the inclusion of R8 and Q5 (in figure 1) to the output high driver section of the circuit. This means that when the output shifts from low to high, there is a lot of current available to charge the comparable load capacitance. It is simple to see how the rise time has improved.

Purpose of some element for Generalized Schmitt TTL NAND Gate:

Q_1-Q_2 => Base-emitter input BJT, base-collector level shifting of transtion width, pull-down of Q_6

R_A => Limits I_{IL}

Q_6 => Drive splitter, provides base driving current to Q_8, base-emitter level shifting for shift of transition width, pull-down of Q_7

R_C => Along with Q_6 provides logic inversion to output-high driver

Q_8 => Output inverting BJT, output low driver for current sourcing pull-down

D_5 => Diode level shifting shifting between V_{cc} and output

R_{D2} => Provides discharge path for saturation stored charge of Q_8

Q_7 => Provides active current-sourcing pull-up

R_{e1} => Part of active pull-up and limits current spikes during output high-to-low transitions

Materials:

- 2N2222 (8)
- 1N4007 (4)
- Resistor (9)
- DC Voltage Source (1)

I used arduino because i need dc voltage source

Part 1 – Theoretical Calculations

I use 8 transistors in my circuit design.I found fan-out value is 40

2N2222 transistor parameters :

$V_{BE(SAT)} = 0.75V \quad V_{CE(SAT)} = 0.15V \quad \beta = 35 \quad \sigma = 0.9$

1N4007 diode parameters :

$V_{D(ON)} = 0.7V$

I assume $N = 40 \Rightarrow \left[\frac{I_{OL}}{I_{IL}}\right]$ and $I_{OL} = 40mA, I_{IL} = 1mA$

$$I_{IL} = \frac{Vcc - V_{BE(SAT),Q1} - V_{CE(SAT),Q8}}{R_A} = \frac{5V - 0.75V - 0.15V}{R_A} = 1mA, \quad R_A = 4.1k\Omega$$

$$I_{OL} = \sigma * \beta * I_{B,Q2} \Longrightarrow 40mA = 0.9 * 35 * I_{B,Q2} \Longrightarrow I_{B,Q2} = 1.27mA$$

I assume R_{D2} is equal to 1kΩ

$$I_{R_{D2}} = \frac{V_{BE(SAT),Q8}}{R_{D2}} = \frac{0.75V}{1k\Omega} = 0.75mA$$

$$I_{E,Q6} = I_{R_{D2}} + I_{B,Q8} = 0.75mA + 1.27mA = 2.02mA$$

I assume $I_{B,Q6} = 1mA \rightarrow \quad R_{D1} = \frac{V_{cc} - V_{BE(SAT),Q1} - V_{CE(SAT),Q6}}{I_{D_1}} = \frac{5V - 0.75V - 0.15V}{1.02mA} = 4.1k\Omega$

$$I_{D_1} = I_{E,Q6} - I_{B,Q6} = 1.02mA$$

I assume $R_{C2=}1\text{k}\Omega \rightarrow \quad V_{B,Q6} = V_{BE(SAT),Q8} + V_{BE(SAT),Q6} \Rightarrow 0.75V + 0.75V = 1.5V$

$$I_{R_{C2}} = \frac{V_{B,Q6}}{R_{C2}} \Longrightarrow \frac{1.5V}{1k\Omega} = 1.5mA$$

$$I_{E,Q5} = I_{B,Q6} + I_{R_{C2}} \Rightarrow 1mA + 1.5mA = 2.5mA$$

I assume $I_{B,Q5} = 1mA \rightarrow \quad R_{C1} = \frac{V_{cc} - V_{CE(SAT),Q5} - V_{D(ON)} - V_{BE(SAT),Q6} - V_{BE(SAT),Q8}}{I_{C_1}}$

$$I_{C_1} = I_{E,Q5} - I_{B,Q5} = 2.5mA - 1mA = 1.5mA$$

$$R_{C1} = \frac{5V - 0.15V - 0.7V - 0.75V - 0.75V}{1.5mA} = 1.77k\Omega$$

$$R_{B2} = \frac{V_{cc} - V_{BE(SAT),Q5} - V_{D(ON)} - V_{BE(SAT),Q6} - V_{BE(SAT),Q8}}{I_{B_2}} = \frac{5V - 0.75V - 0.75V - 0.75V - 0.7V}{1mA}$$
$$= 2.05k\Omega$$

$R_{B1} > R_{B2}$ So I assume $R_{B1} = 2.1k$

Part 2 – Circuit Design and Simulation Results

A) Ltspice simulation and results

For input A=0 and B=0:

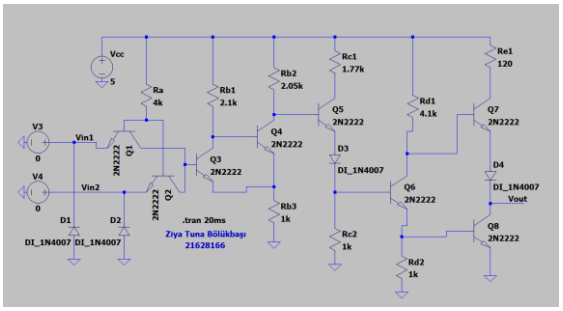

Figure 6: TTL nand gate for specific input A=0 B=0

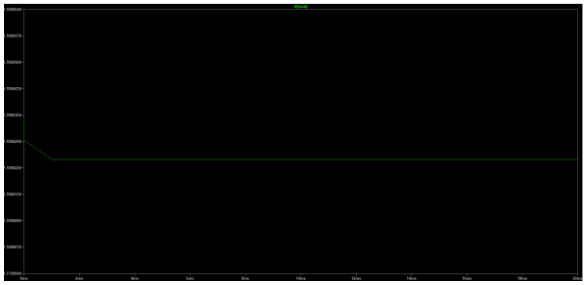

Figure 7: Output graph for specific input A=0 B=0

$\overline{A.B}$ is equal V_{out} and $\overline{0.0}$= 1 so,

V_{out} must be equal to high(High means 1 or 2.78V for this circuit)

For input A=0 and B=1:

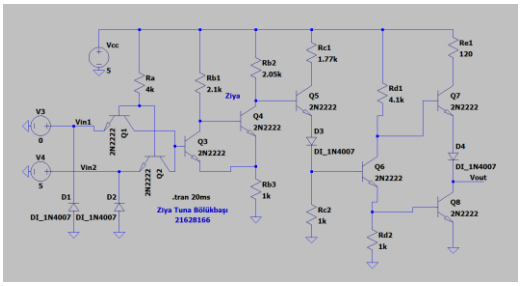

Figure 8: TTL nand gate for specific input A=0 B=1

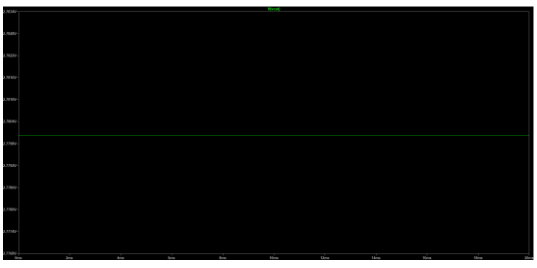

Figure 9: Output graph for specific input A=0 B=1

$\overline{A.B}$ is equal V_{out} and $\overline{0.1}$= 1 so,

V_{out} must be equal to high(High means 1 or 2.78V for this circuit)

For input A=1 and B=0:

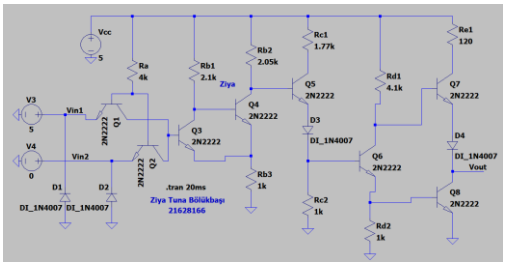

Figure 10: TTL nand gate for A=1 B=0

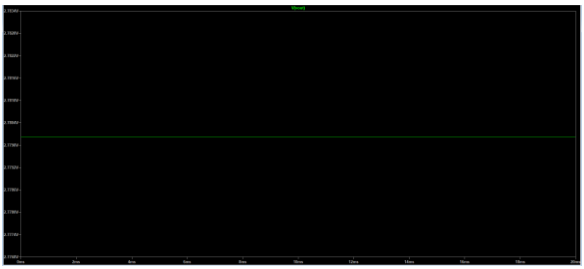

Figure 11: Output graph for specific input A=1 B=0

$\overline{A.B}$ is equal V_{out} and $\overline{1.0}$= 1 so,

V_{out} must be equal to high(High means 1 or 2.78V for this circuit)

For input A=1 and B=1:

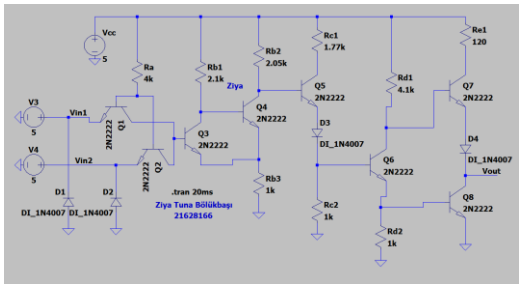

Figure 12: TTL nand gate for specific input A=1 B=1

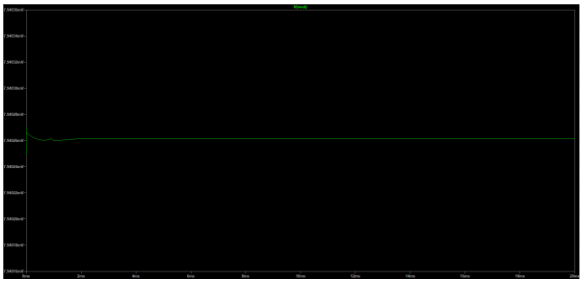

Figure 13: Output graph for specific input A=1 B=1

$\overline{A.B}$ is equal V_{out} and $\overline{1.1}$= 0 so,

V_{out} must be equal to low(Low means 0 or 7.94mV for this circuit)

B) Breadboard Circuit

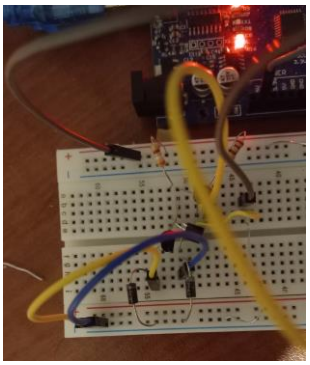

Figure 14:Input Stage

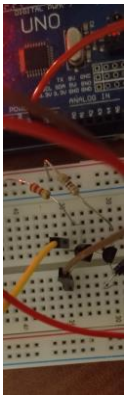

Figure 15: Added Schmitt Trigger

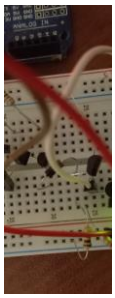

Figure 16: Added Level Shifter

Figure 17: Added Phase splitter and Totem pole

Part 3 - Design of the Circuit and Testing

Figure 18:Input Stage

Figure 19:Schmitt Trigger

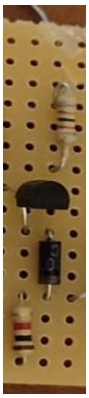

Figure 20: Level Shifter

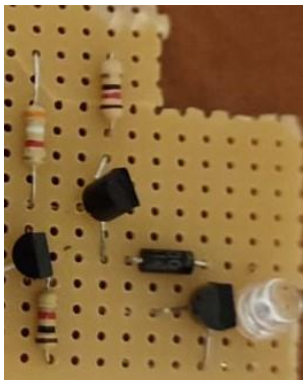

Figure 21: Phase splitter and Totem pole output

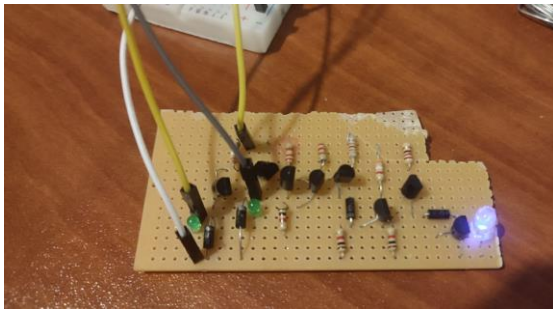

Figure 22:If input A and input B is equal to 0 output will be equal to 1

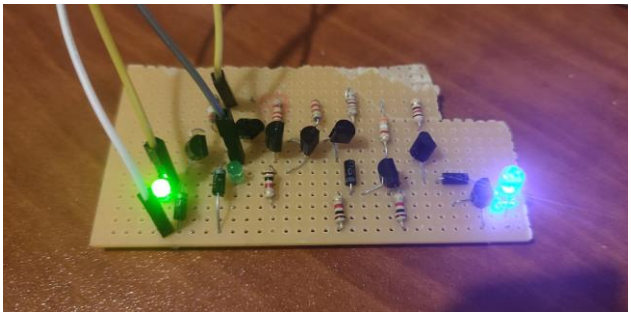

Figure 23:If input A is equal to 1 and input B is equal to 0 output will be equal to 1

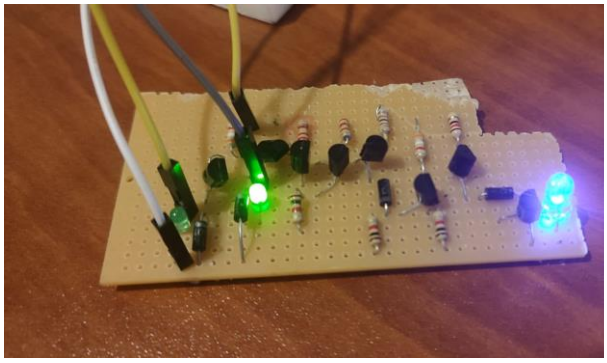

Figure 24:If input A is equal to 0 and input B is equal to 1 output will be equal to 1

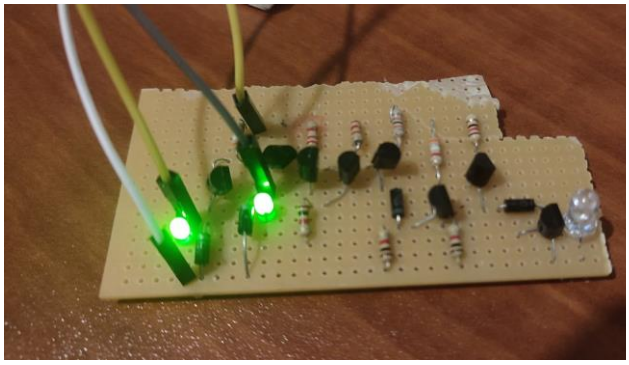

Figure 25:If input A is equal to 1 and input B is equal to 1 output will be equal to 0

Conclusion

In this design assignment, I simulate in a virtual and real environment and conduct a theoretical study of the Schmitt TTL NAND Gate. I went about the theoretical portion making assumptions and used component data sheets for some variables. I utilized a 2N2222 transistor and a 1N407 diode. I had to test my results because I made acceptance in the calculation parts. I verified the precision of my theoretical calculations and examined the circuit's operation in a virtual setting using the LTspice application. To adjust some of the circuit element values to the values I used in theoretical calculations, I changed the saturation levels of the elements in LtSpice to match the experiment results.
I put up the circuit on the breadboard to test it in the real world as in experiments after verifying my theoretical results in the simulation. Values at this point were marginally different. The figures came out somewhat differently at this point, but it had minimal impact on the outcome.

Through this project, I was able to learn about the fundamental characteristics of digital integrated circuits and how the nand gate is constructed. In addition, I made an effort to comprehend ideas like fan-out and schmitt trigger.

Project Assessment Survey

•What are the throublesome points of the project process?

- It was difficult to set up and run the circuit, but the most challenging part for me was the calculations.

•What was your method to solve your problems?

- I created a worksheet for myself. First, I researched what the circuit is and what it does. Then I made the theoretical calculations. I checked the results of these calculations more than once. Then I made the circuit design on the breadboard and pcb, and took notes for my report in the meantime.
Finally, I prepared the report.

•What are your gains from this Project?

- I practiced with digital IC for practice and discovered project difficulties. Of course, when beginning a project, I discovered that I had to first acquire the essential abilities in order to complete it.

•Do you think the project process is successful?

-I think my circuit is working properly and my report is also sufficient. So I think I have successfully completed this Project.So my vote 5 for this Project and report.

List of References

http://www.ee.hacettepe.edu.tr/~usezen/ele312/ttl_gates-4sp.pdf

“Digital Integrated Circuits”, DeMassa and Ciccone, John Wiley & Sons, 1996.

https://www.diodes.com/assets/Datasheets/ds28002.pdf

https://web.mit.edu/6.101/www/reference/2N2222A.pdf