Zi Zhang

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EDUCATION

University of Electronic Science and Technology of China (UESTC) **Chengdu, China**
Major: Electronic Science and Technology (Yingcai Honours Programme of UESTC) **09/2019-06/2023**
Degree: Bachelor of Engineering **GPA:** 3.95/4.00 | **Average Score:** 90.0/100 | **Rank**: 11/161
Major Courses:

Semiconductor Physics A 98/100
Electromagnetic Fields and Waves 91/100
Microelectronic Technology 88/100
EDA Technology B 99/100
Internet of Things Sensor Technology 95/100
Fundamentals of Solid-State Electronics II 88/100
Electronic Devices and Materials A 97/100
Fundamentals of Microelectronic Devices 93/100
Digital Design and MCU System (H) 93/100

RESEARCH EXPERIENCE

Sampling PLLs for Molecular Probing **02/2023-06/2023**

Director: Prof. Cheng Wang

- Behavioral modeling simulation of the sampling phase-locked loop system
- Design of digital-time converter (DTC), sampling phase detector (SPD), gm-cell, and MASH-1 DSM
- Systematic verification, including stability and noise analysis

On-Chip Integrated Molecular Saturation Spectroscopy **05/2021-present**

Director: Prof. Cheng Wang

- 231GHz subharmonic mixer with slot-line enhanced LO leakage rejection, 1 patent submitted
- High efficiency, broadband millimeter-wave multiplier chain
- Millimeter-wave power detector for temperature compensation
- 65nm CMOS process, taped-out in Feb. 2023 (Test completed)

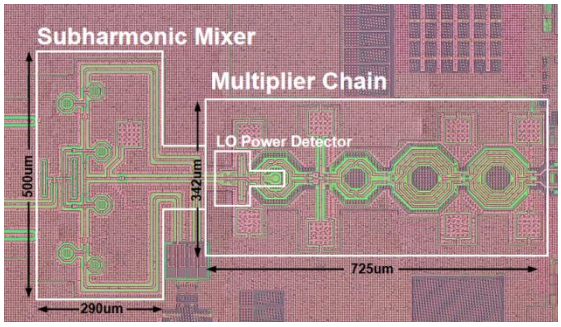

Fig. 1. CMOS RX w/ mixer and multiplier

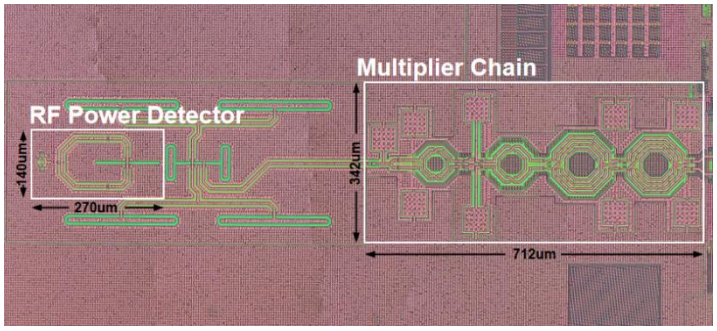

Fig. 2. CMOS TX w/ multiplier chain and power detector

Quantum Key Distribution System Based on BB84 Protocol **09/2020-12/2021**

Director: Prof. Qiang Zhou

- Generated qubit based on the principle of time-bin coding, which can resist disturbance in optical fiber link
- Accomplished qubit projection measurement and state tomography
- Obtained the bit error rate and bit yield rate of the quantum key distribution system
- Mainly responsible for the construction of hardware platform

Design of MCU and Sequencing Application **05/2021-07/2021**

Leading the Course Project (Final Grade: 100)

- Completed the MCU design based on MIPS instruction architecture, which supports add, sub, and, or, slt, lw,

sw, beq and addi instructions

- Completed the sorting of 16 random signed 32-bit binary numbers in a specified way by the design of assembly language, the invocation of machine code
- At the optimization level, the prefix adder is used in the MCU design process, and the dual-core parallel design scheme is realized when the sequencing instruction is executed, which has good performance in terms of speed and resource overhead

HONOURS & AWARDS

First Excellent Student Scholarship(Ranked First for the 2021/22 Academic Year) 12/2022
Outstanding Graduates at the School Level 11/2022
Model Student Scholarship 12/2021
Excellent Research Project in the 2021 UESTC Innovation and Entrepreneurship Training Programme for College Students 12/2021
Excellent Member of the Youth League 05/2021
Third Prize in the UESTC Simulation Contest at the 2021 Mathematical Contest in Modelling 12/2020
Third Prize for Most Creative Group in the 8th National College Students' Photoelectric Design Competition (Southwest Competition Zone) 08/2020
Second Prize in the Electronic Design Competition Freshmen Cup 12/2019

PERSONAL SKILLS & RESEARCH INTEREST

Design of CMOS Integrated Circuit

- Analog circuitry: Cadence for schematic simulation, layout (DRC, LVS), and post-layout extraction (PEX)
- RF Circuitry: ADS and HFSS for RFIC EM co-simulation
- Mixed-signal circuitry: Verilog & Verilog-A modeling for functional verification and co-simulation based on AMS

Other skills

- IC packaging: Altium Designer and Solidworks for chip packaging design
- Programming skills: C, Python and Matlab for chip test
- Instrument skills: 网络分析仪，功率计

Research Interest

- RF/mm-Wave communication and sensing circuits, photonics and quantum systems

Language Skills

- Mandarin Chinese (native), English (proficient)

Personal Website

https://zizhang02.github.io/