1. This lab, we provide designs of the register file, ALU, and the fetch unit for our CPU. We provide the appropriate inputs and outputs of each element, the operations supported by the ALU, and the responsibilities of the fetch unit.
2. Make a table?


6. We support eight ALU operations: and, add, sll, srl, sub, slt, absolute, and seq.
7. Our ALU will not be used for non-arithmetic instructions. Address calculation and branches are calculated in the fetch unit.

10. //The one with the most lines?