

V0.04 Preliminary

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REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Original	Kevin	SW	Dennis	2010/3/16
0.01	Add detail description for Page 0 Register (Command) Add detail description for Page 1 Register (Command) Add maximum series resistance section Add timing example section	Kevin	SW	Dennis	2010/3/25
0.02	1. Page 0 Command Modification 0xB1(bits CGM removed, N565, RGBBP update, Add TE_PWR_SEL) 0xB4(Add vivid color function) 0xB6(Add source data hold time) 0xB7(EQ function for GOA Ctrl signal) 0xB9(Source/VCOM Ctrl in non-display area) 0xBA(0xBB move to 0xBA, Source/VCOM/Gate Ctrl in V porch) 0xBB(0xBC move to 0xBB, Bias current) 0xBC(0xB8 move to 0xBC, inversion type) 0xC7(inversion driving type, update ZG[1:0]→ZZ_RL, ZZ_EO) 0xC8(Display timing update) 0xD0(Add bit CLED_VOL) 2. Page 1 Command Modification 0xB3(Removed, VGH voltage setting by times, merge in 0xB9) 0xB5(Change to VGL_REG cmd, VGL voltage setting by time, merge in 0xBA) 0xB6, 0xB7(Removed AVDD/AVEE 3.5X, 4X function) 0xBA(Removed LVGL, change to VGLX) 0xD1 to 0xD6(Gamma 2.2 to 10 bits control) 0xE9 to 0x0xEB(Gamma1.0, 1.8, 2.5 to 10 bits control) 3. Pad chapter update 4. Timing Example update 5. Auto Sequence update	Kevin		Dennis	2010/04/28



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0.03	1. Page 0 Command Modification Page0/1 switch function modified 0xB1(RGBBP, CREV removed, add Dis_eotp_Hs) 0xB4(vivid color type selection) 0xB9(PTVCM removed, PT[1:0] to PTD1, PTD0, description update) 0xC8(add BSWAP function) 0xD0, 0xD1,0xD6~0xD8,0xDF,0xE002,0xEc(KBBC function removed) 0xD2(CMCT DD_C removed, KBBC related bits) 0xD3~0xD5(description update) 0xD9(removed) 0xB5(resolution typo) 0xB6~0xBB,0xBD(update Default Value) 0xBD,0xBE,0xBF(description update) 0xDD(update description) 0xE1,0xEA,0xEB(Graph update) 2. Page 1 Command Modification 0xB6(AVDD to 1.66X, default value update) 0xB7,0xB8,0xBB,0xD0,0xEE,0xEF,0xD0~0xD6 (update Default Value) 0xBE,0xC6,0xED,0xEF(update description) 3. Maximum resistance (I2C_SAI to RGBBP) 4. component list update	Kevin	sw IR	Dennis	2010/07/27
0.04	General version of Application Note	Kevin	SW	Dennis	2010/11/15
M					

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1 COMMAND DESCRIPTIONS

1.1 Manufacture Command Set Selection

Table 1.1.1 Manufacture Command Set

Address				Parameter											
Instruction	ACT	R/W	МІРІ	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function	
				F000h	00h	0	1	0	1	0	1	0	1	Manufacture command enable	
					F001h	00h	1	0	1	0	1	0	1	0	
MAUCCTR	Dir	W	F0h	F002h	00h	0	1	0	1	0	0	1	0		
				F003h	00h	-	-			MAUC	-	-	1-1		
				F004h	00h	-	-	1	1	-	-	-	PAGE		

NOTE:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line

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MAUCCTR: Manufacture Command Set Control (F000h~F004h)

		Add		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			F000h	00h	0	1	0	1	0	1	0	1
			F001h	00h	1	0	1	0	1	0	1	0
MAUCCTR	W	F0h	F002h	00h	0	1	0	1	0	0	1	0
			F003h	00h	-	-	-	-	MAUC	ı	-	-
			F004h	00h	-	-	-	-	-	•	-	PAGE

NOTE: "-" Don't care

This command is used to enable/disable the Manufacture Command Set and select the page 0 or page 1
of Manufacture Command Set. Address B0xxh~D9xxh, DDxxh~DFxxh and E0xxh~EFxxh for each page.
of Manufacture Command Set. Address Boxxii~Dexxii, DDxxii~Drxxii and Eoxxii~Erxxii each page.

	Bit	Description	Value
Description	MAUC	Manufacture Command Set enable/disable	"0": Manufacture Command Set disable "1": Manufacture Command Set enable
	PAGE	Manufacture Command Set selection	"0": Page 0 "1": Page 1

Note: This command is always enable even Manufacture Command Set is disable.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

U	Default Value						
Status	F000h	F001h	F002h	F003h (MAUC)	F004h (PAGE)		
Power On Sequence	55h	AAh	52h	00h	00h		
S/W Reset	55h	AAh	52h	00h	00h		
H/W Reset	55h	AAh	52h	00h	00h		

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1.2 Manufacture Command Set for Page 0

Table 1.2.1 Manufacture Command Set - Page 0

			Ad	dress		Parameter									
Instruction	ACT	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function	
				B000h	00h	CMRC	VSDL	HSDL	DEDL	PCKP	DEP	HSP	VSP	Set delay, polarity and porch for RGB I/F	
				B001h	00h				VBP	[7:0]					
RGBCTR	DVS	R/W	B0h	B002h	00h				VFP	P[7:0]					
				B003h	00h					[7:0]					
				B004h	00h				HFP	[7:0]					
DOPCTR	Dir	R/W	B1h	B100h	00h	RAMKP	DSITE	DSIG	DSIM	DIS_Eo TP_HS	N565	5 ERR[1:0]		Display optional control	
DOPOTR	DVS	IX/VV	Billi	B101h	00h	-	-	-	TE_PW R_SEL	CRGB	СТВ	CRL	-		
DPCKRGB	DVS	R/W	B3h	B300h	00h	-	-	-	-	-	-	-	ICM	Display clock selection in RGB I/F	
VIVIDCTR	DVS	R/W	B4h	B400h	00h	-	-	-	VCEN	-	-		<u>~ \</u>	Control for vivid color function	
DPRSLCTR	DVS	R/W	B5h	B500h	00h				CGM	/ [7:0]			141	Display resolution control	
SDHDTCTR	DVS	R/W	B6h	B600h	00h	-	-			SDT	[5:0]	15	4117	Set source output data hold time	
GSEQCTR	DVS	R/W	B7h	B700h	00h		GREQ_	ST[3:0]		01	GFEQ	ST[3:0]		EQ control function for gate signals	
GSEQUIK	DVS	IX/VV	D/II	B701h	00h		GREQ_	CK[3:0]		211	GFEQ	CK[3:0]			
				B800h	00h	-	-	-	11-11			ルド	EQMOD	Source control for EQ function	
SDEQCTR	DVS	R/W	B8h	B801h	00h	-			. 11 1.			EQS1[3:0)]		
SDEQUIK	DVS	IX/VV	DOII	B802h	00h			11-11			D	EQS2[3:0			
				B803h	00h			1-1 //	1.7	D .		EQS3[3:0	J.	2 11	
				BB00h	00 h7		ISOP	A[3:0]	U		IGOP	A[3:0]	1117	Set bias current of GOP and SOP	
SGOPCTR	DVS	R/W	BBh	BB01h	00h		T		-		IGOP	B[3:0]	<u> </u>	S.	
				BB02h	00h		ISOP	C[3:0]			IGOP	C[3:0]	<u> </u>		
			5	BC00h	00h	-	-	·	<u>n - </u>	\ -	ΔII	NLA[2:0]		Inversion control	
INVCTR	DVS	R/W	BCh	BC01h	00h	-	-		11-	//-	<i>)</i> `	NLB[2:0]			
		$\Pi \Pi$		BC02h	00h	- /		-	1-1			NLC[2:0]			
		\mathbb{N}		BD00h	00h	n		\\-	ΠV	7.	-	T1A	[9:8]	Display timing control for normal / idle off	
$n \parallel$	// //	$M \square$		BD01h	00h	IIII			T1A	[7:0]				mode in non-RGB I/F	
DPFRCTR1	DVS	R/W	BDh	BD02h	00h	1111		<u>/</u>	VBPD	A[7:0]					
	7)			BD03h	00h	<i>)</i>] \	7		VFPD	A[7:0]					
			0	BD04h	00h		-	-	-	-	-	PSEL	A[1:0]		
N .			11/	BE00h	00h	-	-	-	-	-	-	T1B	[9:8]	Display timing control for idle on mode in	
				BE01h	00h				T1B	[7:0]				non-RGB I/F	
DPFRCTR2	DVS	R/W	BEh	BE02h	00h				VBPD	B[7:0]					
				BE03h	00h				VFPD	B[7:0]					
				BE04h	00h	-	ı	-	-	-	-	PSEL	B[1:0]		
				BF00h	00h					-	-	T1C	[9:8]	Display timing control for partial / idle off	
				BF01h	00h				T1C	[7:0]				mode in non-RGB I/F	
DPFRCTR3	DVS	R.W	BFh	BF02h	00h				VBPD	C[7:0]					
				BF03h	00h				VFPD	C[7:0]					
				BF04h	00h	_	-	-	-	-	-	PSEL	C[1:0]		

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Table 1.2.1 Manufacture Command Set – Page 0 (Continued)

				dress				Para	meter					
Instruction	ACT	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function
				C800h	00h	-	-	-	BSWAP	•	-			Timing control (VGSW=1000, AUO)
				C801h	00h	-	-	-	-	-	-	BI_TY	PE[1:0]	
				C802h	00h				TL1	[7:0]				
				C803h	00h				TL2	7:0]				
				C804h	00h				TL3	7:0]				
				C805h	00h				TL4	7:0]				
				C806h	00h				TR1	[7:0]				
				C807h	00h				TR2	[7:0]				
DPTMCTR8	DVS	R/W	C8h	C808h	00h				TR3	[7:0]				~ //
				C809h	00h				TR4	[7:0]				11 // 22
				C80Ah	00h				TL5	7:0]				
				C80Bh	00h				TL6	7:0]				
				C80Ch	00h				TL7	7:0]			19	// // // // //
				C80Dh	00h				TL8	7:0]			_ 11/2	
				C80Eh	00h				TR5	[7:0]			<i>- 11</i>	Vi -
				C80Fh	00h				TR6	[7:0]	// //	11.11	N	
				C810h	00h				TR7	[7:0]	_//_			
				C811h	00h			Δ	TR8	[7:0]				



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Table 1.2.1 Manufacture Command Set – Page 0 (Continued)

			Ad	dress				Para	meter					
Instruction	ACT	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function
LEDCTRDP	Dir	R/W	D0h	D000h	00h	-	-	LEDON R	LEDON POL	LEDPW M_OEB	CLED _VOL	PWM_E NH_OE	LEDPW POL	Control for LEDON/LEDPWM pins
DIMCTR	DVS	R/W	D2h	D200h	00h	-	-	-	-	SEL_IN	SEL_DE	-	-	Dimming control for CABC and LABC
DIMCTRDP1	DVS	R/W	D3h	D300h	00h		DM_I	N[3:0]	1		DM_D	E[3:0]		Time per step for display brightness by LABC & CABC (fixed-time & fixed- slope)
DIMCTRDP2	DVS	R/W	D4h	D400h	00h	-	-	-	-	-	DMSTP_L[2:0]			Total steps for display brightness by LABC & CABC(fixed-time)
DIMCTRDP3	DVS	R/W	D5h	D500h	00h		STEP_	_IN[3:0]			STEP_	DE[3:0]		Brightness change per step for display brightness by LABC & CABC (fixed-slope)
DIMCTRCB2	DVS	R/W	DDh	DD00h	00h	-	DIM_S	STEP_MC	OV[2:0]	-	DIM_S	TEP_STI	LL[2:0]	Total steps for display brightness by LABC & CABC (fixed-time)
PWMOFFDP	Dir	R/W	DEh	DE00h	00h	-	-	-		PWM_DI	UTY_OFF	SET[4:0]	5	Compensate effective PWM duty for LEDPWM
PWMFRCTR	Dir	R/W	E0h	E000h	00h	-	-	-	-	-	-	حنا	PWMF	PWM frequency adjustment for LEDPWM
	- "			E001h	00h			1	PWMD	IV [7:0]			$\mathcal{L}_{\mathcal{L}_{\mathbf{A}}}$	
FCBRTCB	Dir	R/W	E1h	E100h	00h	-	1	-	255	7/10		1/1	FORCE _CABC_ PWM	Force display brightness for CABC
				E101h	00h			FOF	RCE_CAB	C_DUTY	[7:0]	リー		
				E200h	00h			C	ABC_UI	PWM0[7:	:0]			Display brightness setting corresponding
BRTCBUI	Dir	R/W	E2h	E201h	00h		\Box	C	ABC_UI_	PWM1[7:	:0]	<u> </u>	111	to different gamma algorithm in CABC
BICTOBOT	Dii	10,00	LZII	E202h	00h	(C)	<u> </u>		ABC_UI_			<u>n</u>	11115	UI-mode
				E203h	00h		n		ABC_UI_			<i>> 11</i> -	-11-11	
				E300h	00h	_//_	<i></i>		CABC_P	1/ -		<i>HE</i>	درر	Display brightness setting corresponding
				E301h	00h				CABC_P		1110)) \		to different gamma algorithm in CABC Still-mode
		1 6		E302h E303h	00h 00h			\sim	CABC_P					Sun-mode
		W		E303h E304h				-	CABC_P		_			
BRTCBSTL	Dir	R/W	E3h	E304n E305h	00h 00h	n.		11	CABC_P					
n (// //	AL I		E306h	00h	11 //			CABC_P					
))	M I	-	E307h	00h	-1111		7	CABC_P					
	7)			E308h	00h	-)) \	4		CABC_P					
11 13 -			0	E309h	00h				CABC_P		•			
U			-11	E400h	00h				BC_MOV					Display brightness setting corresponding
			- //	E401h	00h				BC_MOV	•	•			to different gamma algorithm in CABC
			•	E402h	00h				BC_MOV					Moving-mode
				E403h	00h				BC_MOV					
DDTOS (O)	D:	D.444		E404h	00h				BC_MOV		•			
BRTCBMOV	Dir	R/W	E4h	E405h	00h				BC_MOV	•	•			
				E406h	00h				BC_MOV	•	•			
				E407h	00h			CA	BC_MOV	_PWM7[7:0]			
				E408h	00h			CA	BC_MOV	_PWM8[7:0]			
				E409h	00h			CA	BC_MOV	_PWM9[7:0]			

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Table 1.2.1 Manufacture Command Set – Page 0 (Continued)

			٨٨	dress		Parameter										
Instruction	ACT	R/W		Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function		
AMOVCTR	Dir	R/W	E5h	E500h	00h	-			M	OVDET[6	:0]			Automatic moving mode detection control		
AWOVCTR	DII	FC/VV	ESII	E501h	00h	-	-	-		M	IOVSC[4:	0]				
FHYSTCTR	Dir	R/W	E6h	E600h	00h	SET_HY ST		-	-	Н	YST_OU	T_VAL[3:	0]	Final hysteresis result control		
HYSTCTR	Dir	R/W	E7h	E700h	00h	HYST_E N	-	-	-		HYST_	WR[3:0]		Internal hysteresis control		
FLTRCTR	Dir	R/W	E8h	E800h	00h	MRF_ BYS	-	-	-		FKP	[3:0]		Median filter and flicker filter control		
				E900h	00				LS[7:0]				Write given ambient light information into		
WRALSV	Dir	R/W	E9h	E901h	00h				LS[1	15:8]				LABC circuit		
				E902h	00h	-	-	-	-	-	-	-	ALS_W	- 0 N N		
RDBRTDPL	Dir	R	EAh	EA00h	00h				RDPWI	И_L[7:0]				Read display brightness value from LABC		
RDBRTDPC	Dir	R	EBh	EB00h	00h				RDPW	/M[7:0]			2	Read display brightness value from CABC		
RDHYST	Dir	R	EDh	ED00h	00h	-	-	-	-	R	D_HYST	_OUT[3:0		Read output hysteresis result of internal hysteresis block		
RDGMA	Dir	R	EEh	EE00h	00h			F	RD_GMA	SET[7:0		<u> </u>	لار	Read gamma curve for current display		
RDALSV	Dir	R	EFh	EF00h	00				ALSV[7:0]					Read the ambient light information		
NDALGV	ווט	IX.	L 111	EF01h	00h			0	AL\$V[15:8]							

NOTE:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line
M		501

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RGBCTR: RGB Interface Signals Control (B000h~B004h)

		Add	ress				Pa	rameter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
			B000h	00h	CRCM	VSDL	HSDL	DEDL	PCKP	DEP	HSP	VSP		
			B001h	00h	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0		
RGBCTR	R/W	B0h	B002h	00h	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0		
			B003h	00h	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0		
			B004h	00h	HFP7	HFP6	HFP5	HFP4	HFP3	HFP2	HFP1	HFP0		

NOTE: "-" Don't care

This command is used to define the operation status and vertical / horizontal porch of RGB interface. The setting becomes effective as soon as the command is received.

	Bit	Description	Value
	CRCM	Select the RGB mode1/mode 2	"0" = RGB mode 1
	OROW	delect the NGB mode l/mode 2	"1" = RGB mode 2
	VSDL	VS Delay Setting	"0" = No delay
	VODE	ve belay ecting	"1" = Delay 0.5 PCLK
	HSDL	HS Delay Setting	"0" = No delay
	HODE	113 Delay Setting	"1" = Delay 0.5 PCLK
	DEDL	DE Delay Setting	"0" = No delay
G	DEDL	DE Delay Setting	"1" = Delay 0.5 PCLK
N	PCKP	PCLK Fetch Polarity	"0" = Data latched at the rising edge of PCLK
	TONI	PCER Fetch Foliality	"1" = Data latched at the falling edge of PCLK
	DEP	DE Enable Polarity	"0" = High enable for RGB interface
	DLI	DE L'Hable i blafity	"1" = Low enable for RGB interface
	HSP	H-Sync Pulse Level	"0" = Low pulse level sync clock
	MOP	11-3ylic Fuise Level	"1" = High pulse level sync clock
	VSP	V-Sync Pulse Level	"0" = Low pulse level sync clock
	۷۵۱	v-Sylic i dise Level	"1" = High pulse level sync clock
	VBP[7:0]	V-Sync Back Porch	"05h" to "FFh" = 5 to 255 H-Sync clocks
	VFP[7:0]	V-Sync Front Porch	"02h" to "FFh" = 2 to 255 H-Sync clocks
	HBP[7:0]	H-Sync Back Porch	"05h" to "FFh" = 5 to 255 PCLK clocks
	HFP[7:0]	H-Sync Front Porch	"02h" to "FFh" = 2 to 255 PCLK clocks

The registers VBP[7:0], VFP[7:0], HBP[7:0] and HFP[7:0] for vertical and horizontal porch control are used in RGB interface mode 2 only. The setting value "00h" is invalid for all of these four registers.

RGB IF Mode	PCLK	DE	D[23:0]	VS	HS	VBP[7:0], VFP[7:0], HBP[7:0], HFP[7:0]
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Restriction $VFP[7:0] \ge \text{``02h''}, VBP[7:0] \ge \text{``05h''}$ $HFP[7:0] \ge \text{``02h''}, HBP[7:0] \ge \text{``05h''}$

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	Status	i .		Α	vailability	
	Normal Mode On, Idle M	ode Off, Sleep	Out		Yes	
Register	Normal Mode On, Idle M	ode On, Sleep	Out		Yes	
Availability	Partial Mode On, Idle Mo	ode Off, Sleep	Out		Yes	
-	Partial Mode On, Idle Mo	ode On, Sleep	Out		Yes	
	Sleep I	n			Yes	
	_					n
				Default Value	20	
	Status	Doooh	B001h	B002h	B003h	B004h
5 ()		B000h	(VBP)	(VFP)	(HBP)	(HFP)
Default	Power On Sequence	00h	05h	02h	05h	02h
	S/W Reset	00h	05h	02h	05h	02h
	H/W Reset	00h	05h	02h	05h	02h
		Ala Ala				



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DOPCTR: Display Option Control (B100h~B101h)

		Add	ress	Parameter										
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
DOPCTR	R/W	B1h	B100h	00h	RAMKP	DSITE	DSIG	DSIM	DIS_Eo TP_HS	N565	ERR1	ERR0		
DOPCIK	IX/VV	וווט	B101h	00h	-	-	-	TE_PW R_SEL	CRGB	СТВ	CRL	-		

NOTE: "-" Don't care

This command is used to do some optional control for display and application.

		·						\mathcal{I}				
	Bit	Description				V	alue (MH				
	DAMKD	Frame Memory keep/loss in Sleep-in	6	'0": Conte	nts loss i	in s	sleep-in					
	RAMKP	mode	6	'1": Conte	nts keep	in	sleep-in					
	DSITE	TE line enable/disable	"	'0": TE line	e is disal	ole	d					
	DOILE	TE lifte effable/disable	4	"1": TE line is enabled								
	DSIG	Generic read/write data type	4	'0": Gener	ic read/v	vrit	e disable					
	Dolo	enable/disable for MIPI DSI	4	'1": Gener	ic read/v	vrit	e enable					
	DSIM	Video mode data type enable/disable	6	'0": Video	mode da	ata	type disab	le				
	_	for MIPI DSI	_				type enabl					
	DIS_EoT	"DSI Protocol Violation" error					when error					
	P_HS	reporting enable/disable control					ting when e					
۱	N565	16-bit/pixel format (MSB to LSB)					S[2:0]+B[4:0					
		selection in MIPI command mode					B[4 :0]+G[
							n output lov					
þ	ERR[1:0]	ERR pin output signal setting	"01": ERR pin output CRC error only "10": ERR pin output ECC error only									
	~ 111											
	111/4		"11": ERR pin output CRC and ECC err									
	TE DIVID	TE output voltage level selection		TE_PWF	R_SEL	TE Output Voltage Level						
	TE_PWR _SEL	(only valid when DSTB_SEL=0 or DSTB_SEL=1, VSEL=High and		0		VDDI						
	_SEL	VDDI=1.65~3.3V)		0		VDDA						
		VBB1=1.00 0.0V)	ī	0000	T 505		0 1					
				CRGB	RGB		Order	Gamma				
	0000	RGB-BGR Order selection. This bit is		0	0		RGB	Normal				
	CRGB XOR operation with bit RGB of 3600h			0	1		BGR	RB swap				
				1	0		BGR RGB	RB swap				
			L	I			RGB	Normal				
				СТВ	ML		Direc	ction				
		Vertical scanning direction selection		0	0	F	orward (to	p→bottom)				
	СТВ	for gate control signals. This bit is		0	1	F	Reverse(Bo	ttom→top)				
		XOR operation with bit ML of 3600h.		1	0	R	Reverse (Bo	ottom→top)				
				1	1	F	orward (to	p→bottom)				

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	Bit	De	escription			Value
				CRL	RSMX	Direction
			ata shift direction	0	0	S1 → S1440
Description	CRL	,	ection 8.2). This bit is with bit RSMX of	0	1	S1440 → S1
		3600h comman		1	0	S1440 → S1
		300011 comman	u	1	1	S1 → S1440
	L	•				
Restriction	-					0
						-a M //
		Status			Ava	ilability
	Normal	Mode On, Idle Me	ode Off, Sleep Out		\	res
Register			ode On, Sleep Out			res
Availability	Partial	Mode On, Idle Mo	ode Off, Sleep Out			res
·	Partial	Mode On, Idle Mo	ode On, Sleep Out		,	res
		Sleep I			`	(es
		6	2 ()		nn	
		- n		0		Mr.
	150			Defau	ılt Value	
	25/1	Status	B100h		1	B101h
Default	Power	On Sequence	4Ch			00h
	S	W Reset	4Ch	· · · · · · · · · · · · · · · · · · ·		00h
<i> </i>	H,	W Reset	4Ch			00h
	n					
$\pi \sigma$						

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DPCKRGB: Display Clock in RGB Interface (B300h)

Inst / Para	R/W	Address		Parameter									
Inst / Para R/		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
DPCKRGB	Write	Χ	B300h	00h	0	0	0	0	0	0	0	ICM	

NOTE: "-" Don't care

NOTE: "-" Don't car	е							
	Tł	nis comma	and is used to select SRAI	M data input pa	th and displa	y clock in RGB interface.		
		ICM	Data Writ	te to SRAM		SRAM Data Read to Display		
Description		ICIVI	SRAM Write Clock	SRAM Data	Input Path	Internal Display Clock		
Description		0	PCLK	D[23:0]		VS, HS and PCLK	1	
	1 [SCL	SD	l	Internal Oscillator	1	
	Ν	ote: This c	command is active in RGE	interface only.				
Restriction	-						1	
			Status		- 18	Availability		
		Norma	al Mode On, Idle Mode Off	Yes				
Register			al Mode On, Idle Mode On		11 11 11	Yes		
Availability			l Mode On, Idle Mode Off	~ 11 11 3		Yes		
			l Mode On, Idle Mode On	11 11 / / / / / /	U	Yes		
			Sleep In		_ 11	Yes		
		L	/n // /n //					
		1		s ((
4	G		Status			Default Value		
Default	W	11 12	Power On Sequence			ICM = "0"		
Delauli	М	110	S/W Reset	ICM = "0"				
<u> </u>	۱ ر		H/W Reset	"		ICM = "0"		
		7						

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VIVIDCTR: Vivid Color Function Control (B400h)

		Add	ress				Pai	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
VIVIDCTR	R/W	B4h	B400h	00h	-	-	-	VCEN	-	-	-	-

NOTE: "-" Don't care	Э									
	This	command is us	sed to contr	ol vivid color function	•					
		Bit		Description		Value				
Description		VCEN	Enable co	Enable control for vivid color function		"0": Disable				
		VOLIV	Lilabic co			"1": Enable				
Restriction	-									
			Status		1111	Availability				
				ode Off, Sleep Out	<u> اا اا د</u>	Yes				
Register	L			ode On, Sleep Out	11-	Yes				
Availability				de Off, Sleep Out		Yes				
	-	Partial Mode On, Idle Mode On, Sleep Out Yes								
			Sleep Ir		Jie	Yes				
-	2									
P_{∞}			-							
		Status		900	De	efault Value				
N (()) //	ነ Ľ		<u> </u>			B400h				
Default	L	Power On Se		U		00h				
11 2	L'	S/W Res				00h				
		H/W Res	et			00h				
		U								

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DPRSLCTR: Display Resolution Control (B500h)

		Address			Parameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
DPRSLCTR	R/W	B5h	B500h	00h	CGM7	CGM6	CGM5	CGM4	CGM3	CGM2	CGM1	CGM0		

NOTE: "-" Don't care

	CGM[7:0]: display scan lin	e setting.
	CGM[7:0]	Display Resolution
	00h	480RGB x 640
	01h	480RGB x 642
	02h	480RGB x 644
	:	: (2 lines/Step)
Description	28h	480RGB x 720
Description	:	: (2 lines/Step)
	50h	480RGB x 800
	:	: (2 lines/Step)
	6Bh	480RGB x 854
	: 1	: (2 lines/Step)
	70h	480RGB x 864
	Others	reserved

This command is used to control the display resolution.

Note: RGBBP is connected to "VSSI".

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Status	B500h
Power On Sequence	50h
S/W Reset	50h
H/W Reset	50h
·	

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SDHDTCTR: Source Output Data Hold Time Control (B600h)

		Address			Parameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
SDHDTCTR	R/W	B6h	B600h	00h	-	-	SDT5	SDT4	SDT3	SDT2	SDT1	SDT0		

NOTE: "-" Don't care	е	
	This command is used to cor	ntrol the source output data hold time.
	SDT[5:0]: set source output of	data hald tima
		of Clock Data Hold Time
	` ' · ·	0 0.0µs
		10 0.5µs
Description		20 1.0µs
Description	:	: : (0.5µs/Step)
	05h	50 2.5µs
	:	: : (0,5µs/Step)
		610 30.5µs
		520 31.0µs
	3Fh	530 31.5µs
Restriction	- //	
	aris IV	
Π	Statu	us Availability
	Normal Mode On, Idle I	
Register	Normal Mode On, Idle I	Mode On, Sleep Out Yes
Availability	Partial Mode On, Idle N	Mode Off, Sleep Out Yes
	Partial Mode On, Idle N	·
U	Sleep	o In Yes
		5.6 (0)(1
	Status	Default Value
Default	Power On Sequence	B600h (SDT) 05h
Delault	S/W Reset	05h
	H/W Reset	05h
1	1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	1 00

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GSEQCTR: EQ Control Function for Gate Signals (B700h~B701h)

Inst / Para R/M		Address		Parameter									
	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GSEQCTR R/W B	DAM	B7h	B700h	00h	GREQ_ ST3	GREQ_ ST2	GREQ_ ST1	GREQ_ ST0	GFEQ_ ST3	GFEQ_ ST2	GFEQ_ ST1	GFEQ_ ST0	
	D/II	B701h	00h	GREQ_ CK3	GREQ_ CK2	GREQ_ CK1	GREQ_ CK0	GFEQ_ CK3	GFEQ_ CK2	GFEQ_ CK1	GFEQ_ CK0		

NOTE: "-" Don't care

This command is used to control the EQ function for gate signals.

THIS COMMINATIONS	used to contro		n gate signals.							
GREQ_XX[3:0]: time setting of EQ step for rising edge.										
GREQ_ST[3:0	No. of Clock	EQ for Rising Edge	GREQ_CK[3:0]	No. of Clock	EQ for Rising Edge					
0h	0	0.0µs	0h	0	0.0µs					
1h	10	0.5µs	1h)	10	0.5µs					
2h	20	1.0µs	2h	20	1.0µs					
:	:	: (0.5µs/Step)			: (0.5µs/Step)					
7h	70	3.5µs	7h	70	3.5µs					
:	n ((`	: (0.5µs/Step)			: (0.5µs/Step)					
Dh	130	6.5µs	Dh	130	6.5µs					
Eh	140	7.0µs	Eh	140	7.0µs					
Fh	150	7.5µs	Fin	150	7.5µs					

GFEQ XX[3:0]: time setting of EQ step for falling edge.

Description

Of Ed_70t[o.o]. timo	oounig of L	a crop for raining o	ago.		
GFEQ_ST[3:0]	No. of Clock	EQ for Falling Edge	GFEQ_CK[3:0]	No. of Clock	EQ for Falling Edge
Oh	0	0.0µs	0h	0	0.0µs
14	10	0.5µs	1h	10	0.5µs
2h	20	1.0µs	2h	20	1.0µs
	:	: (0.5µs/Step)	:	:	: (0.5µs/Step)
7h	70	3.5µs	7h	70	3.5µs
:		: (0.5µs/Step)	:	••	: (0.5µs/Step)
Dh	130	6.5µs	Dh	130	6.5µs
Eh	140	7.0µs	Eh	140	7.0µs
Fh	150	7.5µs	Fh	150	7.5µs

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	The GREQ_XX and GFEQ_XX are u	used to control E	Q function for differen	t gate signals as below.	
Description	GREQ_ST[3:0], GFEQ_ST[3:0]	GREQ_CK[3	:0], GFEQ_CK[3:0]		
Description	STV B/L V/ END B/L	CLK_R/L, XCI	LK_R/L		
	STV_R/L, V_END_R/L	Bi1_R/L, Bi2	_R/L		
Restriction	-				
	Status		Av	ailability	
	Normal Mode On, Idle Mode O	ff, Sleep Out		Yes	
Register	Normal Mode On, Idle Mode O	n, Sleep Out	Yes		
Availability	Partial Mode On, Idle Mode Of	de Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode Or	n, Sleep Out		Yes	
	Sleep In			Yes	
				1 1 11 11 11 11 11 11 11 11 11 11 11 11	
	Status		Default Value	0	
	B70	00h (GREQ_ST,	GFEQ_ST) B701h	(GREQ_CK, GFEQ_CK)	
Default	Power On Sequence	77h		77h	
	S/W Reset	77h		77h	
	H/W Reset	77h		77h	

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SDEQCTR: EQ Control Function for Source Driver (B800h~B803h)

		Address			Parameter							
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
		B800h	00h	-	-	-	-	-	-	-	EQ MOD0	
SDEQCTR	R/W	B8h	B801h	00h	-	-	-	-	EQS13	EQS12	EQS11	EQS10
			B802h	00h	-	-	-	-	EQS23	EQS22	EQS21	EQS20
			B803h	00h	-	-	-	-	EQS33	EQS32	EQS31	EQS30

NOTE: "-" Don't care

This command is used to control the EQ function for source driver.

EQMOD0: EQ mode 1/mode 2 selection

EQMOD0	EQ Mode
0	EQ mode 1
1	EQ mode 2

EQS1[3:0]: time setting for EQ step 1

EQS1[3:0]	No. of Clock	Time for EQ Step 1
0h	5 / 0	0.0µs
1h,	10	0.5µs
		: (0.5µs/Step)
7h	70	3.5µs
	: 6	: (0.5µs/Step)
Eh	140	7.0µs
Fh	150	7.5µs

Description

E	Q	32	[3:0]: ti	me	set	ting	for	EQ	step	2 (
								_		_	

EQ\$2[3:0]	No. of Clock	Time for EQ Step 2
0h	0	0.0µs
1h	10	0.5µs
:	:	: (0.5µs/Step)
7h	70	3.5µs
:	:	: (0.5µs/Step)
Eh	140	7.0µs
Fh 150		7.5µs

E	EQS3[3:0]: time setting for EQ step 3							
	EQS3[3:0]	No. of Clock	Time for EQ Step 3					
	0h 0		0.0µs					
	1h 10		0.5µs					
	: :		: (0.5µs/Step)					
	7h	70	3.5µs					
	:	:	: (0.5µs/Step)					
	Eh 140		7.0µs					
	Fh 150		7.5µs					

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Description							
Restriction	- When source EQ (EQS1=EQ	S2=EQS3=0), plea	se set the EQMO	DD0 = 0 (EQ Mode	e1).		
	Status			Availability			
Register	Normal Mode On, Idle Me	•		Yes			
Availability	Normal Mode On, Idle M	•		Yes			
7 (Valiability	Partial Mode On, Idle Mo	•		Yes			
	Partial Mode On, Idle Mo	ode On, Sleep Out		Yes			
	Sleep I	n		Yes			
			Defaul	t Value			
	Status	B800h	B801h (EQS1)	B802h (EQS2)	B803h (EQS3)		
Default	Power On Sequence	00h	07h	07h	07h		
	S/W Reset	00h	07h	07h	07h		
	H/W Reset	00h	07h	07h	07h		
		211 111/2	Jn U	THERE			



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SGOPCTR: Source Driver Control (BB00h~BB02h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			BB00h	00h	ISOPA3	ISOPA2	ISOPA1	ISOPA0	IGOPA3	IGOPA2	IGOPA1	IGOPA0
SGOPCTR	R/W	BBh	BB01h	00h	-	-	-	-	IGOPB3	IGOPB2	IGOPB1	IGOPB0
			BB02h	00h	ISOPC3	ISOPC2	ISOPC1	ISOPC0	IGOPC3	IGOPC2	IGOPC1	IGOPC0

NOTE: "-" Don't care

This command is used to control the bias current of GOP and SOP in different display mode.

ISOPA[3:0]: the bias current for source OP in normal / idle off mode.

ISOPC[3:0]: the bias current for source OP in partial / idle off mode.

'	or otoloj, trie bias carre	nicioi source Or in partial	/ laic on mode.	
	ISOPA[3:0]	Bias Current	ISOPA[3:0]	Bias Current
L	ISOPC[3:0]	of Source OP	ISOPC[3:0]	of Source OP
	0h	Minimum	8h	Medium Low
	1h	Minimum High	9h	Medium
	2h	Small Low	Ah	Medium High
	3h	Small	Bh	Large Low
	4h	Small High	Ch	Large
	5h	Small Medium Low	Dh	Large High
	6h	Small Medium	Eh	Maximum Low
	Zh	Small Medium High	J-h	Maximum

Description

IGOPA[3:0]: the bias current for source OP in normal / idle off mode.

IGOPB[3:0]: the bias current for source OP in idle on mode.

IGOPC[3:0]: the bias current for source OP in partial / idle off mode.

IGOPA[3:0] IGOPB[3:0] IGOPC[3:0]	Bias Current of Gamma OP	IGOPA[3:0] IGOPB[3:0] IGOPC[3:0]	Bias Current of Source OP
Oh	Minimum	8h	Medium Low
1h	Small	9h	Medium
2h	Medium Low	Ah	Medium High
3h	Medium	Bh	Large Low
4h	Medium High	Ch	Large
5h	Large	Dh	Large High
6h	Large High	Eh	Maximum Low
7h	Maximum	Fh	Maximum

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Restriction	-			
Register Availability	Status Normal Mode On, Idle Mo Normal Mode On, Idle Mo Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availabili Yes Yes Yes Yes Yes	ty
Default	Status Power On Sequence S/W Reset	BB00h 22h 22h	Default Value BB01h 02h	8B02h 22h 22h
	H/W Reset	22h	02h	22h



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INVCTR: Inversion Driving Control (BC00h~BC02h)

		Add	ress				Pai	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			BC00h	00h	-	-	-	-	-	NLA2	NLA1	NLA0
INVCTR	R/W	BCh	BC01h	00h	-	-	-	-	-	NLB2	NLB1	NLB0
			BC02h	00h	-	-	-	-	-	NLC2	NLC1	NLC0

MOTE ""D "								
NOTE: "-" Don't car	9							
	This command is used to control	ol the inversion mode for	or source driver.					
	NLA[2:0]: the inversion mode for source driver in normal / idle off mode.							
	NLB[2:0]: the inversion mode for source driver in idle on mode.							
	LC[2:0]: the inversion mode for source driver in partial / idle off mode.							
	NLA[2:0], NLB[2:0], NLC[2:		// //n					
Description	000	Colur	nn inversion	V				
Booonplion	001	1-do	of inversion					
	010	2-do	ot inversion					
	011	3-do	ot inversion					
	100	4-dc	ot inversion					
	101//	Zigza	ag inversion					
	110-111		eserved					
Restriction								
M(U)	Status		Availat	ability				
	Normal Mode On, Idle Mo	de Off, Sleep Out	Yes					
Register	Normal Mode On, Idle Mo	-	Yes					
Register Availability	Normal Mode On, Idle Mo Partial Mode On, Idle Mo	ode On, Sleep Out	Yes Yes	3				
111 /1-	Partial Mode On, Idle Mo	ode On, Sleep Out de Off, Sleep Out		3				
111 /1-	16/ 1111 111 2	de On, Sleep Out de Off, Sleep Out de On, Sleep Out	Yes	3 3				
111 /1-	Partial Mode On, Idle Mo Partial Mode On, Idle Mo	de On, Sleep Out de Off, Sleep Out de On, Sleep Out	Yes Yes	3 3				
111 /1-	Partial Mode On, Idle Mo Partial Mode On, Idle Mo	de On, Sleep Out de Off, Sleep Out de On, Sleep Out	Yes Yes	3 3				
111 /1-	Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In	de On, Sleep Out de Off, Sleep Out de On, Sleep Out	Yes Yes	3 3				
111 /1-	Partial Mode On, Idle Mo Partial Mode On, Idle Mo	de On, Sleep Out de Off, Sleep Out de On, Sleep Out	Yes Yes	3 3				
111 /1-	Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In	de On, Sleep Out de Off, Sleep Out de On, Sleep Out	Yes Yes Yes Default Value	S				
Availability	Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In	de On, Sleep Out de Off, Sleep Out de On, Sleep Out n BC00h (NLA)	Yes Yes Yes Default Value BC01h (NLB)	BC02h (NLC)				
Availability	Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In Status Power On Sequence	de On, Sleep Out de Off, Sleep Out de On, Sleep Out n BC00h (NLA) 00h	Pes Yes Yes Default Value BC01h (NLB) 00h	BC02h (NLC) 00h				
Availability	Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In Status Power On Sequence S/W Reset	bode On, Sleep Out de Off, Sleep Out de On, Sleep Out n BC00h (NLA) 00h 00h	Pes Yes Yes Default Value BC01h (NLB) 00h 00h	BC02h (NLC) 00h 00h				

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DPFRCTR1: Display Timing Control in Normal / Idle Off Mode (BD00h~BD04h)

		Add	ress				Pa	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			BD00h	00h	-	-	-	-	-	-	T1A9	T1A8
			BD01h	00h	T1A7	T1A6	T1A5	T1A4	T1A3	T1A2	T1A1	T1A0
			BD02h	00h	VBPDA	VBPDA	VBPDA	VBPDA	VBPDA	VBPDA	VBPDA	VBPDA
DPFRCTR1	R/W	BDh	DD0ZII	0011	7	6	5	4	3	2	1	0
			BD03h	00h	VFPDA	VFPDA	VFPDA	VFPDA	VFPDA	VFPDA	VFPDA	VFPDA
			DD03H	0011	7	6	5	4	3	2	1	0
			BD04h	00h	-	-	-	-	-		PSELA 1	PSELA 0

NOTE: "-" Don't care

This command is used to set the display time of one scan line (Hsync), the vertical blanking porch line, and pixel clock frequency for display timing in normal / idle off mode.

T1A[9:0]: the display time of one scan line in normal / idle off mode.

ir itoloji trio die	play anno or one ocarri	ino in nomial, rate on mode.
T1A[9:0]	No. of Pixel Clock	Display Time for One Scan Line (Pixel Clock=20 MHz)
0d~256d		reserved
257d	258	12.90 µs
258d	259	12.95 µs
		: (0.05 µs/Step)
388d	389	19.45 μs
		: (0.05 µs/Step)
1022d <u> </u>	1023	51.15 μs
10 23 d	1024	51.20 μs

Description

VBPDA[7:0]: the vertical back porch lines in normal / idle off mode.

VFPDA[7:0]: the vertical front porch lines in normal / idle off mode.

٠.	= , 10 1 11.0 1	ordoar front poron lines in front	iai / iaio oii iiioao	-	
	VBPDA[7:0]	No. of Vertical Porch Line	VFPDA[7:0]	No. of Vertical Porch Line	
	00h~01h	reserved	00h~01h	reserved	
	02h	2 lines	02h	2 lines	
	03h	3 lines	03h	3 lines	
	:	: (1 line/Step)	:	: (1 line/Step)	
	1Ch	28 lines	1Ch	28 lines	
	:	: (1 line/Step)	:	: (1 line/Step)	
	FEh	254 lines	FEh	254 lines	
	FFh	255 lines	FFh	255 lines	

PSELA[1:0]: the pixel clock frequency selection in normal / idle off mode.

PSELA[1:0]	Divisor Condition			
00h	1			
01h	2			
02h	4			
03h	8			

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	The display f	rame frequen	cy is decided by	T1A[9:0)] and this verti	cal porch lines	as belov	N.	
			20 MF	łz					
	Frame Rate	=,	PSEL	A					
		T1A×(VBP	DA + VFPDA + V	ertical S	Scanning Lines	s)			
	The Vertical below.	The Vertical Scanning Line in formula and the default values of these registers are fixed by CGM[2:0] as below.							
	CCMIZIO	Display	Default Va	lue	Default Valu	ıe (VBPDA+VF	PDA)	Frame rate	
Description	CGM[7:0]	Resolution	T1A[9:0]	μs	VBPDA[7:0]	VFPDA[7:0]	ms	(Hz)	
	FFh	360x640	01E3h (483d)	24.20	18h (24d)	18h (24d)	1.162	60.06	
	FEh	480x360	0363h (867d)	43.40	0Ch (12d)	0Ch (12d)	1.042	60.00	
	00h	480x640	01E3h (483d)	24.20	18h (24d)	18h (24d)	1.162	60.06	
	28h	480x720	01B1h (433d)	21.70	18h (24d)	18h (24d)	1.042	60.00	
	50h	480x800	0184h (388d)	19.45	1Ch (28d)	1Ch (28d)	1.089	60.06	
	6Bh	480x854	016Ch (364d)	18.25	1Dh (29d)	1Dh (29d)	1.058	60.08	
	70h	480x864	0166h (358d)	17.95	20h (32d)	20h (32d)	1,149	60.03	
				× 11 12					
	T1A[9:0] ≥ 10	, ,		1131		n = n			
Restriction		≥ 3, VFPDA[7	11 \\ 11	11 0		70. "0"			
	VBPDA[7:0]-	FVFPDA[7:0]+	-Vertical Scan Li	nes = m	ultiple of 8 if Pi	RG= U			
				n			.,		
1	M-11	\	atus	<i>211</i>		Availabil	ity		
\mathbb{R}			Mode On, Idle Mode Off, Sleep Out			Yes			
Register			le Mode On, Sle			Yes			
Availability	_		e Mode Off, Slee			Yes			
	Partial	- 11 11	e Mode On, Slee	ep Out		Yes			
11 0		Sie	ep In			Yes			
	11/4								
					Defa	ult Value			
	Status			D01h	BD02h	BD03h		BD04h	
	Default Power On Sequence		(T1A)		(VBPDA)	(VFPDA)		(PSELA)	
Default					1Ch	1Ch		00h	
	S	/W Reset	0184h)	1Ch	1Ch		00h	
		/W Reset	0184h)	1Ch	1Ch		00h	
							_		



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DPFRCTR2: Display Timing Control in Idle On Mode (BE00h~BE04h)

		Add	ress				Pai	rameter						
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
			BE00h	00h	-	-	-	-	-	-	T1B9	T1B8		
			BE01h	00h	T1B7	T1B6	T1B5	T1B4	T1B3	T1B2	T1B1	T1B0		
			BE02h	BE02h	BE02h	00h	VBPDB	VBPDB	VBPDB	VBPDB	VBPDB	VBPDB	VBPDB	VBPDB
DPFRCTR2	R/W	BEh	DLUZII	0011	7	6	5	4	3	2	1	0		
J			BE03h	00h	VFPDB	VFPDB	VFPDB	VFPDB	VFPDB	VFPDB	VFPDB	VFPDB		
			BEUSII	0011	7	6	5	4	3	2	1	0		
			BE04h	00h						- F	PSELB	PSELB		
			DE0411	0011	,		-	•	,		1/1/1	0		

NOTE: "-" Don't care

This command is used to set the display time of one scan line (Hsync), the vertical blanking porch line, and pixel clock frequency for display timing in idle on mode.

T1B[9:0]: the display time of one scan line in idle on mode.

T1B[9:0]	No. of Pixel Clock	Display Time for One Scan Line (Pixel Clock=20 MHz)
0d~256d		reserved
257d	258	12.90 µs
258d	259	12,95 µs
		: (0.05 µs/Step)
388d	389	19.45 µs
		: (0.05 µs/Step)
1022d	1023	51.15 μs
1023d	1024	51.20 μs

Description

VBPDB[7:0]: the vertical back porch lines in idle on mode.

VFPDB[7:0]: the vertical front porch lines in idle on mode.

VBPDB[7:0]	No. of Vertical Porch Line	VFPDB[7:0]	No. of Vertical Porch Line
00h~01h	reserved	00h~01h	reserved
02h	2 lines	02h	2 lines
03h	3 lines	03h	3 lines
:	: (1 line/Step)	:	: (1 line/Step)
1Ch	28 lines	1Ch	28 lines
:	: (1 line/Step)	:	: (1 line/Step)
FEh	254 lines	FEh	254 lines
FFh	255 lines	FFh	255 lines

PSELB[1:0]: the pixel clock frequency selection in idle on mode.

PSELB[1:0]	Divisor Condition
00h	1
01h	2
02h	4
03h	8

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	The display frame frequency is decided by T1B[9:0] and this vertical porch lines as below.							
Description	$Frame Rate = \frac{\frac{20 \text{MHz}}{\text{PSELB}}}{\text{T1B} \times \left(\text{VBPDB} + \text{VFPDB} + \text{Vertical Scanning Lines} \right)}$							
Restriction	T1B[9:0] ≥ 101h (257d) VBPDB[7:0] ≥ 3, VFPDB[7:0] ≥ 3 VBPDB[7:0]+VFPDB[7:0]+Vertical Scan Lines = multiple of 8 if PRG="0"							
	Status Availability							
	Normal Mode On, Idle Mode Off, Sleep Out Yes							
Register	Normal Mode On, Idle Mode On, Sleep Out Partial Mode On Idle Mode Off Sleep Out							
Availability	Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Yes							
	Sleep In Yes							
	Default Value							
	Status BE00h, BE01h BE02h BE03h BE04h							
Default	(T1B) (VBPDB) (VFPDB) (PSELB)							
1	Power On Sequence 0184h 1Ch 1Ch 00h							
	S/W Reset 0184h 1Ch 1Ch 00h							
	H/W Reset 0184h 1Ch 1Ch 00h							

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DPFRCTR3: Display Timing Control in Partial / Idle Off Mode (BF00h~BF04h)

		Add	ress				Pai	rameter						
Inst / Para R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
		_	BF00h	00h	-	-	-	-	-	-	T1C9	T1C8		
			BF01h	00h	T1C7	T1C6	T1C5	T1C4	T1C3	T1C2	T1C1	T1C0		
			DEOOR	BE02h	BF02h	00h	VBPDC	VBPDC	VBPDC	VBPDC	VBPDC	VBPDC	VBPDC	VBPDC
DPFRCTR3	R/W	BFh	DI UZII	0011	7	6	5	4	3	2	1	0		
	,		BF03h	00h	VFPDC	VFPDC	VFPDC	VFPDC	VFPDC	VFPDC	VFPDC	VFPDC		
			DF USIT	oon	7	6	5	4	3	2	1	0		
			BF04h	00h		_	_	_	-	- C [PSELC	PSELC		
			Dru4n	DFU4II	0011						211	111	0	

NOTE: "-" Don't care

This command is used to set the display time of one scan line (Hsync), the vertical blanking porch line, and pixel clock frequency for display timing in partial / idle off.

T1C[9:0]: the display time of one scan line in partial / idle off mode.

T1C[9:0]	No. of Pixel Clock	Display Time for One Scan Line (Pixel Clock=20 MHz)
0d~256d		reserved
257d	258	12.90 µs
258d	259	12,95 µs
		: (0.05 µs/Step)
388d	389	19.45 µs
		: (0.05 µs/Step)
1022d <u> </u>	1023	51.15 μs
1023d	1024	51.20 μs

Description

VBPDC[7:0]: the vertical back porch lines in partial / idle off mode. VFPDC[7:0]: the vertical front porch lines in partial / idle off mode.

V I I	7 FFDG V. oj. tile vertical from porch lines in partial / fule on mode.								
,	VBPDC[7:0]	No. of Vertical Porch Line	VFPDC[7:0]	No. of Vertical Porch Line					
	00h~01h	reserved	00h~01h	reserved					
	02h	2 lines	02h	2 lines					
	03h	3 lines	03h	3 lines					
	:	: (1 line/Step)	:	: (1 line/Step)					
	1Ch	28 lines	1Ch	28 lines					
	:	: (1 line/Step)	••	: (1 line/Step)					
	FEh	254 lines	FEh	254 lines					
	FFh	255 lines	FFh	255 lines					

PSELC[1:0]: the pixel clock frequency selection in partial / idle off mode.

PSELC[1:0]	Divisor Condition
00h	1
01h	2
02h	4
03h	8

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	The display frame frequency is decided by T1[9:0] and this vertical porch lines as below.							
Description	Frame Rate = $\frac{\frac{20\text{MHz}}{\text{PSELC}}}{\text{T1C} \times \left(\text{VBPDC} + \text{VFPDC} + \text{Vertical Scanning Lines}}\right)}$							
Restriction	T1C[9:0] ≥ 101h (257d) VBPDC[7:0] ≥ 3, VFPDC[7:0] ≥ 3 VBPDC[7:0]+VFPDC[7:0]+Vertical Scan Lines = multiple of 8 if PRG="0"							
	Status Availability							
	Normal Mode On, Idle Mode Off, Sleep Out Yes							
Register	Normal Mode On, Idle Mode On, Sleep Out Partial Mode On Idle Mode Off Sleep Out							
Availability	Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Yes							
	Sleep In Yes							
	Default Value							
	Status BF00h, BF01h BF02h BF03h BF04h							
Default	(T1C) (VBPDC) (VFPDC) (PSELC)							
Deladit	Power On Sequence 0184h 1Ch 1Ch 00h							
	S/W Reset 0184h 1Ch 1Ch 00h							
	H/W Reset 0184h 1Ch 1Ch 00h							

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DPTMCTR8: Display Timing Control 8 (C800h~C809h)

		Add	ress				Pa	rameter					
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
			C800h	00h	-	-	-	BSWAP	-	-	-	GOARL X	
			C801h	00h	1	1	-	-	-	1	BI_ TYPE1	BI_ TYPE0	
			C802h	00h	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10	
			C803h	00h	TL27	TL26	TL25	TL24	TL23	TL22	TL21	TL20	
			C804h	00h	TL37	TL36	TL35	TL34	TL33	TL32	TL31	TL30	
		R/W C8h	C805h	00h	TL47	TL46	TL45	TL44	TL43	TL42	TL41	TL40	
			C806h	00h	TR17	TR16	TR15	TR14	TR13	TR12	TR11	TR10	
			C807h	00h	TR27	TR26	TR25	TR24	TR23	TR22	TR21	TR20	
DPTMCTR8	R/W		₹/W C8h	C808h	00h	TR37	TR36	TR35	TR34	TR33	TR32	TR31	TR30
			C809h	00h	TR47	TR46	TR45	TR44	TR43	TR42	TR41	TR40	
			C80Ah	00h	TL57	TL56	TL55	TL54	TL53	TL52	TL51	TL50	
				C80Bh	00h	TL67	TL66	TL65	₹L64	TL63	TL62	TL61	TL60
			C80Ch	0 0h	TL77	TL76	TL75	TL74	TL73	TL72	TL71	TL70	
		7	C80Dh	00h	TL87	TL86	TL85	TL84	TL83	TL82	TL81	TL80	
n		1/ //	C80Eh	00h	TR57	TR56	TR55	TR54	TR53	TR52	TR51	TR50	
		(C80Fh	00h	TR67	TR66	TR65	TR64	TR63	TR62	TR61	TR60	
$W \ W \ _{\mathcal{H}}$		0 -	C810h	00h	TR77	TR76	TR75	TR74	TR73	TR72	TR71	TR70	
		-6	C811h	00h	TR87	TR86	TR85	TR84	TR83	TR82	TR81	TR80	

NOTE: "-" Don't care

This command is used to control display timing for VGSW[3:0]="1000".

BSWAP: output signal control for Bi1_L→Bi2_L swap and Bi1_R→Bi2_R swap.

GOARLX: output signal control for XXXX_L↔XXXX_R swap.

Description

The supplier control for 70000 _ Ex 70000 _ Ex 30000 _ Ex 300000 _ Ex 30000 _								
	Output Signal							
Pad Name	GOAR	LX="0"	GOARLX="1"					
	BSWAP="0"	BSWAP="1"	BSWAP="0"	BSWAP="1"				
STV_L	STV_L	STV_L	STV_R	STV_R				
CLK_L	CLK_L	CLK_L	CLK_R	CLK_R				
XCLK_L	XCLK_L	XCLK_L	XCLK_R	XCLK_R				
Bi1_L	Bi1_L	Bi2_L	Bi1_R	Bi2_R				
Bi2_L	Bi2_L	Bi1_L	Bi2_R	Bi1_R				
V_END_L	V_END_L	V_END_L	V_END_R	V_END_R				
STV_R	STV_R	STV_R	STV_L	STV_L				
CLK_R	CLK_R	CLK_R	CLK_L	CLK_L				
XCLK_R	XCLK_R	XCLK_R	XCLK_L	XCLK_L				
Bi1_R	Bi1_R	Bi2_R	Bi1_L	Bi2_L				
Bi2_R	Bi2_R	Bi1_R	Bi2_L	Bi1_L				
V_END_R	V_END_R	V_END_R	V_END_L	V_END_L				

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Description

BI_TYPE[1:0]: gate driving type select according to Bi1/2_R/L signal.

BI_TYPE[1:0]	Gate Driving Type
00	Type 3 (AC w/ 4-lines)
01	Type 1 (DC)
10	Type 2 (AC w/ 2-lines)
11	Type 3 (AC w/ 4-lines)

TL1[7:0]: delay time for rising edge of Bi1_L signal.

TL2[7:0]: delay time for falling edge of Bi1 L signal.

٠.	ELE[7:0]: doldy time for failing dags of Bri_L digital.								
	TL1[7:0]	No. of Clock	Delay Time	TL2[7:0]	No. of Clock	Delay Time			
	00h	0	0.00µs	00h	0	0.00µs			
	01h	1	0.05µs	01h	1	0.05µs			
	:	:	: (0.05µs/Step)	:		: (0.05µs/Step)			
	78h	120	6.00µs	50h	80	4.00µs			
	:	:	: (0.05µs/Step)	. 5		: (0.05µs/Step)			
	FEh	254	12.70µs	PEh	254	12.70µs			
	FFh	255	12. 7 5µs	/ FFI	255	12.75µs			

TL3[7:0]: delay time for rising edge of Bi2_L signal.

TL4[7:0]: delay time for falling edge of Bi2_L signal.

1 <u>= 1[7 .0]. dola</u>	y third for family o				
TL3[7:0]	No. of Clock	Delay Time	TL4[7:0]	No. of Clock	Delay Time
00h	0	0.00µs	00h	0	0.00µs
01h	1	0.05µs	01h	1	0.05µs
	: 1	: (0.05µs/Step)	:	:	: (0.05µs/Step)
78h	120	6.00µs	50h	80	4.00µs
: ($\gg \parallel \parallel \parallel \parallel$: (0.05µs/Step)	:		: (0.05µs/Step)
FEh	254	12.70µs	FEh	254	12.70µs
FFh	255	12.75µs	FFh	255	12.75µs

TR1[7:0]: delay time for rising edge of Bi1_R signal.

TR2[7:0]: delay time for falling edge of Bi1_R signal.

TR1[7:0]	No. of Clock	Delay Time	TR2[7:0]	No. of Clock	Delay Time
00h	0	0.00µs	00h	0	0.00µs
01h	1	0.05µs	01h	1	0.05µs
:	:	: (0.05µs/Step)	:	:	: (0.05µs/Step)
78h	120	6.00µs	50h	80	4.00µs
:	:	: (0.05µs/Step)	:	:	: (0.05µs/Step)
FEh	254	12.70µs	FEh	254	12.70µs
FFh	255	12.75µs	FFh	255	12.75µs

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TR3[7:0]: delay time for rising edge of Bi2_R signal.

TR4[7:0]: delay time for falling edge of Bi2_R signal.

TR3[7:0]	No. of Clock	Delay Time	TR4[7:0]	No. of Clock	Delay Time
00h	0	0.00µs	00h	0	0.00µs
01h	1	0.05µs	01h	1	0.05µs
:	:	: (0.05µs/Step)	:	:	: (0.05µs/Step)
78h	120	6.00µs	50h	80	4.00µs
:	:	: (0.05µs/Step)	:	:	: (0.05µs/Step)
FEh	254	12.70µs	FEh	254	12.70µs
FFh	255	12.75µs	FFh	255	12. 7 5µs

TL5[7:0]: delay time for STV_L signal.

<u> </u>					
TL5[7:0]	No. of Clock	Delay Time			
00h	0	0.00µs			
01h	1	0.05µs			
:	:	: (0.05µs/Step)			
C8h	200	10.00µs			
:	:	: (0.05µs/Step)			
FEh	254	12.70µs			
FFh	255	12.75µs			

Description

TL6[7:0]: delay time for CLK_L signal.

TL6[7:0]	No. of Clock	Delay Time	
00h	0 0	0.00µs	
01h		0.05µs	
: (: (0.05µs/Step)	
C8h	200	10.00µs	
111/11		: (0.05µs/Step)	
FEh	254	12.70µs	
FFh	255	12.75µs	

TL7[7:0]: delay time for XCLK_L signal.

TL7[7:0]	No. of Clock	Delay Time			
00h	0	0.00µs			
01h	1	0.05µs			
:	:	: (0.05µs/Step)			
C8h	200	10.00µs			
:	:	: (0.05µs/Step)			
FEh	254	12.70µs			
FFh 255		12.75µs			

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	TL8[7:0]: del	ay time for V_END	_L signal.	
	TL8[7:0]	No. of Clock	Delay Time	
	00h	0	0.00µs	
	01h	1	0.05µs	
	:	:	: (0.05µs/Step)	
	C8h	200	10.00µs	
	:	:	: (0.05µs/Step)	
	FEh	254	12.70µs	
	FFh	255	12.75µs	
	TR5[7:0]: de	ay time for STV_R	signal	100
	TR5[7:0]: dc	No. of Clock	Delay Time	
	00h	0	0.00µs	
	01h	1	0.05µs	
	:	:	: (0.05µs/Step)	
	C8h	200	10.00µs	
	:	:	: (0.05µs/Step)	
	FEh	254	12.70µs	
	FFh	255	12.75µs	
Description	'			
	TR6[7:0]: de	ay time for CLK_R	signal.	
	TR6[7:0]	No. of Clock	Delay Time	
~ 1	00h	0	0.00µs	
	01h	1	0.05µs	
W = W + W + W + W + W + W + W + W + W +	l I		: (0.05µs/Step)	
	C8h	200	10.00µs	
	<i>\(\(\)</i> : <i>\(\)</i>		: (0.05µs/Step)	
U	FEh	254	12.70µs	
	FFh	255	12.75µs	I
	TR7[7:0]: de	ay time for XCLK_	R signal.	
	TR7[7:0]	No. of Clock	Delay Time	
	00h	0	0.00µs	
	01h	1	0.05µs	
	:	:	: (0.05µs/Step)	
	C8h	200	10.00µs	
	:	:	: (0.05µs/Step)	
	FEh	254	12.70µs	
	FFh	255	12.75µs	I

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I -	LB8[2:0]: 4ela	y time for V_END	P signal		
	TR8[7:0]	No. of Clock	Delay Time		
	00h	0	0.00µs		
	01h	1	0.05µs		
		:	: (0.05µs/Step)		
Description	C8h	200	10.00µs		
	:	:	: (0.05µs/Step)		
	FEh	254	12.70µs		
	FFh	255	12.75µs		
5			1	<u> </u>	
Restriction -					
		Otatus		1	
	<u> </u>	Status	1 0" 01 0 1	AV	ailability
Dogistor			de Off, Sleep Out		Yes
Register Availability		· ·	de On, Sleep Out		Yes
Availability			de Off, Sleep Out		Yes
	Partial N		de On, Sleep Out		Yes
		Sleep In	> ((7/1/	Yes
		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	n v		
	1			Data It Value	U
41	3911	Status		Default Value	
			C800h (GSWAP, GOARLX)	00h
	100		C8	01h (BI_TYPE)	00h
	V _	~ \L \\\		C802h (TL1)	78h
	n ((C803h (TL2)	50h
	M/M			C804h (TL3)	78h
o l				C805h (TL4)	50h
	11 2		(C806h (TR1)	78h
			(C807h (TR2)	50h
	Power C	n Sequence	(C808h (TR3)	78h
Default	FowerC	on Sequence	(C809h (TR4)	50h
				C80Ah (TL5)	C8h
				C80Bh (TL6)	C8h
				C80Ch (TL7)	C8h
				C80Dh (TL8)	C8h
				C80Eh (TR5)	C8h
				C80Fh (TR6)	C8h
				C810h (TR7)	C8h
				C811h (TR8)	C8h
	S/V	V Reset		Same above	
		V Reset		Same above	
		•			

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LEDCTRDP: Control for LEDPWM/LEDON Pins (D000h)

		Add	ress				Pa	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
LEDCTRDP	R/W	D0h	D000h	00h	-	-	LEDON R	LEDON POL	LEDPW M_OEB	CLED _VOL	PWM_E NH_OE	LEDPW POL

NOTE: "-" Don't care

Description

This command is used to control the voltage level, driving ability and active polarity of LEDON and LEDPWM pins.

LEDONR: the On/Off control for LEDON pin.

LEDONR	LEDONPOL	Status of LEDON Pin
0	0	Keep "Low"
0	1	Keep "High"
1	0	Keep "High"
1	1	Keep "Low"

LEDONPOL: the PWM active polarity for LEDON pin.

LEDONPOL	Polarity of LEDON Pin					
LEDONPOL	Lit Period	Non-lit Period				
0	High	Low				
15 N //	Low	High				

LEDPWM_OEB: the enable control for LEDPWM pins.

C[1:0]	LEDPWN	LOEB=0	LEDDWM OFF 1
(Command 5500h)	LEDPWMPOL=0	LEDPWMPOL=1	LEDPWM_OEB=1
00, CABC off	High (100% duty)	Low (100% duty)	Hi-Z
01, UI mode	DW/M way of a rm	PWM waveform	
10, Still mode	PWM waveform (active high)	(active low)	Hi-Z
11, Moving mode	(active mgm)	(active low)	

CLED_VOL: the voltage level for LEDON and LEDPWM pins.

This bit is valid when (1) DSTB_SEL=Low or (2) DSTB_SEL=High, VDDI=1.65~3.3V and VSEL=High . For other conditions, the output voltage level is DIOPWR depend on VDDI input voltage and VSEL (refer to the section Pin Description for VSEL pin).

CLED_VOL	Voltage Level of LEDON/LEDPWM Pins
0	VSSI to VDDI
1	VSSI to VDDA

PWM_ENH_OE: the driving ability control for LEDPWM pin.

PWM_ENH_OE	Driving Ability of LEDPWM Pin
0	1X driving ability
1	2X driving ability

LEDPWPOL: the PWM active polarity for LEDPWM pin.

LEDPWPOL	Polarity of LEDPWM Pin				
LEDPWPOL	Lit Period	Non-lit Period			
0	High	Low			
1	Low	High			

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Restriction	-				
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep I	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes		
	Status	Default Value			
Default	Power On Sequence		000		
	S/W Reset	00h			
	H/W Reset	00h			



NT35510

DIMCTR: Dimming Control for LABC and CABC (D200h)

		Add	ress	Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTR	R/W	D2h	D200h	00h	-	-	-	-	SEL_IN	SEL_DE	-	-

NOTE: "-" Don't care	e						
	This command is used to control	the dimming method for LABC/CABC for display brightness.					
	SEL_IN: the rising dimming type for display brightness change by LABC function.						
	SEL_IN R	Rising Dimming Type for LABC					
Decemination	0	"Fixed Time" type					
Description	1	"Fixed Slope" type					
	SEL_DE: the falling dimming type	e for display brightness change by LABC function.					
	SEL_DE F	alling Dimming Type for LABC					
	0	"Fixed Time" type					
	1	"Fixed Slope" type					
Restriction	-						
	Status	Availability					
	4 // 11						
Deviates	Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Yes Yes						
Register Availability	Partial Mode On, Idle Mode						
Availability	Partial Mode On, Idle Mode On, Sleep Out Yes						
	Sleep In	Yes					
$W \parallel \parallel$	Sieepiii						
U	Status	Default Value					
	Status	D200h					
Default	Power On Sequence	00h					
	S/W Reset	00h					
	H/W Reset	00h					

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DIMCTRDP1: Display Brightness Dimming Control 1 for LABC and CABC (D300h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRDP1	R/W	D3h	D300h	00h	DM_IN3	DM_IN2	DM_IN1	DM_IN0	DM_DE3	DM_DE2	DM_DE1	DM_DE0

NOTE: "-" Don't care

This command is used to control the time per dimming step for fixed-time / fixed-slope type dimming method which used for display brightness change by LABC and CABC.

DM_IN[3:0]: the time of each rising dimming step for Fixed-Time type and Fixed-Slope type.

DM_DF[3:0]: the time of each falling dimming step for Fixed-Time type and Fixed-Slope type.

Description

L	0 M_DE[3:0]: the time of ϵ	ixed-Slope type.		
	DM_IN[3:0]	Time of Rising Dimming Step	DM_IN[3:0]	Time of Rising Dimming Step
	0h	1 frame	0h	1 frame
	1h	2 frames	16	2 frames
	2h	3 frames	2h	3 frames
	:			
	Bh	12 frames	Bh	12 frames
	Ch	13 frames	Ch	13 frames
	Dh 📶	14 frames	Dh	14 frames
	Eh~Fh	reserved	Eh∼Fh	reserved

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Giaius	D300h (DM_IN, DM_DE)	
Power On Sequence	00h	
S/W Reset	00h	
H/W Reset	00h	

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DIMCTRDP2: Display Brightness Dimming Control 2 for LABC and CABC (D400h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRDP2	R/W	D4h	D400h	00h	-	-	-	-	-	DMSTP _L2	DMSTP _L1	DMSTP _L0

NOTE: "-" Don't care

This command is used to control the total dimming steps for fixed-time type dimming method which used for display brightness change by LABC and CABC.

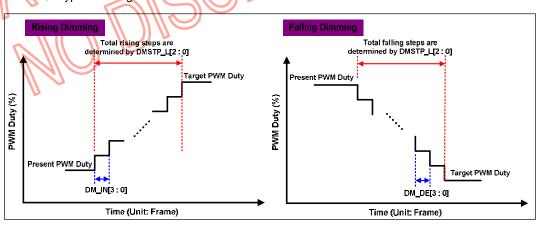
DMSTP_L[2:0]: the total rising/falling dimming steps for Fixed-Time type in Off-Mode and UI-Mode of CABC.

DMSTP_L[2:0]	Total Steps of Rising/Falling Dimming
0h	2 steps
1h	4 steps
2h	8 steps
3h	16 steps
4h	32 steps
5h	64 steps
6h	128 steps
7h, ()	256 steps

Note: The setting of DMSTP_L[2:0] is available when dimming type is set to "Fixed-Time" type and CABC is set to "Off-Mode" and "UI-Mode".

Fixed-Time Type dimming in Off-Mode and UI-Mode





Example 1:

 $DM_IN[3:0]$ is set to 0x03 and DMSTP_L[2:0] is set to 0x06, this means that the time of each rising dimming step is 4 frames and 128 total dimming steps.

So the total dimming time length is 128x4=512 frames for LABC and CABC Off-Mode/UI-Mode. Example 2:

DM_DE[3:0] is set to 0x04 and DMSTP_L[2:0] is set to 0x03, this means that the time of each falling dimming step is 5 frames and 16 total dimming steps.

So the total dimming time length is 16x5=80 frames for LABC and CABC Off-Mode/UI-Mode.

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Restriction	-				
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle Mo	ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes		
Availability	Partial Mode On, Idle Mo	ode On, Sleep Out	Yes Yes		
	Status		Default Value D400h (DMSTR_L)		
Default	Power On Sequence S/W Reset H/W Reset		04h 04h 04h		
	THIV RESEL				



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DIMCTRDP3: Display Brightness Dimming Control 3 for LABC and CABC (D500h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRDP3	R/W	D5h	D500h	00h	STEP _IN3	STEP _IN2	STEP _IN1	STEP _IN0	STEP _DE3	STEP _DE2	STEP _DE1	STEP _DE0

NOTE: "-" Don't care

This command is used to control the brightness change per step for fixed-slope type dimming method which used for display brightness change by LABC and CABC.

STEP_IN[3:0]: the increment of PWM duty for rising dimming for Fixed-Slope type.

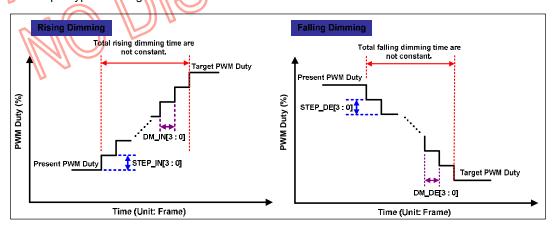
STEP_DE[3:0]: the decrement of PWM duty for falling dimming for Fixed-Slope type.

STEP_IN[3:0]	Increment of PWM Duty	STEP_DE[3:0]	Decrement of PWM Duty
0h	reserved	Oh	reserved
1h	1	1h	1
2h	2	2h	2
3h	3	3h	3
:			
Dh	13	Dh	13
Eb 1	14	Eh\\\	14
Fh	15	THU P	15

Note: The setting of STEP_IN[3:0] and STEP_DE[3:0] are available when dimming type is set to "Fixed-Slope" type.

Description

Fixed-Slope Type dimming



Example 1

DM_IN[3:0] is set to 0x03 and STEP_IN[3:0] is set to 0x0E, this means that the PWM duty will increase 14 (around 14/256=5.47%) per 4 frames until the PWM duty reaches target PWM duty.

Example 2:

DM_DE[3:0] is set to 0x06 and STEP_DE[3:0] is set to 0x05, this means that the PWM duty will decrease 5 (around 5/256=1.95%) per 7 frames until the PWM duty reaches target PWM duty.

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Restriction	-					
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle M Partial Mode On, Idle M Sleep I	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes			
	Status	Default Value D500h (STEP_IN, STEP_DE)				
Default	Power On Sequence		11h2			
	S/W Reset		11/1h			
	H/W Reset		11h			

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DIMCTRCB2: Display Brightness Control 1 for LABC and CABC (DD00h)

		Add	ress				Pa	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DIMCTRCB2	R/W	DDh	DD00h	00h	-	DIM_ STEP_ MOV2	DIM_ STEP _MOV1	DIM_ STEP_ MOV0	•	DIM_ STEP_ STILL2	DIM_ STEP_ STILL1	DIM_ STEP_ STILL0

NOTE: "-" Don't care

This command is used to control the total dimming steps for fixed-time type dimming method which used for display brightness change by LABC and CABC (Moving-Mode and Still-Mode respectively). DIMSTEP_MOV[2:0]: the total rising/falling dimming steps in Moving-Mode of CABC.

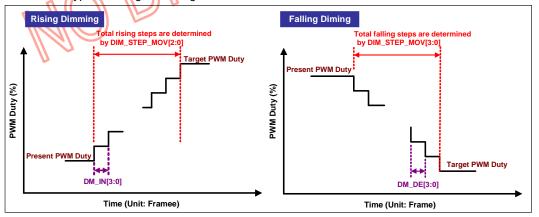
DIMSTEP_STILL[2:0]: the total rising/falling dimming steps in Still-Mode of CABC.

AMOTEL _6TIEL[2.0]: the total hallighalling diffining steps in oth Mode of CABO.										
DIM_STEP_MOV[2:0]	Total Steps of Rising/Falling Dimming	DIM_STEP_STILL[2:0]	Total Steps of Rising/Falling Dimming							
0h	2 steps	0h	2 steps							
1h	4 steps	16	4 steps							
2h	8 steps	2h	8 steps							
3h	16 steps	3h	16 steps							
4h	32 steps	4h	32 steps							
5h	64 steps	5h	64 steps							
6h 1	128 steps	6h	128 steps							
7h	256 steps	7h	256 steps							

Description

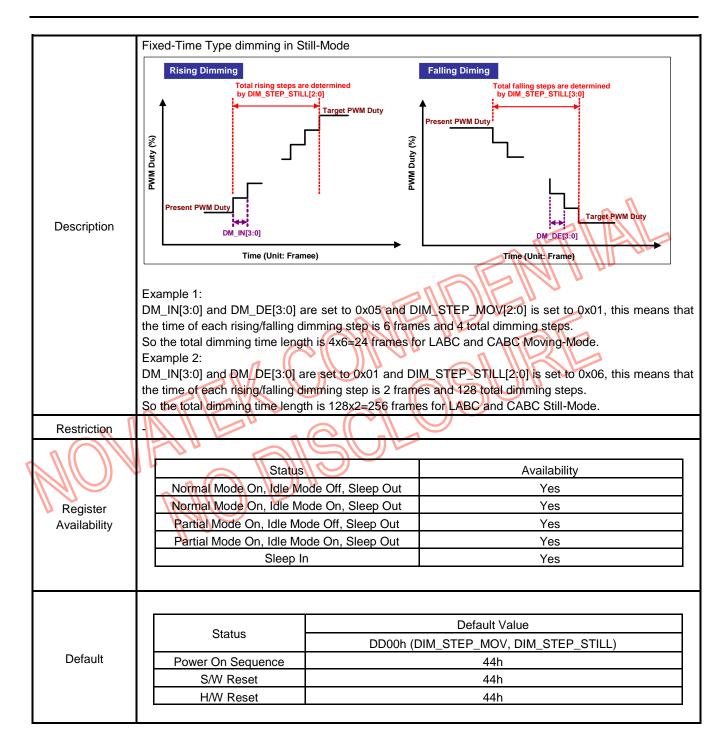
Note: The setting of DM_STEP_MOV[2:0] is available when dimming type is set to "Fixed-Time" type and CABC is set to "Moving-Mode". The setting of DM_STEP_STILL[2:0] is available when dimming type is set to "Fixed-Time" type and CABC is set to "Still-Mode".





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PWMOFFDP: Offset Compensation for LEDPWM Pin (DE00h)

		Add	ress		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
PWMOFFDP	R/W	DEh	DE00h	00h	-	-	-	_	_	_	PWM_D UTY_OF FSET1	_	

NOTE: "-" Don't care	9						
		pensate the effective PWM duty for LEDPWM pin.					
	PWM_DUTY_OFFSET[4:0]: cc	ompensate the effective PWM duty for LEDPWM pin.					
	PWM_DUTY_OFFSET[4	4:0] PWM Duty Offset					
Decemination	0h	+0					
Description	1h	+1					
	:						
	3h	+30					
	4h	1 +31					
Restriction	- 6						
	. // ((
	Status	Availability					
	Normal Mode On, Idle Mo						
Register 1	Normal Mode On, Idle Mo						
Availability	Partial Mode On, Idle Mo						
$n \cap M$	Partial Mode On, Idle Mo						
$V \subset M \cap M$	Sleep Ir						
11 -							
		Default Value					
	Status	DE00h (PWM_DUTY_OFFSET)					
Default	Power On Sequence	00h					
	S/W Reset	00h					
	H/W Reset	00h					
		**					

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PWMFRCTR: PWM Frequency Control for LEDPWM (E000h~E001h)

	Add		ddress		Parameter							
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
		R/W E0h	E000h	00h	-	-	-	-	-	-	-	PWMF
PWMFRCTR RA	R/W		E001h	00h	PWM	PWM	PWM	PWM	PWM	PWM	PWM	PWM
			LOUIII	0011	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0

NOTE: "-" Don't care

This command is used to control the PWM clock frequency for LEDPWM pins.

PWMF: select the internal frequency source Fosc for generating the PWM signals.

PWMF	Fosc
0	5 MHz
1	10 MHz

PWMDIV[7:0]: the PWM frequency for LEDPWM pin.

 $PWM Frequency = \frac{Fosc}{256 \times PWMDIV[7:0]}$

Description

			ווח	
	PWMF	= "0"	PWMF	= "1"
	PWMDIV[7:0]	PWM Frequency	PWMDIV[7:0]	PWM Frequency
	00h	Setting Disabled	00h	Setting Disabled
٢	01h	19.53 KHz	01h	39.06 KHz
	02h	9.77 KHz	02h	19.53 KHz
	03h	6.51 KHz	03h	13.02 KHz
			:	:
	FDh	77.20 Hz	FDh	154.40 Hz
	FEh	76.89 Hz	FEh	153.79 Hz
	FFb	76.59 Hz	FFh	153.19 Hz

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

	Default Value							
Status	E000h (PWMF)	E001h (PWMDIV)	E002h (PWMDIV_KBB)					
Power On Sequence	00h	01h	01h					
S/W Reset	00h	01h	01h					
H/W Reset	00h	01h	01h					

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FCBRTCB: Force Display Brightness for CABC (E100h~E101h)

		Add	ress	Parameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
FCBRTCB	R/W	E1h	E100h	00h	-	-	-	-	-	-	-	FORCE_ CABC_ PWM	
POBRICE	IX/VV		E101h		FORCE_ CABC_ DUTY7	FORCE_ CABC_ DUTY6	FORCE_ CABC_ DUTY5	FORCE_ CABC_ DUTY4	FORCE_ CABC_ DUTY3	FORCE_ CABC_ DUTY2	FORCE_ CABC_ DUTY1	FORCE_ CABC_ DUTY0	

NOTE: "-" Don't care	Э		
			BC display brightness regardless the display content. display brightness as the setting of FORCE_CABC_DUTY[7:0].
	Bit	Description	Value
	FORCE_C ABC_PW M	Force CABC PWM duty enable/disable	"0": Force CABC PWM duty disable. CABC PWM duty is decided by CABC algorithm. "1": Force CABC PWM duty enable. CABC PWM duty is set by FORCE_CABC_DUTY[7:0].
	FORCE_CABO	C_DUTY[7:0]: the setting	display brightness of CABC when FORCE_CABC_PWM="1".
Description	FORCE	_CABC_DUTY[7:0]	Display Brightness of CABC Off
		2h	2/256 3/256
		FDh	254/256 255/256
		FFh	1

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Restriction	-		
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle M Partial Mode On, Idle M Sleep	lode Off, Sleep Out lode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes Yes
	Status	E100h (FORCE_C	Default Value CABC_PWM) E101h (FORCE_CABC_DUTY)
Default	Power On Sequence	00h	FFh
	S/W Reset	00h	FFh
	H/W Reset	00h	F Fh



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BRTCBUI: Display Brightness Control for CABC UI-Mode (E200h~E203h)

		Add	ress		Parameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
			E200h	00h	_	_	_	_	_	_	CABC_UI _PWM01	_		
BRTCBUI	R/W	E2h	E201h	00h	_	_	_	_	_	_	CABC_UI _PWM11	CABC_UI _PWM10		
BRICBUI	IX/VV		E202h	00h	CABC_UI _PWM27	_	_	_	_	_	CABC_UI _PWM21	CABC_UI _PWM20		
			E203h	00h	_	_	_	_	_		CABC_UI _PWM31	_		

NOTE: "-" Don't care

This command is used to control the display brightness corresponding to different gamma algorithm in CABC UI-Mode.

The CABC UI-Mode is used to keep the good display quality and brightness, so the variance s of display brightness and estimated gamma curve are small. In other words, base on different image content, the CABC function will determine a better display brightness and estimated gamma curve in order to keep the approximated display brightness and quality.

Description

The display brightness can be calculated by below.

Display Brightness = CABC_UI_PWMn[7:0]+1

For example:

If CABC_UI_PWM0[7:0] is set to 0xF3, the display brightness for this setting will be

Display Brightness = $\frac{243+1}{256} \approx 95.3\%$

Restriction

Register
Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Ctatus	Default Value										
Status	E200h	E201h	E202h	E203h							
Power On Sequence	F3h	ECh	E7h	DFh							
S/W Reset	F3h	ECh	E7h	DFh							
H/W Reset	F3h	ECh	E7h	DFh							

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BRTCBSTL: Display Brightness Control for CABC Still-Mode (E300h~E309h)

		Add	ress				Pa	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			E300h	00h	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_
			200011		PWM07	PWM06	PWM05	PWM04	PWM03	PWM02	PWM01	PWM00
			E301h	00h	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_
			L30111	0011	PWM17	PWM16	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10
			Fanah	00h	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_
			E302h	0011	PWM27	PWM26	PWM25	PWM24	PWM23	PWM22	PWM21	PWM20
			E2026	00h	CABC_	CABC_	CABC_ CABC_ CABC_ CABC	CABC_	CABC_	CABC_		
			E303h	00h	PWM37	PWM36	PWM35	PWM34	PWM33	PWM32	PWM31	PWM30
			E0041	001-	CABC_	CABC_	CABC_	CABC_	_ CABC_ CABC_ CABC_ CA		CABC_	
BRTCBSTL	R/W	E3h	E304h	00h	PWM47	PWM46	PWM45	PWM44	PWM43	PWM42	PWM41	PWM40
BRICBSIL	K/VV	ESN	E0051	001-	CABC_	CABC_	CABC	CABC	CABC_	CABC_	CABC_	CABC_
			E305h	00h	PWM57	PWM56	PWM55	PWM54	PWM53	PWM52	PWM51	PWM50
			E0001	001-	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_
			E306h	00h	PWM67	PWM66	PWM65	PWM64	PWM63	PWM62	PWM61	PWM60
			E0071		CABC_	CABC	CABC_	CABC	CABC	CABC_	CABC_	CABC_
			E307h	00h	PWM77	PWM76	PWM75	PWM74	PWM73	PWM72	PWM71	PWM70
			-0.4	П	CABC_	CABC	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_
		35	E308h	00h	PWM87	PWM86	PWM85	PWM84	PWM83	PWM82	PWM81	PWM80
			Food	001-	CABC	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_	CABC_
			E309h	00h	PWM97		PWM95	PWM94	PWM93	PWM92	PWM91	PWM90

NOTE: "-" Don't care

This command is used to set the display brightness corresponding to different gamma algorithm in CABC Still-Mode.

Base on different image content, the CABC function will determine a better display brightness and estimated gamma curve in order to keep the approximated display brightness and quality.

The display brightness can be calculated by below.

Description

Display Brightness =
$$\frac{CABC - PWMn[7:0] + 1}{256}$$

For example:

If CABC_UI_PWM0[7:0] is set to 0x99, the display brightness for this setting will be

Display Brightness =
$$\frac{153+1}{256} \approx 60.2\%$$



Restriction	-
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes
	Default Value
	Status E300h E301h E302h E303h E304h E305h E306h E307h E308h E309h
Default	Power On Sequence F3h D9h CCh C0h B3h A6h 99h 99h 99h 95h
	S/W Reset F3h D9h CCh C0h B3h A6h 99h 99h 99h 95h
	H/W Reset F3h D9h CCh C0h B3h A6h 99h 99h 99h 95h



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BRTCBMOV: Display Brightness Control for CABC Moving-Mode (E400h~E409h)

		Add	ress				Pa	rameter																												
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0																								
			E400h	00h	CABC_ MOV_ PWM07	CABC_ MOV_ PWM06	CABC_ MOV_ PWM05	CABC_ MOV_ PWM04	CABC_ MOV_ PWM03	CABC_ MOV_ PWM02	CABC_ MOV_ PWM01	CABC_ MOV_ PWM00																								
			E401h	00h	CABC_ MOV_ PWM17	CABC_ MOV_ PWM16	CABC_ MOV_ PWM15	CABC_ MOV_ PWM14	CABC_ MOV_ PWM13	CABC_ MOV_ PWM12	CABC_ MOV_ PWM11	CABC_ MOV_ PWM10																								
			E402h	00h	CABC_ MOV_ PWM27	CABC_ MOV_ PWM26	CABC_ MOV_ PWM25	CABC_ MOV_ PWM24	CABC_ MOV_ PWM23	CABC_ MOV_ PWM22	CABC_ MOV_ PWM21	CABC_ MOV_ PWM20																								
			E403h	00h	CABC_ MOV_ PWM37	CABC_ MOV_ PWM36	CABC_ MOV_ PWM35	CABC_ MOV_ PWM34	CABC_ MOV_ PWM33	CABC_ MOV_ PWM32	CABC_ MOV_ PWM31	CABC_ MOV_ PWM30																								
BRTCBMOV	R/W	E4h	E404h	00h	CABC_ MOV_ PWM47	CABC_ MOV_ PWM46	CABC_ MOV_ PWM45	CABC_ MOV_ PWM44	CABC_ MOV_ PWM43	CABC_ MOV_ PWM42	CABC_ MOV_ PWM41	CABC_ MOV_ PWM40																								
BRICDINOV	K/VV	C4II	E405h	00h	CABC_ MOV_ PWM57	CABC_ MOV_ PWM56	CABC_ MOV_ PWM55	CABC_ MOV_ PWM54	CABC_ MOV_ PWM53	CABC MOV_ PWM52	CABC_ MOV_ PWM51	CABC_ MOV_ PWM50																								
																											E406h	00h	CABC_ MOV_ PWM67	CABC_ MOV_ PWM66	CABC_ MOV_ PWM65	CABC_ MOV_ PWM64	CABC_ MOV_ PWM63	CABC_ MOV_ PWM62	CABC_ MOV_ PWM61	CABC_ MOV_ PWM60
																											י מנו	an m		an n	IN (מוני שנו	מון יו מון יו			
		M	E408h	00h	CABC_ MOV_ PWM87	CABC_ MOV_ PWM86	CABC_ MOV_ PWM85	CABC_ MOV_ PWM84	CABC_ MOV_ PWM83	CABC_ MOV_ PWM82	CABC_ MOV_ PWM81	CABC_ MOV_ PWM80																								
			E409h	00h	CABC_ MOV_ PWM97	CABC_ MOV_ PWM96	CABC_ MOV_ PWM95	CABC_ MOV_ PWM94	CABC_ MOV_ PWM93	CABC_ MOV_ PWM92	CABC_ MOV_ PWM91	CABC_ MOV_ PWM90																								

NOTE: "-" Don't care

This command is used to set the display brightness corresponding to different gamma algorithm in CABC Moving-Mode.

Base on different image content, the CABC function will determine a better display brightness and estimated gamma curve in order to keep the approximated display brightness and quality.

The display brightness can be calculated by below.

Description

Display Brightness =
$$\frac{CABC_MOV_PWMn[7:0]+1}{256}$$

For example:

If CABC_UI_PWM0[7:0] is set to 0xB3, the display brightness for this setting will be

Display Brightness =
$$\frac{179+1}{256} \approx 70.3\%$$

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Restriction	-										
	St	atus						Availab	ilitv		
	Normal Mode On, Id	le Mode	Off, Sle	ep Out				Yes			
Register Availability	Normal Mode On, Id	le Mode	On, Sle				Yes				
	Partial Mode On, Idl	e Mode	Off, Sle	ep Out				Yes			
	Partial Mode On, Idl		Yes								
	Sle	ep In		Yes							
										n -	
									ne	V	
	Ctatus					Default	t Value	4	IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII		
	Status	E400h	E401h	E402h	E403h	E404h	E405h	E406h	E407h	E408h	E409h
Default	Power On Sequence	F3h	D9h	CCh	C0h	B3h	A6h	99h	99h	99h	95h
Delault	S/W Reset	F3h	D9h	CCh	C0h	B3h	A6h	99h	99h	99h	95h
	H/W Reset	F3h	D9h	CCh	C0h	B3h	A6h	99h	99h	99h	95h
				W		1	ns				



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AMOVCTR: Automatic Moving-Mode Detection Control (E500h~E501h)

		Add	ress				Pai	ameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
AMOVCTR R/W	R/W	R/W E5h	E500h	00h	-	MOV DET6	MOV DET5	MOV DET4	MOV DET3	MOV DET2	MOV DET1	MOV DET0
AMOVETR	K/VV	ESII	E501h	00h	-	-	-	MOV SC4	MOV SC3	MOV SC2	MOV SC1	MOV SC0

NOTE: "-" Don't care

This command is used to set the condition for automatic Moving-Mode selection for CABC.

The Moving-Mode means that the frame memory is continuously updated for displaying. The CABC function provides three CABC modes – UI-Mode, Still-Mode and Moving-Mode. This function is only available in Normal Display Mode (command NORON) with CABC mode is set to Still-Mode (C[1:0] of command 5500h is "10"). In other words, the "Moving-Mode Detection" function does not work when CABC has been set in UI-Mode (C[1:0] of command 5500h is "01") or Moving-Mode (C[1:0] of command 5500h is "11").

MOVDET[6:0]: the frame memory updated rate for Moving-Mode detection.

This setting is applied to set a period which the driver IC will monitor frame memory updating rate each specified period. This function is turned off when MOVDET[6:0] is set to "00h".

Description

MOVDET[6:0] //	Detection Condition							
0h	Moving-Mode detection disable							
1h	2 frames							
2h	3 frames							
3h	4 frames							
7Dh	126 frames							
7Eh	127 frames							
7Fh	128 frames							

For example:

If MOVDET[6:0] is set to 0x0A, this means the driver IC will check frame memory updated rate each 10-frame time period..

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MOVSC[4:0]: set the de-bounce times of frame memory updated each specified time. There is an internal counter to calculate how many time does frame memory has been updated each specified time period. If the frame memory has been updated (even only been updated one time) each specified time length, the internal counter will increase 1. Otherwise, if the frame memory has not been updated any time each specified time length, the internal counter will decrease 1. Finally, if the value of internal counter larger than the value of MOVSC[4:0], the CABC mode will be changed from "Still-Mode" to "Moving-Mode" automatically. If the value of internal counter equals to 0, the CABC mode will be changed from "Moving-Mode" to "Still-Mode". MOVSC[4:0] **De-bounce Times** 00h 1 time 01h 2 times 02h 3 times 03h 4 times 5 times 04h Description : 30 times 1Dh 1Eh 31 times 1Fh 32 times For example: If host 's frame memory updated rate is once per 10 frames, then set MOVDET[7:0] to 0x0A. And set MOVSC[4:0] as 0x06 for de-bounce 6 times to avoid the non-moving frame memory writing be detected. Whenever frame memory updated within each 10 frames, the internal counter will increase 1. Until the value of internal counter equal to 6 (MOVSC[4:0]), the CABC mode will be changed from "Still-Mode" to "Moving-Mode" automatically. However, if the frame memory updated rate is 1 stopped per 12 frames, this means the frame memory will be updated 0.83 time during 10 frames period (MOVDET[6:0]), the internal counter will decrease 1 every 20 frames. Until the value of internal counter equals to 0, the CABC mode will be changed from "Moving-Mode" to "Still-Mode". Only available in Normal Display Mode with CABC mode is set in "Still-Mode". Restriction Availability Status Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Register Partial Mode On, Idle Mode Off, Sleep Out Yes Availability Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes **Default Value** Status E500h (MOVDET) E501h (MOVSC) Default Power On Sequence 04h 00h S/W Reset 00h 04h H/W Reset 00h 04h

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FHYSTCTR: Final Hysteresis Result Control (E600h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
FHYSTCTR	R/W	E6h	E600h	00h	SET_ HYST	-	-	-	HYST_ OUT_ VAL3	HYST_ OUT_ VAL2	HYST_ OUT_ VAL1	HYST_ OUT_ VAL0

								VAL3	VAL2	VAL1	VALU
NOTE: "-" Don't car	e										
	This co	mmand is used	to control th	e final hy	steresis ı	esult for	LABC.				
		YST: select the	•		•		•		function	s enable	or not.
		OUT_VAL[3:0]:			is result v					HH	
Description	S	SET_HYST	HYST_ 0	_EN		Fin	al Hyster	- 11	ult		
		0					HYST V		<u> </u>	11	
			1		Internal hysteresis result HYST_OUT_VAL[3:0]						
		1	Х			<u>n II HY</u>	SILOUI	_VAL[3:	0]		
				_ ^		١١١/ ١					
Restriction	-				AII	U	ח -				
		. 1	((, 7			6	2// //				
	Status Availability										
	N	ormal Mode On	Out	1110	Yes Yes						
Register [N	ormal Mode On	, Idle Mode	Out							
Availability		artial Mode On,	Out								
$U \cap U \cap D$	P	artial Mode On,	Idle Mode (On, Sleep	Out Yes						
			Sleep In					Yes	i		
	2										
V											
	\	Status				De	efault Val	ue			
		Status			E600h	(SET_H	YST, HY	ST_OUT	Γ_VAL)		
Default	Р	ower On Seque	ence				00h				
		S/W Reset					00h				
		H/W Reset					00h				

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HYSTCTR: Internal Hsyteresis Function Control (E700h)

		Add	ress	Parameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
HYSTCTR	R/W	E7h	E700h	00h	HYST_ EN	-	-	1	HYST_ WR3	HYST_ WR2	HYST_ WR1	HYST_ WR0	

NO	TF.	"_"	Don't	care

This command is used to control the internal hysteresis function for LABC.

HYST_EN: enable/disable the internal hsyteresis function.

HYST_WR[3:0]: set the specified hysteresis result when HYST_EN="0".

Description

HYST_EN	Internal Hysteresis Function
0	Disable
1	Enable

The external host can set HYST_EN="0" to disable internal hysteresis function and do hysteresis by external host itself. Based on the read value of register FFSV[15:0], the external host can write its hysteresis result into HYST_WR[3:0] to specified the hysteresis result.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	E700h (HYST_EN, HYST_WR)
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

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FLTCTR: Median Filter and Flicker Filter Control (E800h)

		Add	ress				Pai	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
FLTCTR	R/W	E8h	E800h	00h	MRF_ BYS	-	-	-	FKP3	FKP2	FKP1	FKP0

NOTE: "-" Don't care

This command is used to control the internal Median Filter and internal Flicker Filter for LABC.

MRF_BYS: decide the value of register FSV[15:0] to pass or bypass the internal Median Filter.

MRF_BYS	Value of FSSV[15:0]				
0	FSV[15:0] proceeded by Median Filter				
1	1 Equal to FSV[15:0]				

Description

FKP[3:0]: the averaging time period for Flicker Filter.								
	FKP[3:0]	Averaging Time Period for Flicker Filter						
	0h	0.2 sec						
	1h	0.4 sec						
	2h	0.6 sec						
	: 1	: (0.2 sec/Step)						
	Dh	2.8 sec						
	Eh	3.0 sec						
	Fh	Reserved						

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Restriction	-					
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep I	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes			
	Status	Default Value E800h (MRF_BYS, FKP)				
Default	Power On Sequence		0.0h			
	S/W Reset	00h				
	H/W Reset	00h				



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WRALSV: Write Ambient Light Information (E900h~E902h)

		Add	ress				Pa	rameter							
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0			
	R/W	R/W	R/W	R/W		E900h	00h	LS7	LS6	LS5	LS4	LS3	LS2	LS1	LS0
WRALSV					R/W	R/W	R/W	R/W E9h	E901h	00h	LS15	LS14	LS13	LS12	LS11
	E902h	00h	-	-	-	-	-	-	-	ALS_W					

NO	TF.	"_"	Don't	care

This command is used to write the given ambient light information into LABC circuit.

LS[7:0]: the LSBs of ambient light information.

LS[15:0]: the MSBs of ambient light information.

ALS_W: send the ambient light information LS[15:0] into the internal circuit.

Description The step to write ambient light information LS[15:0]

Step 1: First, write the value into register LS[7:0] for updating the LSBs of LS[15:0].

Step 2: Second, write the value into register LS[15:8] for updating the MSBs of LS[15:0].

Step3: Finally, set the register bit ALS_W="1", then the value of LS[15:0] will be completely send into the internal circuit. The bit ALS_W becomes "0" after LS[15:0] is written completely.

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Restriction	-		
	Status	S	Availability
	Normal Mode On, Idle M	ode Off, Sleep Out	Yes
Register	Normal Mode On, Idle M	ode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mo	ode Off, Sleep Out	Yes
	Partial Mode On, Idle Mo	ode On, Sleep Out	Yes
	Sleep I	n	Yes
	Status		Default Value
	Clarac	E900h, E901	h (LS) E902h (ALS_W)
Default	Power On Sequence	0000h	00h
	S/W Reset	0000h	00h
	H/W Reset	0000h	00h

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RDBRTDPL: Read Display Brightness from LABC (EA00h)

		Add	ress				Pa	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBRTDPL	R	EAh	EA00h	00h	RDPWM _L7	RDPWM _L6	RDPWM _L5	RDPWM _L4	RDPWM _L3	RDPWM _L2	RDPWM _L1	RDPWM _L0

NOTE: "-" Don't care

This command is used to read the display brightness value which proceeded by LABC blocks.

RDPWM_L[7:0]: the display brightness value from LABC block.

RDPWM_L[7:0]	PWM Duty for Display from LABC
00h	Off
01h	2/256
02h	3/256
:	
FDh	254/256
FEh	255/256
FFh	

Description

The below table lists the relation between LABC output and DBV[7:0] (here means from WRDISBV command).

Register bit "A"	Register bit "DB"	RDPWM_L[7:0]
		DBV[7:0] (here means from WRDISBV command)
0	1	DBV[7:0] (here means from WRDISBV command)
1	(6)	DBV[7:0] (here means from WRDISBV command)
1		Display Brightness Value by LABC Modified

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Restriction	-					
	Status		Availability			
	Normal Mode On, Idle Mo	ode Off, Sleep Out	Yes			
Register	Normal Mode On, Idle Mo	ode On, Sleep Out	Yes			
Availability	Partial Mode On, Idle Mo	•	Yes			
	Partial Mode On, Idle Mo		Yes			
	Sleep Ir	1	Yes			
			7			
	21.1		Default Value			
	Status		EA00h (RDPWM_L)			
Default	Power On Sequence	OOH				
	S/W Reset	00h				
	H/W Reset	00h				
	6					
	ATEM					



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RDBRTDPC: Read Display Brightness from CABC (EB00h)

		Add	ress Parameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBRTDPL	R	EBh	EB00h	00h	RDPWM 7	RDPWM 6	RDPWM 5	RDPWM 4	RDPWM 3	RDPWM 2	RDPWM 1	RDPWM 0

NOTE: "-" Don't care

This command is used to read the display brightness value which proceeded by CABC blocks.

RDPWM[7:0]: the display brightness value from CABC block.

RDPWM[7:0]	PWM Duty for Display from CABC
00h	Off
01h	2/256
02h	3/256
:	
FDh	254/256
FEh	255/256
FFh	1

Description

The below table lists the relation between CABC output and RDPWM[7:0].

FORC	E_CABC_PWM="0"	FORCE	E_CABC_PWM="1"
CABC Mode	RDPWM[7:0]	CABC Mode	RDPWM[7:0]
Off-Mode	FFh	Off-Mode	FORCE_CABC_DUTY[7:0]
UI-Mode	Value by CABC Modified	UI-Mode	FORCE_CABC_DUTY[7:0]
Still-Mode	Value by CABC Modified	Still-Mode	FORCE_CABC_DUTY[7:0]
Moving-Mode	Value by CABC Modified	Moving-Mode	FORCE_CABC_DUTY[7:0]

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Restriction	-		_			
	Status		Availability			
	Normal Mode On, Idle Mod	de Off, Sleep Out	Yes			
Register	Normal Mode On, Idle Mod	de On, Sleep Out	Yes			
Availability	Partial Mode On, Idle Mod	le Off, Sleep Out	Yes			
	Partial Mode On, Idle Mod	le On, Sleep Out	Yes			
	Sleep In		Yes			
	01.1		Default Value			
	Status		EB00h (RDPWM)			
Default	Power On Sequence	FFH				
	S/W Reset	FFh				
	H/W Reset	FFR				
		<i>9</i> ~ ((
П						
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		500				
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NT35510

RDHYST: Read Hysteresis Result (ED00h)

		Address		Address Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDHYST	R	EDh	ED00h	00h	-	-	-	-	RD_HYS T_OUT3			RD_HYS T_OUT0

NOT	-⊏-	"	"	Don	14	care	
NOI	- :	-		เวดท	ľΤ	care	,

NOTE: "-" Don't car	re
Description	This command is used to read the hysteresis result from the output of internal hysteresis function block of LABC.
Restriction	- an M
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes
Default	Status Default Value ED00h (RD_HYST_OUT) Power On Sequence 00h S/W Reset 00h H/W Reset 00h

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RDGMA: Read Gamma Curve (EE00h)

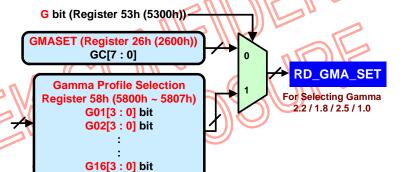
04h

08h

		Address		Address Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGMA	R	EEh	EE00h	uun	RD_GM A_SET7						RD_GM A_SET1	RD_GM A_SET0

NOTE: "-" Don't care

Description



Gamma Curve 3 (G=2.5)

Gamma Curve 4 (G=1.0)

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Status	EE01h (RD_GMA_SET)
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

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RDALSV: Read Ambient Light Information (EF00h~EF01h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDALSV	R	EFh	EF00h	00h	ALSV7	ALSV6	ALSV5	ALSV4	ALSV3	ALSV2	ALSV1	ALSV0
			EF01h	00h	ALSV15	ALSV14	ALSV13	ALSV12	ALSV11	ALSV10	ALSV9	ALSV8

	21 0 111 0 011 ALOV 15 ALOV 14 ALOV 15 ALOV 12 ALOV 11 ALOV 10 ALOV 6					
NOTE: "-" Don't care						
Description	This command is used to read the ambient light information which sent into LABC. ALSV[7:0]: the LSBs of ambient light information. ALSV[15:0]: the MSBs of ambient light information.					
Restriction						
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Default Value					
Default	Status EF00h, EF01 (ALSV) Power On Sequence 0000h SW Reset 0000h					
	HW Reset 0000h					





1.3 Manufacture Command Set for Page 1

Table 1.3.1 Manufacture Command Set - Page 1

			Ad	dress				Para	meter					
Instruction	ACT	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function
				B000h	00h	-	-	-		,	VBPA[4:0	0]		Set AVDD voltage
SETAVDD	Dir	R/W	B0h	B001h	00h					,	VBPB[4:0	0]		
				B002h	00h					,	VBPC[4:0	0]		
				B100h	00h	-	-	-		,	VBNA[4:0	0]		Set AVEE voltage
SETAVEE	Dir	R/W	B1h	B101h	00h	1	-	-		,	VBNB[4:0	0]		
				B102h	00h	1	-	-		,	VBNC[4:	0]		
				B200h	00h	-	-	-	-	-	-	VBCL	A[1:0]	Set VCL voltage
SETVCL	Dir	R/W	B2h	B201h	00h	-	-	-	-	-	-	VBCL	B[1:0]	~ //
				B202h	00h	-	-	-	-	-	-	VBCL	C[1:0]	
				B600h	00h	-		BTPA[2:0]	-		PCKA[2:0]	Set AVDD boosting times/frequency
BT1CTR	Dir	R/W	B6h	B601h	00h	-		BTPB[2:0]	-		PCKB[2:0	1	
				B602h	00h	-		3TPC[2:0]	-		PCKC[2:0		N N NU -
				B700h	00h	-		BTNA[2:0]	-		NCKA[2:0	1	Set AVEE boosting times/frequency
BT2CTR	Dir	R/W	B7h	B701h	00h	-		BTNB[2:0]	31		NCKB[2:0		
				B702h	00h	-	E	3TNC[2:0]	211		NCKC[2:0		
				B800h	00h	-	-	BTCL	A [1:0]	٠,١		CLCKA[2:	0]	Set VCL boosting times/frequency
BT3CTR	Dir	R/W	B8h	B801h	00h	-	-	BTCLI	B [1:0]			CLCKB[2:	0]	
				B802h	00h	-		BTCL	C [1:0]	Λ -	7	CLCKC[2:	0]	
				B900h	00h		- 11 <	BTHA	A[1:0]	U.		HCKA[2:0	1	Set VGH boosting times/frequency
BT4CTR	Dir	R/W	B9h	B901h	00h	[[-		BTH	B[1:0]	-		HCKB[2:0	1	
				B902h	00h	11	U/S	ВТНО	C[1:0]			HCKC[2:0]	3 -
				BA00h	00h		<i>)</i>]-	BTLA	A[1:0]			LCKA[2:0	<u>' ע</u>	Set VGLX boosting times/frequency
BT5CTR	Dir	R/W	BAh	BA01h	00h	-	-	BTLE	3[1:0]	<u> </u>		LCKB[2:0		
		1 G		BA02h	00h	-	-	BTLC		11-	<i>)</i> `	LCKC[2:0	1	
		W		BC00h	00h	- /		M .	VGMP		_	_	VGSP	Set VGMP/VGSP voltages
SETVGP	Dir	R/W	BCh			$-\Pi_{-}$		//	[8]				[8]	
n = n	11.11	$M \square$		BC01h	00h	HL				P[7:0]				
	- 11	A .	•	BC02h	00h	-11 11				P[7:0]		1		
	<i>)</i>			BD00h	00h	<u>)</u>) \	7	_	VGMN	_	_	_		Set VGMN/VGSN voltages
SETVGN	Dir	R/W	BDh	-11 11	- 11 - 11				[8]				[8]	
11-11-11			1//	BD01h	00h					N[7:0]				
				BD02h	00h		ı	1		N[7:0]		1		
			1	BE00h	00h	-	-	_	VCMOF	-	_	-	VCM[8]	Setting DC VCOM offset
SETVCMOFF	Dir	R/W	BEh					1	FSEL	1	İ	1	5[0]	1
				BE01h	00h				VCN	1[7:0]				

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Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

			Ad	dress				Para	meter					
Instruction	ACT	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function
				C500h	00h				ID41	[7:0]				Read ID4 for
RDIDIC	Dir	R	C5h	C501h	00h		1	1	ID42	[7:0]				Chip Code (ID41~42)
				C502h	00h	-	-	-	-		ID4	3[3:0]		Chip Version (ID43)
				C600h	00h	-	-			ID51	1[5:0]			Read ID5 for
				C601h	00h	-	-			ID52	2[5:0]			Lot ID(ID51~53)
				C602h	00h	-	-			ID53	3[5:0]			Wafer ID (ID54)
RDIDPRD	Dir	R	C6h	C603h	00h	-	-	-			ID54[4:0	1		Wafer Map (ID55~56)
				C604h	00h	-	-	-	-	-	-	ID55	[9:8]	
				C605h	00h				ID55	[7:0]				n
				C606h	00h	-	-	-	-		ID5	6[3:0]		
				C700h	00h				ID1[7:0]				Write display ID code
WRDID	Dir	R/W	C7h	C701h	00h				ID2[7:0]				(for User Command Set DA00h~DC00h)
				C702h	00h				ID3[7:0]			~ \	
				C800h	00h	Bkx	[1:0]	Bky[[1:0]	Wx	[1:0]	Wy	[1:0]	Write panel color characteristics
				C801h	00h				Bkx	9:2]			<u> </u>	(for User Command Set 7000h~7E00h)
				C802h	00h				Bky	711			_ //	V
				C803h	00h				Wx[\mathcal{A}	11 1/r	<u> </u>	
				C804h	00h				Wy[111	リレ		
				C805h	00h	Rx[1:0]	Ry[$\overline{}$	—	[1:0]	Gy[1:0]	
				C806h	00h			<i>7111.</i>	Rx[**		-		
WRPCLRC	Dir	R/W	C8h	C807h	00h		<u> </u>	-117	Ry[-		n '	11 11	211/2
				C808h	00h	H	_//_	י וע	Gx[-		-//-	11 11	
				C809h	00h	_//_)) >		Gy[Щ.		-11 /	
				C80Ah	00h	Bx[1:0]	By[<u> </u>		[1:0]	Ay[1:0]	
			5	C80Bh	00h				Bx[**	110	<u> </u>		
		n li		C80Ch	00h				By[-	<i>))</i> `			
	7	WW	7/	C80Dh	00h	-a (Ш—	Ax[$\overline{}$				
	HH	H		C80Eh	00h	-H		\mathcal{A}	Ay[-				
<i> </i>	11 /	NI I)	C900h	00h	HH			SID					Write DDB
WRDDB	Dir	R/W	C9h	C901h	00h	-11-7.			SID[(for User Command Set A1xxh, A8xxh)
MMG				C902h	00h	<u> </u>	U L		MID	•				4
				C903h	00h				MID[15:8]				



Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

			Ad	dress	-			Para	meter					
Instruction	ACT	R/W			D[15:8]	D7	De			Do	Da	D4	Do	Function
			MIPI	Others	(Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
				D100h	00h	-	-	-	-	-	-	V0R1	[9:8]	Set gamma 2.2 correction characteristic
				D101h	00h				V0R ²	1[7:0]				for positive "Red"
				D102h	00h	-	ı	-	-	-	-	V1R1	[9:8]	
				D103h	00h				V1R′	1[7:0]				
				D104h	00h	-	ı	-	-	-	-	V3R1	[9:8]	
				D105h	00h				V3R′	1[7:0]				
				D106h	00h	-	-	-	-	-	-	V5R1	[9:8]	
				D107h	00h				V5R′	1[7:0]				
				D108h	00h	-	-	-	-	-	-	V7R1	[9:8]	•
				D109h	00h				V7R′	1[7:0]				<i>⋒</i> //
				D10Ah	00h	-	-	-	-	-	-	V11R	1[9:8]	
				D10Bh	00h			•	V11R	1[7:0]				
				D10Ch	00h	-	-	-	-	-	-	V15R	1[9:8]	
				D10Dh	00h			•	V15R	1[7:0]			101	// // // // // // // // // // // // //
				D10Eh	00h	-	-	-	-	-		V23R	1[9:8]	41 0
				D10Fh	00h			1	V23R	1[7:0]			<u> </u>	V
				D110h	00h	-	-	-		2-11	<u> </u>	V31R	1[9:8]	
				D111h	00h		1	-	V31R	1[7:0]	111	リレ		
				D112h	00h	-		1		-		V47R	1[9:8]	
				D113h	00h			<i>71111.</i>	V47R					
				D114h	00h		<u> </u>	1-1-1	U	D.	-	V63R	1[9:8]	211/2
				D115h	00h	H	_//	<i></i> `	V63R	1[7:0]		-//-	<i>11 11</i>	
				D116h	00h	-//)) >		-		<u> </u>	V95R	1[9:8]	
				D117h	00h				V95R	1[7:0]	\sim	2)/6		
			9	D118h	00h	-	-		// -	// -	110	V127F	R1[9:8]	
GMRCTR1	Dir	R/W	D1h	D119h	00h			(C)	V127F	R1[7:0]	// 			1
	\mathcal{D}	\mathbb{N}	7/	D11Ah	00h	n (<u>~</u>	 - 	11,4,005		-	V128F	(1[9:8]	
a (C	// //	$I \cap I$		D11Bh	00h	- 11 /		-//-	V128F	(1[7:0]		1/4005	1410.01	1
< // // // /	111	$M \mid$	1	D11Ch	00h	11-11)) 	·		-	V160F	(1[9:8]	
1111/1/	<i>))</i>	V		D11Dh D11Eh	00h 00h	- 11 \			V160F	R1[7:0]	_	V192F	14[0.0]	
11/1/16				D11Fh	00h		-	-	1	R1[7:0]	-	V 192F	(1[9:8]	
$\parallel \parallel \sim \parallel$			10	D11711	00h	-	-		V 192F	-	_	V208F	18-011	
			- 11	D121h	00h				\/208E	R1[7:0]		V2001	(1[3.0]	1
			\	D121h	00h	_	_	_	-	-	_	V224F	18-0119	
				D123h	00h			1	V224F	R1[7:0]	1	V Z Z -11	(1[0.0]	
				D124h	00h	_	_	_	-	-	_	V232F	119:81	
				D125h	00h	J			V232F	R1[7:0]			[]	
				D126h	00h	-	-	-	-	-	-	V240F	R1[9:8]	
				D127h	00h		•		V240F	R1[7:0]			•	
				D128h	00h	-	-	-	-	-	-	V244F	R1[9:8]	
				D129h	00h		•	•	V244F	R1[7:0]				
				D12Ah	00h	-	-	-	-	-	-	V248F	R1[9:8]	
				D12Bh	00h				V248F	R1[7:0]				
				D12Ch	00h	•	-	-	-		-	V250F	R1[9:8]	
				D12Dh	00h				V250F	R1[7:0]				
				D12Eh	00h		-	-	-	-	-	V252F	R1[9:8]	
				D12Fh	00h				V252F	R1[7:0]		_		
				D130h	00h	-	-	-	-	-	-	V254F	R1[9:8]	
				D131h	00h			1	V254F	R1[7:0]	1	1		
				D132h	00h	-	-	-	-	-	-	V255F	R1[9:8]	
				D133h	00h				V255F	R1[7:0]				

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Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

			Ad	dress				Para	meter					
Instruction	ACT	R/W			D[15:8]	D7	De			Do	Da	D4	Do	Function
			MIPI	Others	(Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
				D200h	00h	-	-	-	-	-	-	V0G	1[9:8]	Set gamma 2.2 correction characteristic
				D201h	00h				V0G1	1[7:0]				for positive "Green"
				D202h	00h	-	-	-	-	-	-	V1G ²	1[9:8]	
				D203h	00h				V1G1	1[7:0]				
				D204h	00h	-	-	-	-	-	-	V3G ²	1[9:8]	
				D205h	00h				V3G1	1[7:0]				
				D206h	00h	-	-	-	-	-	-	V5G ²	1[9:8]	
				D207h	00h				V5G1	1[7:0]	1			
				D208h	00h	-	-	-	-	-	-	V7G ²	1[9:8]	n
				D209h	00h		1	1	V7G1		1			- M //
				D20Ah	00h	-	-	-	-	-	-	V11G	1[9:8]	
				D20Bh	00h		I	I	V11G	1[7:0]	1	1450	410.01	
				D20Ch	00h	-	-	-	-	4[7:0]	-	V15G	1[9:8]	
				D20Dh	00h	-	_	_	V15G	1[7:0]		Vaac	1[9:8]	
				D20Eh D20Fh	00h 00h	-	_	_		1[7:0]		V23G	1[9:6]	1/2 n
				D20FII	00h	_	_	l _	V23G	1[7.0]	// 	V31G	1[9:8]	
				D211h	00h				V31G	1[7:0]	111		1[5.0]	
				D211h	00h	_		17	11.1	-	W 1/-	V47G	1[9:8]	
				D213h	00h			111	V47G	117:01	0		.[0.0]	
				D214h	00h		P ((11/1/	177	0	-	V63G	1[9:8]	
				D215h	00 h7	((\mathcal{H}	۱ (ز	V63G	1[7:0]		. 11	11 17	
				D216h	00h	11	T-	9 .	-			V95G	1[9:8]	3
				D217h	00h				V95G	1[7:0]		2//	ノ)	
				D218h	00h	-	-		7 -	<u> </u>		V1270	31[9:8]	
GMGCTR1	Dir	R/W	D2h	D219h	00h				V1270	31[7:0]	<u> </u>			1
	1	\mathbb{N}	7/	D21Ah	00h	<u> </u>		 		_	-	V1280	31[9:8]	
4	IIII	M M		D21Bh	00h	- 11 		$-\mu$	V1280	31[7:0] I	1			-
<i>、</i>	11 7	$M \sqcup$	1	D21Ch	00h	//-//			-	-	-	V1600	61[9:8]	-
1111/20])	O		D21Dh	00h	-11-1/			V160G	31[7:0] 	T -	1/4000	24[0:0]	-
11/1/16				D21Eh D21Fh	00h 00h		-	-	V192G		1 -	V1920	1[9:8]	1
11 0			10	D21FII D220h	00h	-	_		V 1920	-	T -	V2080	18-011	1
				D221h	00h		l	l	V208G	31[7:0]	- II	12000	71[0.0]	1
				D222h	00h	_	_	_	-	-	_	V2240	18:81	1
				D223h	00h				V224G	31[7:0]	•			1
				D224h	00h	-	-	-	-	-	-	V2320	31[9:8]	
				D225h	00h				V2320	31[7:0]				
				D226h	00h	-	-	-	-	-	-	V2400	91[9:8]	
				D227h	00h		1	1	V2400	31[7:0]	1	1		
				D228h	00h	-	-	-	-	-	-	V2440	91[9:8]	1
				D229h	00h		1	1	V2440	31[7:0]	1	1		-
				D22Ah	00h	-	-	-	-	-	-	V2480	91[9:8]	-
				D22Bh	00h		1	1	V248G	31[7:0] I				-
				D22Ch	00h	-	-	-	-	-	-	V2500	61[9:8]	1
				D22Dh	00h				V250G	[7:0] اخ		1/0500	24[0.0]	1
				D22Eh	00h	-	-	-	- \/252G		-	V2520	61[9:8]	1
				D22Fh D230h	00h 00h	_	_	_	V2520	- [[/:0]	T -	\/2510	S1[9:8]	1
				D230fi D231h	00h	-	ı -	<u> </u>	V254G	31[7:0]	<u> </u>	v 2540	[0.6]	1
				D231h	00h	-	_	_	-	-	_	V2550	31[9:8]	1
				D233h	00h				V2550	G1[7:0]	•		[0]	1

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Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

			Ad	dress				Para	meter					
Instruction	ACT	R/W	MIPI	Others	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Function
			IVIII	Others	(Non-MIPI)	וט	Ъ	DJ	D4	DS	DZ	וט	DU	
				D300h	00h	-	-	-	-	-	-	V0B1	[9:8]	Set gamma 2.2 correction characteristic
				D301h	00h		1	1	V0B1	[7:0]	1	1		for positive "Blue"
				D302h	00h	-	-	-	-	-	-	V1B1	1[9:8]	
				D303h	00h				V1B1	[7:0]				
				D304h	00h	-	-	-	-	-	-	V3B1	1[9:8]	
				D305h	00h				V3B1	1[7:0]				
				D306h	00h	-	-	-	-	-	-	V5B1	1[9:8]	
				D307h	00h				V5B1	1[7:0]				
				D308h	00h	-	-	-	-	-	-	V7B1	1[9:8]	•
				D309h	00h				V7B1	[7:0]				<i>⋒</i> //
				D30Ah	00h	-	-	-	-	-	-	V11B	1[9:8]	
				D30Bh	00h				V11B	1[7:0]				
				D30Ch	00h	-	-	-	-	-	-	V15B	1[9:8]	
				D30Dh	00h				V15B	1[7:0]			197	// // //U
				D30Eh	00h	-	-	-	-	-		V23B	1[9:8]	Al n
				D30Fh	00h				V23B	1[7:0]			<u> </u>	
				D310h	00h	-	-	-		211	\\-	V31B	1[9:8]	
				D311h	00h				V31B	1[7:0]		リド		
				D312h	00h	-				-		V47B	1[9:8]	
				D313h	00h			$M_{ m L}$	V47B	1[7:0]	<u> </u>			
				D314h	00h		<u> </u>	1-1 \	\cup	U .	-	V63B	1[9:8]	215
				D315h	00 h /	11	_//		√ V63B	1[7:0]			11.17	
				D316h	00h	- //	Π^{\sim}		-		((- '	V95B	1[9:8]	•
				D317h	00h				V95B	1[7:0]		711	<u>' (ر</u>	
			5	D318h	00h	-	-		<u> </u>	<u> </u>	110	V127E	31[9:8]	
GMBCTR1	Dir	R/W	D3h	D319h	00h				V127E	31[7:0]	<u> </u>			_
	\cap	MM	7/	D31Ah	00h	- i		<u> </u>	_//		-	V128E	31[9:8]	1
		M M		D31Bh	00h	_ // /		$\mathcal{M}_{\mathcal{A}}$	V128E	31[7:0]	1			-
. // //	11 7	$M \sqcup$		D31Ch	00h	//-//	-		-	-	-	V160E	31[9:8]	-
IIII/A))	O		D31Dh	00h	-11-7			V160E		1	ı		-
11/1/16				D31Eh	00h	<i>- (</i> (- د	-	-	-	-	V192E	31[9:8]	
$\parallel \cup$				D31Fh	00h		ı	1	V192E	31[7:0] 	ı			
D			- ///	D320h	00h	-	-	-	-	-	-	V208E	31[9:8]	-
			\	D321h	00h		ı		V208E	31[7:0]		1/00/15		-
				D322h	00h	-	-	-			-	V224E	31[9:8]	-
				D323h D324h	00h	-	1	_	V224E	1[7:0]		V232E	110.01	1
					00h	-	_	-	L	21[7:0]	-	V232E	1[9:8]	1
				D325h D326h	00h 00h	-		Ι.	V232E	1[7:0]	_	V240E	110.01	1
				D326H	00h		_		V240E	21[7:0]		V240E	01[9.0]	1
				D32711	00h	-		Ι.	V240E	1[7.0]		V244E	21[0.9]	1
				D328h	00h	-	_	-	V244E	21[7:0]	-	V244E	1[9:8]	1
				D329H	00h	-	_	_	V Z 44E	-	_	1/2/195	21[0.9]	1
				D32An	00h	-	_	_	V248E		_	V248E	01[9.0]	1
				D32Ch	00h	-	l <u>.</u>	_	V Z 4 O L	J _	_	V250E	21[0-8]	1
				D32Dh	00h				V250E	31[7:0]		V 2.30L	, i[a.o]	1
				D32Eh	00h	-	_	_	-	-	_	V252F	31[9:8]	1
				D32Fh	00h			1	V252E		•		[0]	1
				D330h	00h	-	-	-	-	-	-	V254E	31[9:8]	1
				D331h	00h			•	V254E	31[7:0]	•		,	1
				D332h	00h	-	-	-	-	-	-	V255E	31[9:8]	1
				D333h	00h		-	•	V255E	31[7:0]	•			1

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Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

			Ad	dress				Para	meter					
Instruction	ACT	R/W			D[15:8]	D-7					-	D4	-	Function
			MIPI	Others	(Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
				D400h	00h	-	-	-	-	-	-	V0R2	2[9:8]	Set gamma 2.2 correction characteristic
				D401h	00h			•	V0R2	2[7:0]	•			for negative "Red"
				D402h	00h	-	-	-	-	-	-	V1R2	2[9:8]	1
				D403h	00h				V1R2	2[7:0]				
				D404h	00h	-	-	-	-	-	-	V3R2	2[9:8]	
				D405h	00h				V3R2	2[7:0]				
				D406h	00h	-	-	-	-	-	-	V5R2	2[9:8]	
				D407h	00h				V5R2	2[7:0]]
				D408h	00h	-	-	-	-	-	-	V7R2	2[9:8]	
				D409h	00h		1	ı	V7R2	2[7:0]	1	1		-
				D40Ah	00h	-	-	-	-	-	-	V11R	2[9:8]	- N IN II
				D40Bh	00h		1		V11R	2[7:0]	1	1		
				D40Ch	00h	-	-	-	-	-	-	V15R	2[9:8]	11 11 11 11
				D40Dh	00h			1	V15R	2[7:0]	1		191	W // //p
				D40Eh	00h	-	-	-	-	-		V23R	2[9:8]	41 11
				D40Fh	00h			1	V23R	2[7:0]			_ //	
				D410h	00h	-	-	-		2-\\	11-	V31R	2[9:8]	4
				D411h	00h	 _			V31R	2[7:0]		リレ		
				D412h	00h	-		41	- 	-		V47R	2[9:8]	
				D413h	00h			<i>71111.</i>	100	2[7:0]		· ·		0) (
				D414h	00h		<u> </u>	-11/	U	-	<u> </u>	V63R	2[9:8]	
				D415h	00h	Щ.		' (ر	V63R	2[7:0]		}	$\frac{1111}{11}$	
				D416h	00h	+)) 	_	-		46	V95R	2[9:8]	<u>}</u>
				D417h	00h				V95R		$\mathcal{H} =$			4
			9	D418h	00h	-	-		-	-	\mathscr{S}^{H}	V127F	(2[9:8]	-
GMRCTR2	Dir	R/W	D4h	D419h	00h	-		(V127F	(2[/:0]	<i>/</i> .	\/4005	2010-01	-
	\mathcal{L}	\mathbb{N}	7/	D41Ah D41Bh	00h	\sim	\sim	// -	V128F	-	-	V128F	R2[9:8]	4
a (C	U = U	$\langle \parallel \parallel \parallel$		D41Bh D41Ch	00h 00h	\ 		-tt	V 120F	2[7:0]		V160F	10.010	1
<i>\ \\\\\</i>	<i>\\\</i>	A	1	D41Dh	00h	11-11)	V160F		1 -	V 1001	(2[9.0]	1
JIII/II	J			D41Eh	00h	- 11 V		-	V 1001	.2[7.0]	T _	V/192F	R2[9:8]	1
11/41 0			~	D41Fh	00h				V192F	22[7:0]		V 1321	(2[3.0]	1
11 0			10	D420h	00h	-	_	_	-	-	-	V208F	R2[9:8]	1
			- \\	D421h	00h				V208F	2[7:0]	1		_[0.0]	1
				D422h	00h	-	-	_	-	-	-	V224F	R2[9:8]	1
				D423h	00h			•	V224F	R2[7:0]	•			1
				D424h	00h	-	-	-	-	-	-	V232F	R2[9:8]	1
				D425h	00h				V232F	R2[7:0]]
				D426h	00h	-	-	-	-	-	-	V240F	R2[9:8]	
				D427h	00h				V240F	R2[7:0]				
				D428h	00h	-	-	-	-	-	-	V244F	R2[9:8]]
				D429h	00h				V244F	R2[7:0]]
				D42Ah	00h	-	-	-	-	-	-	V248F	R2[9:8]	<u> </u>
				D42Bh	00h		1		V248F	R2[7:0]		1		_
				D42Ch	00h	-	-	-	-	-	-	V250F	R2[9:8]	1
				D42Dh	00h		1		V250F	R2[7:0]	1			4
				D42Eh	00h	-	-	-	-	-	-	V252F	R2[9:8]	4
				D42Fh	00h	<u> </u>	l		V252F		1	l		4
				D430h	00h	-	-	-	-	-	-	V254F	R2[9:8]	4
				D431h	00h		l		V254F	R2[7:0]	1	l		4
				D432h	00h	-	-	-	-	-	<u> </u>	V255F	R2[9:8]	4
				D433h	00h	L			V255F	R2[7:0]				

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Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

			Ad	dress				Para	meter					
Instruction	ACT	R/W	MIPI		D[15:8]	D7	De		D4	Da	D2	D1	D0	Function
			WIIPI	Others	(Non-MIPI)	יט	D6	D5	D4	D3	DZ	וט	D0	
				D500h	00h	-	-	-	-	-	-	V0G	2[9:8]	Set gamma 2.2 correction characteristic
				D501h	00h				V0G2	2[7:0]				for negative "Green"
				D502h	00h	-	-	-	-	-	-	V1G	2[9:8]	
				D503h	00h				V1G2	2[7:0]				
				D504h	00h	-	-	-	-	-	-	V3G	2[9:8]	_
				D505h	00h				V3G2	2[7:0]		•		
				D506h	00h	-	-	-	-	-	-	V5G	2[9:8]	
				D507h	00h				V5G2	2[7:0]		1		
				D508h	00h	-	-	-	-	-	-	V7G	2[9:8]	n
				D509h	00h		ı	ı	V7G2	2[7:0]	1	1		- M
				D50Ah	00h	-	-	-	-	-	-	V11G	32[9:8]	
				D50Bh	00h		ı	1	V11G	2[7:0]	1			
				D50Ch	00h	-	-	-	-		-	V15G	32[9:8]	1 11 1111 22
				D50Dh	00h		_	_	V15G	2[7:0]		1/220	G2[9:8]	
				D50Eh D50Fh	00h 00h	-			\/23G	2[7:0]		V23G	2[9.6]	61 n
				D50FII	00h	-	_	I _	V23G	2[7.0]	\\ . \	V31G	52[9:8]	
				D510H	00h	_			V31G	2[7:0]	111	Voice	2[3.0]	1 4
				D511h	00h	_	-	1.7	l li	-10-41		V47G	32[9:8]	
				D512h	00h			HF	V47G	217:01	11	V+11C	,2[0.0]	
				D514h	00h		5 ((1.11	1	<u> </u>	-	V63G	2[9:8]	
				D515h	00h7	((\mathcal{H}		V63G	2[7:0]		. 11	11 11	
				D516h	00h	- //	Π	9	-			V95G	62[9:8]	772
				D517h	00h		IJ		V95G	2[7:0]		2/1/	J)	1
				D518h	00h	-	-		Λ-		M_{∞}	V1270	G2[9:8]	
GMGCTR2	Dir	R/W	D5h	D519h	00h				V1270	2[7:0]	<i>)</i>]			_
			7/	D51Ah	00h	- i 1		<u> </u>	_//		-	V1280	G2[9:8]	
	III	M M		D51Bh	00h	-11.1			V1280	2[7:0]				4
. // ((11 7	$M \sqcup$		D51Ch	00h	//-//	-		-	-	-	V1600	G2[9:8]	4
IIIIII))	0		D51Dh	00h	-11-1/			V160G	32[7:0]	1			-
11/41/6			~	D51Eh D51Fh	00h 00h		-	-	- \/4000	-	-	V1920	G2[9:8]	-
\parallel \sim			19	D51FII	00h		_	_	V1920	-	I -	V/2080	G2[9:8]	1
			- \\\	D521h	00h				V208G	2[7:0]	1	V2000	J2[J.U]	1
			\	D522h	00h	_	_	_	-	-	_	V2240	G2[9:8]	1
				D523h	00h		ı		V2240	32[7:0]	1		[]	1
				D524h	00h	-	-	-	-	-	-	V2320	G2[9:8]	1
				D525h	00h				V2320	32[7:0]				
				D526h	00h	-	-	-	-	-	-	V2400	G2[9:8]	
				D527h	00h				V2400	32[7:0]				_
				D528h	00h	-	-	-	-	-	-	V2440	G2[9:8]	
				D529h	00h		1		V2440	2[7:0]		Ti .		4
				D52Ah	00h	-	-	-	-	-	-	V2480	G2[9:8]	4
				D52Bh	00h		ı	ı	V2480		ı			
				D52Ch	00h	-	-	-	-	-	-	V2500	G2[9:8]	-
				D52Dh	00h				V250G	2[7:0]		1/0501	2010-01	-
				D52Eh	00h	-	-	-	1/2520		-	v2520	G2[9:8]	1
				D52Fh D530h	00h 00h	_	_	_	V252G	.∠[1.U] -	_	V/25/1	G2[9:8]	1
				D530H	00h				V254G	- 32[7:01		v 204(عدرت.0]	1
				D531h	00h	-	-	_	-	-[r.o]	_	V2550	G2[9:8]	1
				D533h	00h		L	L	V2550	32[7:0]			[0.0]	1

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Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

Natruction ACT R/W MIPI Others D[15:8] (Non-MIPI) D7 D6 D5 D4 D3 D2 D1 D0 Function	eristic
D600h	eristic
D601h	eristic
D602h	
D603h	
D604h	
D605h	
D606h	
D607h	
D608h 00h - - - - V7B2[9:8] D609h 00h V7B2[7:0] V11B2[9:8] D60Ah 00h - - - V11B2[7:0] D60Bh 00h - - - - V15B2[9:8]	
D609h 00h V7B2[7:0] D60Ah 00h - - - - V11B2[9:8] D60Bh 00h V11B2[7:0] - V15B2[9:8]	
D60Ah 00h - - - - - V11B2[9:8] D60Bh 00h V11B2[7:0] V15B2[9:8]	
D60Bh	
D60Ch 00h V15B2[9:8]	
	2
D60Eh 00h - - - - V23B2[9:8]	
D60Fh 00h V23B2[7:0]	
D610h 00h V31B2[9:8]	
D611h 00h V31B2[7:0]	
D612h 00h V47B2[9:8]	
D613h 00h V47B2[7:0] D614h 00h V63B2[9:8]	
D615h 00h V63B2[7:0] D616h 00h V95B2[9:8]	
30.00	
D617h 00h V95B2[7:0]	
CMPCTP3 Dir BAW Deb D619h 00h V127B2[9:8]	
GMBCTR2 Dir R/W D6h D61Ah 00h V128B2[9:8]	
D61Bh 00h V128B2[7:0]	
D61Ch 00h V160B2[9:8]	
D61Dh 00h V160B2[7:0]	
D61Eh 00h V192B2[9:8]	
D61Fh 00h V192B2[7:0]	
0620h 00h V208B2[9:8]	
D621h 00h V208B2[7:0]	
D622h 00h V224B2[9:8]	
D623h 00h V224B2[7:0]	
D624h 00h - - - - V232B2[9:8]	
D625h 00h V232B2[7:0]	
D626h 00h - - - - V240B2[9:8]	
D627h 00h V240B2[7:0]	
D628h O0h - - - - V244B2[9:8]	
D629h 00h V244B2[7:0]	
D62Ah 00h - - - - V248B2[9:8]	
D62Bh 00h V248B2[7:0]	
D62Ch 00h V250B2[9:8]	
D62Dh	
30211 0011	
D62Fh	
D630H 00H V254B2[9.6] D631h 00h V254B2[7:0]	
D632h	
D633h 00h V255B2[7:0]	

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Table 1.3.1 Manufacture Command Set – Page 1 (Continued)

				dress				Para	meter							
Instruction	ACT	R/W	МІРІ	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	Function		
MTPDET	Dir	R	ECh	EC00h	00h	-	-	-	-	-	-	-	MTP_D ET	MTP power detection		
MTPEN	Dir	R/W	EDh	ED00h	00h				MTP_E	N1[7:0]				MTP enable		
				EE00h	00h	1	0	1	0	0	1	0	1	MTP write		
MTPWR	Dir	W	EEh	EE01h	00h	0	1	0	1	1	0	1	0			
				EE02h	00h	0	0	1	1	1	1	0	0			
RDMTP	Dir	R	EFh	EF00h	00h				MTP_ST	US1[7:0]				Read MTP status		
KDWIF	DII	K	EFII	EF01h	00h				MTP_ST	US2[7:0]						

NOTE:

 The following description is indicates the executing time of instruction 	tions.	instructi	of	time	executina	the	indicates	is	ption	descri	vina	follov	. The	1.
--	--------	-----------	----	------	-----------	-----	-----------	----	-------	--------	------	--------	-------	----

No.	Symbol	Executing Time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame
3	DHS (Display Horizontal Sync.)	Synchronized with the next line



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SETAVDD: Setting AVDD Voltage (B000h~B002h)

		Add	ress				Pa	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			B000h	00h	-	-	1	VBPA4	VBPA3	VBPA2	VBPA1	VBPA0
SETAVDD	R/W	B0h	B001h	00h	-	-	1	VBPB4	VBPB3	VBPB2	VBPB1	VBPB0
			B002h	00h	-	-	-	VBPC4	VBPC3	VBPC2	VBPC1	VBPC0

NOTE: "-" Don't care

This command is used to control the AVDD voltage in different display mode.

VBPA[4:0]: the step-up circuit 1 output voltage AVDD in normal / idle off mode.

VBPB[4:0]: the step-up circuit 1 output voltage AVDD in idle on mode.

VBPC[4:0]: the step-up circuit 1 output voltage AVDD in partial / idle off mode.

Description

VBPA[4:0], VBPB[4:0], VBPC[4:0]	AVDD Voltage
00h	6.5V
01h	6.4V
0 2h	6.3∀
	. (0.1 V/Step)
05h	6.0V
	: (0.1V/Step)
12h	4.7V
135	4.6V
14h	4.5V
15h~1Fh	reserved

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

	Default Value						
Status	B000h (VBPA) B001h (VBPB)		B002h (VBPC)				
Power On Sequence	05h	05h	05h				
S/W Reset	05h	05h	05h				
H/W Reset	05h	05h	05h				

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SETAVEE: Setting AVEE Voltage (B100h~B102h)

	Address			Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
		B100h	00h	-	-	-	VBNA4	VBNA3	VBNA2	VBNA1	VBNA0	
SETAVEE	R/W	B1h	B101h	00h	-	-	-	VBNB4	VBNB3	VBNB2	VBNB1	VBNB0
			B102h	00h	-	-	-	VBNC4	VBNC3	VBNC2	VBNC1	VBNC0

NOTE: "-" Don't care

This command is used to control the AVEE voltage in different display mode.

VBNA[4:0]: the step-up circuit 2 output voltage AVEE in normal / idle off mode.

VBNB[4:0]: the step-up circuit 2 output voltage AVEE in idle on mode,

VBNC[4:0]: the step-up circuit 2 output voltage AVEE in partial / idle off mode.

Description

VBNA[4:0], VBNB[4:0], VBNC[4:0]	AVEE Voltage
00h	-6.5V
01h	-6.4V
02h	-6.3V
	: (0.1V/Step)
05h	-6.0V
	: (0.1V/Step)
12h	-4.7V
135	-4.6V
14h	-4.5V
15h~1Fh	reserved

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Default Value						
B100h (VBNA)	B101h (VBNB)	B102h (VBNC)				
05h	05h	05h				
05h	05h	05h				
05h	05h	05h				
	05h 05h	B100h (VBNA) B101h (VBNB) 05h 05h 05h 05h				

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SETVCL: Setting VCL Voltage (B200h~B202h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
		B200h	00h	1	-	-	-	-	1	VBCLA 1	VBCLA 0	
SETVCL	R/W	B2h	B201h	00h	-	-	-	-	-	-	VBCLB 1	VBCLB 0
			B202h	00h		-	-	-	-		VBCLC 1	VBCLC 0

NOTE: "-" Don't care

This command is used to control the VCL voltage in different display mode.

VBCLA[1:0]: the step-up circuit 3 output voltage VCL in normal / idle off mode.

VBCLB[1:0]: the step-up circuit 3 output voltage VCL in idle on mode.

Description

VBCLC[1:0]: the step-up circuit 3 output voltage VCL in partial / idle off mode.

VBCLA[1:0], VBCLB[1:0], VBCLC[1:0]	VCL Voltage
00	-2.5V
V _{Q1}	-3.0V
10	-3.5V
11	-4.0V

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

	Default Value							
Status	B200h (VBCLA)	B201h (VBCLB)	B202h (VBCLC)					
Power On Sequence	00h	00h	00h					
S/W Reset	00h	00h	00h					
H/W Reset	00h	00h	00h					

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NT35510

BT1CTR: BT1 Power Control for AVDD (B600h~B602h)

	Address				Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
	B600h	00h	-	BTPA2	BTPA1	BTPA0	•	PCKA2	PCKA1	PCKA0			
BT1CTR	R/W	B6h	B601h	00h	-	BTPB2	BTPB1	BTPB0	•	PCKB2	PCKB1	PCKB0	
			B602h	00h	-	BTPC2	BTPC1	BTPC0	-	PCKC2	PCKC1	PCKC0	

NOTE: "-" Don't care

This command is used to control the boosting times and booster clock frequency of step-up circuit 1 (AVDD) in different display mode.

BTPA[2:0]: the boosting times for step-up circuit 1 in normal / idle off mode.

PCKA[2:0]: the booster clock frequency for step-up circuit 1 in normal / idle off mode.

BTPB[2:0]: the boosting times for step-up circuit 1 in idle on mode.

PCKB[2:0]: the booster clock frequency for step-up circuit 1 in idle on mode..

BTPC[2:0]: the boosting times for step-up circuit 2 in partial / idle off mode.

PCKC[2:0]: the booster clock frequency for step-up circuit 1 in partial / idle off mode.

Description

BTPA[2:0] BTPB[2:0] BTPC[2:0]	Boosting Times	РСКА[2:0] РСКВ[2:0] РСКС[2:0]	Clock Frequency (Synchronized to Hsync)		
0h	Disable	Oh Oh	Hsync / 32		
1h	1.5 x VDDB	1h	Hsync / 16		
2h	1.66 x VDDB	2h	Hsync / 8		
3h	2.0 x VDDB	3h	Hsync / 4		
4h	2.5 x VDDB	4h	Hsync / 2		
5h	3.0 x VDDB	5h	Hsync		
6h	reserved	6h	2 x Hsync		
7h	reserved	7h	4 x Hsync		

Note: When BTPA/B/C[2:0]="000", the boosting times is controlled by internal circuit automatically which according to the AVDD setting voltage (by command B0xxh of page 1) and VDDB input voltage.

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NT35510

Restriction	-					
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep I	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes			
		I				
5 ()	Status	B600h (BTPA, PCKA)	Default Value B601h (BTPB, PCKB)	B602h (BTPC, PCKC)		
Default	Power On Sequence	04h	04h	04h		
	S/W Reset	04h	04h	04 h		
	H/W Reset	04h	04h	04h		
		211 11/1/20				



NT35510

BT2CTR: BT2 Power Control for AVEE (B700h~B702h)

		Add	ress	Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT2CTR	R/W B7h	/W B7h	B700h	00h	-	BTNA2	BTNA1	BTNA0	•	NCKA2	NCKA1	NCKA0
			B701h	00h	-	BTNB2	BTNB1	BTNB0	•	NCKB2	NCKB1	NCKB0
			B702h	00h	-	BTNC2	BTNC1	BTNC0	-	NCKC2	NCKC1	NCKC0

NOTE: "-" Don't care

This command is used to control the boosting times and booster clock frequency of step-up circuit 2 (AVEE) in different display mode.

BTNA[2:0]: the boosting times for step-up circuit 2 in normal / idle off mode.

NCKA[2:0]: the booster clock frequency for step-up circuit 2 in normal / idle off mode.

BTNB[2:0]: the boosting times for step-up circuit 2 in idle on mode.

NCKB[2:0]: the booster clock frequency for step-up circuit 2 in idle on mode...

BTNC[2:0]: the boosting times for step-up circuit 2 in partial / idle off mode.

NCKC[2:0]: the booster clock frequency for step-up circuit 2 in partial / idle off mode.

Description

BTNA[2:0] BTNB[2:0] BTNC[2:0]	Boosting Times	NCKA[2:0] NCKB[2:0] NCKC[2:0]	Clock Frequency (Synchronized to Hsync)
Oh	Disable	Oh	Hsync / 32
1h	-1.5-x VDDB	1h	Hsync / 16
2h	-2.0 x VDDB	2h	Hsync / 8
3h	-2.5 x VDDB	3h	Hsync / 4
4h	-3.0 x VDDB	4h	Hsync / 2
5h	reserved	5h	Hsync
6h	reserved	6h	2 x Hsync
7h	reserved	7h	4 x Hsync

Note: When BTNA/B/C[2:0]="000", the boosting times is controlled by internal circuit automatically which according to the AVEE setting voltage (by B1xxh of page 1) and VDDB input voltage.

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NT35510

Restriction	-				
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep I	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availat Yes Yes Yes Yes	5 5 5	
	Status	B700h (BTNA, NCKA)	Default Value B701h (BTNB, NCKB)	B702h (BTNC, NCKC)	
Default	Power On Sequence	04h	04h 04h	04h 04h	
	S/W Reset H/W Reset	04h 04h	04h	04h	



NT35510

BT3CTR: BT3 Power Control for VCL (B800h~B802h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT3CTR	-		B800h	00h	1	-	BTCLA 1	BTCLA 0	-	CLCKA 2	CLCKA 1	CLCKA 0
		B801h	00h	-	1	BTCLB 1	BTCLB 0	-	CLCKB 2	CLCKB 1	CLCKB 0	
			B802h	00h		-	BTCLC 1	BTCLC 0		CLCKC 2	CLCKC 1	CLCKC 0

NOTE: "-" Don't care

This command is used to control the boosting times and booster clock frequency of step-up circuit 3 (VCL) in different display mode.

BTCLA[1:0]: the boosting times for step-up circuit 3 in normal / idle off mode.

CLCKA[2:0]: the booster clock frequency for step-up circuit 3 in normal / idle off mode.

BTCLB[1:0]: the boosting times for step-up circuit 3 in idle on mode.

CLCKB[2:0]: the booster clock frequency for step-up circuit 3 in idle on mode.

BTCLC[1:0]: the boosting times for step-up circuit 3 in partial / idle off mode.

CLCKC[2:0]: the booster clock frequency for step-up circuit 3 in partial / idle off mode.

Description

BTCLA[1:0] BTCLB[1:0] BTCLC[10]	Boosting Times	CLCKA[2:0] CLCKB[2:0] CLCKC[2:0]	Clock Frequency (Synchronized to Hsync)
Oh-	Disable	0h	Hsync / 32
16 \\	-0.5 x VDDB	1h	Hsync / 16
2h	-1.0 x VDDB	2h	Hsync / 8
3h	-2.0 x VDDB	3h	Hsync / 4
11 2		4h	Hsync / 2
		5h	Hsync
		6h	2 x Hsync
		7h	4 x Hsync

Note: When BTCLA/B/C[2:0]="00", the boosting times is controlled by internal circuit automatically which according to the VCL setting voltage (by B2xxh of page 1) and VDDB input voltage.

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NT35510

Restriction	-					
Register Availability	Status Normal Mode On, Idle Mode Normal Mode On, Idle Mode Partial Mode On, Idle Mode Partial Mode On, Idle Mode Sleep In	On, Sleep Out Off, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes Yes			
Default	Status (B800h BTCLA, CLCKA)	Default Value B801h (BTCLB, CLCKB)	B802h (BTCLC, CLCKC)		
Default	Power On Sequence S/W Reset H/W Reset	04h 04h 04h	04h 04h 04h	04h 04h 04h		
		(1)11/210				



NT35510

BT4CTR: BT4 Power Control for VGH (B900h~B902h)

		Add	ress	Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT4CTR			B900h	00h	-	-	BTHA1	BTHA0	-	HCKA2	HCKA1	HCKA0
	R/W	W B9h	B901h	00h	-	-	BTHB1	BTHB0	-	HCKB2	HCKB1	HCKB0
			B902h	00h	-	-	BTHC1	BTHC0	-	HCKC2	HCKC1	HCKC0

NOTE: "-" Don't care

This command is used to control the boosting times and booster clock frequency of step-up circuit 4 (VGH) in different display mode.

BTHA[1:0]: the boosting times for step-up circuit 4 in normal / idle off mode.

HCKA[2:0]: the booster clock frequency for step-up circuit 4 in normal / idle off mode.

BTHB[1:0]: the boosting times for step-up circuit 4 in idle on mode.

HCKB[2:0]: the booster clock frequency for step-up circuit 4 in idle on mode...

BTHC[1:0]: the boosting times for step-up circuit 4 in partial / idle off mode.

HCKC[2:0]: the booster clock frequency for step-up circuit 4 in partial / idle off mode.

Description

	BTHA[1:0] BTHB[1:0] BTHC[10]	Boosting Times	HCKA[2:0] HCKB[2:0] HCKC[2:0]	Clock Frequency (Synchronized to Hsync)		
	Oh	AVDD+VDDB	Oh	Hsync / 32		
	1h	2xAVDD	1h	Hsync / 16		
۱	2h	AVDD-AVEE+VDDB	2h	Hsync / 8		
ľ	3h	2xAVDD-AVEE	3h	Hsync / 4		
			4h	Hsync / 2		
	The output of AVEE	will be VCL voltage level	5h	Hsync		
	when BT2 is inactive		6h	2 x Hsync		
	V		7h	4 x Hsync		

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NT35510

Restriction	-				
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep I	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes		
	Status	B900h (BTHA, HCKA)	Default Value B901h (BTHB, HCKB)	B902h (BTHC, HCKC)	
Default	Power On Sequence	14h	14h	14h	
	S/W Reset	14h	14h	14h	
	H/W Reset	14h	14h	14h	
	1	211 111 an			



NT35510

BT5CTR: BT5 Power Control for VGLX (BA00h~BA02h)

Inst / Para		Address		Parameter								
	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
BT56CTR			BA00h	00h	-	-	BTLA1	BTLA0	-	LCKA2	LCKA1	LCKA0
	R/W	W BAh	BA01h	00h	-	-	BTLB1	BTLB0	-	LCKB2	LCKB1	LCKB0
			BA02h	00h	-	-	BTLC1	BTLC0	-	LCKC2	LCKC1	LCKC0

NOTE: "-" Don't care

This command is used to control the boosting times and booster clock frequency of step-up circuit 5 (VGLX) in different display mode.

BTLA[1:0]: the boosting times for step-up circuit 5 in normal / idle off mode.

LCKA[2:0]: the booster clock frequency for step-up circuit 5 in normal / idle off mode.

BTLB[1:0]: the boosting times for step-up circuit 5 in idle on mode.

LCKB[2:0]: the booster clock frequency for step-up circuit 5 in idle on mode...

BTLC[1:0]: the boosting times for step-up circuit 5 in partial / idle off mode.

LCKC[2:0]: the booster clock frequency for step-up circuit 5 in partial / idle off mode.

Description

	BTLA[1;0] BTLB[1:0] BTLC[10]	Boosting Times	LCKA[2:0] LCKB[2:0] LCKC[2:0]	Clock Frequency (Synchronized to Hsync)
	Oh	AVEE+VCL	Oh	Hsync / 32
	1h	AVEE-AVDD	1h	Hsync / 16
١	2h	AVEE+VCL-AVDD	2h	Hsync / 8
ľ	3h	2xAVEE-AVDD	3h	Hsync / 4
			4h	Hsync / 2
	The output of AVEE	will be VCL voltage level	5h	Hsync
	when BT2 is inactive		6h	2 x Hsync
	V		7h	4 x Hsync

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NT35510

Restriction	-					
Register Availability	Status Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle M Partial Mode On, Idle M Sleep I	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes			
			Default Value			
D ()	Status	BA00h (BTLA, LCKA)	BA01h (BTLB, LCKB)	BA02h (BTLC, LCKC)		
Default	Power On Sequence	14h	14h	14h		
	S/W Reset	14h	14h	14h		
	H/W Reset	14h	14h	14h		
		211 11/1/20				



NT35510

SETVGP: Setting VGMP and VGSP Voltage (BC00h~BC02h)

		Add	ress	Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			BC00h	00h	-	-	-	VGMP8	-	-	-	VGSP8
SETVGP	R/W	BCh	BC01h	00h	VGMP7	VGMP6	VGMP5	VGMP4		VGMP1	VGMP0	
			BC02h	00h	VGSP7	VGSP6	VGSP5	VGSP4	VGSP3	VGSP2	VGSP1	VGSP0

NOTE: "-" Don't care

This command is used to set the regulator output voltage VGMP/VGSP for positive gamma divider.

VGMP1[7:0]: the high voltage for positive gamma divider. VGSP[7:0]: the low voltage for positive gamma divider.

Description

V	Gor [7.0]. the low voltage	e ioi positive garriria divid	ICI.	
	VGMP[8:0]	VGMP Voltage	VGSP[8:0]	VGSP Voltage
	000h	3.0000V	00h	0V (GND)
	001h	3.0125V	01h	0.30000V
	002h	3.0250V	02h	0.30125V
	:	: (12.5mV/Step)		
	C8h	5.5000V		: (12.5mV/Step)
	:	: (12.5mV/Step)		
	106h	6.2750V	10Eh	3.6750V
	107h	6.2875V	10Fh	3.6875V
	108h	6.3000V	110h	3.7000V
	109h~1FFh	reserved	111h~1FFh	reserved
.		. // 311 11 2		

Restriction -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Ctatus	Default Value							
Status	BC00h	BC01h (VGMP)	BC02h (VGSP)					
Power On Sequence	00h	C8h	00h					
S/W Reset	00h	C8h	00h					
H/W Reset	00h	C8h	00h					

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SETVGN: Setting VGMN and VGSN Voltage (BD00h~BD02h)

		Add	ress		Parameter							
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			BD00h	00h	-	-	-	VGMN8	-	-	-	VGSN8
SETVGP	R/W E	BDh	BD01h	00h	VGMN7	VGMN6	VGMN5	VGMN4	VGMN3	VGMN2	VGMN1	VGMN0
			BD02h	00h	VGSN7	VGSN6	VGSN5	VGSN4	VGSN3	VGSN2	VGSN1	VGSN0

NOTE: "-" Don't care

This command is used to set the regulator output voltage VGMP/VGSP for negative gamma divider.

VGMN[7:0]: the high voltage for negative gamma divider.

VGSN[7:0]: the low voltage for negative gamma divider.

Description

VGSN[7.0]. the low voltage	e ioi negative ganina divi	der.	
VGMN[8:0]	VGMN Voltage	VGSN[8:0]	VGSN Voltage
000h	-3.0000V	00h	0V (GND)
001h	-3.0125V	01h	-0.30000V
002h	-3.0250V	02h	-0.30125V
:	: (12.5mV/Step)	03h	-0.30250V
C8h	-5.5000V		: (12.5mV/Step)
:	: (12.5mV/Step)		
106h	-6.2750V	10Eh	-3.6750V
107h	-6.2875V	10Fh	-3.6875V
108h	-6.3000V	110h	-3.7000V
109h~1EFh	reserved	111h~1FFh	reserved

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Ctatus	Default Value							
Status	BD00h	BD01h (VGMN)	BD02h (VGSN)					
Power On Sequence	00h	C8h	00h					
S/W Reset	00h	C8h	00h					
H/W Reset	00h	C8h	00h					

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NT35510

SETVCMOFF: Setting VCOM Offset Voltage (BE00h~BE01h)

		Add	ress	Parameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
SETVCMOFF	R/W	BEh	BE00h	00h	-	-	-	VCMOF FSEL	-	•		VCM8	
			BE01h	00h	VCM7	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	

NOTE: "-" Don't care

This command is used to adjust the DC VCOM offset voltage for panel.

VCMOFFSEL: select the voltage common voltage offset mode.

VCMOFFSEL	Common Voltage Offset Mode
0	VCOM voltage offset mode
1	Gamma voltage offset mode

VCM[8:0]: the common voltage offset for panel.

v Civi[6.0]. trie cor	ninon voltage onset for pari	el.
	VCMOFFSEL="0"	VCMOFFSEL="1"
VCM[8:0]	VCOM Output Voltage	Internal Register Offset for Gamma Voltage (VGMP[8:0], VGSP[8:0], VGMN[8:0], VGSN[8:0])
000h	0V	0
001h	-0.0125V	
002h	-0.0250V	2
	: (12.5mV/Step)	
09Fh	-1.9875V	159
0A0h	-2.0000V	160
0A1h	-2.0125V	161
	: (12.5mV/Step)	: (1/Step)
0 C 7h	-2,48 7 5V	199
0C8h	-2.5000V	200
0C9h	-2.5125V	201
11: 0	: (12.5mV/Step)	: (1/Step)
0EFh	-2.9875V	239
0F0h	-3.0000V	240
0F1h	-3.0125V	241
:	: (12.5mV/Step)	: (1/Step)
117h	-3.4875V	279
118h	-3.5000V	280
119h~1FFh	reserved	reserved

Notes:

1. When VCOM voltage offset mode is selected:

The larger adjusted VCOM offset range the larger power consumption. The most negative VCOM voltage is clamped at VCL+0.5V. Select the proper adjusted VCOM range (by setting VCL voltage) according to panel characteristics to avoid unnecessary power consumption.

2. When Gamma voltage offset mode is selected:

The VCOM voltage will be fixed at 0V (GND). The larger AVDD (for more positive VGMP) and is necessary for gamma voltage offset.

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Restriction	-		
Register Availability	Status Normal Mode On, Idle Mode Of Normal Mode On, Idle Mode Of Partial Mode On, Idle Mode Of Partial Mode On, Idle Mode Or Sleep In	n, Sleep Out f, Sleep Out	Availability Yes Yes Yes Yes Yes Yes Yes Yes
Default	Status Power On Sequence S/W Reset H/W Reset	BE00h 00h 00h	Default Value BE01h (VCM) 00h 00h 00h

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RDIDIC: Read ID for IC Vender Code (C500h~C502h)

Inst / Para R/W		Address		Parameter								
	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDIDIC		R D5h	D500h	00h	ID417	ID416	ID415	ID414	ID413	ID412	ID411	ID410
	R		D501h	00h	ID427	ID426	ID425	ID424	ID423	ID422	ID421	ID420
			D502h	00h	-	-	1	-	ID433	ID432	ID431	ID430

NOTE: "-" Don't car	9										
	This command returns the internal ID code.										
Description	1 st and 2 nd parameters: Chip ID code. "5510h" means NT35510 3 rd parameter: ID43-ID40: Chip version code.										
Restriction											
	Status Availability										
	Normal Mode On, Idle Mode Off, Sleep Out Yes										
Register	Normal Mode On, Idle Mode On, Sleep Out Yes										
Availability	Partial Mode On, Idle Mode Off, Sleep Out Yes										
	Partial Mode On, Idle Mode On, Sleep Out										
	Sleep In Yes										
1											
20	Default Value										
	Status D500h (ID41) D501h (ID42) D502h (ID43)										
Default	Power On Sequence 55h 10h XXh										
	SW Reset 55h 10h XXh										
11 ~	HW Reset 55h 10h XXh										



NT35510

RDIDPRD: Read ID for IC Production Code (C600h~C605h)

		Add	ress	Parameter									
Inst / Para R	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
			C600h	00h	-	-	ID515	ID514	ID513	ID512	ID511	ID510	
			C601h	00h	-	-	ID525	ID524	ID523	ID522	ID521	ID520	
			C602h	00h	-	-	ID535	ID534	ID533	ID532	ID531	ID530	
RDIDIC	R	C6h	C603h	00h	-	-	-	ID544	ID543	ID542	ID541	ID540	
			C604h	00h	-	-	-	-	-	-	ID559	ID558	
			C605h	00h	ID557	ID556	ID555	ID554	ID553	ID552	ID551	ID550	
			C606h	00h	-	-	-	-	ID563	ID562	ID561	ID560	

NOTE: "-" Don't care

NOTE: "-" Don't car	е										
Description	4 th parameter: Wafer ID code 5 th and 6 th parameters: Wafer	his command returns the internal ID code. st to 3 rd parameters: IC Lot No. ID code (0~9, A~Z for each register). th parameter: Wafer ID code (0~25d). th and 6 th parameters: Wafer Map ID code (X-axis coordinate). th parameter: Wafer Map ID code (Y-axis coordinate).									
Restriction	- a ((~ (())	11 2		111123						
Register Availability	Normal Mode On, Idle M Normal Mode On, Idle M Partial Mode On, Idle M Partial Mode On, Idle M Sleep	lode Off, Slee lode On, Slee ode Off, Slee ode On, Slee	ep Out		Availab Yes Yes Yes Yes	6 6 6					
	0			Default	t Value						
Default	Status	C600h (ID51)	C601h (ID52)	C602h (ID53)	C603h (ID54)	C604h C605h (ID55)	C606h (ID56)				
	Power On Sequence	XXh	XXh	XXh	XXh	XXh	XXh				
	S/W Reset	XXh	XXh	XXh	XXh	XXh	XXh				
	H/W Reset	XXh	XXh	XXh	XXh	XXh	XXh				

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WRDID: Write Display ID (C700h~C702h)

Inst / Para R/W		Address		Parameter									
	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRDID R/W		R/W C7h C7	C700h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
	R/W		C701h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
			C702h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: "-" Don't care

This command is used to define the 24-bit display identification information.

The 1st parameter (ID1): module's manufacturer ID.

Description The 2nd parameter (ID27 to ID20): module/driver version ID (Parameter Range: 80h to FFh, i.e. the ID27 is always set to "1").

The 3rd parameter (ID37 to ID30): module/driver ID.

Note: The parameter ID1, ID2, ID3 correspond to read data of commands RDID1/2/3(DAh, DBh, DCh) respectively.

Restriction -

Register Availability

Status		Availability
Normal Mode On, Idle Mode	Off, Sleep Out	Yes
Normal Mode On, Idle Mode	On, Sleep Out	Yes
Partial Mode On, Idle Mode	Off, Sleep Out	Yes
Partial Mode On, Idle Mode	On, Sleep Out	Yes
Sleep In		Yes

Default

Status	Default Value							
Status	C700h (ID1)	C701h (ID2)	C702h (ID3)					
Power On Sequence	00h	80h	00h					
S/W Reset	00h	80h	00h					
H/W Reset	00h	80h	00h					
	·	<u> </u>						

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NT35510

WRPCLRC: Write Panel Color Characteristics (C800h~C80Eh)

		Add	ress				Pai	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			C800h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0
			C801h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2
			C802h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2
			C803h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2
			C804h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2
			C805h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0
			C806h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2
WRPCLRC	R/W	C8h	C807h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2
			C808h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2
			C809h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2
			C80Ah	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0
			C80Bh	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2
			C80Ch	00h	By9	By8	By7	By6	By5	By4	Ву3	By2
			C80Dh	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2
			C80Eh	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ау3	Ay2

NOTE: "-" Don't care

This command is used to define the panel color characteristics for black, white, red, green, blue and A The Bkx[9:0] and Bky[9:0]: black color characteristics. The Wx[9:0] and Wy[9:0]: white color characteristics. The Rx[9:0] and Ry[9:0]: red color characteristics. Description The Gx[9:0] and Gy[9:0]: green color characteristics. The Bx[9:0] and By[9:0]: blue color characteristics. The Ax[9:0] and Ay[9:0]: A color characteristics. Note: The parameters Bkx, Bky, Wx, Wy, Rx, Ry, Gx, Gy, Bx, By, Ax, Ay correspond to read data of commands 70h to 7Eh respectively. Restriction Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Register Normal Mode On, Idle Mode On, Sleep Out Yes Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes **Default Value** Status Power On Sequence All are 00h Default S/W Reset All are 00h H/W Reset All are 00h

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NT35510

WRDDB: Write DDB (C900h~C903h)

	Inst / Para R/W	Address		Parameter								
Inst / Para		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
		DAM COL	C900h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
WRDDB	R/W		C901h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
WRDDB R/W	C9h	C902h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
			C903h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8

		C903H 00F	I WIID IS WIID IT	MIDI3 MIDI2 MIDI1	MID 10 MID9 MID8							
NOTE: "-" Don't car	е											
Description	This command is used to define the supplier identification, display module identification and revision identification. Note: The parameters SID and MID correspond to read data of command RDDDBS (A1h) or command RDDDBC (A8h) respectively.											
Restriction	-											
Register Availability		Status Normal Mode On, Idle Mo Normal Mode On, Idle Mo Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In	ode Off, Sleep Out ode On, Sleep Out ode Off, Sleep Out ode On, Sleep Out	Availal Yes Yes Yes Yes	S S S							
Default	7	Status Power On Sequence	C900h, C901h (SID) 0000h	Default Value C902h, C903h (MID) 0000h	C900h, C901h (RID) 0000h							
V		S/W Reset H/W Reset	0000h 0000h	0000h 0000h	0000h 0000h							

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NT35510

GMRCTR1: Setting Gamma 2.2 Correction for Red (Positive) (D100h~D133h)

		Addı	ress		Parameter							
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			D100h	00h	-	-	-	-	-	-	V0R19	V0R18
			D101h	00h	V0R17	V0R16	V0R15	V0R14	V0R13	V0R12	V0R11	V0R10
			D102h	00h	-	-	-	-	-	-	V1R19	V1R18
			D103h	00h	V1R17	V1R16	V1R15	V1R14	V1R13	V1R12	V1R11	V1R10
			D104h	00h	-	-	-	-	-	-	V3R19	V3R18
			D105h	00h	V3R17	V3R16	V3R15	V3R14	V3R13	V3R12	V3R11	V3R10
			D106h	00h	-	-	-	-	-	7	V5R19	V5R18
			D107h	00h	V5R17	V5R16	V5R15	V5R14	V5R13	V5R12	V5R11	V5R10
			D108h	00h	-	-	-	-25		-	V7R19	V7R18
			D109h	00h	V7R17	V7R16	V7R15	V7R14	V7R13	V7R12	V7R11	V7R10
			D10Ah	00h	-	-			11-13	-	V11R19	V11R18
			D10Bh	00h	V11R17	V11R16	V11R15	V11R14	V11R13	V11R12	V11R11	V11R10
			D10Ch	00h	1-		1117	<i>-</i>	- 5		V15R19	V15R18
			D10Dh	00h	V15R17	V15R16	V15R15	V15R14	V15R13	V15R12	V15R11	V15R10
			D10Eh	00h)) \'	Ž,	-	<u> </u>			V23R19	V23R18
		Dth	D10Fh	00h 🎵	V23R17	V23R16	V23R15	V23R14	V23R13	V23R12	V23R11	V23R10
			D110h	00h	-	· - ((1110		-	-	V31R19	V31R18
1			D111h	00h	V31R17	V31R16	V31R15	V31R14	V31R13	V31R12	V31R11	V31R10
P_{∞}			D112h	00h	<u> </u>	'صالم	<u>)</u>	-	-	-	V47R19	V47R18
GMRCTR1	R/W		D113h	00h	V47R17	V47R16	V47R15	V47R14	V47R13	V47R12	V47R11	
N (()) //			D114h	00h	J)	-	-	-	-	-	V63R19	V63R18
			D115h	00h	V63R17	V63R16	V63R15	V63R14	V63R13	V63R12	V63R11	
11 2			D116h	00h	-	-	-	-	-	-	V95R19	V95R18
			D117h	00h	V95R17	V95R16	V95R15	V95R14	V95R13	V95R12	V95R11	
			D118h	00h	-	-	-	-	-	-	V127 R19	V127 R18
			D119h	00h	V127 R17	V127 R16	V127 R15	V127 R14	V127 R13	V127 R12	V127 R11	V127 R10
			D11Ah	00h	-	-	-	-	-	-	V128 R19	V128 R18
			D11Bh	00h	V128 R17	V128 R16	V128 R15	V128 R14	V128 R13	V128 R12	V128 R11	V128 R10
					N17	KIO	KIO	N14	N13	NIZ	V160	V160
			D11Ch	00h	-	-	-	-	-	-	R19	R18
			DAADI	001	V160							
			D11Dh	00h	R17	R16	R15	R14	R13	R12	R11	R10
			D11Eh	00h	-	-	-	-	-	-	V192	V192
					V192	V192	V192	V192	V192	V192	R19 V192	R18 V192
			D11Fh	00h	R17	R16	R15	R14	R13	R12	R11	R10

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		Addı	ress		Parameter							
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			D120h	00h	-	-	-	-	-	-	V208 R19	V208 R18
			D121h	00h	V208 R17	V208 R16	V208 R15	V208 R14	V208 R13	V208 R12	V208 R11	V208 R10
			D122h	00h	-	-	-	-	-	-	V224	V224
			D123h	00h	V224	V224	V224	V224	V224	V224	R19 V224	R18 V224
					R17	R16	R15	R14	R13	R12	R11 V232	R10 V232
			D124h	00h	-	-	-		1,000	-\\	R19	R18
			D125h	00h	V232 R17	V232 R16	V232 R15	V232 R14	V232 R13	V232 R12	V232 R11	V232 R10
		D ₁ h	D126h	00h	-	n	<u>\\-</u> \\))\ <u>\</u>	ار م	<u> </u>	V240 R19	V240 R18
			D127h	00h	V240	V240	V240	V240	V240	V240	V240	V240
			D128h	00h	R17\\	R16	R15	R14	R13	R12	R11 V244	R10 V244
			DIZOII	VOII)	-	26		נו (-	R19	R18
			D129h	00h	V244 R17	V244 R16	V244 R15	V244 R14	V244 R13	V244 R12	V244 R11	V244 R10
GMRCTR1	R/W		D12Ah	ooh C			-	-	-	-	V248	V248
M(U)						1/0/10	1/0/10	1 (0 (0	1/0.40	1/0/10	R19	R18
			D12Bh	00h	V248 R17	V248 R16	V248 R15	V248 R14	V248 R13	V248 R12	V248 R11	V248 R10
11 2			D12Ch	00h	-	-	-	-	-	-	V250 R19	V250 R18
			D12Dh	00h	V250	V250	V250	V250	V250	V250	V250	V250
			D12Eh	00h	R17	R16	R15	R14	R13	R12	R11 V252	R10 V252
			DIZLII	0011	-	-	-	-	-	-	R19	R18
			D12Fh	00h	V252 R17	V252 R16	V252 R15	V252 R14	V252 R13	V252 R12	V252 R11	V252 R10
			D130h	00h	-	-	-	-	-	-	V254 R19	V254 R18
			D131h	00h	V254	V254	V254	V254	V254	V254	V254	V254
					R17	R16	R15	R14	R13	R12	R11 V255	R10 V255
			D132h	00h	-	-	-	-	-	-	R19	R18
			D133h	00h	V255 R17	V255 R16	V255 R15	V255 R14	V255 R13	V255 R12	V255 R11	V255 R10

NOTE: "-" Don't care

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NT35510

	This command is used to adju	st the gamma 2.2 corre	ection for the red (posit	ive).			
Description		-					
	VnR1[9:0]: gamma voltage Vn	for gamma 2.2 correc	tion of red data (positiv	e).			
Restriction	-						
	2			9.1.99			
	Status			nilability			
	Normal Mode On, Idle M	·		Yes			
Register	Normal Mode On, Idle M	·		Yes			
Availability	Partial Mode On, Idle M	•		Yes			
	Partial Mode On, Idle Mo			Yes Yes			
	Зіеер і	III		Tes .			
				11 11 110			
	Status	<u> </u>					
		11/04/	00h, D101h (V0R1)	005 275			
			001, 01010 (V0R1) 02h, D103h (V1R1)	00h, 37h 00h, 61h			
	an (* // \\\\ \\\\	04h, D105h (V3R1)	00h, 92h			
			06h, D107h (V5R1)	00h, B4h			
			08h, D109h (V7R1)	00h, CEh			
	SEPTEM IN		Ah, D10Bh (V11R1)	00h, F6h			
_ 1			Ch, D10Dh (V15R1)	01h, 14h			
			Eh, D10Fh (V23R1)	01h, 48h			
M = M + M		D11	0h, D111h (V31R1)	01h, 6Bh			
	Power On Sequence	D11	2h, D113h (V47R1)	01h, A7h			
		D11	4h, D115h (V63R1)	01h, D3h			
U		D11	6h, D117h (V95R1)	02h, 18h			
		D118	3h, D119h (V127R1)	02h, 50h			
Default	Tower On Sequence	D11/	h, D11Bh (V128R1)	02h, 52h			
		D110	Ch, D11Dh (V160R1)	02h, 87h			
		D11E	h, D11Fh (V192R1)	02h, BEh			
		D120)h, D121h (V208R1)	02h, E2h			
		D122	2h, D123h (V224R1)	03h, 0Fh			
			lh, D125h (V232R1)	03h, 30h			
			Sh, D127h (V240R1)	03h, 5Ch			
			3h, D129h (V244R1)	03h, 77h			
			h, D12Bh (V248R1)	03h, 94h			
			Ch, D12Dh (V250R1)	03h, 9Fh			
			Eh, D12Fh (V252R1)	03h, ACh			
			0h, D131h (V254R1)	03h, BAh			
		D132	2h, D133h (V255R1)	03h, C1h			
	S/W Reset		Same above				
	H/W Reset		Same above				
		-	-				

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NT35510

GMGCTR1: Setting Gamma 2.2 Correction for Green (Positive) (D200h~D233h)

		Add	ress		Parameter							
Inst / Para	R/W			D[15:8]	5-	D.o.	5-	5.4	D 0	D.o.	D .4	D 0
		MIPI	Others	(Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			D200h	00h	-	-	-	-	-	-	V0G19	V0G18
			D201h	00h	V0G17	V0G16	V0G15	V0G14	V0G13	V0G12	V0G11	V0G10
			D202h	00h	-	-	-	-	-	-	V1G19	V1G18
			D203h	00h	V1G17	V1G16	V1G15	V1G14	V1G13	V1G12	V1G11	V1G10
			D204h	00h	-	-	-	-	-	-	V3G19	V3G18
			D205h	00h	V3G17	V3G16	V3G15	V3G14	V3G13	V3G12	V3G11	V3G10
			D206h	00h	-	-	-	-	-	1	V5G19	V5G18
			D207h	00h	V5G17	V5G16	V5G15	V5G14	V5G13	V5G12	V5G11	V5G10
			D208h	00h	-	-	-	-15		- \\	V7G19	V7G18
			D209h	00h	V7G17	V7G16	V7G15	V7G14	V7G13	V7G12	V7G11	V7G10
			D20Ah	00h	-	-			$U \cdot U$	-	V11G19	V11G18
			D20Bh	00h	V11G17	V11G16	V11G15	V11G14	V11G13	V11G12	V11G11	V11G10
			D20Ch	00h	a-		1117	<i>J</i> -	-5		V15G19	V15G18
			D20Dh	00h	V15G17	V15G16	V15G15	V15G14	V15G13	V15G12	V15G11	V15G10
			D20Eh	0 0h)) \	5	-	<u> </u>				V23G18
	R/W	D2h	D20Fh	00h	V23G17	V23G16	V23G15	V23G14	V23G13	V23G12	V23G11	V23G10
			D210h	00h	- ,	- ((11		-	-	V31G19	V31G18
1			D211h	00h	V31G17	V31G16	V31G15	V31G14	V31G13	V31G12	V31G11	V31G10
\mathbb{Z}_{∞}			D212h	00h	<u> </u>	نصتلاه).	-	-	-	V47G19	V47G18
GMGCTR1			D213h	00h	V47G17	V47G16	V47G15	V47G14	V47G13			
N (()) M			D214h	00h	<u> </u>	-	-	-	-		V63G19	
			D215h	00h		V63G16	V63G15	V63G14	V63G13	V63G12		
11 0			D216h	00h	-	-	-	-	-	-		V95G18
			D217h	00h	V95G17	V95G16	V95G15	V95G14	V95G13	V95G12		
			D218h	00h	-	-	-	-	-	-	V127 G19	V127 G18
			DO4.01-	004	V127							
			D219h	00h	G17	G16	G15	G14	G13	G12	G11	G10
			D21Ah	00h	-	-	-	-	-	-	V128	V128
					1/400	1/400	1/400	1/400	1/400	1/400	G19	G18
			D21Bh	00h	V128 G17	V128 G16	V128 G15	V128 G14	V128 G13	V128 G12	V128	V128 G10
					G17	010	GIS	G14	<u> </u>	GIZ	G11 V160	V160
			D21Ch	00h	-	-	-	-	-	-	G19	G18
			D0/5:	25:	V160							
			D21Dh	00h	G17	G16	G15	G14	G13	G12	G11	G10
			D24Ek	00h							V192	V192
			D21Eh	00h	-	-	-	-	-	-	G19	G18
			D21Fh	00h	V192							
			J2 11 11	5511	G17	G16	G15	G14	G13	G12	G11	G10

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		Address		Parameter										
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
			D220h	00h	-	-	-	-	-	-	V208 G19	V208 G18		
			D221h	00h	V208 G17	V208 G16	V208 G15	V208 G14	V208 G13	V208 G12	V208 G11	V208 G10		
			D222h	00h	1	-	1	-	1	-	V224 G19	V224 G18		
			D223h	00h	V224 G17	V224 G16	V224 G15	V224 G14	V224 G13	V224 G12	V224 G11	V224 G10		
			D224h	00h	-	-	-	-			V232 G19	V232 G18		
			D225h	00h	V232 G17	V232 G16	V232 G 15	V232 G14	V232 G13	V232 G12	V232 G11	V232 G10		
		D2h	D226h	00h	. <				שב	<u></u>	V240 G19	V240 G18		
			D227h	00h	V240 G17	V240 G16	V240 G15	V240 G14	V240 G13	V240 G12	V240 G11	V240 G10		
			D228h	00h		-	26			-	V244 G19	V244 G18		
	R/W		D229h	00h	V244 G17	V244 G16	V244 G15	V244 G14	V244 G13	V244 G12	V244 G11	V244 G10		
GMGCTR1			711		D22Ah	00h			-	-	-	-	V248 G19	V248 G18
				D22Bh	00h	V248 G17	V248 G16	V248 G15	V248 G14	V248 G13	V248 G12	V248 G11	V248 G10	
11 2			D22Ch	00h	-	-	-	-	-	-	V250 G19	V250 G18		
			D22Dh	00h	V250 G17	V250 G16	V250 G15	V250 G14	V250 G13	V250 G12	V250 G11	V250 G10		
			D22Eh	00h	-	-	-	-	-	-	V252 G19	V252 G18		
			D22Fh	00h	V252 G17	V252 G16	V252 G15	V252 G14	V252 G13	V252 G12	V252 G11	V252 G10		
			D230h	00h	-	-	-	-	-	-	V254 G19	V254 G18		
			D231h	00h	V254 G17	V254 G16	V254 G15	V254 G14	V254 G13	V254 G12	V254 G11	V254 G10		
			D232h	00h	-	•	-	•	-	-	V255 G19	V255 G18		
			D233h	00h	V255 G17	V255 G16	V255 G15	V255 G14	V255 G13	V255 G12	V255 G11	V255 G10		

NOTE: "-" Don't care

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NT35510

	This command is used to adju	ust the gamma 2.2 corre	ection for the green (po	sitive).			
Description	The command to accuse as	aot ino gamma =1= 00m	ээнэн нэ длаан (ра	S 7).			
	VnG1[9:0]: gamma voltage V	n for gamma 2.2 correc	tion of green data (posi	itive).			
Restriction	-						
	Statu	IS	Ava	ilability			
	Normal Mode On, Idle N	Mode Off, Sleep Out	,	Yes			
Register	Normal Mode On, Idle N	Mode On, Sleep Out	,	Yes			
Availability	Partial Mode On, Idle M	Node Off, Sleep Out	,	Yes			
,	Partial Mode On, Idle M	Node On, Sleep Out	,	Yes			
	Sleep	In	,	Yes			
				11 11 112			
	Status		Default Value				
		\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	00h, D201h (V0G1)	00h, 37h			
			02h, D203h (V1G1)	00h, 61h			
		-)4h, D205h (V3G1)	00h, 92h			
)6h, D207h (V5G1)	00h, B4h			
			08h, D209h (V7G1)	00h, CEh			
		D20	Ah, D20Bh (V11G1)	00h, F6h			
_ [D20	Ch, D20Dh (V15G1)	01h, 14h			
		D20	Eh, D20Fh (V23G1)	01h, 48h			
M = M = M = M		D21	0h, D211h (V31G1)	01h, 6Bh			
		D21	2h, D213h (V47G1)	01h, A7h			
		D21	4h, D215h (V63G1)	01h, D3h			
U		D21	6h, D217h (V95G1)	02h, 18h			
	Power On Sequence		3h, D219h (V127G1)	02h, 50h			
Default			Ah, D21Bh (V128G1)	02h, 52h			
			Ch, D21Dh (V160G1)	02h, 87h			
			Eh, D21Fh (V192G1)	02h, BEh			
			0h, D221h (V208G1)	02h, E2h			
			2h, D223h (V224G1)	03h, 0Fh			
			1h, D225h (V232G1)	03h, 30h			
			Sh, D227h (V240G1)	03h, 5Ch			
			3h, D229h (V244G1)	03h, 77h			
			Ah, D22Bh (V248G1) Ch, D22Dh (V250G1)	03h, 94h			
			Eh, D22Fh (V250G1)	03h, 9Fh			
			Oh, D231h (V254G1)	03h, ACh			
			2h, D231h (V254G1)	03h, BAh			
		D232	03h, C1h				
	S/W Reset		Same above				
	H/W Reset						

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GMBCTR1: Setting Gamma 2.2 Correction for Blue (Positive) (D300h~D333h)

		Add	ress			/ (rameter																	
Inst / Para	R/W	7100		D[15:8]			<u> </u>	amotor																	
		MIPI	Others	(Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0													
			D300h	00h	-	-	-	-	-	-	V0B19	V0B18													
			D301h	00h	V0B17	V0B16	V0B15	V0B14	V0B13	V0B12	V0B11	V0B10													
			D302h	00h	-	-	-	-	-	-	V1B19	V1B18													
			D303h	00h	V1B17	V1B16	V1B15	V1B14	V1B13	V1B12	V1B11	V1B10													
			D304h	00h	-	-	-	-	-	-	V3B19	V3B18													
			D305h	00h	V3B17	V3B16	V3B15	V3B14	V3B13	V3B12	V3B11	V3B10													
			D306h	00h	-	-	-	-	-	7	V5B19	V5B18													
			D307h	00h	V5B17	V5B16	V5B15	V5B14	V5B13	V5B12	V5B11	V5B10													
			D308h	00h	-	-	-	775		// -//	V7B19	V7B18													
			D309h	00h	V7B17	V7B16	V7B15	V7B14	V7B13	V7B12	V7B11	V7B10													
			D30Ah	00h	-	-			$U \cdot U$	'	V11B19	V11B18													
			D30Bh	00h	V11B17	V11B16	V11B15	V11B14	V11B13	V11B12	V11B11	V11B10													
			D30Ch	00h	\\ \Lambda		111	<i>J</i> -	- 5		V15B19	V15B18													
			D30Dh	00h	V15B17	V15B16	V15B15	V15B14	V15B13	V15B12	V15B11	V15B10													
			D30Eh	00h	/ ((-	,	- (n- 11		1	V23B19	V23B18													
			D30Fh	00h 👖	V23B17	V23B16	V23B15	V23B14	V23B13	V23B12	V23B11	V23B10													
			D310h	00h	-	((-	ı	V31B19	V31B18													
4				1/ //		آ	1/ //	1/ //	1/ //	D311h	00h	V31B17	V31B16	V31B15	V31B14	V31B13	V31B12	V31B11	V31B10						
GMBCTR1			D312h	00h	-ا د)	-	-	-	V47B19	V47B18													
GIVIDOTRY	R/W	D3h	D313h	00h	V47B17	V47B16	V47B15	V47B14	V47B13	V47B12	V47B11	V47B10													
			D314h	00h) ار	-	-	-	-	-	V63B19	V63B18													
						D315h	00h	V63B17	V63B16	V63B15	V63B14	V63B13	V63B12	V63B11	V63B10										
11 0												IIII	IIII	////	11112	D316h	00h	-	-	-	-	-	-	V95B19	V95B18
												D317h	00h	V95B17	V95B16	V95B15	V95B14	V95B13	V95B12	V95B11	V95B10				
													11 0	11 0	11 0	D318h	00h	-	-	-	-	-	-	V127 B19	V127 B18
						Dodol	001-	V127	V127	V127	V127	V127	V127	V127	V127										
				D319h	00h	B17	B16	B15	B14	B13	B12	B11	B10												
													ı		D31Ah	00h		-	-	_	-	_	V128	V128	
					1/400	1/400		1/400	1/400	1/400	B19	B18													
			D31Bh	00h	V128	V128	V128	V128	V128	V128	V128	V128 B10													
			-		B17	B16	B15	B14	B13	B12	B11														
			D31Ch	00h	-	-	-	-	-	-	V160 B19	V160 B18													
					V160	V160	V160	V160	V160	V160	V160	V160													
			D31Dh	00h	B17	B16	B15	B14	B13	B12	B11	B10													
			D 0 : =:	05:							V192	V192													
			D31Eh	00h	-	-	-	-	-	-	B19	B18													
			DO4 EI-	004	V192	V192	V192	V192	V192	V192	V192	V192													
		D31Fh	00h	B17	B16	B15	B14	B13	B12	B11	B10														

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		Addı	ress				Pa	rameter																	
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0													
			D320h	00h	-	-	-	-	-	-	V208 B19	V208 B18													
			D321h	00h	V208 B17	V208 B16	V208 B15	V208 B14	V208 B13	V208 B12	V208 B11	V208 B10													
			D322h	00h	1	-	1	-	1	-	V224 B19	V224 B18													
			D323h	00h	V224 B17	V224 B16	V224 B15	V224 B14	V224 B13	V224 B12	V224 B11	V224 B10													
			D324h	00h	-	-	-		75		V232 B19	V232 B18													
			D325h	00h	V232 B17	V232 B16	V232 B15	V232 B14	V232 B13	V232 B12	V232 B11	V232 B10													
			D326h	00h	. <				מי וייי	j	V240 B19	V240 B18													
					D327h	00h	V240 B17	V240 B16	V240 B15	V240 B14	V240 B13	V240 B12	V240 B11	V240 B10											
			D328h	00h		<u> </u>				1	V244 B19	V244 B18													
GMBCTR1 1		D3h D32Ah D32Bh D32Ch D32Dh D32Eh D32Fh	D329h	00h	V244 B17	V244 B16	V244 B15	V244 B14	V244 B13	V244 B12	V244 B11	V244 B10													
	R/W		D32Ah	00h			-	-	-	-	V248 B19	V248 B18													
					D32Bh	00h	V248 B17	V248 B16	V248 B15	V248 B14	V248 B13	V248 B12	V248 B11	V248 B10											
11 2															D32Ch	00h	-	-	-	-	-	-	V250 B19	V250 B18	
															D32Dh	00h	V250 B17	V250 B16	V250 B15	V250 B14	V250 B13	V250 B12	V250 B11	V250 B10	
																D32Eh	00h	1	-	-	-	-	-	V252 B19	V252 B18
															D32Fh	00h	V252 B17	V252 B16	V252 B15	V252 B14	V252 B13	V252 B12	V252 B11	V252 B10	
														D330h	00h	-	-	-	-	-	-	V254 B19	V254 B18		
			D331h	00h	V254 B17	V254 B16	V254 B15	V254 B14	V254 B13	V254 B12	V254 B11	V254 B10													
			D332h	00h	-	-	-	-	-	-	V255 B19	V255 B18													
			D333h	00h	V255 B17	V255 B16	V255 B15	V255 B14	V255 B13	V255 B12	V255 B11	V255 B10													

NOTE: "-" Don't care

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	This command is used to adju	ust the gamma 2.2 corre	ection for the blue (pos	itive).			
Description		g	(1	/.			
	VnB1[9:0]: gamma voltage Vr	n for gamma 2.2 correc	tion of blue data (positi	ve).			
Restriction	-						
	Statu	S	Ava	nilability			
	Normal Mode On, Idle N	Mode Off, Sleep Out		Yes			
Register	Normal Mode On, Idle N	Mode On, Sleep Out		Yes			
Availability	Partial Mode On, Idle M	lode Off, Sleep Out		Yes			
•	Partial Mode On, Idle M	lode On, Sleep Out		Yes 🐧			
	Sleep	In		Yes			
				11 11 11			
	Status		Default Value				
		D30	00h, D301h (V0B1)	00h, 37h			
			02h, D303h (V1B1)	00h, 61h			
		-	04h, D305h (V3B1)	00h, 92h			
		D30	06h, D307h (V5B1)	00h, B4h			
		D30	08h, D309h (V7B1)	00h, CEh			
		D30	Ah, D30Bh (V11B1)	00h, F6h			
~ [\\D30	Ch, D30Dh (V15B1)	01h, 14h			
		\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Eh, D30Fh (V23B1)	01h, 48h			
W = W = W		D31	0h, D311h (V31B1)	01h, 6Bh			
		D31	2h, D313h (V47B1)	01h, A7h			
			4h, D315h (V63B1)	01h, D3h			
U			6h, D317h (V95B1)	02h, 18h			
	Power On Sequence		3h, D319h (V127B1)	02h, 50h			
Default			Ah, D31Bh (V128B1)	02h, 52h			
			Ch, D31Dh (V160B1)	02h, 87h			
			Eh, D31Fh (V192B1)	02h, BEh			
			Oh, D321h (V208B1)	02h, E2h			
			2h, D323h (V224B1) 4h, D325h (V232B1)	03h, 0Fh			
			6h, D327h (V240B1)	03h, 30h 03h, 5Ch			
			Bh, D329h (V244B1)	03h, 77h			
			Ah, D328h (V248B1)				
			Ch, D32Dh (V250B1)	03h, 94h 03h, 9Fh			
			Eh, D32Fh (V250B1)	03h, ACh			
			Oh, D331h (V254B1)	03h, BAh			
			2h, D333h (V255B1)	03h, C1h			
		2002					
	S/W Reset	Same above					
	H/W Reset		Same above				

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GMRCTR2: Setting Gamma 2.2 Correction for Red (Negative) (D400h~D433h)

		Add	ress			,,,,		rameter																
Inst / Para	R/W	7100		D[15:8]			1 4	amotor																
mot/ raid	1,7,7,	MIPI	Others	(Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0												
			D400h	00h	-	-	-	-	-	-	V0R29	V0R28												
			D401h	00h	V0R27	V0R26	V0R25	V0R24	V0R23	V0R22	V0R21	V0R20												
			D402h	00h	-	-	-	-	-	-	V1R29	V1R28												
			D403h	00h	V1R27	V1R26	V1R25	V1R24	V1R23	V1R22	V1R21	V1R20												
			D404h	00h	-	-	-	-	-	-	V3R29	V3R28												
			D405h	00h	V3R27	V3R26	V3R25	V3R24	V3R23	V3R22	V3R21	V3R20												
			D406h	00h	-	-	-	-	-	آ ت	V5R29	V5R28												
			D407h	00h	V5R27	V5R26	V5R25	V5R24	V5R23	V5R22	V5R21	V5R20												
			D408h	00h	-	-	-	-15		- \\	V7R29	V7R28												
			D409h	00h	V7R27	V7R26	V7R25	V7R24	V7R23	V7R22	V7R21	V7R20												
			D40Ah	00h	-	-				•	V11R29	V11R28												
			D40Bh	00h	V11R27	V11R26	V11R25	V11R24	V11R23	V11R22	V11R21	V11R20												
			D40Ch	00h	2-		11/1		- (V15R29	V15R28												
			D40Dh	00h	V15R27	V15R26	V15R25	V15R24	V15R23	V15R22	V15R21	V15R20												
			D40Eh	00h	/ ((-	,	- (n- 11		1	V23R29	V23R28												
			D40Fh	00h 🞵	V23R27	V23R26	V23R25	V23R24	V23R23	V23R22	V23R21	V23R20												
			D410h	00h	-	((7 -	-	V31R29	V31R28												
4		11 17	D411h	00h	V31R27	V31R26	V31R25	V31R24	V31R23	V31R22	V31R21	V31R20												
2			D412h	00h	-ا د)	-	-	-	V47R29	V47R28												
GMRCTR2	R/W	D4h	D413h	00h	V47R27	V47R26	V47R25	V47R24	V47R23	V47R22	V47R21	V47R20												
			D414h	00h	<i>J</i>).	-	-	-	-	-	V63R29	V63R28												
								D415h	00h	V63R27	V63R26	V63R25	V63R24	V63R23	V63R22	V63R21	V63R20							
11 0											llll	/////	/////	IIII	D416h	00h	-	-	-	-	-	-	V95R29	V95R28
											D417h	00h	V95R27	V95R26	V95R25	V95R24	V95R23	V95R22	V95R21	V95R20				
											11 0	11 0	11 0		D418h	00h	-	-	-	-	-	-	V127 R29	V127 R28
											0.01	V127	V127	V127	V127	V127	V127	V127	V127					
				D419h	00h	R27	R26	R25	R24	R23	R22	R21	R20											
					ı								D41Ah	00h	_	-	-	-			V128	V128		
			7 1711	0011							R29	R28												
			D41Bh	00h	V128	V128	V128	V128	V128	V128	V128	V128												
					R27	R26	R25	R24	R23	R22	R21	R20												
			D41Ch	00h	_	_	_	_	-	_	V160	V160												
											R29	R28												
			D41Dh	00h	V160	V160	V160	V160	V160	V160	V160	V160												
			<u> </u>		R27	R26	R25	R24	R23	R22	R21	R20												
			D41Eh	00h	-	-	-	-	-	-	V192 R29	V192 R28												
		1			V192	V192	V192	V192	V192	V192	V192	V192												
		D41Fh	00h	R27	R26	R25	R24	R23	R22	R21	R20													
							0		0	- :														

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		Add	ress				Pa	rameter																	
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0													
		MIPI D4h	D420h	00h	-	-	-	-	-	-	V208 R29	V208 R28													
			D421h	00h	V208 R27	V208 R26	V208 R25	V208 R24	V208 R23	V208 R22	V208 R21	V208 R20													
			D422h	00h	-	-	-	-	-	-	V224 R29	V224 R28													
			D423h	00h	V224 R27	V224 R26	V224 R25	V224 R24	V224 R23	V224 R22	V224 R21	V224 R20													
			D424h	00h	-	-	-	-	RE	711	V232 R29	V232 R28													
			D425h	00h	V232 R27	V232 R26	V232 R25	V232 R24	V232 R23	V232 R22	V232 R21	V232 R20													
			D426h	00h	. <				י מב	'n	V240 R29	V240 R28													
							D427h	00h	V240 R27	V240 R26	V240 R25	V240 R24	V240 R23	V240 R22	V240 R21	V240 R20									
			D428h	00h		- (1	V244 R29	V244 R28													
		D429h	00h	V244 R27	V244 R26	V244 R25	V244 R24	V244 R23	V244 R22	V244 R21	V244 R20														
GMRCTR2	R/W	D4h	D4h	D42Ah	00h			-	-	-	-	V248 R29	V248 R28												
			D42Bh	00h	V248 R27	V248 R26	V248 R25	V248 R24	V248 R23	V248 R22	V248 R21	V248 R20													
110									1/21							D42Ch	00h	-	-	-	-	-	-	V250 R29	V250 R28
															D42Dh	00h	V250 R27	V250 R26	V250 R25	V250 R24	V250 R23	V250 R22	V250 R21	V250 R20	
															D42Eh	00h	-	-	-	-	-	-	V252 R29	V252 R28	
															D42Fh	00h	V252 R27	V252 R26	V252 R25	V252 R24	V252 R23	V252 R22	V252 R21	V252 R20	
															D430h	00h	-	-	-	-	-	-	V254 R29	V254 R28	
			D431h	00h	V254 R27	V254 R26	V254 R25	V254 R24	V254 R23	V254 R22	V254 R21	V254 R20													
			D432h	00h	-	-	-	-	-	-	V255 R29	V255 R28													
			D433h	00h	V255 R27	V255 R26	V255 R25	V255 R24	V255 R23	V255 R22	V255 R21	V255 R20													

NOTE: "-" Don't care

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	This command is used to adi	upt the gamme 2.2 corr	action for the rad (nega	tivo	
Description	This command is used to adj	ust the gamma 2.2 corr	ection for the red (nega	itive).	
Description	VnR2[9:0]: gamma voltage V	'n for gamma 2.2 correc	tion of red data (negative	(AV	
Restriction	- gariina voitage v	THO Gamma 2.2 conec	tion of red data (negati	ve).	
restriction					
	Statu	10	Λνσ	ailability	
	Normal Mode On, Idle			ailability Yes	
	Normal Mode On, Idle	•		Yes	
Register	Partial Mode On, Idle	•			
Availability	Partial Mode On, Idle N	•		Yes Yes	
	Sleep	•		Yes	
	Sieep	· III		163	
			-0		
				11 11 110	
	Status		Default Value	V ·	
	Clarac		Dolugii Valuoji		
			00h, D401h (V0R2)	00h, 37h	
		D40	02h, D403h (V1R2)	00h, 61h	
	a ((04h, D405h (V3R2)	00h, 92h	
			06h, D407h (V5R2)	00h, B4h	
			08h, D409h (V7R2)	00h, CEh	
	92112111		Ah, D40Bh (V11R2)	00h, F6h	
		. ((3))	Ch, D40Dh (V15R2)	01h, 14h	
			Eh, D40Fh (V23R2)	01h, 48h	
< // // // // // // // // // // // // //			0h, D411h (V31R2)	01h, 6Bh	
		/ V	2h, D413h (V47R2)	01h, A7h	
			4h, D415h (V63R2)	01h, D3h	
V			6h, D417h (V95R2)	02h, 18h	
Defecult	Power On Sequence		3h, D419h (V127R2)	02h, 50h	
Default			Ah, D41Bh (V128R2)	02h, 52h	
			Ch, D41Dh (V160R2)	02h, 87h	
			Eh, D41Fh (V192R2) Dh, D421h (V208R2)	02h, BEh	
			2h, D423h (V224R2)	02h, E2h	
			4h, D425h (V232R2)	03h, 0Fh 03h, 30h	
			6h, D427h (V240R2)	03h, 5Ch	
			3h, D429h (V244R2)	03h, 77h	
			Ah, D42Bh (V248R2)	03h, 94h	
			Ch, D42Dh (V250R2)	03h, 94h	
			Eh, D42Fh (V250R2)	03h, ACh	
			Dh, D431h (V254R2)	03h, BAh	
			2h, D433h (V255R2)		
			32h, D433h (V255R2) 03h, C1h		
	S/W Reset		Same above		
	H/W Reset		Same above		

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GMGCTR2: Setting Gamma 2.2 Correction for Green (Negative) (D500h~D533h)

		Add	ress				Pa	rameter																
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0												
			D500h	00h	-	-	-	-	-	-	V0G29	V0G28												
			D501h	00h	V0G27	V0G26	V0G25	V0G24	V0G23	V0G22	V0G21	V0G20												
			D502h	00h	-	-	-	-	-	-	V1G29	V1G28												
			D503h	00h	V1G27	V1G26	V1G25	V1G24	V1G23	V1G22	V1G21	V1G20												
			D504h	00h	-	-	-	-	-	-	V3G29	V3G28												
			D505h	00h	V3G27	V3G26	V3G25	V3G24	V3G23	V3G22	V3G21	V3G20												
			D506h	00h	-	-	1	•	-	7 F	V5G29	V5G28												
			D507h	00h	V5G27	V5G26	V5G25	V5G24	V5G23	V5G22	V5G21	V5G20												
			D508h	00h	-	-	-	-15		-	V7G29	V7G28												
			D509h	00h	V7G27	V7G26	V7G25	V7G24	V7G23	V7G22	V7G21	V7G20												
			D50Ah	00h	-	-				-	V11G29	V11G28												
			D50Bh	00h	V11G27	V11G26	V11G25	V11G24	V11G23	V11G22	V11G21	V11G20												
			D50Ch	00h	4			<i>J</i> -	- 5		V15G29	V15G28												
			D50Dh	00h	V15G27	V15G26	V15G25	V15G24	V15G23	V15G22	V15G21	V15G20												
			D50Eh	00h	-)) \	Ž,	-	Π- <i>\</i> \			V23G29	V23G28												
			D50Fh	00h	V23G27	V23G26	V23G25	V23G24	V23G23	V23G22	V23G21	V23G20												
			D510h	00h	-	((110		-	-	V31G29	V31G28												
1			D511h	00h	V31G27	V31G26	V31G25	V31G24	V31G23	V31G22	V31G21	V31G20												
2		. // //	D512h	00h	<u> </u>)	-	-	-	V47G29	V47G28												
GMGCTR2	R/W	D5h	D513h	00h	V47G27	V47G26	V47G25	V47G24	V47G23	V47G22	V47G21	V47G20												
<u> </u>			D514h	00h	<u>س</u> ۔ `	-	-	-	-	-	V63G29	V63G28												
													D515h	00h	V63G27	V63G26	V63G25	V63G24	V63G23	V63G22	V63G21	V63G20		
11 0													VIII)			D516h	00h	-	-	-	-	-	-	V95G29
												D517h	00h	V95G27	V95G26	V95G25	V95G24	V95G23	V95G22	V95G21	V95G20			
												110	11 2	11 2	11 2	D518h	00h	-	-	-	-	-	-	V127 G29
									DEAOL	004	V127	V127	V127	V127	V127	V127	V127	V127						
			D519h	00h	G27	G26	G25	G24	G23	G22	G21	G20												
					Ì						Ī	}	D51Ah	00h					-	_	V128	V128		
			2017111	5511							G29	G28												
			D51Bh	00h	V128	V128	V128	V128	V128	V128	V128	V128												
					G27	G26	G25	G24	G23	G22	G21	G20												
			D51Ch	00h	-	-	-	-	-	-	V160	V160												
					1/400	1/400	1/400	1/400	1/400	1/400	G29	G28												
			D51Dh	00h	V160	V160 G26	V160	V160 G24	V160	V160 G22	V160	V160												
					G27	G26	G25	G24	G23	G22	G21	G20												
			D51Eh	00h	-	-	-	-	-	-	V192 G29	V192 G28												
					V192	V192	V192	V192	V192	V192	V192	V192												
			D51Fh	00h	G27	G26	G25	G24	G23	G22	G21	G20												

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		Add	ress				Pa	rameter																
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0												
			D520h	00h	-	-	-	-	-	-	V208 G29	V208 G28												
			D521h	00h	V208 G27	V208 G26	V208 G25	V208 G24	V208 G23	V208 G22	V208 G21	V208 G20												
			D522h	00h	1	-	1	-	1	-	V224 G29	V224 G28												
			D523h	00h	V224 G27	V224 G26	V224 G25	V224 G24	V224 G23	V224 G22	V224 G21	V224 G20												
			D524h	00h	-	-	-	-			V232 G29	V232 G28												
			D525h	00h	V232 G27	V232 G26	V232 G2 5	V232 G24	V232 G23	V232 G22	V232 G21	V232 G20												
			D526h	00h	. <				מי וייי	j	V240 G29	V240 G28												
					D527h	00h	V240 G27	V240 G26	V240 G25	V240 G24	V240 G23	V240 G22	V240 G21	V240 G20										
			D528h	00h		-	2)C				V244 G29	V244 G28												
		D529h	00h	V244 G27	V244 G26	V244 G25	V244 G24	V244 G23	V244 G22	V244 G21	V244 G20													
GMGCTR2	R/W		D52Ah	00h			-	-	-	-	V248 G29	V248 G28												
				D52Bh	00h	V248 G27	V248 G26	V248 G25	V248 G24	V248 G23	V248 G22	V248 G21	V248 G20											
11/2									110						D52Ch	00h	-	-	-	-	-	-	V250 G29	V250 G28
															D52Dh	00h	V250 G27	V250 G26	V250 G25	V250 G24	V250 G23	V250 G22	V250 G21	V250 G20
															D52Eh	00h	-	-	-	-	-	-	V252 G29	V252 G28
														D52Fh	00h	V252 G27	V252 G26	V252 G25	V252 G24	V252 G23	V252 G22	V252 G21	V252 G20	
														D530h	00h	-	-	-	-	-	-	V254 G29	V254 G28	
			D531h	00h	V254 G27	V254 G26	V254 G25	V254 G24	V254 G23	V254 G22	V254 G21	V254 G20												
			D532h	00h	-	-	-	-	-	-	V255 G29	V255 G28												
			D533h	00h	V255 G27	V255 G26	V255 G25	V255 G24	V255 G23	V255 G22	V255 G21	V255 G20												

NOTE: "-" Don't care

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	This command is used to ad	just the gamma 2.2 corre	ection for the green (ne	egative).		
Description		-				
	VnG2[9:0]: gamma voltage V	n for gamma 2.2 correc	tion of green data (neg	ative).		
Restriction	-					
	State	us	Ava	ailability		
	Normal Mode On, Idle	·		Yes		
Register	Normal Mode On, Idle	Mode On, Sleep Out		Yes		
Availability	Partial Mode On, Idle I	•		Yes		
	Partial Mode On, Idle I	·		Yes		
	Sleep) In		Yes		
	Status		Default/olu	Al II no		
	Status		Default Value			
		D50	00h, D501h (V0G2)	00h, 37h		
			02h, D503h (V1G2)	00h, 61h		
		D50	04h, D505h (V3 G2)	00h, 92h		
		D50	06h, D507h (V5G2)	00h, B4h		
		D50	08h, D509h (V7G2)	00h, CEh		
		D50.	Ah, D50Bh (V11G2)	00h, F6h		
ا ہ		\\D500	Ch, D50Dh (V15G2)	01h, 14h		
			Eh, D50Fh (V23G2)	01h, 48h		
			0h, D511h (V31G2)	01h, 6Bh		
			2h, D513h (V47G2)	01h, A7h		
			4h, D515h (V63G2)	01h, D3h		
U			6h, D517h (V95G2)	02h, 18h		
-	Power On Sequence		3h, D519h (V127G2)	02h, 50h		
Default			Ah, D51Bh (V128G2)	02h, 52h		
			Ch, D51Dh (V160G2)	02h, 87h		
			Eh, D51Fh (V192G2)	02h, BEh		
			0h, D521h (V208G2)	02h, E2h		
			2h, D523h (V224G2)	03h, 0Fh		
			1h, D525h (V232G2)	03h, 30h		
			Sh, D527h (V240G2)	03h, 5Ch		
			8h, D529h (V244G2)	03h, 77h		
			Ah, D52Bh (V248G2) Ch, D52Dh (V250G2)	03h, 94h		
			Eh, D52Fh (V250G2)	03h, 9Fh		
			Oh, D531h (V254G2)	03h, ACh 03h, BAh		
			2h, D533h (V255G2)	03h, C1h		
		D332	-11, DUUUII (V2UUUZ)	USH, UTH		
	S/W Reset		Same above			
	H/W Reset		Same above			

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GMBCTR2: Setting Gamma 2.2 Correction for Blue (Negative) (D600h~D633h)

		Addı	ress				Pa	rameter																
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0												
			D600h	00h	-	-	-	-	-	-	V0B29	V0B28												
			D601h	00h	V0B27	V0B26	V0B25	V0B24	V0B23	V0B22	V0B21	V0B20												
			D602h	00h	-	-	-	-	-	-	V1B29	V1B28												
			D603h	00h	V1B27	V1B26	V1B25	V1B24	V1B23	V1B22	V1B21	V1B20												
			D604h	00h	-	-	-	-	-	-	V3B29	V3B28												
			D605h	00h	V3B27	V3B26	V3B25	V3B24	V3B23	V3B22	V3B21	V3B20												
			D606h	00h	-	-	-	-	-	- 5	V5B29	V5B28												
			D607h	00h	V5B27	V5B26	V5B25	V5B24	V5B23	V5B22	V5B21	V5B20												
			D608h	00h	-	-	-	- 5		\\ -\\\	V7B29	V7B28												
			D609h	00h	V7B27	V7B26	V7B25	V7B24	V7B23	V7B22	V7B21	V7B20												
			D60Ah	00h	-	-			U- $ $	٠.	V11B29	V11B28												
			D60Bh	00h	V11B27	V11B26	V11B25	V11B24	V11B23	V11B22	V11B21	V11B20												
			D60Ch	00h	7		1111	<i>y</i> -	- (V15B29	V15B28												
			D60Dh	00h	V15B27	V15B26	V15B25	V15B24	V15B23	V15B22	V15B21	V15B20												
			D60Eh	00h	-)) \	A.	-	n- 11			V23B29													
			D60Fh	00h	V23B27	V23B26	V23B25	V23B24	V23B23	V23B22	V23B21	V23B20												
		715	D610h	00h	-	- ((110) -	-	V31B29	V31B28												
1		11 17	D611h	00h	V31B27	V31B26	V31B25	V31B24	V31B23	V31B22	V31B21													
\mathcal{D}_{\sim}		. // //	D612h	00h	<u> </u>	'وسئلام	<u> </u>	-	-	-	V47B29													
GMBCTR2	R/W	D6h	D613h	00h	V47B27	V47B26	V47B25	V47B24	V47B23	V47B22	V47B21													
N (()) //			D614h	00h	J)- `	-	-	-	-	-	V63B29													
												M	M_{\star}	D615h	00h	V63B27			V63B24		V63B22	V63B21		
11 2													D616h	00h	-	-	-	-	-	-	V95B29			
											D617h	00h	V95B27	V95B26	V95B25	V95B24	V95B23	V95B22	V95B21					
														11 2	D618h	00h	-	-	-	-	-	-	V127 B29	V127 B28
														D619h	00h	V127 B27	V127 B26	V127 B25	V127 B24	V127 B23	V127 B22	V127 B21	V127 B20	
																	D61Ah	00h	-	-	-	-	-	-
					V128	V128	V128	V128	V128	V128	V128	V128												
			D61Bh	00h	B27	B26	B25	B24	B23	B22	B21	B20												
			D040'	001							V160	V160												
			D61Ch	00h	-	-	-	-	-	-	B29	B28												
			D61Dh	00h	V160	V160	V160	V160	V160	V160	V160	V160												
			חחו סט	UUII	B27	B26	B25	B24	B23	B22	B21	B20												
			D61Eh	00h	-	-	-		-	-	V192	V192												
				5511							B29	B28												
			D61Fh	00h	V192	V192	V192	V192	V192	V192	V192	V192												
					B27	B26	B25	B24	B23	B22	B21	B20												

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		Add	ress				Pa	rameter									
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0					
			D620h	00h	-	-	-	-	•	-	V208 B29	V208 B28					
			D621h	00h	V208	V208	V208	V208	V208	V208	V208	V208					
			D02 III	0011	B27	B26	B25	B24	B23	B22	B21	B20					
			D622h	00h	-	-	-	-	-	-	V224	V224					
					1/00/4	1/00/4	1/004	1/004	1/004	1/00/4	B29	B28					
			D623h	00h	V224 B27	V224 B26	V224 B25	V224 B24	V224 B23	V224 B22	V224 B21	V224 B20					
					DZT	D20	525	D24	D23	DZZ	V232	V232					
			D624h	00h	-	-	-	-	" UL	\ -\\	B29	B28					
			Deach	004	V232	V232	V232	V232	V232	V232	V232	V232					
			D625h	00h	B27	B26	B25	B24	B23	B22	B21	B20					
			D626h	00h			// <u>/</u> //		20		V240	V240					
			D02011	0011			11.11	リレ			B29	B28					
			D627h	00h	V240	V240	V240	V240	V240	V240	V240	V240					
			-		B27	B26	B25	B24	B23	B22	B21	B20					
			D628h	00h		-	$\sim (C$	5/1/	111 /		V244	V244					
			D629h			V244	V244	V244	V244	V244	V244	B29 V244	B28 V244				
				00h	B27	W244 B26	V244 B25	B24	W244 B23	W244 B22	W244 B21	B20					
GMBCTR2	R/W	D6h		2.0	> // ·		<u>DZ</u> 0	DZ I	DEO	DEE	V248	V248					
				7 "	7 "	7 11 .	D62Ah	00h			-	-	-	-	B29	B28	
N (()) //				D62Bh	OOh	V248	V248	V248	V248	V248	V248	V248	V248				
				n/	n (\mathcal{M}	$\mathcal{N}(\mathcal{C})$	DOZBII	00h	B27	B26	B25	B24	B23	B22	B21	B20
11 2				D62Ch	00h	_	_	_	_	_	_	V250	V250				
		11 121.									B29	B28					
		U	D62Dh	00h	V250	V250	V250	V250	V250	V250	V250	V250					
					B27	B26	B25	B24	B23	B22	B21	B20					
			D62Eh	00h	-	-	-	-	-	-	V252 B29	V252 B28					
					V252	V252	V252	V252	V252	V252	V252	V252					
			D62Fh	00h	B27	B26	B25	B24	B23	B22	B21	B20					
			Deack	004							V254	V254					
			D630h	00h	-	-	-	-	-	-	B29	B28					
			D631h	00h	V254	V254	V254	V254	V254	V254	V254	V254					
			203111	0011	B27	B26	B25	B24	B23	B22	B21	B20					
			D632h	00h	_	_	_	_	_	_	V255	V255					
											B29	B28					
			D633h	00h	V255	V255	V255	V255	V255	V255	V255	V255					
					B27	B26	B25	B24	B23	B22	B21	B20					

NOTE: "-" Don't care

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	This command is used to adju	st the gamma 2.2 corre	ection for the blue (neg	ative).		
Description		-	· -	•		
	VnB2[9:0]: gamma voltage Vn	for gamma 2.2 correc	tion of blue data (negat	tive).		
Restriction	-					
	_					
	Status		Availability			
	Normal Mode On, Idle M	·	Yes			
Register		Normal Mode On, Idle Mode On, Sleep Out		Yes		
Availability	Partial Mode On, Idle M	•	Yes			
	Partial Mode On, Idle Mo			Yes Yes		
	Зіеер і			163		
	Status		Default Value	V		
		A Maria)0h DC04h ((/0D2)	005 075		
			00h, D601h (V0B2) 02h, D603h (V1B2)	00h, 37h 00h, 61h		
	6	*	04h, D605h (V3B2)	00h, 92h		
	~ // ((\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	06h, D607h (V5B2)	00h, B4h		
			08h, D609h (V7B2)	00h, CEh		
			Ah, D60Bh (V11B2)	00h, F6h		
~ N		\\D60	Ch, D60Dh (V15B2)	01h, 14h		
		\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Eh, D60Fh (V23B2)	01h, 48h		
W(U)		D61	0h, D611h (V31B2)	01h, 6Bh		
			2h, D613h (V47B2)	01h, A7h		
			4h, D615h (V63B2)	01h, D3h		
			6h, D617h (V95B2)	02h, 18h		
Default	Power On Sequence		3h, D619h (V127B2) Ah, D61Bh (V128B2)	02h, 50h		
Delault			Ch, D61Dh (V160B2)	02h, 52h 02h, 87h		
			Eh, D61Fh (V192B2)	02h, 87h		
			Oh, D621h (V208B2)	02h, E2h		
			2h, D623h (V224B2)	03h, 0Fh		
			1h, D625h (V232B2)	03h, 30h		
		D626	6h, D627h (V240B2)	03h, 5Ch		
		D628	3h, D629h (V244B2)	03h, 77h		
		D62/	Ah, D62Bh (V248B2)	03h, 94h		
			Ch, D62Dh (V250B2)	03h, 9Fh		
			h, D62Fh (V252B2)	03h, ACh		
			0h, D631h (V254B2)	03h, BAh		
		D632	2h, D633h (V255B2)	03h, C1h		
	S/W Reset		Same above			
	H/W Reset		Same above			

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MTPDET: MTP Power Detection (EC00h)

		Add	ress				Pai	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MTPDET	R	ECh	EC00h	00h	-	-	-	-	-	•	1	MTP_ DET

NOTE: "-" Don't care

NOTE: "-" Don't ca	are
Description	This command is used to check the external power for MTP programming which is ready or not. When the pad MTP_PWR is floating or connected to ground, the read out value of MTP_DET register is "0". When the external power 7.5V is connected to the pad MTP_PWR, the read our value of MTP_DET register is "1".
Restriction	
Register Availability	Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes
Default	Status Default Value Power On Sequence 00h S/W Reset 00h H/W Reset 00h

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MTPEN: MTP Enable Control (ED00h~ED01h)

		Add	ress				Pa	rameter				
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MTPEN	R/W	EDh	ED00h	00h	MTP_ EN17	MTP_ EN16	MTP_ EN15	MTP_ EN14	MTP_ EN13	MTP_ EN12	MTP_ EN11	MTP_ EN10

MO.	TF.	"_"	Don't	cara
1411	1 -	-	,,,,,,,	Care

This command is used to enable the different group data for MTP programming respectively.

	Bit	Description	Value
	MTP_EN1[7]	MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)	"0": Disable "1": Enable
	MTP_EN1[6]	MTP for gamma 2.2 correction (D0xxh~D6xxh of page 1)	"0": Disable "1": Enable
	MTP_EN1[5]	MTP for panel color and DDB (C8xxh, C9xxh of page 1)	"0": Disable "1": Enable
Description	MTP_EN1[4]	Fixed to 0	-
	MTP_EN1[3]	Fixed to 0	-
	MTP_EN1[2]	Fixed to 0	
	MTP_EN1[1]	Fixed to 0	-
4	MTP_EN1[0]	Fixed to 0	-
	MILL TEIMIN	HACU TO O	-

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Default Value
00h
00h
00h

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NT35510

MTPWR: MTP Write (EE00h~EE02h)

		Address		Parameter								
Inst / Para	R/W	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
			EE00h	00h	1	0	1	0	0	1	0	1
MTPWR W	W	EEh	EE01h	00h	0	1	0	1	1	0	1	0
			EE02h	00h	0	0	1	1	1	1	0	0

NOTE: "-" Don't ca	NOTE: "-" Don't care										
	This command is MTP write co	mmand.		1							
Description	MTP programming.	The MTP write sequence EE00h+0x00A5 → EE01h+0x005A → EE02h+0x3Ch must be followed for MTP programming. This function is active when the sequence above is complete and the EE02 command is executed.									
Restriction	-	•		// ///							
Register Availability	Status Normal Mode On, Idle Mo Normal Mode On, Idle Mo Partial Mode On, Idle Mo Partial Mode On, Idle Mo Sleep In	de On, Sleep Out de Off, Sleep Out de On, Sleep Out	Availal Ye. Ye. Ye. Ye.								
Default	Status Power On Sequence S/W Reset H/W Reset	EE00h A5h A5h A5h	Default Value EE01h 5Ah 5Ah 5Ah	EE02h 3Ch 3Ch 3Ch							

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RDMTP: Read MTP Status (EF00h~EF01h)

	R/W	Address		Parameter								
Inst / Para		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DOMTO	R	EFh	EF00h	00h		MTP_S TUS16	_	_	_		_	_
RDMTP	K	EFII	EF01h	00h		MTP_S TUS26	_	_	_		_	MTP_S TUS20

NOTE: "-" Don't care

This command is represent the current status which the group data shown in command ED00h, ED01h is programmed or not.

	Bit	Description	Value							
	MTP_STUS1[7]	1 st time MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)	"0": Not programmed "1": Programmed							
	MTP_STUS1[6]	2 nd time MTP for ID1/2/3 VGMP VGSP VGMN VGSN								
	MTP_STUS1[5]	"0": Not programmed "1": Programmed								
	MTP_STUS1[4]	P_STUS1[4] 4 th time MTP for ID1/2/3, VGMP, VGSP, VGMN, VGSN and VCOM offset (C7xxh, BCxxh~BExxh of page 1)								
	MTP_STUS1[3]	Not defined	X							
1	MTP_STUS1[2]	MTP_STUS1[2] Not defined								
	MTP_STUS1[1]	1 st time MTP for gamma 2.2 correction (D0xxh~D6xxh of page 1)	"0": Not programmed "1": Programmed							
	MTP_STUS1[0]	2 nd time MTP for gamma 2.2 correction								

Description

Bit	Description	Value
MTP_STUS2[7]	Not defined	X
MTP_STUS2[6]	Not defined	X
MTP_STUS2[5]	1 st time MTP for panel color and DDB (C8xxh, C9xxh of page 1)	"0": Not programmed "1": Programmed
MTP_STUS2[4]	1 st time MTP for panel color and DDB (C8xxh, C9xxh of page 1)	"0": Not programmed "1": Programmed
MTP_STUS2[3]	Not defined	X
MTP_STUS2[2]	Not defined	X
MTP_STUS2[1]	Not defined	X X
MTP_STUS2[0]	Not defined	X

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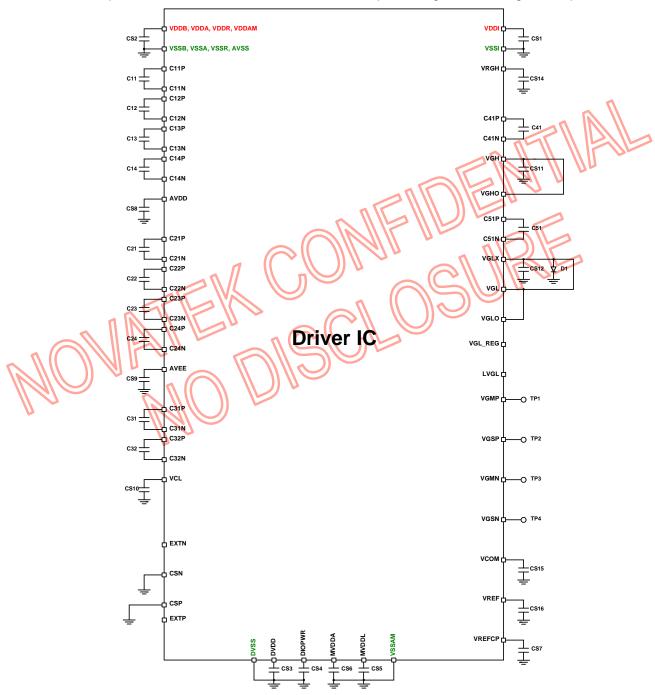
Restriction	-		
Register Availability	Status	<u> </u>	Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep I	n	Yes
Default	Status	Default Value	
	Status	MTP_STU	JS1 MTP_STUS2
	Power On Sequence	00h (XXh after MTP) 00h (XXh after MTP)	
	S/W Reset	00h (XXh after MTP) 00h (XXh after MTP)	
	H/W Reset	00h (XXh afte	er MTP) 00h (XXh after MTP)



2 POWER GENERATION CIRCUIT

2.1 DC/DC Converter Circuit

The DC-DC converter is highly efficient step-up voltage generator circuits that generate the high voltage level AVDD/AVEE required for source drivers and VGHO/VGLO required for gate control signals for panel.



Notes:

1. Input voltage VDDB=2.6~4.8V when using charge pump for AVDD/AVEE voltage.

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3 MAXIMUM SERIES RESISTANCE

The driver will operate in "Chip on Glass" applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in below table.

Name	Туре	Maximum Series Resistance	Unit
VDDI	Power supply	10	Ω
VDDA, VDDR	Power supply	10	Ω
VDDB	Power supply	5	Ω
VDDAM	Power supply	10	Ω
DVDD	Power supply	10	a M b
DIOPWR, MVDDA, MVDDL	Power supply	10	Q
VSSI	Power supply	10	Ω
DVSS	Power supply	10	Ω
VSSA, VSSR, AVSS	Power supply	10	Ω
VSSB	Power supply	5	Ω
VSSAM	Power supply	10	Ω
IM[3:0], VSEL, I2C_SA0, RGBBP, LANSEL, DSWAP, PSWAP, VGSW[3:0], NBWSEL, DSTB_SEL	Input	C 100	Ω
RESX	Input	50	Ω
CSX, WRX/SCL/I2C_SCL, RDX, SDI/I2C_SDA	Input C	50	Ω
SDO, TE, ERR, GPO[3:0], LEDPWM, LEDON, KBBC	Output	50	Ω
D23 to D0	Input / Output	50	Ω
PCLK, DE, VS, HS	Input	50	Ω
HSSI_CLK_P/N, HSSI_DATA0_P/N, HSSI_DATA1_P/N	Input	10	Ω
VREF_PWR, VREFCP	Power output	10	Ω
VGMP, VGSP, VGMN, VGSN	Power output	10	Ω
VCOM	Capacitor connection	5	Ω
AVDD, AVEE, VCL	Capacitor connection	5	Ω
C11P/N~C14P/N	Capacitor connection	5	Ω
C21P/N~C24P/N	Capacitor connection	5	Ω
C31P/N~C32P/N	Capacitor connection	5	Ω
VGH, VGLX, VGL_REG	Capacitor connection	10	Ω
C41P/N, C51P/N	Capacitor connection	5	Ω
EXTP, EXTN	MOS connection	10	Ω
CSP, CSN	Resistor connection	20	Ω
MTP_PWR	Power supply	10	Ω

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4 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Typical Value
VDDI	VDDI, connect to capacitor (Max 6V) VDDI GND	1.0µF
VDDA, VDDR, VDDB, VDDAM	VDD2, connect to capacitor (Max 6V) VDD2 GND	2.2~4.7μF
DVDD	Connect to Capacitor (Max 3V): DVDD GND	1.0µF
DIOPWR	Connect to Capacitor (Max 3V): DIOPWR GND	1.0µF
MVDDA	Connect to Capacitor (Max 3V): MVDDA GND	1.0µF
MVDDL	Connect to Capacitor (Max 3V): MVDDL GND	1.0µF
VSSI, DVSS	Interface and Digital ground (Connect to GND)	-
VSSB, VSSA, VSSR, AVSS	Analog ground (Connect to GND)	2
VSSAM	MIPI ground (Connect to GND)	
C11P, C11N	Connect to Capacitor (Max 6V): C11P C11N	1.0µF
C12P, C12N	Connect to Capacitor (Max 10V): C12P C12N	1.0µF
C13P, C13N	Connect to Capacitor (Max 6V): C13P C13N	1.0µF
C14P, C14N	Connect to Capacitor (Max 10V): C14P C14N	1.0µF
C21P, C21N	Connect to Capacitor (Max 10V): C21P C21N	1.0µF
C22P, C22N	Connect to Capacitor (Max 16V): C22P C22N	1.0µF
C23P, C23N	Connect to Capacitor (Max 10V): C23P C23N	1.0µF
C24P, C24N	Connect to Capacitor (Max 16V): C24P C24N	1.0µF
C31P, C31N	Connect to Capacitor (Max 6V): C31P C31N	1.0µF
C32P, C32N	Connect to Capacitor (Max 10V): C32P C32N	1.0µF
C41P, C41N	Connect to Capacitor (Max 16V): C41P C41N	1.0µF
C51P, C51N	Connect to Capacitor (Max 16V): C51P C51N	1.0µF
AVDD	Connect to Capacitor (Max 10V): AVDD GND	4.7μF
AVEE	Connect to Capacitor (Max 10V): AVEE GND	4.7μF
VCL	Connect to Capacitor (Max 6V): VCL GND	2.2µF
VGH	Connect to Capacitor (Max 25V): VGH GND	2.2µF
VGLX, VGL	Connect to Capacitor (Max 25V): VGLX GND L GND L VGL	2.2µF
VGL_REG (can be open if not used)	Connect to Capacitor (Max 25V): VGL_REG GND	1.0μF
VRGH (can be open if not used)	Connect to Capacitor (Max 10V): VRGH GND	1.0µF
VREFCP	Connect to Capacitor (Max 6V): VREFCP GND	1.0µF
VCOM	Connect to Capacitor (Max 6V): VCOM GND	2.2µF
VREF_PWR	Connect to Capacitor (Max 6V): VREF GND	2.2µF
VGMP, VGSP, VGMN, VGSN	Test point on FPC for measurement purpose	-

NOTE: The specification of Schottky Diode: VF<0.4V at 100mA, VR>30V.

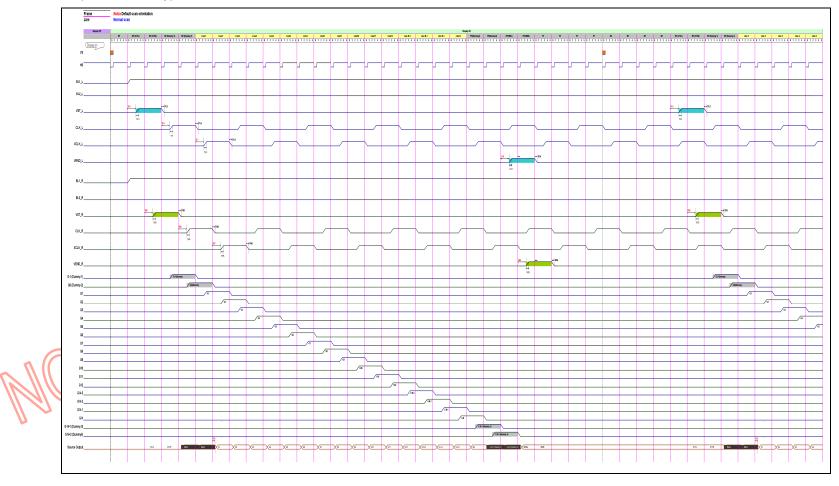
The recommane component:Panasonic MA27D29



5 Timing Example

In this section we listed timing example for GOA Type1 to Type3. The relative setting registers are presented in Display timing control section.

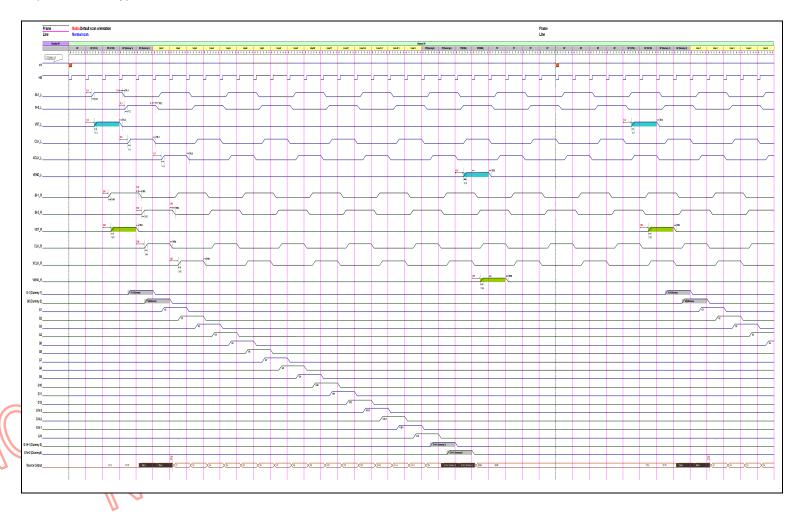
This is example for GOA Type1.



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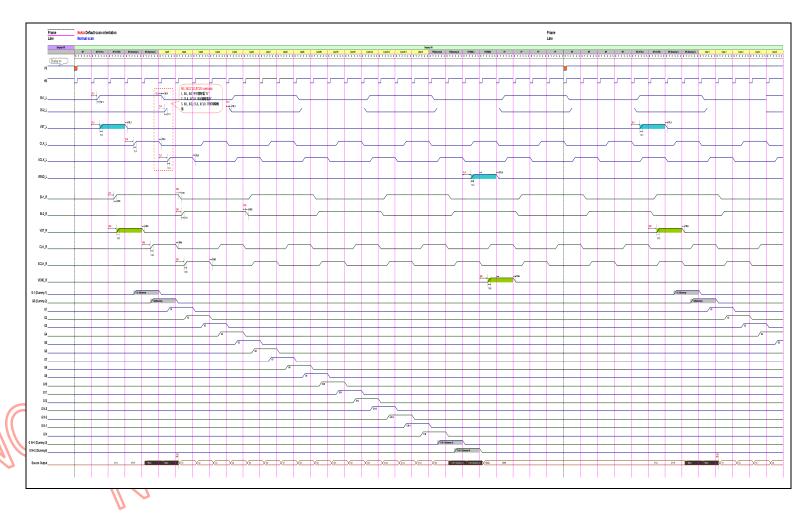
This is example for GOA Type2.



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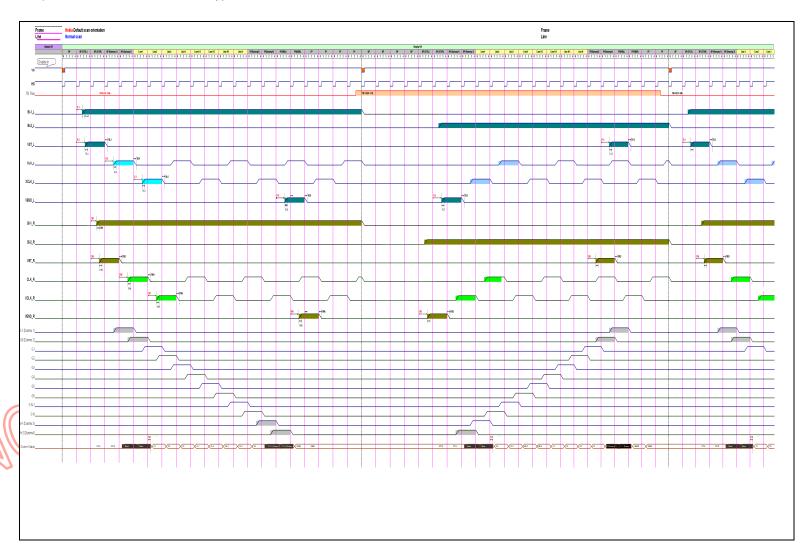
This is example for GOA Type3.



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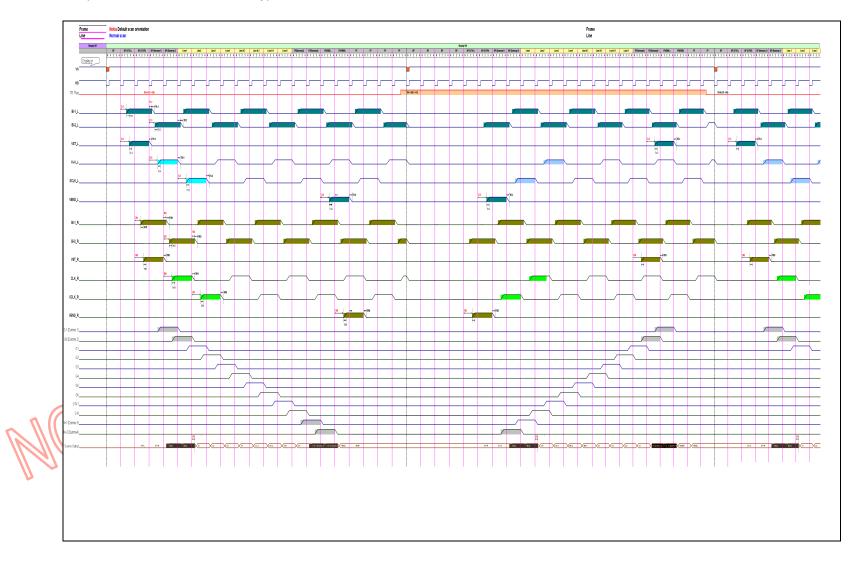
This is example for GOA Scan Direction Type1.



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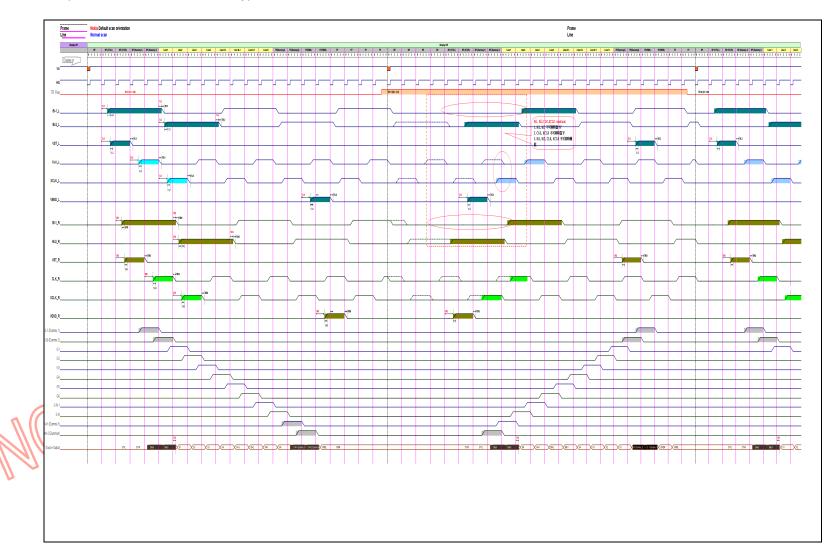
This is example for GOA Scan Direction Type2.



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This is example for GOA Scan Direction Type3.



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