

CSAmplifierDesign

Junchao Zhou

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1 Design Specification

Design a CS stage amplifier with current-source load.

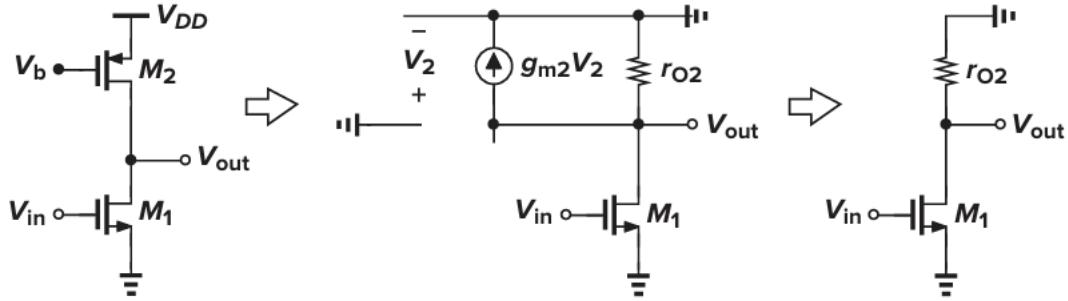


Figure 3.18 CS stage with current-source load.

The specifications are following:

$$V_{DD} = 1.2V$$

$$V_{out} = 0.6V$$

$$I_d = 100\mu A$$

$$C_L = 1pF$$

$$A_v > 42dB$$

$$GBW > 100MHz$$

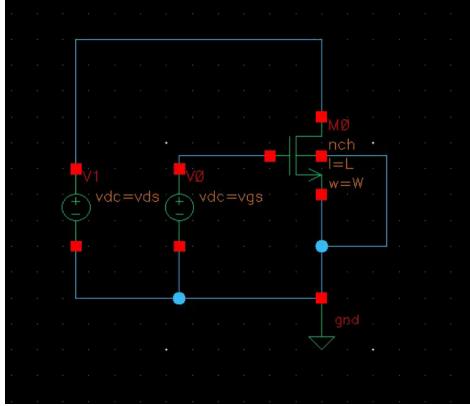
$$\text{Input-referred Noise (1kHz - 1MHz)} < 8\mu V$$

2 Design Procedure

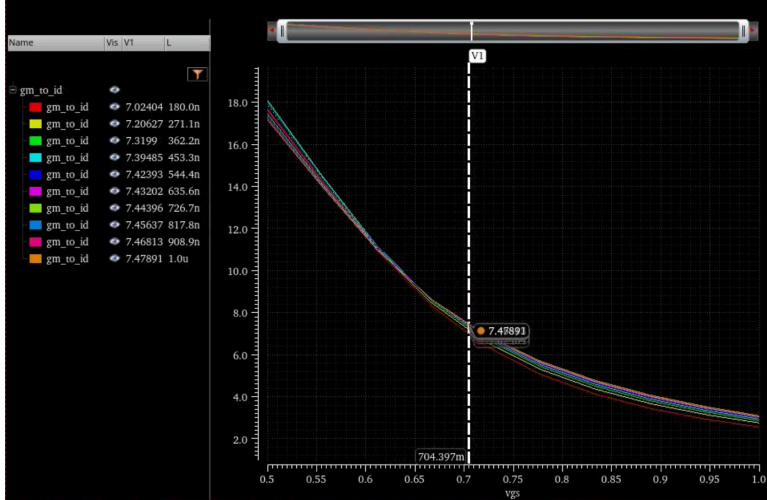
2.1 NMOS Design

$\frac{g_m}{i_d}$, transconductance to drain current ratio, is a crucial parameter to determine the efficiency of converting input voltage to current. It is mostly dependent on V_{gs} since $\frac{g_m}{i_d} = \frac{2}{V_{gs}-V_{th}}$. Because we know $I_d = 100\mu A$, in order to find $\frac{g_m}{i_d}$ we need to find the g_m first. And as we are given $GBW > 100MHz$ (we ignore $f_T = \frac{g_m}{C_{gg}}$ because it is usually greater than 1GHz), $C_L = 1pF$, $GBW = \frac{g_m}{2\pi C_L}$, we can find $g_m = GBW \times 2\pi \times C_L > 0.628mS$.

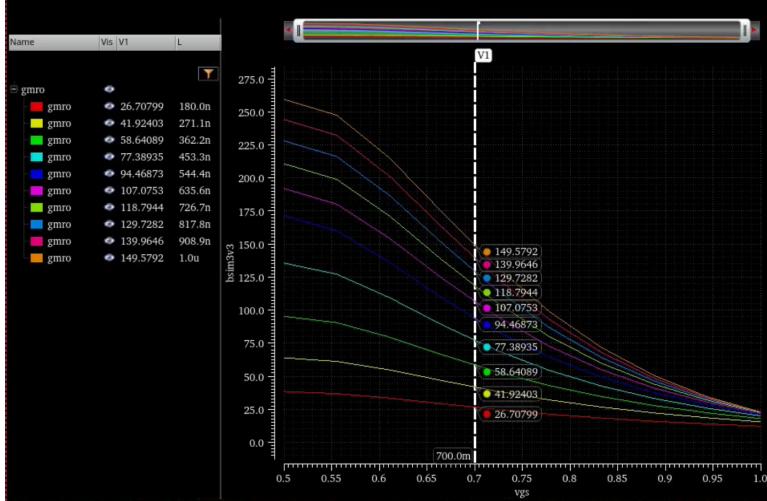
After we know the value of g_m and i_d , we can use $\frac{g_m}{i_d}$ vs. V_{gs} graph to find the required V_{gs} for $\frac{g_m}{i_d} > 6.28 \approx 7$.



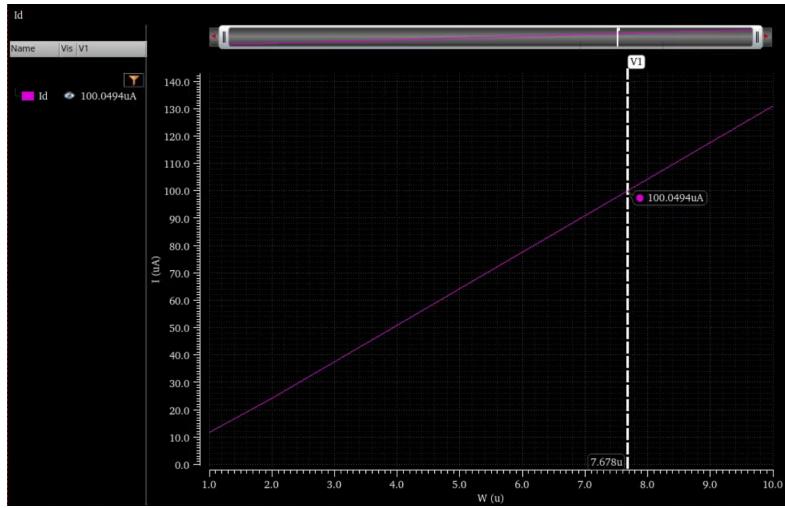
Through a DC sweep simulation, we can find $V_{gs} < 0.7V$.



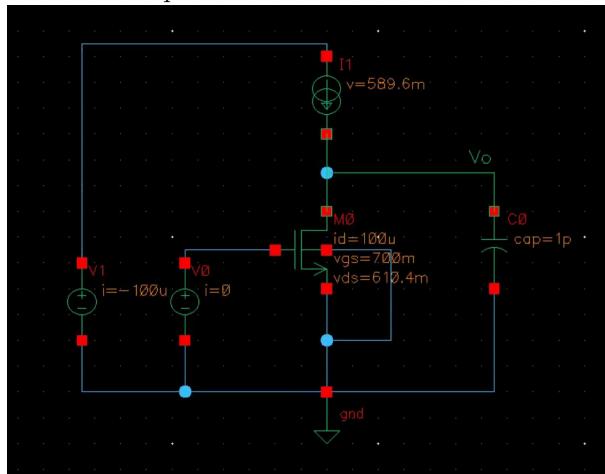
And for $A_v = g_m r_o > 42dB = 10^{42/20} \approx 126$ and suppose $V_{gs} = 0.7V$, through simulation, we can find $L > 820nm$.



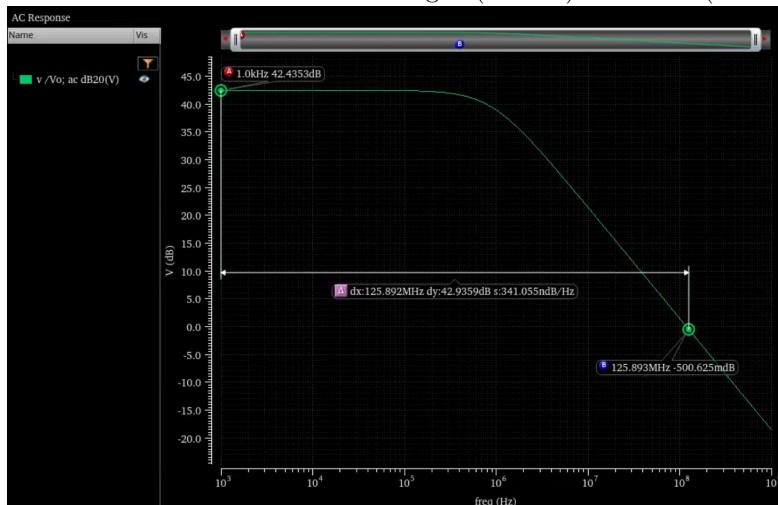
Then, we set $V_{ds} = 0.6V, V_{gs} = 0.7V, L = 820nm$, and sweep the W to find the value of W for $I_d = 100\mu A$. And we can find $W = 7.67\mu m$



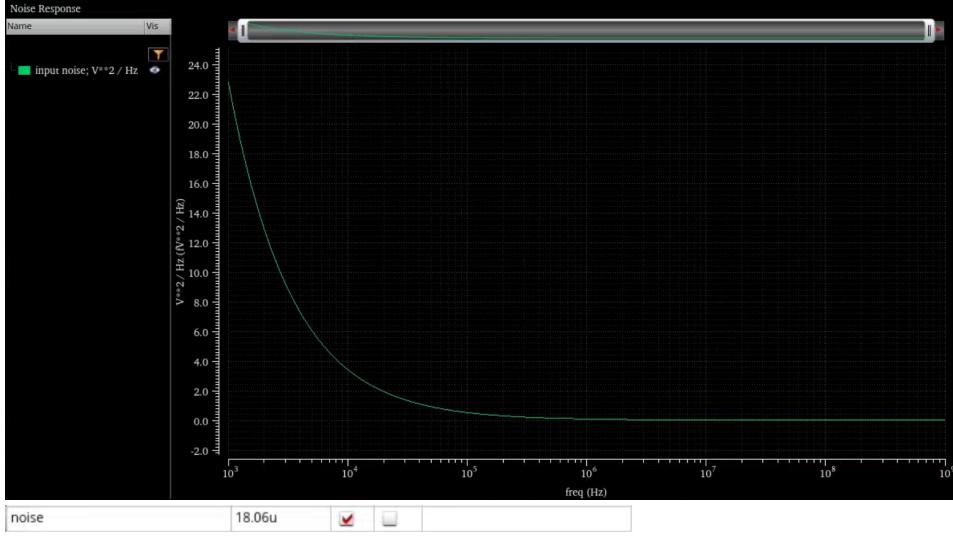
After we decided our NMOS parameters, we can add a current source load by an ideal current source, and a load capacitor to test our circuit.



And from AC result we can see the gain(42.4dB) and GBW(125MHz) met our expectation.



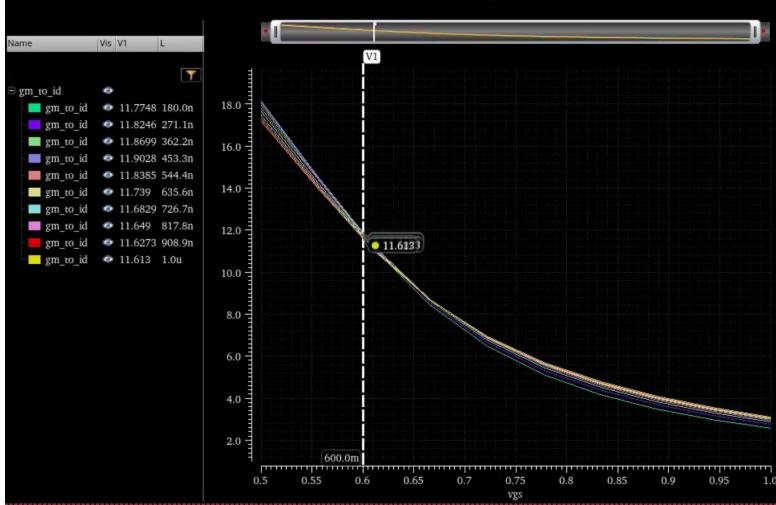
But the input referred noise is quite large (18uV).



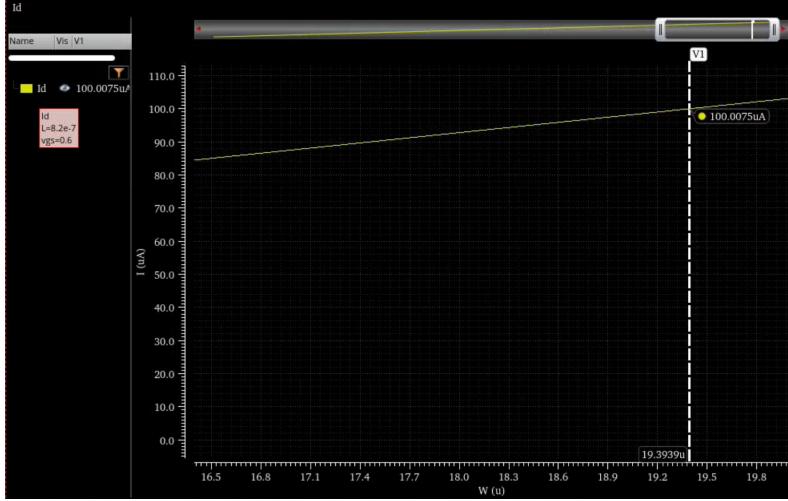
2.2 Noise Reduction

From text we know $\overline{V_{in,n}^2} = \frac{4kT\gamma}{g_m} + \frac{K}{C_{ox}WL}\frac{1}{f}$.

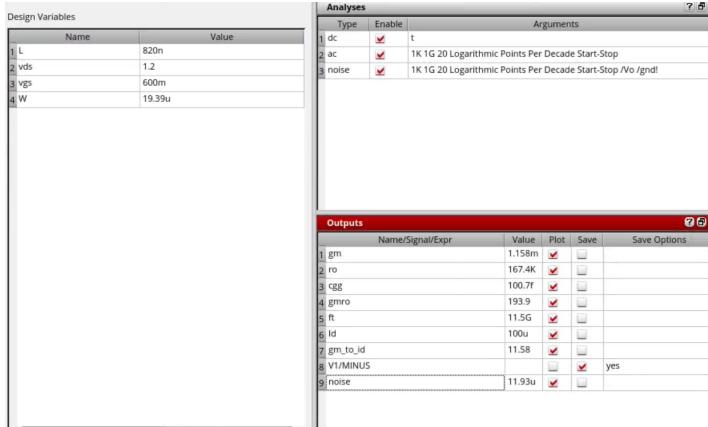
We can increase the g_m to decrease the thermal noise and increase the area to reduce the flicker noise. To increase the g_m , and keep I_D constant, we can decrease V_{gs} since $g_m = \frac{2I_D}{V_{gs} - V_{th}}$. Using g_m/i_d graph, we can select $V_{gs} = 0.6V$ instead of 0.7V.



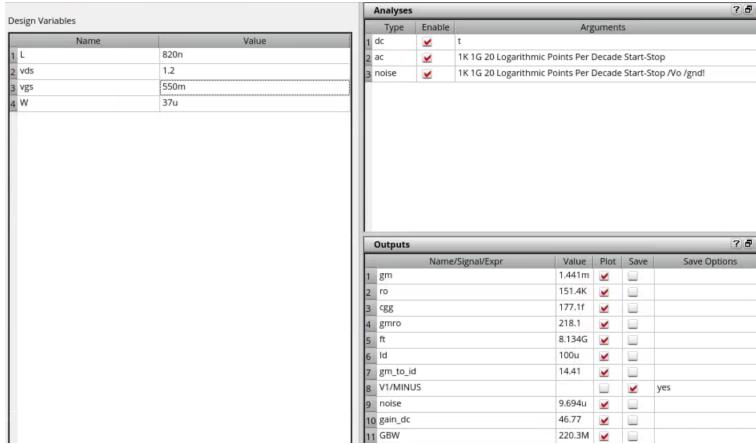
After we chose new V_{gs} , we can keep length as same as 820nm in order to increase W since $I_d = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$ since I_d is constant. Though sweeping W , we can find $W = 19.39\mu m$



After choose our new $V_{gs} = 0.6V$ and $W = 19.39\mu m$, we re-run the simulation for noise. But we found this noise is still larger than we expected.



We decreased the V_{gs} to 0.55V and increased W to 37um, and right now the noise is around 9.7uV. Suppose this value is good enough and we can start to design the PMOS.

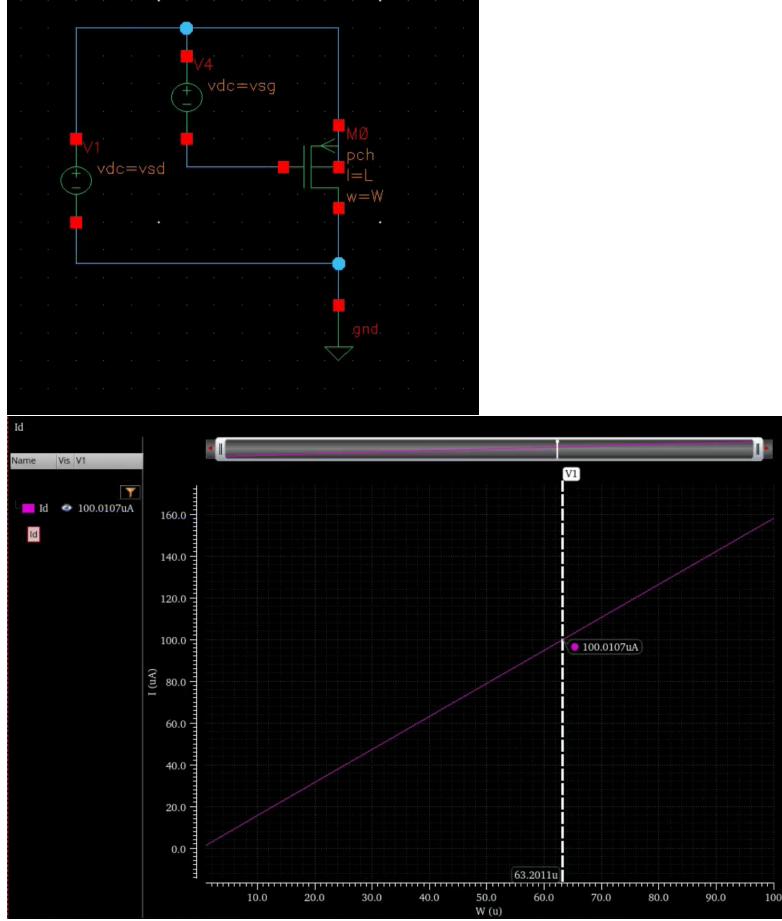


2.3 PMOS Design

For PMOS, we need to consider two points. Firstly, $r_{op} > r_{on}$ to make the gain close to $g_m r_{on}$. To increase r_{op} , we can increase the length of PMOS because current is constant, $r_{op} = \frac{1}{\lambda I_d} \propto L$. Secondly, g_{m2} should be low enough to reduce the noise current because $\overline{V_{pmos,in}^2} = 4kT\gamma \frac{g_{m2}}{g_{m1}^2}$. To reduce g_{m2} , we can increase V_{gs} . But we cannot increase the length and V_{gs} too much. For same V_{gs} , increasing L will also increase W to keep current constant, but it will increase the parasitic capacitance at the same time, which could reduce f_T . So we limit $L_{pmos} < 10L_{nmos}$. And for the same L , increasing V_{gs} will reduce

the output swing and degrade the linearity. So we limit $|V_{gs2}| < 0.9V$.

Same for NMOS design, we firstly choose $L_p = 3L_n = 2.46\mu m$ and $|V_{gs,p}| = 800mV$, and we ran the simulation to find the value of W.



3 Design Result

After we designed both NMOS and PMOS, we combined them together and simulated.

We could see the final result meet our expectations.

But for right now, we ignored how to produce the bias voltage, and how to prevent the shift of common mode point due to PVT.

$$A_v = 43.85dB$$

$$GBW = 204.1MHz$$

$$\overline{V_{in}} = 9.887uV$$

