

DeisgnofAnalogCMOSProlems

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1 IntroductiontoAnalogDesign

2 BasicMOSDevicePhsics

2.1

For $W/L = 50/0.5$, plot the drain current of an NFET and a PFET as a function of $|V_{GS}|$ as $|V_{GS}|$ varies from 0 to 3V. Assume that $|V_{DS}| = 3V$.

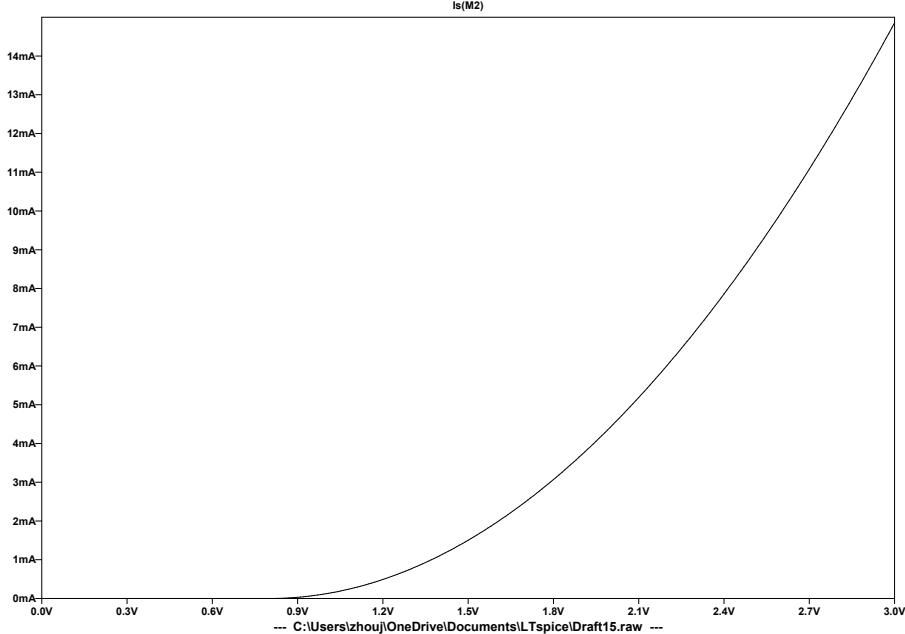
For NMOS and PMOS in cut-off region($V_{gs} < V_{th}$), $I_D = 0$

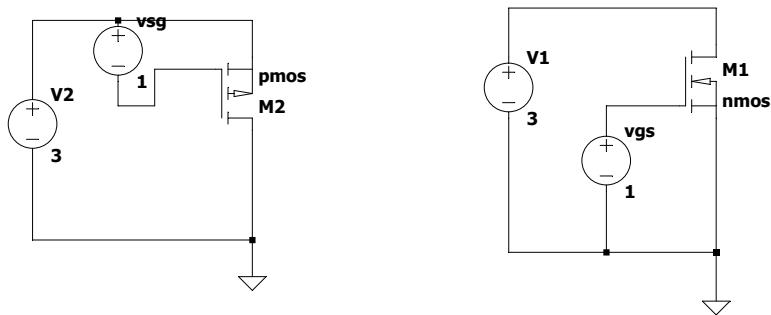
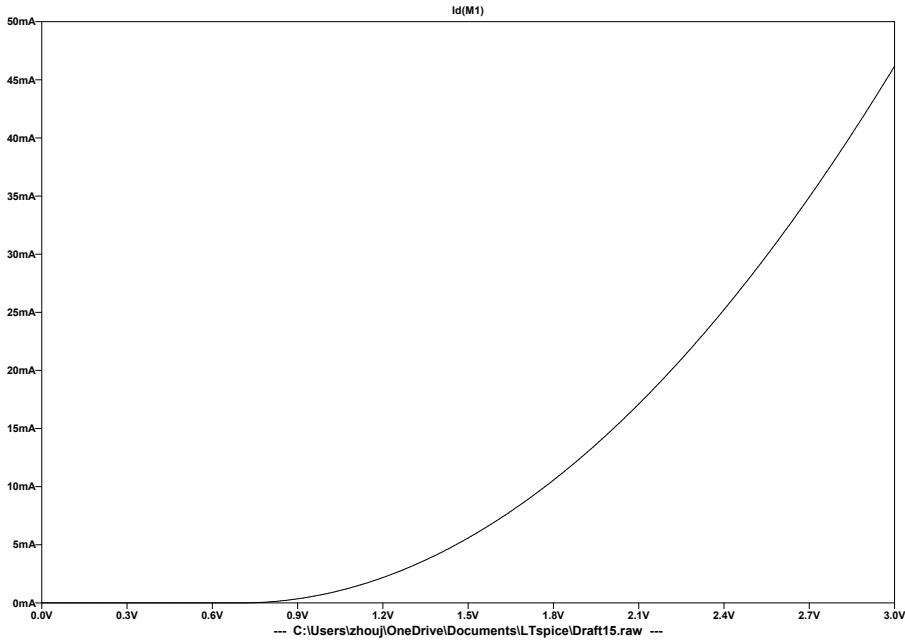
For NMOS and PMOS in saturation region($V_{gs} > V_{th}, V_{ds} > V_{D,sat}$) and consider the channel length effect:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)^2 (1 + \lambda |V_{DS}|)$$

Because we know for PMOS, $VTO = -0.8, TOX = 9e - 9[m], UO = 100[cm^2/V/s], \lambda = 0.2, C_{ox} = \frac{\epsilon}{TOX} = \frac{3.45 \times 10^{-11}}{9 \times 10^{-9}} = 3.833 \times 10^{-3}[F/m^2] = 3.833 \times 10^{-7}[F/cm^2]$, $I_D = 1.9165 \times (|V_{GS}| - 0.8)^2 (1 + 0.2 \times 3)[mA]$, when $V_{GS} = 3, I_D = 14.9mA$

Similar for NMOS, $VTO = 0.7, TOX = 9e - 9[m], UO = 350[cm^2/V/s], \lambda = 0.1, C_{ox} = 3.833 \times 10^{-3}[F/m^2]$, $I_D = 6.7 \times (|V_{GS}| - 0.7)^2 (1 + 0.1 \times 3)[mA]$, when $V_{GS} = 3, I_D = 46mA$





```
.model pmos PMOS(W=50 L=0.5 LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
```

```
.model nmos NMOS(W=50 L=0.5 LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```

```
.dc vgs 0 3 0.01
```

```
.dc vsg 0 3 0.01
```

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2.2

For $W/L = 50/0.5$, and $|I_D| = 0.5mA$, calculate the transconductance and output impedance of both NMOS and PMOS devices. Also, find the "intrinsic gain," defined as $g_m r_o$. $g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$.

For PMOS, $g_m = \sqrt{2 \times 100 \times 3.833 \times 10^{-7} \times 100 \times 0.5 \times 10^{-3}} = 1.957[mS]$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.2 \times 0.5 \times 10^{-3}} = 10k[\Omega]$$

$$g_m r_o = 19.57$$

For NMOS, $g_m = \sqrt{2 \times 350 \times 3.833 \times 10^{-7} \times 100 \times 0.5 \times 10^{-3}} = 3.663[mS]$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.1 \times 0.5 \times 10^{-3}} = 20k[\Omega]$$

$$g_m r_o = 73.26$$

2.3

Derive expressions for $g_m r_o$ in terms of I_D and W/L . Plot $g_m r_o$ as a function of I_D with L as a parameter. Note that $\lambda \propto 1/L$.

$$g_m r_o = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \times \frac{1}{\lambda I_D} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \times \frac{\frac{L_0}{L}}{\lambda I_D} = \sqrt{\frac{2\mu_n C_{ox} W L}{I_D}} \times \frac{1}{L_0 \lambda}$$

2.4

Plot I_D versus V_{GS} for a MOS transistor (a) with V_{DS} as a parameter, and (b) with V_{BS} as a parameter. Identify the break points in the characteristics.

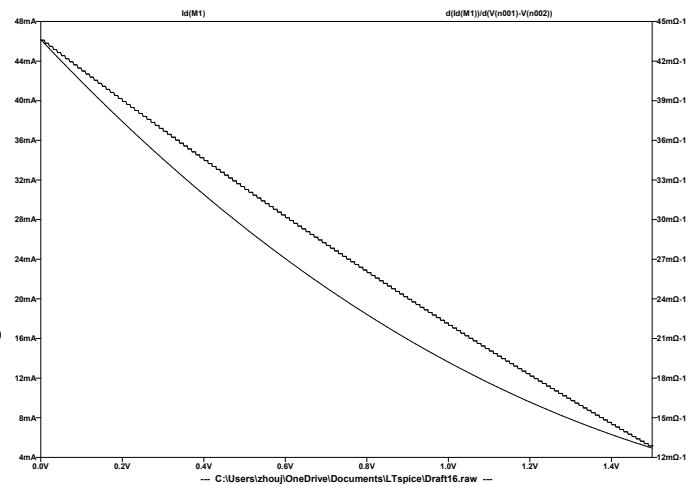
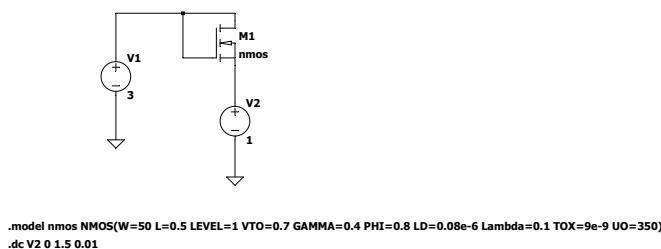
(a) Like the figure in 2.1. When $V_{gs} < V_{th}$, $I_D = 0$. When $V_{gs} > V_{th}$, $V_{gs} - V_{th} < V_{ds}$, it goes into saturation region, $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)^2 (1 + \lambda |V_{DS}|)$. And as $V_{gs} - V_{th} > V_{ds}$, it goes into triode region, $I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2]$.

(b) As $V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{|2\phi_F|})$. A higher $|V_{SB}|$ will move the whole I_D versus V_{GS} graph to right while a lower $|V_{SB}|$ will move it to left.

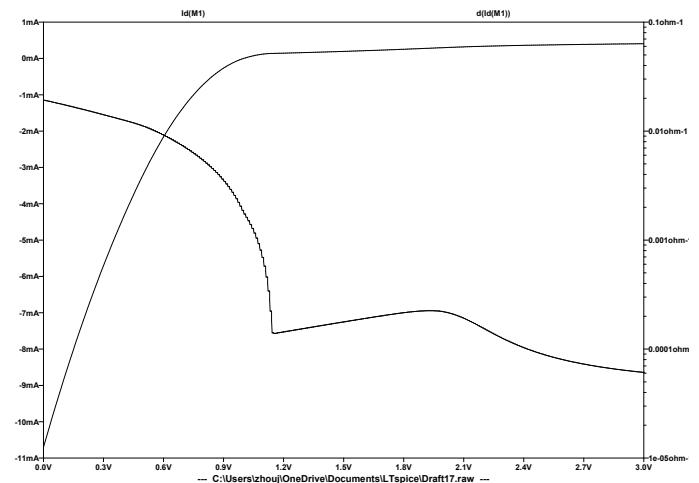
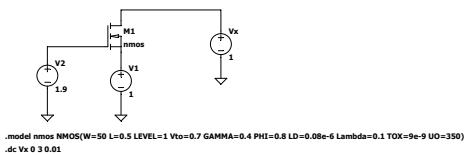
2.5

Sketch I_X and the transconductance of the transistor as a function of V_X for each circuit in Fig.2.47 as V_X varies from 0 to V_{DD} . In part (a), assume that V_X varies from 0 to 1.5V.

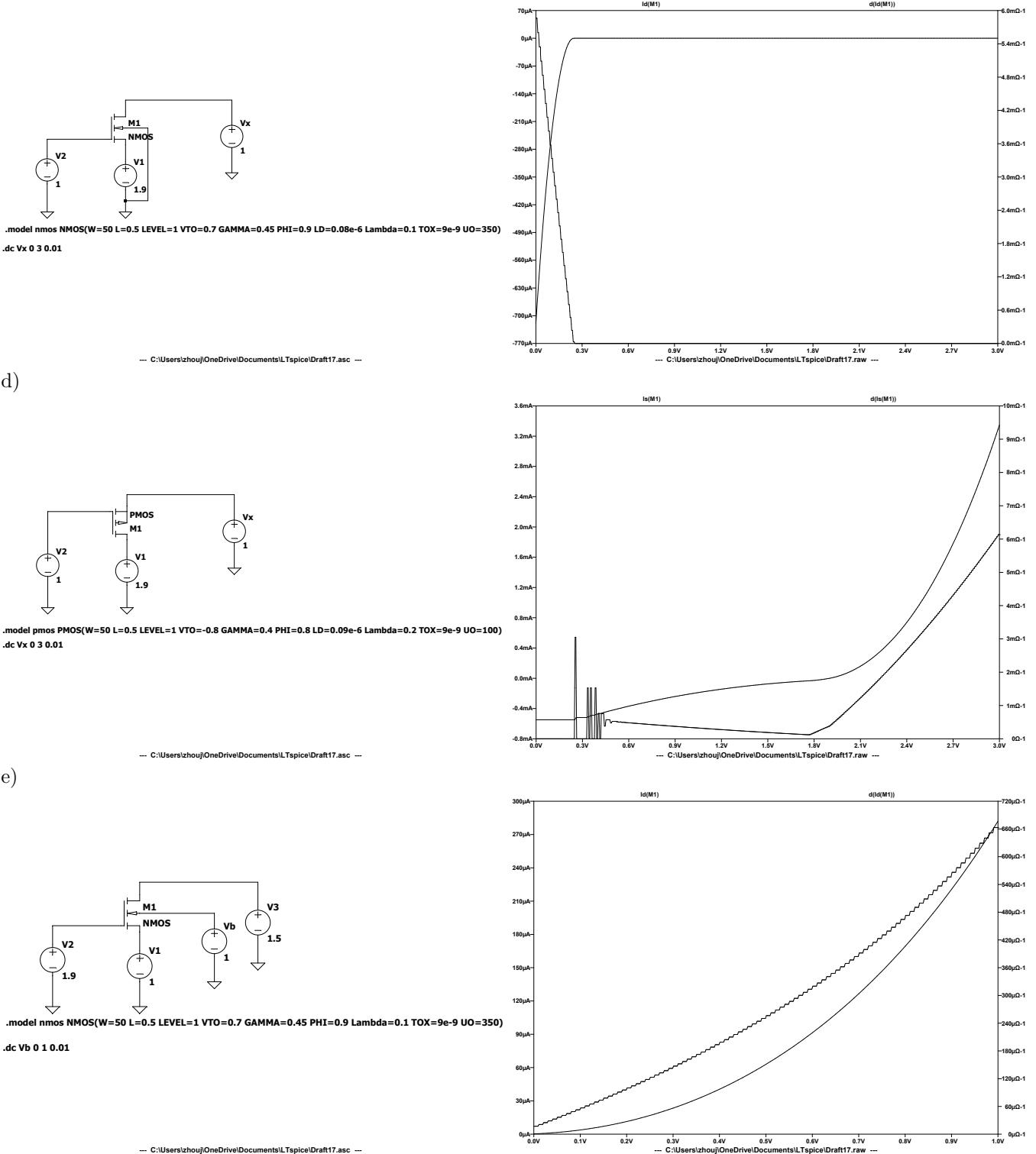
(a)



(b)



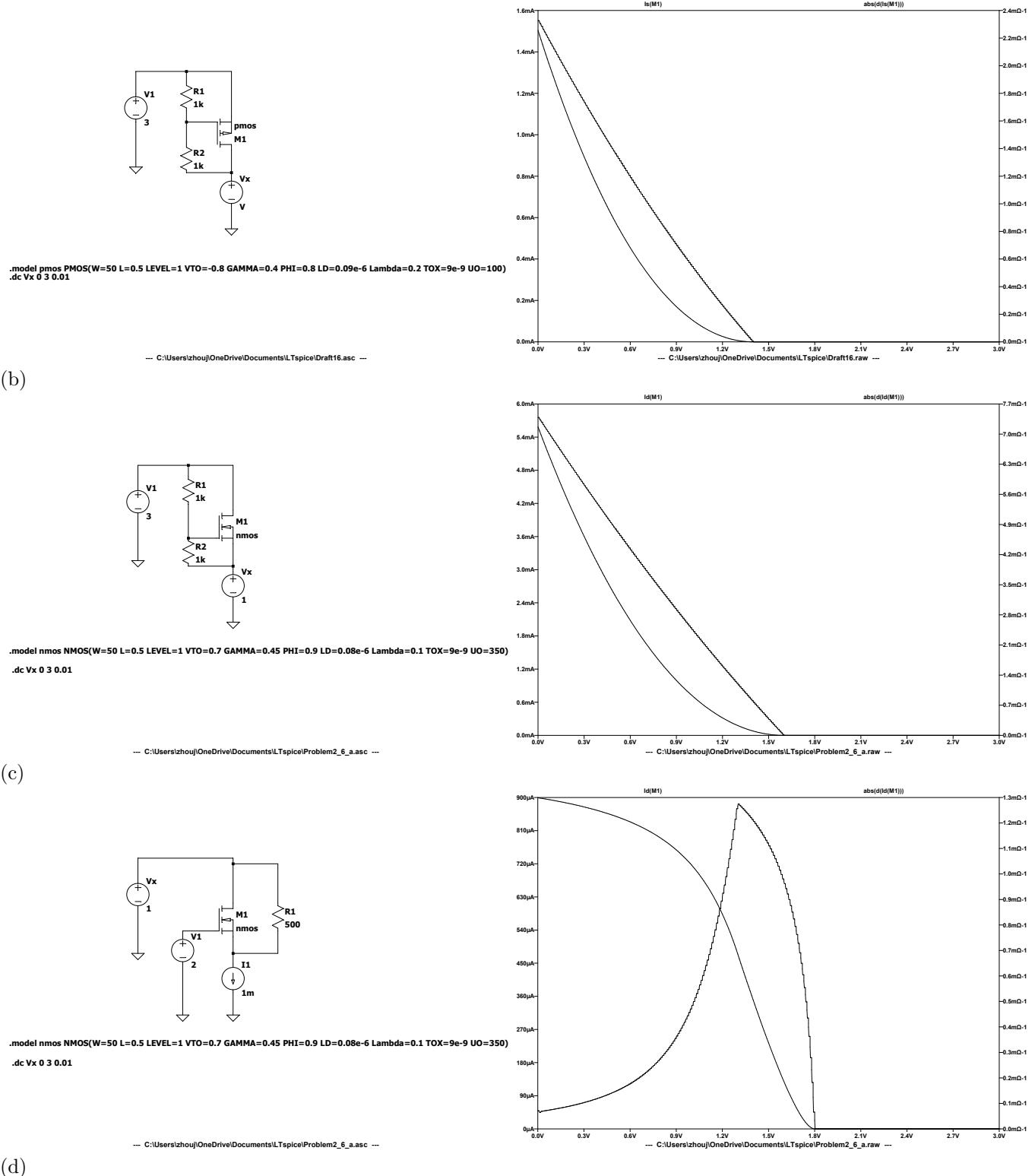
(c)

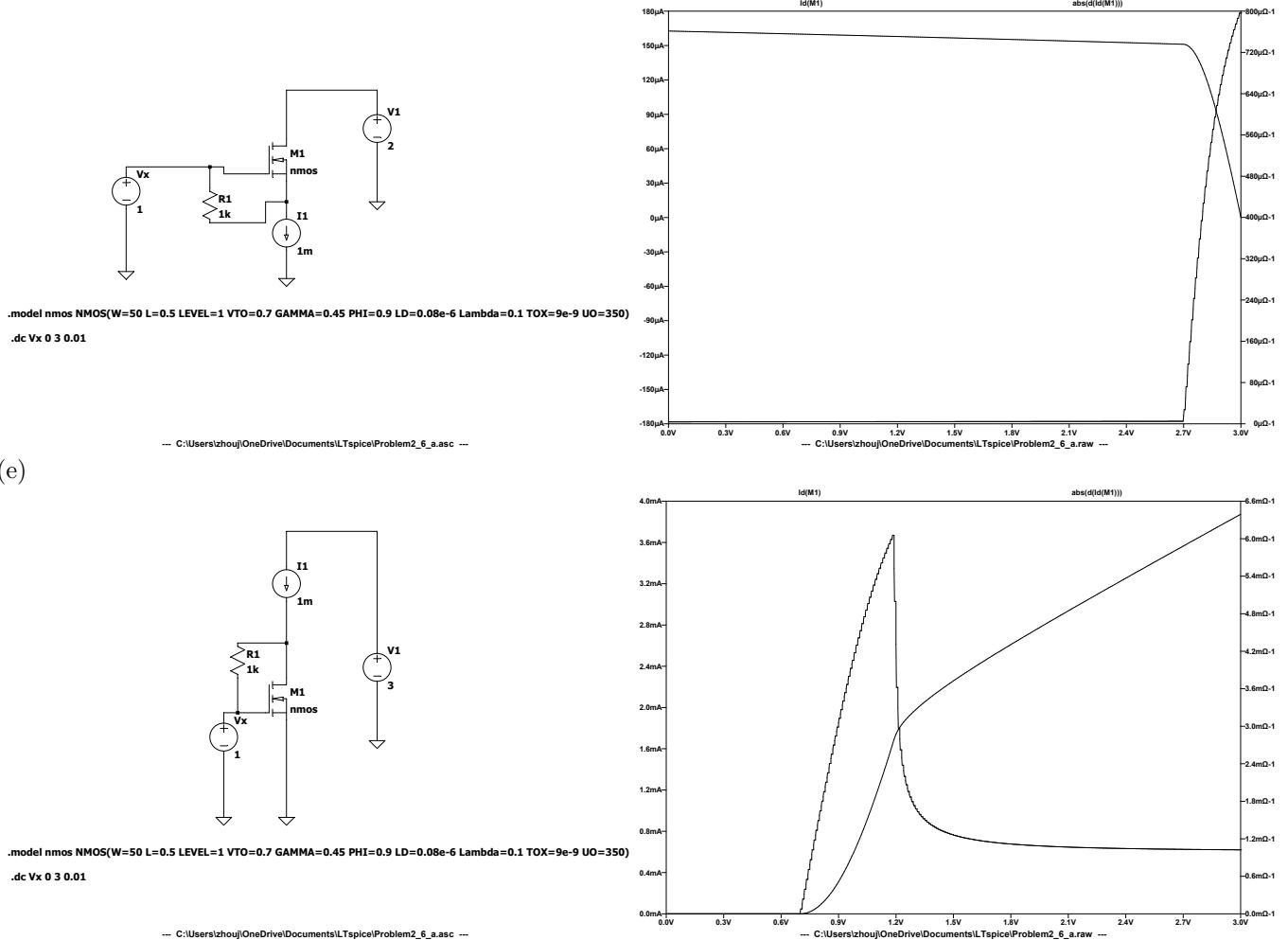


2.6

Sketch I_x and the transconductance of the transistor as a function of V_x for each circuit in Fig.2.48 as V_x varies from 0 to V_{DD} .

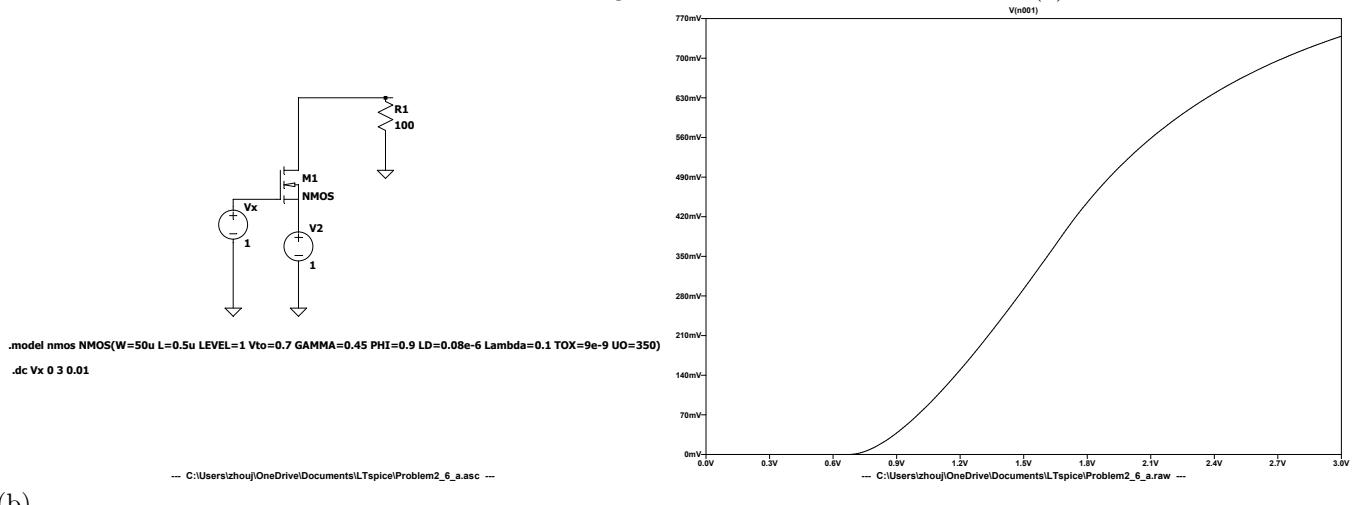
(a)

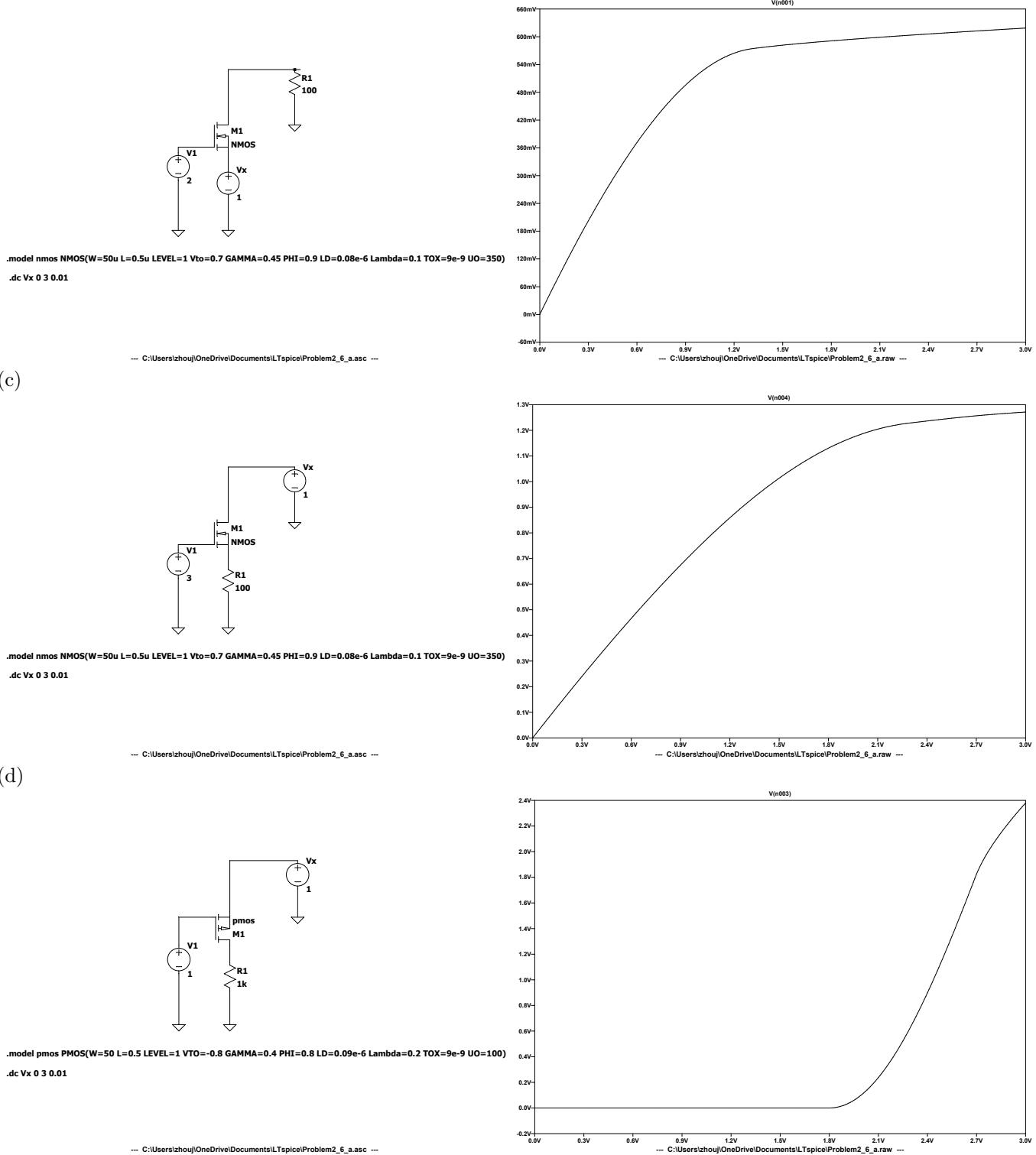




2.7

Sketch V_{out} as a function of V_{in} for each circuit in Fig.2.49 as V_{in} varies from 0 to V_{DD} . (a)

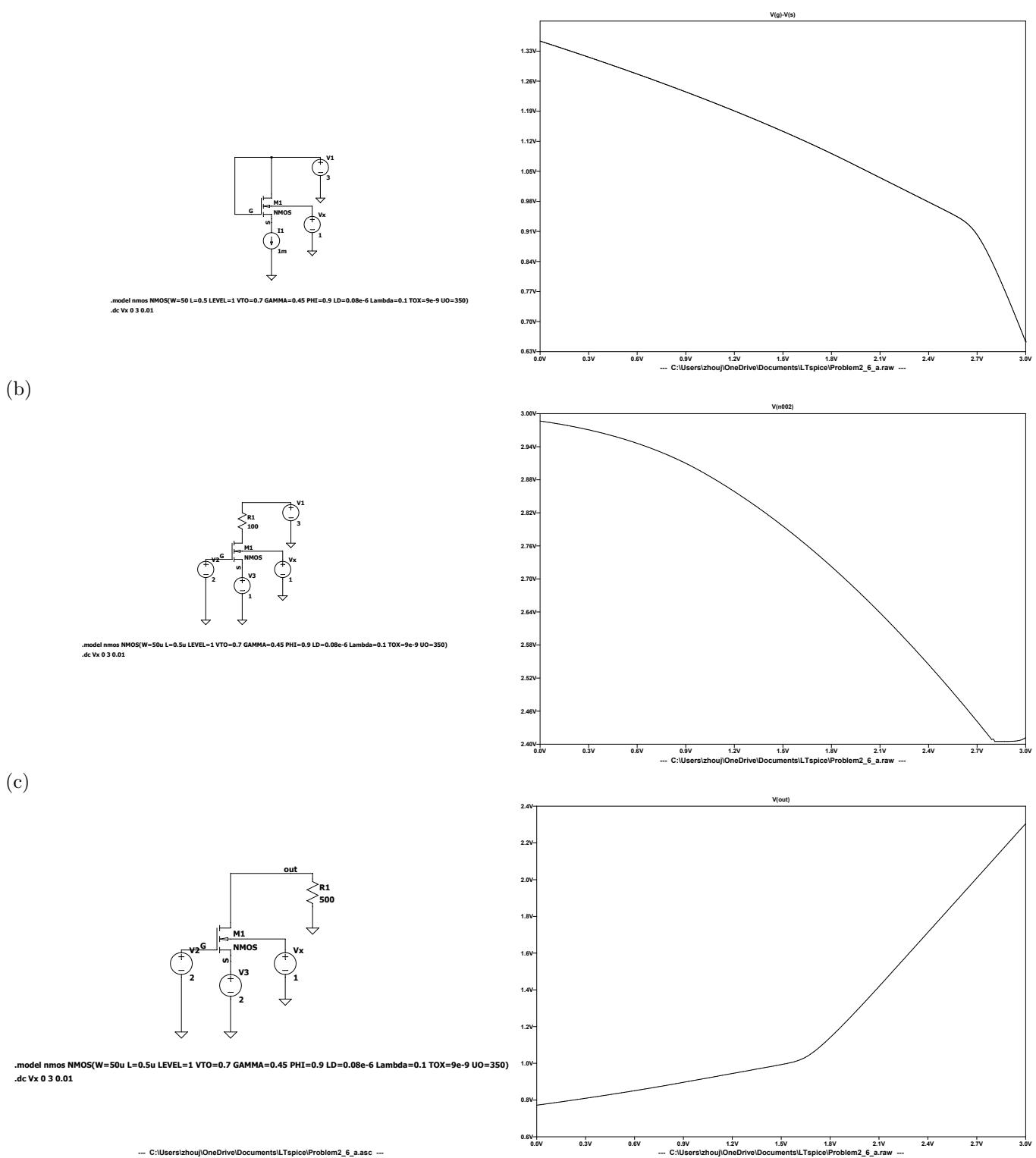




2.8

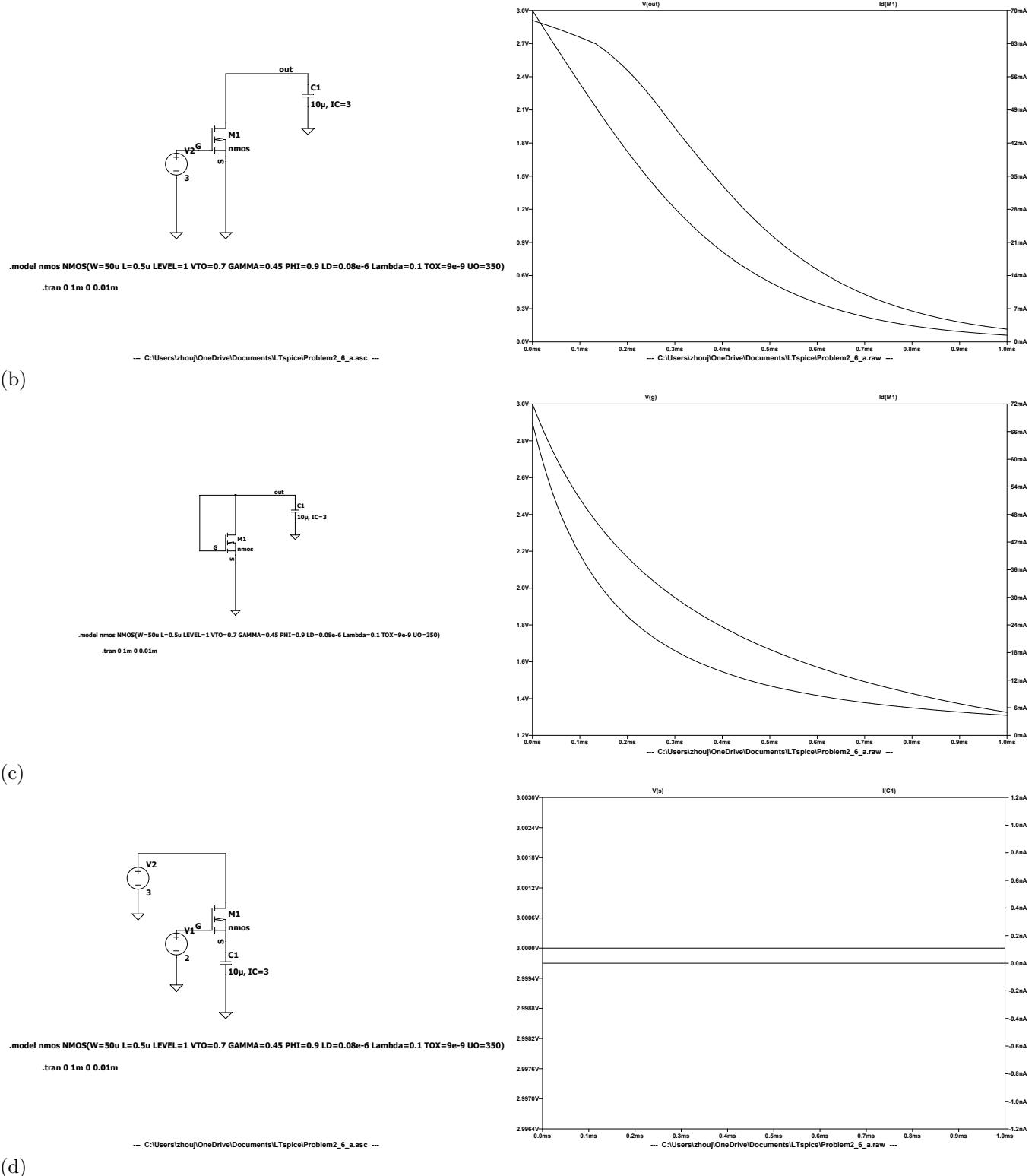
Sketch V_{out} as a function of V_{in} for each circuit in Fig.2.50 as V_{in} varies from 0 to V_{DD} .

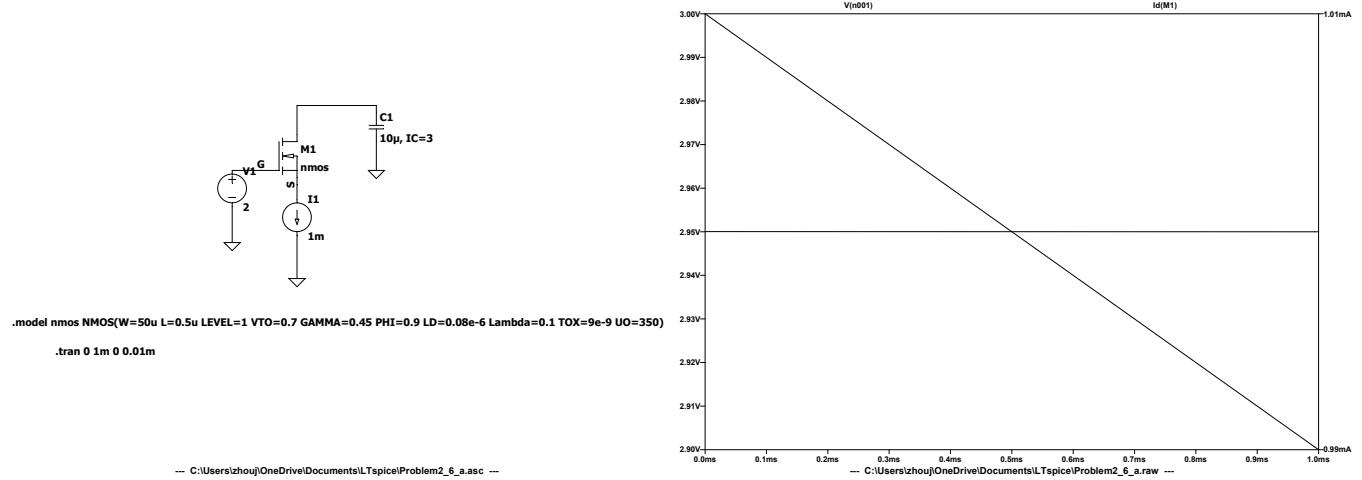
(a)



2.9

Sketch V_X and I_X as a function of time for each circuit in Fig.2.51. The initial voltage of C_1 is equal to 3V. In part (e), assume that the switch turns off at $t = 0$. (a)

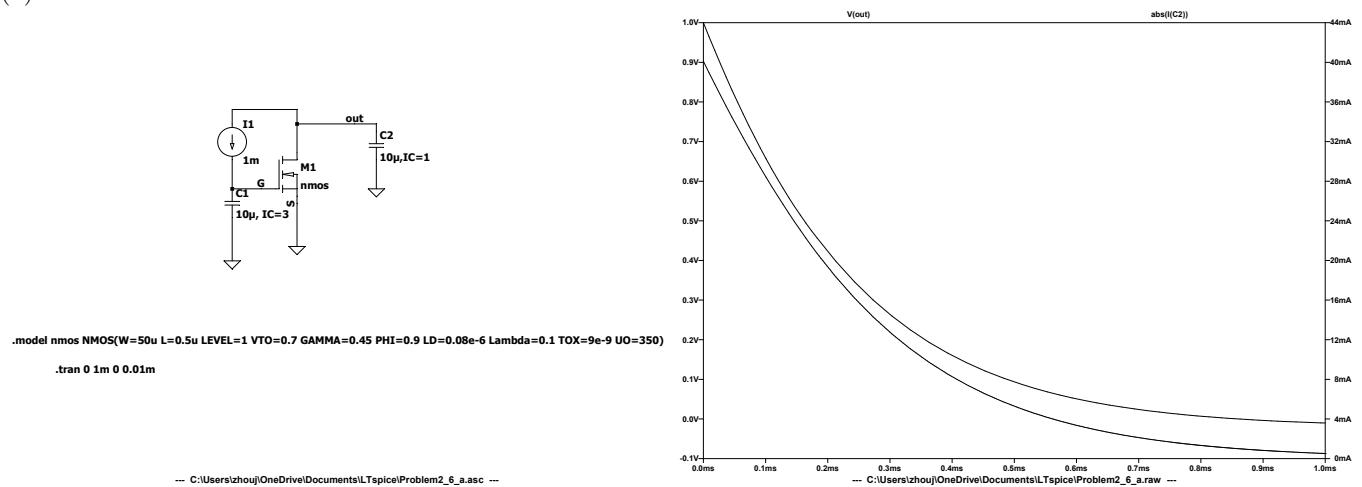




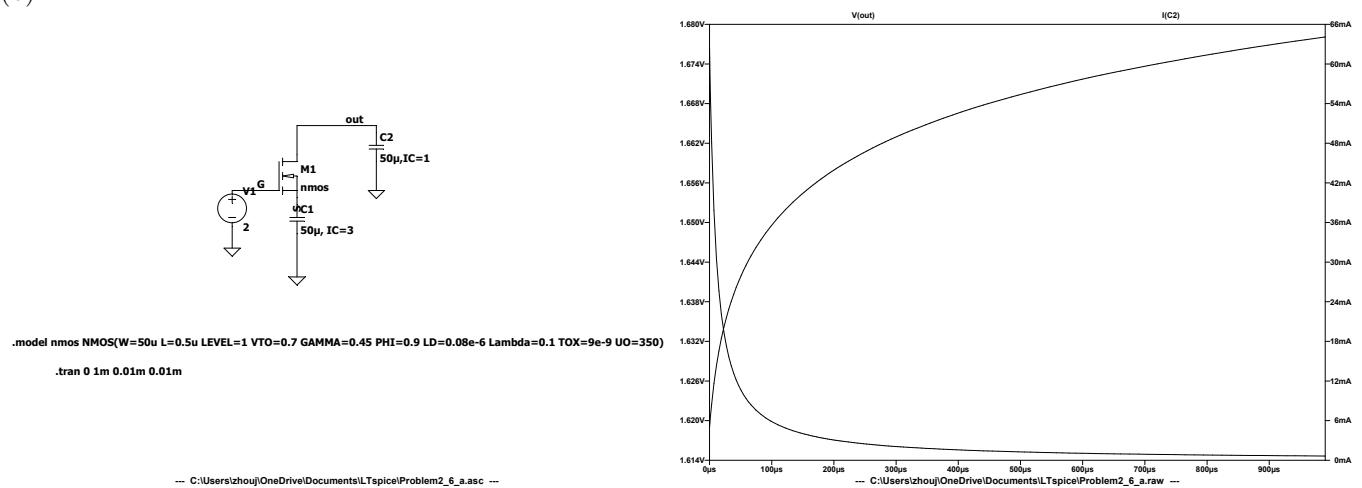
2.10

Sketch V_X and I_X as a function of time for each circuit in Fig.2.52. The initial voltage of each capacitor is shown, $C1 = 1V$, $C2 = 3V$.

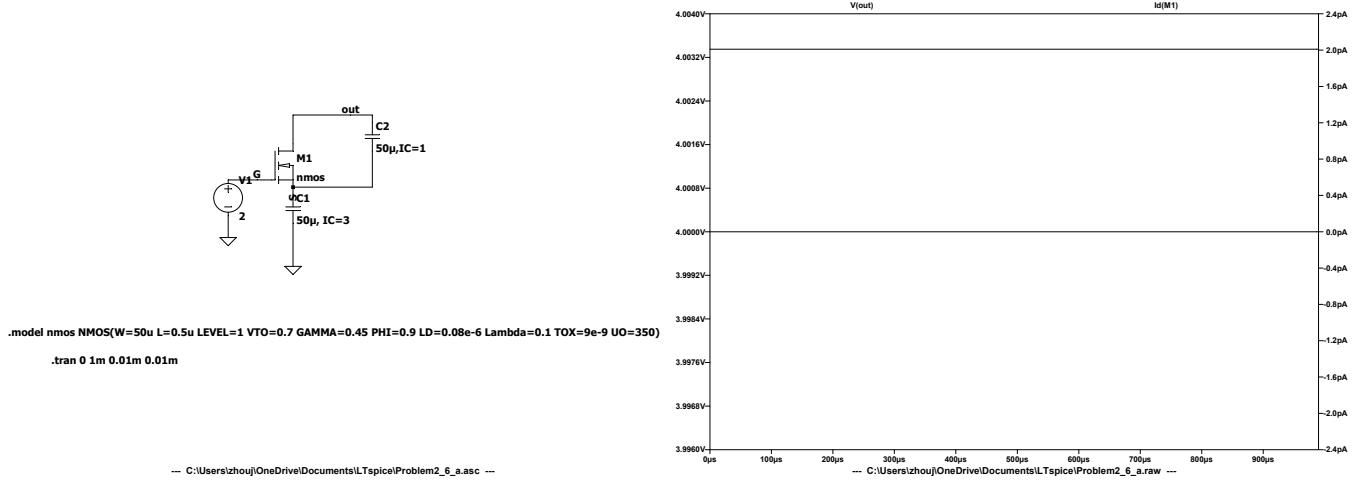
(a)



(b)



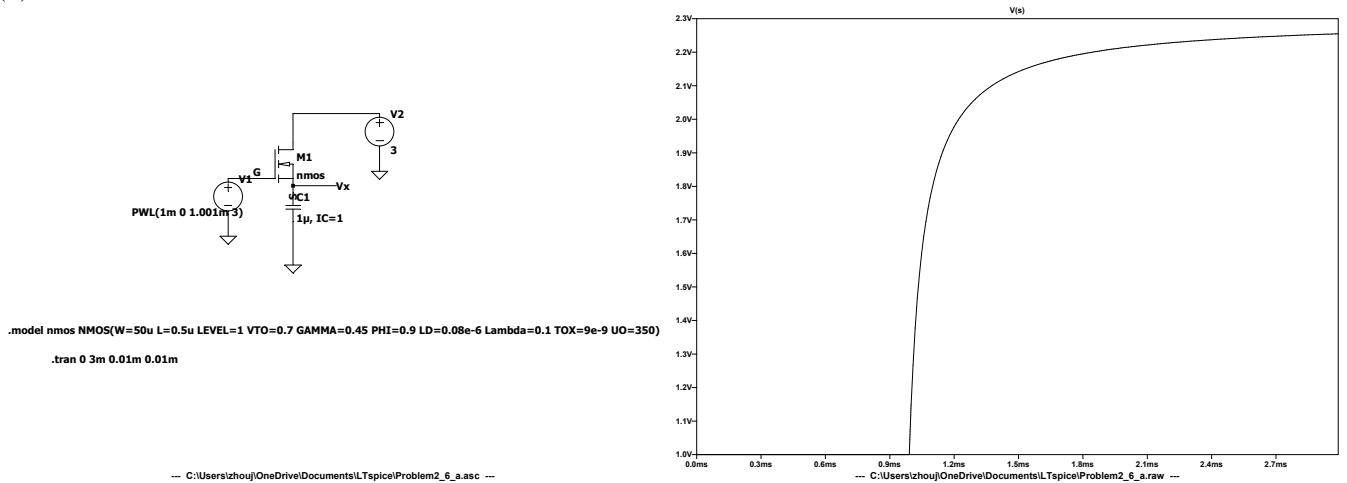
(c)



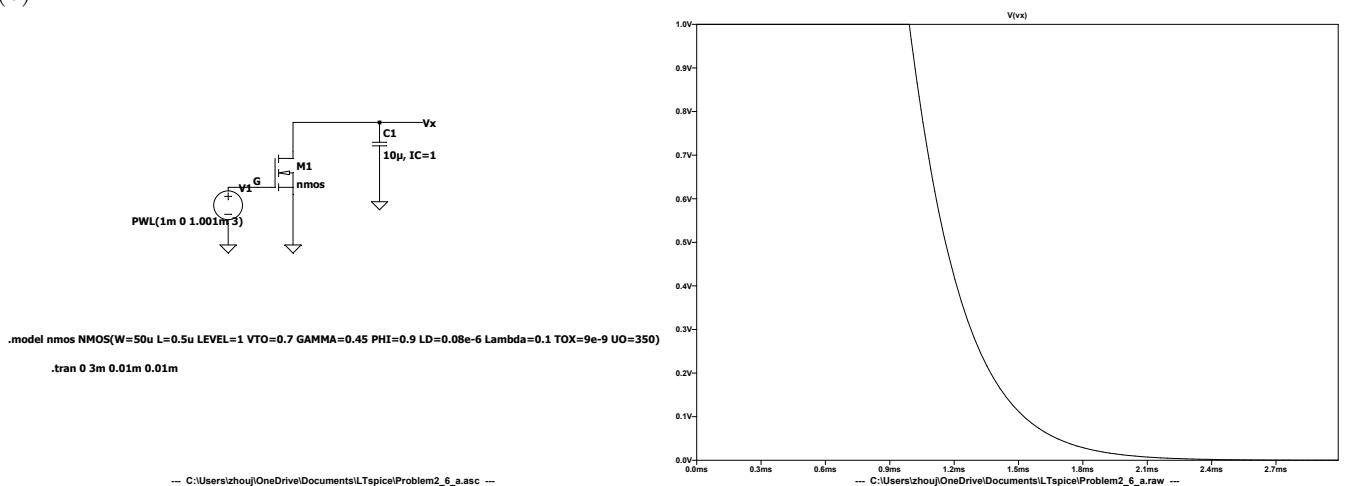
2.11

Sketch V_X as a function of time for each circuit in Fig.2.53. The initial voltage of each capacitor is shown.

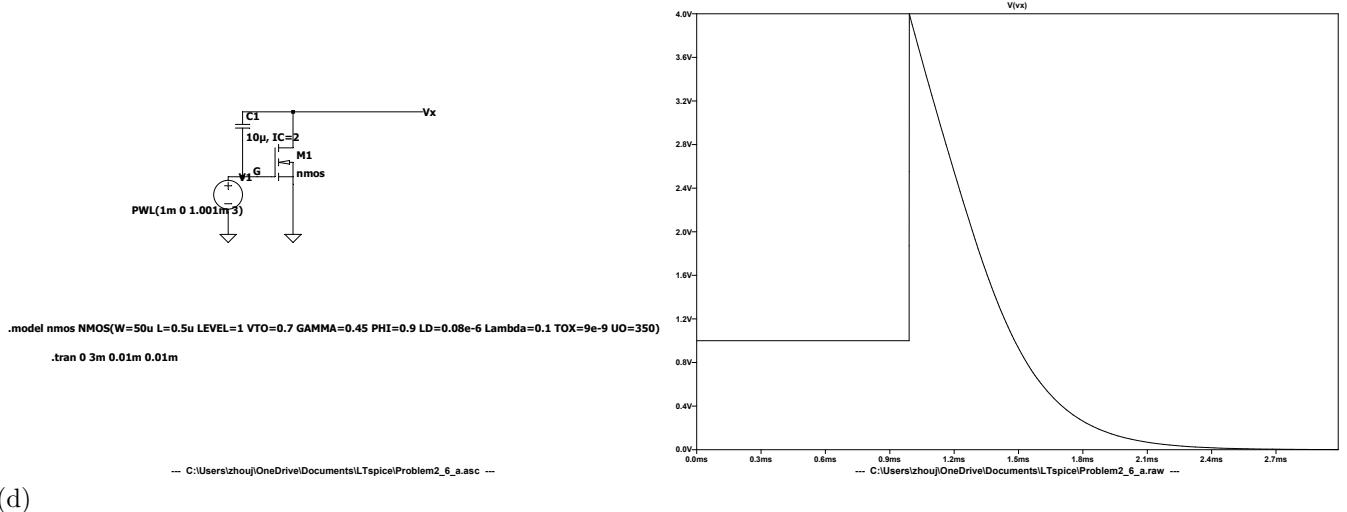
(a)



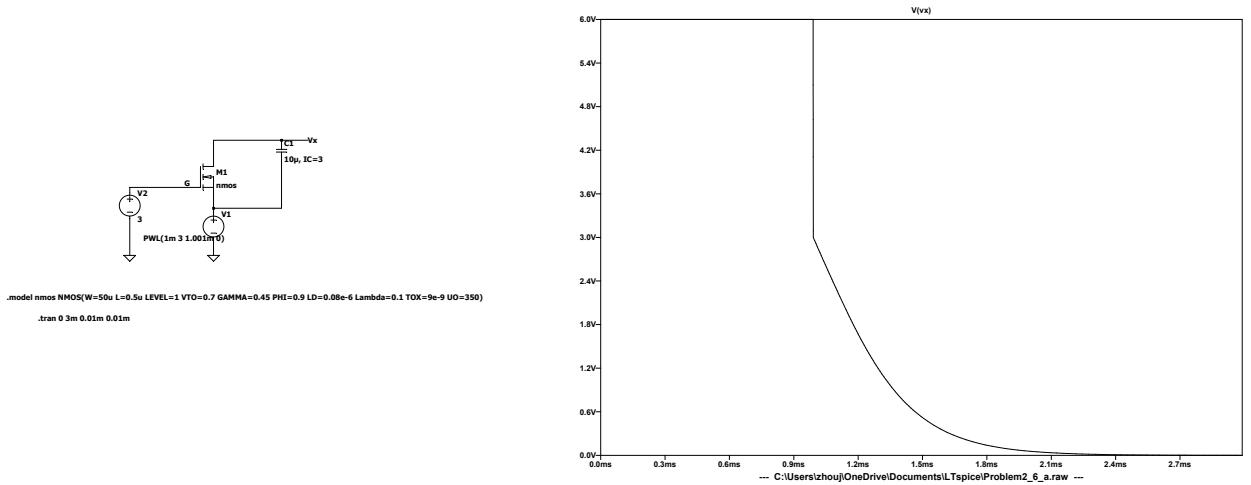
(b)



(c)



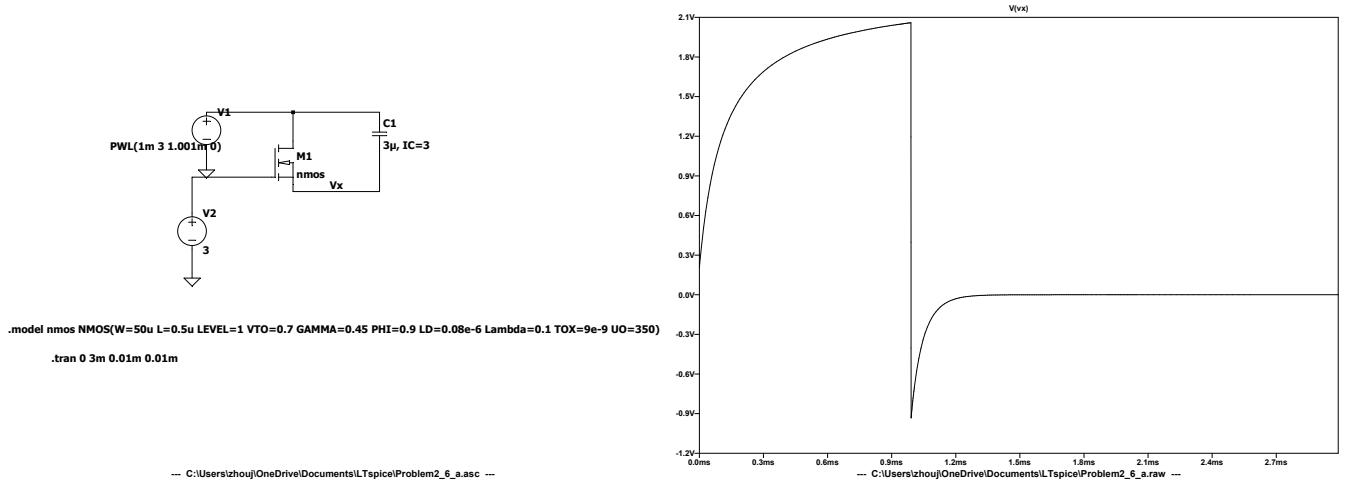
(d)



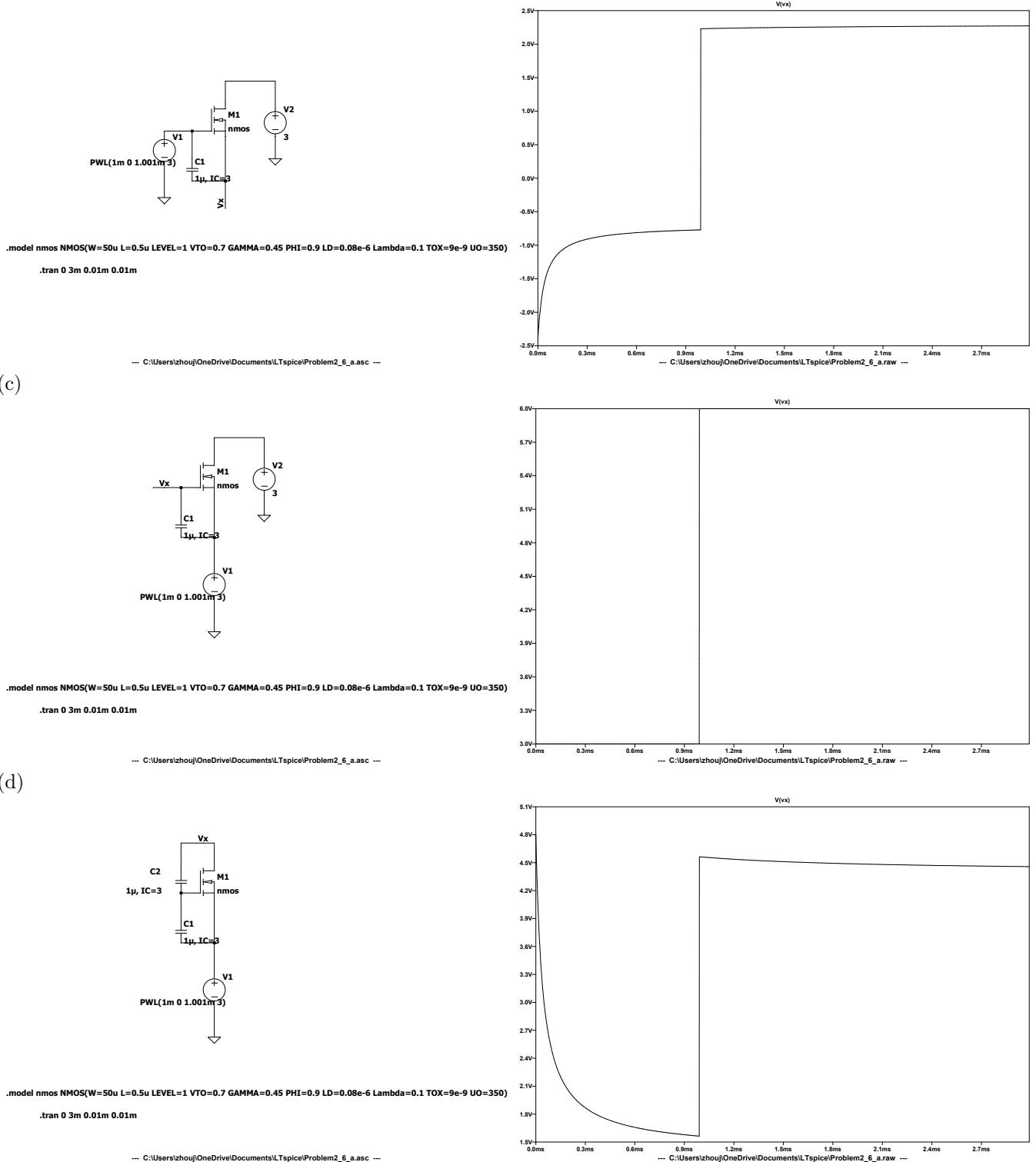
2.12

Sketch V_X as a function of time for each circuit in Fig.2.54. The initial voltage of each capacitor is shown.

(a)



(b)

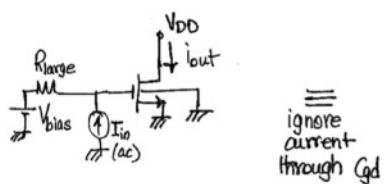


2.13

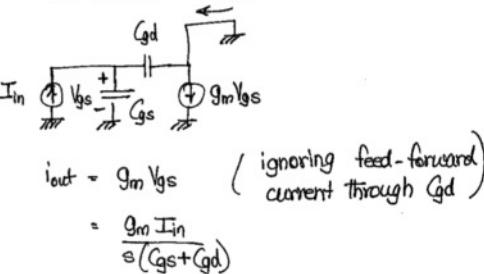
The transit frequency, f_T , of a MOSFET is defined as the frequency at which the small- signal current gain of the device drops to unity while the source and drain terminals are held at ac ground.

(a) Prove that $f_T = \frac{g_m}{2\pi(C_{GD} + C_{GS})}$. Note that f_T does not include the effect of the S/D junction capacitance.

f_T : Unity Current-Gain Frequency

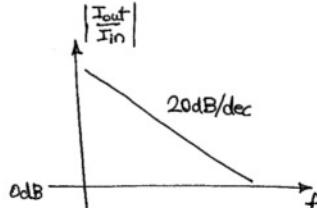


This is a measure of the speed of the MOSFET

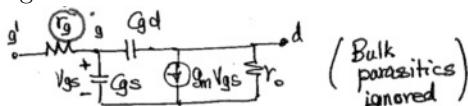


$$\left| \frac{I_{out}}{I_{in}} \right| = \frac{g_m}{2\pi f (C_{gs} + C_{gd})} \quad . \quad \text{Setting } \left| \frac{I_{out}}{I_{in}} \right| = 1 \Rightarrow f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

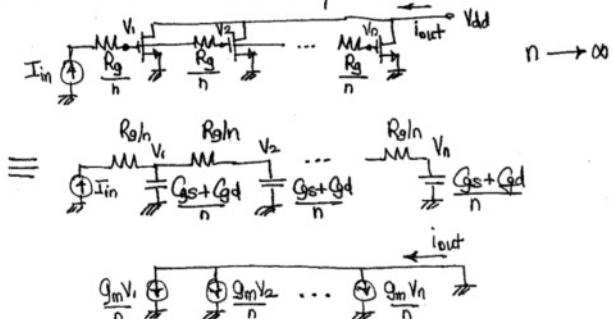
$$\left| \frac{I_{out}}{I_{in}} \right| = \frac{f_T}{f} \quad \text{in general}$$



- (b) Suppose the gate resistance, R_G is significant and the device is modeled as a distributed set of n transistors, each with a gate resistance equal to R_G/n . Prove that the f_T of the device is independent of R_G and still equal to the value given above.



let us assume that f_T is the important metric...



$$i_{out} = \frac{g_m}{n} (V_1 + V_2 + \dots + V_n) \quad I_{in} = s(C_{gs} + C_{gd}) \cdot \frac{1}{n} (V_1 + V_2 + \dots + V_n)$$

$$\therefore \frac{I_{out}}{I_{in}} = \frac{g_m}{s(C_{gs} + C_{gd})} \quad \text{and} \quad f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

Distributed Gate Resistance does not impact f_T

- (c) For a given bias current, the minimum allowable drain-source voltage for operation in saturation can be reduced only by increasing the width and hence the capacitance of the transistor. Using square-law characteristics, prove that $f_T = \frac{\mu_n}{2\pi} \frac{V_{GS} - V_{TH}}{L^2}$.

This relation indicates how the speed is limited as a device is designed to operate with lower supply voltages.

$$f_T = \frac{g_m}{2\pi(C_{GD} + C_{GS})} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \times \frac{1}{2\pi(C_{GD} + C_{GS})}$$

$$= \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \times \frac{1}{2\pi \times W L C_{ox}} = \frac{\mu_n}{2\pi} \frac{V_{GS} - V_{TH}}{L^2}$$

2.14

Calculate the f_T of a MOS device in the subthreshold region and compare the result with that obtained in Prob.2.13.

$$I_D = I_0 \exp \frac{V_{GS}}{\xi V_T}$$

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \frac{I_0}{\xi V_T} \exp \frac{V_{GS}}{\xi V_T}$$

$$f_T = \frac{g_m}{2\pi(C_{GD}+C_{GS})} = \frac{I_0}{\xi V_T} \exp \frac{V_{GS}}{\xi V_T} \frac{1}{2\pi \times 2WC_{ov}}$$

2.15

For a saturated NMOS device having $W = 50\mu\text{m}$ and $L = 0.5\mu\text{m}$, calculate all the capacitances. Assume that the minimum(lateral) dimension of the S/D areas is $1.5\mu\text{m}$ and that the device is folded as shown in Fig.2.33(b). What is the f_T if the drain current is 1mA.

$$C_{DB} = \frac{W}{2} E C_j + 2(\frac{W}{2} + E) C_{jsw}$$

$$C_{SB} = W E C_j + 2(W + 2E) C_{jsw}$$

$$C_{gs} = \frac{2}{3} W L C_{ox} + W C_{ov}$$

$$C_{gd} = W C_{ov}$$

$$f_T = \frac{g_m}{2\pi(C_{GD}+C_{GS})}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

2.16

Consider the structure shown in *Fig.2.55*. Determine I_D , as a function of V_{GS} and V_{DS} , and prove that the structure can be viewed as a single transistor having an aspect ratio $W/(2L)$. Assume that $\lambda = \gamma = 0$.

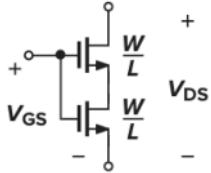


Figure 2.55

(1). $V_{GS} < V_{TH}$, $I_D = 0$;

(2). $V_{GS} > V_{TH}$, V_X (the node between two transistor) $< V_{GS} - V_{TH}$ because otherwise there is no current flow from top. M1(the lower one) is in linear region.

a. $V_{DS} > V_{GS} - V_{TH}$, M2 is in saturation region. $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_X - V_X^2] = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_X - V_{TH})^2$, and we could get $V_X = (1 - \frac{\sqrt{2}}{2})(V_{GS} - V_{TH})$. $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2$.

b. $V_{DS} < V_{GS} - V_{TH}$, M2 is in linear region. $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_X - V_X^2] = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH} - V_X)(V_{DS} - V_X) - (V_{DS} - V_X)^2]$.

And we could get $V_X = V_{GS} - V_{TH} - \sqrt{(V_{GS} - V_{TH})^2 - (V_{GS} - V_{TH})V_{DS} + 0.5V_{DS}^2}$. $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2$.

2.17

For an NMOS device opearting in saturation, plot W/L versus $V_{GS} - V_{TH}$ if (a) I_D is constant, and (b) g_m is constant.

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})$$

2.18

Explain why the structures shown in Fig.2.56 cannot operate as current sources even though the transistors are in saturation.

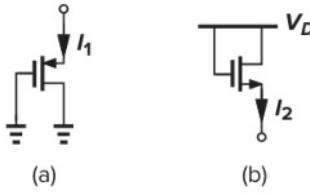


Figure 2.56

Because the output impedance for those two transistors are $\frac{1}{g_m} || r_o$, and $r_o \gg \frac{1}{g_m}$. The output impedance is close to $\frac{1}{g_m}$, which is pretty small and absorbs large amount of current.

2.19

Considering the body effect as "back-gate effect", explain intuitively why γ is directly proportional to $\sqrt{N_{sub}}$ and inversely proportional to C_{ox} .

The substrate doping N_{sub} controls the strength of the electric field needed to invert the surface (i.e., create a conducting channel). A higher N_{sub} means the channel requires a stronger field to invert, because more negative charges are present in the depletion region.

C_{ox} reflects how strongly the gate controls the channel (via the gate oxide). A higher C_{ox} (thinner oxide) means the gate has more control, so it can better overcome the influence of the body — i.e., the body effect is weaker.

2.20

A "ring" MOS structure is shown in Fig.2.57. Explain how the device operates and estimate its equivalent aspect ratio. Compare the drain junction capacitance of this structure with that of the devices shown in Fig.2.33.

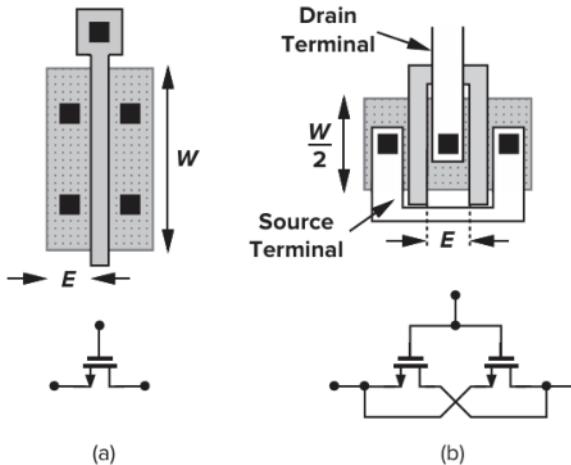


Figure 2.33

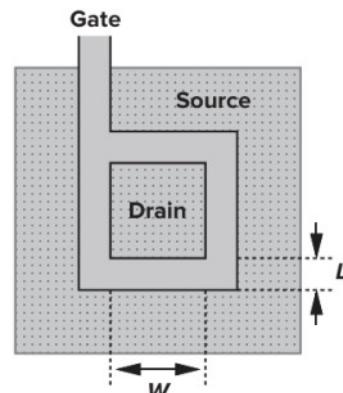


Figure 2.57

$$\text{Aspect ratio} = 4W/L.$$

$$C_{DB} = W^2 C_j + 4WC_{jsw}.$$

2.21

Suppose we have received an NMOS transistor in a package with four unmarked pins. Describe the minimum number of dc measurement steps using an ohmmeter that is necessary to determine the gate, source/drain, and bulk terminals of the device.

1. Identify gate (isolated pin).
2. Identify bulk (diode junction behavior with source/drain).
3. Distinguish source/drain by checking connection to bulk or assigning arbitrarily.

2.22

Repeat Prob.2.21 if the type of the device(NFET or PFET) is not known.

Same as before. For NMOS: P-type bulk, junctions to N-type source/drain \rightarrow diode conducts when positive lead is on source/drain. PMOS: N-type bulk, junctions to P-type source/drain \rightarrow diode conducts when positive lead is on bulk.

2.23

For an NMOS transistor, the threshold voltage is known, but $\mu_n C_{ox}$ and W/L are not. Assume that $\lambda = \gamma = 0$. If we cannot measure C_{ox} independently, is it possible to devise a sequence of dc measurement tests to determine $\mu_n C_{ox}$ and W/L ? What if we have two transistors and we know that one has a twice the aspect ratio of the other?

No, it is impossible to find $\mu_n C_{ox}$ and W/L no matter using one or two transistors.

2.24

Sketch I_X versus V_X for each of the composite structures shown in Fig.2.58 with V_G as a parameter. Also, sketch the equivalent transconductance. Assume that $\lambda = \gamma = 0$.

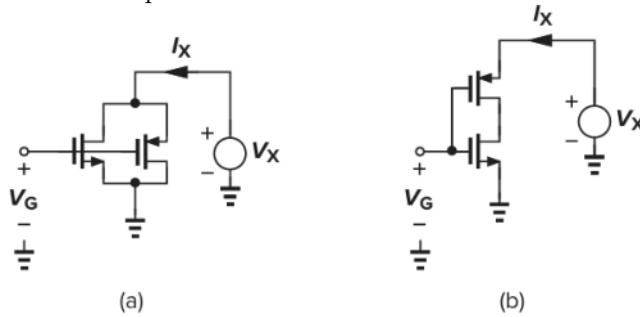
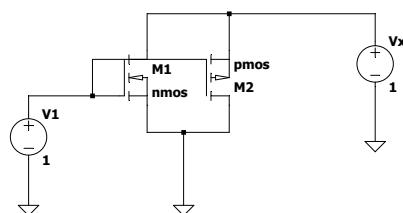


Figure 2.58

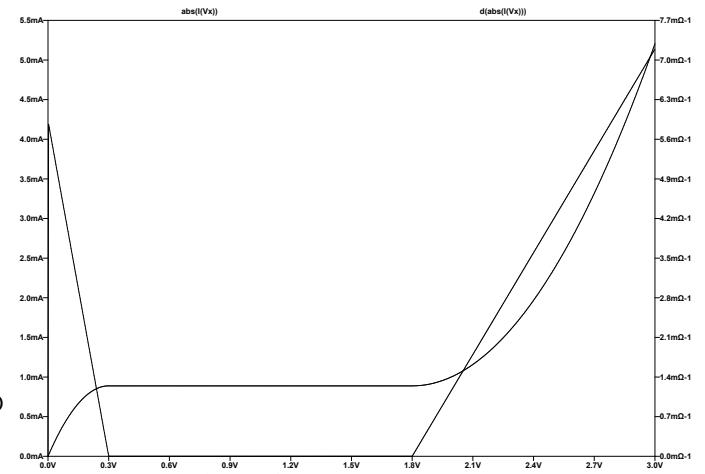
(a)

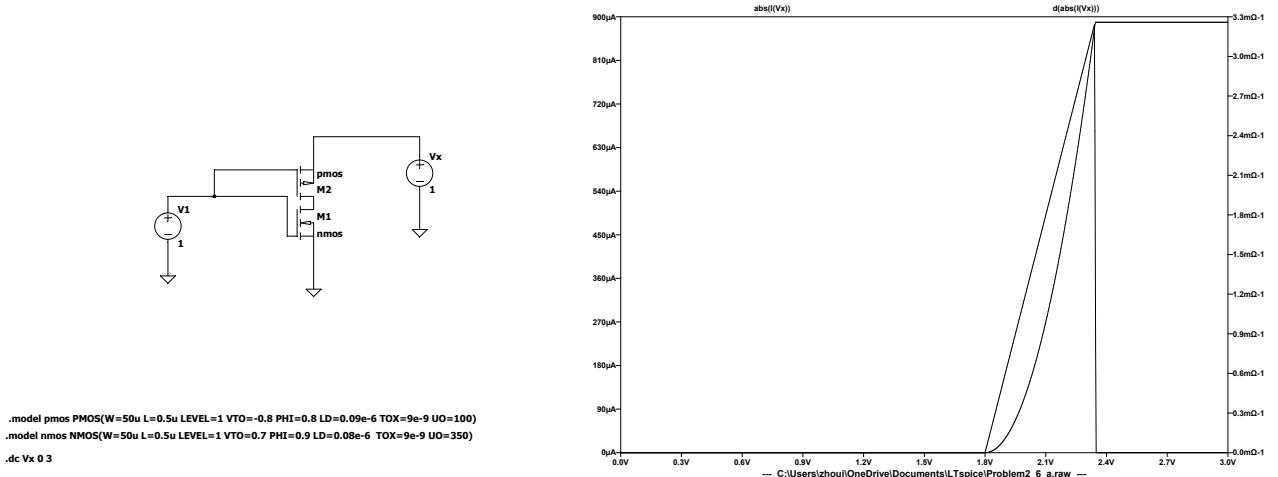


```
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 PHI=0.8 LD=0.09e-6 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 PHI=0.9 LD=0.08e-6 TOX=9e-9 UO=350)

.dc Vx 0 3
```

(b)





2.25

An NMOS current source with $I_D = 0.5mA$ must operate with drain-source voltages as low as 0.4V. If the minimum required output impedance is $20\text{k}\Omega$, determine the width and length of the device. Calculate the gate-source, gate-drain, and drain-substrate capacitance if the device is folded as in Fig.2.33 and $E = 3\mu\text{m}$.

$r_o = \frac{1}{\lambda I_D} = 20k$, $\lambda = 0.1$ Suppose $L = 0.5\mu\text{m}$, from $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{ov})^2$, we could get $W = 23.2\mu\text{m}$.

$$C_{DB} = \frac{W}{2} E C_j + 2(\frac{W}{2} + E) C_{jsw}$$

$$C_{SB} = W E C_j + 2(W + 2E) C_{jsw}$$

$$C_{gs} = \frac{2}{3} W L C_{ox} + W C_{ov}$$

$$C_{gd} = W C_{ov}$$

2.26

Consider the circuit shown in Fig.2.59, where the initial voltage at node X is equal to V_{DD} . Assuming that $\lambda = \gamma = 0$ and neglecting other capacitances, plot V_X and V_Y versus time if (a) V_{in} is a positive step with amplitude $V_0 > V_{TH}$, and (b) V_{in} is a negative step with amplitude $V_0 = V_{TH}$.

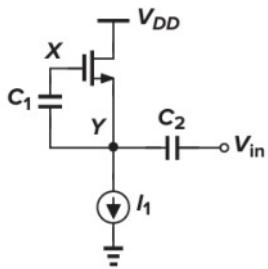
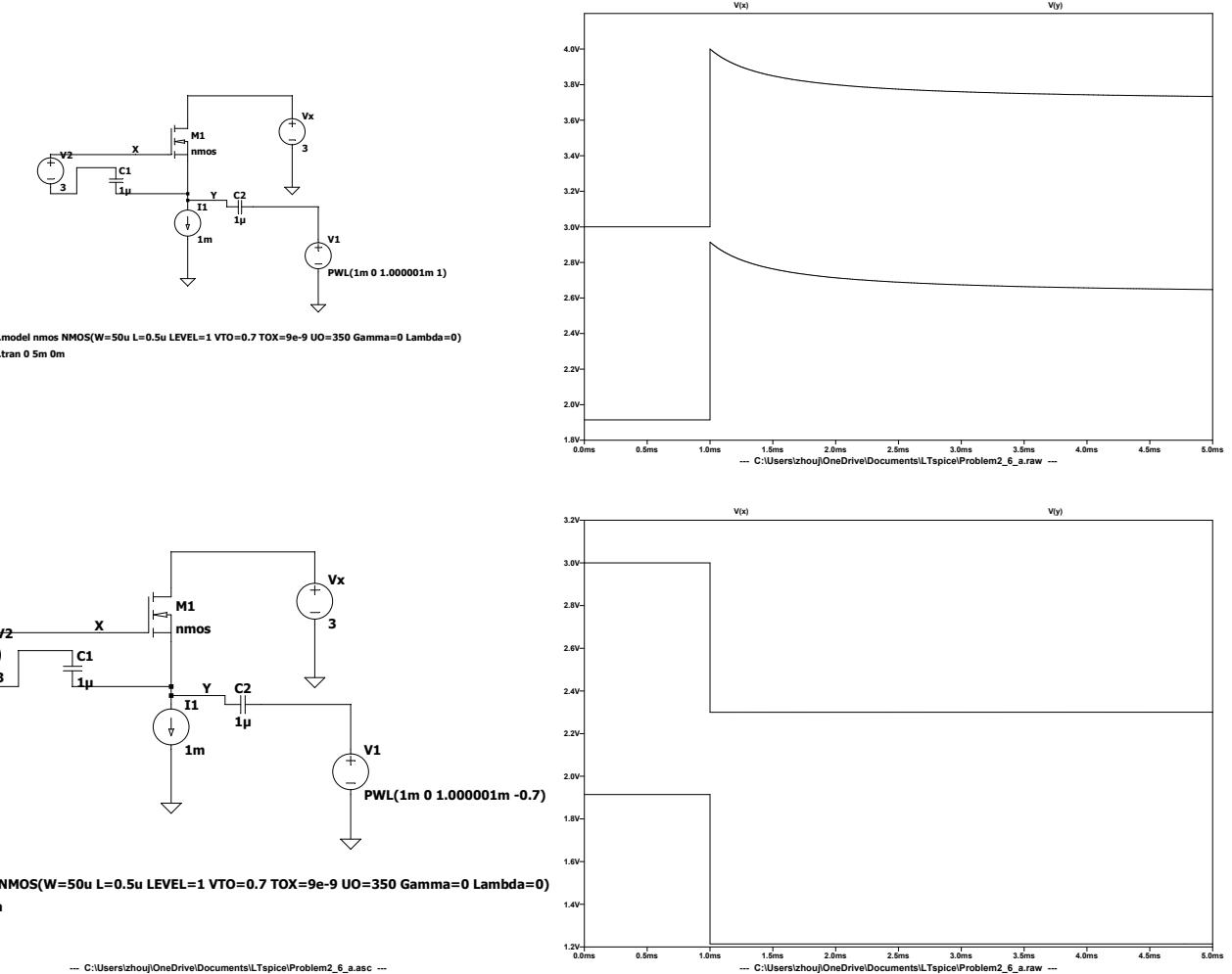
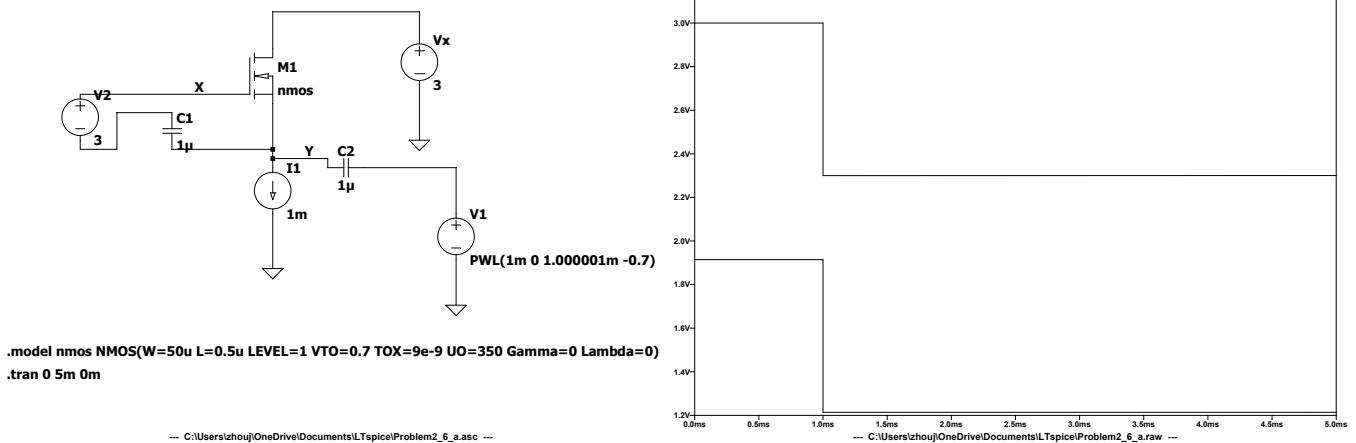


Figure 2.59

(a)



(b)



2.27

An NMOS device operating in the subthreshold region has a ξ of 1.5. What variation in V_{GS} results in a tenfold change in I_D ? If $I_D = 10\mu A$, what is g_m ?

$$I_D = I_0 e^{\frac{V_{GS}}{\xi V_T}} = I_0 e^{\frac{V_{GS} + \delta V}{\xi V_T}}, 10 = e^{\frac{\delta V}{\xi V_T}}$$

$$\delta V = 89.8mV$$

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = I_D \times \frac{1}{\delta V_T} = 0.256mS$$

2.28

Consider an NMOS device with $V_G = 1.5V$ and $V_S = 0$. Explain what happens if we continually decrease V_D below zero or increase V_{sub} above zero.

The drain and source terminal will switch if V_D is below zero. And the NMOS will not work properly since there is current flow through substrate to source if we increase V_{sub} above 0.

2.29

Consider the arrangement shown in Figure 2.60. Explain what happens to the pinch-off point as V_G increases.

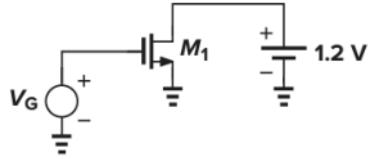


Figure 2.60

When $V_G < 0.7V$, there is no pinch-off point since it is in cutoff region.

When $0.7V < V_G < 1.9V$, it is in saturation region, and the pinch-off point will move towards Drain terminal as V_G increases.

When $V_G > 1.9V$, there is no pinch-off point since the mos is in linear/triode region.

2.30

From Fig.2.20, plot I_D vs. $V_{GS} - V_{TH}$ if W/L is constant, $V_{GS} - V_{TH}$ vs. I_D if W/L is constant, and W/L vs. $V_{GS} - V_{TH}$ if I_D is constant.

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

2.31

Plotted in Fig.2.61 are the characteristics of a square-law NMOS device with $W/L_{drawn} = 5\mu m/40nm$ and $t_{ox} = 18A$. Here, V_{GS} is incremented in equal steps. Estimate μ_n , V_{TH} , λ and the V_{GS} steps.

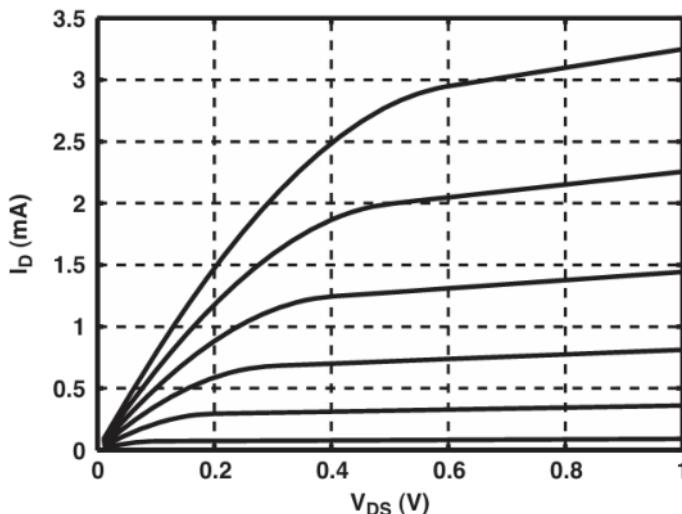


Figure 2.61

$$V_{DS} = V_{GS} - V_{TH}, \delta V_{DS} = \delta V_{GS} = 0.11V.$$

$$C_{ox} = 17.25fF/\mu m^2 \times 20/18 = 19.17fF/\mu m^2.$$

$$\mu_n = \frac{2I_D}{C_{ox} \frac{W}{L} V_{D,sat}^2} = 6.96 \times 10^{-3} m^2/V/s.$$

$$\text{In Saturation region: } \frac{\delta I_D}{\delta V_{DS}} = I_D \lambda, \lambda = \frac{0.3mA}{0.4V} \times \frac{1}{3mA} = 0.25V^{-1}.$$

3 Simple-Stage Amplifiers

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

3.1

For the circuit of Fig.3.13, calculate the small-signal voltage gain if $(W/L)_1 = 50/0.5$, $(W/L)_2 = 10/0.5$, and $I_{D1} = I_{D2} = 0.5mA$. What is the gain if M_2 is implemented as a diode-connected PMOS device (Fig.3.16)?

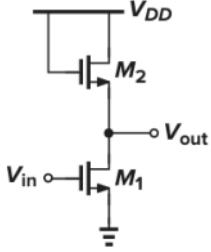


Figure 3.13 CS stage with diode-connected load.

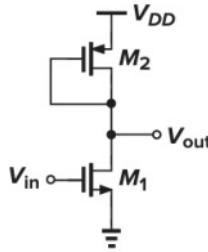


Figure 3.16 CS stage with diode-connected PMOS device.

$$(a) A_v = -G_M R_{out} = -g_{m1} \times \left(\frac{1}{g_{m2}} \parallel \frac{1}{g_{mb}} \right) = \frac{-g_{m1}}{g_{m2} \times (1 + \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}})} = -1.95$$

$$V_{SB} = V_{out}$$

$$\frac{g_{m1}}{g_{m2}} = \sqrt{\frac{(\frac{W}{L})_1}{(\frac{W}{L})_2}} = \sqrt{5}.$$

From equations $V_{th} = V_{th0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{|2\phi_F|})$ and $I_{D2} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_2(V_{DD} - V_{out} - V_{th})^2$, we can get $V_{out} = 1.47V$.

And we replace the V_{SB} in the A_V , we could get $A_V = -1.95$.

$$(b) A_v = -G_M R_{out} = -g_{m1} \times \frac{1}{g_{m2}} = \sqrt{\frac{\mu_n(\frac{W}{L})_1}{\mu_p(\frac{W}{L})_2}} = -\sqrt{\frac{350 \times 100}{100 \times 20}} = -4.18.$$

3.2

In the circuit of Fig.3.18, assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 50/2$, and $I_{D1} = I_{D2} = 0.5mA$ when both devices are in saturation. Recall that $\lambda \propto 1/L$.

(a) Calculate the small-signal voltage gain.

(b) Calculate the maximum output voltage swing while both devices are saturated.

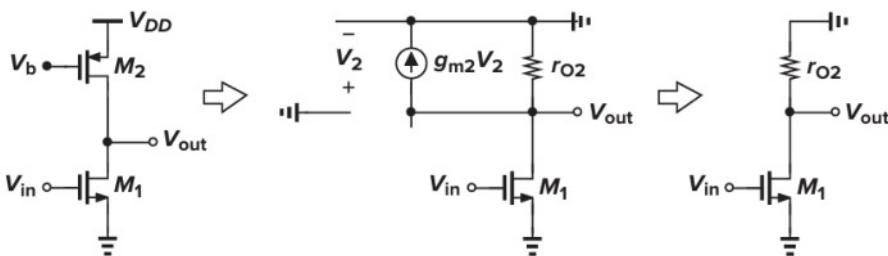


Figure 3.18 CS stage with current-source load.

$$(a) A_v = -g_{m1}(r_{o1} || r_{o2})$$

$$g_m = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_1 I_{D1}}$$

$$r_{o1} = \frac{1}{\lambda I_{D1}}$$

$$r_{o2} = \frac{1}{\lambda I_{D2}}$$

$$A_v = -48.8.$$

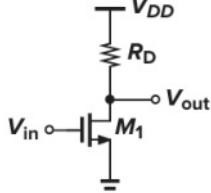
$$(b) V_{out,max} = V_b + |V_{th,p}|$$

And from $I_D = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_2(V_b - V_{DD} - V_{th,p})^2[1 + \lambda(V_{DD} - V_{out})]$, we could get $V_{out,max} = 2V$. And we could also get $V_{out,min} = V_{in} + V_{th,n} = 0.27V$.

3.3

In the circuit of Fig.3.4(a), assume that $(W/L)_1 = 50/0.5$, $R_D = 2k\Omega$, and $\lambda = 0$.

- (a) What is the small-signal gain if M_1 is in saturation and $I_D = 1mA$?
- (b) What input voltage places M_1 at the edge of the triode region? What is the small-signal gain under this condition?
- (c) What input voltage drives M_1 into the triode region by 50mV? What is the small-signal gain under that condition?



(a)

$$(a) A_v = -g_m R_D = -\sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_D} R_D = -10$$

(b) From $V_{out} = V_{in} - V_{th}$ and $\frac{V_{DD}-V_{out}}{R_D} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th})^2$, we could get $V_{in} = 1.137V$.

$$A_v = -g_m R_D = -\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th}) R_D = -11.7$$

(c) From $V_{out} = V_{in} - V_{th} - 50mV$ and $\frac{V_{DD}-V_{out}}{R_D} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} [2(V_{in} - V_{th})V_{out} - V_{out}^2]$, we can get $V_{in} = 1.144V$, $V_{out} = 0.394V$. $A_v = -G_m R_{out} = -g_{m1}(r_{o1}||R_D)$. $g_{m1} = \frac{\delta I_D}{\delta V_{in}} = \mu_n C_{ox} \frac{W}{L} V_{out}$, $r_{o1} = \frac{1}{g_{ds}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th} - V_{out})} = 1.49k\Omega$, $A_v = -4.31$.

3.4

Suppose the common-source stage of Fig.3.4(a) is to provide an output swing from 1V to 2.5V. Assume that $(W/L)_1 = 50/0.5$, $R_D = 2k\Omega$, and $\lambda = 0$.

- (a) Calculate the input voltages that yield $V_{out} = 1V$ and $V_{out} = 2.5V$.
- (b) Calculate the drain current and the transconductance of M_1 for both cases.
- (c) How much does the small-signal gain, $g_m R_D$, vary as the output goes from 1V to 2.5V? (Variation of small-signal gain can be viewed as nonlinearity).

$$(a) I_D = \frac{V_{DD}-V_{out}}{R_D} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)^2$$

When $V_{out} = 1V$, $V_{in} = 1.09V$. When $V_{out} = 2.5V$, $V_{in} = 0.893V$.

$$(b) I_D = \frac{V_{DD}-V_{out}}{R_D}, g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_D}$$

When $V_{out} = 1V$, $I_D = 1mA$, $g_m = 5.18mS$. When $V_{out} = 2.5V$, $I_D = 0.25mA$, $g_m = 2.59mS$.

(c) $V_{out} = 1V$, $g_m R_D = 10.4$. $V_{out} = 2.5V$, $g_m R_D = 5.18$.

3.5

Calculate the intrinsic gain of an NMOS device and a PMOS device operating in saturation with $W/L = 50/0.5$ and $|I_D| = 0.5mA$. Repeat these calculations if $W/L = 100/1$.

$$g_m r_o = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_D} \times \frac{1}{\lambda I_D} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1 \frac{1}{I_D}} \times \frac{1}{\lambda}$$

For $W/L = 50/0.5$, $A_{v,pmos} = 20$, $A_{v,nmos} = 73$.

For $W/L = 100/1$, as L double, $1/\lambda$ also double. $A_{v,pmos} = 40$, $A_{v,nmos} = 146$.

3.6

Assuming a constant L, plot the intrinsic gain of a saturated device versus the gate-source voltage if (a) the drain current is constant, (b) W is constant.

$$(a) A_v = g_m r_o = \frac{2I_D}{V_{GS}-V_{TH}} \times \frac{1}{\lambda I_D} = \frac{2}{(V_{GS}-V_{TH})\lambda}$$

$$(b) A_v = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \times \frac{2}{\lambda \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2} = \frac{2}{(V_{GS} - V_{TH}) \lambda}, \text{ the same as (a).}$$

3.7

Assuming a constant L, plot the intrinsic gain of a saturated device versus W/L if (a) the gate-source voltage is constant, (b) the drain current is constant.

$$(a) A_v = \frac{2}{(V_{GS} - V_{TH}) \lambda}, \text{ which is a constant.}$$

$$(b) A_v = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_D} \times \frac{1}{\lambda I_D} = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_1 \frac{1}{I_D}} \times \frac{1}{\lambda}.$$

3.8

An NMOS transistor with $W/L = 50/0.5$ is biased with $V_G = +1.2V$ and $V_S = 0$. The drain voltage is varied from 0 to 3V.

(a) Assuming the bulk voltage is zero, plot the intrinsic gain versus V_{DS} .

(b) Repeat part (a) for a bulk voltage of -1V.

$$(a) \text{ In Saturation region, } V_{DS} > V_{GS} - V_{th} = 0.5V. A_v = g_m r_o = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})(1 + \lambda V_{DS}) \frac{2}{\lambda \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2} = \frac{2(1 + \lambda V_{DS})}{\lambda(V_{GS} - V_{th})} = 40 + 4V_{DS}.$$

In Linear region, $g_m = \mu_n C_{ox} \frac{W}{L} V_{DS}$. $r_o = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})}$

$$A_v = \frac{V_{DS}}{V_{GS} - V_{TH} - V_{DS}} = \frac{V_{GS} - V_{TH}}{V_{GS} - V_{TH} - V_{DS}} - 1.$$

(b) $V_{th} = V_{th0} + \gamma(\sqrt{2\phi_F} + V_{SB} - \sqrt{|2\phi_F|})$

3.9

For an NMOS device operating in saturation, plot g_m , r_o , and $g_m r_o$ as the bulk voltage goes from 0 to $-\infty$ while other terminal voltages remain constant.

$$V_{th} = V_{th0} + \gamma(\sqrt{2\phi_F} + V_{SB} - \sqrt{|2\phi_F|})$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

$$r_o = \frac{1}{\frac{1}{2} \lambda \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2}$$

$$g_m r_o = \frac{2}{(V_{GS} - V_{TH}) \lambda}$$

3.10

Consider the circuit of Fig.3.13 with $(W/L)_1 = 50/0.5$ and $(W/L)_2 = 10/0.5$. Assume that $\lambda = \gamma = 0$.

(a) At what input voltage is M_1 at the edge of the triode region? What is the small-signal gain under this condition?

(b) What input voltage drives M_1 into the triode region by 50mV? What is the small-signal gain under this condition?

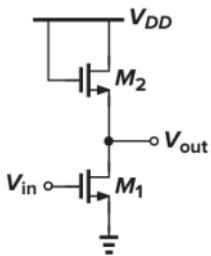


Figure 3.13 CS stage with diode-connected load.

$$(a) V_{out} = V_{in} - V_{th}$$

$$\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{th})^2 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{in} - V_{th})^2$$

We can get $V_{out} = 0.711V$, $V_{in} = 1.411V$.

$$A_v = -G_M R_{out} = -g_{m1} \times \frac{1}{g_{m2}} = -\sqrt{\frac{(\frac{W}{L})_1}{(\frac{W}{L})_2}} = -\sqrt{5}.$$

(b) $V_{out} = V_{in} - V_{th} - 50mV$
 $\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_2(V_{DD} - V_{out} - V_{th})^2 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1[2(V_{in} - V_{th})V_{out} - V_{out}^2].$
 We can get $V_{out} = 0.677V$, $V_{in} = 1.427V$.
 $A_v = -G_m R_{out} = -g_{m1}(r_{o1}||\frac{1}{g_{m2}})$. $g_{m1} = \frac{\delta I_D}{\delta V_{in}} = \mu_n C_{ox} \frac{W}{L} V_{out}$, $g_{m2} = \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{out} - V_{th})$,
 $r_{o1} = \frac{1}{g_{ds}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th} - V_{out})}$
 $A_v = -1.807$

3.11

Repeat Problem 3.10 if body effect is not neglected.

(a) $V_{th2} = V_{th0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{|2\phi_F|}) = 0.844V$.

$$V_{out} = V_{in} - V_{th}$$

$$\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_2(V_{DD} - V_{out} - V_{th2})^2 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1(V_{in} - V_{th1})^2$$

$$V_{out} = 0.666V$$
, $V_{in} = 1.366V$.
 $A_v = -g_{m1} \times \frac{1}{g_{m2} + g_{mb2}} = -1.895$

(b) $V_{th2} = V_{th0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{|2\phi_F|}) = 0.838V$.

$$V_{out} = V_{in} - V_{th} - 50mV$$

$$\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_2(V_{DD} - V_{out} - V_{th2})^2 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1[2(V_{in} - V_{th1})V_{out} - V_{out}^2]$$

$$V_{out} = 0.63V$$
, $V_{in} = 1.385V$.
 $A_v = -g_{m1} \times \frac{1}{g_{m2} + g_{mb2} + g_{ds1}} = -1.546$

3.12

In the circuit of Fig.3.17, $(W/L)_1 = 50/0.5$, $I_1 = 1mA$, and $I_S = 0.75mA$. Assuming $\lambda = 0$, calculate $(W/L)_2$ such that M_1 is at the edge of the triode region. What is the small-signal voltage gain under this condition?

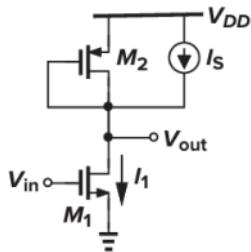


Figure 3.17

From $I_1 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1(V_{in} - V_{th,n})^2$ we could get $V_{out} = V_{in} - V_{th,n} = 0.386V$
 $I_1 - I_s = 0.25mA = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_2(V_{DD} - V_{out} - |V_{th,p}|)^2$

We could get $(W/L)_2 = 4$

$$A_v = \frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{4\mu_n(W/L)_1}{\mu_p(W/L)_2}} = -18.8$$

3.13

Plot the small-signal gain of the circuit shown in Fig.3.17 as I_S goes from 0 to $0.75I_1$. Assume that M_1 is always saturated, and neglect channel-length modulation and body effect.

$$A_v = \frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{\mu_n(W/L)_1 I_1}{\mu_p(W/L)_2 I_2}}$$
 and I_2 goes from I_1 to $0.25I_1$.

3.14

The circuit of Fig.3.18 is designed to provide an output voltage swing of 2.2V with a bias current of 1mA and a small-signal voltage gain of 100. Calculate the dimensions of M_1 and M_2 .

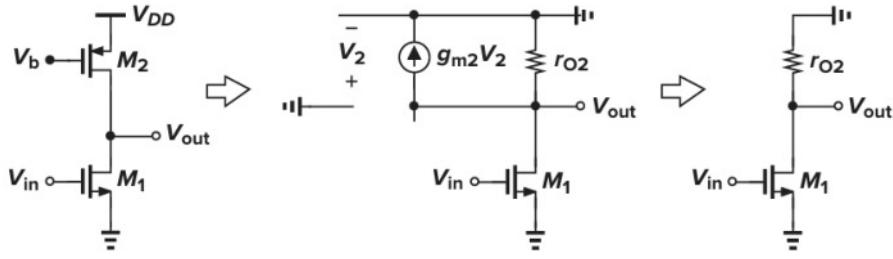


Figure 3.18 CS stage with current-source load.

$$A_v = -G_m R_{out} = -g_m 1 (r_{o1} || r_{o2}) = -g_m 1 \left(\frac{1}{\lambda_1 I_d} || \frac{1}{\lambda_2 I_d} \right).$$

If $L_1 = L_2 = 0.5\mu m$, $\lambda_1 = 0.1$, $\lambda_2 = 0.2$, $g_m = 30mS$.

$$g_m 1 = \frac{2I_D}{V_{GS} - V_{TH,N}}, V_{GS} - V_{TH,N} = 66.7mV. \text{(Which is too small).}$$

So suppose $V_{GS} - V_{TH,N} = 0.15V$, $g_m 1 = 13.3mS$. $\lambda_1 + \lambda_2 = 0.133$. If $\lambda_1 = \lambda_n = 0.1$, $\lambda_2 = 0.033$, $\lambda_2 \times L_2 = \lambda_p \times 0.5\mu m$. We could get $L_2 = 3\mu m$ and $L_1 = 0.3\mu m$. $g_m = \mu_n C_{ox} (\frac{W}{L})_1 (V_{GS} - V_{TH})$, $(W/L)_1 = 662$, $W_1 = 331\mu m$.

$$2.2 = V_{DD} - (V_{in} - V_{th,n}) - (V_{DD} - V_b - |V_{th,p}|) = 0.65 + V_b, V_b = 1.55V.$$

$$I_{D2} = \frac{1}{2} \mu_p C_{ox} (\frac{W}{L})_2 (V_{DD} - V_b - |V_{th,p}|)^2, W_2 = 369\mu m, (W/L)_2 = 123.$$

3.15

Sketch V_{out} versus v_{in} for the circuits of Fig.3.78 as V_{in} varies from 0 to V_{DD} . Identify important transition points.

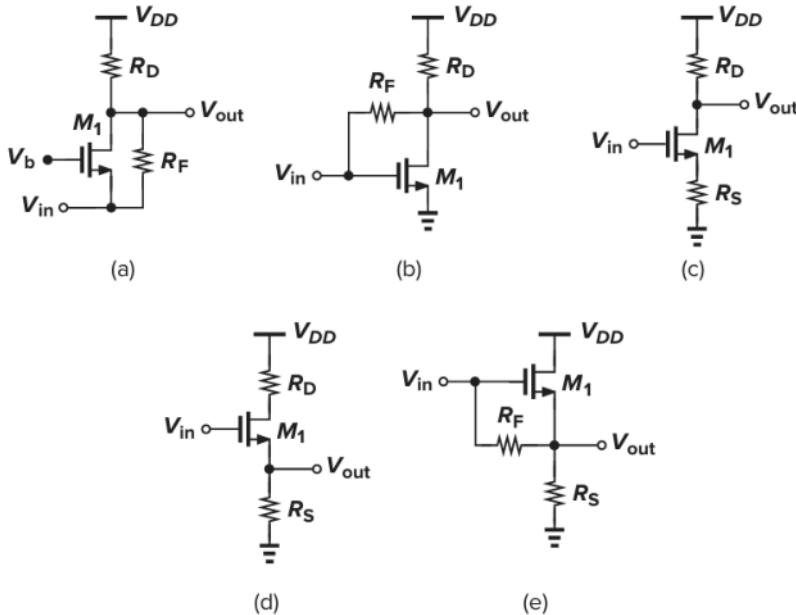
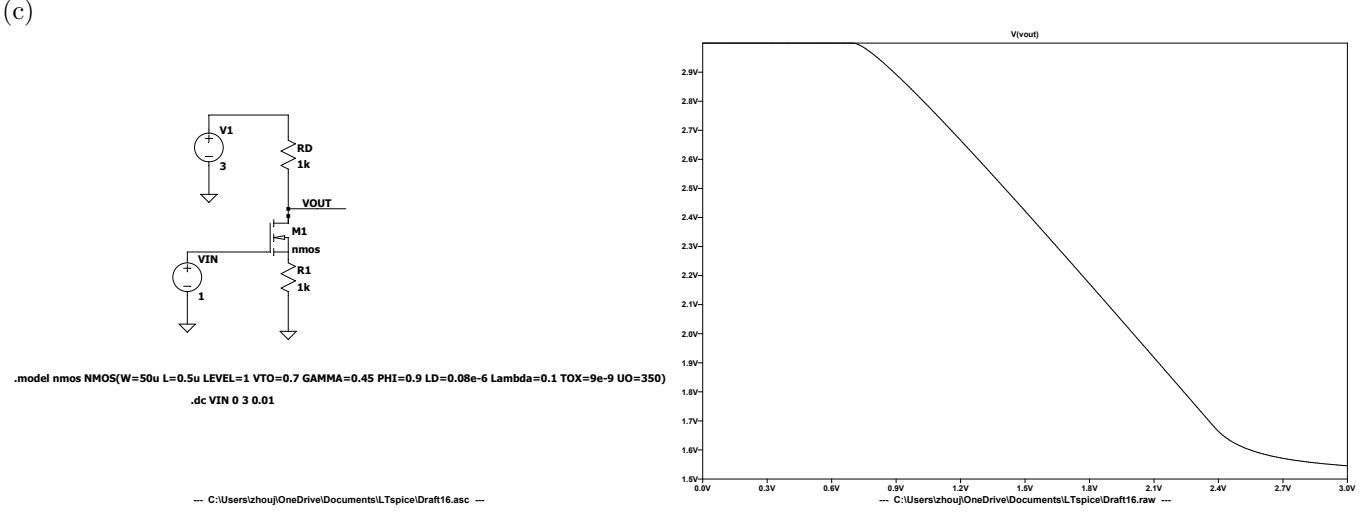
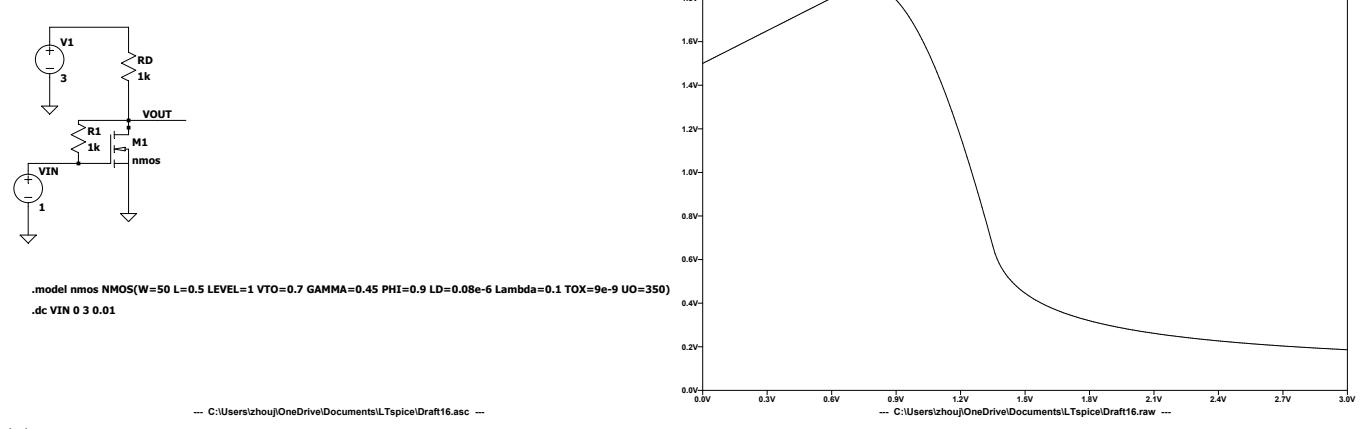
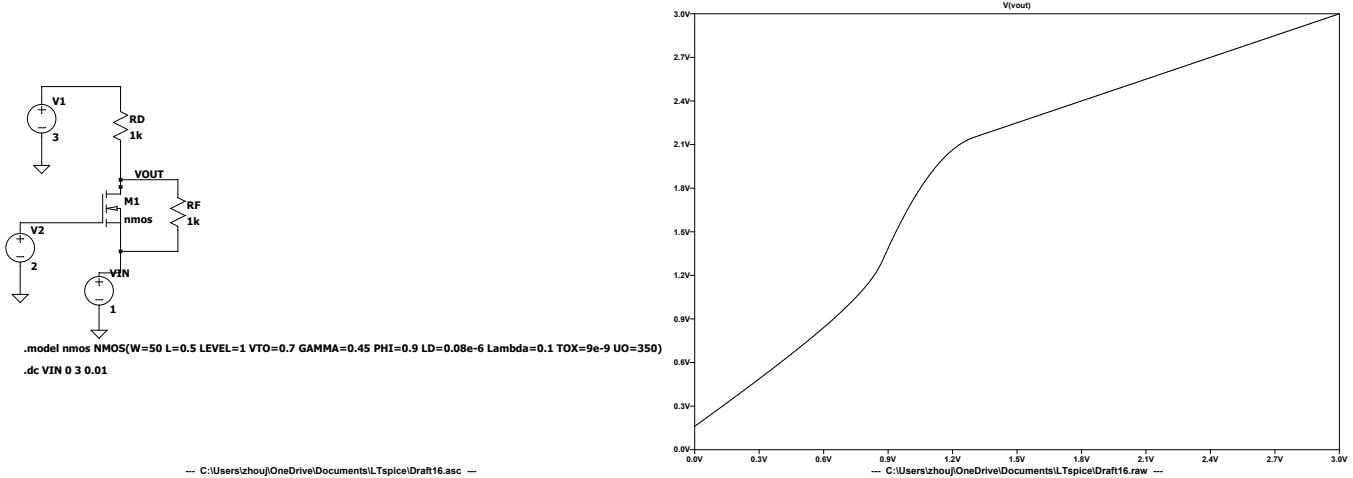
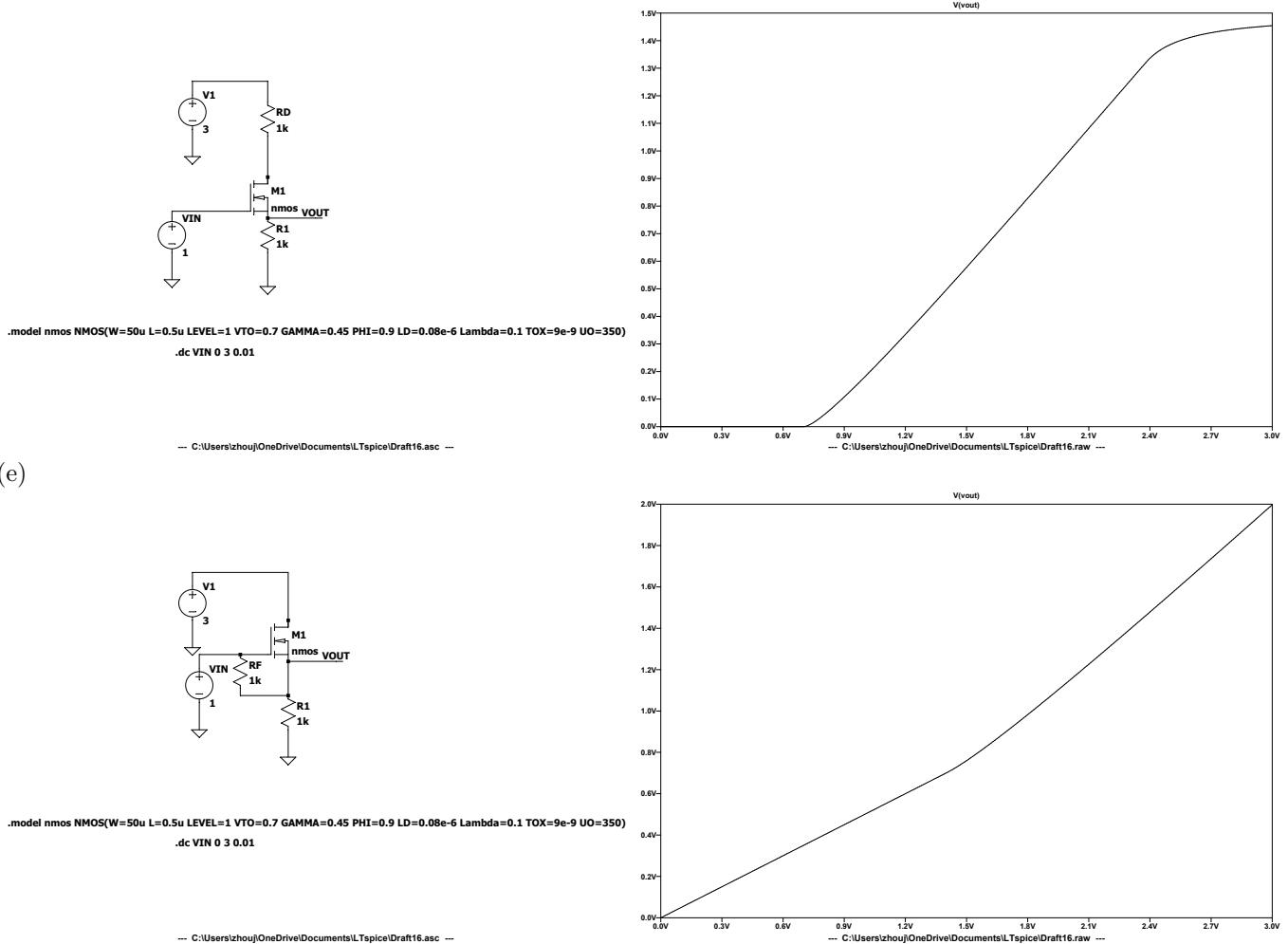


Figure 3.78

(a)





3.16

Sketch V_{out} versus V_{in} for the circuits of Fig.3.79 as V_{in} varies from 0 to V_{DD} . Identify important transition points.

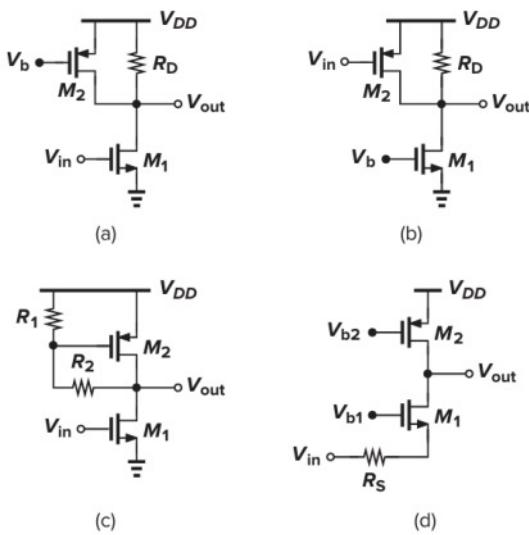
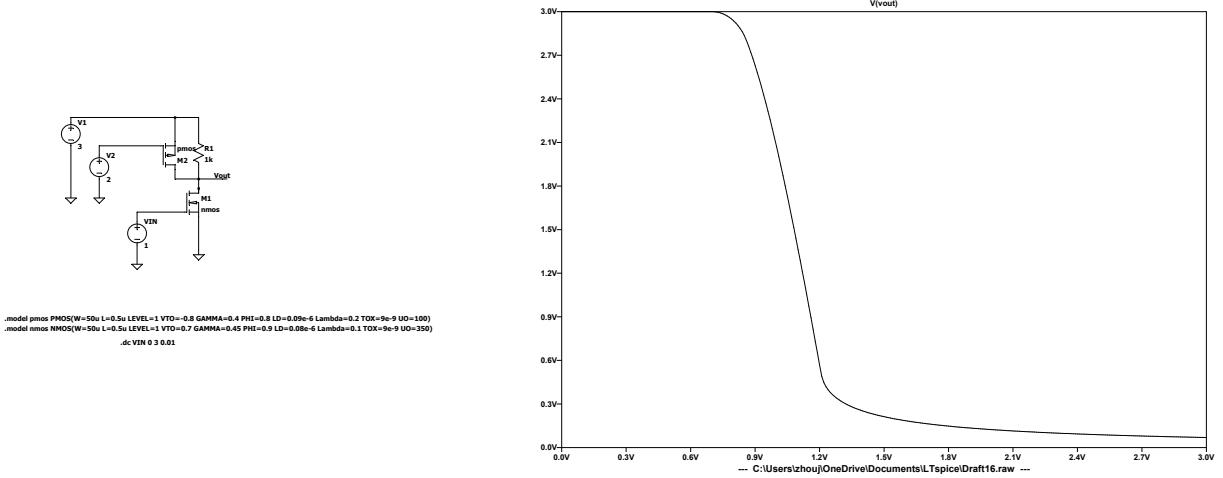
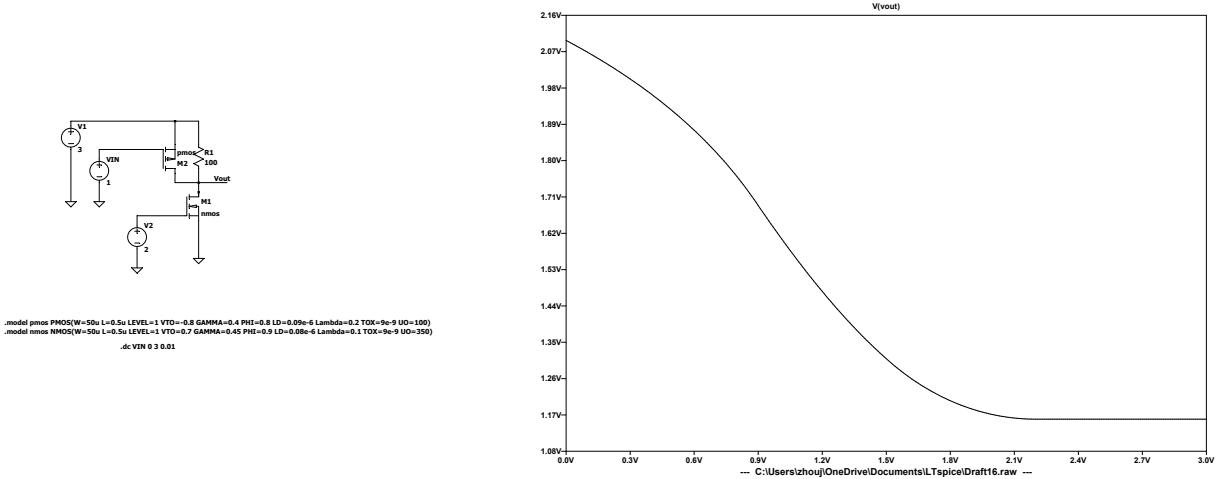


Figure 3.79

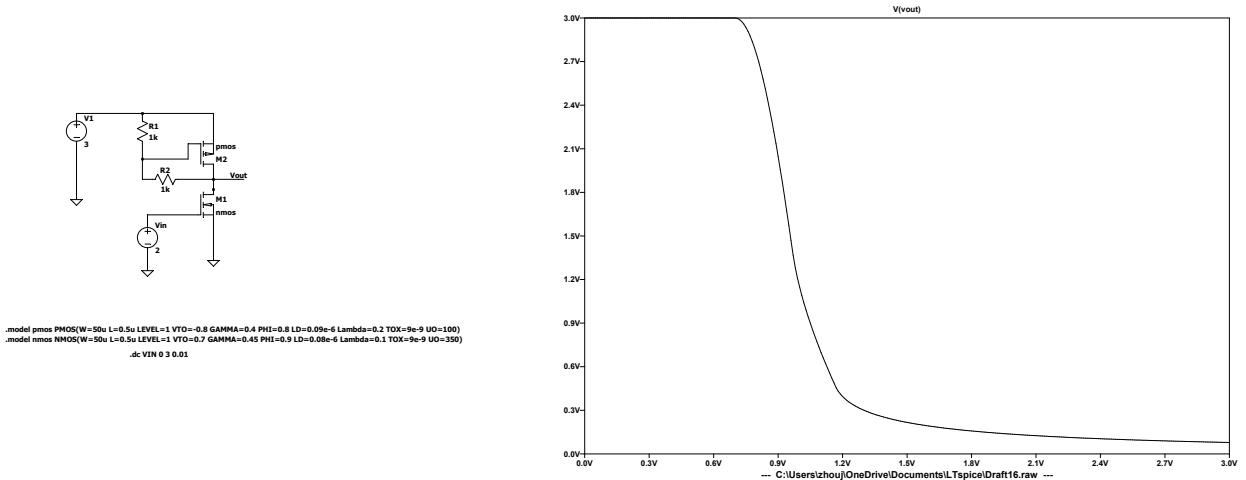
(a)



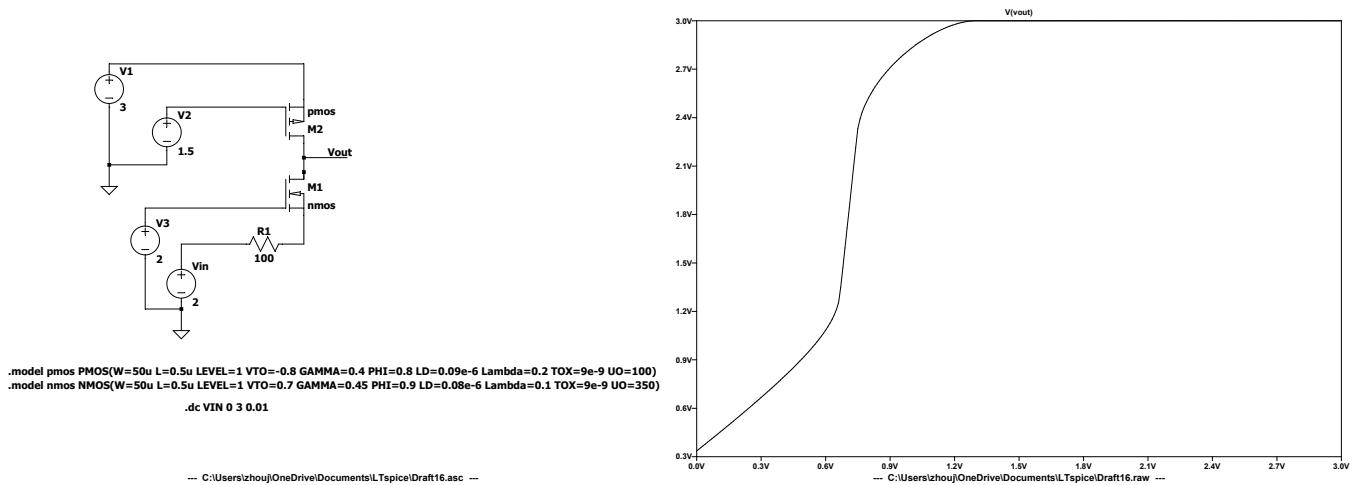
(b)



(c)



(d)



3.17

Sketch V_{out} versus V_{in} for the circuits of Fig.3.80 as V_{in} varies from 0 to V_{DD} . Identify important transition points.

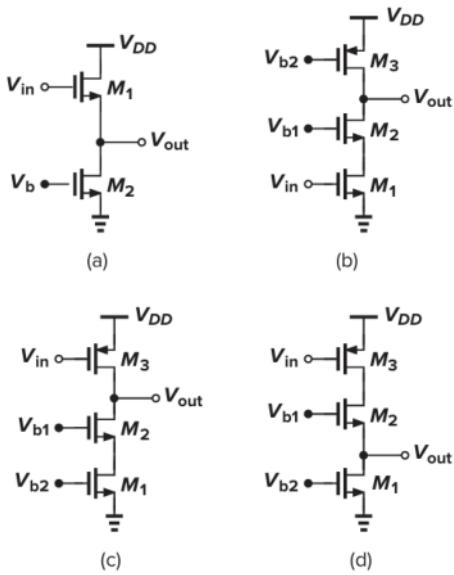
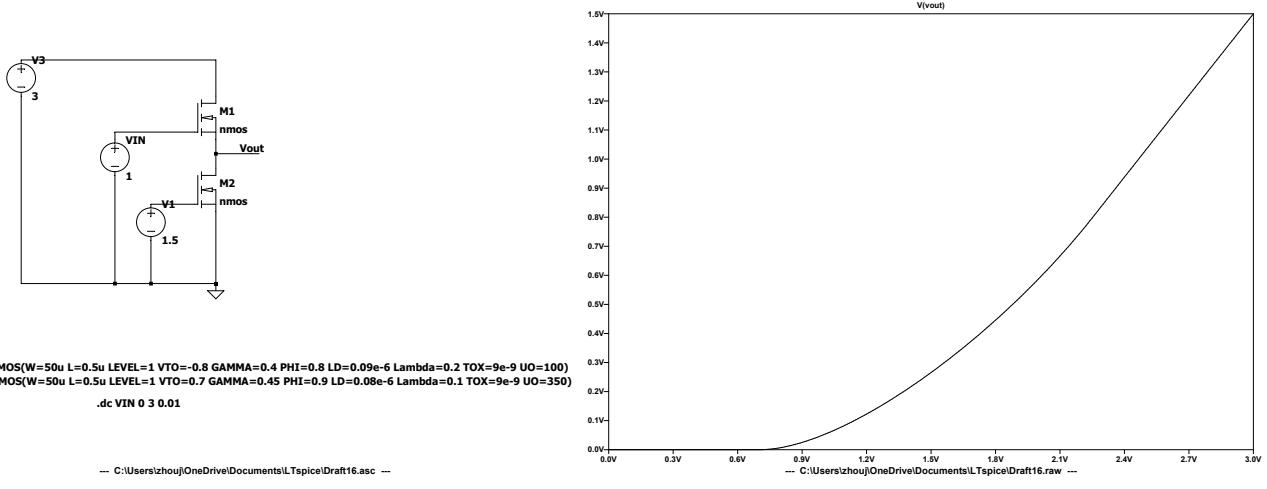
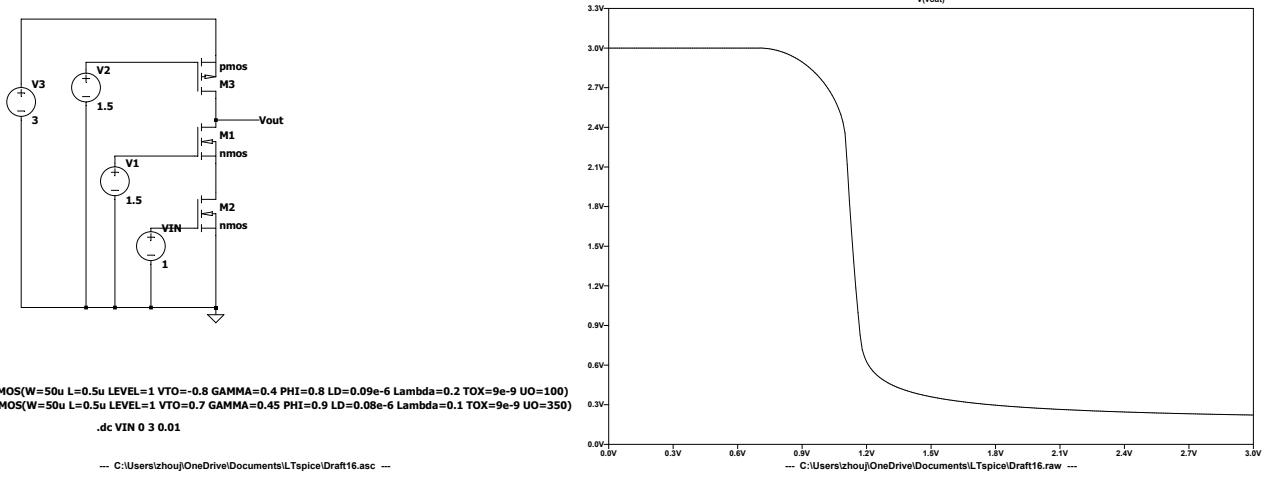


Figure 3.80

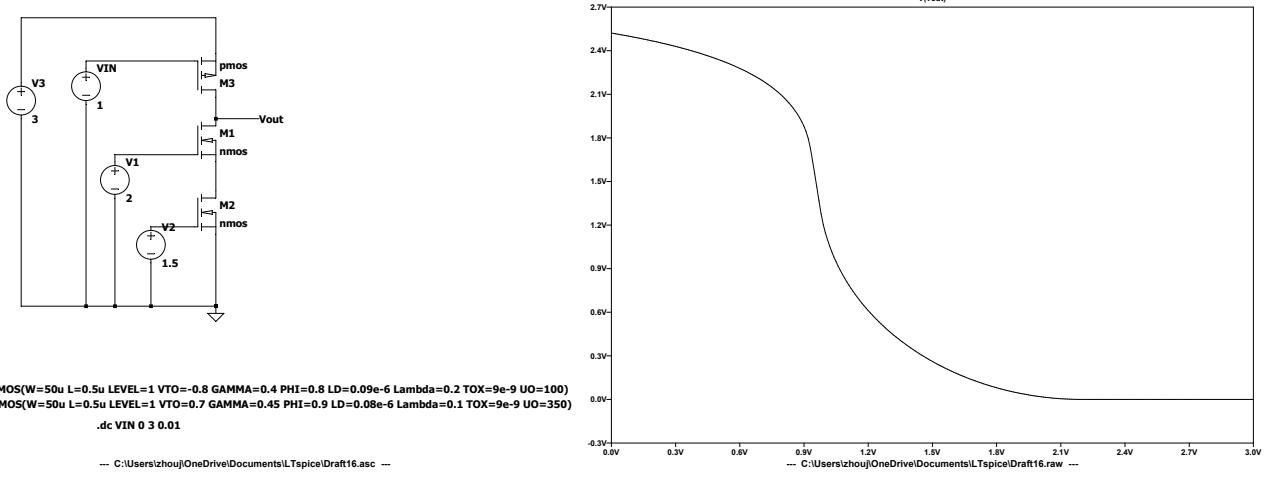
(a)



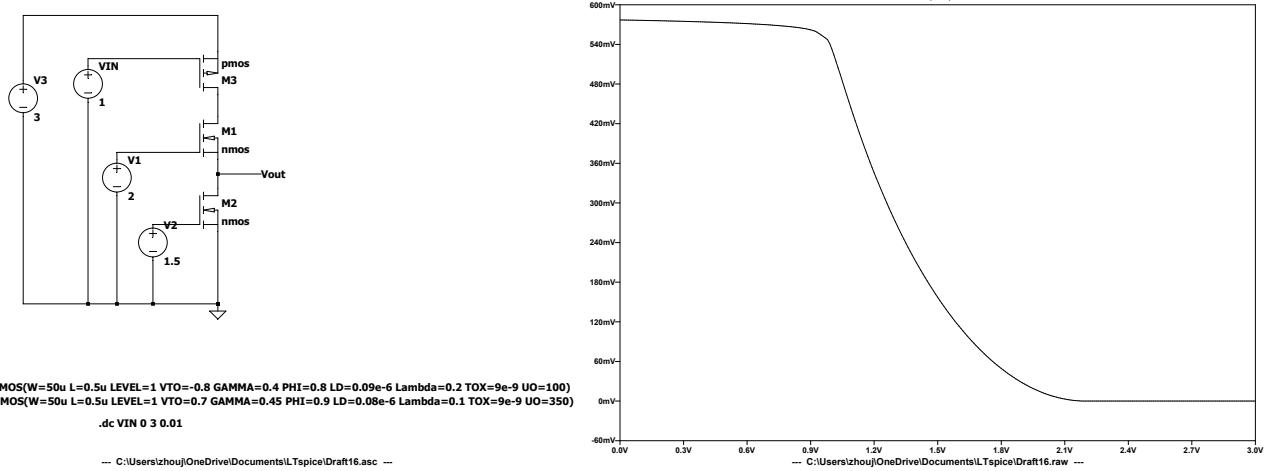
(b)



(c)



(d)



3.18

Sketch I_X versus V_X for the circuits of Fig.3.81 as V_X varies from 0 to V_{DD} . Identify important transition points.

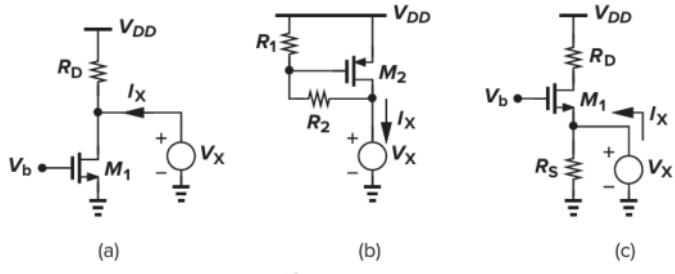
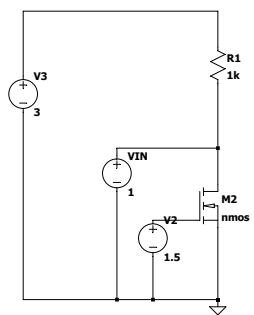


Figure 3.81

(a)



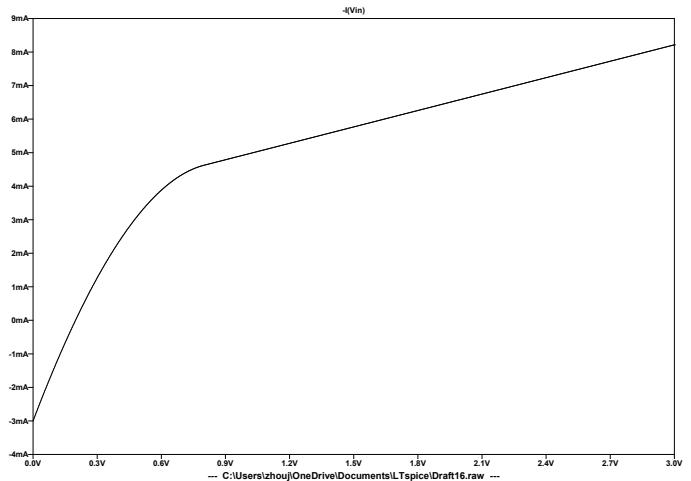
```

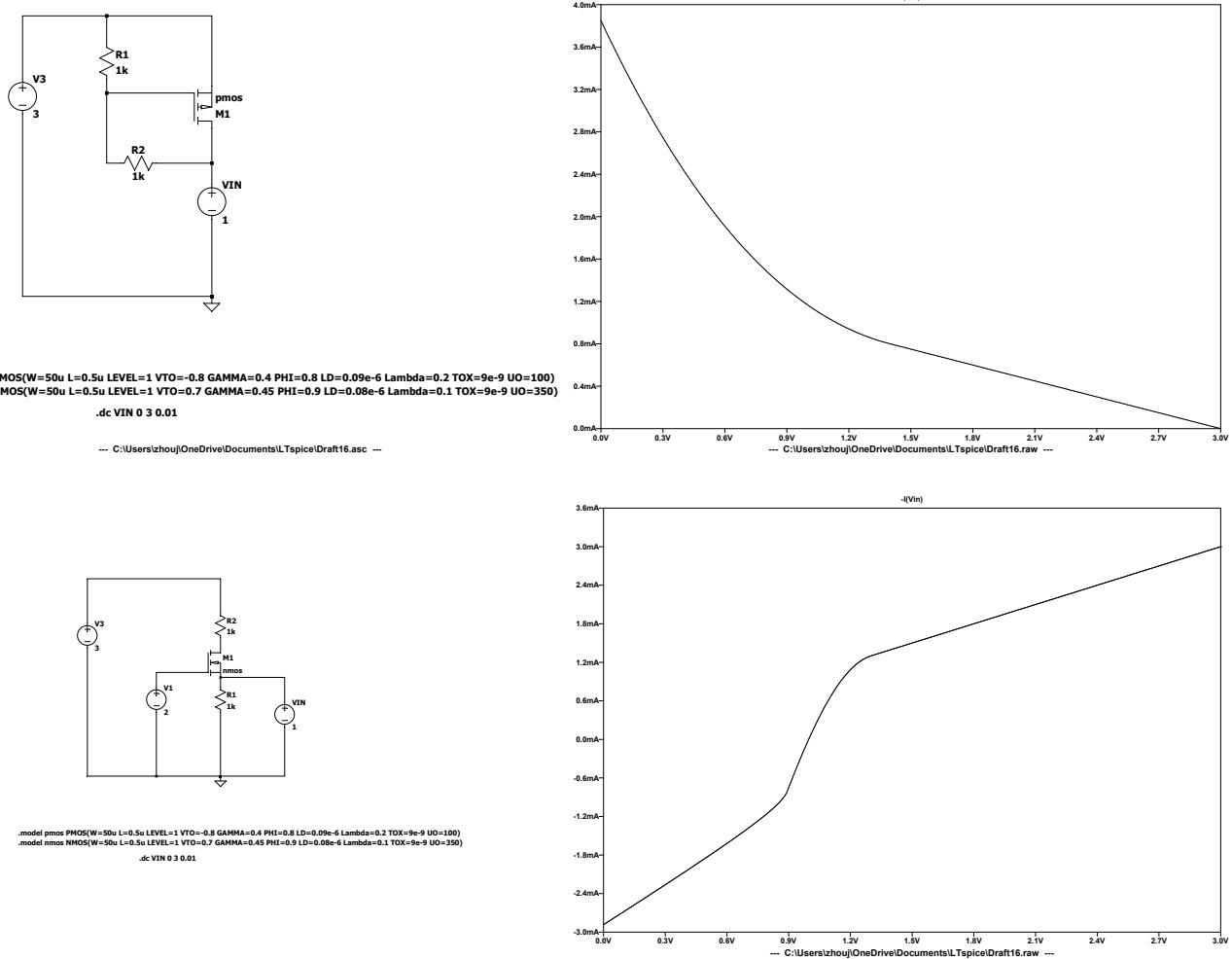
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
.dc VIN 0 3 0.01

```

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(b)





3.19

Sketch I_X versus V_X for the circuits of Fig.3.82 as V_X varies from 0 to V_{DD} . Identify important transition points.

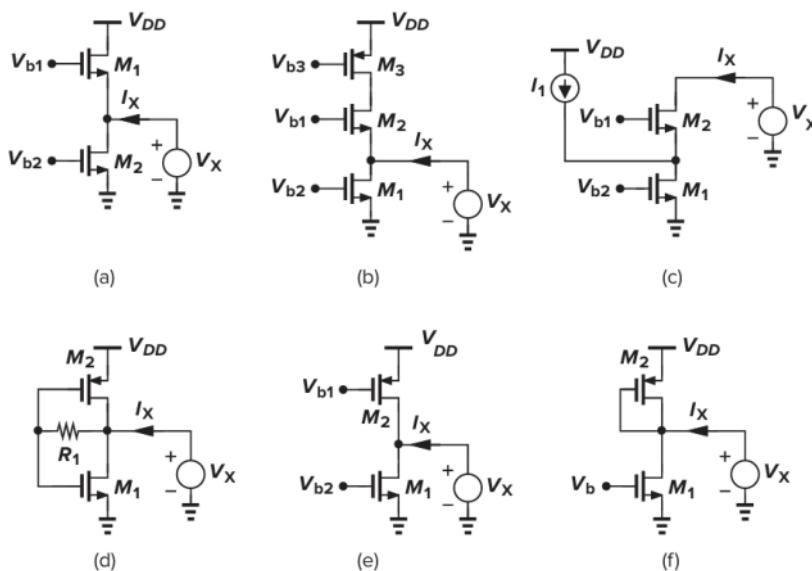
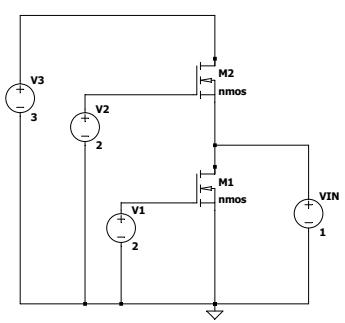


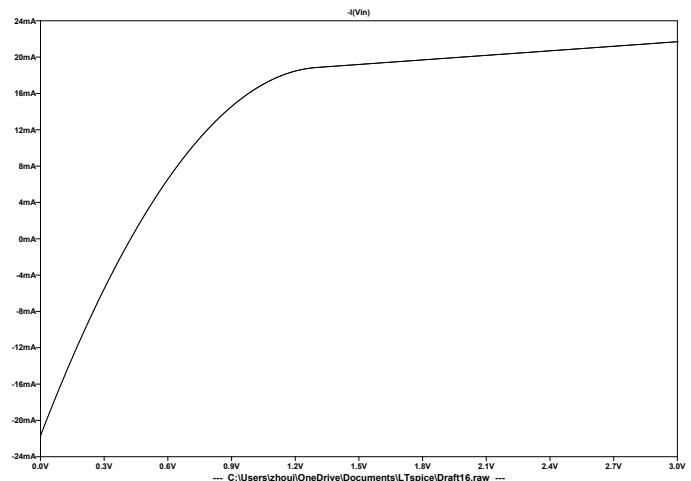
Figure 3.82

(a)

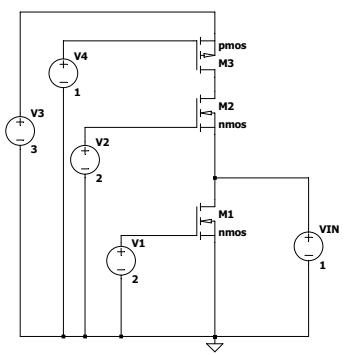


```
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
.dc VIN 0 3 0.01
```

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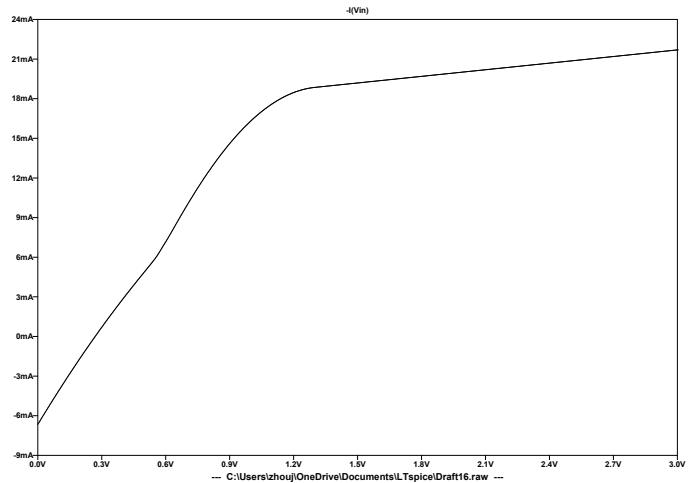


(b)

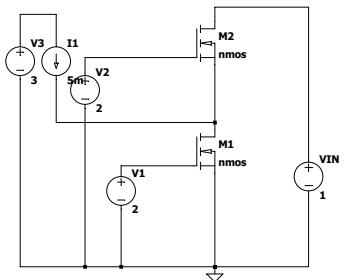


```
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
.dc VIN 0 3 0.01
```

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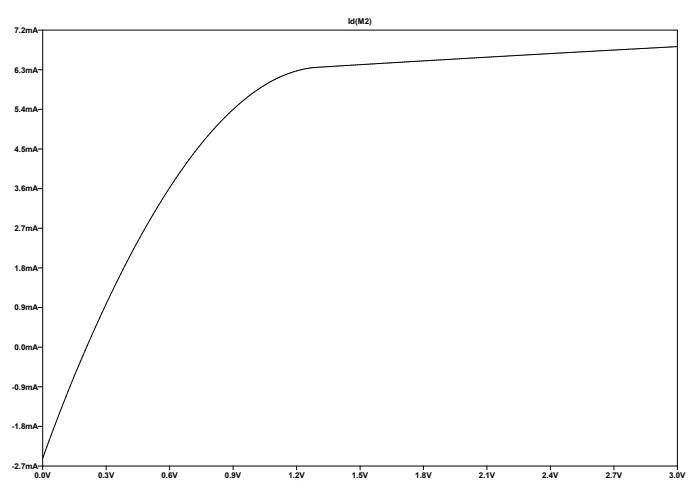


(c)

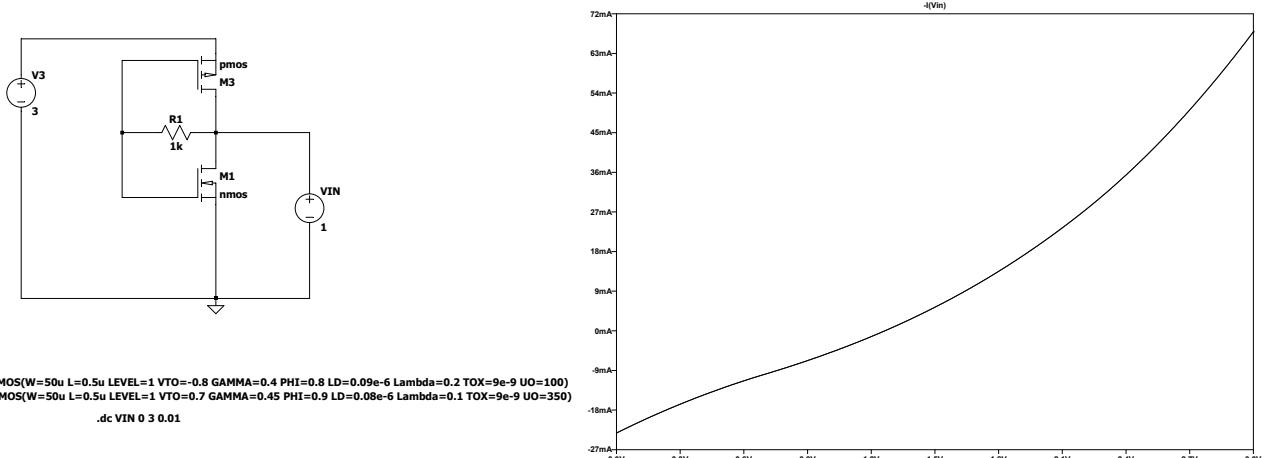


```
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
.dc VIN 0 3 0.01
```

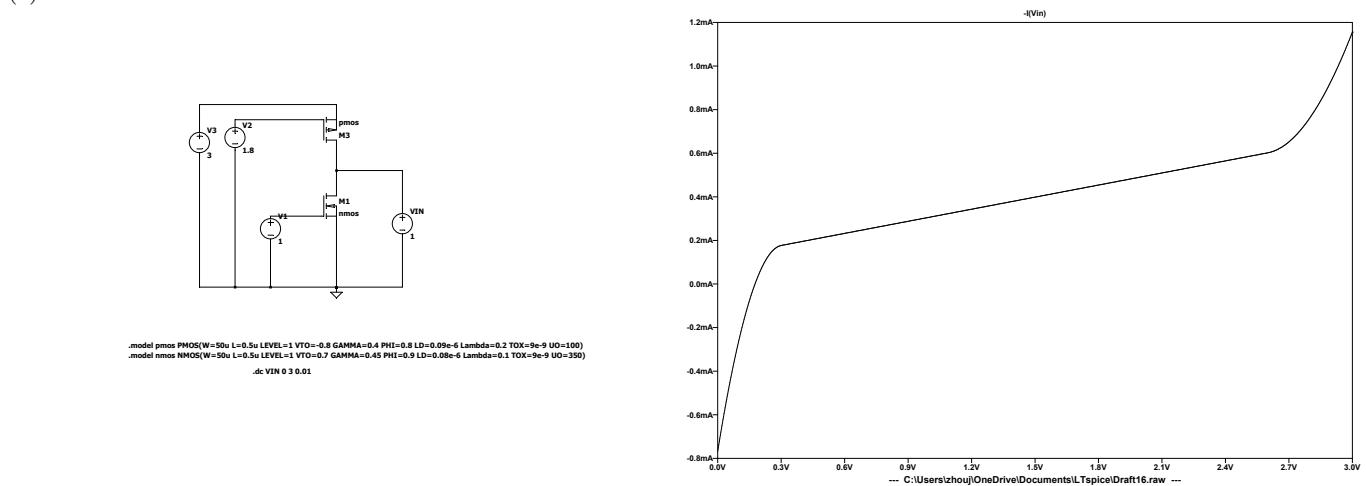
-- C:\Users\zhou\OneDrive\Documents\LTspice\Draft16.asc --



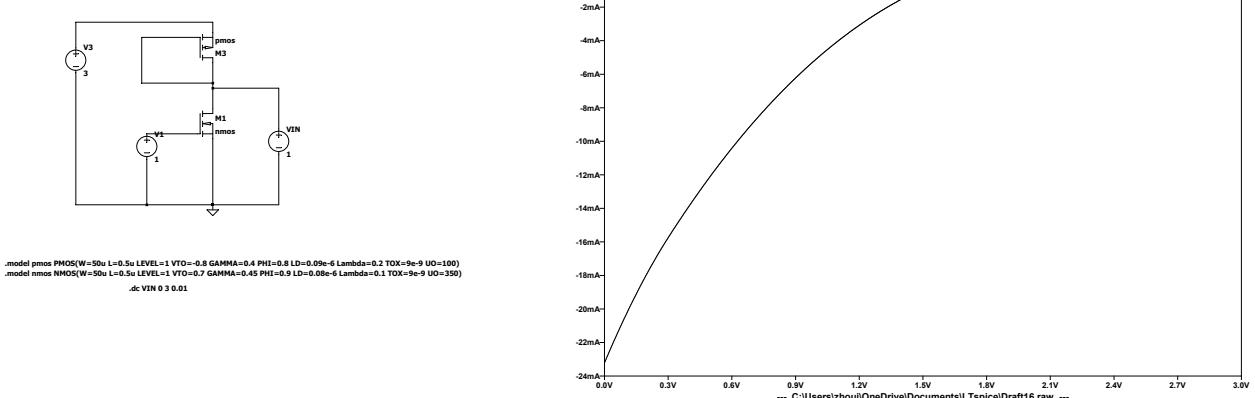
(d)



(e)



(f)



3.20

Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of each circuit in Fig.3.83 ($\lambda \neq 0, \gamma = 0$).

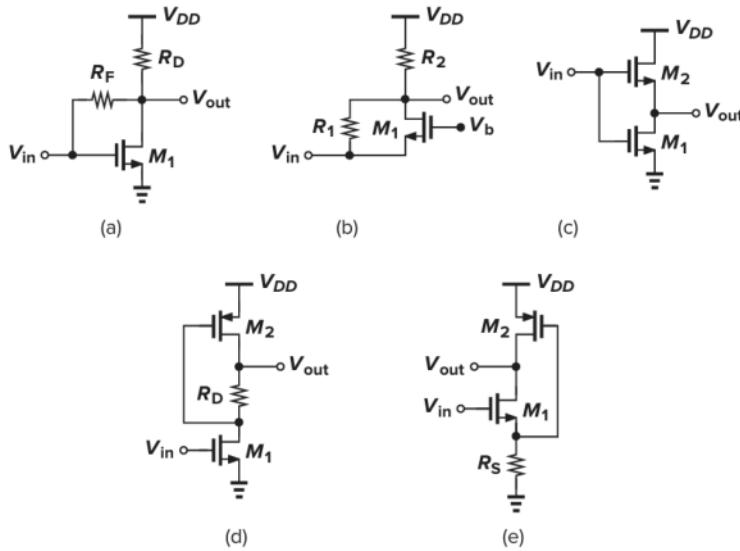


Figure 3.83

$$(a) \frac{V_{in} - V_{out}}{R_F} - g_m V_{in} - \frac{V_{out}}{r_o || R_D} = 0$$

$$A_v = \frac{V_{out}}{V_{in}} = (\frac{1}{R_F} - g_m)(R_F || r_o || R_D)$$

$$(b) \frac{V_{out} - V_{in}}{R_1 || r_o} - g_m V_{in} + \frac{V_{out}}{R_2} = 0$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{\frac{g_m}{r_o} + \frac{1}{R_1 || r_o}}{\frac{1}{R_1 || R_2 || r_o}}$$

$$(c) g_{m2}(V_{in} - V_{out}) - \frac{V_{out}}{r_{o2}} - g_{m1}V_{in} - \frac{V_{out}}{r_{o1}} = 0$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m2} - g_{m1}}{g_{m2} + \frac{1}{r_{o1} || r_{o2}}}$$

(d) Suppose the node between M1 and R_D is x.

$$g_{m1}V_{in} + \frac{V_x}{r_{o2}} = \frac{V_{out} - V_x}{R_D}$$

$$g_{m2}V_x + \frac{V_{out}}{r_{o2}} = \frac{V_x - V_{out}}{R_D}$$

Use the above two formula to cancel V_x and get $A_v = \frac{g_{m1}(\frac{1}{R_D} - g_{m2})}{(\frac{1}{R_D} + \frac{1}{r_{o2}})(\frac{1}{R_D} + \frac{1}{r_{o1}}) + \frac{1}{R_D}(g_{m2} - \frac{1}{R_D})}$

$$(e) g_{m1}(V_{in} - V_s) + \frac{V_{out} - V_s}{r_{o1}} = \frac{V_s}{R_s}$$

$$g_{m2}V_s + \frac{V_{out}}{r_{o2}} = \frac{-V_s}{R_s}$$

Use the above two formula to cancel V_s and get $A_v = \frac{-g_{m1}(\frac{1}{R_s} + g_{m2})}{\frac{1}{r_{o1}}(\frac{1}{R_s} + g_{m2}) + \frac{1}{r_{o2}}(\frac{1}{r_{o1}} + \frac{1}{R_s} + g_{m1})}$

3.21

Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of each circuit in Fig.3.84 ($\lambda \neq 0, \gamma = 0$).

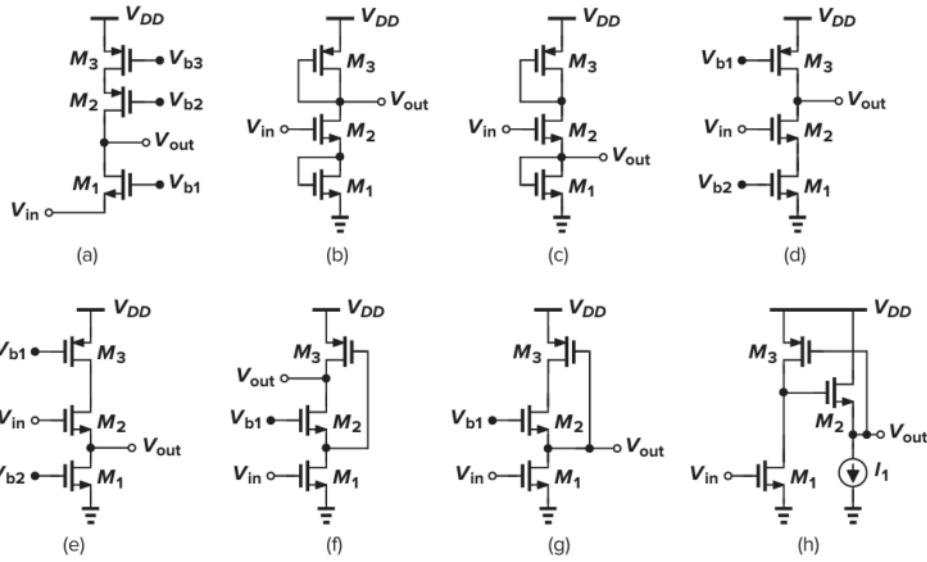


Figure 3.84

$$\begin{aligned}
 (a) A_v &= g_{m1} [r_{o1} || (1 + g_{m2} r_{o2}) r_{o3}] \\
 (b) A_v &= -\frac{g_{m2}}{1 + \frac{g_{m2}}{g_{m1}}} \left[\frac{1}{g_{m3}} \right] || (1 + g_{m2} r_{o2}) \frac{1}{g_{m1}} \\
 (c) A_v &= \frac{g_{m2}}{1 + \frac{g_{m2}}{g_{m3}}} \times \left[\frac{1}{g_{m1}} \right] || \frac{\frac{1}{g_{m3}} + r_{o2}}{(1 + g_{m2} r_{o2})} \\
 (d) A_v &= -\frac{g_{m2}}{1 + g_{m2} r_{o1}} \times r_{o3} || (1 + g_{m2} r_{o2}) r_{o1} \\
 (e) A_v &= \frac{g_{m2}}{1 + g_{m2} r_{o3}} \times r_{o1} || \frac{r_{o2} + r_{o3}}{1 + g_{m2} r_{o2}} \\
 (f) G_m &= -g_{m1} + g_{m1} (r_{o1} || \frac{1}{g_{m2}}) g_{m3} \\
 R_{out} &= (1 + g_{m2} r_{o2}) r_{o1} || r_{o3} || \frac{\Delta V}{(1 + g_{m2} r_{o2}) r_{o1} g_{m3}}
 \end{aligned}$$

$$A_v = G_m R_{out}$$

$$(g) G_m = -g_{m1}$$

$$R_{out} = r_{o1} || \frac{r_{o2} + r_{o3}}{(1 + g_{m2} r_{o2})} || \frac{\Delta V}{g_{m3} \Delta V \times \frac{r_{o3}}{r_{o2} + r_{o3}}}$$

$$A_v = G_m R_{out}$$

$$(h) G_m = -g_{m1} (r_{o1} || r_{o3}) g_{m2}$$

$$R_{out} = \frac{1}{g_{m2}} || \frac{\Delta V}{\Delta V g_{m3} (r_{o1} || r_{o3}) g_{m2}}$$

$$A_v = G_m R_{out}$$

3.22

Sketch V_X and V_Y as a function of time for each circuit in Fig.3.85. The initial voltage across C_1 is equal to V_{DD} .

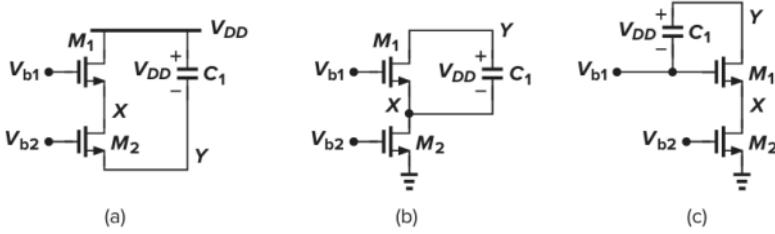
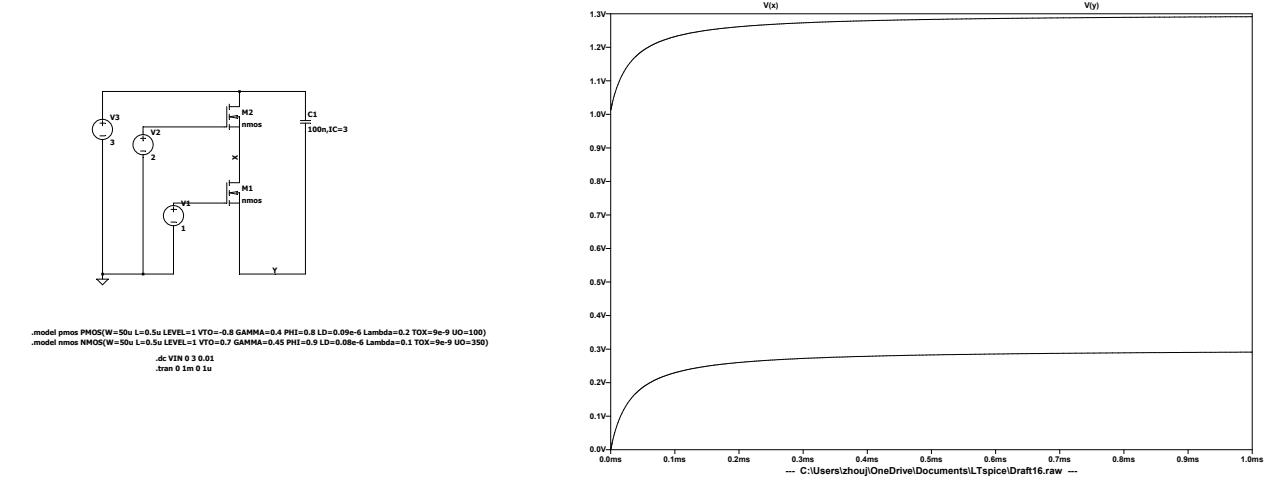
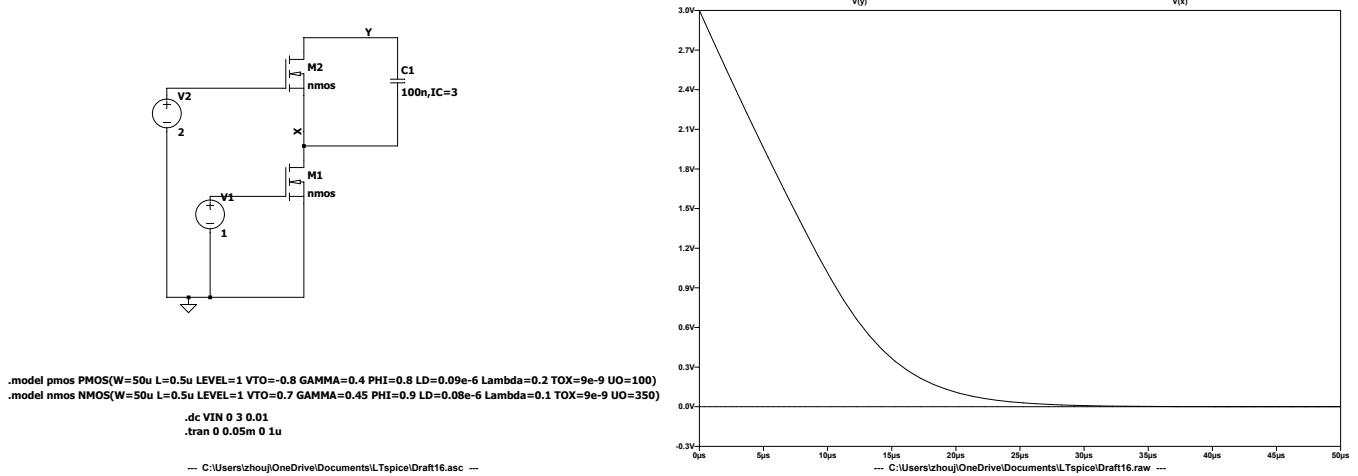


Figure 3.85

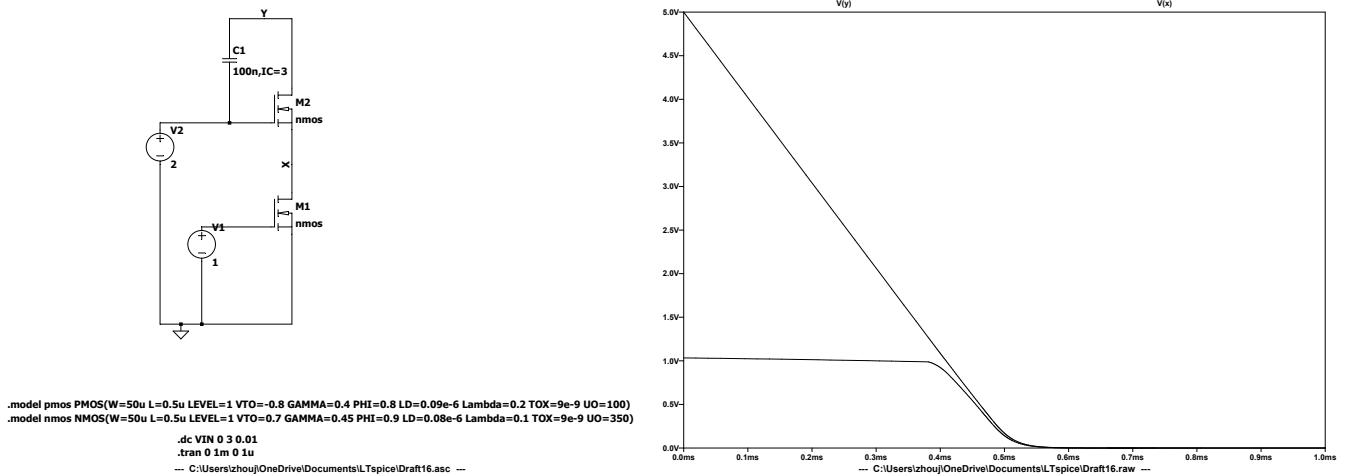
(a)



(b)



(c)



3.23

In the cascode stage of Fig.3.59, assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 10/0.5$, $I_{D1} = I_{D2} = 0.5mA$, and $R_D = 1k\Omega$.

- Choose V_b such that M_1 is 50mV away from the triode region.
- Calculate the small-signal voltage gain.
- Using the value of V_b found in part (a), calculate the maximum output voltage swing. Which device enters the triode region first as V_{out} falls.
- Calculate the swing at node X for the maximum output swing obtained above.

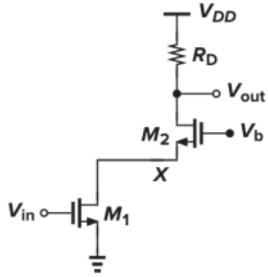


Figure 3.59 Cascode stage.

(a) Using $V_{DS,1} = V_{in} - V_{th} + 50mV$ and $I_D = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1(V_{in} - V_{th})^2$, we can get $V_{in} = 0.973V$, $V_x = 0.323V$

$I_D = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1(V_b - V_x - V_{th})^2$, we can get $V_b = 1.634V$

(b) $A_v = -g_m R_D = -\sqrt{2\mu_n C_{ox}(\frac{W}{L})_1 I_D R_D} = -3.66$

(c) $g_{m2} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_2 I_D} = 1.638mS$, $\frac{1}{g_{m2}} = 600\Omega$
 $V_{out} = V_{DD} - I_D R_D = 2.5V$.

M1 first goes into triode region.

$V_x = V_{in} - V_{th}$, $I_D = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1(V_{in} - V_{th})^2 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_2(V_b - V_{th} - V_{th})^2$
 $V_x = 0.289V$, $I_D = 0.558mA$, $V_{out,min} = 2.442V$.

$V_{out,max} = 3V$

(d) $V_{x,min} = 0.289V$.

$V_{x,max} = V_b - V_{th} = 0.934V$

3.24

Consider the circuit of Fig.3.23 with $(W/L)_1 = 50/0.5$, $R_D = 2k\Omega$, $R_S = 200\Omega$.

(a) Calculate the small-signal voltage gain if $I_D = 0.5mA$.

(b) Assuming $\lambda = \gamma = 0$, calculate the input voltage that places M_1 at the edge of the triode region.
 What is the gain under this condition?

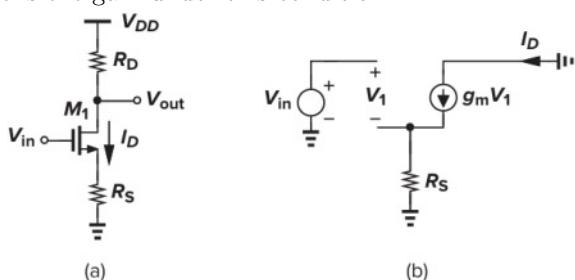


Figure 3.23 CS stage with source degeneration.

$$(a) g_m = \sqrt{2\mu_n C_{ox}(\frac{W}{L}) I_D} = 3.66mS$$

$$V_{sb} = R_S I_D = 0.1$$

$$r_o = 20k\Omega$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}} = 0.225g_m$$

$$A_v = G_m R_{out} = \frac{-g_m}{1 + (g_m + g_{mb})R_s + \frac{R_s}{r_o}} \times R_D || [1 + (g_m + g_{mb})r_o] = -3.48$$

$$(b) V_{out} = V_{in} - V_{th}$$

$$\frac{V_{DD} - V_{out}}{R_D} = \frac{V_s}{R_s} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{in} - V_s - V_{th})^2$$

$$V_{out} = 0.653V$$

$$V_{in} = 1.353V$$

$$V_s = 0.235V$$

$$I_D = \frac{V_{DD} - V_{out}}{R_D} = 1.174mA$$

$$A_v = \frac{-g_m}{1 + g_m R_s} \times R_D = -5.29$$

3.25

Suppose the circuit of Fig.3.22 is designed for a voltage gain of 5. If $(W/L)_1 = 20/0.5$, $I_D1 = 0.5mA$, and $V_b = 0V$:

- (a) Calculate the aspect ratio of M_2 .
- (b) What input level places M_1 at the edge of the triode region? What is the small-signal gain under this condition?
- (c) What input level places M_2 at the edge of the triode region? What is the small-signal gain under this condition?

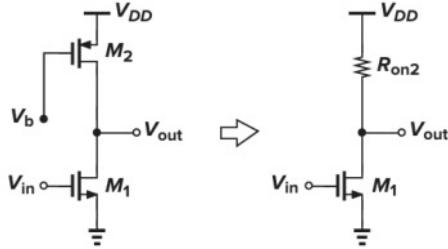


Figure 3.22 CS stage with triode load.

$$(a) A_v = -g_m1 R_{on2}, g_{m1} = \sqrt{2\mu_n C_{ox} (\frac{W}{L})_1 I_D} = 2.31mS$$

$$R_{on2} = 5/g_{m1} = 2159\Omega$$

$$(W/L)_2 = \frac{1}{\mu_p C_{ox} R_D (V_{DD} - V_b - |V_{THP}|)} = 5.5$$

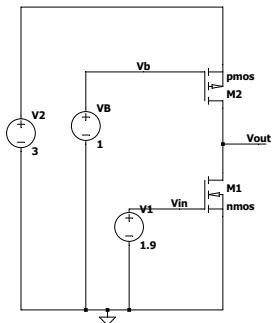
$$(b) V_{out} = V_{in} - V_{th}, V_{out} = V_{DD} - I_D R_{on2} = V_{DD} - R_{on2} \times \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_b - |V_{THP}|)^2$$

3.26

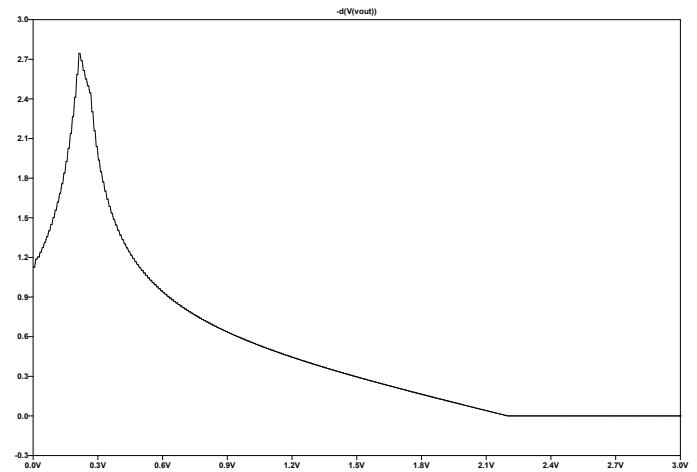
Sketch the small-signal voltage gain of the circuit shown in Fig.3.22 as V_b varies from 0 to V_{DD} . Consider two cases:

- (a) M_1 enters the triode region before M_2 is saturated.
- (b) M_1 enters the triode region after M_2 is saturated.

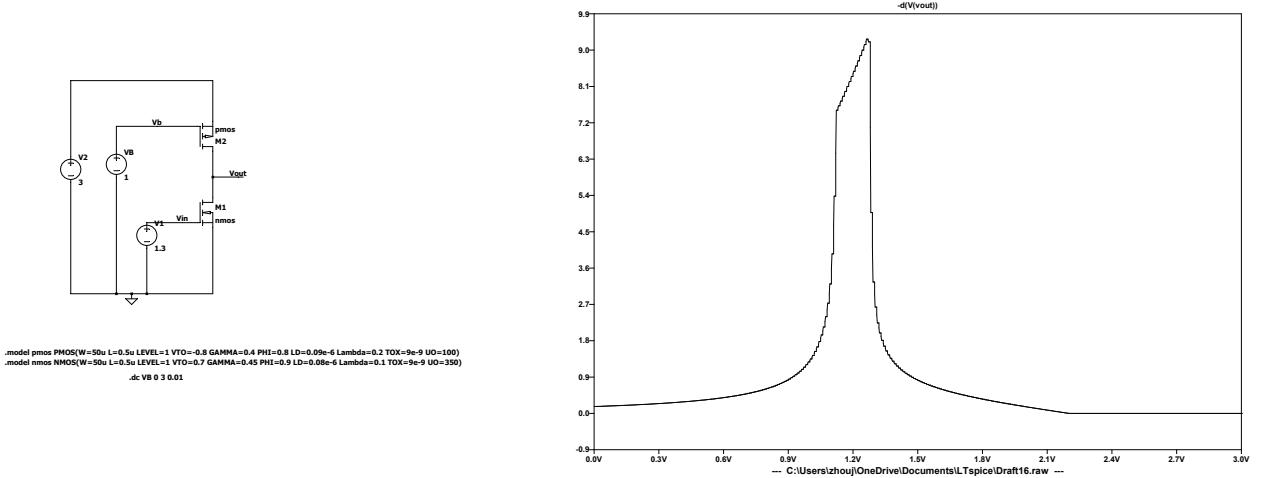
(a)



```
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
.dc VB 0 3 0.01
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(b)



3.27

A source follower can operate as a level shifter. Suppose the circuit of Fig.3.37(b) is designed to shift the voltage level by 1V, i.e., $V_{in} - V_{out} = 1V$.

- (a) Calculate the dimensions of M_1 and M_2 if $I_{D1} = I_{D2} = 0.5mA$, $V_{GS2} - V_{GS1} = 0.5V$, and $\lambda = \gamma = 0$.
- (b) Repeat part(a) if $\gamma = 0.45V^{-1}$ and $V_{in} = 2.5V$. What is the minimum input voltage for which M_2 remains saturated?

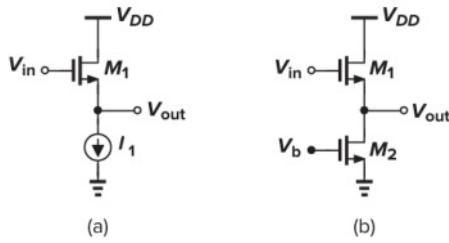


Figure 3.37 Source follower using
(a) an ideal current source, and (b) an
NMOS transistor as a current source.

$$(a) I_D = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{th1})^2 = 0.5mA.$$

$$I_D = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_b - V_{th2})^2 = 0.5mA.$$

$$V_b - (V_{in} - V_{out}) = 0.5V$$

$$V_b = 1.5V, \left(\frac{W}{L}\right)_1 = 82.8, \left(\frac{W}{L}\right)_2 = 11.6.$$

$$(b) V_{th1} = V_{thn} + \gamma(\sqrt{2\phi_F + V_{out}} - \sqrt{2\phi_F})$$

$$V_{out} = 1.5V$$

$$V_{th1} = 0.97V$$

$$\left(\frac{W}{L}\right)_1 = 8280, \left(\frac{W}{L}\right)_2 = 11.6.$$

$$V_{out,min} = V_b - V_{th2} = 0.8V$$

$$V_{th1'} = 0.86V$$

$$1 - 0.97 = V_{in} - V_{out} - V_{th1'}$$

$$V_{in,min} = 1.69V$$

3.28

Sketch the small-signal gain, V_{out}/V_{in} , of the cascode stage shown in Fig.3.59 as V_b goes from 0 to V_{DD} . Assume that $\lambda = \gamma = 0$.

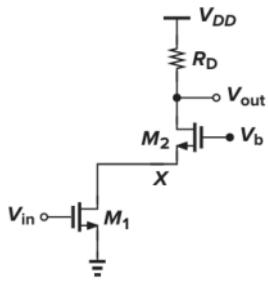
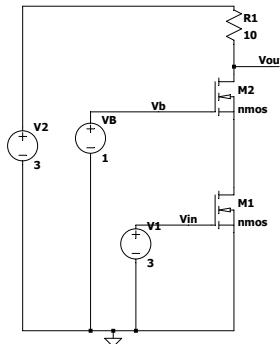
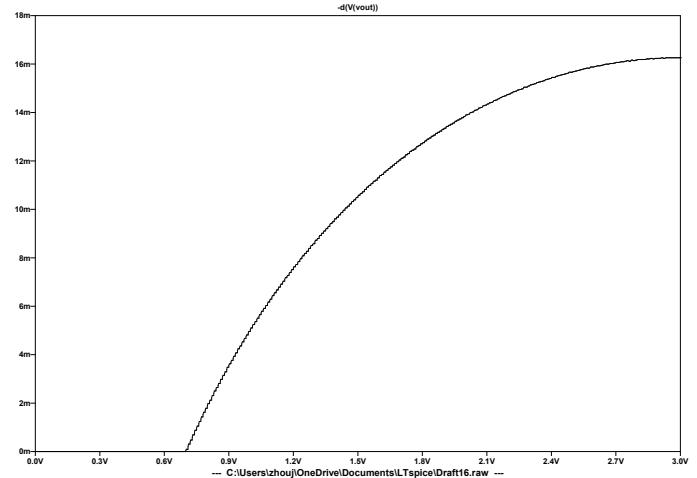


Figure 3.59 Cascode stage.



```
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0 Lambda=0)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0 Lambda=0)
.dc VB 0 3 0.01
-- C:\Users\zhouj\OneDrive\Documents\LTspice\Draft16.asc --
```



3.29

The cascode of Fig.3.70 is designed to provide an output swing of 1.9V with a bias current of 0.5mA. If $\gamma = 0$ and $(W/L)_{1-4} = W/L$, calculate V_{b1} , V_{b2} , and W/L . What is the voltage gain if $L = 0.5\mu m$?

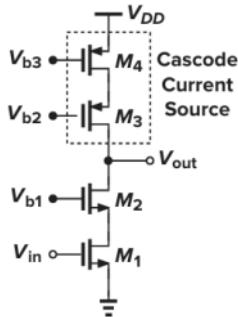


Figure 3.70 NMOS cascode amplifier with PMOS cascode load.

$$Swing = V_{b2} + |V_{THP}| - (V_{b1} - V_{THN}) = 1.9V$$

We cannot solve this one because we don't know voltage on the nodes between M1 and M2.

3.30

Consider the gate-source voltage of M_1 in Fig.3.23(a): $V_{GS} = V_{in} - I_D R_S$. Determine ΔV_{GS} in response to a change in V_{in} and show that it decreases as $g_m R_S$ increases. How does this trend show that the circuit becomes more linear?

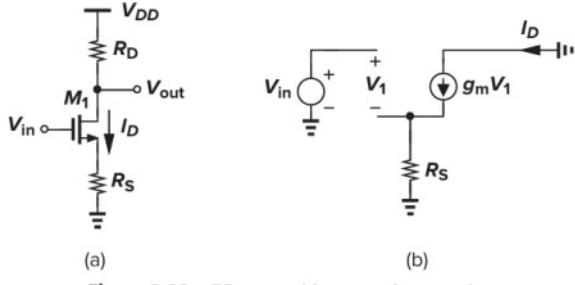


Figure 3.23 CS stage with source degeneration.

$$g_m(\Delta V_{in} - \Delta V_s) = \frac{\Delta V_s}{R_s}$$

$$\Delta V_s = \frac{g_m R_s}{g_m R_s + 1} \Delta V_{in}$$

$$\Delta V_{GS} = \frac{\Delta V_{in}}{g_m R_s + 1}$$

As we can see, as Vin increase, g_m also increase, and makes the change of V_{GS} slow, which is more linear.

3.31

Prove that the voltage gain from V_{DD} to V_{out} in Fig.3.21 is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_m r_{o2} + 1}{r_{o2} + r_{o1}} r_{o1}$$

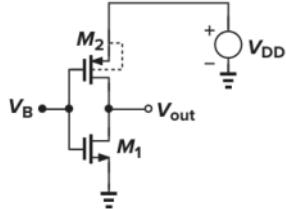


Figure 3.21 Arrangement for studying supply sensitivity of CS stage with active load.

$$A_v = G_m R_{out} = (g_m 2 + \frac{1}{r_{o2}})(r_{o1} || r_{o2}) = \frac{g_m 2 r_{o2} + 1}{r_{o2} + r_{o1}} r_{o1}$$

3.32

In the circuit shown in Fig.3.86, prove that $\frac{V_{out1}}{V_{out2}} = \frac{-R_D}{R_S}$, where V_{out1} and V_{out2} are small-signal quantities and $\lambda, \gamma > 0$.

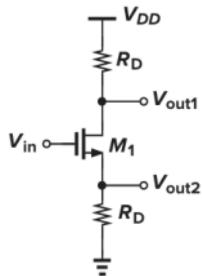


Figure 3.86

$$\frac{V_{out1}}{V_{DD}} = -R_D \Delta I$$

$$\frac{V_{out2}}{V_{DD}} = R_S \Delta I$$

$$\frac{V_{out1}}{V_{out2}} = -R_D / R_S$$

$$\frac{V_{out1}}{V_{in}} = G_m R_{out} = \frac{-g_m}{1 + (g_m + g_{mb}) R_s + \frac{r_o}{r_o}} \times R_D || [1 + (g_m + g_{mb}) r_o] R_s$$

$$\frac{V_{out2}}{V_{in}} = G_m R_{out} = g_m \frac{r_o}{r_o + R_D} \times [R_s || \frac{r_o + R_D}{1 + (g_m + g_{mb}) r_o}]$$

3.33

The CG stage of Fig.3.51(a) is designed such that its input resistance (seen at node X) matches the signal source resistance, R_S . If $\lambda, \gamma > 0$, prove that $\frac{V_{out}}{V_{in}} = \frac{1 + (g_m + g_{mb}) r_o}{2(1 + \frac{r_o}{R_D})}$

Also, prove that $\frac{V_{out}}{V_{in}} = \frac{R_D}{2R_s}$

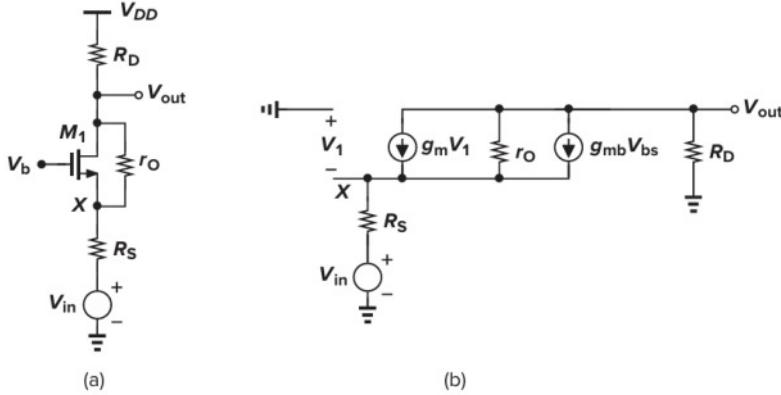


Figure 3.51 (a) CG stage with finite transistor output resistance; (b) small-signal equivalent circuit.

$$R_s = \frac{R_D + r_o}{1 + g_m' r_o}$$

$$A_v = G_m R_{out} = \frac{1}{R_s + \frac{1}{g_m'} || r_o} \times R_D | [(1 + g_m' r_o) R_S + r_o] = \frac{1 + (g_m + g_{mb}) r_o}{2(1 + \frac{r_o}{R_D})} = \frac{R_D}{2R_S}$$

3.34

Calculate the voltage gain of a source follower using the lemma $A_v = G_m R_{out}$. Assume that the circuit drives a load resistance of R_L and $\lambda, \gamma > 0$.

$$A_v = G_m R_{out} = g_m \times [R_L | \frac{r_o}{1 + (g_m + g_{mb}) r_o}]$$

3.35

Calculate the voltage gain of a common-gate stage using the lemma $A_v = G_m R_{out}$. Assume a source resistance of R_S and $\lambda, \gamma > 0$.

$$A_v = G_m R_{out} = (g_m + \frac{1}{r_o})(R_S | | r_o)$$

3.36

How many amplifier topologies can you create using each of the structures shown in Fig.3.87 and no other transistors? (The source and drain terminals can be swapped).

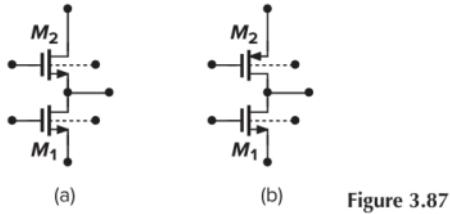


Figure 3.87

(a)CS, CG, SF.

(b)Same.

4 Differential Amplifiers

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

4.1

Suppose the total capacitance between adjacent lines in Fig.4.2 is 10fF and the capacitance from the drains of M_1 and M_2 to ground is 100fF.

- (a) What is the amplitude of the glitches in the analog output in Fig.4.2(a) for a clock swing of 3V?
- (b) If in Fig.4.2(b), the capacitance between L_1 and L_2 is 10% less than that between L_1 and L_3 , what is the amplitude of the glitches in the differential analog output for a clock swing of 3V?

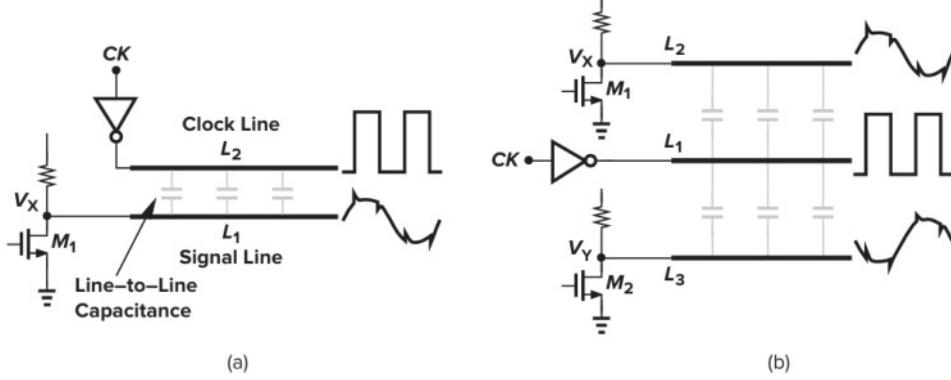


Figure 4.2 (a) Corruption of a signal due to coupling; (b) reduction of coupling by differential operation.

$$(a) \Delta V = 3V \frac{\frac{1}{sC_2}}{\frac{1}{sC_1} + \frac{1}{sC_2}} = 0.273V$$

$$(b) \text{Similar to (a), } \Delta V_1 = 3V \frac{\frac{1}{sC_2}}{\frac{1}{sC_1} + \frac{1}{sC_2}} = 0.248V$$

$$\Delta V_2 = 3V \frac{\frac{1}{sC_3}}{\frac{1}{sC_1} + \frac{1}{sC_3}} = 0.273V$$

$$\Delta V = |\Delta V_1 - \Delta V_2| = 0.025V$$

4.2

Sketch the small-signal differential voltage gain of the circuit shown in Fig.4.9(a) if V_{DD} varies from 0 to 3V. Assume that $(W/L)_{1-3} = 50/0.5$, $V_{in,CM} = 1.3V$, and $V_b = 1V$.

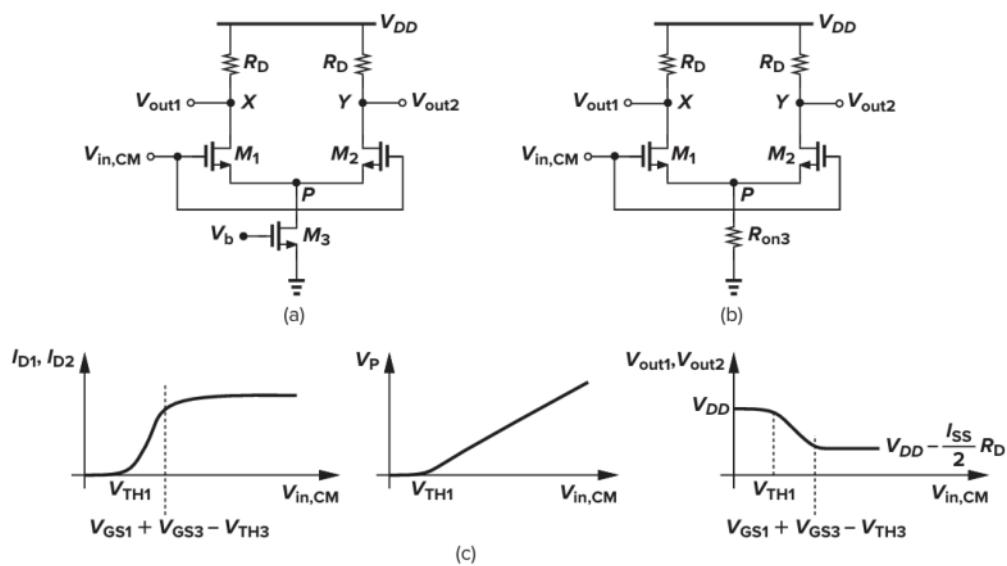
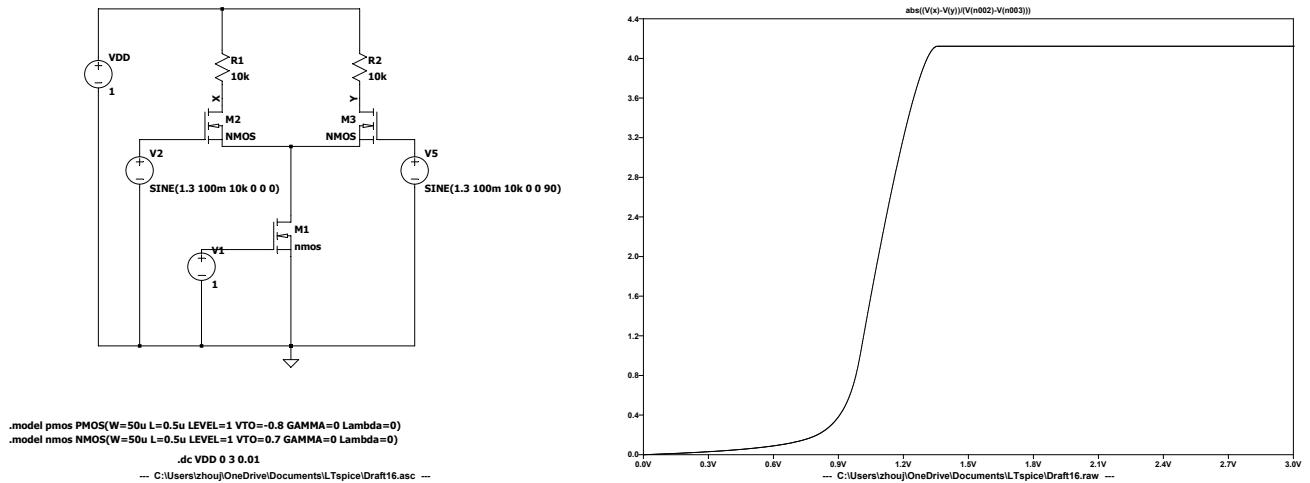
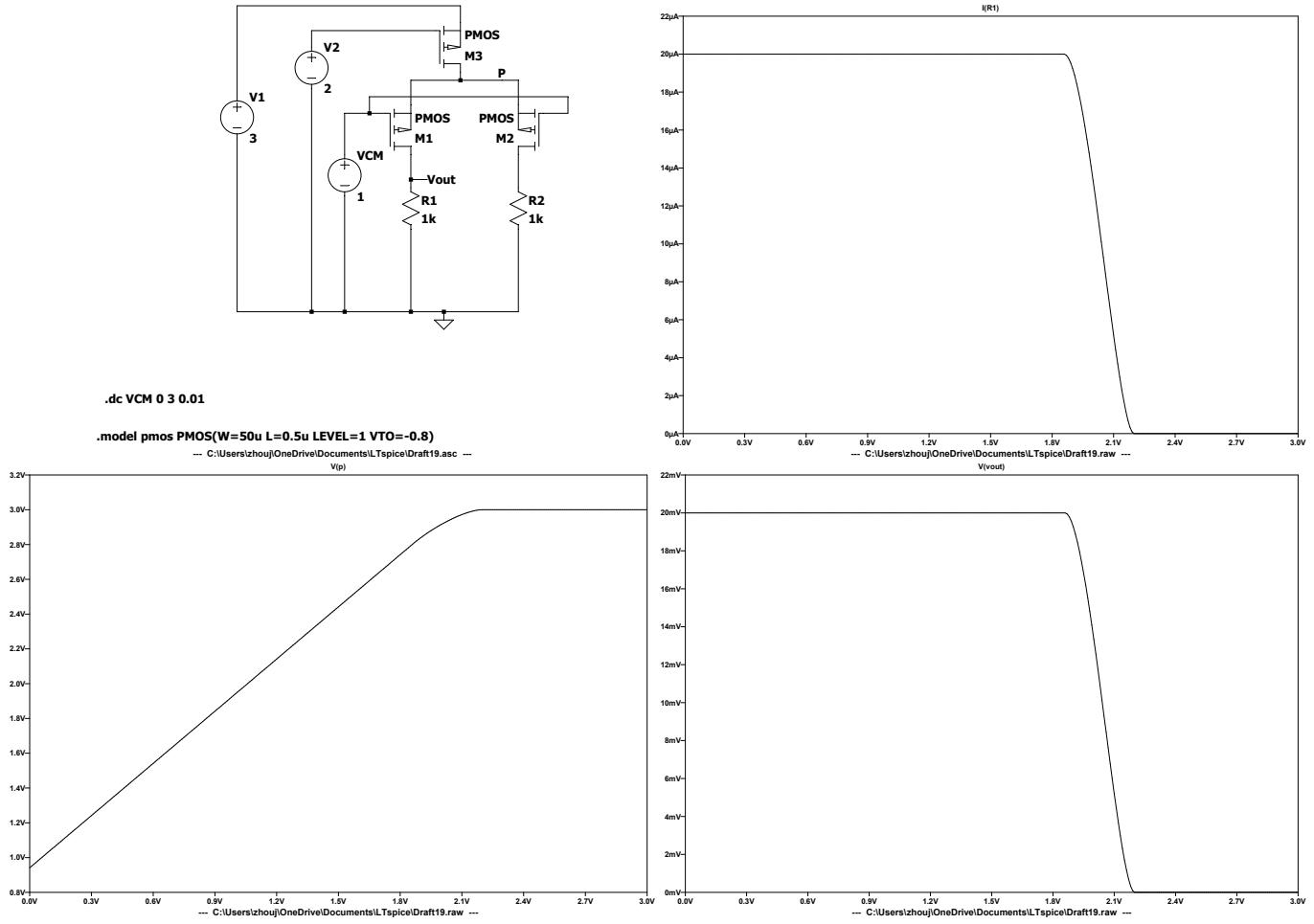


Figure 4.9 (a) Differential pair sensing an input common-mode change; (b) equivalent circuit if M_3 operates in the deep triode region; (c) common-mode input-output characteristics.



4.3

Construct the plots of Fig.4.9(c) for a differential pair using PMOS transistors.



4.4

In the circuit of Fig.4.11, $(W/L)_{1,2} = 50/0.5$ and $I_{SS} = 0.5mA$.

- (a) What is the maximum allowable output voltage swing if $V_{in,CM} = 1.2V$?
- (b) What is the voltage gain under this condition?

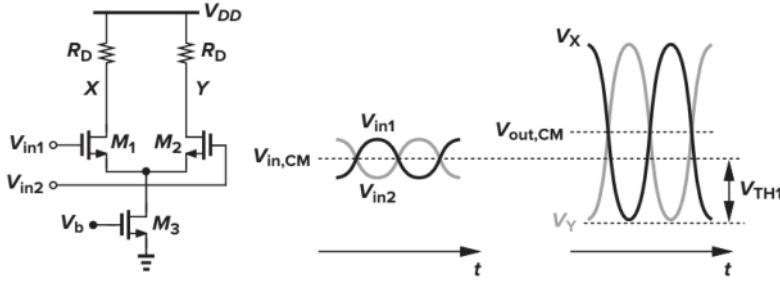


Figure 4.11 Maximum allowable output swings in a differential pair.

$$(a) V_{out} < V_{DD}$$

$$V_{out} \geq V_{in,CM} - V_{th} = 1.2 - 0.7 = 0.5V$$

Single ended : $0.5V - 3V$

Double ended output swing = $2(3 - 0.5) = 5V$

$$(b) g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 2.59mS$$

$$V_{out,CM} = 0.5(3 + 0.5) = 1.75V = V_{DD} - 0.5R_D \times I_{SS}$$

$$R_D = 5k\Omega$$

$$A_v = -g_m R_D = -13$$

4.5

A differential pair uses input NMOS devices with $W/L = 50/0.5$ and a tail current of 1mA.

(a) What is the equilibrium overdrive voltage of each transistor?

(b) How is the tail current shared between the two sides if $V_{in1} - V_{in2} = 50mA$?

(c) What is the equivalent G_m under this condition?

(d) For what value of $V_{in1} - V_{in2}$ does the G_m drop 10%? By 90%?

(a) For input transistors: $\frac{1}{2}I_{SS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} V_{ov}^2$

$$V_{ov} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 0.273V$$

For tail current transistor: $V_{ov} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 0.386V$

$$(b) I_1 + I_2 = I_{SS}$$

$$I = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$$

$$V_{gs} = \sqrt{\frac{2I}{\mu_n C_{ox} \frac{W}{L}}} + V_{th}$$

$$V_{gs1} - V_{gs2} = 50mV$$

$$\sqrt{\frac{2I_1}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_2}{\mu_n C_{ox} \frac{W}{L}}} = 50mV$$

Through calculation, we can get $I_1 = 0.591mA$, $I_2 = 0.409mA$.

$$(c) G_m = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \frac{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - 2\Delta V_{in}}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - \Delta V_{in}^2}} = 3.61mS$$

$$(d) G_{m,max} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 3.66mS$$

And we can replace $0.9G_m$ and $0.1G_m$ to find ΔV .

4.6

Repeat Problem 4.5 with $W/L = 25/0.5$ and compare the results.

(a) For input transistors: $\frac{1}{2}I_{SS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} V_{ov}^2$

$$V_{ov} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 0.386V$$

For tail current transistor: $V_{ov} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 0.546V$

$$(b) \Delta I = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \Delta V \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - \Delta V^2} = 0.129mA$$

$$I_1 + I_2 = 1mA$$

$$I_1 = 0.5645mA, I_2 = 0.4355mA$$

$$(c) G_m = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}} = 2.57mS$$

$$(d) G_{m,max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L}} = 2.588mS$$

4.7

Repeat Problem 4.5 with a tail current of 2mA and compare the results.

$$(a) \text{For input transistors: } \frac{1}{2} I_{SS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2$$

$$V_{ov} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 0.386V$$

$$\text{For tail current transistor: } V_{ov} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 0.546V$$

$$(b) \Delta I = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \Delta V \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} - \Delta V^2 = 0.2583mA$$

$$I_1 + I_2 = 2mA$$

$$I_1 = 1.12915mA, I_2 = 0.87085mA$$

$$(c) G_m = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}} = 5.144mS$$

$$(d) G_{m,max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L}} = 5.176mS$$

4.8

Sketch I_{D1} and I_{D2} in Fig.4.19 versus $V_{in1} - V_{in2}$. For what value of $V_{in1} - V_{in2}$ are the two currents equal?

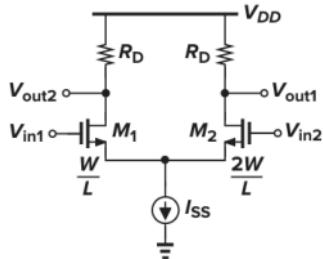


Figure 4.19

$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_p - V_{th})^2$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{2W}{L} (V_{in2} - V_p - V_{th})^2$$

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{2W}{L}}}$$

$$I_{D1} + I_{D2} = I_{SS}$$

$$V_{in1} - V_{in2} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} (1 - \frac{1}{\sqrt{2}})$$

4.9

Consider the circuit of Fig.4.32, assuming $(W/L)_{1,2} = 50/0.5$ and $R_D = 2k\Omega$. Suppose R_{SS} represents the output impedance of an NMOS current source with $(W/L)_{SS} = 50/0.5$ and a drain current of 1mA. The input signal consists of $V_{in,DM} = 10mV_{pp}$ and $V_{in,CM} = 1.5V + V_n(t)$, where $V_n(t)$ denotes noise with a peak-to-peak amplitude of 100mV. Assume that $\Delta R/R = 0.5\%$.

(a) Calculate the output differential signal-to-noise ratio, defined as the signal amplitude divided by the noise amplitude.

(b) Calculate the CMRR.

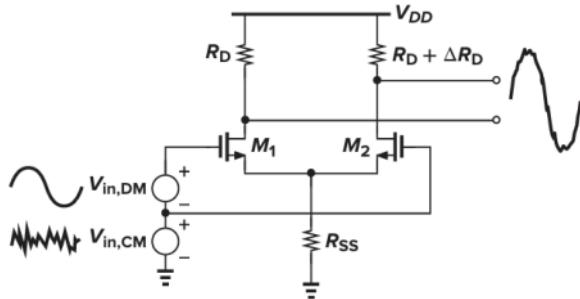


Figure 4.32 Effect of CM noise in the presence of resistor mismatch.

$$(a) A_{DM-DM} = -g_m R_D \quad A_{CM-DM} = -\frac{g_m \Delta R_D}{1+g_m 2R_{SS}}$$

$$SNR = \frac{(A_{DM-DM} V_{in,DM})^2}{(A_{CM-DM} V_{noise})^2} = \left(\frac{g_m R_D}{\frac{g_m \Delta R_D}{1+g_m 2R_{SS}}}\right)^2 \left(\frac{V_{in,DM}}{V_{noise}}\right)^2 = CMRR^2 \left(\frac{V_{in,DM}}{V_{noise}}\right)^2 = 63dB$$

$$(b) g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I} = 3.66mS$$

$$R_{SS} = \frac{1}{\Delta I_D} = 10k\Omega$$

$$CMRR = 14840$$

4.10

Repeat Problem 4.9 if $\Delta R_D = 0$, but M_1 and M_2 suffer from a threshold voltage mismatch of 1mV.

$$A_{DM-DM} = -g_m R_D$$

$$A_{CM} = \frac{-\Delta g_m R_D}{1+g_m 2R_{SS}}$$

$$CMRR = \frac{1+g_m 2R_{SS}}{\frac{\Delta g_m}{g_m}} = 20266.6 = 86dB$$

$$SNR = |CMRR^2| \left(\frac{V_{in,DM}}{V_{noise}}\right)^2 = 4107350 = 66dB$$

4.11

Suppose the differential pair of Fig.4.37(a) is designed with $(W/L)_{1,2} = 50/0.5$, $(W/L)_{3,4} = 10/0.5$, and $I_{SS} = 0.5mA$. Also, I_{SS} is implemented with an NMOS device having $(W/L)_{SS} = 50/0.5$.

(a) What are the minimum and maximum allowable input CM levels if the differential swings at the input and output are small?

(b) For $V_{in,CM} = 1.2V$, sketch the small-signal differential voltage gain as V_{DD} goes from 0 to 3V.

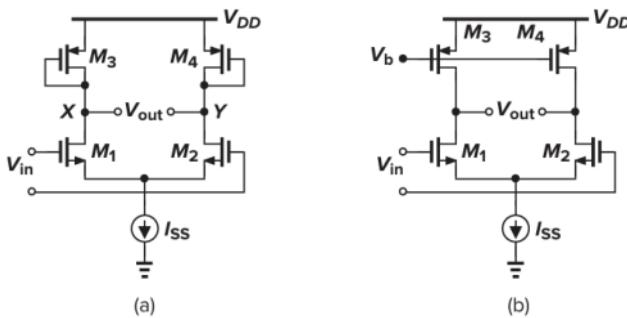


Figure 4.37 Differential pair with (a) diode-connected and (b) current-source loads.

$$(a) V_{gs} - V_{th} = \sqrt{\frac{2I_1}{\mu_n C_{ox} (\frac{W}{L})_1}}$$

$$V_{in} - V_p - V_{th,n} = \sqrt{\frac{2I_1}{\mu_n C_{ox} (\frac{W}{L})_1}}$$

$$V_p \geq (V_{gs} - V_{th})_{SS} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} (\frac{W}{L})_{SS}}}$$

$$V_{in,CM,min} = \sqrt{\frac{2I_1}{\mu_n C_{ox} (\frac{W}{L})_1}} + \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} (\frac{W}{L})_{SS}}} + V_{th,n} = 1.166V$$

$$\text{For M3, } |V_{gs} - V_{th,p}| = \sqrt{\frac{2I_3}{\mu_n C_{ox} (\frac{W}{L})_3}} = 0.8058V$$

$$V_{sg} = 1.6057V$$

$$V_{x,max} = V_{DD} - V_{sg} = 1.29V \quad V_{in,CM,max} - V_p - V_{th,n} \leq V_{x,max} - V_p$$

$$V_{in,CM,max} \leq 2.0943V$$

$$(b) A_v = -g_m \frac{1}{g_{m3}} = \sqrt{\frac{\mu_n C_{ox} \frac{W}{L_1}}{\mu_p C_{ox} \frac{W}{L_2}}} = -4.17$$

4.12

In Problem 4.11, M_1 and M_2 have a threshold voltage mismatch of 1mV. What is the CMRR?

$$CMRR = \frac{A_{DM-DM}}{A_{CM-DM}}$$

ΔV_{th} makes $i_{d1} \neq i_{d2}$

$$i_{d1} = g_{m1}(V_{in,cm} - V_p)$$

$$i_{d2} = g_{m12}(V_{in,cm} - V_p)$$

$$V_{out} = V_{DD} - \frac{1}{g_{m3}} I_{D1}$$

$$v_{out1} = -\frac{1}{g_{m3}} i_{d1} = -\frac{1}{g_{m3}} g_{m1}(V_{in,cm} - V_p)$$

$$v_{out2} = -\frac{1}{g_{m4}} i_{d2} = -\frac{1}{g_{m4}} g_{m2}(V_{in,cm} - V_p)$$

$$v_{out1} - v_{out2} = 0$$

$$A_{CM-DM} = 0$$

$$CMRR = \infty$$

4.13

In Problem 4.11, suppose $W_3 = 10\mu m$, but $W_4 = 11\mu m$. Calculate the CMRR.

$$A_{DM-DM} = -g_m R_D = -g_{m1} \frac{1}{g_{m3}}$$

$$A_{CM-DM} = -\frac{g_m \Delta R_D}{1 + g_m 2R_{SS}}$$

$$CMRR = \frac{1 + g_{m1} 2R_{SS}}{g_{m3} \Delta R_D}$$

$$\Delta R_D = \left| \frac{1}{g_{m3}} - \frac{1}{g_{m4}} \right|$$

$$CMRR = 2246 = 67.03dB$$

4.14

For the differential pairs of Fig.4.37(a) and (b), calculate the differential voltage gain if $I_{SS} = 1mA$, $(W/L)_{1,2} = 50/0.5$, and $(W/L)_{3,4} = 50/1$. What is the minimum allowable input CM level if I_{SS} requires at least 0.4V across it? Using this value for $V_{in,CM}$, calculate the maximum output voltage swing in each case.

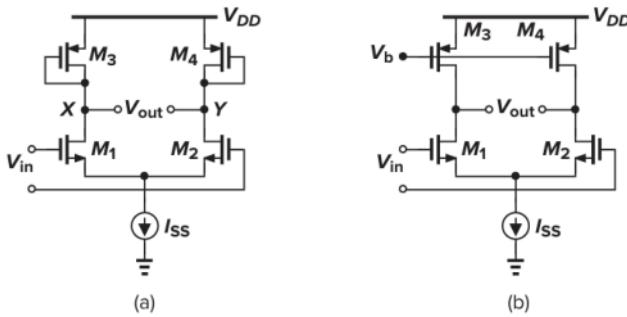


Figure 4.37 Differential pair with (a) diode-connected and (b) current-source loads.

$$(a) A_v = -g_m R_D = -g_{m1} \frac{1}{g_{m3}} = \sqrt{\frac{\mu_n C_{ox} \frac{W}{L_1}}{\mu_p C_{ox} \frac{W}{L_3}}} = -2.644$$

$$V_{in,CM} - V_p - V_{th} = \sqrt{\frac{2I_1}{\mu_n C_{ox} (\frac{W}{L})_1}} = 0.273V$$

$$V_{in,CM} = 0.273 + 0.4 + 0.7 = 1.373V$$

$$V_{out,max} = V_{DD} - |V_{th,p}| = 2.2V$$

$$V_{out,min} = V_{in,CM} - V_{th,n} = 0.673V$$

But, the maximum current for pmos to get is I_{SS} , $|V_{GS}| - |V_{th,p}| = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} (\frac{W}{L})_3}} = 1.02V$

$$|V_{GS}| = 1.82V$$

$$V_{out,min} = 3V - 1.82V = 1.18V$$

$$\text{Maximum ouput voltage swing} = 2(2.2 - 1.18) = 2.04V$$

$$(b) A_v = -g_m(r_{op}||r_{on})$$

$$r_{op} = \frac{1}{\lambda_p I_3} = 20k\Omega$$

$$r_{on} = \frac{1}{\lambda_n I_3} = 20k\Omega$$

$$A_v = -\sqrt{2\mu_n C_{ox}(\frac{W}{L})_1 I_1} 10k\Omega = -36.6 V_{in,CM} - V_p - V_{th} = \sqrt{\frac{2I_1}{\mu_n C_{ox}(\frac{W}{L})_1}} = 0.273V$$

$$V_{in,CM} = 0.273 + 0.4 + 0.7 = 1.373V$$

The top PMOS must operate in triode region.

$$|V_{GS} - V_{th,p}| = \sqrt{\frac{I_{SS}}{\mu_n C_{ox}(\frac{W}{L})_3}} = 0.722V$$

$$V_{x,max} = 3 - 0.722 = 2.28V$$

$$V_{out,min} = V_{in,CM} - V_{th,n} = 0.673V$$

$$\text{Maximum output voltage swing} = 2(2.28 - 0.673) = 3.22V$$

4.15

In the circuit of Fig.4.39(a), assume that $I_{SS} = 1mA$ and $W/L = 50/0.5$ for all the transistors.

(a) Determine the voltage gain.

(b) Calculate V_b such that $I_{D5} = I_{D6} = 0.8(I_{SS}/2)$

(c) If I_{SS} requires a minimum voltage of 0.4V, what is the maximum differential output swing?

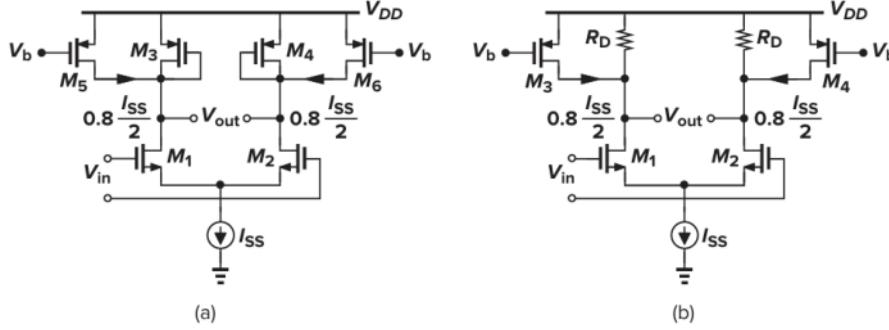


Figure 4.39 Addition of current sources to increase the voltage gain with (a) diode-connected loads and (b) resistive loads.

$$(a) A_v = -g_{m1} \frac{1}{g_{m3}} = \sqrt{\frac{\mu_n C_{ox} \frac{W}{L} I_{D1}}{\mu_p C_{ox} \frac{W}{L} I_{D3}}} = \sqrt{\frac{\mu_n}{\mu_p}} \sqrt{5} = -4.18$$

$$(b) |V_{GS} - V_{th,p}| = \sqrt{\frac{2 \times 0.8 \times I_{SS}/2}{\mu_n C_{ox}(\frac{W}{L})_3}} = 0.457V$$

$$|V_{GS}| = 1.257V$$

$$V_b = 3 - 1.257 = 1.743V$$

$$(c) \text{For M1, } V_{GS} - V_{th} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox}(\frac{W}{L})_1}} = 0.273V$$

$$V_{GS} = 0.973V$$

$$V_{out,min} - V_p \geq 0.273V$$

$$V_{out,min} \geq 0.673V \text{ Another minimum is when M3 absorbs the current on M4.}$$

$$|V_{GS} - V_{th,p}| = \sqrt{\frac{2 \times 0.2 \times I_{SS}/2}{\mu_n C_{ox}(\frac{W}{L})_3}} = 0.323V$$

$$V_{GS} = 0.323 + 0.8 = 1.123V$$

$$V_{out,min} = V_{DD} - V_{GS} = 1.877V$$

$$V_{out,max} = V_{DD} - |V_{th,p}| = 2.2V$$

$$\text{Maximum output voltage swing} = 2(2.2 - 1.877) = 0.646V$$

4.16

Assuming that all the circuits shown in Fig.4.44 are symmetric, sketch V_{out} as (a) V_{in1} and V_{in2} vary differentially from zero to V_{DD} , and (b) V_{in1} and V_{in2} are equal and vary from zero to V_{DD} .

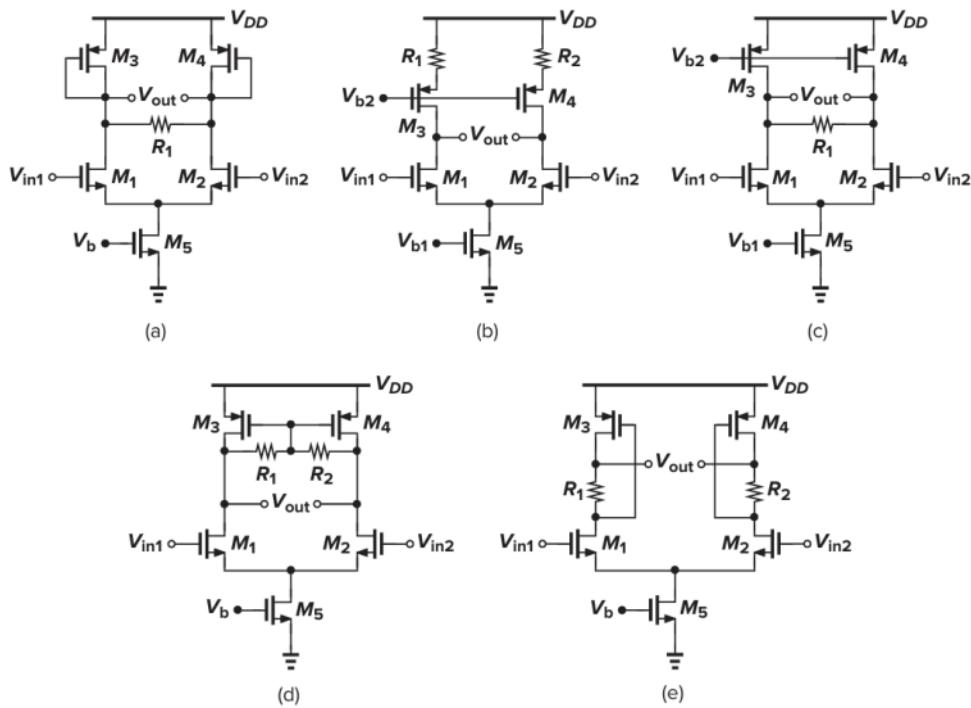
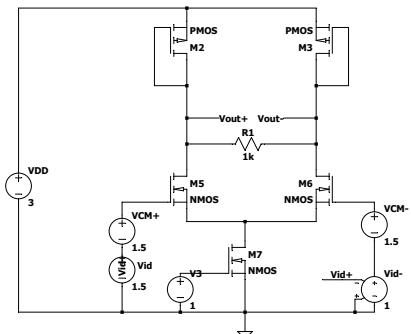
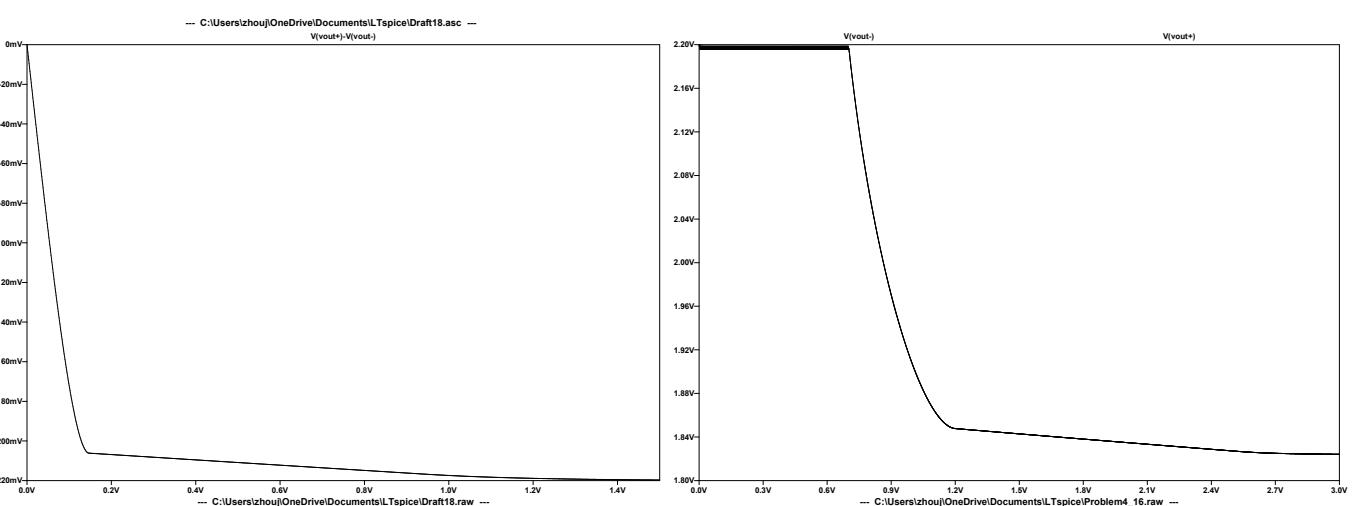


Figure 4.44



```
.dc Vid 0 1.5 0.001
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



Others are similar.

4.17

Assuming that all the circuits shown in Fig.4.45 are symmmatric, sketch V_{out} as (a) V_{in1} and V_{in2} vary differentially from zero to V_{DD} , and (b) V_{in1} and V_{in2} are equal and vary from zero to V_{DD} .

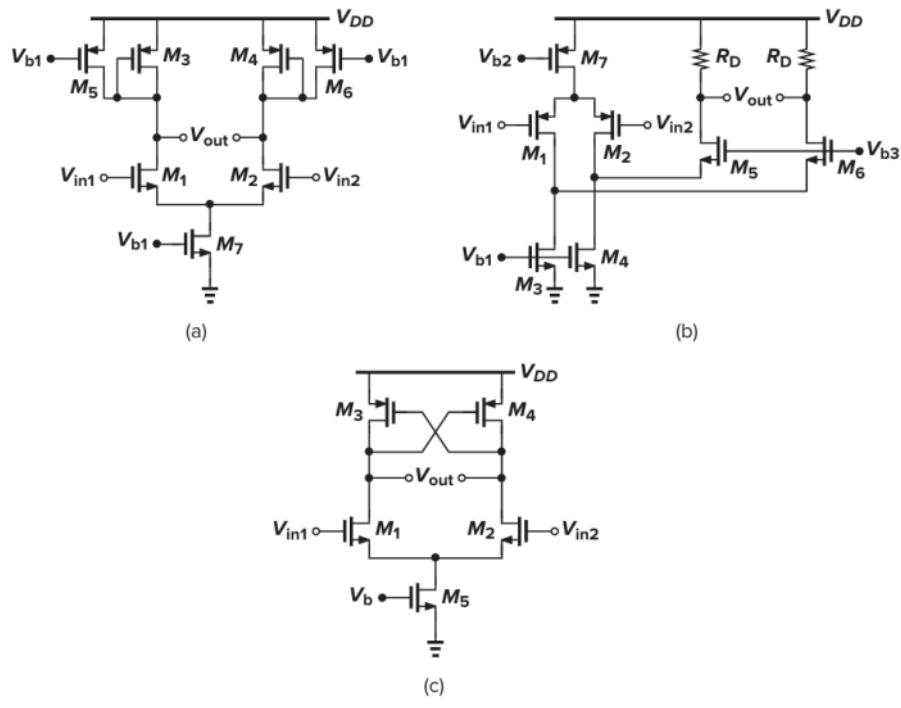


Figure 4.45

Similar as 4.16.

4.18

Assuming that all the transistors in the circuits of Figs.4.44 and 4.45 are saturated and $\lambda \neq 0$, calculate the small-signal differential voltage gain of each circuit.

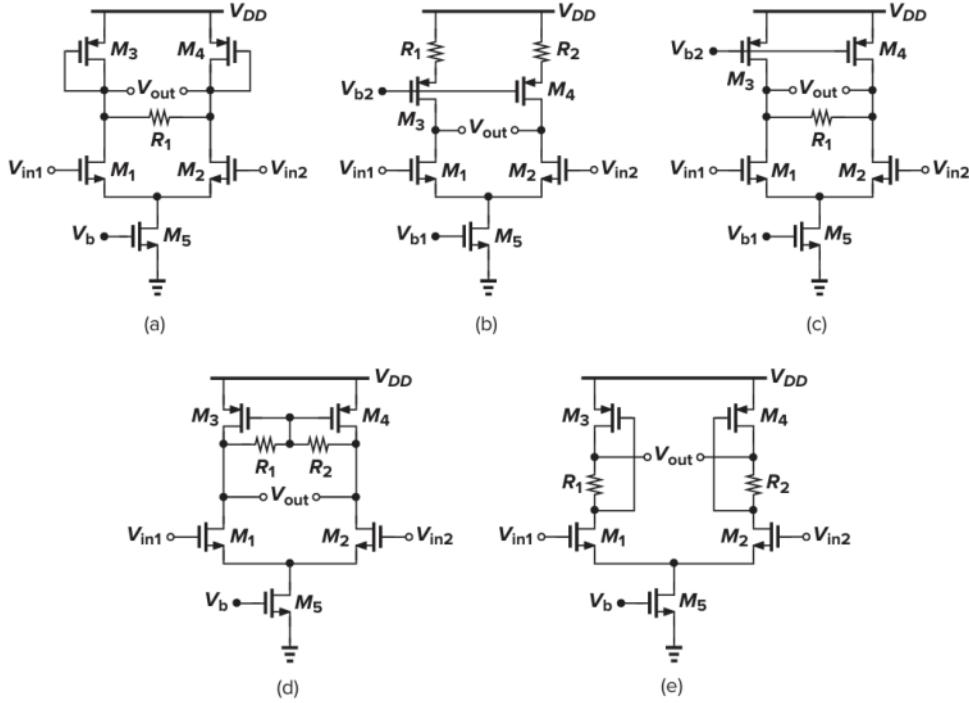


Figure 4.44

$$(a) A_v = -g_{m1} \left(\frac{1}{g_{m3}} \parallel 0.5R_1 \parallel r_{o1} \parallel r_{o3} \right) = -g_{m1} \left(\frac{1}{g_{m3}} \parallel 0.5R_1 \right)$$

$$(b) A_v = -g_{m1} (r_{o1} \parallel g_{m3} r_{o3} R_1)$$

$$(c) A_v = -g_{m1} (r_{o3} \parallel 0.5R_1 \parallel r_{o1})$$

$$(d) A_v = -g_{m1} (r_{o3} \parallel R_1 \parallel r_{o1})$$

$$(e) \text{Use small-signal diagram, } g_{m3}V_x + \frac{V_{out}}{r_{o3}} + \frac{V_{out} - V_x}{R_1} = 0$$

$$\frac{V_{out} - V_x}{R_1} = \frac{V_x}{r_{o1}} + g_{m1}V_{in}$$

$$A_v = \frac{-g_{m1}}{g_{m3}} (1 - g_{m3}R_1)$$

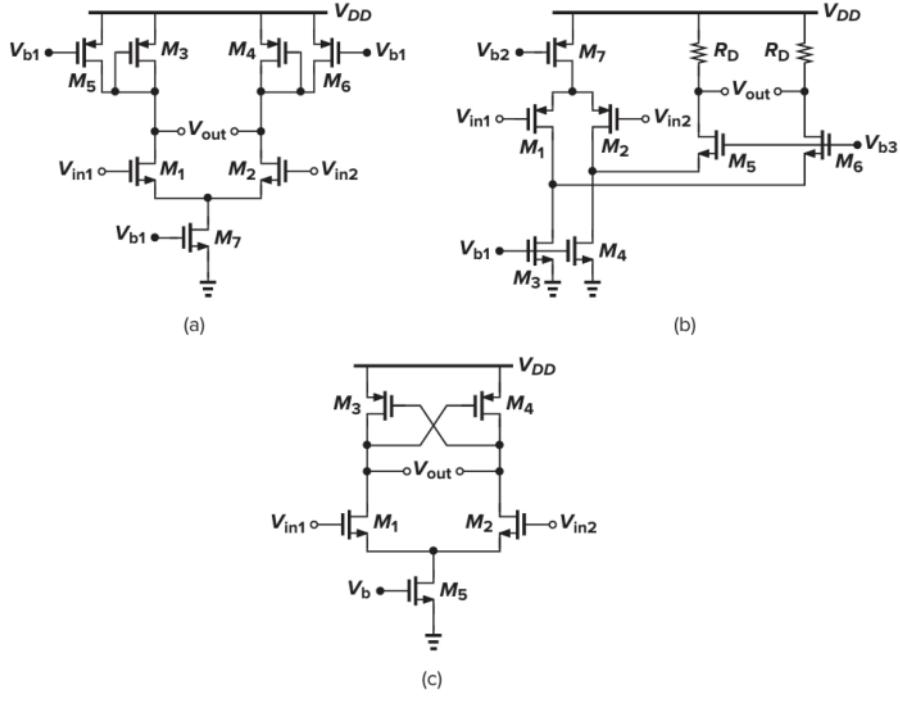


Figure 4.45

- (a) $A_v = -g_{m1} \left(\frac{1}{g_{m3}} || r_{o1} || r_{o3} || r_{o5} \right)$
- (b) $A_v = -G_m R_{out} = -g_{m1} [R_D || g_{m6} r_{o6} (r_{o3} || r_{o1})]$
- (c) $A_v = -g_{m1} \left(-\frac{1}{g_{m3}} || r_{o3} || r_{o1} \right)$

4.19

Consider the circuit shown in Fig.4.46.

- (a) Sketch V_{out} as V_{in1} and V_{in2} vary differentially from zero to V_{DD} (b) If $\lambda = 0$, obtain an expression for the voltage gain. What is the voltage gain if $W_{3,4} = 0.8W_{5,6}$?

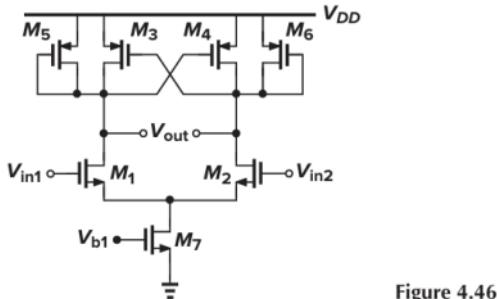
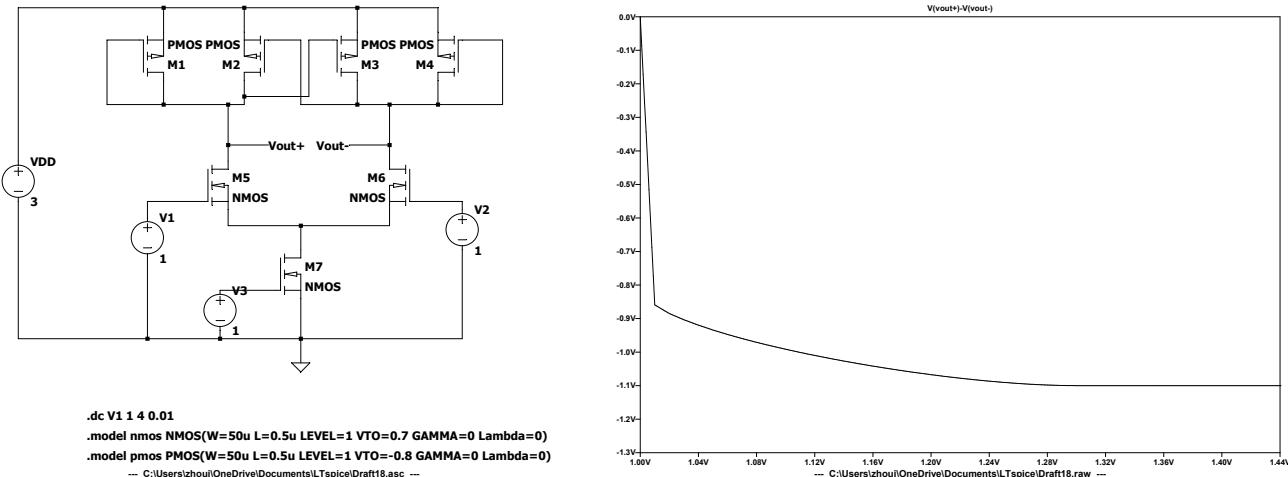


Figure 4.46



$$\begin{aligned}
 & .dc V1 1 4 0.01 \\
 & .model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0 Lambda=0) \\
 & .model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0 Lambda=0) \\
 & \dots C:\Users\zhouj\OneDrive\Documents\LTspice\Draft18.asc \dots \\
 (a) \quad & A_v = -g_m 1 \left(\frac{1}{g_m 5} \parallel \frac{-1}{g_m 3} \right) = \frac{-g_m 1}{g_m 3 - g_m 5} \\
 & \frac{g_m 3}{g_m 5} = 0.8 \\
 & A_v = 5 \frac{g_m 1}{g_m 5}
 \end{aligned}$$

4.20

For the circuit shown in Fig.4.47,

- (a) Sketch V_{out} , V_X and V_Y as V_{in1} and V_{in2} vary differentially from zero to V_{DD} .
- (b) Calculate the small-signal differential voltage gain.

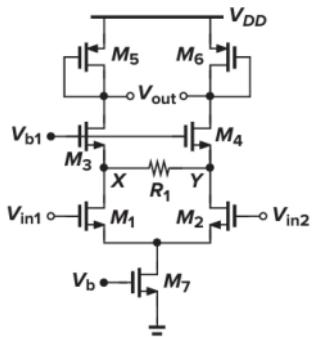
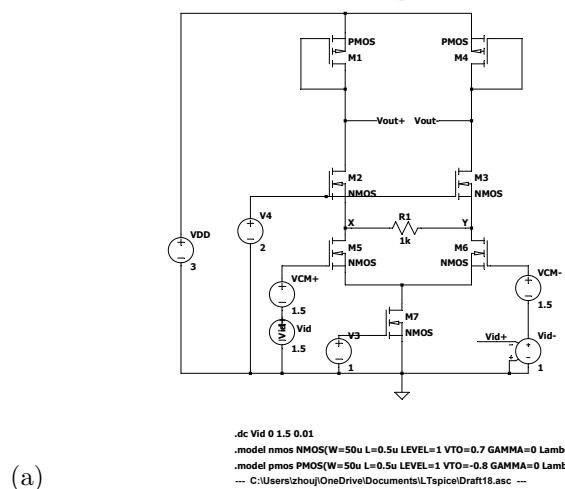
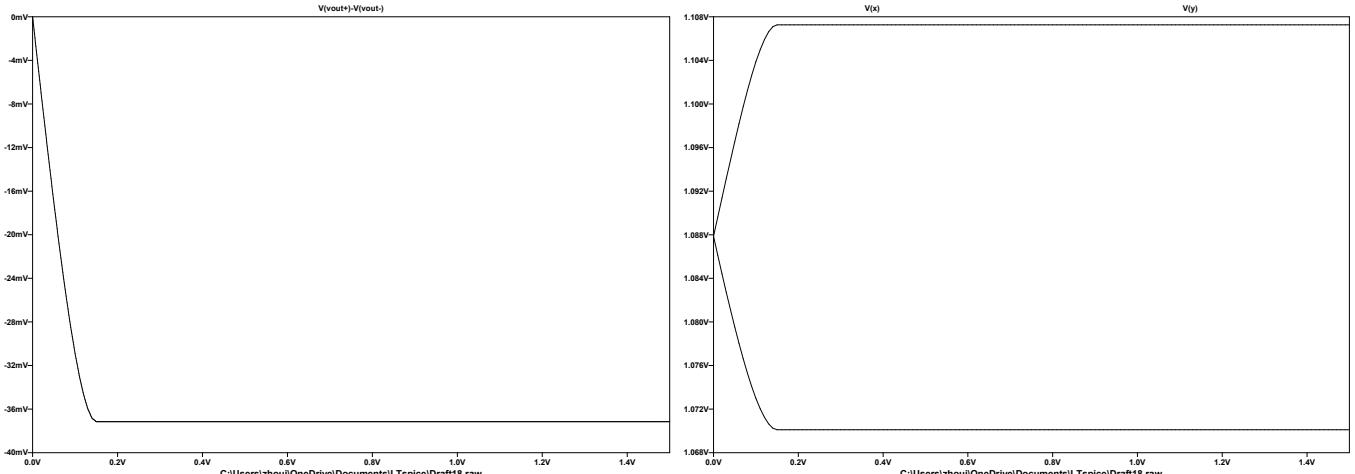


Figure 4.47



$$\begin{aligned}
 & .dc Vid 0 1.5 0.01 \\
 & .model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0 Lambda=0) \\
 & .model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0 Lambda=0) \\
 & \dots C:\Users\zhouj\OneDrive\Documents\LTspice\Draft18.asc \dots
 \end{aligned}$$

(a)



$$(b) G_m = \frac{g_{m1} 0.5 R_1}{\frac{1}{g_{m3}} + 0.5 R_1} = \frac{g_{m1} g_{m3} R_1}{2 + g_{m3} R_1}$$

$$R_{out} \approx \frac{1}{g_{m5}}$$

$$A_v = -G_m R_{out}$$

4.21

Assuming no symmetry in the circuit of Fig.4.48 and using no equivalent circuits, calculate the small-signal voltage gain $(V_{out})/(V_{in1} - V_{in2})$ if $\lambda = 0$ and $\gamma \neq 0$.

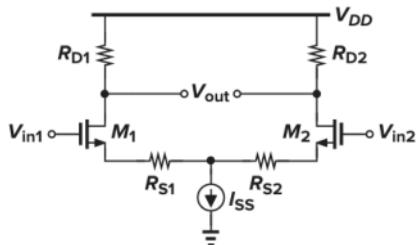


Figure 4.48

$$R_{eq} = R_{S1} + R_{S2} + \frac{1}{g_{m2} + g_{mb2}}$$

$$V_{out} = -(G_{m1} \Delta V_{in1} - G_{m2} \Delta V_{in2})(R_1 + R_2)$$

4.22

Due to a manufacturing defect, a large parasitic resistance has appeared between the drain and source terminals of M_1 in Fig.4.49. Assuming $\lambda = \gamma = 0$, calculate the small-signal gain, common-mode gain, and CMRR.

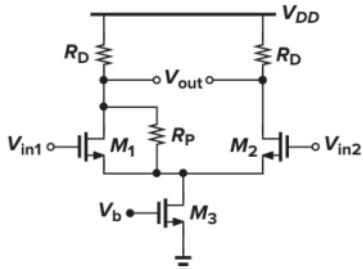


Figure 4.49

$$A_{DM-DM} = -g_m R_D$$

$$A_{CM-DM} = A_x - A_y = -g_m R_D || R_p - (-g_m R_D) = g_m \frac{R_D^2}{R_D + R_p}$$

$$CMRR = \frac{A_{DM-DM}}{A_{CM-DM}} = 1 + \frac{R_p}{R_D}$$

4.23

Due to a manufacturing defect, a large parasitic resistance has appeared between the drains of M1 and M4 in the circuit of Fig.4.50. Assuming $\lambda = \gamma = 0$, calculate the small-signal gain, common-mode gain, and CMRR.

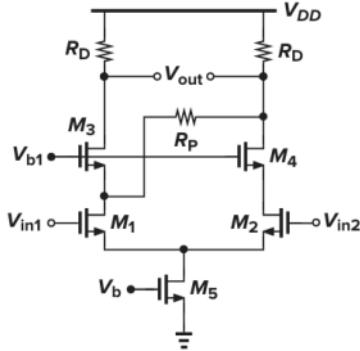


Figure 4.50

$$A_{DM-DM} = -G_m R_{out} = g_m R_D$$

$$A_{CM-DM} = 0$$

$$CMRR = \infty$$

4.24

In the circuit of Fig.4.51, all of the transistors have a W/L of 50/0.5, and M_3 and M_4 are to operate in the deep triode region with an on-resistance of $2k\Omega$. Assuming that $I_{D5} = 20\mu A$ and $\lambda = \gamma = 0$, calculate the input common-mode level that yields such resistance. Sketch V_{out1} and V_{out2} as V_{in1} and V_{in2} vary differentially from 0 to V_{DD} .

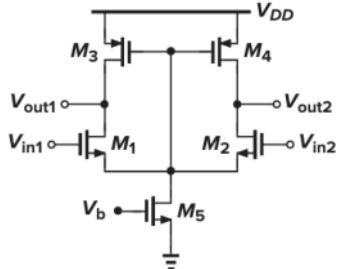


Figure 4.51

$$I = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (2(V_{GS} - V_{th})V_{DS} - V_{DS}^2)$$

When it is in deep triode region, V_{DS} is very small.

$$I = \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})V_{DS}$$

$$R_{on} = \frac{V_{DS}}{I} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})} = 2k\Omega$$

And we could get $|V_{GS} - V_{THP}| = 0.130V$

$$V_{GS} = 0.93V$$

$$\text{For } M1, V_{GS} - V_{thn} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} = 0.0386V$$

$$V_p = V_{DD} - V_{GS3} = 2.07V$$

$$V_{in,CM} = V_p + V_{GS1} = 2.8V$$

4.25

In the circuit of Fig.4.37(b), $(W/L)_{1-4} = 50/0.5$, and $I_{SS} = 1mA$.

(a) What is the small-signal differential gain?

(b) For $V_{in,CM} = 1.5V$, what is the maximum allowable output voltage swing?

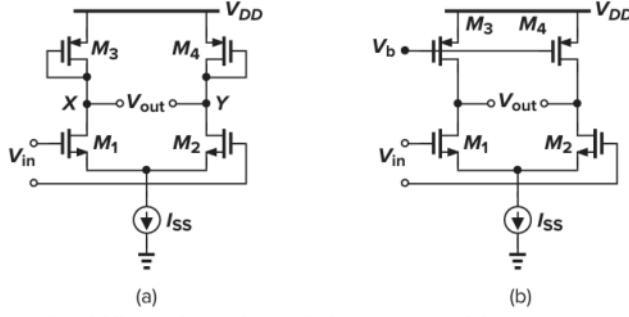


Figure 4.37 Differential pair with (a) diode-connected and (b) current-source loads.

$$(a) A_v = -g_{m1}r_{o1}||r_{o2}$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_1} I_1 = 3.66 \mu A$$

$$r_{o1} = \frac{1}{\lambda_n I_1} = 20 k\Omega$$

$$r_{o2} = \frac{1}{\lambda_p I_1} = 10 k\Omega$$

$$A_v = -24.4$$

$$(b) V_{out,min} - V_p > V_{in} - V_p - V_{thn}$$

$$|V_{GS} - V_{th,p}| = \sqrt{\frac{I_{SS}}{\mu_n C_{ox}(\frac{W}{L})_3}} = 0.51 V$$

$$V_{out,max} = 3 - 0.51 = 2.49 V$$

$$Swing = 2(2.49 - 0.8) = 3.38 V$$

4.26

In the circuit of Fig.4.39, assume that $M5$ and $M6$ have a small threshold voltage mismatch of ΔV and I_{SS} as an output impedance R_{SS} . Calculate the CMRR.

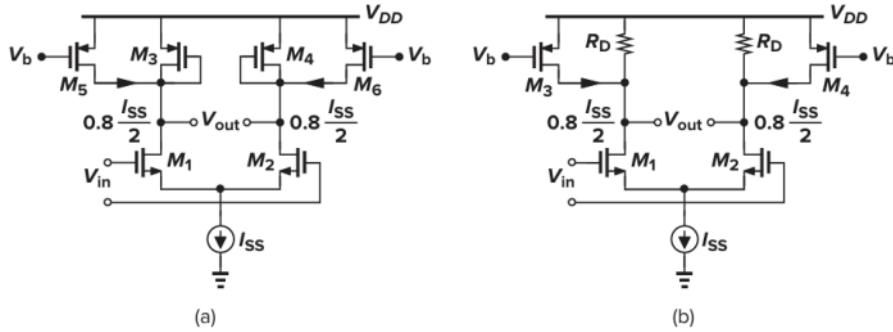


Figure 4.39 Addition of current sources to increase the voltage gain with (a) diode-connected loads and (b) resistive loads.

$$A_{DM-DM} = -g_{m1}/g_{m3} = \sqrt{\frac{\mu_n}{\mu_p}} \sqrt{5}$$

$$g_m = \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{th})$$

$$\Delta g_m = \mu_p C_{ox} \frac{W}{L} \Delta V_{th}$$

$$A_{CM-DM} = A_x - A_y = -\frac{\Delta g_m}{g_{m3}(1+2g_{m1}R_{SS})}$$

$$CMRR = \left| \frac{A_{DM-DM}}{A_{CM-DM}} \right| = \frac{(1+2g_m R_{SS})g_{m3}}{\Delta g_m}$$

4.27

What happens if R_{SS} in Eq.(4.56) become very large? Can we obtain the same result by analyzing a differential pair having an ideal tail current source but $g_{m1} \neq g_{m2}$?

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}$$

If R_D become very large, $|A_{DM}| = g_m R_D$

4.28

In Example 4.5, how much input dc imbalance can be tolerated if the small-signal gain must not drop by more than 5 %?

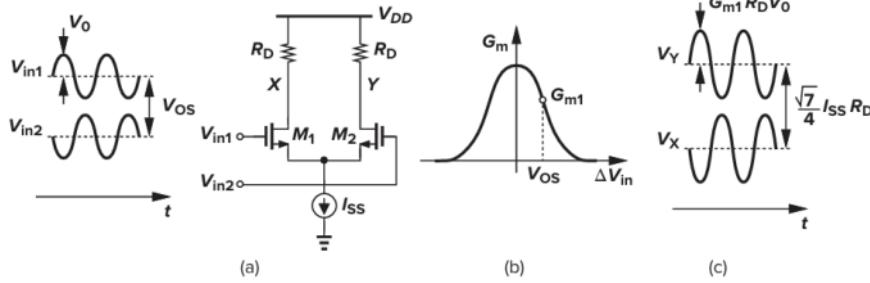


Figure 4.15

$$G_m = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}$$

$$G_{m0} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

$$0.95G_{m0} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - \Delta V_{in}^2}}$$

We can get $\Delta V_{in} = 0.25V_{ov}$

4.29

In the lemma illustrated in Fig. 4.20, suppose channel-length modulation is not neglected. Assuming the two devices are connected to two equal load resistors, explain intuitively why the lemma still holds.

Lemma Consider the symmetric circuit shown in Fig. 4.20(a), where D₁ and D₂ represent any three-terminal active device. Suppose V_{in1} and V_{in2} change differentially, the former from V₀ to V₀ + ΔV_{in} and the latter from V₀ to V₀ - ΔV_{in} [Fig. 4.20(b)]. Then, if the circuit remains linear, V_P does not change.

Assume λ = 0.

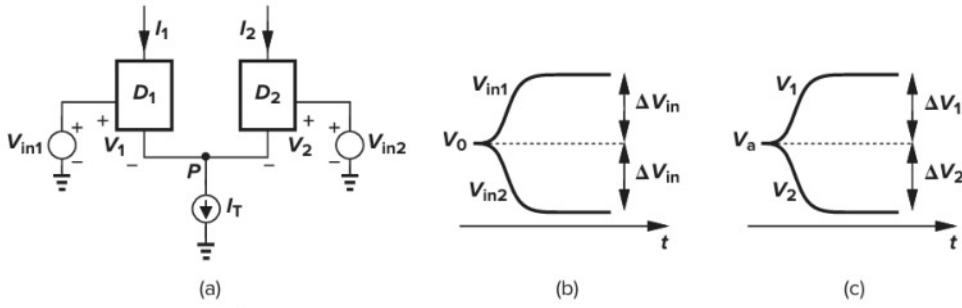


Figure 4.20 Illustration of why node P is a virtual ground.

Use Thevenin's theorem to replace current source in parallel with a resistor with a voltage source in series with a resistor. $\frac{\Delta V_p - g_m(\Delta V_{in} - \Delta V_p)r_o}{r_o + R_D} + \frac{\Delta V_p - g_m(-\Delta V_{in} - \Delta V_p)r_o}{r_o + R_D}$
 $\Delta V_p = 0$

4.30

Does the lemma in Fig. 4.20 still hold if the device have body effect? Explain.

$$\Delta I_1 = g_m(\Delta V_{in} - \Delta V_p) + g_{mb}(0 - \Delta V_p)$$

$$\Delta I_2 = g_m(-\Delta V_{in} - \Delta V_p) + g_{mb}(0 - \Delta V_p)$$

As $\Delta I_1 + \Delta I_2 = 0$

$$\Delta V_p = 0$$

4.31

Repeat Example 4.7 using Method I.

Calculate the differential gain of the circuit of Fig.4.22(a) if $\lambda \neq 0$

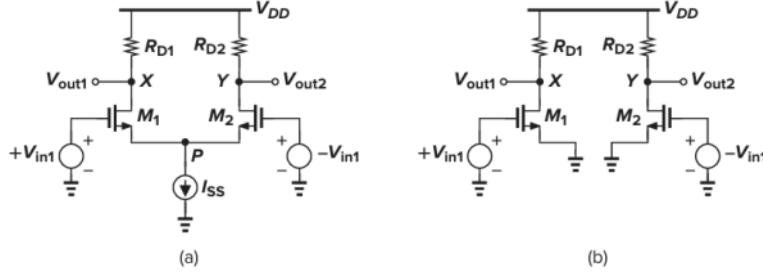


Figure 4.22 Application of the half-circuit concept.

Use small-signal diagram

$$\frac{-V_X}{R_D} = g_m(V_{in1} - V_p) + \frac{V_X - V_p}{r_o}$$

$$\frac{-V_Y}{R_D} = g_m(-V_p) + \frac{V_Y - V_p}{r_o}$$

$$\frac{-V_X}{R_D} = \frac{V_Y}{R_D}$$

$$(V_Y - V_X) = \frac{g_m}{\frac{1}{R_D} + \frac{1}{r_o}} V_{in1}$$

$$(V_X - V_Y) = \frac{g_m}{\frac{1}{R_D} + \frac{1}{r_o}} V_{in2}$$

$$A_V = \frac{V_Y - V_X}{V_{in1} - V_{in2}} = \frac{1}{2} \frac{g_m}{\frac{1}{R_D} + \frac{1}{r_o}}$$

4.32

Prove the lemma illustrated in Fig.4.20 if the tail current source is replaced by a resistor R_T .

$$\Delta I_1 = g_m(\Delta V_{in} - \Delta V_p)$$

$$\Delta I_2 = g_m(-\Delta V_{in} - \Delta V_p)$$

$$\Delta I_p = \Delta V_p / R_{SS}$$

$$\Delta I_1 + \Delta I_2 = \Delta I_p$$

$$\Delta V_p = 0$$

4.33

What happens to the plots on Fig.4.13 as W/L increases? Determine the area under the G_m plot and use the result to explain why the peak G_m must increase as W/L increases.

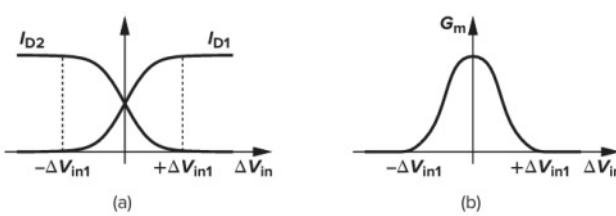


Figure 4.13 Variation of drain currents and overall transconductance of a differential pair versus input voltage.

The area under the G_m is ΔI .

As W/L increases, V_{od} decreases, and as I is constant, peak G_m must increase.

4.34

Assuming that I_1 and I_{SS} in Fig.4.52 are ideal and $\lambda, \gamma > 0$, determine V_{out1}/V_{in} and V_{out2}/V_{in} .

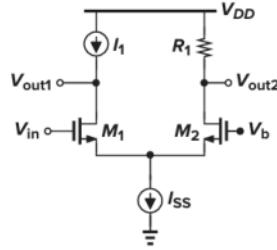


Figure 4.52

$$V_{out2}/V_{in} = 0$$

$$V_{out}/V_{in} = g_{m1}r_o$$

4.35

In Problem 4.11, suppose $M3$ and $M4$ have a threshold voltage mismatch of 1mV. Calculate the CMRR.

Suppose the differential pair of Fig.4.37(a) is designed with $(W/L)_{1,2} = 50/0.5$, $(W/L)_{3,4} = 10/0.5$, and $I_{SS} = 0.5mA$. Also, I_{SS} is implemented with an NMOS device having $(W/L)_{SS} = 50/0.5$.

(a) What are the minimum and maximum allowable input CM levels if the differential swings at the input and output are small?

(b) For $V_{in,CM} = 1.2V$, sketch the small-signal differential voltage gain as V_{DD} goes from 0 to 3V.

$$CMRR = \left| \frac{A_{DM-DM}}{A_{CM-DM}} \right| A_{DM-DM} = g_{m1} \frac{1}{g_{m3}}$$

$$A_{CM-DM} = \frac{\frac{g_{m1}}{g_{m3}} \frac{\Delta g_{m3}}{g_{m3}}}{1 + 2r_o g_m}$$

$$CMRR = \frac{1 + g_m 2r_o}{\frac{\Delta g_{m3}}{g_{m3}}} = 83928$$

5 CurrentMirrorsAndBiasingTechniques

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

5.1

In Fig.5.2, assume that $(W/L)_1 = 50/0.5$, $\lambda = 0$, $I_{out} = 0.5mA$, and M_1 is saturated.

- (a) Determine R_2/R_1 .
- (b) Calculate the sensitivity of I_{out} to V_{DD} , defined as $\delta I_{out}/\delta V_{DD}$ and normalized to I_{out} .
- (c) How much does I_{out} change if V_{TH} changes by 50mV?
- (d) If the temperature dependence of μ_n is expressed as $\mu_n \propto T^{-3/2}$ but V_{TH} is independent of temperature, how much does I_{out} vary if T changes from 300K to 370K?
- (e) What is the worst-case change in I_{out} if V_{DD} changes by 10 %, V_{TH} changes by 50mV, and T changes from 300K to 370K?

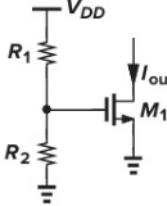


Figure 5.2 Definition of current by resistive divider.

$$(a) V_b = \sqrt{\frac{2I_{out}W}{\mu_n C_{ox} L}} + V_{th} = 0.97V$$

$$R_2/(R_2 + R_1) = 0.97/3$$

$$R_2/R_1 = 0.48$$

$$(b) I_{out} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \left(\frac{R_2}{R_1+R_2} V_{DD} - V_{th} \right)^2$$

$$\frac{\delta I_{out}}{\delta V_{DD}} = \mu_n C_{ox} \frac{W}{L} \left(\frac{R_2}{R_1+R_2} V_{DD} - V_{th} \right) \frac{R_2}{R_1+R_2}$$

$$\frac{\delta I_{out}}{\delta V_{DD}} = 2.376 I_{out}$$

$$(c) I_{out'}/I_{out} = \frac{\left(\frac{R_2}{R_1+R_2} V_{DD} - V_{th'} \right)^2}{\left(\frac{R_2}{R_1+R_2} V_{DD} - V_{th} \right)^2} = 0.667$$

$$(d) I = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$I_{out'}/I_{out} = \left(\frac{T'}{T} \right)^{-3/2} = (370/300)^{-3/2} = 0.73$$

$$(e) I = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{1}{2}kT^{-3/2}C_{ox} \frac{W}{L} \left(\frac{R_2}{R_1+R_2} V_{DD} - V_{th} \right)^2$$

$$I_{out'}/I_{out} = \left(\frac{T'}{T} \right)^{-3/2} \frac{\left(\frac{R_2}{R_1+R_2} 0.9V_{DD} - V_{th'} \right)^2}{\left(\frac{R_2}{R_1+R_2} V_{DD} - V_{th} \right)^2} = 0.155$$

5.2

Consider the circuit of Fig.5.7. Assuming I_{REF} is ideal, sketch I_{out} versus V_{DD} varies from 0 to 3V.

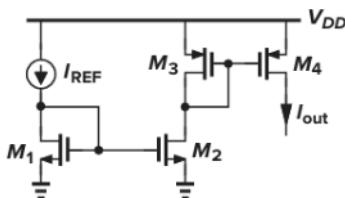
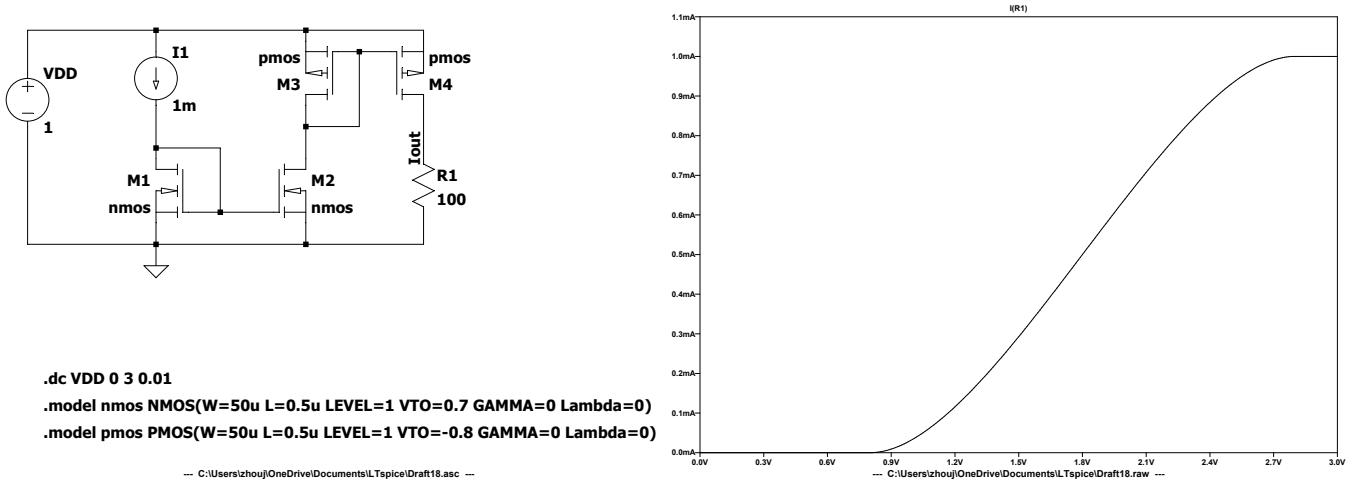


Figure 5.7



5.3

In the circuit of Fig.5.8, $(W/L)_N = 10/0.5$, $(W/L)_P = 10/0.5$, and $I_{REF} = 100\mu\text{A}$. The input CM level applied to the gates of M_1 and M_2 is equal to 1.3V.

- (a) Assuming $\lambda = 0$, calculate V_p and the drain voltage of the PMOS diode-connected transistors.
- (b) Now take channel-length modulation into account to determine I_T and the drain current of the PMOS diode-connected transistors more accurately.

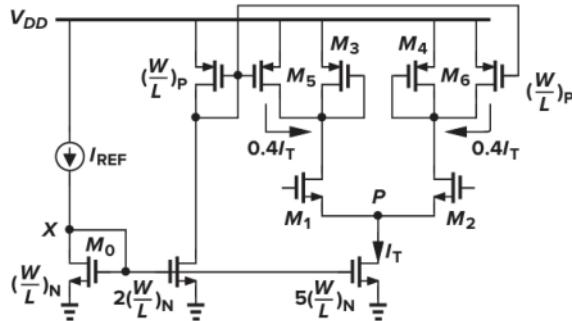


Figure 5.8 Current mirrors used to bias a differential amplifier.

$$(a) \text{ For } M_1, V_{GS} - V_{TH} = \sqrt{\frac{I_T}{\mu_n C_{ox} (W/L)_1}} = 0.43V.$$

$$V_{GS} = 1.13V$$

$$V_P = 0.168V$$

$$\text{For } M_3, V_{GS} - |V_{TH,P}| = \sqrt{\frac{0.2I_T}{\mu_p C_{ox} (W/L)_3}} = 0.361V.$$

$$|V_{GS}| = 1.161V$$

$$V_D = 3V - 1.161V = 1.83V$$

$$(b) I_X = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$I_T = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS,T})$$

$$\Delta I = I_{REF} \lambda \Delta V_{DS} = 0.08I_{REF}$$

$$I_T = I - \Delta I = 0.92I_{REF} = 460\mu\text{A}$$

5.4

In the circuit of Fig.5.11, sketch V_{out} versus V_{DD} as V_{DD} varies from 0 to 3V.

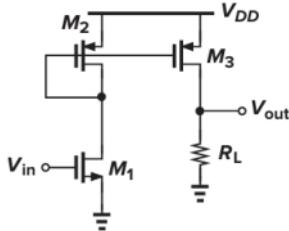
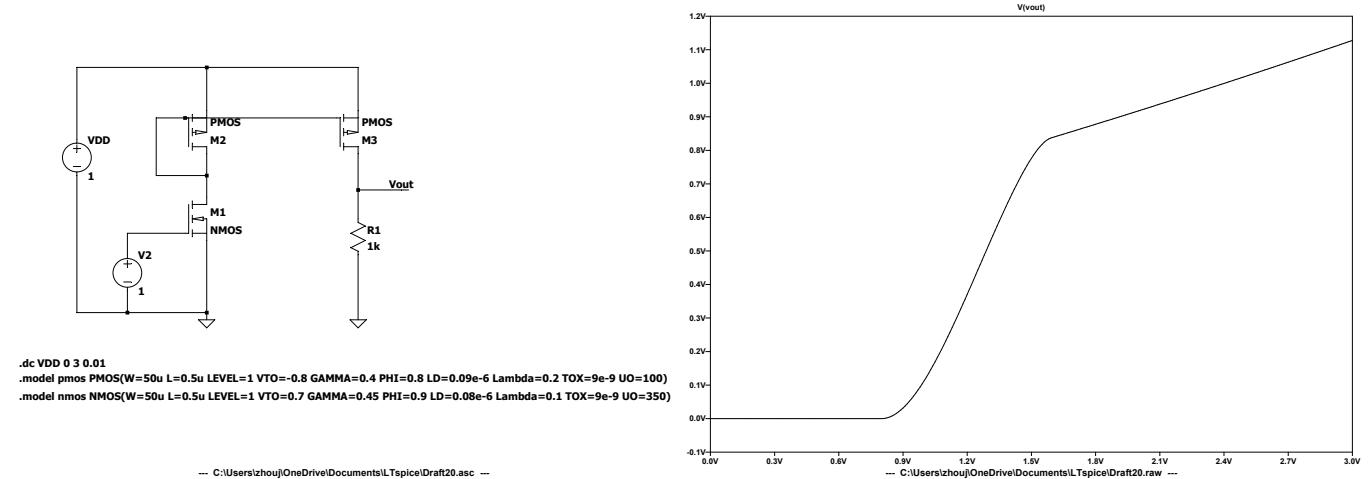


Figure 5.11



5.5

Consider the circuit of Fig.5.12(a), assuming $(W/L)_{1-3} = 40/0.5$, $I_{REF} = 0.3mA$, and $\gamma = 0$.

- (a) Determine V_b such that $V_X = V_Y$.
- (b) If V_b deviates from the value calculated in part (a) by 100mV, what is the mismatch between I_{out} and I_{REF} ?
- (c) If the circuit fed by the cascode current source changes V_p by 1V, how much does V_Y change?

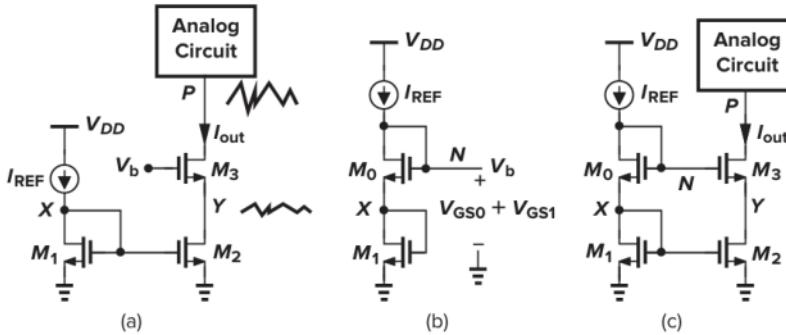


Figure 5.12 (a) Cascode current source, (b) modification of mirror circuit to generate the cascode bias voltage, and (c) cascode current mirror.

$$(a) V_{GS,3} - V_{th} = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} (W/L)_3}}$$

$$V_b = V_x + V_{th,n} + \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} (W/L)_3}} = 2(V_{th,n} + \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} (W/L)_3}}) = 1.873V$$

$$(b) I_{REF} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{GS})$$

$$I_{out} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda (V_{GS} + \Delta V))$$

$$\frac{I_{out}}{I_{REF}} = \frac{1 + \lambda (V_x + \Delta V)}{1 + \lambda V_x} \quad \Delta I = \frac{\lambda \Delta V}{1 + \lambda V_x} I_{REF} = 0.01 I_{REF} = 0.0274mA$$

$$(c) \Delta V_Y = \frac{\Delta V_P}{g_m M_3 r_o} = \frac{1V}{84} = 0.012V$$

5.6

The circuit of Fig.5.18(b) is designed with $(W/L)_{1,2} = 20/0.5$, $(W/L)_{3,0} = 60/0.5$, and $I_{REF} = 100\mu A$.

(a) Determine V_X and the acceptable range of V_b .

(b) Estimate the deviation of I_{out} from $300\mu A$ if the drain voltage of M_3 is higher than V_X by 1V.

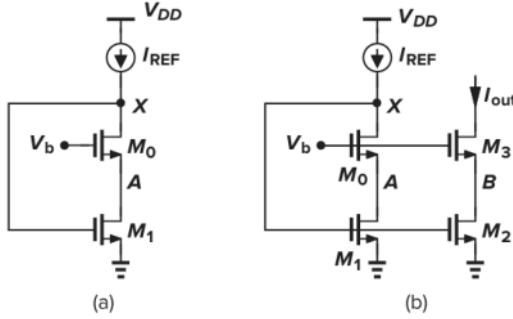


Figure 5.18 Modification of cascode mirror for low-voltage operation.

$$(a) I_{REF} = 100\mu A, V_{GS} - V_{th} = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox} (W/L)_1}} = 0.193V$$

$$V_X = 0.893V$$

$$V_b = V_a + 0.893V \geq 1.086V$$

$$V_b = 0.893V + V_a < 1.593V$$

$$(b) g_{m3} = \sqrt{2\mu_n C_{ox} (W/L)_3 I_{out}} = 3.106mS$$

$$r_{o3} = \frac{1}{\lambda I} = 33.3k\Omega$$

$$\Delta V_b = \frac{\Delta V}{g_{m3} r_{o3}} = 9.66mV$$

$$I_{out} - 3I_{REF} = 0.29\mu A$$

5.7

The circuit of Fig.5.23(a) us designed with $(W/L)_{1-4} = 50/0.5$ and $I_{SS} = 2I_1 = 0.5mA$.

(a) Calculate the small-signal voltage gain.

(b) Determine the maximum output voltage swing if the input CM level is 1.3V.

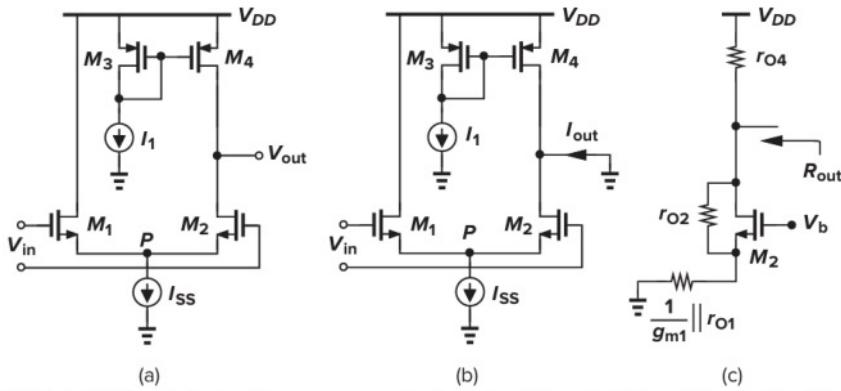


Figure 5.23 (a) Differential pair with current-source load; (b) circuit for calculation of G_m ; (c) circuit for calculation of R_{out} .

$$(a) A_v = \frac{1}{2} g_{m1} [2r_{o2} || r_{o4}]$$

$$g_{m1} = \sqrt{2\mu_n C_{ox} (W/L)_1 \frac{1}{2} I_{SS}} = 2.588mS$$

$$r_{o2} = \frac{1}{\lambda I} = 40k\Omega$$

$$r_{o4} = 20k\Omega$$

$$A_v = 20.7$$

$$(b) V_{out,min} \geq V_{in,CM} - V_{th} = 0.6V$$

$$V_{out,min} \leq V_{DD} - V_{od4} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{ox} (W/L)}} = 2.639V$$

5.8

Consider the circuit of Fig.5.29(a) with $(W/L)_{1-5} = 50/0.5$ and $I_{D5} = 0.5mA$.

- Calculate the deviation of V_{out} from V_F if $|V_{TH3}|$ is 1mV less than $|V_{TH4}|$.
- Determine the CMRR of the amplifier.

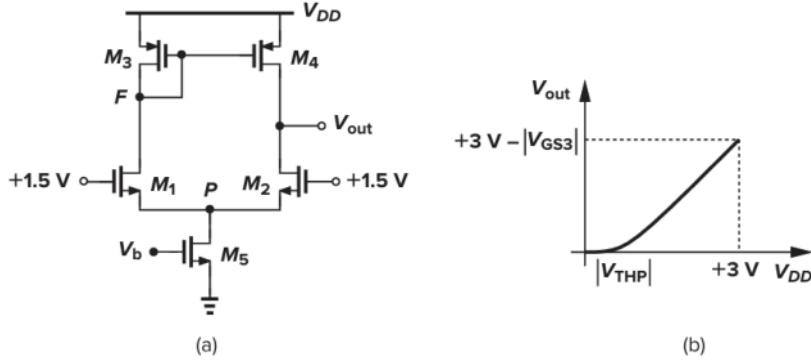


Figure 5.29

$$(a) I_1 = I_2 = I_3 = I_4 = \frac{1}{2}I_{SS}$$

$$I_3 = \frac{1}{2}\mu_p C_{ox} (W/L)_3 (V_{GS3} - V_{th})^2 (1 + \lambda V_{DS3})$$

$$I_4 = \frac{1}{2}\mu_p C_{ox} (W/L)_3 (V_{GS3} - V_{th} - \Delta V)^2 (1 + \lambda(V_{DS3} + \Delta V_x))$$

$$\Delta V_x = g_m r_o (1 + \lambda V_{GS}) \Delta V$$

$$(b) CMRR = g_{m1} r_{o2} || r_{o4} \frac{g_{m3}(1+2g_{m1}R_{SS})}{g_{m1}} = (1 + 2g_{m1}R_{SS})g_{m3}(r_{o1}||r_{o3})$$

5.9

Sketch V_X and V_Y as a function of V_{DD} for each circuit in Fig.5.52. Assume the transistors in each circuit are identical.

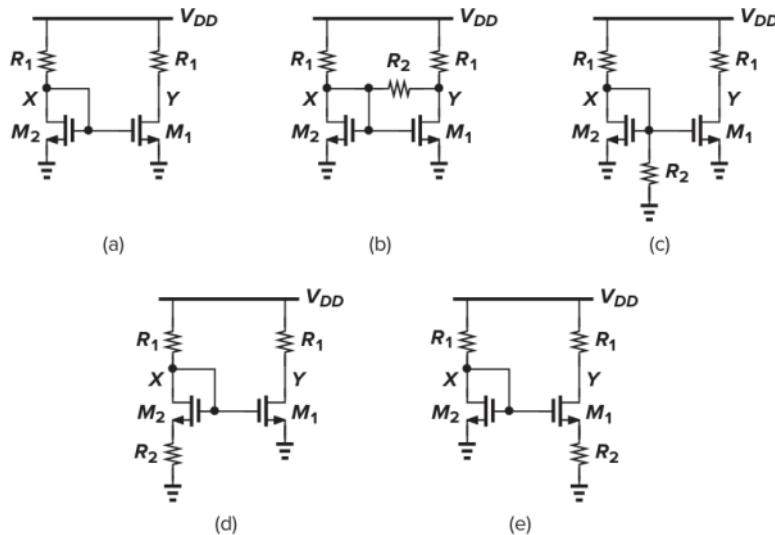
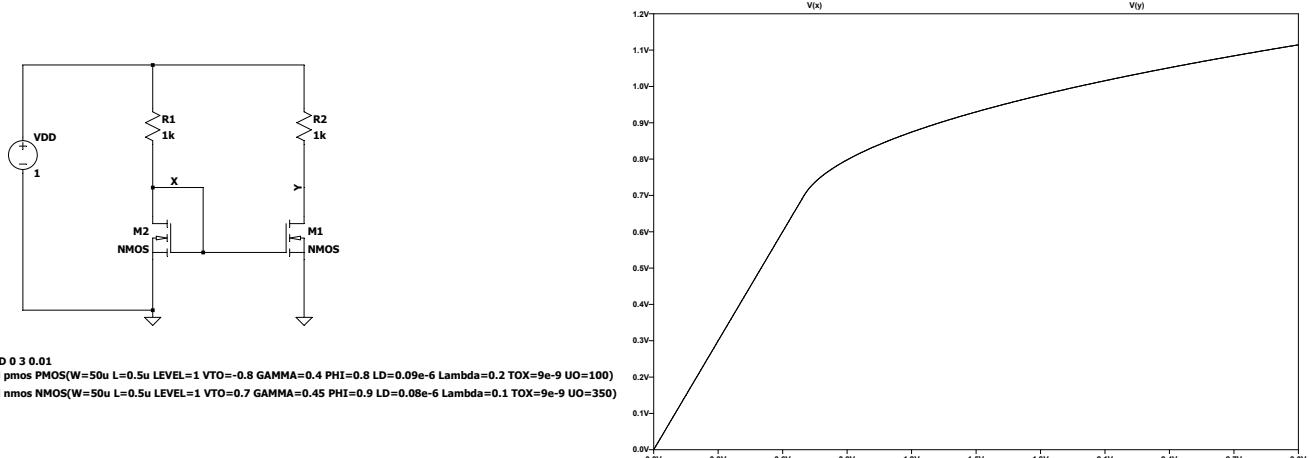
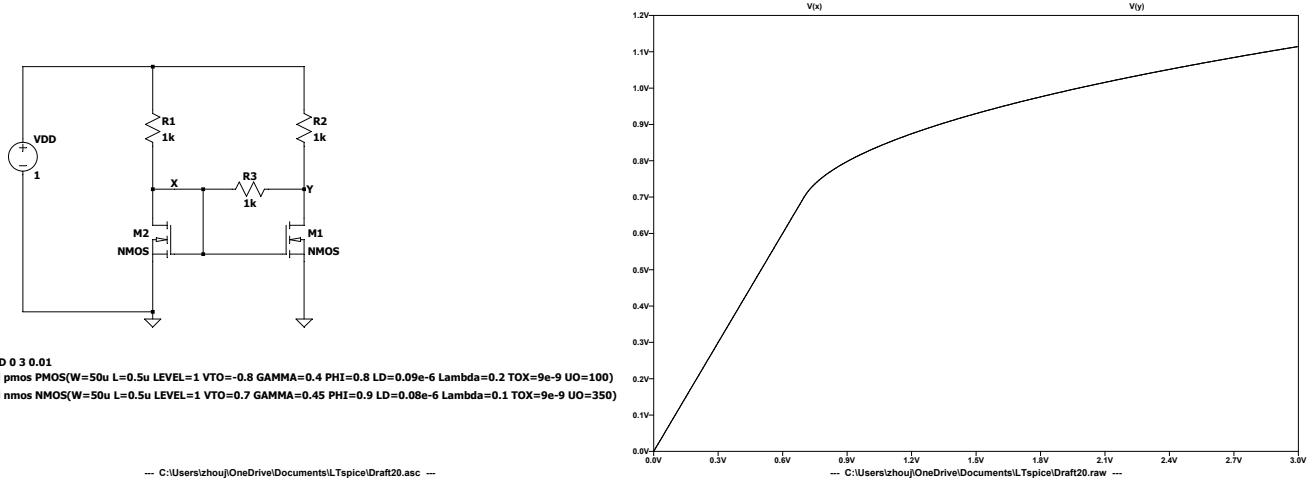


Figure 5.52

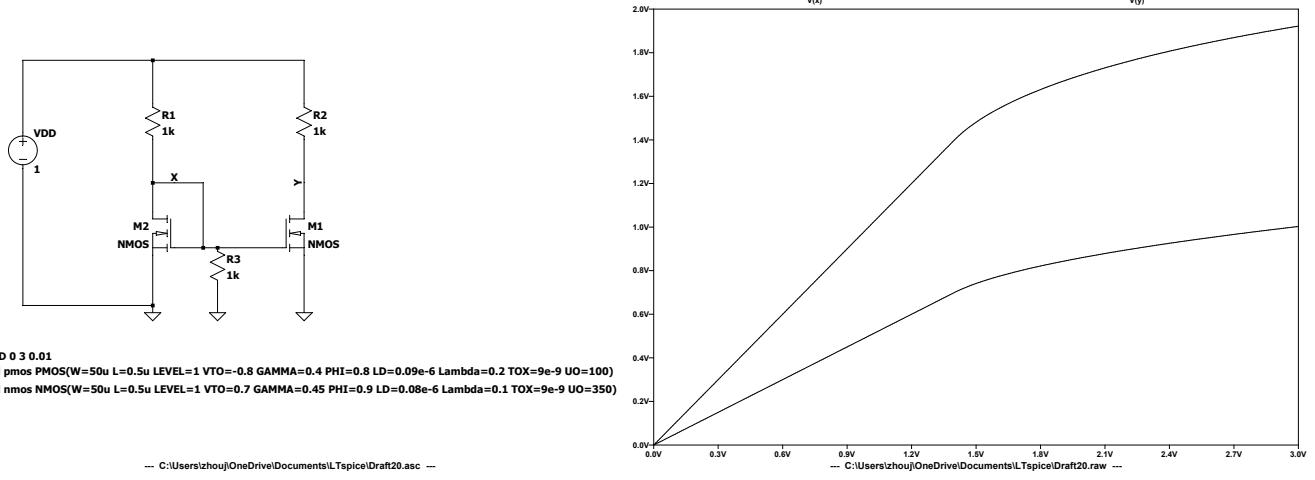
(a)



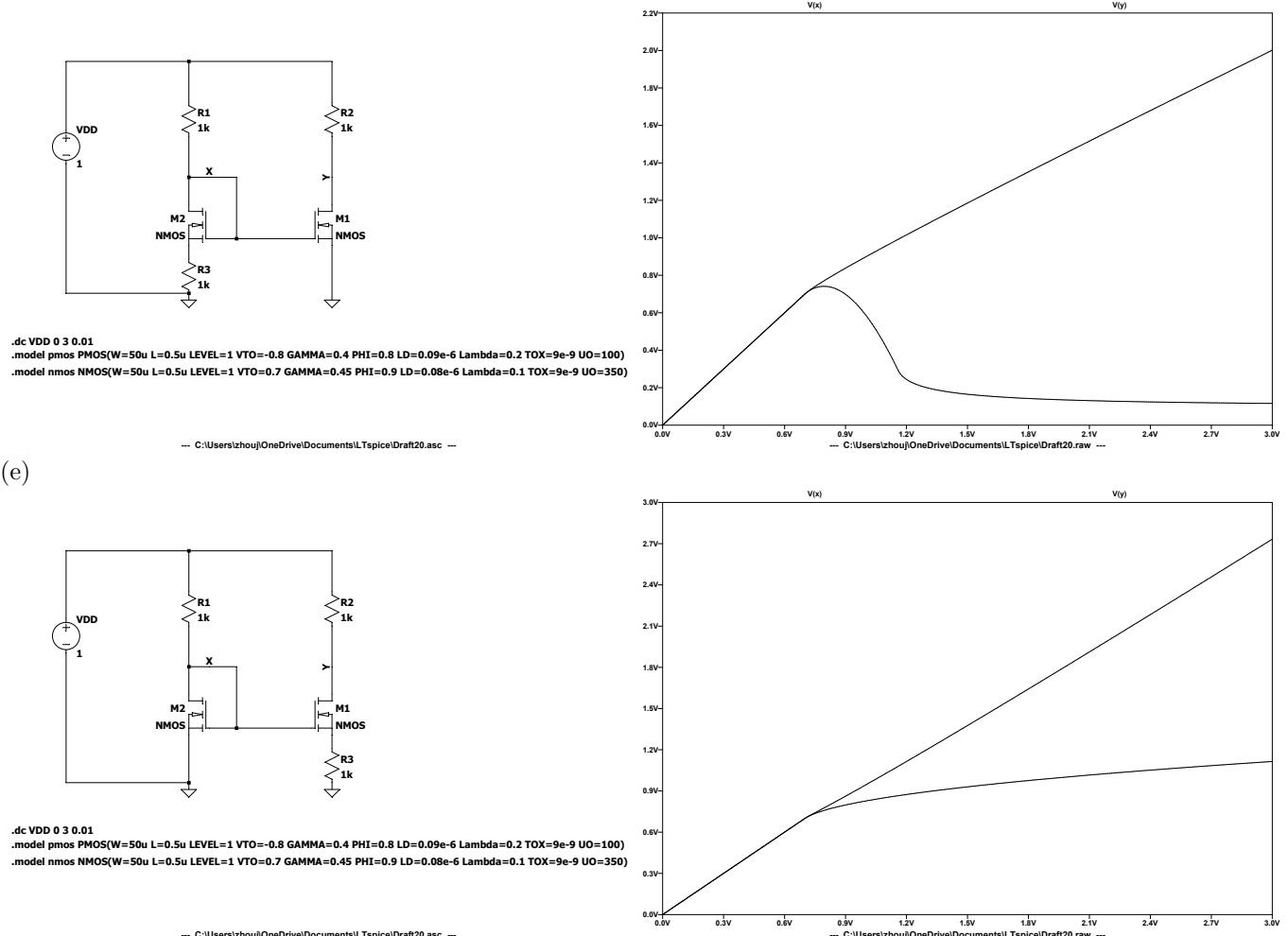
(b)



(c)



(d)



5.10

Sketch V_X and V_Y as a function of V_{DD} for each circuit in Fig.5.53. Assume the transistors in each circuit are identical.

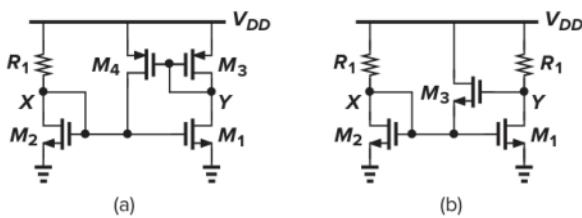
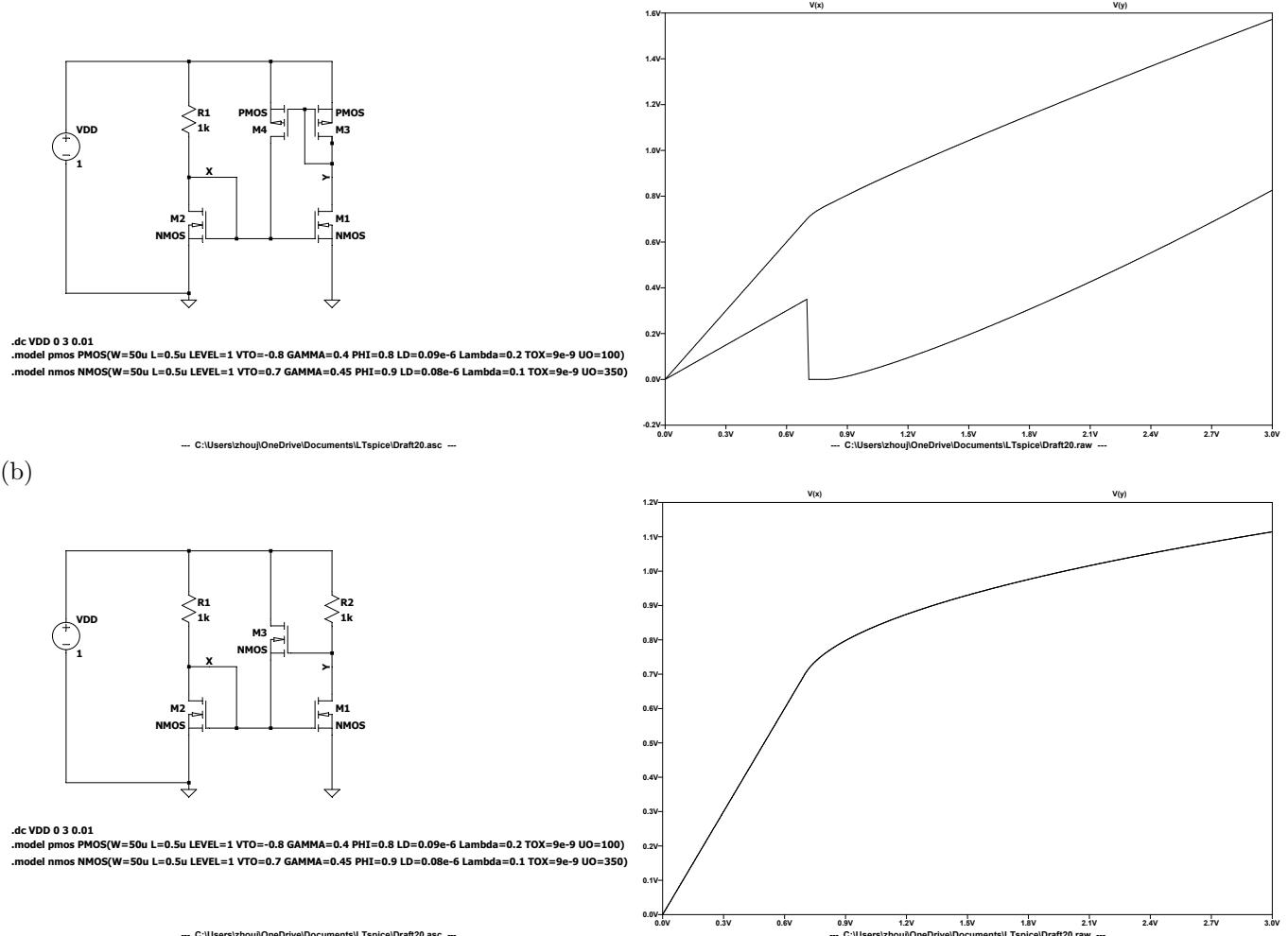


Figure 5.53

(a)



5.11

For each circuit in Fig.5.54, sketch V_X and V_Y as a function of V_1 for $0 < V_1 < V_{DD}$. Assume the transistors in each circuit are identical.

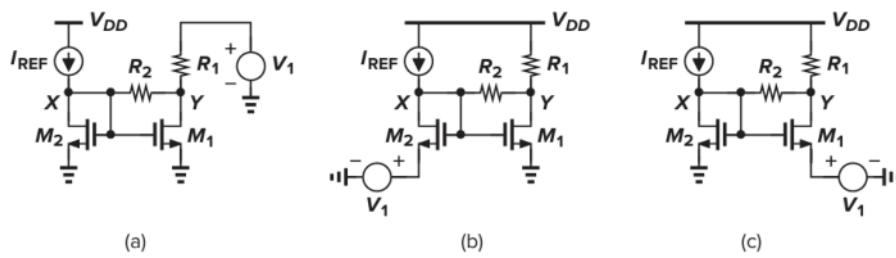
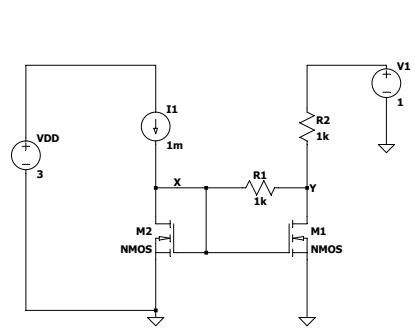
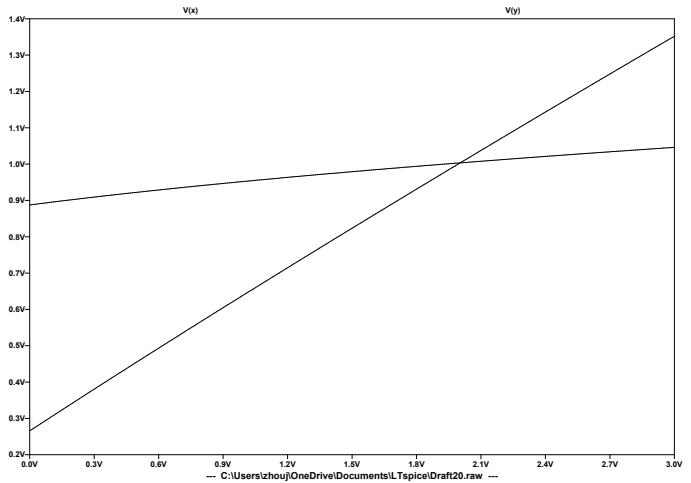


Figure 5.54

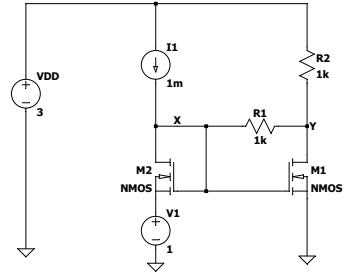
(a)



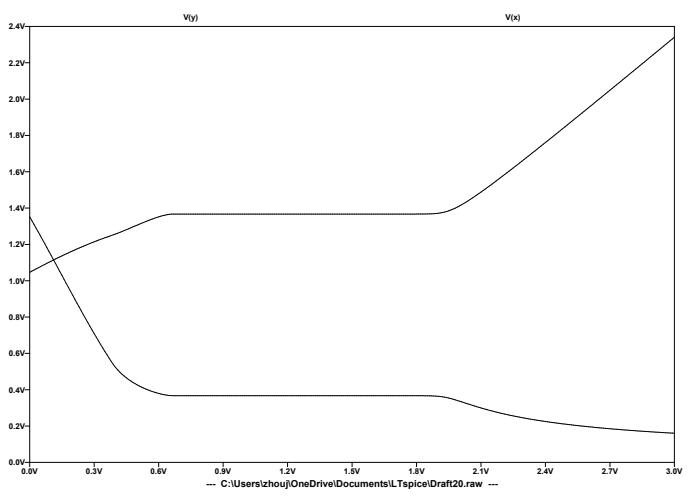
```
.dc V1 0 3 0.01
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



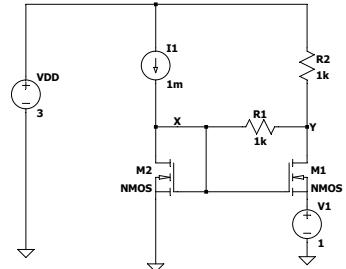
(b)



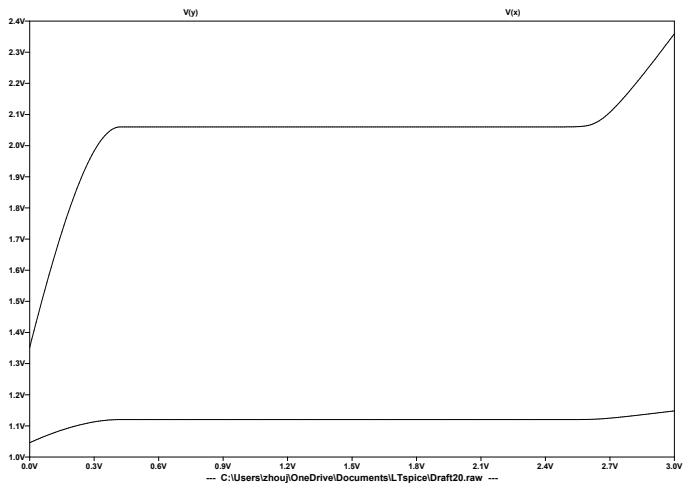
```
.dc V1 0 3 0.01
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



(c)



```
.dc V1 0 3 0.01
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



5.12

For each circuit in Fig.5.55, sketch V_X and V_Y as a function of V_1 for $0 < V_1 < V_{DD}$. Assume the transistors in each circuit are identical.

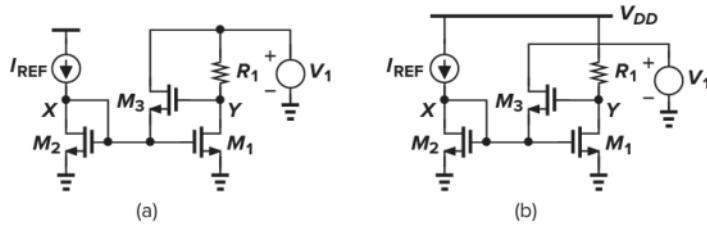
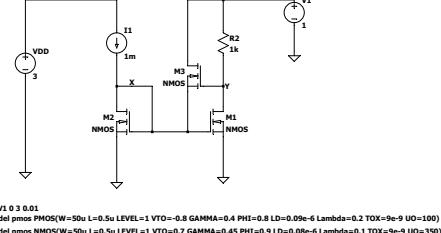
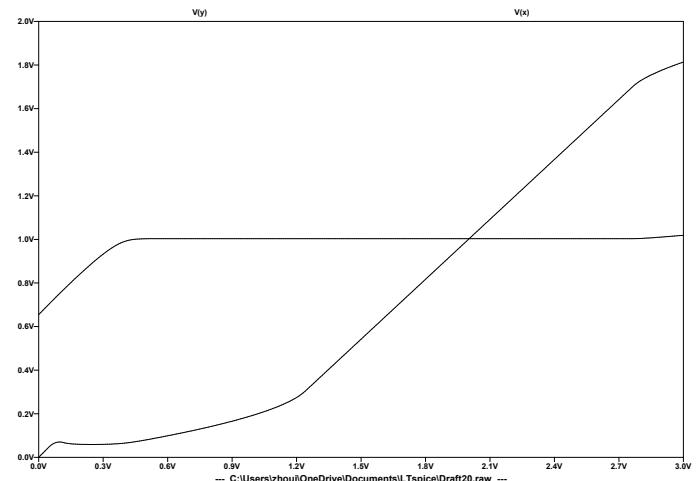


Figure 5.55

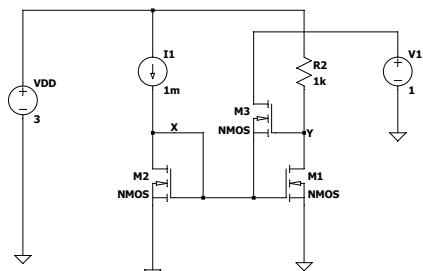
(a)



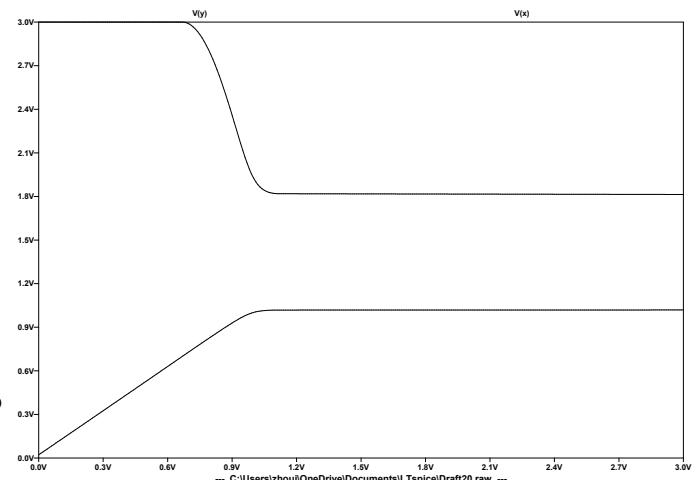
```
.dc V1 0 3 0.01
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



(b)



```
.dc V1 0 3 0.01
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



5.13

For each circuit in Fig.5.56, sketch V_X and V_Y as a function of I_{REF} .

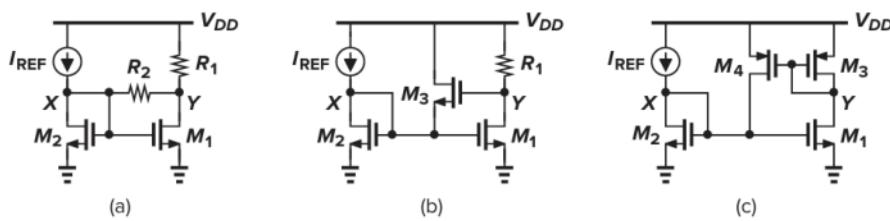
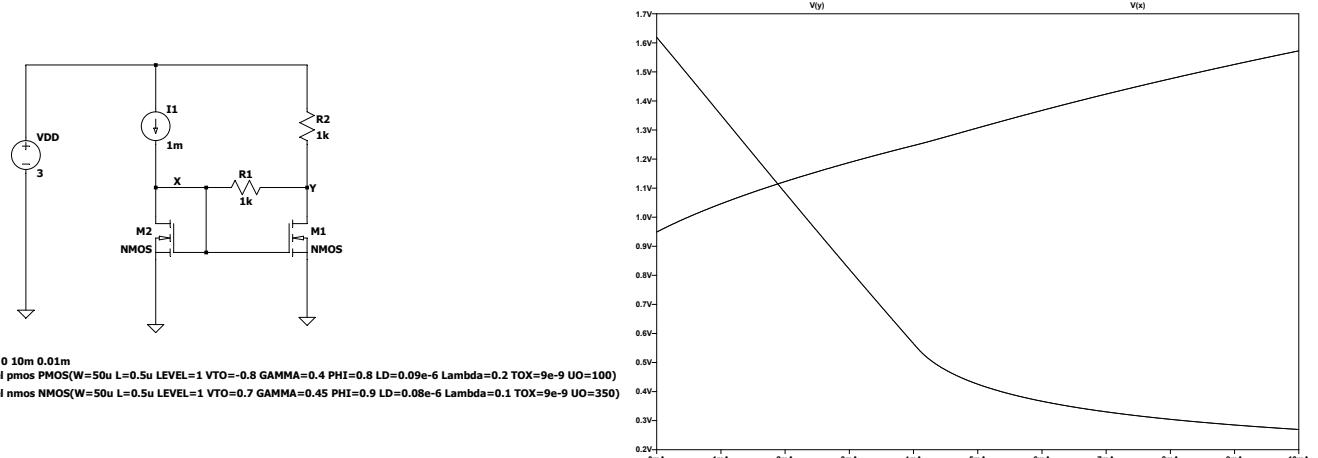
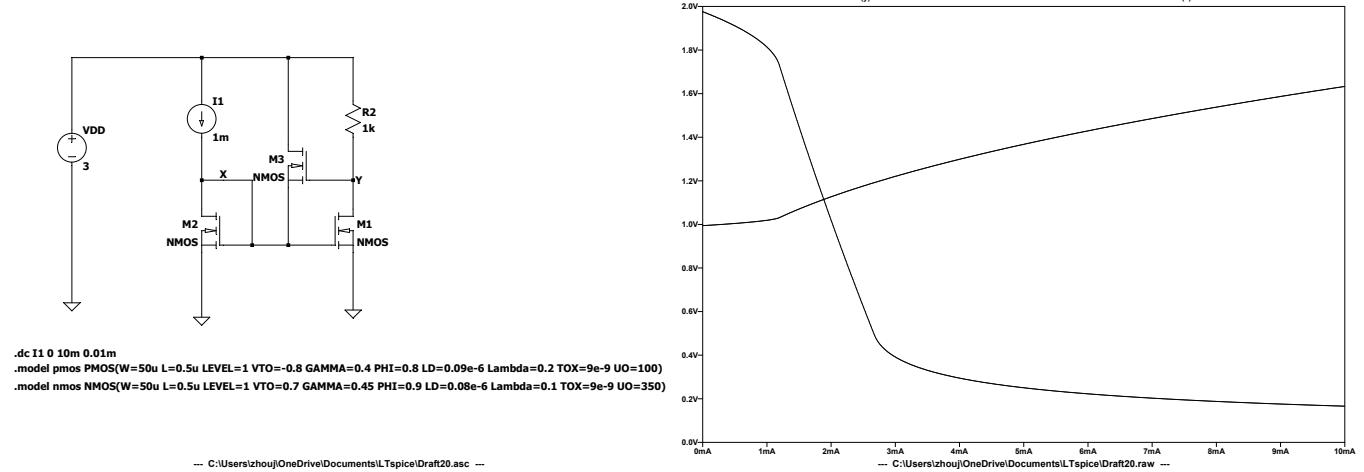


Figure 5.56

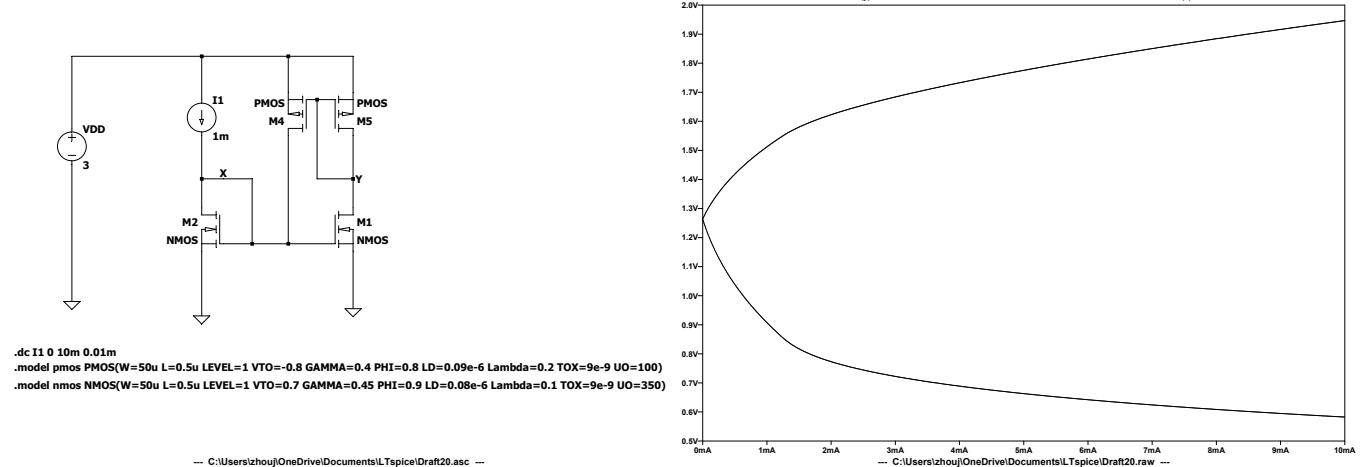
(a)



(b)



(c)



5.14

For each circuit of Fig.5.57, sketch I_{out} , V_X , V_A , and V_B as a function of (a) I_{REF} , (b) V_b .

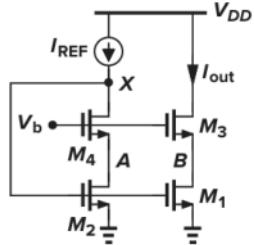
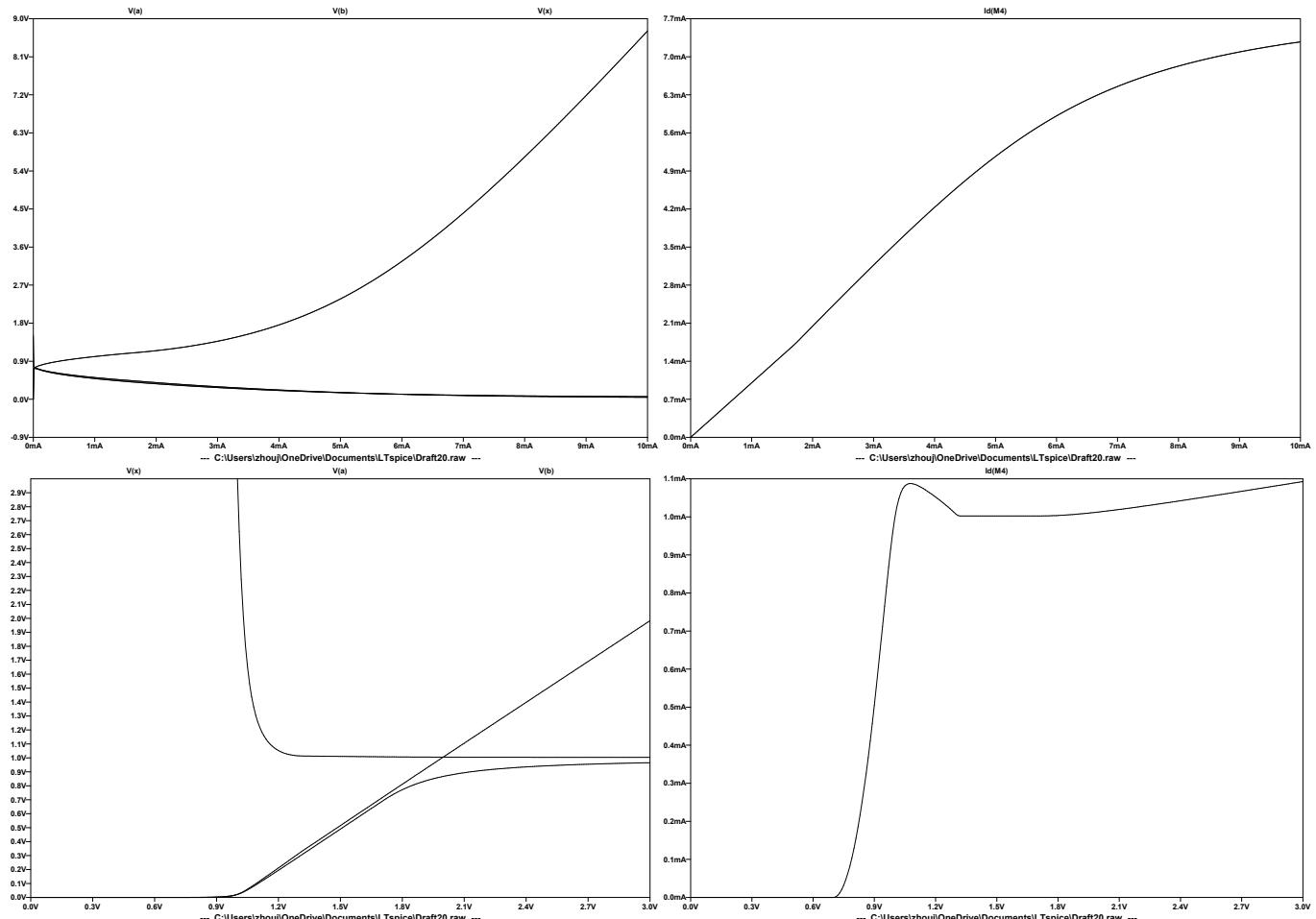
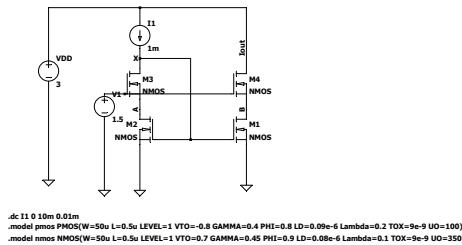


Figure 5.57



5.15

In the circuit shown in Fig.5.58, a source follower using a wide transistor and a small bias current is inserted in series with the gate of M_3 so as to bias M_2 at the edge of saturation. Assuming $M_0 - M_3$ are identical and $\lambda \neq 0$, estimate the mismatch between I_{out} and I_{REF} if (a) $\gamma = 0$, $\gamma \neq 0$.

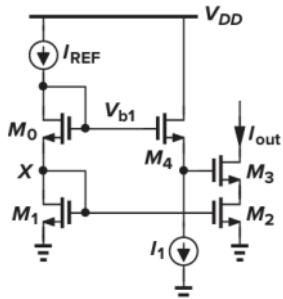


Figure 5.58

- (a) $I_{REF} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$
 $\Delta I/I_{ref} = \lambda \Delta V_{ds} = \lambda V_{th}$
(b) As $\gamma \neq 0$, mismatch increases as V_{th} increases.

5.16

Sketch V_X and V_Y as a function of time for each circuit in Fig.5.59. Assume the transistors in each circuit are identical.

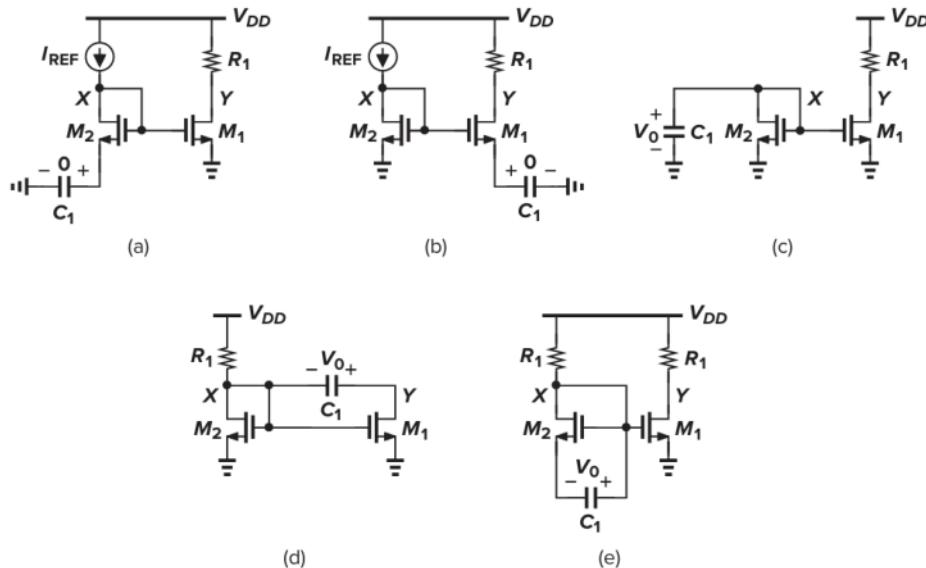
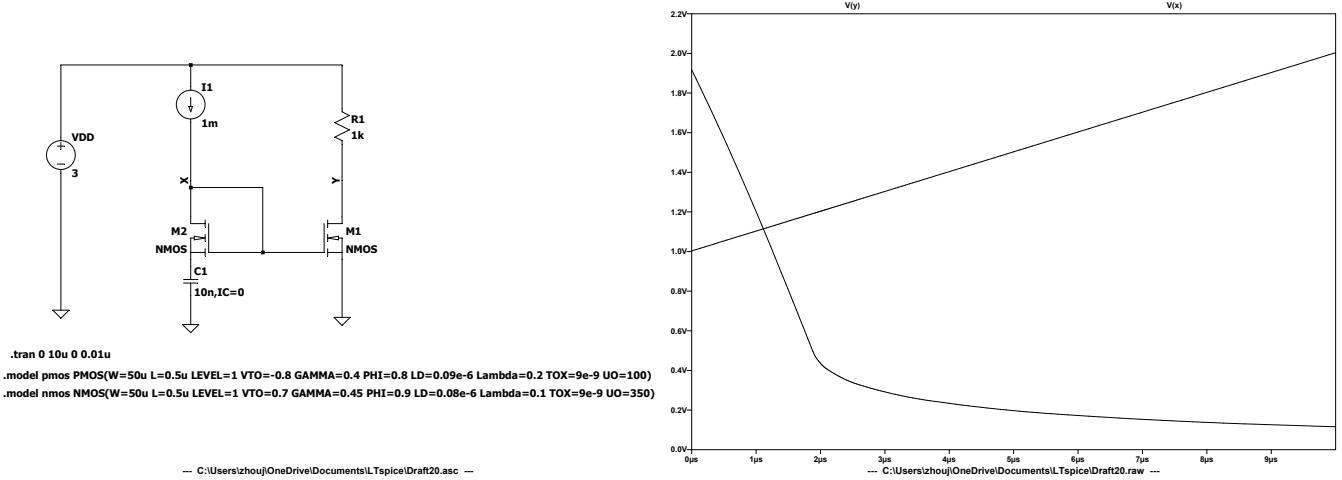
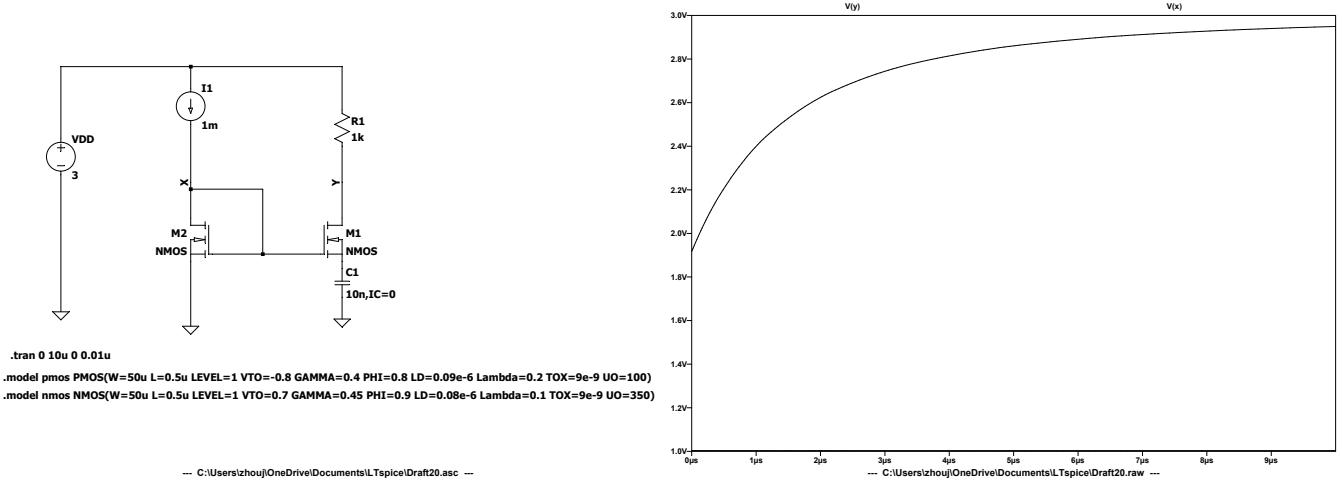


Figure 5.59

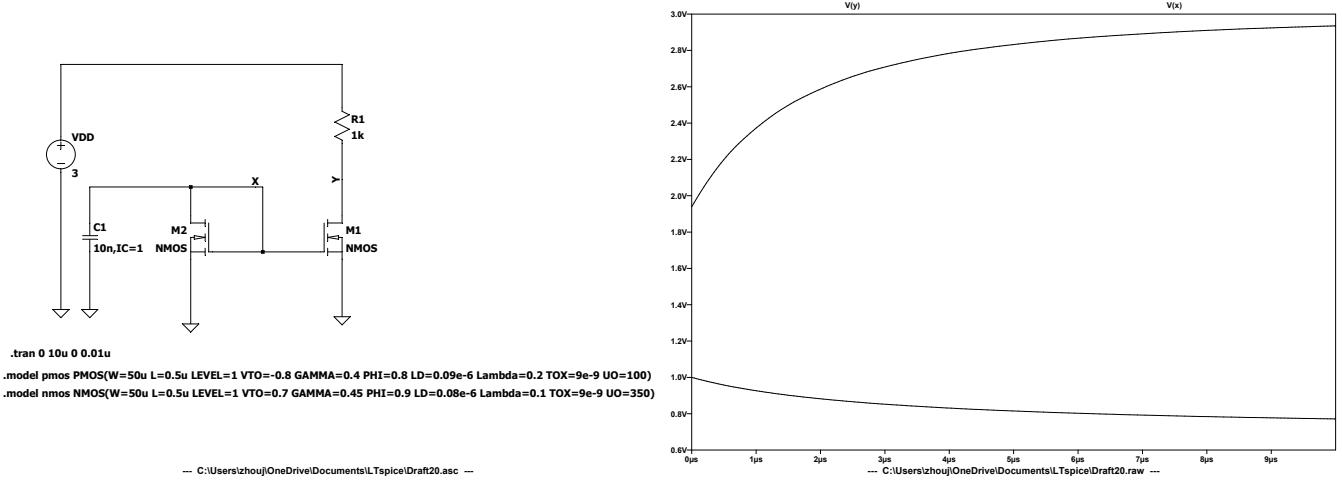
(a)



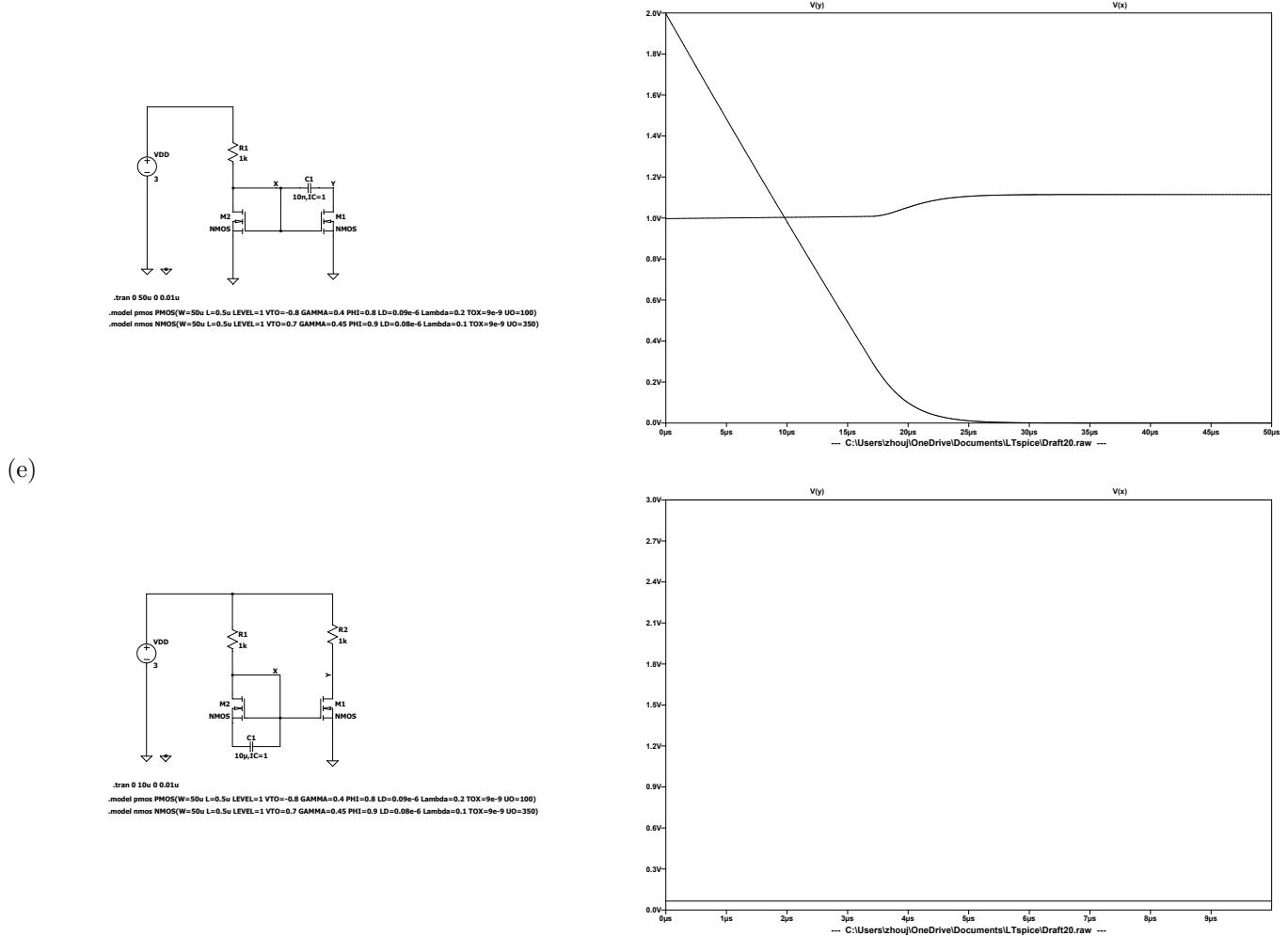
(b)



(c)



(d)



5.17

Sketch V_X and V_Y as a function of time for each circuit in Fig.5.60. Assume the transistors in each circuit are identical.

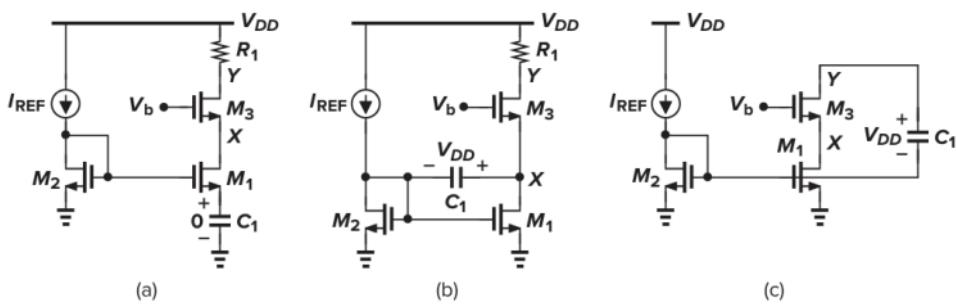
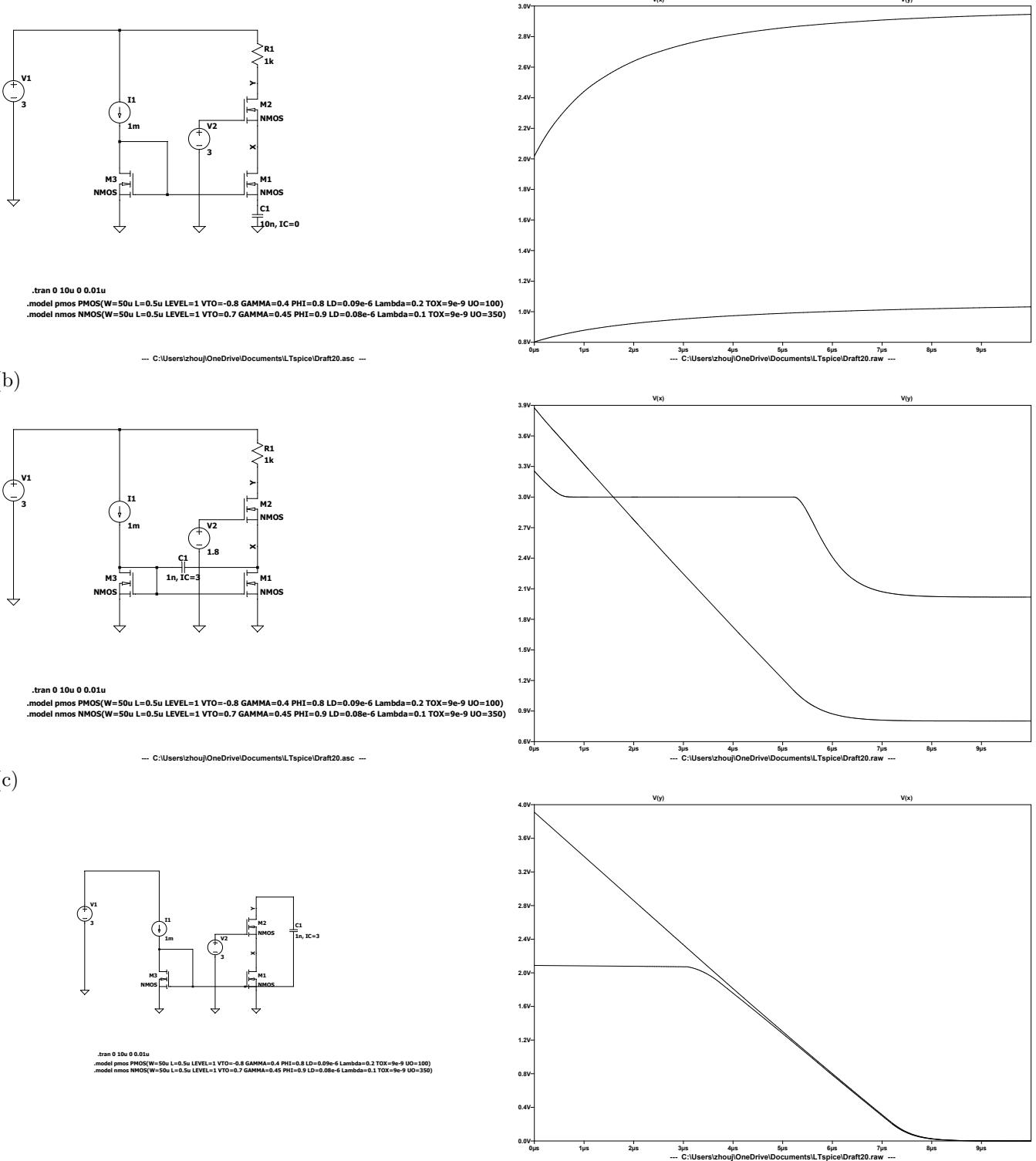


Figure 5.60

(a)



5.18

Sketch V_X and V_Y as a function of time for each circuit in Fig.5.61. Assume the transistors in each circuit are identical.

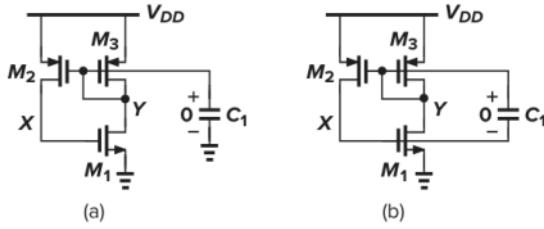
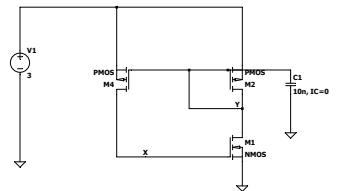
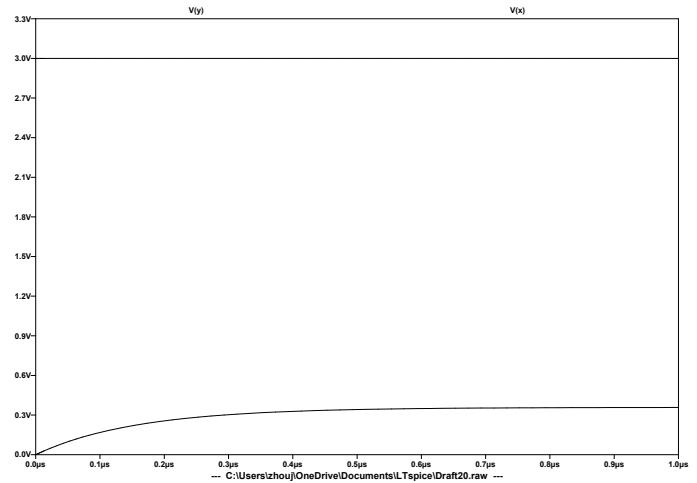


Figure 5.61

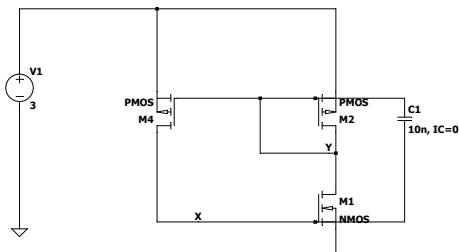
(a)



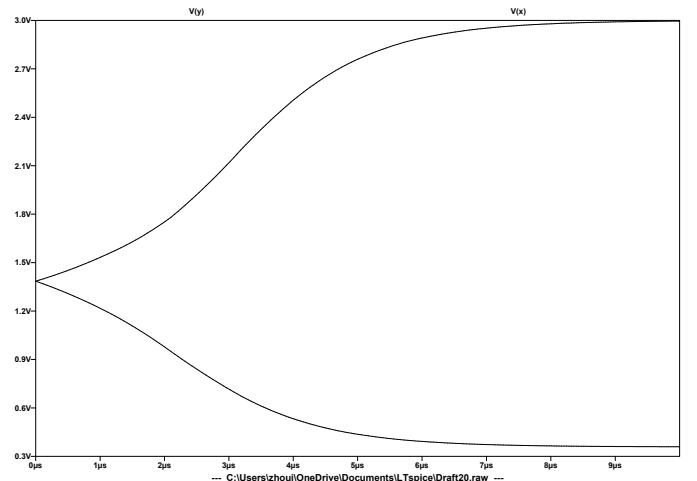
```
.tran 0 1u 0.01u
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



(b)



```
.tran 0 10u 0.01u
.model pmos PMOS(W=50u L=0.5u LEVEL=1 VTO=-0.8 GAMMA=0.4 PHI=0.8 LD=0.09e-6 Lambda=0.2 TOX=9e-9 UO=100)
.model nmos NMOS(W=50u L=0.5u LEVEL=1 VTO=0.7 GAMMA=0.45 PHI=0.9 LD=0.08e-6 Lambda=0.1 TOX=9e-9 UO=350)
```



5.19

The circuit shown in Fig.5.62 exhibits a negative input inductance. Calculate the input impedance of the circuit and identify the inductive component.

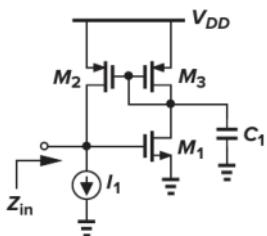


Figure 5.62

Use small-signal diagram, we can find $I_{in} = g_{m2}V_1$ and $g_{m1}V_{in} + g_{m3}V_1 + \frac{V_1}{1/sC_1} = 0$

$$\frac{V_{in}}{I_{in}} = -\frac{g_{m3} + sC_1}{g_{m2}g_{m1}}$$

5.20

Due to a manufacturing defect, a large parasitic resistance, R_1 , has appeared in the circuits of Fig.5.63. Calculate the gain of each circuit if $\lambda > 0$.

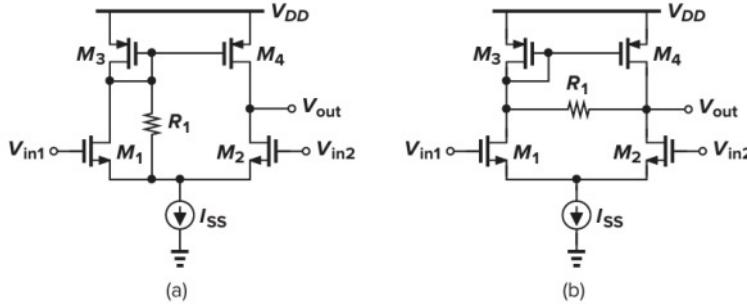


Figure 5.63

- (a) $A_v = -g_{m2}(r_{o2}||r_{o4})$
- (b) $A_v = -g_{m2}(r_{o2}||r_{o4}||R_1)$

5.21

In digital circuits such as memories, a differential pair with an active current mirror is used to convert a small differential signal to a large single-ended swing (Fig.5.64). In such applications, it is desirable that the output levels be as close to the supply rails as possible. Assuming moderate differential input swings (e.g., $\Delta V = 0.1V$) around a common-mode level $V_{in,CM}$ and a high gain in the circuit, explain why V_{min} depends on $V_{in,CM}$.

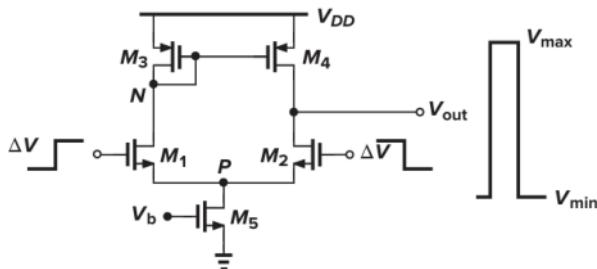


Figure 5.64

$$V_{out,min} = V_p + V_{Dsat,2} = V_{in,CM} - V_{gs2} + V_{Dsat,2}$$

5.22

Sketch V_X and V_Y for each circuit in Fig.5.65 as a function of time. The initial voltage across C_1 is shown.

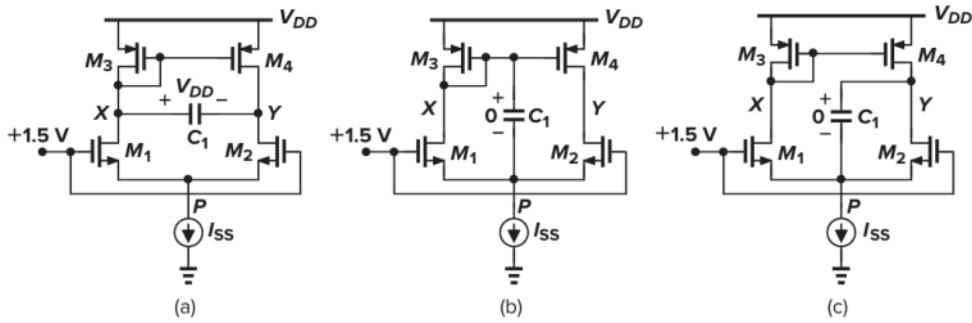
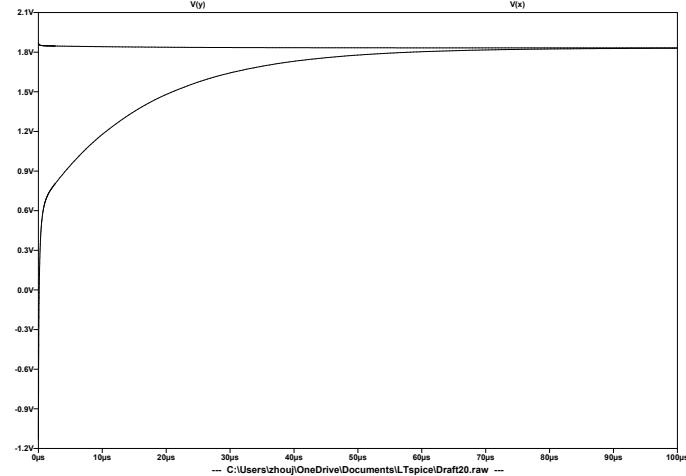
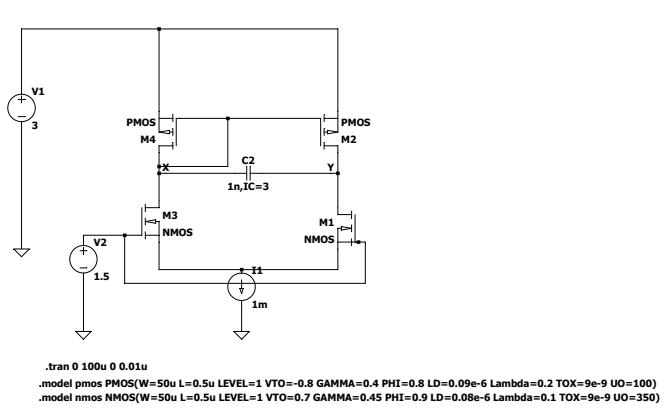
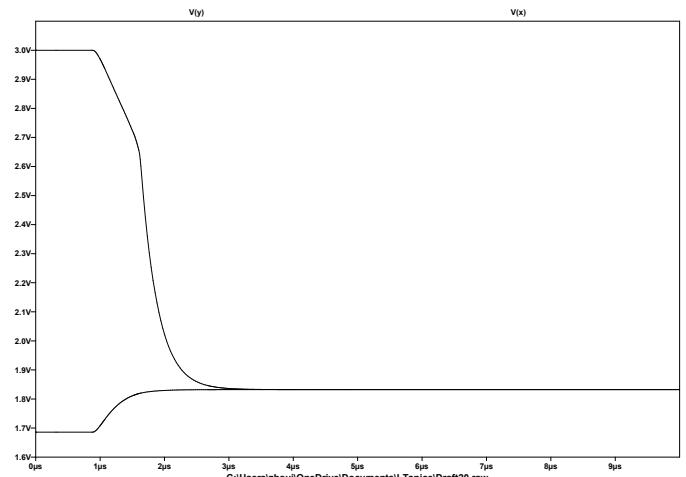
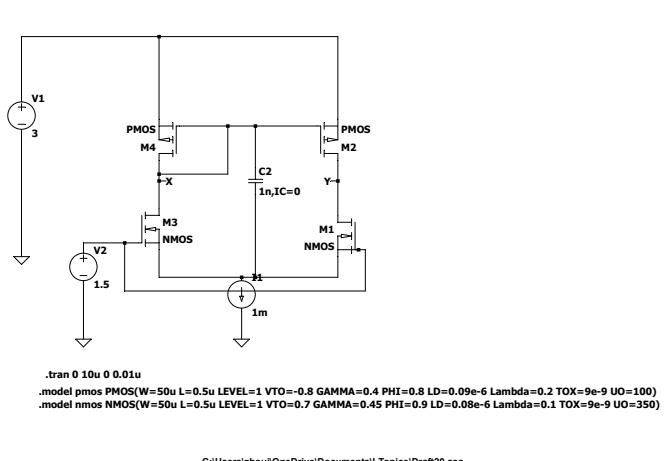


Figure 5.65

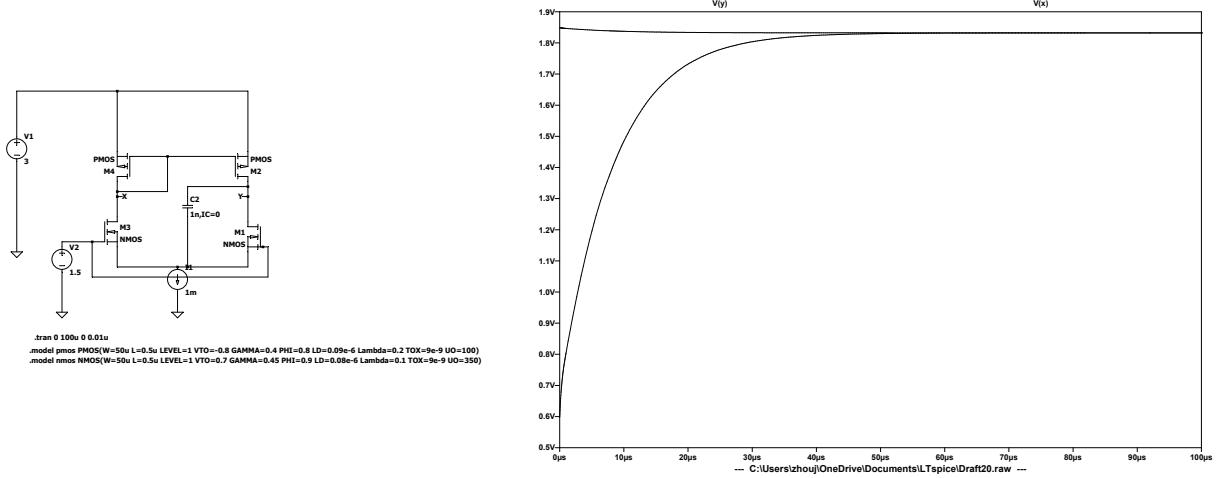
(a)



(b)



(c)



5.23

If in Fig.5.66, ΔV is small enough that all of the transistors remain in saturation, determine the time constant and the initial and final values of V_{out} .

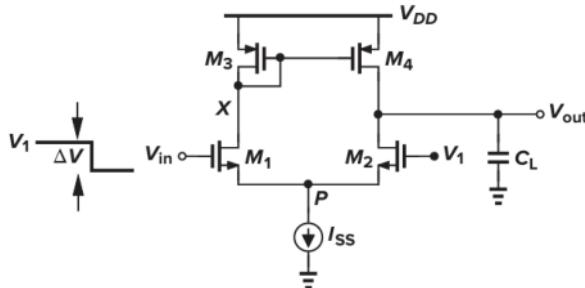


Figure 5.66

$$\text{Initial, } V_{out} = V_X = V_{DD} - V_{SG3}$$

$$\text{Final, } A_V = g_m(r_{o4}||r_{o2})$$

$$V_{out} = V_{DD} - V_{SG3} - A_v \Delta V$$

$$\tau = \frac{1}{2\pi(r_{o4}||r_{o2})C_L}$$

5.24

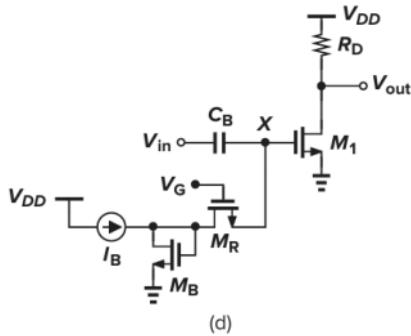
For a device operating in the subthreshold region, we have

$$I_D = \mu_n C_d \frac{W}{L} V_T^2 (\exp \frac{V_{GS} - V_{TH}}{V_T}) (1 - \exp \frac{-V_{DS}}{V_T})$$

(a) If the device is in the deep triode region, $V_{DS} \ll V_T$. Using $\exp(-\epsilon) \approx 1 - \epsilon$, determine the on-resistance.

(b) If the device is in saturation, $V_{DS} >> V_T$. Compute the transconductance.

(c) Find the relation between $g_{m,B}$ and $R_{on,R}$ in Fig.5.43(d) using the above results.



$$(a) I_D = \mu_n C_d \frac{W}{L} V_T^2 (\exp \frac{V_{GS} - V_{TH}}{V_T}) \frac{V_{DS}}{V_T} = \mu_n C_d \frac{W}{L} V_{DS} V_T (\exp \frac{V_{GS} - V_{TH}}{V_T})$$

$$R_{on} = \frac{1}{\delta I_D} = \frac{1}{\mu_n C_d \frac{W}{L} V_T (\exp \frac{V_{GS} - V_{TH}}{V_T})}$$

$$(b) (c) g_{m,B} = \mu_n C_d \left(\frac{W}{L}\right)_B V_T e^{\frac{V_X - V_{th}}{V_T}}$$

$$R_{on} = \frac{1}{\mu_n C_d \left(\frac{W}{L}\right)_R V_T e^{\frac{V_G - V_X - V_{th}}{V_T}}} g_{m,B} R_{on} = \frac{\left(\frac{W}{L}\right)_B}{\left(\frac{W}{L}\right)_R}$$

5.25

Determine the corner frequency resulting from C_{in} in Fig.5.47(d). For simplicity, assume C_1 is a short circuit.

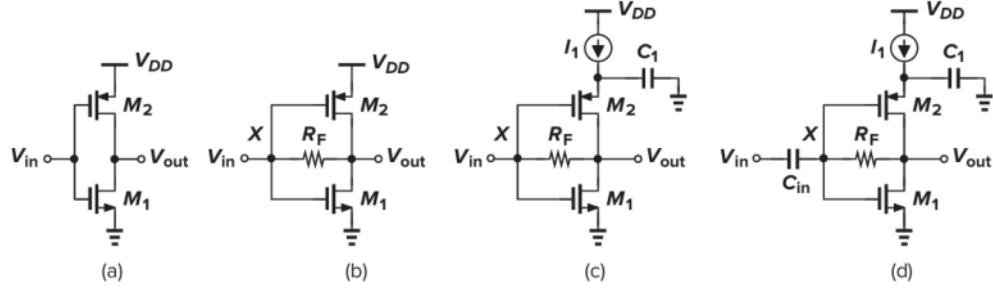


Figure 5.47 (a) Complementary CS stage, (b) self-biased topology, (c) accurate definition of bias current, and (d) use of ac coupling at input.

$$\omega = \frac{1}{C_{in} \frac{R_F}{A_V}}$$

5.26

Determine the supply rejection of the circuit shown in Fig.5.67.

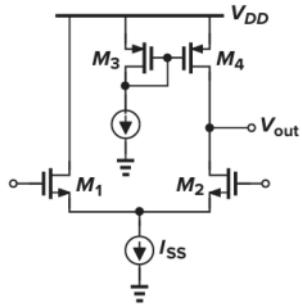


Figure 5.67

$$PSRR = \frac{A_v}{A_{VDD-OUT}} = \frac{0.5g_{m2}(r_{o2}||r_{o4})}{\frac{1}{r_{o4}+r_{o2}}} = 0.5g_{m2}(r_{o2}||r_{o4})(r_{o2} + r_{o4})$$

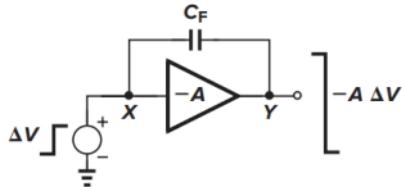
6 Frequency Response of Amplifiers

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

6.1

In the circuit of Fig.6.3(c), suppose the amplifier has a finite output resistance R_{out} .

- (a) Explain why the output jumps up by ΔV before it begins to go down. This indicates the existence of a zero in the transfer function.
- (b) Determine the transfer function and the step response without using Miller's theorem.



(c)

(a) The reason of output jumps up by ΔV before it begins to go down is the voltage change between the ideal capacitor cannot be sudden.

$$(b) \frac{\frac{V_o(s)-V_{in}(s)}{\frac{1}{sC_F}} + \frac{V_o(s)-AV_{in}(s)}{R_{out}}}{0}$$

$$H(s) = \frac{sC_F - \frac{A}{R_{out}}}{\frac{1}{R_{out}} + sC_F}$$

Suppose for step response $V_{in} = \frac{a}{s}$

$$V_o(s) = V_{in}(s)H(s) = \frac{a}{s} \frac{sC_F - \frac{A}{R_{out}}}{\frac{1}{R_{out}} + sC_F}$$

$$V_o(t) = a[(A+1)e^{-\frac{t}{C_F R_{out}}} - Au(t)]$$

When $t = 0, V_o(t) = a$

When $t = \infty, V_o(t) = -aA$

6.2

Repeat Problem 6.1 if the amplifier has an output resistance R_{out} and the circuit drives a load capacitance C_L .

$$(a) \Delta V_o = \frac{C_F}{C_F + C_L}$$

$$(b) \frac{\frac{V_o(s)-V_{in}(s)}{\frac{1}{sC_F}} + \frac{V_o(s)-AV_{in}(s)}{R_{out}} + \frac{V_o(s)}{\frac{1}{sC_L}}}{0} = 0$$

$$H(s) = \frac{sC_F - \frac{A}{R_{out}}}{\frac{1}{R_{out}} + sC_F + sC_L}$$

$$V_o(t) = a[(A + \frac{C_F}{C_F + C_L})e^{-\frac{t}{(C_F + C_L)R_{out}}} - Au(t)]$$

6.3

The CS stage of Fig.6.13 is designed with $(W/L)_1 = 50/0.5, R_S = 1k\Omega$, and $R_D = 2k\Omega$. If $I_D = 1mA$, determine the poles and zero of the circuit.

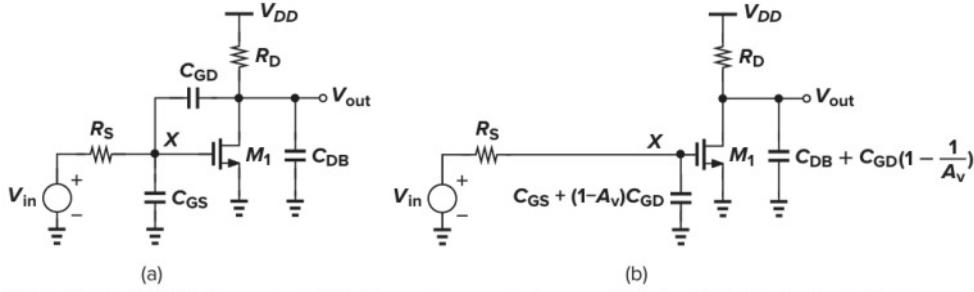


Figure 6.13 (a) High-frequency model of a common-source stage, and (b) simplified circuit using Miller's approximation.

$$V_{DS} = V_{DD} - I_D R_D = 1V$$

$$C_{gs} = \frac{2}{3} WLC_{ox} + WC_{ov} = 83.8fF$$

$$C_{gd} = WC_{ov} = 20fF$$

$$g_m = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_1 I_D (1 + \lambda V_{ds})} = 5.43mS$$

$$r_{o1} = \frac{1 + \lambda V_{DS}}{\lambda I_D} = 11k\Omega$$

$$r_{o1} || R_D = 1.64k\Omega$$

$$A_v = G_m R_{out} = -g_m (r_o || R_D) = -9.18$$

$$w_z = \frac{g_m}{C_{gd}} = 0.272 \times 10^{12}$$

$$w_{p1} = \frac{1}{R_s [(1 - A_v)C_{gd}] + C_{gs}} = 3.48 \times 10^9$$

$$w_{p2} = \frac{1}{(r_o || R_D)(1 - \frac{1}{A_v})C_{gd}} = 26.7 \times 10^9$$

6.4

Consider the CS stage of Fig.6.16, where \$I_1\$ is realized by a PMOS device operating in saturation. Assume that \$(W/L)_1 = 50/0.5\$, \$I_D = 1mA\$, and \$R_S = 1k\Omega\$.

(a) Determine the aspect ratio of the PMOS transistor such that the maximum allowable output level is 2.6V. What is the maximum peak-to-peak swing?

(b) Ddetermine the poles and zeros.

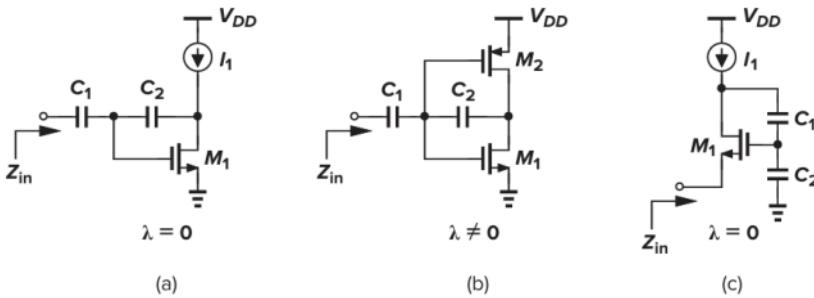


Figure 6.58

$$(a) V_{od,p} = V_{DD} - 2.6 = 0.4V$$

$$I_{op} = \frac{1}{2} \mu_p C_{ox} (\frac{W}{L})_p V_{od,p}^2 = 1mA$$

$$(\frac{W}{L})_p = 326$$

$$I_{od} = \frac{1}{2} \mu_n C_{ox} (\frac{W}{L})_1 V_{od,n}^2 = 1mA$$

$$V_{od,n} = 0.386V$$

$$V_{pp,out} = V_{DD} - V_{od,p} - V_{od,n} = 2.214V$$

$$(b) w_z = \frac{g_m}{C_{gd}} = 0.272 \times 10^{12}$$

6.5

A source follower employing an NFET with \$W/L = 50/0.5\$ and a bias current of 1mA is driven by a source impedance of \$10k\Omega\$. Calculate the equivalent inductance seen at the output.

$$I_X = V_X \frac{\frac{1}{sC_{gs}}}{R_{in} + \frac{1}{sC_{gs}}} g_m$$

$$\frac{V_X}{I_X} = \frac{1 + sR_{in}C_{gs}}{g_m}$$

$$L_{eq} = \frac{R_{in}C_{gs}}{g_m} = 162nH$$

6.6

Neglecting other capacitance, calculate the input impedance of each circuit shown in Fig.6.58.

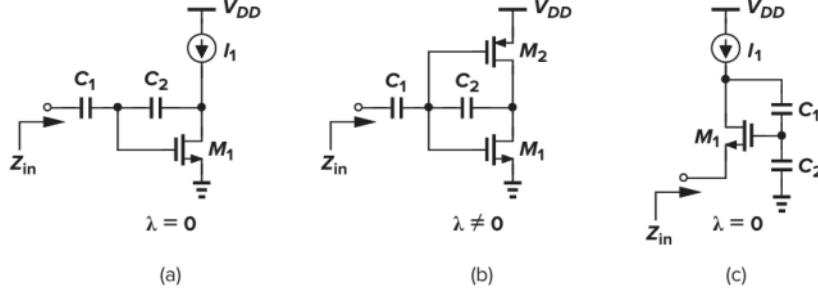


Figure 6.58

(a) Using small-signal diagram, $I_{in} = \frac{V_{in} - V_g}{\frac{1}{sC_1}} = g_m V_g$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1 + \frac{sC_1}{g_m}}{sC_1}$$

$$(b) I_{in} = \frac{V_{in} - V_g}{\frac{1}{sC_1}} = \frac{V_g - V_d}{\frac{1}{sC_2}} = (g_{m1} + g_{m2})V_g + \frac{V_d}{r_{o1}||r_{o2}}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1 + \frac{(g_{m1} + g_{m2})}{sC_1} + \frac{\frac{1}{sC_1} + \frac{1}{sC_2}}{r_{o1} || r_{o2}}}{g_{m1} + g_{m2} + \frac{1}{sC_1 || sC_2}}$$

$$(c) \quad I_{in} = -g_m(V_g - V_{in}) = \frac{V_g}{\frac{sC_1}{sC_2} + r_o}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1 + \frac{g_m}{sC_2}}{g_m}$$

6.7

Estimate the poles of each circuit in Fig.6.59.

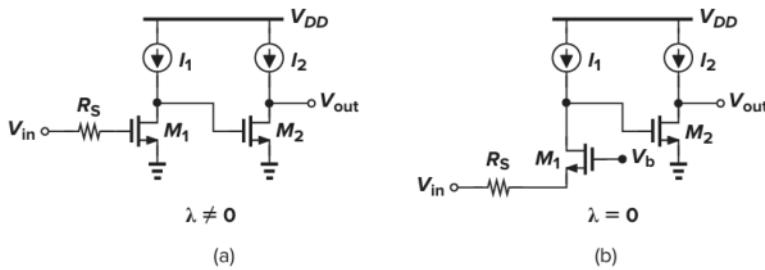


Figure 6.59

$$(a) w_1 = \frac{1}{R_s[C_{gs1} + C_{gd1}(1 + g_{m1}r_{o1})]}$$

$$w_2 = \frac{1}{r_{o1}[C_{db1} + C_{gd1} + C_{gs2} + C_{gd2}(1 + g_{m2}r_{o2})]}$$

$$w_3 = \frac{1}{r_{o2}(C_{gd2} + C_{db2})}$$

$$(b) \frac{V_{in} - V_s}{R_s} - \frac{V_s}{\frac{1}{sC_1}} - (g_{m1} + g_{mb1})V_s = 0$$

$$V_s(g_{m1} + g_{mb1}) - \frac{V_{g2}}{\frac{1}{sC_{d1}}} + \frac{V_{out} - V_{g2}}{\frac{1}{sC_{q2d}}} = 0$$

$$\frac{V_{out}}{V_{g2}} = \frac{sC_{gd2} - g_{m2}}{s(C_{gd2} + C_{d2})}$$

$$\overset{\circ}{w_3} = 0$$

$$w_2 = \frac{C_{gd2}g_{m2}}{C_{gd2}C_{d2} + C_{d1}(C_{gd2} + C_{d2})}$$

$$w_1 = \frac{\frac{1}{R_s} + g_{m1} + g_{mb1}}{C_{s1}}$$

6.8

Calculate the input impedance and the transfer function of each circuit in Fig.6.60.

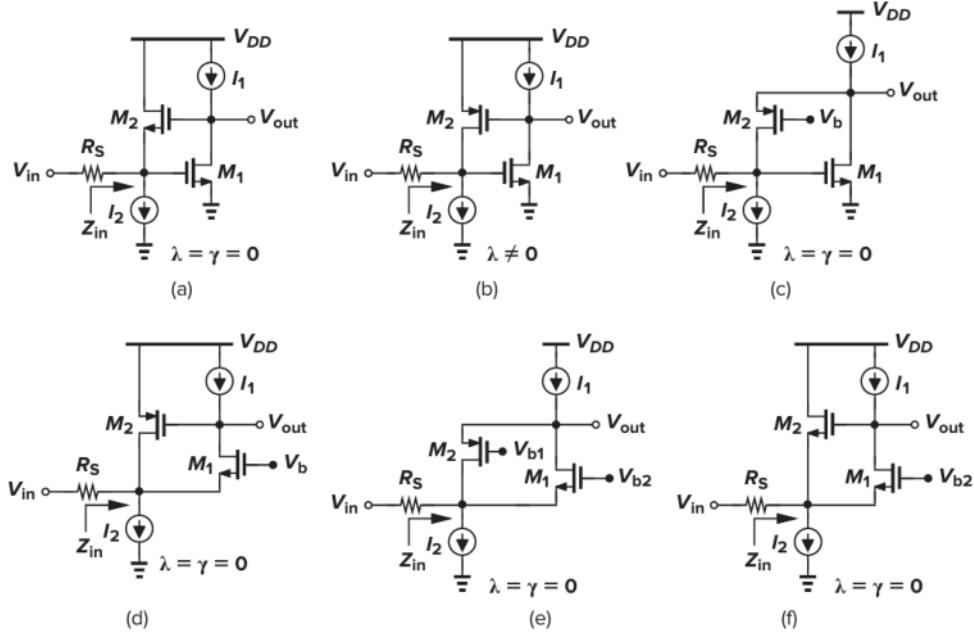


Figure 6.60

(a) Draw small-signal diagram. $C_1 = C_{sb2} + C_{gs1}$

$$C_2 = C_{gs2} + C_{gd1}$$

$$C_3 = C_{gd2} + C_{db1}$$

$$\frac{V_{in}-V_{g1}}{R_s} + g_{m2}(V_{out} - V_{g1}) + \frac{V_{out}-V_{g1}}{\frac{1}{sC_2}} + \frac{V_{g1}}{\frac{1}{sC_1}} = 0$$

$$\frac{V_{g1}-V_{out}}{\frac{1}{sC_2}} - g_{m1}V_{g1} - \frac{V_{out}}{\frac{1}{sC_3}} = 0$$

We can solve and get $\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_s}(sC_2 - g_m)}{g_{m1}g_{m2} + (\frac{C_2+C_3}{R_s} + g_{m1}C_2 + g_{m2}C_3)s + (C_1C_2 + C_1C_3 + C_2C_3)s^2}$

(b) Similar with (a), $C_1 = C_{db2} + C_{gs1}$

$$C_2 = C_{gd2} + C_{gd1}$$

$$C_3 = C_{gs2} + C_{db1}$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_s}(sC_2 - g_{m1})}{\frac{1}{r_{o1}}(\frac{1}{r_{o2}} + \frac{1}{R_3}) - g_{m1}g_{m2} + [(\frac{1}{r_{o1}} + \frac{1}{R_s})(C_2 + C_3) + \frac{C_1 + C_2}{r_{o1}} + C_2(g_{m1} + g_{m2})]s + (C_1C_2 + C_1C_3 + C_2C_3)s^2}$$

$$(c) \frac{V_{in}-V_{g1}}{R_s} - sC_1V_{g1} + g_{m2}V_{out} - \frac{V_{out}-V_{g1}}{\frac{1}{sC_2}} = 0$$

$$\frac{V_{g1}-V_{out}}{\frac{1}{sC_2}} - g_{m1}V_{g1} - V_{out}g_{m2} - V_{out}sC_2 = 0$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_s}(sC_2 - g_{m1})}{(g_{m2} + sC_2)(g_{m1} - sC_2) + (g_{m2} + sC_2 + sC_3)(\frac{1}{R_s} + sC_2 + sC_1)}$$

$$C_1 = C_{db2} + C_{gd2} + C_{gs1}$$

$$C_2 = C_{gd1}$$

$$C_3 = C_{sb2} + C_{gs2} + C_{db1}$$

$$(d) \frac{V_{in}-V_x}{R_s} - g_{m2}V_{out} - \frac{V_x}{\frac{1}{sC_1}} + \frac{V_{out}-V_x}{\frac{1}{sC_2}} - g_{m1}V_x = 0$$

$$\frac{V_x-V_{out}}{\frac{1}{sC_2}} - \frac{V_{out}}{\frac{1}{sC_3}} + g_{m1}V_x = 0$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_s}(sC_3 + g_{m1})}{g_{m1}g_{m2} + (\frac{C_2+C_3}{R_s} + g_{m1}C_2 + g_{m2}C_3)s + (C_1C_2 + C_1C_3 + C_2C_3)s^2}$$

$$C_1 = C_{db2} + C_{sb1} + C_{gs1}$$

$$C_2 = C_{gd2}$$

$$C_3 = C_{gs2} + C_{db1} + C_{gd1}$$

$$(e) \frac{V_{in}-V_x}{R_s} + g_{m2}V_{out} - \frac{V_x}{\frac{1}{sC_1}} - g_{m1}V_x = 0$$

$$-g_{m2}V_{out} + g_{m1}V_x - \frac{V_{out}}{\frac{1}{sC_2}} = 0$$

$$C_1 = C_{db2} + C_{gd2} + C_{sb1} + C_{gs1}$$

$$C_2 = C_{sb2} + C_{gs2} + C_{db1} + C_{gd1}$$

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{g_{m1}}{g_{m2} + (C_2 + g_{m1}R_sC_2 + g_{m2}R_sC_1)s + C_1C_2R_ss^2} \\ (\text{f}) \frac{V_{out}-V_x}{R_s} + g_{m2}(V_{out} - V_x) - \frac{V_x}{sC_1} - g_{m1}V_x + \frac{V_{out}-V_x}{sC_2} &= 0 \\ \frac{V_x-V_{out}}{sC_2} + g_{m1}V_x - \frac{V_{out}}{sC_3} &= 0 \\ \frac{V_{out}}{V_{in}} &= \frac{\frac{1}{R_s}(sC_3 + g_{m1})}{-g_{m1}g_{m2} + (\frac{C_2+C_3}{R_s} + g_{m2}C_2 + g_{m1}C_2)s + (C_1C_2 + C_1C_3 + C_2C_3)s^2} \end{aligned}$$

6.9

Calculate the gain of each circuit in Fig.6.61 at very low and very high frequencies. Neglect all other capacitances and assume that $\lambda = 0$ for circuits (a) and (b) and $\gamma = 0$ for all of the circuits.

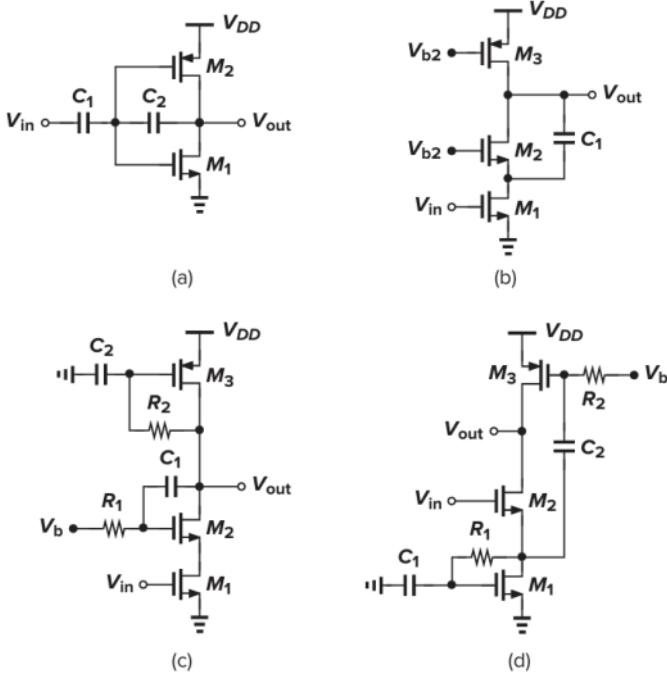


Figure 6.61

$$(\text{a}) A_{vh} = 1$$

$$\frac{V_{in}-V_g}{\frac{1}{sC_1}} = V_g(g_{m1} + g_{m2})$$

$$V_{out} = V_{in} - V_g(g_{m1} + g_{m2})(\frac{1}{sC_1} + \frac{1}{sC_2})$$

$$A_{vl} = -\frac{C_1}{C_2}$$

$$(\text{b}) A_{vh} = -g_{m1}(r_{o3}||r_{o1})$$

$$A_{vl} = -g_{m1}[r_{o3}||(1 + g_{m2}r_{o2})r_{o1}]$$

$$(\text{c}) A_{vl} = -g_{m1}[\frac{1}{g_{m3}}||(1 + g_{m2}r_{o2})r_{o1}]$$

$$A_{vh} = -g_{m1}[R_2||r_{o3}||R_1||(\frac{1}{g_{m2}} + r_{o1})]$$

$$(\text{d}) A_{vl} = \frac{-g_{m2}}{1+g_{m2}r_{o2}+\frac{g_{m1}}{r_{o2}}}[r_{o3}||(1 + g_{m2}r_{o2})\frac{1}{g_{m1}}]$$

$$-g_{m3}V_x - \frac{V_{out}}{r_{o3}} = g_{m2}(V_{in} - V_x) + \frac{V_{out}-V_x}{r_{o2}} = \frac{V_x}{R_s}$$

$$A_{vh} = \frac{-g_{m2}}{\frac{1}{r_{o2}}+(\frac{1}{R_s}+\frac{1}{r_{o2}}+g_{m2})\frac{1}{r_{o3}(g_{m3}+\frac{1}{R_s})}}$$

6.10

Calculate the gain of each circuit in Fig.6.62 at very low and very high frequencies. Neglect all other capacitances and assume that $\lambda = \gamma = 0$

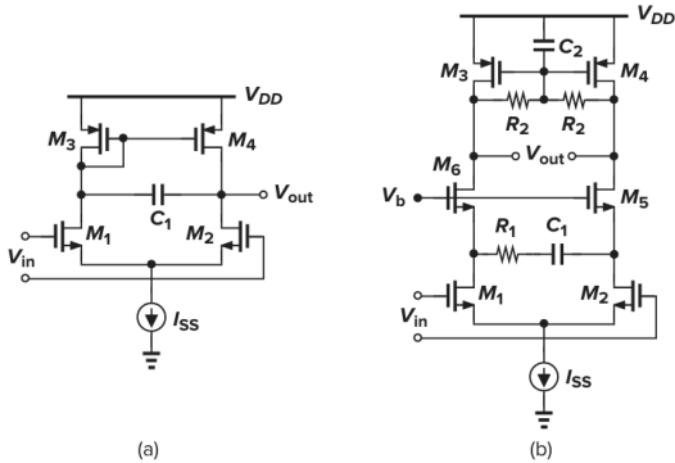


Figure 6.62

$$(a) A_{vl} = g_{m1}(r_{o4} || r_{o2})$$

$$A_{vh} = 0$$

$$(b) A_{vl} = -g_{m1}R_2$$

$$A_{vh} = -g_{m1} \frac{\frac{R_1}{2}}{\frac{1}{g_{m6}} + \frac{R_1}{2}} R_2$$

6.11

Consider the cascode stage shown in Fig.6.63. In our analysis of the frequency response of a cascode stage, we assumed that the gate-drain overlap capacitance of M_1 is multiplied by $g_{m1}/(g_{m2} + g_{mb2})$. Recall from Chapter 3, however, that with a high resistance loading the drain of M_2 , the resistance seen looking into the source of M_2 can be quite high, suggesting a much higher Miller multiplication factor for C_{GD1} . Explain why C_{GD1} is still multiplied by $1 + g_{m1}/(g_{m2} + g_{mb2})$ if C_L is relatively large.

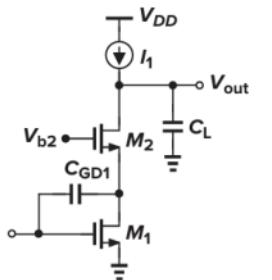


Figure 6.63

$$A_v = -g_{m1} [r_{o1} || (\frac{r_{o2} + \frac{1}{sC_L}}{1 + (g_{m2} + g_{mb2})r_{o2}})]$$

$$\text{If } C_L \text{ is very large, } A_v = \frac{-g_{m1}}{g_{m2} + g_{mb2}}$$

$$\text{Miller coefficient} = 1 - A_v$$

6.12

Neglecting other capacitance, calculate Z_X in the circuits of Fig.6.64. Sketch $|Z_X|$ versus frequency.

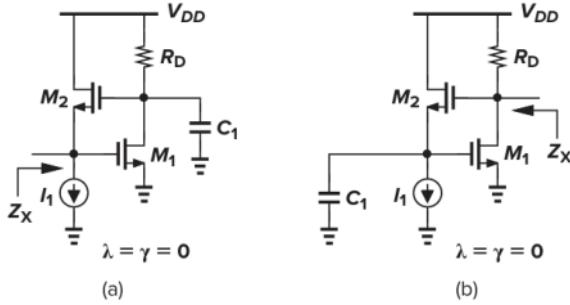


Figure 6.64

$$(a) I_x = [-g_{m1}(R_D \parallel \frac{1}{sC_1})V_x - V_x]g_{m2} \times (-1)$$

$$Z_x = \frac{V_x}{I_x} = \frac{1}{g_{m2}(1 + \frac{1}{R_D} + sC_1)}$$

$$(b) I_x = \frac{V_x}{R_D} + V_x g_{m2} (\frac{1}{g_{m2}} \parallel \frac{1}{sC_1}) g_{m1}$$

$$Z_x = \frac{V_x}{I_x} = \frac{1}{\frac{1}{R_D} + \frac{g_{m1}g_{m2}}{g_{m2} + sC_1}}$$

6.13

The common-gate stage of Fig.6.31 is designed with $(W/L)_1 = 50/0.5$, $I_{D1} = 1mA$, $R_D = 2k\Omega$, and $R_S = 1k\Omega$. Assuming $\lambda = 0$, determine the poles and the low-frequency gain. How do these results compare with those obtained in Problem 6.9?

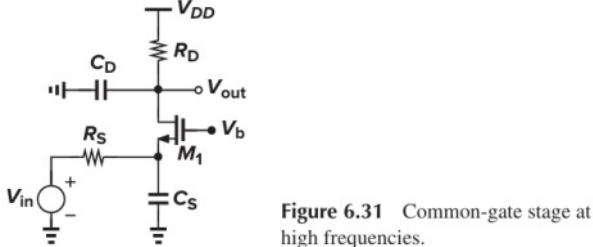


Figure 6.31 Common-gate stage at high frequencies.

$$C_S = C_{gs} = \frac{2}{3}WLC_{ox} + WC_{ov} = 83.8fF$$

$$C_D = C_{gd} = WC_{ov} = 20fF$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 5.18mS$$

$$A_v = G_m R_{out} = \frac{1}{R_S + \frac{1}{g_m}} R_D = 1.68$$

$$w_1 = \frac{1}{(R_S \parallel \frac{1}{g_m}) C_s} = 73.7 \times 10^9$$

$$w_2 = \frac{1}{R_D C_D} = 25 \times 10^9$$

6.14

Suppose that in the cascode stage of Fig.6.34, a resistor R_G appears in series with the gate of M_2 . Including only C_{GS2} , neglecting other capacitances, and assuming $\lambda = \gamma = 0$, determine the transfer function.

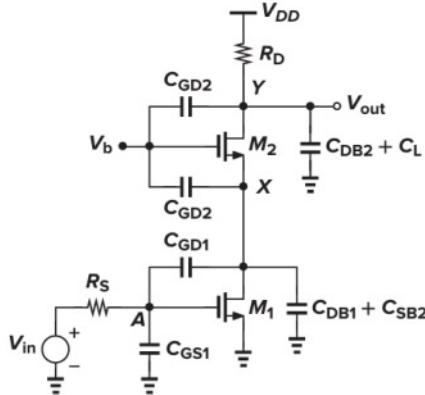


Figure 6.34 High-frequency model of a cascode stage.

$$g_{m2}(V_{g2} - V_{s2}) - g_{m1}V_{in} + \frac{V_{g2} - V_{s2}}{\frac{1}{sC_{g2}}} = 0$$

$$V_{out} = -g_{m2}(V_{g2} - V_{s2})R_D$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}g_{m2}R_D}{g_{m2} + sC_{g2}}$$

6.15

Apply the method of Fig.6.18 to the circuit of Fig.6.41(b) to determine the zero of the transfer function.

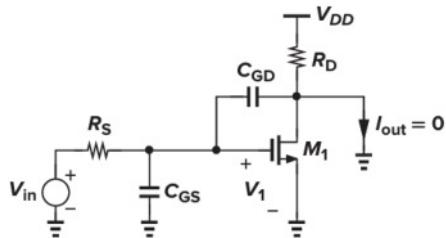


Figure 6.18 Calculation of the zero in a CS stage.

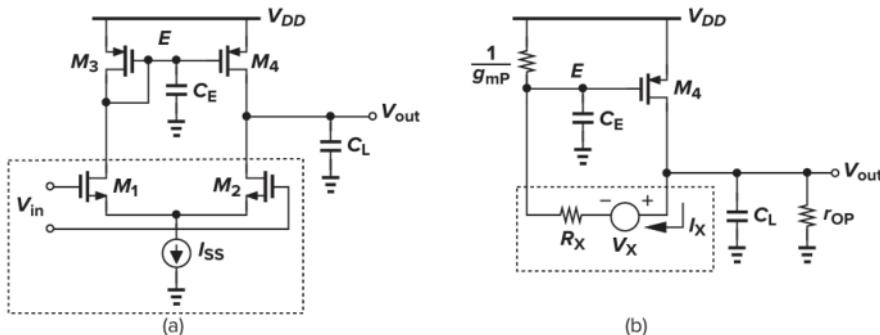


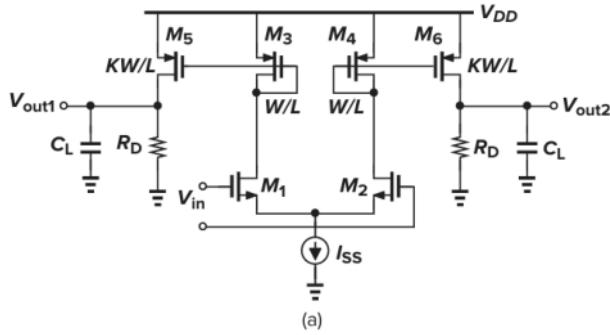
Figure 6.41 (a) Simplified high-frequency model of differential pair with active current mirror; (b) circuit of (a) with a Thevenin equivalent.

$$I_x + I_x \frac{1}{g_{mp} + sC_E} g_{mp} = 0$$

$$s_z = -\frac{2g_{mp}}{C_E}$$

6.16

The circuit of Fig.6.42(a) is designed with $(W/L)_{1,2} = 50/0.5$ and $(W/L)_{3,4} = 10/0.5$. If $I_{SS} = 100\mu A$, $K = 2$, $C_L = 0$, and R_D is implemented by an NFET having $W/L = 50/0.5$, estimate the poles and zeros of the circuit. Assume the amplifier is driven by an ideal voltage source.



$$w_z = \frac{g_{m5}}{C_{gd5}}$$

$$w_1 = \frac{1}{\frac{1}{g_{m3}}(1-A_{v5})C_{gd5}}$$

$$w_2 = \frac{1}{(r_{o5}||R_D)(C_{gd5}+C_{gdD})}$$

$$g_{m3} = \sqrt{2\mu_n C_{ox} (\frac{W}{L})_3 I_{SS} \frac{1}{2}} = 0.277 mS$$

$$C_{gd5} = W_5 C_{ovp} = 6 fF$$

$$r_{o5}||R_D = \frac{1}{(\lambda_n + \lambda_p) \frac{I_{SS}}{2} K} = 33.3 k\Omega$$

$$g_{m5} = \sqrt{2} g_{m3} = 0.392 mS$$

$$A_{v5} = -g_{m5}(r_{o5}||R_D) = -13.1$$

6.17

A differential pair driven by an ideal voltage source is required to have a total phase shift of 135° at the frequency where its gain drops to unity.

(a) Explain why a topology in which the load is realized by diode-connected devices or current sources does not satisfy this condition.

(b) Consider the circuit shown in Fig.6.65. Neglecting other capacitances, determine the transfer function. Explain under what conditions the load exhibits an inductive behavior. Can this circuit provide a total phase shift of 135° at the frequency where its gain drops to unity?

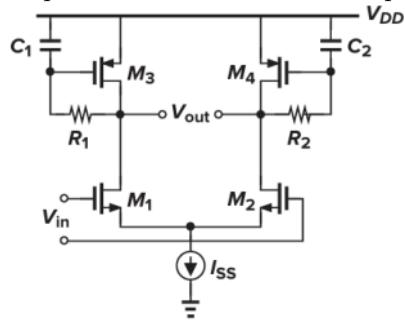


Figure 6.65

(a) These types of loads are purely capacitive or resistive, and they result in a single-pole frequency response in the differential amplifier.

$$(b) I_x = \frac{V_x}{R_1 + \frac{1}{sC_1}} + V_x \frac{\frac{1}{sC_1}}{\frac{1}{sC_1} + R_1} g_{mp}$$

$$Z_x = \frac{V_x}{I_x} = R_1 \frac{s + \frac{1}{R_1 C_1}}{s + \frac{g_{mp}}{C_1}}$$

When $\frac{1}{R_1 C_1} \ll \frac{g_{mp}}{C_1}$, it exhibits inductive behavior.

$$A_v = g_{mn}(Z_x || \frac{1}{sC_0})$$

6.18

Repeat Example 6.3, but assume that I_1 is replaced with a resistor R_1 .

Calculate the input resistance of the circuit shown in Fig. 6.7(a).

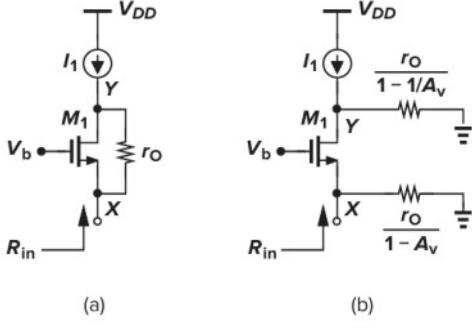


Figure 6.7

$$R_{in} = \frac{r_o + R_1}{1 + (g_m + g_{mb})r_o}$$

6.19

A resistively-degenerated common-source stage bootstraps C_{GS} in a manner similar to a source follower. Estimate the input capacitance of such a stage.

$$A_v = g_m \frac{r_o + R_D}{r_o + R_D} R_s \parallel \frac{r_o + R_D}{1 + (g_m + g_{mb})r_o}$$

$$C_{in} = C_{gs}(1 - A_v)$$

6.20

Determine the transfer function of a CG stage with a resistance R_G in series with the gate, including only C_{GS} and C_{GD} . Assume $\lambda = \gamma = 0$.

$$\frac{V_g}{R_g} + \frac{\frac{V_g - V_{in}}{sC_{gs}}}{\frac{1}{sC_{gs}}} +$$

$$\frac{V_g - V_{out}}{sC_{gd}} = 0$$

$$\frac{V_{out} - V_g}{sC_{gd}} + g_m(V_g - V_{in}) + \frac{V_{out}}{R_D} = 0$$

$$\text{We can solve and get } H(s) = \frac{s^2 C_{gs} C_{gd} + s g_m C_{gd} + \frac{g_m}{R_G}}{s^2 C_{gs} C_{gd} + s(\frac{C_{gd}}{R_G} + \frac{C_{gd} + C_{gs}}{R_D} + g_m C_{gd}) + \frac{1}{R_D R_G}}$$

6.21

Determine the transfer function of a CG stage with a resistance R_G in series with the gate, including only C_{GD} and C_{DB} . Assume $\lambda = \gamma = 0$.

$$V_g = \frac{R_g}{R_g + \frac{1}{sC_{gd}}} V_{out}$$

$$V_{out} = -g_m \left(\frac{R_g}{R_g + \frac{1}{sC_{gd}}} V_{out} - V_{in} \right) [R_D \parallel \frac{1}{sC_{db}}] (R_G + \frac{1}{sC_{gd}})$$

$$\text{And we can get } A_v = \frac{g_m}{\frac{1}{R_D} + sC_{db} + \frac{1 + g_m R_G}{R_G + \frac{1}{sC_{gd}}}}$$

6.22

Determine the transfer function of a differential pair with current-source loads for differential signals. Assume that each input is driven by a series resistance of R_S .

$$\frac{V_{in} - V_g}{R_s} + \frac{V_{out} - V_g}{\frac{1}{sC_{gd}}} - \frac{V_g}{\frac{1}{sC_{gs}}} = 0$$

$$\frac{V_g - V_{out}}{\frac{1}{sC_{gd}}} - g_m V_g - \frac{V_{out}}{r_o \parallel \frac{1}{sC_{db}}} = 0$$

$$H(s) = \frac{\frac{1}{R_s}}{\frac{[\frac{1}{R_s} + s(C_{gd} + C_{gs})][\frac{1}{r_o} + s(C_{gd} + C_{db})]}{sC_{gd} - g_m} - sC_{gd}}$$

6.23

Consider a circuit containing only one capacitor, C_1 . We set the main input to zero and apply a current source, I_X , in parallel with C_1 , obtaining the voltage across it, V_X , and hence $V_X(s)/I_X(s)$ (Fig.6.66). This impedance has the same pole as the main transfer function. Prove that the pole is given by $1/(R_1 C_1)$, where R_1 is the resistance seen by C_1 .

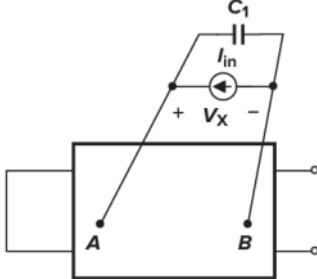


Figure 6.66

$$\frac{V_x}{I_x} = \frac{1}{\frac{1}{R_1} + sC_1} = \frac{R_1}{1 + sR_1 C_1}$$

6.24

Repeat Example 6.22, but with $\lambda > 0$ and $\gamma > 0$.

Estimate the -3-dB bandwidth of a resistively-degenerated common-source stage. Assume $\lambda = \gamma = 0$.

Solution

Shown in Fig. 6.53(a), the small-signal model is of third order,⁸ providing little intuition. The zero-value time constant method can give a rough estimate of the circuit's bandwidth, thereby revealing the contribution of each capacitor.

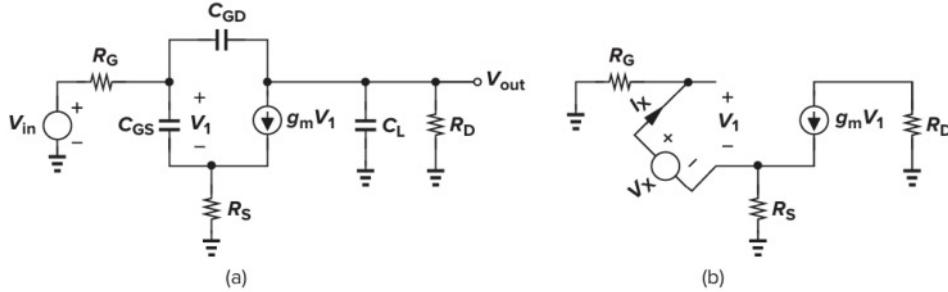


Figure 6.53

$$G_m = \frac{-g_m}{1 + (g_m + g_m b)R_s + \frac{R_s}{r_o}}$$

$$R_{out} = R_D \parallel (1 + g_m r_o)R_s$$

$$A_v = G_m R_{out}$$

$$C_{out} = C_L + C_{db} + C_{gd}$$

$$w_{-3dB}^{-1} = R_{out} C_{out} + R_G A_v C_{gd}$$

6.25

Prove that the -3dB bandwidth of N first-order identical gain stage is given by $\sqrt{N}\sqrt{2 - 1}w_p$, where w_p denotes the pole of one stage.

$$H(w) = \left(\frac{A}{1+jw/w_p}\right)^N$$

$$|H(w)| = \frac{A^N}{\left(\sqrt{1+\frac{w^2}{w_p^2}}\right)^N} = \frac{A^N}{\sqrt{2}}$$

$$w = w_p \sqrt{2^{\frac{1}{N}} - 1}$$

6.26

Prove that if $C_{GD} = 0$, then Eq.(6.30) reducecs to the product of two transfer functions that can simply be obtained by association of poles with the input and output nodes.

$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}-g_m)R_D}{R_S R_D \xi s^2 + [R_S(1+g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})s] + 1}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{R_S R_D C_{GS} C_{DB} s^2 + (R_S C_{GS} + R_D C_{DB})s + 1} = \frac{1}{R_s C_{GS} s + 1} \frac{-g_m R_D}{R_D C_{DB} s + 1}$$

7 Noise

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

7.1

A common-source stage incorporates a $50\mu m/0.5\mu m$ NMOS device biased at $I_D = 1mA$ along with a load resistor of $2k\Omega$. What is the total input-referred thermal noise voltage in a 100-MHz bandwidth?

$$\overline{V_{n,in}^2} = (4kT \frac{\gamma}{g_m} + \frac{4kT}{g_m^2 R_D}) \times 100MHz$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 5.18mS$$

$$\overline{V_{n,in}} = 15.6\mu V/\sqrt{Hz}$$

7.2

Consider the common-source stage of Fig.7.42. Assume that $(W/L)_1 = 50/0.5$, $I_{D1} = I_{D2} = 0.1mA$, and $V_{DD} = 3V$. If the contribution of M_2 to the input-referred noise voltage (noise voltage squared) must be one-fifth of that of M_1 , what is the maximum output voltage swing of the amplifier?

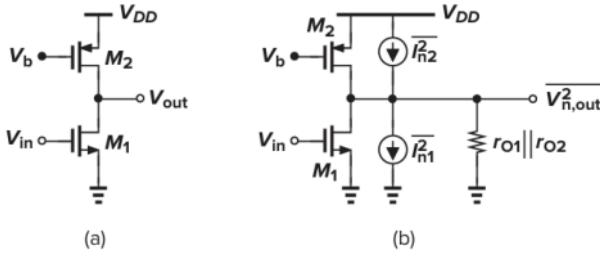


Figure 7.42

$$\overline{I_{n,out}^2} = 4kT\gamma(g_{m1} + g_{m2})$$

$$g_{m2} = \frac{1}{5}g_{m1}$$

$$V_{out,max} = V_{DD} - V_{ov2}$$

$$V_{out,max} = V_{od1}$$

$$g_m = \frac{2I_D}{V_{od}}$$

$$V_{od2} = 5V_{od1} = 5\sqrt{\frac{2I_D}{\mu_n C_{ox}}} = 0.61V$$

$$V_{out,max} = 2.39V, V_{out,min} = 0.122V$$

7.3

Using the distributed model of Fig.7.21(c) and ignoring the channel thermal noise, prove that, for gate noise calculations, a distributed gate resistance of R_G can be replaced by a lumped resistance equal to $R_G/3$. (Hint: model the noise of R_{Gj} by a series voltage source and calculate the total drain noise current. Watch for correlated sources of noise.)

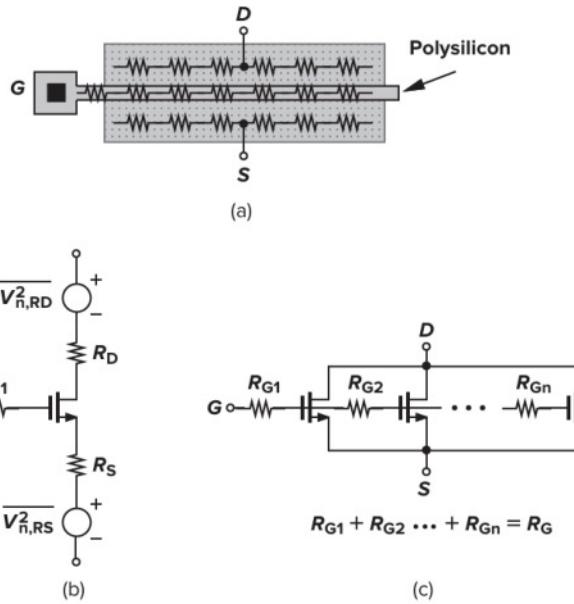
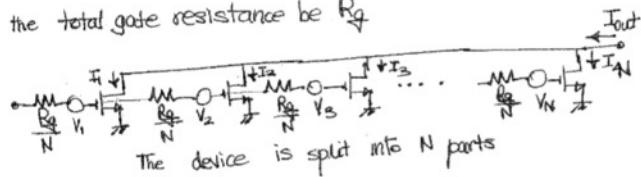


Figure 7.21 (a) Layout of a MOSFET indicating the terminal resistances; (b) circuit model; (c) distributed gate resistance.

Let the total gate resistance be R_g



Ignoring all capacitive parasitics, $\gamma_0 \dots$

$$\begin{aligned} I_{out} &= I_1 + I_2 + \dots + I_N \\ &= \frac{g_m}{N} V_1 + \frac{g_m}{N} (V_1 + V_2) + \dots + \frac{g_m}{N} (V_1 + V_2 + \dots + V_N) \quad \left(\frac{g_m}{N} \text{ is the transconductance of each piece} \right) \\ &= \frac{g_m}{N} (N V_1 + (N-1) V_2 + \dots + V_N) \end{aligned}$$

$$\begin{aligned} \frac{I_{out}^2}{\Delta f} &= \frac{g_m^2}{N^2} \left(N^2 \frac{4kT R_g}{N} + (N-1)^2 \frac{4kT R_g}{N} + \dots + \frac{4kT R_g}{N} \right) \quad \left(\text{The noise generated by the individual gate resistance pieces are uncorrelated} \right) \\ &= \frac{g_m^2}{N^3} \times 4kT R_g \times \sum_{i=1}^N i^2 \\ &= \frac{g_m^2}{N^3} \times 4kT R_g \times \frac{(N)(N+1)(2N+1)}{6} \end{aligned}$$

As $N \rightarrow \infty$, $\frac{I_{out}^2}{\Delta f} = g_m^2 \times \frac{4kT R_g}{3}$ \rightarrow equivalent lumped gate resistance that produces the same output current noise.

7.4

Prove that the output noise current of Fig.7.39(c) is given by Eq.(7.73).

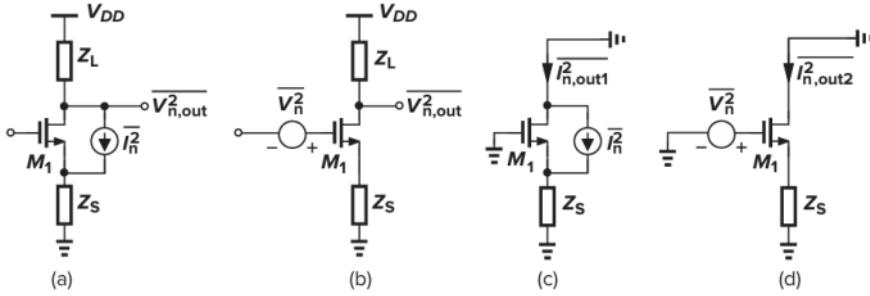


Figure 7.39 Equivalent CS stages.

$$I_{n,out1} = \frac{I_n}{Z_s(g_m + g_{mb} + 1/r_o) + 1} \quad (7.73)$$

$$I_{n,out} = g_m(-Z_s I_{n,out}) + \frac{-Z_s I_{n,out}}{r_{o1}} + I_n$$

$$I_{n,out} = \frac{I_n}{1 + Z_s(g_m + \frac{1}{r_o})}$$

7.5

Calculate the input-referred flicker noise voltage of the circuit shown in Fig.7.70.

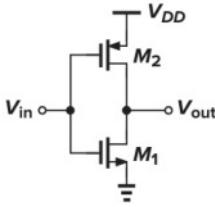


Figure 7.70

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_v} = \frac{(\frac{K}{C_{ox}(WL)_1 f} g_{m1}^2 + \frac{K}{C_{ox}(WL)_2 f} g_{m2}^2)(r_{o1} || r_{o2})^2}{(g_{m1} + g_{m2})(r_{o1} || r_{o2})} = \frac{(\frac{K}{C_{ox}(WL)_1 f} g_{m1}^2 + \frac{K}{C_{ox}(WL)_2 f} g_{m2}^2)(r_{o1} || r_{o2})}{(g_{m1} + g_{m2})}$$

7.6

Calculate the input-referred thermal noise voltage of each circuit in Fig.7.71. Assume that $\lambda = \gamma = 0$.

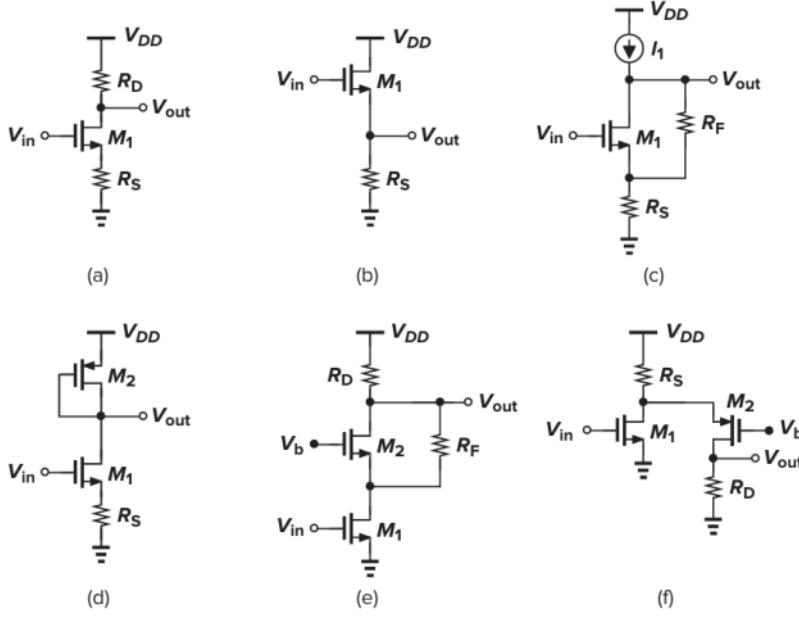


Figure 7.71

$$(a) \overline{V_{in,M1}^2} = 4kT\gamma \frac{1}{g_m}, \overline{V_{in,R_S}^2} = 4kTR_s, \overline{V_{in,R_D}^2} = \frac{4kTR_D}{(\frac{g_m R_D}{1+g_m R_s})^2}$$

$$(b) \overline{V_{n,out}^2} = (4kT\gamma g_m + \frac{4kT}{R_s})(\frac{1}{g_m}||R_S)^2, A_v = \frac{g_m R_s}{1+g_m R_s}, \overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_v^2}$$

$$(c) I_{n,out} = g_{m1}(-V_y) + I_{n,m1} + I_{n,R_F} + \frac{-V_y}{R_F} = \frac{V_y}{R_s} + I_{n,R_F}$$

$$G_m = \frac{g_m / R_s}{(1/R_s + 1/R_F + g_{m1})}$$

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{G_m^2}$$

$$(d) \overline{V_{in,M1+R_S}^2} = 4kT\gamma \frac{1}{g_m} + 4kTR_S, \overline{V_{in,M2}^2} = 4kT\gamma \frac{1}{g_m}/A_v^2, A_v = G_m R_{out} = \frac{g_{m1}}{(1+g_{m1}R_s)g_{m2}}$$

$$\overline{V_{in}^2} = \overline{V_{in,M1+R_S}^2} + \overline{V_{in,M2}^2}$$

$$(e) \overline{V_{out}^2} = (4kT/R_D + 4kT\gamma g_{m1})R_D^2, |A_v| = g_m R_D, \overline{V_{in}^2} = \overline{V_{out}^2}/|A_v|^2$$

(f) Use small signal diagram.

7.7

Calculate the input-referred thermal noise voltage of each circuit in Fig.7.72. Assume that $\lambda = \gamma = 0$.

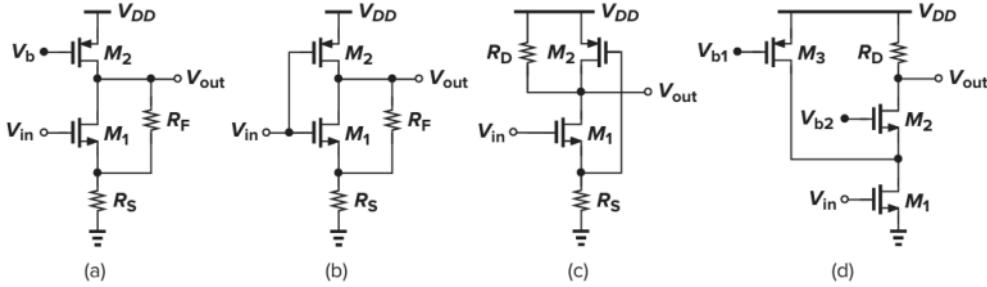


Figure 7.72

$$(a) I_{n,M2} + I_{n,out} = g_{m1}(-V_y) + I_{n,m1} + I_{n,R_F} + \frac{-V_y}{R_F}$$

$$V_y = (I_{n,out} + I_{n,M2} - I_{n,R_s})R_s$$

Use these two equations we can get $\overline{I_{n,out}^2}$.

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m R_F}{R_F + R_S + g_m R_F R_S}$$

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{G_m^2}$$

(b) $\overline{I_{n,out}^2}$ is as same as (a).

And we can get G_m using small signal diagram.

(c) Similar.

$$(d) \overline{V_{n,out}^2} = (4kT\gamma g_{m1} + 4kT\gamma g_{m3} + 4kT/R_D)R_D^2$$

$$|A_V| = g_m R_D$$

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_v^2}$$

7.8

Calculate the input-referred thermal noise voltage and current of each circuit in Fig.7.73. Assume that $\lambda = \gamma = 0$.

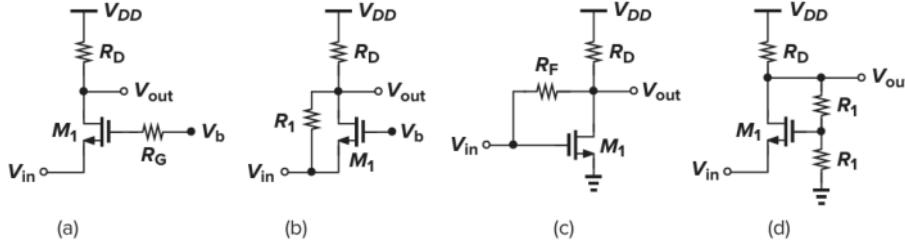


Figure 7.73

$$(a) A_v = g_{m1}R_D$$

When the input is short, $\overline{V_{n,out}^2} = 4kTR_D + (4kTR_G + 4kT\gamma/g_{m1})g_{m1}^2R_D^2$

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_v^2} = 4kT(\frac{1}{g_{m1}^2R_D} + R_G + \gamma/g_{m1})$$

When the input is open, $\overline{V_{n,out}^2} = 4kTR_D$.

$$V_{out}/I_{in} = R_D, \overline{I_{n,in}^2} = 4kT/R_D$$

$$(b) \text{ When the input is short, } \overline{V_{n,out}^2} = 4kT(\frac{1}{R_D} + \frac{1}{R_1} + \gamma g_{m1})(R_D||R_1)^2$$

$$G_m = -g_{m1} - \frac{1}{R_1}$$

$$A_V = -G_m R_{out} = (-g_{m1} - \frac{1}{R_1})(R_D||R_1)$$

$$\overline{V_{n,in}^2} = 4kT \frac{1}{g_{m1} + \frac{1}{R_1}} (1/R_D + 1/R_1 + \gamma g_{m1})$$

When the input is open, $\overline{V_{n,out}^2} = 4kTR_D$.

$$V_{out}/I_{in} = R_D, \overline{I_{n,in}^2} = 4kT/R_D$$

$$(c) \overline{I_{n,out}^2} = 4kT/R_D + 4kT/R_F + 4kT\gamma g_{m1}$$

Using small signal diagram, $G_m = g_{m1} - \frac{1}{R_F}$

$$\overline{V_{n,in}^2} = \overline{I_{n,out}^2}/G_m^2$$

$$\text{When the input is open, } \overline{I_{n,out}^2} = \frac{4kT}{R_D} + 4kT\gamma g_{m1} + 4kTR_F g_{m1}^2$$

$$A_i = \frac{I_{out}}{I_{in}} = \frac{I_{in} + I_{in}R_F(-g_m)}{I_{in}} = 1 - g_{m1}R_F$$

(d) Using small signal diagram.

7.9

Calculate the input-referred thermal noise voltage and current of each circuit in Fig. 7.74. Assume that $\lambda = \gamma = 0$.

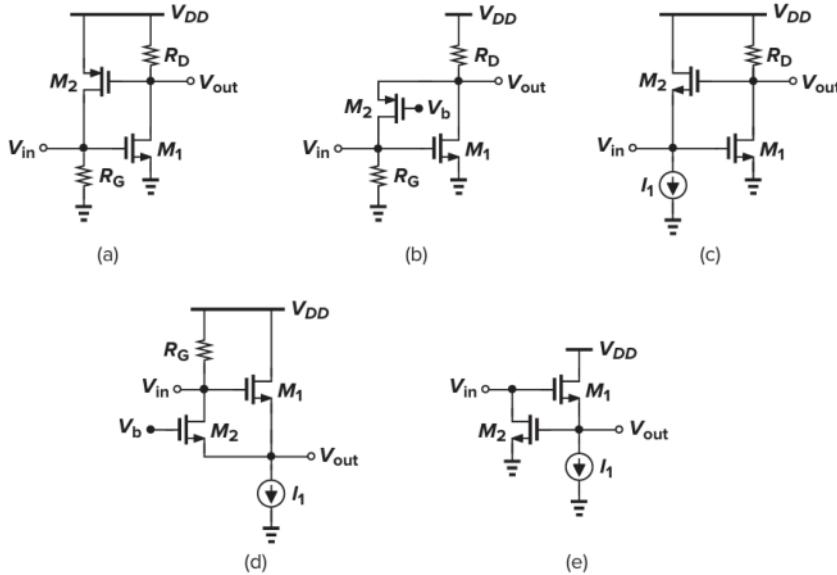


Figure 7.74

(a) For V: $\overline{I_{n,out}^2} = 4kT/R_D + 4kT\gamma g_{m1}$

$$G_m = \frac{-g_{m1}}{R_G}$$

For I: $\overline{I_{n,out}^2} = 4kT/R_D + 4kT\gamma g_{m1} + 4kT(\frac{1}{R_G} + \gamma g_{m2})R_G^2 g_{m1}^2$

$$A_I = -R_G g_{m1}$$

(b) For V: $\overline{I_{n,out}^2} = 4kT/R_D + 4kT\gamma(g_{m1} + g_{m2})$, $G_m = -g_{m1}$

For I: $\overline{I_{n,out}^2} = 4kT/R_D + 4kT\gamma g_{m1} + 4kTR_G g_{m1}^2 + 4kT\gamma g_{m2}(1 + (R_G g_{m1}))^2$, $A_I = -R_G g_{m1}$

(c) For V: $\overline{I_{n,out}^2} = 4kT/R_D + 4kT\gamma g_{m1}$

$$G_m = \frac{-g_{m1}}{R_G}$$

For I: $\overline{I_{n,out}^2} = 4kT/R_D + 4kT\gamma g_{m1} + 4kT\gamma g_{m2}(\frac{1}{g_{m2}})^2(g_{m1})^2$

$$A_I = -\frac{1}{g_{m2}} g_{m1}$$

(d) For V: $\overline{I_{n,out}^2} = 4kT\gamma(g_{m1} + g_{m2})$

$$G_m = \frac{-g_{m1}}{R_G}$$

For I: $\overline{I_{n,out}^2} = 4kT\gamma g_{m1} + 4kTR_G g_{m1}^2 + 4kT\gamma g_{m2}(1 + R_G g_{m1})^2$

$$A_I = -R_G g_{m1}$$

(e) For V: $\overline{I_{n,out}^2} = 4kT\gamma g_{m1}$

$$G_m = -g_{m1}$$

7.10

Calculate the input-referred 1/f noise voltage and current of Fig.7.49 if the two capacitors are removed.

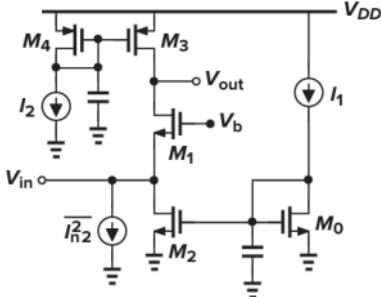


Figure 7.49

$$\overline{I_{n,out}^2} = \overline{I_{n4}^2} + \overline{I_{n3}^2} + \overline{I_{n2}^2} + \overline{I_{n0}^2}$$

$$A_v = 1$$

$$\overline{I_{n,in}^2} = \overline{I_{n,out}^2}/A_v^2$$

$$\text{For } V_{n,in}, \overline{I_{n,out}^2} = \overline{I_{n4}^2} + \overline{I_{n3}^2} + \overline{I_{n1}^2}$$

$$G_m = g_{m1}$$

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{G_m^2}$$

7.11

Calculate the input-referred 1/f noise voltage of the source follower shown in Fig.7.51.

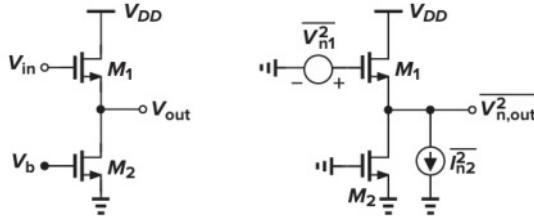


Figure 7.51 (a) Source follower; (b) circuit including noise sources.

$$\overline{V_{n,in}^2} = \overline{V_{n1}^2} + \frac{\overline{I_{n2}^2}}{g_{m1}^2} = \frac{K_n}{C_{ox}(WL)_1 f} + \frac{K_n}{C_{ox}(WL)_1 f} \frac{g_{m2}^2}{g_{m1}^2}$$

7.12

Assuming that $\lambda = \gamma = 0$, calculate the input-referred thermal noise voltage of each circuit in Fig.7.75. For part(a), assume that $g_{m3,4} = 0.5g_{m5,6}$.

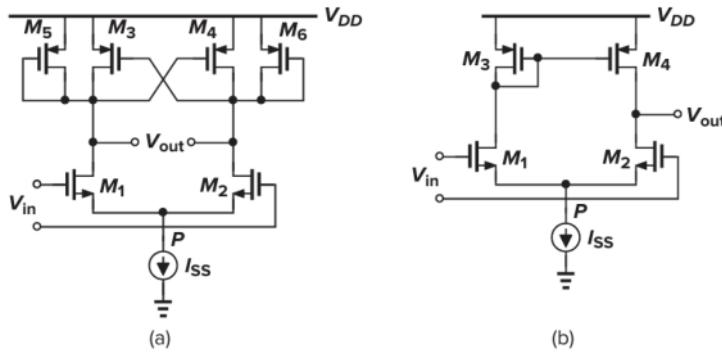


Figure 7.75

$$(a) \overline{V_{n,in}^2} = \frac{4kT\gamma}{g_{m1}^2} (g_{m1} + g_{m3} + g_{m5}) \times 2 = \frac{8kT\gamma}{g_{m1}^2} (g_{m1} + 1.5g_{m5})$$

$$(b) \overline{V_{n,in}^2} = 2 \times 4kT\gamma \frac{1}{g_{m1}^2} + 4kT\gamma g_{m4} \frac{1}{g_{m1}^2} \times 2 = \frac{8kT\gamma}{g_{m1}^2} (g_{m1} + g_{m3})$$

7.13

Consider the degenerated common-source stage shown in Fig.7.76.

(a) Calculate the input-referred thermal noise voltage if $\lambda = \gamma = 0$.

(b) Suppose linearity requirements necessitate that the dc voltage drop across R_S be equal to the overdrive voltage of M1. How does the thermal noise contributed by R_S compare with that contributed by M1?

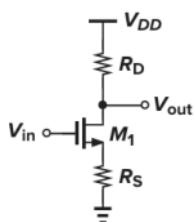


Figure 7.76

$$(a) \overline{V_{n,in}^2} = 4kT(\gamma/g_m + R_s) + 4kT/R_D \left(\frac{1+g_{m1}R_s}{g_{m1}} \right)^2$$

$$(b) IR_s = V_{dsat} = V_{gs} - V_{th}$$

$$I = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{dsat}^2$$

$$g_{m1} = \frac{2}{R_s}$$

$$4kTR_S = 3 \times 4kT \frac{2/3}{g_m}$$

7.14

Explain why Miller's theorem cannot be applied to calculate the effect of the thermal noise of a floating resistor.

For an amplifier with a floating resistor, we got $\overline{V_{n,in}^2} = 4kTR(\frac{A}{A+1})^2$ without using Miller's theorem. But we got the wrong answer $\overline{V_{n,in}^2} = 4kTRA$ if using Miller's theorem.

7.15

The circuit of Fig. 7.20 is designed with $(W/L)_1 = 50/0.5$ and $I_{D1} = 0.05mA$. Calculate the total RMS thermal noise voltage at the output in a 50-MHz bandwidth.

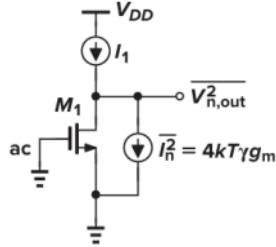


Figure 7.20

$$\overline{V_{n,out}^2} = 4kT\gamma g_m \left(\frac{1}{\lambda I_D} \right)^2 \times 50M$$

$$g_m = \sqrt{2\mu_n C_{ox} (W/L)_1 I_D}$$

$$\overline{V_{n,out}^2} = 990\mu V$$

7.16

For the circuit shown in Fig. 7.77, calculate the total output thermal and 1/f noise in a bandwidth [fL, fH]. Assume that $\lambda \neq 0$, but neglect other capacitances.

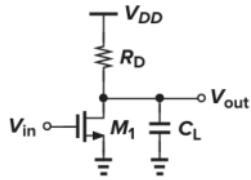


Figure 7.77

$$\overline{V_{n,out}^2} = (4kT/R_D + 4kT\gamma g_m + \frac{K_n}{C_{ox}WL_f} g_m^2)(R_D || r_o || \frac{1}{sC_L})^2$$

$$\overline{V_{n,out}^2} = \int_{f_L}^{f_H} \overline{V_{n,out}^2} df$$

7.17

Suppose in the circuit of Fig. 7.42, $(W/L)_{1,2} = 50/0.5$ and $I_{D1} = |I_{D2}| = 0.5mA$. What is the input-referred thermal noise voltage?

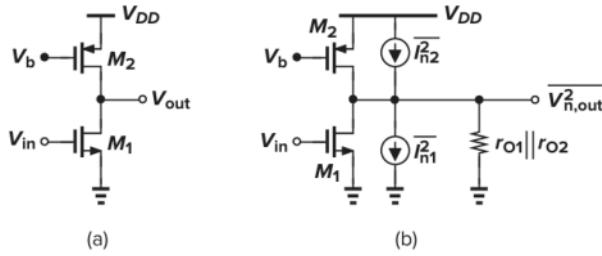


Figure 7.42

$$\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_{m1}} + 4kT\gamma g_{m2} \frac{1}{g_{m1}^2}$$

$$g_{mn} = \sqrt{2\mu_{n/p}C_{ox}(\frac{W}{L})_n I_{Dn}}$$

7.18

The circuit of Fig. 7.42 is modified as depicted in Fig. 7.78.

(a) Calculate the input-referred thermal noise voltage.

(b) For a given bias current and output voltage swing, what value of R_S minimizes the input-referred thermal noise?

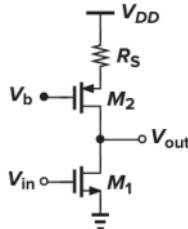


Figure 7.78

$$(a) \overline{V_{n,in}^2} = (4kT\gamma g_{m1} + 4kT\gamma g_{m2} \frac{1}{1+g_{m2}R_s})^2 + 4kT \frac{1}{R_s} \left(\frac{R_s}{R_s + \frac{1}{g_{m1}}} \right)^2 R_{out}^2$$

$$R_{out} = r_{o1} || [(1 + (g_{m2} + g_{mb2})r_{o2})R_s + r_{o2}]$$

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{|A_v|^2}$$

(b) R_S as large as possible.

7.19

A common-gate stage incorporates an NMOS device with $W/L = 50/0.5$ biased at $ID = 1 \text{ mA}$ and a load resistor of $1 \text{ k}\Omega$. Calculate the input-referred thermal noise voltage and current.

$$\overline{V_{n,in}^2} = 4kT[\gamma/g_{m1} + 1/(g_m^2 R_D)]$$

$$\overline{I_{n,in}^2} = 4kT/R_D$$

$$g_m = \sqrt{2I_D \mu_n C_{ox} \frac{W}{L}} = 16 \text{ mA/V}$$

$$\overline{V_{n,in}^2} = 7.5 \times 10^{-19} \text{ V}^2/\text{Hz}$$

$$\overline{I_{n,in}^2} = 16.56 \times 10^{-24} \text{ A}^2/\text{Hz}$$

7.20

The circuit of Fig. 7.48 is designed with $(W/L)_1 = 50/0.5$, $I_{D1} = I_{D2} = 0.5 \text{ mA}$, and $R_D = 1 \text{ k}\Omega$.

(a) Determine $(W/L)_2$ such that the contribution of M2 to the input-referred thermal noise current (not current squared) is one-fifth of that due to R_D .

(b) Now calculate the minimum value of V_b to place M2 at the edge of the triode region. What is the maximum allowable output voltage swing?

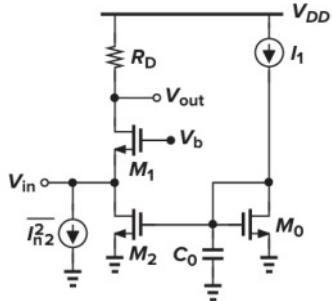


Figure 7.48 Noise contributed by bias-current source.

$$(a) \overline{I_{n,in}^2} = 4kT/R_D + 4kT\gamma g_{m2}$$

$$g_{m2} = \frac{1}{25\gamma R_D} = \sqrt{2I_D\mu_n C_{ox}(\frac{W}{L})_2}$$

$$(\frac{W}{L})_2 = 0.0268$$

$$(b) V_{ds} = V_{dsat}$$

$$g_{m2} = \frac{2I_D}{V_{dsat2}}$$

$$V_b = V_{dsat1} + V_{th} + V_{ds2}$$

$$V_{dsat1} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(\frac{W}{L})_1}}$$

$$V_{out,max} = V_{DD}$$

$$V_{out,min} = V_{dsat1} + V_{dsat2}$$

7.21

Design the circuit of Fig. 7.48 for an input-referred thermal noise voltage of $3nV/\sqrt{Hz}$ and maximum output swing. Assume that $I_{D1} = I_{D2} = 0.5mA$.

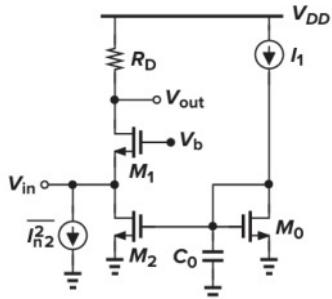


Figure 7.48 Noise contributed by bias-current source.

$$\overline{I_{n,out}^2} = 4kT/R_D + 4kT\gamma g_{m1}$$

$$G_m = g_{m1} + g_{mb} + \frac{1}{r_{o1}}$$

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{G_m^2}$$

7.22

Consider the circuit of Fig. 7.49. If $(W/L)_{1-3} = 50/0.5$ and $I_{D1-3} = 0.5mA$, determine the input-referred thermal noise voltage and current.

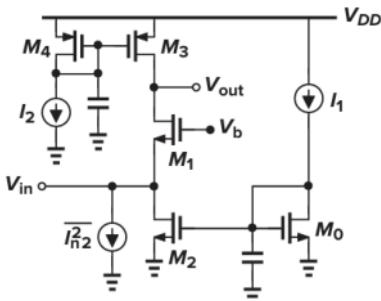


Figure 7.49

$$\overline{V_{n,in}^2} = 4kT\gamma(1/g_{m1} + g_{m3}/g_{m1}^2)$$

$$\begin{aligned}\overline{I_{n,in}^2} &= 4kT\gamma(g_{m2} + g_{m3}) \\ g_{m1} &= g_{m2} = \sqrt{2I_{D1,2}\mu_nC_{ox}(\frac{W}{L})_{1,2}} = 3.66mA/V \\ g_{m3} &= \sqrt{2I_{D3}\mu_pC_{ox}(\frac{W}{L})_3} = 1.96mA/V \\ \overline{V_{in}} &= 2.14nV/\sqrt{Hz} \\ \overline{I_{in}} &= 7.87pA/\sqrt{Hz}\end{aligned}$$

7.23

The circuit of Fig. 7.49 is designed with $(W/L)_1 = 50/0.5$ and $I_{D1-3} = 0.5mA$. If an output swing of 2 V is required, estimate by iteration the dimensions of M2 and M3 such that the input-referred thermal noise current is minimum.

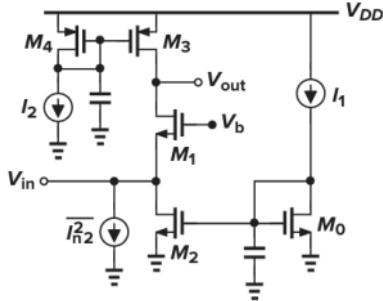


Figure 7.49

$$\begin{aligned}\overline{I_{n,in}^2} &= 4kT\gamma(g_{m2} + g_{m3}) \\ g_{m1} &= \sqrt{2I_{D1}\mu_nC_{ox}(\frac{W}{L})_1} = 3.66mA/V \\ V_{dsat} &= \frac{2I_{D1}}{g_{m1}} = 273.33mV \\ \text{Out Swing} &= V_{DD} - |V_{dsat3}| - V_{dsat1} - V_{dsat2} = 2V \\ |V_{dsat3}| - V_{dsat2} &= 0.73V \quad I_{n,in}^2 = 4kT\gamma(\frac{2I_{D2}}{V_{sat2}} + \frac{2I_{D3}}{V_{sat3}}) \\ \text{When } V_{dsat2} &= V_{dsat3} = \frac{0.73}{2} = 0.365V, \text{ the input-referred thermal noise current is minimum.} \\ (\frac{W}{L})_2 &= \frac{g_{m2}^2}{2I_{D2}\mu_nC_{ox}} = 56.4 \\ (\frac{W}{L})_3 &= 197.4\end{aligned}$$

7.24

The source follower of Fig. 7.51 is to provide an output resistance of 100 with a bias current of 0.1 mA. (a) Calculate $(W/L)_1$.

(b) Determine $(W/L)_2$ such that the input-referred thermal noise voltage (not voltage squared) contributed by M2 is one-fifth of that due to M1. What is the maximum output swing?

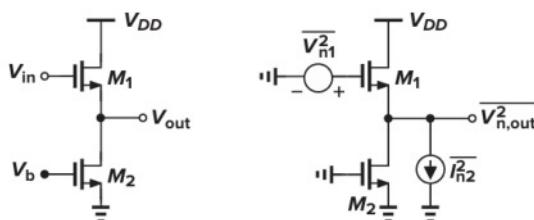


Figure 7.51 (a) Source follower; (b) circuit including noise sources.

$$(a) g_m = \frac{1}{R_{out}} = \sqrt{2\mu_nC_{ox}(\frac{W}{L})_1 I_D}$$

$$(\frac{W}{L})_1 = 3726$$

$$(b) \overline{V_{n,out}^2} = \overline{I_{n,out}^2} R_{out}^2$$

$$I_{m1,out}^2 = 4kT\gamma g_{m1} = 25 \times 4kT\gamma g_{m2}$$

$$(\frac{W}{L})_2 = 5.96$$

$$V_{o,max} = V_{DD} - V_{dsat1} = 2.98V$$

$$V_{o,min} = V_{dsat2} = 0.5V$$

7.25

The cascode stage of Fig. 7.52(a) exhibits a capacitance C_X from node X to ground. Neglecting other capacitances, determine the input-referred thermal noise voltage.

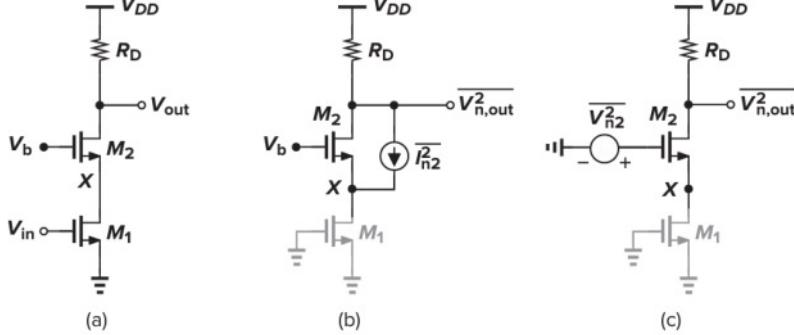


Figure 7.52 (a) Cascode stage; (b) noise of M_2 modeled by a current source; (c) noise of M_2 modeled by a voltage source.

$$\overline{V_{n,in1}^2} = 4kT\gamma \frac{1}{g_{m1}}$$

$$\overline{V_{n,in2}^2} = \frac{\overline{I_{n,in2}^2}}{G_m^2} = \frac{4kT\gamma g_{m2} \left(\frac{r_{o2}||\frac{1}{g_{m2}}}{r_{o2}||\frac{1}{g_{m2}} + r_{o1}||\frac{1}{sC_x}} \right)^2}{(g_{m1} \frac{r_{o1}||\frac{1}{sC_x}}{r_{o1}||\frac{1}{sC_x} + \frac{1}{g_{m2}}})^2}$$

$$\overline{V_{n,inD}^2} = 4kT \frac{1}{R_D} \frac{1}{G_m^2}$$

7.26

Determine the input-referred thermal and 1/f noise voltages of the circuits shown in Fig. 7.79 and compare the results. Assume that the circuits draw equal supply currents.

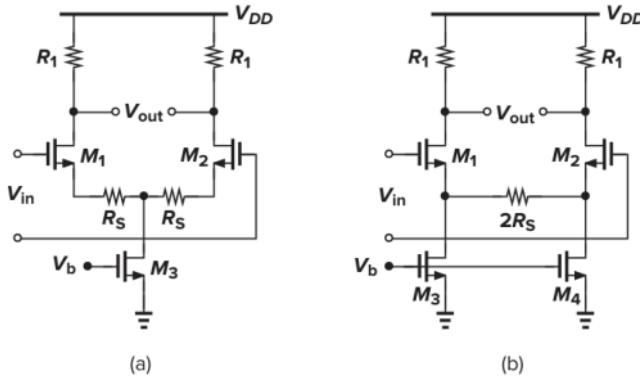


Figure 7.79

$$(a) G_m = \frac{1}{\frac{1}{g_{m1}} + R_S}$$

$$\overline{V_{n,in1}^2} = 4kT\gamma/g_{m1} + \frac{K_n}{C_{ox}(WL)_1 f} + 4kTR_S + 4kT/(R_1 G_m^2)$$

$$\overline{V_{n,in}^2} = 2\overline{V_{n,in1}^2}$$

$$(b) \overline{I_{n,out,m3}^2} = \overline{I_{n,m3}^2} \left(\frac{R_S}{R_S + \frac{1}{g_{m1}}} \right)$$

$$G_m = \frac{1}{\frac{1}{g_{m1}} + R_S}$$

$$\overline{V_{n,in1}^2} = 4kT\gamma/g_{m1} + \frac{K_n}{C_{ox}(WL)_1 f} + 4kTR_S + 4kT/(R_1 G_m^2) + \overline{I_{n,out,m3}^2}/G_m^2$$

$$\overline{V_{n,in}^2} = 2\overline{V_{n,in1}^2}$$

7.27

Repeat the analysis in Example 7.13 but assume that $\lambda > 0$.

Determine the input-referred noise voltage and current for the amplifier shown in Fig. 7.38(a). Assume that I_1 is noiseless and $\lambda = 0$.

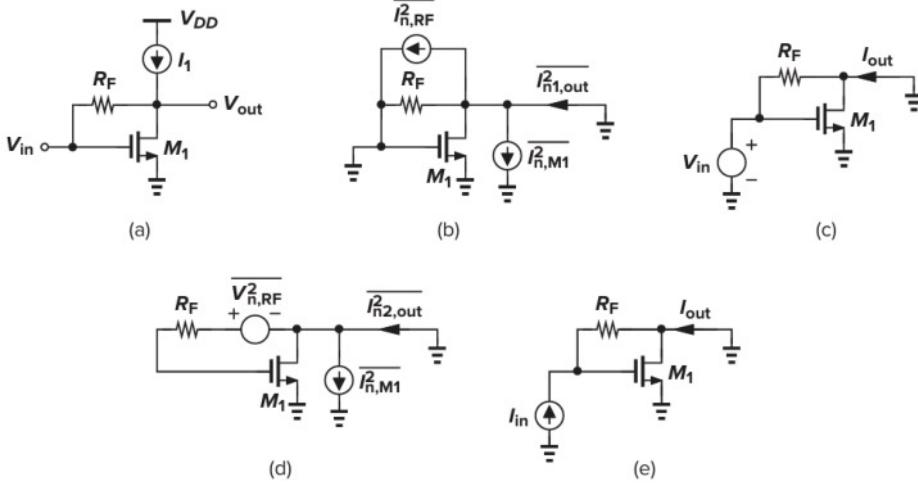


Figure 7.38

$$\overline{V_{n,out}^2} = (4kT/R_F + 4kT\gamma g_m)(r_o || R_F)^2$$

Using small signal diagram to find Gain.

$$A_v = \frac{r_{o1}(1-g_m R_F)}{R_F+r_{o1}}$$

$$\overline{V_{n,in}^2} = \frac{4kT/R_F + 4kT\gamma g_m}{(g_m - \frac{1}{R_F})^2}$$

$$\overline{V_{n,out}^2} = \frac{4kT\gamma g_m r_{o1}^2 + 4kT R_F (g_m r_{o1})^2}{(1+g_m r_{o1})^2}$$

$$\overline{I_{n,in}^2} = \frac{4kT R_F g_m^2 + 4kT\gamma g_m}{(1-g_m R_F)^2}$$

7.28

Suppose the circuit of Fig. 7.38(a) is driven by a finite source impedance, as shown in Fig. 7.80. Assume that $\lambda = 0$, and neglect the noise of R_S .

(a) Determine the output noise voltage of the circuit.

(b) In a manner similar to the analysis of Fig. 7.37, compute in terms of $V_{n,RF}$ and $V_{n,M1}$ the input-referred noise voltage and current, paying close attention to their correlation.

(c) Using superposition of voltages and currents (not powers), calculate the output noise voltage in terms of $V_{n,in}$ and $I_{n,in}$, as obtained in (b). Now make the substitution $\overline{V_{n,RF}^2} = 4kTR_F$ and $\overline{I_{n,M1}^2} = 4kT\gamma g_m$. Is this result the same as that derived in (a)?

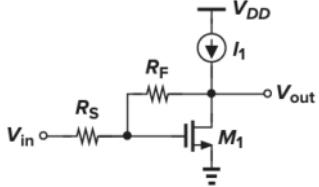


Figure 7.80

$$(a) \overline{I_{n,out}^2} = 4kTR_F \left[\frac{1}{R_s+R_F} + \frac{R_s}{R_s+R_F} g_m \right]^2$$

$$\overline{I_{n,out1}^2} = 4kT\gamma g_m$$

$$R_{out} = (R_s + R_F) \left| \frac{1}{\frac{R_s}{R_s+R_F} g_m} \right|$$

$$\overline{V_{n,out}^2} = (\overline{I_{n,out}^2} + \overline{I_{n,out1}^2}) R_{out}^2$$

$$(b) I_{n,out} = V_{n,RF} \left(\frac{1}{R_s+R_F} + \frac{R_s}{R_s+R_F} \times g_m \right) + V_{n,M1} g_m$$

$$G_m = \frac{1}{R_s+R_F} - \frac{R_F}{R_s+R_F} g_m$$

$$V_{n,in} = \frac{I_{n,out}}{G_m}$$

$$I_{n,out} = V_{n,RF} g_m + V_{n,M1} g_m$$

$$A_v = 1 - R_F g_m$$

$$I_{n,in} = \frac{I_{n,out2}}{A_v}$$

$$(c) V_{n,out} = V_{n,in} G_m R_{out} + I_{n,in} A_v \frac{1}{g_m} = I_{n,out1} R_{out} + I_{n,out2} R_{out} = 2V_{n,RF} + (1 + \frac{R_F + R_S}{1 + g_m R_s} g_m) V_{n,M1}$$

7.29

Consider the circuits in Figs. 7.39(c) and (d), but include CGS and a noiseless impedance Z_1 in series with the gate. Derive expressions for $I_{n,out1}$ and $I_{n,out2}$. Does the lemma hold in this case?

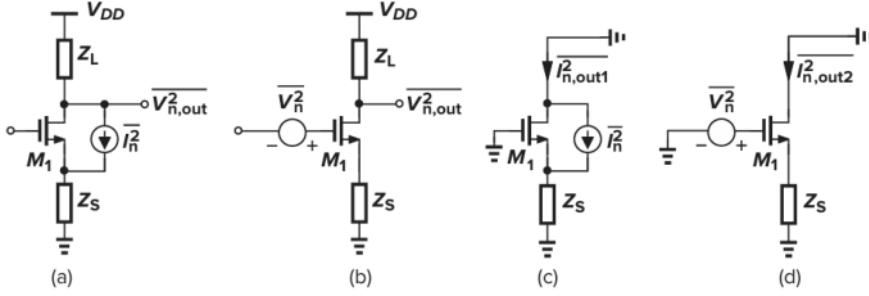


Figure 7.39 Equivalent CS stages.

$$(c) V_g = V_s \frac{Z_1}{Z_1 + \frac{1}{sC_p}}$$

$$g_m(V_g - V_s) + I_n = V_s \left(\frac{1}{Z_s} + \frac{1}{Z_1 + \frac{1}{sC_{gs}}} \right)$$

$$\overline{I_{n,out}^2} = |1 - \frac{g_m}{g_m + sC_{gs} + \frac{1+sC_{gs}Z_1}{Z_s}}|^2 \overline{I_n^2}$$

$$(d) \frac{V_g - V_n}{Z_1} + \frac{V_g - V_s}{\frac{1}{sC_{gs}}} = 0$$

$$(V_g - V_s)(g_m + sC_{gs}) = \frac{V_s}{Z_s}$$

$$\overline{I_{n,out2}^2} = | \frac{g_m}{1 + sC_{gs}Z_1 + Z_s(g_m + sC_{gs})} | \overline{V_n^2}$$

7.30

Repeat Example 7.14 while including C_{GS} and an impedance Z_1 in series with the gate. Does the lemma hold in this case?

Lemma The circuits shown in Fig. 7.39(a) and (b) are equivalent at low frequencies if $\overline{V_n^2} = \overline{I_n^2}/g_m^2$ and the circuits are driven by a finite impedance.

No, V_n will affect the current in C_{gs} .

7.31

Model the thermal noise of M1 in Fig. 7.49 by a voltage source in series with its gate and assuming the input is open,

(a) Determine the resulting output voltage. (The voltage gain for a degenerated CS stage was derived in Chapter 3.)

(b) Now refer this voltage to the input as a current and compare the result with the contributions of M2 and M3.

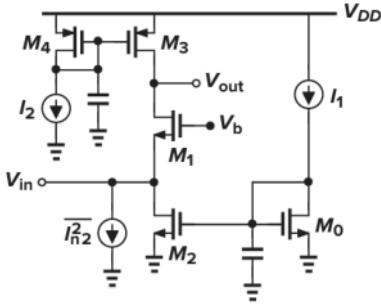


Figure 7.49

$$(a) \overline{V_{n,out}^2} = [4kTg_{m3} + 4kT\gamma g_{m2}(\frac{r_{o2}}{r_{o2} + \frac{1}{g_{m1}} || r_{o1}})^2 + 4kT\gamma \frac{1}{g_{m1}} (\frac{g_{m1}}{1+g_{m1}r_{o2}+\frac{r_{o2}}{r_{o1}}})^2][r_{o3}||(1+g_{m1}r_{o1})r_{o2}]^2$$

$$(b) G_m = \frac{r_{o2}r_{o1}}{r_{o2} + \frac{1}{1+g_{m1}r_{o1}}}$$

$$\overline{I_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{G_m^2}$$

7.32

Figure 7.81 shows a noiseless amplifier driven by a source resistance of R_S . If the amplifier can be modeled by a low-frequency gain of A_0 and a single pole at w_0 , determine the total integrated noise at the output due to R_S .



Figure 7.81

$$\overline{V_{n,out}^2} = 4kTR_s \left| \frac{A_0}{1+j\frac{w}{w_0}} \right|^2$$

$$\int_0^\infty \overline{V_{n,out}^2} dw = 2\pi kT R_s A_0^2 w_0$$

7.33

Considering only thermal noise in Fig. 7.82, determine the output noise spectrum and the total integrated noise. Assume that $\lambda > 0$.

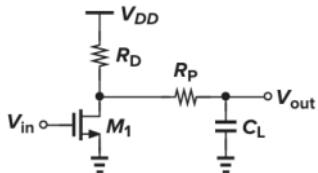


Figure 7.82

$$\overline{V_{n,out}^2} = 4kT[(\gamma g_{m1} + \frac{1}{R_D})(r_o || R_D)^2 + R_p] \left(\frac{\frac{1}{jwC_L}}{\frac{1}{jwC_L} + R_p + r_o || R_D} \right)^2$$

$$\int \overline{V_{n,out}^2} = \frac{2\pi kT[(\gamma g_{m1} + \frac{1}{R_D})(r_o || R_D)^2 + R_p]}{(r_o || R_D + R_p) C_L}$$

7.34

Calculate the input-referred thermal and flicker noise of the circuit shown in Fig. 7.83, where the output of interest is $I_{D3} - I_{D4}$. Consider two cases: (a) the current sources are ideal, and (b) the current sources are realized by MOSFETs. Neglect channel-length modulation and body effect.

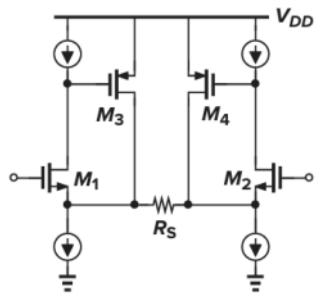


Figure 7.83

$$(a) \overline{I_{n,out}^2} = 2\left(\frac{4kT}{R_s/2} + 4kT\gamma g_{m3,4} + \frac{K}{C_{ox}WL_{3,4}} \frac{g_{m3,4}^2}{f}\right) A = \frac{2}{R_s}$$

$$\overline{V_{n,in}^2} = \frac{\overline{I_{n,out}^2}}{A^2} + 2\left(\frac{4kT\gamma}{g_{m1,2}} + \frac{K}{C_{ox}WL_{1,2}} \frac{1}{f}\right)$$

$$(b) \overline{I_{n,out}^2} = \overline{I_{n,outa}^2} + 2(4kT\gamma g_{m,biasn} + \frac{K}{C_{ox}WL_{biasn}} \frac{g_{m,biasn}^2}{f})$$

8 Feedback

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

8.1

Consider the circuit of Fig. 8.3(b), assuming that I_1 is ideal and gm_1r_{O1} cannot exceed 50. If a gain error of less than 5% is required, what is the maximum closed-loop voltage gain that can be achieved by this topology? What is the low-frequency closed-loop output impedance under this condition?

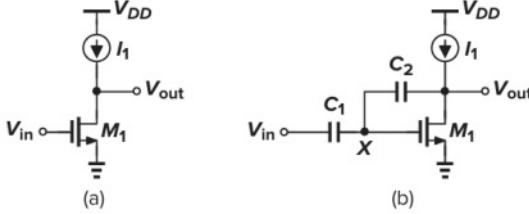


Figure 8.3 (a) Simple common-source stage; (b) circuit of (a) with feedback.

$$A_v = \frac{|A|}{1+|A|F} \geq 0.95 \frac{1}{F}$$

$$F \geq \frac{19}{|A|} \geq \frac{19}{50}$$

$$|A| = |g_m r_{out}| \leq 50$$

$$|A_{v,max}| = \frac{1}{F_{min}} \times 0.95 = 2.5$$

$$r_{out} = \frac{r_{o1}}{1+|A|F} = 0.05r_{o1}$$

8.2

In the circuit of Fig. 8.8(a), assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 100/0.5$, $R_D = 2k\Omega$, and $C_2 = C_1$. Neglecting channel-length modulation and body effect, determine the bias current of M_1 and M_2 such that the input resistance at low frequencies is equal to 50Ω .

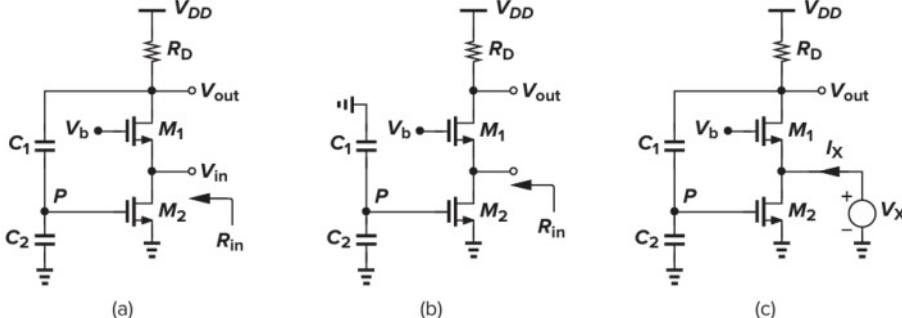


Figure 8.8 (a) Common-gate circuit with feedback; (b) open-loop circuit; (c) calculation of input resistance.

$$r_{in,open} = \frac{1}{g_{m1}}$$

$$r_{in} = \frac{r_{in,open}}{1+g_{m2}R_D \frac{C_1}{C_1+C_2}} = 50\Omega$$

$$g_{m2} = \sqrt{2}g_{m1}$$

$$g_{m1} = 3.42mS = \sqrt{2\mu_n C_{ox} (\frac{W}{L})_1 I_D}$$

$$I_D = 435mA$$

8.3

Calculate the output impedance of the circuit shown in Fig. 8.9(a) at relatively low frequencies if R_D is replaced by an ideal current source.

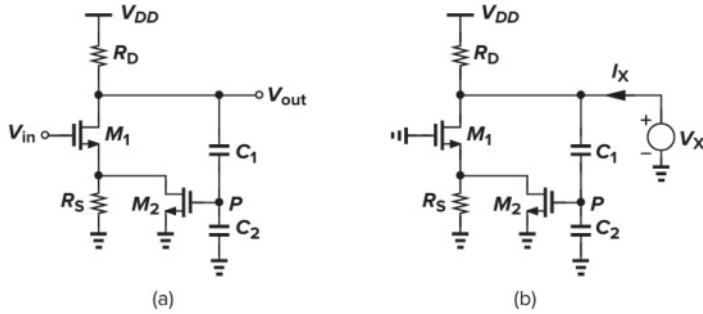


Figure 8.9 (a) CS stage with feedback; (b) calculation of output resistance.

$$Z_{out} = \frac{(1+g_{m1}r_{o1})(R_s||r_{o2})}{1 + \frac{C_1}{C_1+C_2} g_{m2}(r_{o2}||R_s||\frac{1}{g_{m1}+g_{mb1}})(g_{m1}+g_{mb1})r_{o1}}$$

8.4

Consider the example illustrated in Fig. 8.11. Suppose an overall voltage gain of 500 is required with maximum bandwidth. How many stages with what gain per stage must be placed in a cascade? (Hint: first find the 3-dB bandwidth of a cascade of n identical stages in terms of that of each stage.)

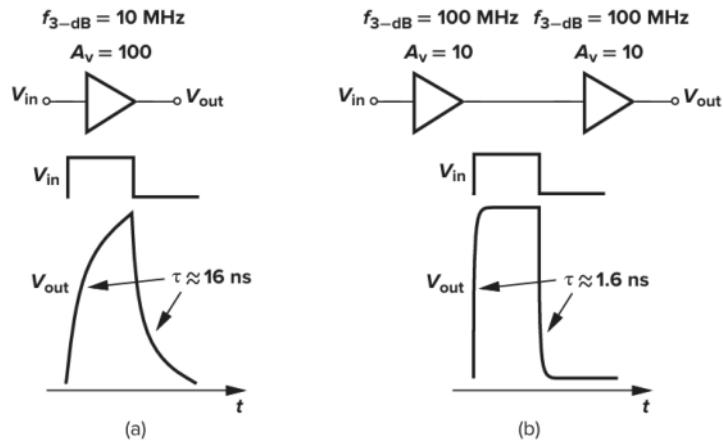


Figure 8.11 Amplification of a 20-MHz square wave by (a) a 10-MHz amplifier and (b) a cascade of two 100-MHz feedback amplifiers.

Suppose $H(f) = \left(\frac{A}{1+j\frac{f}{f_p}}\right)^n$

$$|H^n(f_n)| = \frac{A^n}{(1+\frac{f^2}{f_p^2})^{\frac{n}{2}}}$$

$$A^n = 500\sqrt{2}$$

$$(1 + \frac{f^2}{f_p^2})^{\frac{n}{2}} = \sqrt{2}$$

8.5

If in Fig. 8.22(b), amplifier \$A_0\$ exhibits an output impedance of \$R_0\$, calculate the closed-loop voltage gain and output impedance, taking into account loading effects.

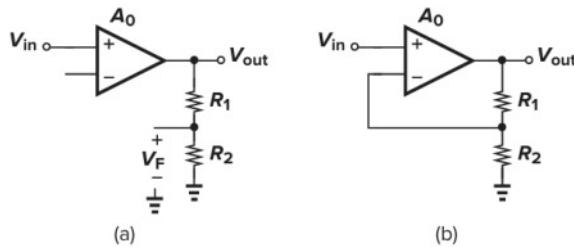


Figure 8.22 (a) Amplifier with output sensed by a resistive divider; (b) voltage-voltage feedback amplifier.

$$A = A_0 \frac{R_1 + R_2}{R_0 + R_1 + R_2}$$

$$F = \frac{R_2}{R_1 + R_2}$$

$$r_{open} = (R_1 + R_2) \parallel R_0$$

$$A_v = \frac{A}{1+AF}$$

$$r_o = \frac{r_{o,open}}{1+AF}$$

8.6

Consider the circuit of Fig. 8.25(a), assuming that $(W/L)_{1,2} = 50/0.5$ and $(W/L)_{3,4} = 100/0.5$. If $ISS = 1 \text{ mA}$, what is the maximum closed-loop voltage gain that can be achieved if the gain error is to remain below 5%?

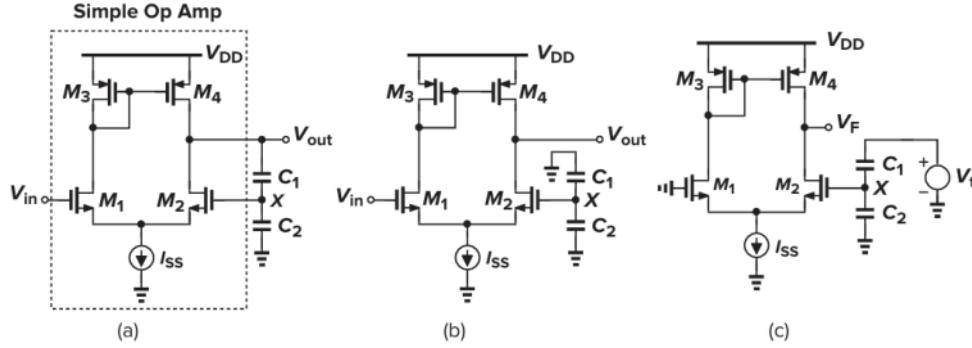


Figure 8.25

$$\frac{A}{1+AF} \geq 0.95/F$$

$$F \geq \frac{19}{A}$$

$$A = g_{m1}(r_{o2} \parallel r_{o4}) = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_1 I_D \frac{1}{(\lambda_n + \lambda_p) I_D}} = 24.4$$

$$A_{v,max} = 0.95 \frac{1}{F_{min}} = \frac{A}{20} = 1.22$$

8.7

The circuit of Fig. 8.42 can operate as a transimpedance amplifier if I_{out} flows through a resistor, R_{D2} , connected to V_{DD} , producing an output voltage. Replacing R_S with an ideal current source and assuming that $\lambda = \gamma = 0$, calculate the transimpedance of the resulting circuit. Also, calculate the input-referred noise current per unit bandwidth.

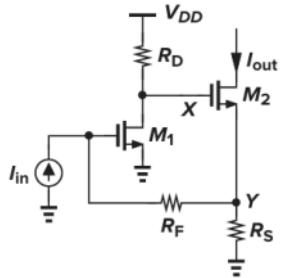


Figure 8.42

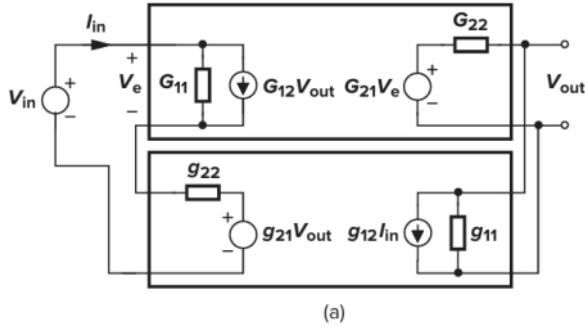
$$\frac{V_{out}}{I_{in}} = R_{D2}$$

$$\frac{I_{n,out}^2}{I_{n,in}^2} = 4kT/R_{D2}$$

$$I_{n,in}^2 = 4kT/R_D$$

8.8

For the circuit of Fig. 8.51(a), calculate the closed-loop gain without neglecting $g_{12}I_{in}$. Prove that this term can be neglected if $g_{12} \ll A_0 Z_{in}/Z_{out}$.



(a)

$$V_{in} = I_{in}(Z_{in} + g_{21}) + g_{21}V_{out}$$

$$\frac{V_{out}}{Z_{out}} - A_o V_e + \frac{V_{out}}{g_{11}} + g_{12}I_{in} = 0$$

$$V_e = I_{in}Z_{in}$$

We can solve to get $I_{in}\left(\frac{A_o Z_{in}}{Z_{out}} - g_{12}\right) = \left(\frac{1}{Z_{out}} + \frac{1}{g_{11}}\right)V_{out}$

8.9

Calculate the loop gain of the circuit in Fig. 8.54 by breaking the loop at node X. Why is this result somewhat different from $G_{21}A_{v,open}$?

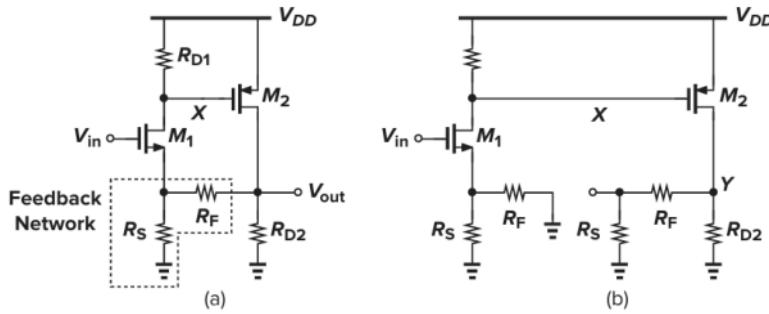


Figure 8.54

$$A_v = g_{m2} \frac{R_{D2}}{R_{D2} + R_F + (R_s \parallel \frac{1}{g_m})} \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_s} R_s g_{m1} R_{D1}$$

8.10

Using feedback techniques, calculate the input and output impedance and voltage gain of each circuit in Fig. 8.95.

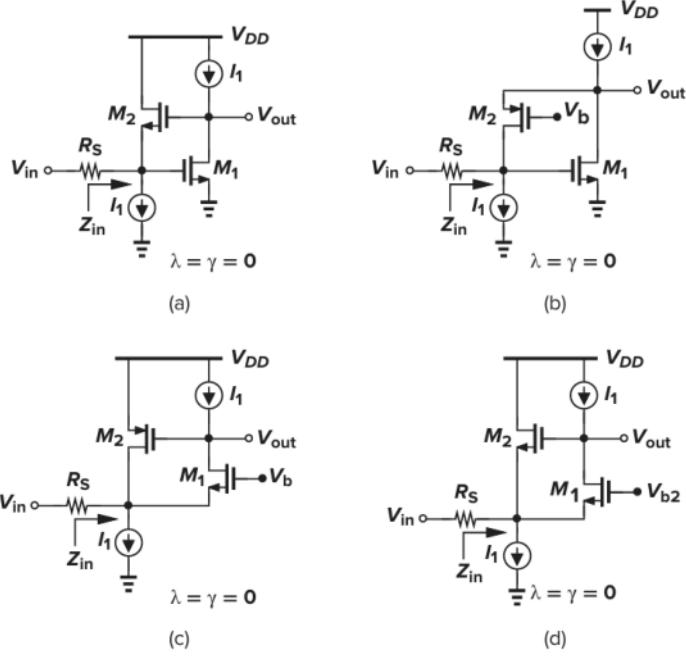


Figure 8.95

$$(a) F = -g_{m2}$$

$$A = -(R_S \parallel \frac{1}{g_{m2}}) g_{m1} r_{o1}$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF}/R_S = \frac{1}{g_{m2} R_S}$$

$$Z_{in} = \frac{\frac{1}{g_{m2}}}{1+g_{m2}g_{m1}r_{o1}(R_S \parallel \frac{1}{g_{m2}})} \quad Z_{out} = \frac{r_{o1}}{1+AF} = \frac{R_S + \frac{1}{g_{m2}}}{g_m R_S}$$

$$(b) F = -g_{m2}$$

$$A = -R_S g_{m1} \frac{1}{g_{m2}}$$

$$\frac{V_{out}}{V_{in}} = (\frac{A}{1+AF})/R_S$$

$$Z_{in} = \infty \quad Z_{out} = \frac{1/g_{m2}}{1+AF}$$

$$(c) F = g_{m2}$$

$$A = (R_s \parallel \frac{1}{g_{m2}}) g_{m1} r_{o1}$$

$$\frac{V_{out}}{V_{in}} = (\frac{A}{1+AF})/R_S = \frac{1}{g_{m2} R_S}$$

$$Z_{in} = \frac{\frac{1}{g_{m1}}}{1+AF} = 0$$

$$Z_{out} = \frac{(1+g_{m1}r_{o1})R_S}{1+AF}$$

$$(d) F = g_{m2}$$

$$A = (R_S \parallel \frac{1}{g_{m2}} \parallel \frac{1}{g_{m1}}) g_{m1} r_{o1}$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF}/R_S = \frac{1}{g_{m2} R_S}$$

$$Z_{in} = \frac{\frac{1}{g_{m1}} \parallel \frac{1}{g_{m2}}}{1+AF}$$

$$Z_{out} = \frac{(1+g_{m1}r_{o1})R_S}{1+AF} = \frac{R_S}{g_{m2}(R_S \parallel \frac{1}{g_{m1}} \parallel \frac{1}{g_{m2}})}$$

8.11

Using feedback techniques, calculate the input and output impedances of each circuit in Fig. 8.96.

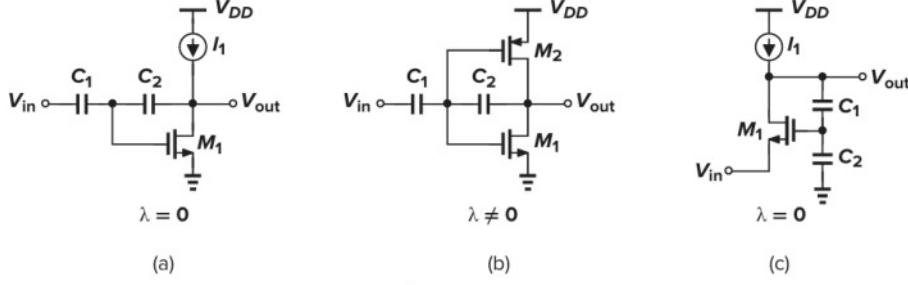


Figure 8.96

$$(a) Z_{in} = \frac{1}{sC_1} + \frac{1}{g_{m1}} \\ Z_{out} = \left(\frac{1}{sC_1} + \frac{1}{sC_2} \right) \parallel \frac{1}{g_{m1} \frac{1}{C_1 + C_2}}$$

$$(b) Z_{in} = \frac{1}{sC_1} + \frac{r_o + \frac{1}{sC_2}}{1 + g_m r_o} \\ Z_{out} = \left(\frac{1}{sC_1} + \frac{1}{sC_2} \right) \parallel \frac{1}{g_{m1} \frac{1}{C_1 + C_2}} \parallel (r_{o1} \parallel r_{o2})$$

$$(c) (I_{in} \frac{1}{sC_2} - V_{in}) g_m = -I_{in} \\ Z_{in} = \frac{g_{m1} + sC_2}{g_{m1} sC_2} \\ Z_{out} = \left(\frac{1}{sC_1} + \frac{1}{sC_2} \right) \parallel \frac{1}{g_{m1} \frac{1}{C_1 + C_2}}$$

8.12

Consider the circuit of Fig. 8.54(a), assuming that $(W/L)_1 = (W/L)_2 = 50/0.5, \lambda = \gamma = 0$, and each resistor is equal to $2\text{k}\Omega$. If $I_{D2} = 1\text{mA}$, what is the bias current of M1? What value of V_{in} gives such a current? Calculate the overall voltage gain.

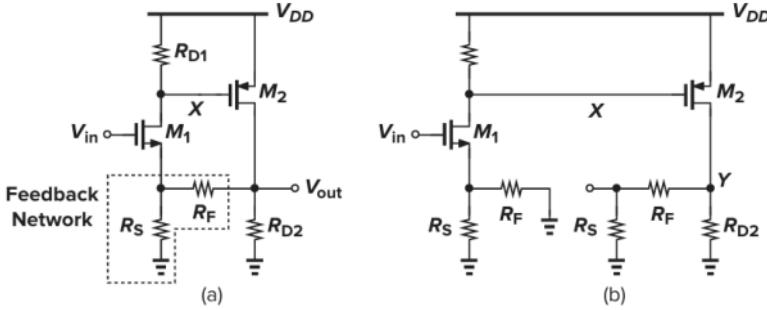


Figure 8.54

$$I_{D2} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_2 (V_x - V_{DD} - V_{thp})^2$$

$$V_x = 1.48V$$

$$I_{D1} = \frac{V_{DD} - V_x}{R_{D1}} = 0.76mA$$

$$V_s = R_s (I_{D1} \frac{2}{3} + I_{D2} \frac{1}{3}) = 1.68V$$

$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{in} - V_s - V_{thn})^2$$

$$V_{in} = 2.72V$$

$$g_{m1} = \frac{2I_{D1}}{V_{in} - V_s - V_{thn}} = 4.52mS$$

$$g_{m2} = 2.77mS$$

$$F = -0.5$$

$$A = \frac{g_{m1} R_{D1}}{1 + g_{m1} (R_s \parallel R_F)} (-g_{m2}) [R_{D2} \parallel (R_F + R_s)] = -6.05$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1 + AF} = -1.5$$

8.13

Suppose the amplifier of the circuit shown in Fig. 8.22 has an open-loop transfer function $A_0/(1 + s/w_0)$ and an output resistance R_0 . Calculate the output impedance of the closed-loop circuit and plot the

magnitude as a function of frequency. Explain the behavior.

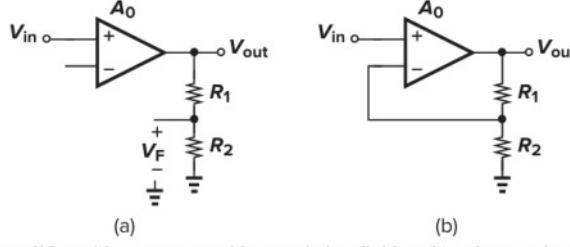


Figure 8.22 (a) Amplifier with output sensed by a resistive divider; (b) voltage-voltage feedback amplifier.

$$BA = \frac{A}{1 + \frac{s}{w_0}} \frac{R_2}{R_0 + R_1 + R_2}$$

$$r_o = \frac{R_0 || (R_1 + R_2)}{1 + BA} = R_0 || (R_1 + R_2) \frac{1 + \frac{s}{w_0}}{1 + \frac{s}{w_0} + \frac{A_0 R_2}{R_0 + R_1 + R_2}}$$

8.14

Calculate the input-referred noise voltage of the circuit shown in Fig. 8.25(a) at relatively low frequencies.

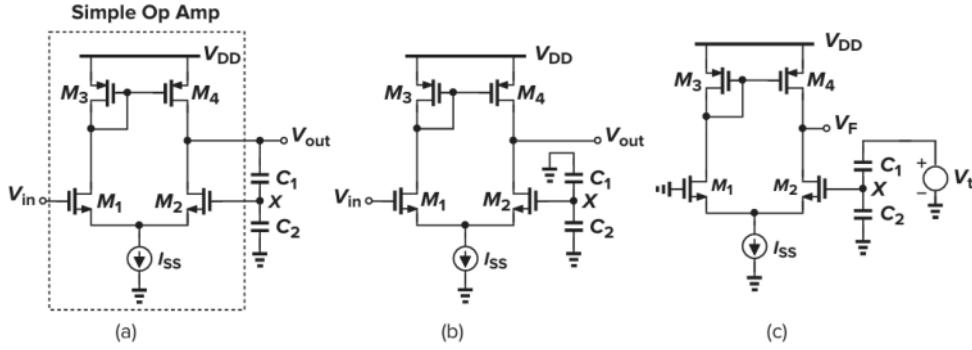


Figure 8.25

$$\overline{V_{n,in}^2} = 2 \times 4kT\gamma(g_{m1} + g_{m3})/g_{m1}^2$$

8.15

A differential pair with current-source loads can be represented as in Fig. 8.97(a), where $R_0 = r_{ON}||r_{OP}$ and r_{ON} and r_{OP} denote the output resistance of NMOS and PMOS devices, respectively. Consider the circuit shown in Fig. 8.97(b), where G_{m1} and G_{m2} are placed in a negative feedback loop.

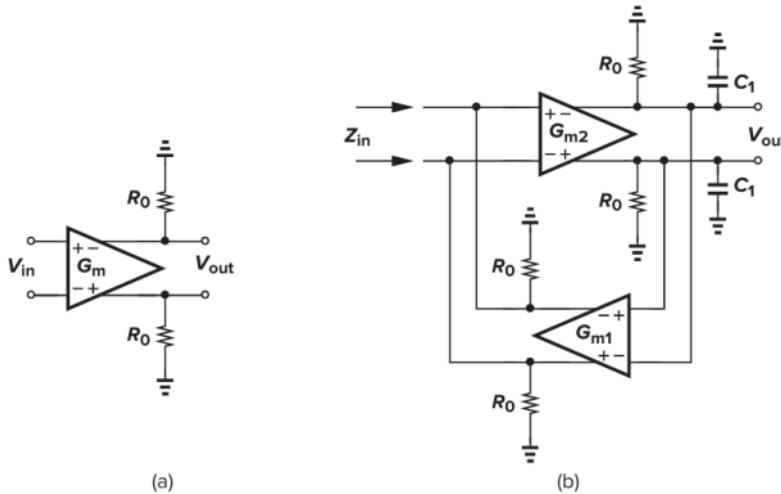


Figure 8.97

- (a) Neglecting all other capacitances, derive an expression for Z_{in} . Sketch $|Z_{in}|$ versus frequency.
- (b) Explain intuitively the behavior observed in part (a).

(c) Calculate the input-referred thermal noise voltage and current in terms of the input-referred noise voltage of each Gm stage.

$$(a) Z_{in} = \frac{2R_0}{1 + G_{m2} \frac{\frac{1}{2R_0} + jw \frac{C_1}{2}}{\frac{1}{2R_0} + jw \frac{C_1}{2}}} G_{m1} 2R_0 = \frac{1 + jw R_0 C_1}{\frac{1}{2R_0} + jw \frac{C_1}{2} + G_{m1} G_{m2} 2R_0}$$

(b) When the frequency is very high, there is no feedback and $Z_{in} = 2R_0$.

$$(c) V_{out} = [[I_{in} - G_{m1}(V_{out} + V_{n1})]2R_0 + V_{n2}]G_{m2}Z_{out}$$

$$I_{n,in}^2 = V_{n1}^2 G_{m1}^2 + V_{n2}^2 \frac{1}{4R_D^2}$$

$$V_{n,in}^2 = I_{n,in}^2 Z_{in}^2$$

8.16

In the circuit of Fig. 8.98, $(W/L)_{1-3} = 50/0.5$, $I_{D1} = |I_{D2}| = |I_{D3}| = 0.5mA$, and $R_{S1} = R_F = R_{D2} = 3k\Omega$.

(a) Determine the input bias voltage required to establish the above currents.

(b) Calculate the closed-loop voltage gain and output resistance.

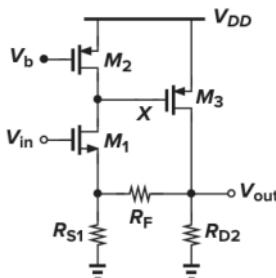


Figure 8.98

$$(a) V_{s1} = R_{s1}(I_{d1}\frac{2}{3} + |I_{d3}|\frac{1}{3}) = 1.5V$$

$$I_{d1} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1(V_{in} - V_{s1} - V_{thn})^2$$

$$V_{in} = 2.47V$$

$$(b) A = \frac{-g_{m1}}{1 + g_{m1}(R_{s1}||R_F) + \frac{R_{s1}||R_F}{r_{o1}}} [r_{o2}||(1 + g_{m1}r_{o1})(R_{s1}||R_F)] \times (-g_{m3})[r_{o3}||R_{D2}||(R_F + R_{s1})]$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_1} I_{d1} = 3.66mS$$

$$g_{m2} = g_{m3} = 1.96mS$$

$$r_{o1} = \frac{1}{\lambda I_{d1}} = 20k\Omega$$

$$r_{o2} = r_{o3} = 10k\Omega$$

$$A = 18.4$$

$$F = \frac{R_{s1}}{R_{s1}+R_F} = 0.5$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF} = 1.8$$

$$R_{o,open} = 1.67k\Omega$$

$$R_{o,close} = 164\Omega$$

8.17

The circuit of Fig. 8.98 can be modified as shown in Fig. 8.99, where a source follower, M4, is inserted in the feedback loop. Note that M1 and M4 can also be viewed as a differential pair. Assume that $(W/L)_{1-4} = 50/0.5$, $I_D = 0.5mA$, for all transistors $R_{S1} = R_F = R_{D2} = 3k\Omega$, and $V_{b2} = 1.5V$. Calculate the closed-loop voltage gain and output resistance, and compare the results with those obtained in the previous problem.

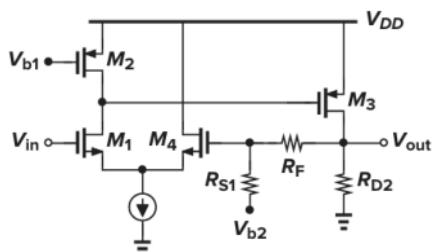


Figure 8.99

$$F = 0.5$$

$$A_1 = \frac{-g_{m1}}{1+g_{m1}\frac{1}{g_{m4}} + \frac{1}{r_{o1}}} [r_{o1}||(1+g_{m1}r_{o1})\frac{1}{g_{m4}}] = -\frac{1}{2}g_{m1}(r_{o1}||r_{o2})$$

$$A = -\frac{1}{2}g_{m1}(r_{o1}||r_{o2})(-g_{m3})[r_{o3}||R_{D2}||(R_F + R_{s1})] = 39.84$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF} = 1.9$$

$$R_{o,open} = 1.67k\Omega$$

$$R_{o,close} = 79.8\Omega$$

8.18

Consider the circuit of Fig. 8.100, where $(W/L)_{1-4} = 50/0.5$, $|I_{D1-4}| = 0.5mA$, and $R_2 = 3k\Omega$.

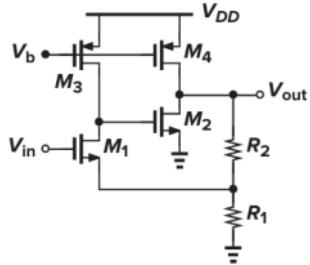


Figure 8.100

(a) For what range of R_1 are the above currents established while M_2 remains in saturation? What is the corresponding range of V_{in} ?

(b) Calculate the closed-loop gain and output impedance for R_1 in the middle of the range obtained in part(a).

$$(a) I_{d3} = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L}_3)(V_b - V_{DD} - V_{thp})^2 = 0.5mA$$

$$V_b = 1.689V$$

$$I_{d1} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L}_3)(V_{gsn} - V_{thn})^2 = 0.5mA$$

$$V_{gsn} = 0.973V$$

$$V_{gsn} - V_{thn} < V_{out} = I_D R_1 < V_b + V_{thp}$$

$$0.546k\Omega < R_1 < 4.978k\Omega \quad V_{in} = I_D R_1 + V_{gsn} < V_{gsn} + V_{thn}$$

$$R_1 < 1.4k\Omega$$

$$0.973V < V_{in} < 1.673V$$

$$(b) R_1 = 0.982k\Omega$$

$$F = \frac{R_1}{R_1 + R_2} = 0.247$$

$$A = \frac{-g_{m1}}{1+g_{m1}(R_1||R_2)+\frac{1}{r_{o1}}} [r_{o3}||(1+g_{m1}r_{o1})(R_1||R_2)] - g_{m2}[r_{o2}||r_{o4}||(R_1 + R_2)] = 76.2$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF} = 3.84$$

$$R_{out} = 125.8\Omega$$

8.19

In the circuit of Fig. 8.101, suppose all resistors are equal to $2k\Omega$ and $g_{m1} = g_{m2} = 1/(200\Omega)$. Assuming that $\lambda = \gamma = 0$, calculate the closed-loop gain and output impedance.

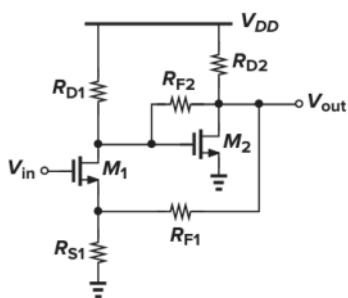


Figure 8.101

$$F_1 = 0.5$$

$$A = \frac{-g_{m1}}{1+g_{m1}(R_{S1}||R_{F1})} (R_{D1}||R_{in2}) A_{2,closed}$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF_1}$$

$$R_{out} = \frac{R_{out2,closed}}{1+AF_1}$$

$$F_2 = -\frac{1}{R_{F2}}$$

$$A_2 = -R_{F2}g_{m2}[R_{D2}||(R_{F1} + R_{S1})||(R_{F2} + R_{D1})] = -10k\Omega$$

$$R_{in2} = \frac{R_{F2}}{1+AF_2} = 0.333k\Omega$$

$$R_{out2,closed} = 0.167k\Omega$$

$$A_{2,closed} = \frac{A_2}{1+A_2F_2}/R_{in} = -5$$

8.20

A CMOS inverter can be used as an amplifier with or without feedback (Fig. 8.102). Assume that $(W/L)_{1,2} = 50/0.5$, $R_1 = 1k\Omega$, $R_2 = 10k\Omega$, and the dc levels of V_{in} and V_{out} are equal.

(a) Calculate the voltage gain and the output impedance of each circuit.

(b) Calculate the sensitivity of each circuit's output with respect to the supply voltage. That is, calculate the small-signal "gain" from V_{DD} to V_{out} . Which circuit exhibits less sensitivity?

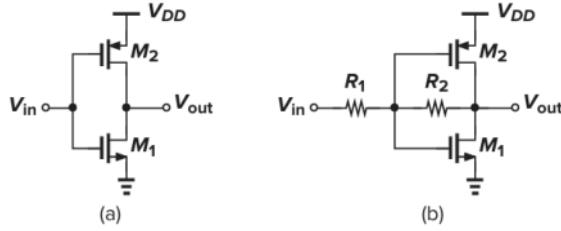


Figure 8.102

$$(a) F = -\frac{1}{R_2}$$

$$A = -(R_1||R_2)(g_{m1} + g_{m2})[r_{o1}||r_{o2}||(R_2 + R_1)]$$

$$\frac{V_{out}}{V_{in}} = \left(\frac{A}{1+AF}\right)/R_1 = -g_m \frac{\frac{r_o R_2}{r_o + R_1 + R_2}}{1 + g_m \frac{r_o R_1}{r_o R_1 + R_2}}$$

$$Z_{out} = \frac{r_o || (R_1 + R_2)}{1 + AF}$$

$$(b) \frac{\delta V_{out}}{\delta V_{DD}} = g_{m2} Z_{out}$$

8.21

Calculate the input-referred thermal noise voltage of the circuits shown in Fig. 8.102.

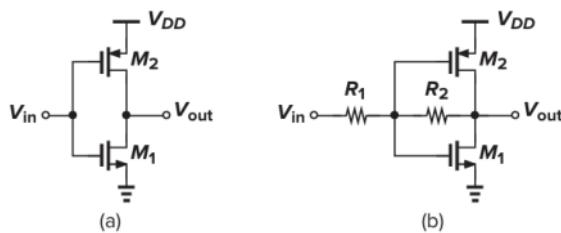


Figure 8.102

$$F = -\frac{1}{R_2}$$

$$A = -R_2 g_m (r_o || R_2)$$

$$g_m = g_{m1} + g_{m2}$$

$$r_o = r_{o1} || r_{o2}$$

$$\frac{V_{out}}{V_{in}} = \frac{\frac{A}{1+AF}}{\frac{R_2}{1+AF}} = -g_m (r_o || R_2)$$

$$\overline{V_n^2} = 4kT R_1 + \frac{(4kT\gamma g_m + 4kT \frac{1}{R_2}) R_{out}^2}{A_v^2}$$

8.22

The circuit shown in Fig. 8.103 employs positive feedback to produce a negative input capacitance. Using feedback analysis techniques, determine Z_{in} and identify the negative capacitance component.

Assume that $\lambda = \gamma = 0$.

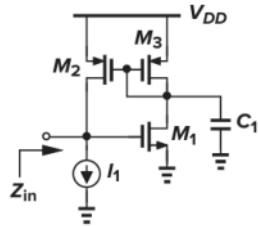


Figure 8.103

$$Z_{in} = \frac{r_{o2}}{1 - g_{m1} \frac{1}{jwC_1 + g_{m3}} g_{m2} r_{o2}} = -\frac{jwC_1 + g_{m3}}{g_{m1} g_{m2}}$$

8.23

In the circuit of Fig. 8.104, assume that $\lambda = 0$, $g_{m1,2} = 1/(200\Omega)$, $R_{1-3} = 2k\Omega$, and $C_1 = 100pF$. Neglecting other capacitances, estimate the closed-loop voltage gain at very low and very high frequencies.

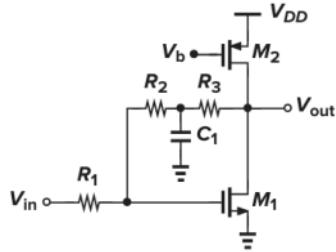


Figure 8.104

$$(1) f = \infty, \frac{V_{out}}{V_{in}} = \frac{R_2}{R_1 + R_2} g_{m1} R_3 = -5$$

$$(2) f = 0, F = \frac{-1}{R_2 + R_3}$$

$$I_{in} = \frac{V_{in}}{R_{in}}$$

$$A = [R_1](R_2 + R_3)g_{m1}(R_1 + R_2 + R_3) = -g_{m1}R_1(R_2 + R_3)$$

$$\frac{V_{out}}{I_{in}} = \frac{A}{1+AF} = 3.64k\Omega$$

$$\frac{V_{out}}{V_{in}} = -1.82$$

9 Operational Amplifier

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

9.1

- (a) Derive expressions for the transconductance and output resistance of a MOSFET in the triode region. Plot these quantities and $g_m r_o$ as a function of V_{DS} , covering both triode and saturation regions.
 (b) Consider the amplifier of Fig. 9.6(b), with $(W/L)_{1-4} = 50/0.5$, $I_{SS} = 1mA$, and input CM level of 1.3 V. Calculate the small-signal gain and the maximum output swing if all transistors remain in saturation.
 (c) For the circuit of part (b), suppose we allow each PMOS device to enter the triode region by 50 mV so as to increase the allowable differential swing by 100 mV. What is the small-signal gain at the peaks of the output swing?

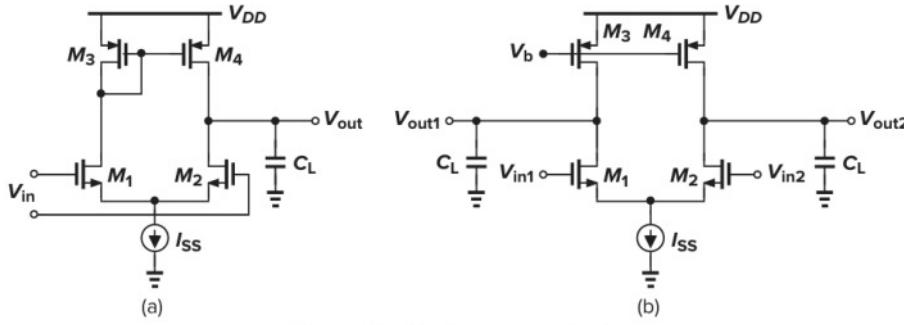


Figure 9.6 Simple op amp topologies.

$$(a) g_m = \frac{\delta I_D}{\delta V_{GS}} = \frac{\delta \mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2]}{\delta V_{gs}} = \mu_n C_{ox} \frac{W}{L} V_{ds}$$

$$r_o = \frac{1}{\frac{\delta I_D}{\delta V_{ds}}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_{th}) - V_{ds}]}$$

$$(b) V_{out,min} \geq V_g - V_{th} = 0.6V$$

$$V_{dsat3,4} = \sqrt{\frac{2I_3}{\mu_p C_{ox} (\frac{W}{L})_3}} = 0.51V$$

$$V_{out,max} \leq V_{DD} - V_{dsat3,4} = 2.489V$$

$$A_v = -g_m (r_{o4} || r_{o2}) \quad g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I} = 3.66 \text{ mS}$$

$$r_{o4} = \frac{1}{\lambda_p I} = 10k\Omega$$

$$r_{o2} = \frac{1}{\lambda_n I} = 20k\Omega$$

$$A_v = -24.41$$

$$(c) r_{o4} = \frac{1}{\mu_p C_{ox} \frac{W}{L} [(V_{gs} - V_{th}) - V_{ds}]} = 1.5k\Omega$$

$$A_v = -5.1$$

9.2

In the circuit of Fig. 9.9, assume that $(W/L)_{1-4} = 100/0.5$, $I_{SS} = 1mA$, $V_b = 1.4V$, and $\gamma = 0$.

- (a) If $M_5 - M_8$ are identical and have a length of 0.5 μ m, calculate their minimum width such that M_3 operates in saturation.
 (b) Calculate the maximum output voltage swing.
 (c) What is the open-loop voltage gain?
 (d) Calculate the input-referred thermal noise voltage.

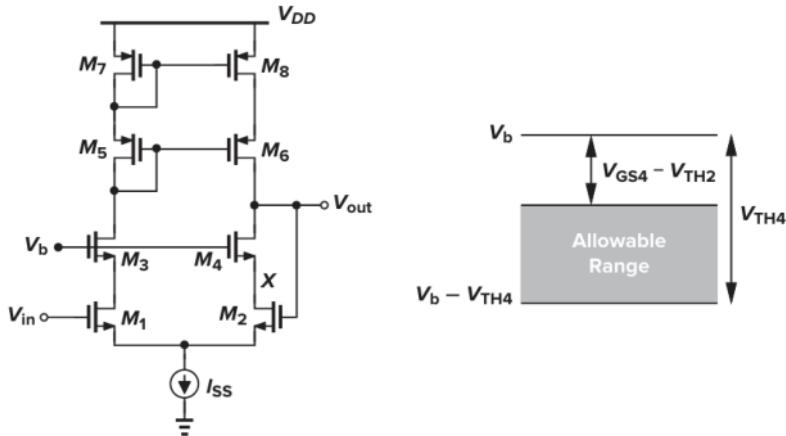


Figure 9.9 Telescopic cascode op amp with input and output shorted.

$$(a) V_D \geq V_G - V_{th} = 0.7V$$

$$2V_{gs,max} = 3 - 0.7 = 2.3V$$

$$I = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$$

$$W = 65\mu m$$

$$(b) V_{out} - 0.7 \leq V_x$$

$$V_{out} \geq V_b - V_{th,n4}$$

$$V_x = V_b - V_{gs4}$$

$$V_b - V_{th4} \leq V_{out} \geq V_b - (V_{gs4} - V_{th2})$$

$$(c) A_v = -g_{m1}(g_{m6}r_{o6}r_{o8}||g_{m4}r_{o4}r_{o2})$$

$$g_{m1,2,3,4} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I} = 5.18mS$$

$$g_{m5,6,7,8} = \sqrt{2\mu_p C_{ox} \frac{W}{L} I} = 2.22mS$$

$$r_{o2,4} = \frac{1}{\lambda I} = 20k\Omega$$

$$r_{o6,8} = \frac{1}{\lambda I} = 10k\Omega$$

$$A_v = -1038$$

$$(d) \overline{V_{n,in}^2} = 2(4kT\gamma \frac{1}{g_{m1}} + 4kT\gamma \frac{g_{m7}}{g_{m1}^2})$$

9.3

Design the folded-cascode op amp of Fig. 9.15 for the following requirements: maximum differential swing = 2.4 V, total power dissipation = 6 mW. If all of the transistors have a channel length of $0.5\mu m$, what is the overall voltage gain? Can the input common-mode level be as low as zero?

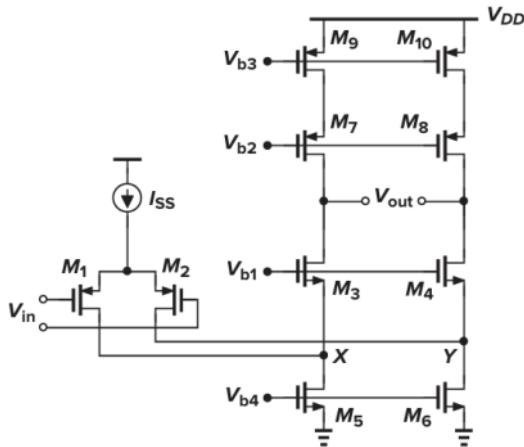


Figure 9.15 Folded-cascode op amp with cascode PMOS loads.

$$2(V_{DD} - |V_{od9}| - |V_{od7}| - V_{od3} - V_{od5}) = 2.4V$$

$$|V_{od9}| - |V_{od7}| - V_{od3} - V_{od5} = 3 - 1.2 = 1.8V$$

We set PMOS overdrive voltage to be greater than NMOS as NMOS mobility is greater than PMOS. So we set $M5$ overdrive to be 0.5V, $M3$ to be 0.3V, $M7$ and $M9$ to be 0.5V.

$$P = UI, 6mW = 3V \times 2I_5$$

$$I_5 = 1mA$$

We assume $I1$ and $I2$ to be 0.5mA.

$$I_{1/7/9} = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_9(V_{gs} - V_{th})^2$$

$$(\frac{W}{L})_9 = 104.3$$

$$W_{1/7/9} = 52.15\mu m$$

$$I_3 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_3(V_{gs} - V_{th})^2$$

$$(\frac{W}{L})_3 = 82.79$$

$$W_3 = 41.4\mu m$$

$$I_5 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_5(V_{gs} - V_{th})^2$$

$$(\frac{W}{L})_5 = 30$$

$$W_5 = 15\mu m$$

$$A_v = g_{m1}[(g_{m7}r_{o7})r_{o9}]||[(g_{m3}r_{o3})(r_{o1}||r_{o5})]$$

$$g_m = \frac{2I}{V_{gs} - V_{th}}$$

$$r_o = \frac{1}{\lambda I}$$

$$A_v = 276$$

Suppose I_{SS} is a PMOS with overdrive voltage of 0.4V. $V_{in} \leq V_{DD} - 0.4V - |V_{gs1}| = 1.3V$ $V_X \geq V_{od5}$

$$V_x \leq V_{in} + |V_{thp}|$$

$$V_{in} \geq -0.3V$$

It is ok to set input common-mode level to 0V.

9.4

In the op amp of Fig. 9.21(b), $(W/L)_{1-8} = 100/0.5$, $I_{SS} = 1mA$, and $V_{b1} = 1.7V$. Assume that $\gamma = 0$.

(a) What is the maximum allowable input CM level?

(b) What is V_X ?

(c) What is the maximum allowable output swing if the gate of M_2 is connected to the output?

(d) What is the acceptable range of V_{b2} ?

(e) What is the input-referred thermal noise voltage?

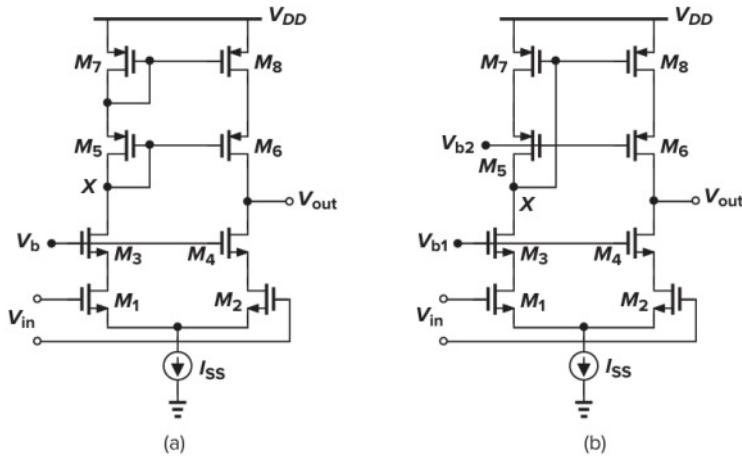


Figure 9.21 Cascode op amps with single-ended output.

$$(a) V_{in,CM} - V_p - V_{th} \leq V_{m1,D} - V_p$$

$$V_{in,CM} \leq V_{m1,D} + V_{th}$$

$$I_3 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_3(V_{gs} - V_{th})^2$$

$$V_{gs3} - V_{th} = \sqrt{\frac{2I_3}{\mu_n C_{ox}(\frac{W}{L})_3}} = 0.193V$$

$$V_{gs3} = 0.893V$$

$$V_{in,CM} \leq V_{in,CM} - V_{gs3} + V_{th} = 1.507V$$

$$(b) I_7 = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_7(V_{gs} - V_{th})^2$$

$$|V_{gs}| - |V_{th}| = 0.361V$$

$$|V_{gs}| = 1.161V$$

$$V_x = 3 - 1.161 = 1.839V$$

$$(c) Outputrange = V_{th4} - (V_{gs4} - V_{th2})$$

$$= V_{th2} - (V_{gs4} - V_{th4})$$

$$(V_{gs4} - V_{th4}) = \sqrt{\frac{2I}{\mu_n C_{ox}(\frac{W}{L})}} = 0.193V$$

$$Outputrange = 0.507V$$

$$(d) V_{DD} - V_{m7,d} \geq V_{od7} = \sqrt{\frac{2I}{\mu_n C_{ox}(\frac{W}{L})}} = 0.361V$$

$$V_{m7,d} \leq 2.639V$$

$$|V_{b2} - V_{m7,d}| - |V_{thp}| = V_{od5}$$

$$V_{b2} < 1.478V$$

$$|V_x - V_{m5,s}| \geq V_{od}$$

$$V_{m5,s} - V_{od} \geq V_x$$

$$V_{m5,s} - V_b = V_{od} + V_{th} = 1.161V$$

$$V_b \geq 1.039V$$

$$(e) V_{n,in}^2 = 2 \times (\overline{V_{in,1}^2} + \overline{V_{in,7}^2}) = 2 \times (4kT\gamma \frac{1}{g_{m1}} + 4kT\gamma g_{m7}/g_{m1}^2) = 6.54 \times 10^{-18}V^2/Hz$$

9.5

Design the op amp of Fig. 9.21(b) for the following requirements: maximum differential swing = 2.4 V, total power dissipation = 6 mW. (Assume that the gate of M_2 is never shorted to the output.)

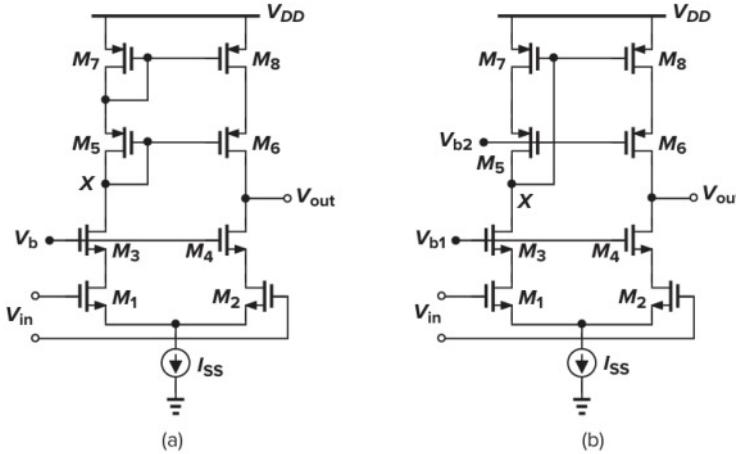


Figure 9.21 Cascode op amps with single-ended output.

$$P = UI$$

$$I = 2mA$$

$$I_{1-8} = 1mA$$

Because it is single-ended output, it is impossible to get 2.4V output swing.

9.6

If in Fig. 9.23, $(W/L)_{1-8} = 100/0.5$ and $I_{SS} = 1mA$,

(a) What CM level must be established at the drains of M3 and M4 so that $I_{D5} = I_{D6} = 1mA$? How does this constrain the maximum input CM level?

(b) With the choice made in part (a), calculate the overall voltage gain and the maximum output swing.

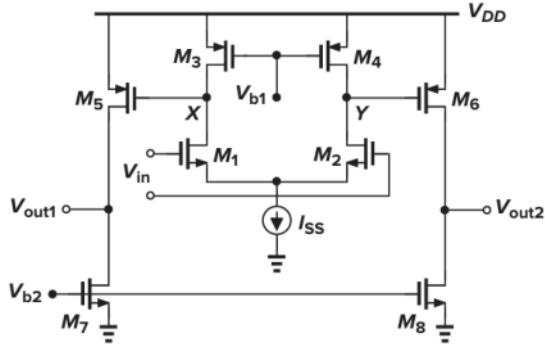


Figure 9.23 Simple implementation of a two-stage op amp.

$$\begin{aligned}
 \text{(a)} \quad & I_1 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{gs1} - V_{th})^2 \\
 & V_{gs1} - V_{thn} = \sqrt{\frac{2I}{\mu_n C_{ox} \left(\frac{W}{L} \right)_1}} = 0.193V \\
 & \text{Use the same way we can get } V_{gs5} - V_{thp} = 0.511V \\
 & V_{gs5} = 1.311V \\
 & V_x = V_{DD} - 1.311 = 1.692V \\
 & V_{in,CM} \leq V_x + V_{thn} = 2.4V \\
 \text{(b)} \quad & |A_v| = g_m 1 (r_{o1} || r_{o3}) g_m 5 (r_{o5} || r_{o7}) = 451 \\
 & \text{swing} = 2(V_{DD} - V_{od5} - V_{od7}) = 4.43V
 \end{aligned}$$

9.7

Design the opamp of Fig.9.23 for the following requirements: maximum differential swing = 4 V, total power dissipation = 6mW, $I_{SS} = 0.5$ mA.

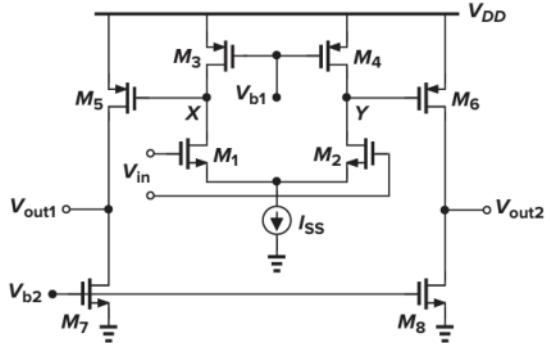


Figure 9.23 Simple implementation of a two-stage op amp.

$$\begin{aligned}
 P &= UI \\
 I &= 2mA \\
 I_{5-8} &= 0.5 \times (2 - 0.5) = 0.75mA \\
 \text{Swing} &= 2(V_{DD} - V_{od5} - V_{od7}) = 4V \\
 V_{od5} + V_{od7} &= 1V \\
 \text{So we set } V_{od5} &= 0.6V \text{ and } V_{od7} = 0.4V. \\
 I_5 &= \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_5 (V_{gs1} - V_{th})^2 \\
 \left(\frac{W}{L} \right)_5 &= \frac{2I}{\mu_p C_{ox} V_{od}^2} = 108 \\
 \left(\frac{W}{L} \right)_7 &= 70 \\
 V_{gs5} &= 0.6 + 0.8 = 1.4V \\
 V_x &= 3 - 1.4 = 1.6V \\
 \left(\frac{W}{L} \right)_3 &= 145 \\
 \left(\frac{W}{L} \right)_1 &= 93
 \end{aligned}$$

9.8

Suppose the circuit of Fig. 9.24 is designed with ISS equal to 1 mA, $I_{D9} - I_{D12}$ equal to 0.5 mA, and $(W/L)_{9-12} = 100/0.5$.

- What CM level is required at X and Y?
- If I_{SS} requires a minimum voltage of 400 mV, choose the minimum dimensions of $M_1 - M_8$ to allow a peak-to-peak swing of 200 mV at X and at Y.
- Calculate the overall voltage gain.

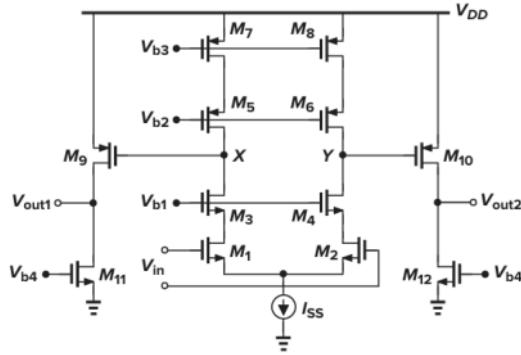


Figure 9.24 Two-stage op amp employing cascoding.

$$(a) I_9 = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{gs} - V_{th,p})^2$$

$$V_{gs} - V_{thp} = \sqrt{\frac{2I_9}{\mu_p C_{ox} \frac{W}{L}}} = 0.361V$$

$$|V_{gs}| = 1.161V$$

$$V_X = V_Y = V_{DD} - |V_{gs}| = 1.839V$$

$$(b) V_{x,max} = 1.839V + 0.5 \times 200mV = 1.939V$$

$$V_{x,min} = 1.839V - 0.5 \times 200mV = 1.739V$$

$$V_{DD} - |V_{od7}| - |V_{od5}| = 1.939V$$

$$V_{od5} = V_{od7} = 0.53V$$

$$V_{od1} = V_{od3} = 0.5(1.739 - 0.4) = 0.67V$$

$$(\frac{W}{L})_{5,7} = \frac{2I}{\mu_p C_{ox} V_{od}^2} = 92.83$$

$$(\frac{W}{L})_{1,3} = 16.6$$

$$(c) A_v = g_{m1} [(g_{m3} r_{o3}) r_{o1} || (g_{m5} r_{o5}) r_{o7}] g_{m9} (r_{o9} || r_{o11}) = 3200$$

9.9

In Fig. 9.88, calculate the input-referred thermal noise if I1 and I2 are implemented by PMOS devices.

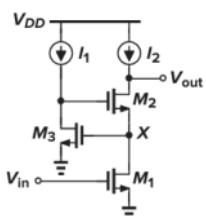


Figure 9.88

$$\overline{V_{in,n}^2} = 4kT\gamma \left(\frac{1}{g_{m1}} + \frac{g_{m5}}{g_{m1}^2} \right)$$

9.10

Suppose that in Fig. 9.88, $I_1 = 100\mu A$, $I_2 = 0.5mA$, and $(W/L)_{1-3} = 100/0.5$. Assuming that I_1 and I_2 are implemented with PMOS devices having $(W/L)_P = 50/0.5$,

- Calculate the gate bias voltages of M2 and M3.
- Determine the maximum allowable output voltage swing.
- Calculate the overall voltage gain and the input-referred thermal noise voltage.

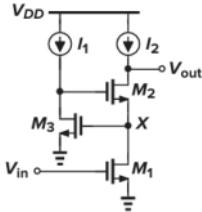


Figure 9.88

$$(a) I_3 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th,n})^2$$

$$V_{gs} - V_{th,n} = \sqrt{\frac{2I_3}{\mu_n C_{ox} \frac{W}{L}}} = 0.086V$$

$$V_{gs3} = 0.786V$$

$$V_{gs2} = 0.893V$$

$$V_{G,m2} = 0.893 + 0.786 = 1.679V$$

$$(b) V_{out,max} = V_{DD} - V_{od5}$$

$$V_{out,min} = V_{od2} + V_{gs3}$$

$$swing = V_{DD} - |V_{od5}| - V_{od2} - V_{od3} = 1.51V$$

$$(c) A_v = g_{m1}(1 + g_{m3}r_{o3})|r_{o5})g_{m2}r_{o2}r_{o1} \approx g_{m1}r_{o5} = 51.8$$

$$\frac{V_{in,n}^2}{V_{in,n}} = 4kT\gamma(\frac{1}{g_{m1}} + \frac{g_{m5}}{g_{m1}^2})$$

9.11

In the circuit of Fig. 9.53, each branch is biased at a current of 0.5 mA. Choose the dimensions of M7 and M8 such that the output CM level is equal to 1.5 V and $V_P = 100mV$.

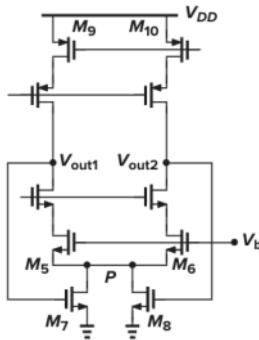


Figure 9.53 CMFB using triode devices.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [(V_{gs} - V_{th})V_{ds} - \frac{1}{2} V_{ds}^2]$$

$$(\frac{W}{L})_{7,8} = 99.35$$

9.12

Consider the CMFB network in Fig. 9.51. The amplifier sensing $V_{out,CM}$ is to be implemented as a different pair with active current mirror load.

- (a) Should the input pair of the amplifier use PMOS devices or NMOS devices?
- (b) Calculate the loop gain for the CMFB network.

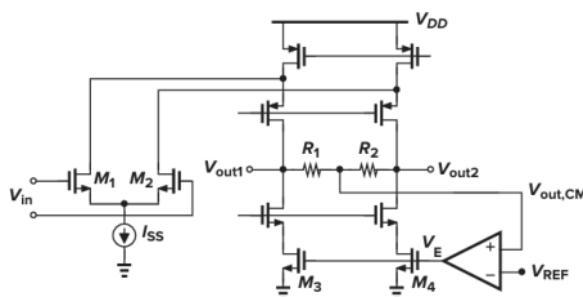


Figure 9.51 Sensing and controlling output CM level.

- (a) PMOs devices are better.
(b) $\frac{V_x}{V_{test}} = -g_{m3}[(g_{m5}r_{o5}r_{o3})||(g_{m7}r_{o7}(r_{o9}||r_{o1})]g_{m13}(r_{o11}||r_{o13})$

9.13

Repeat Problem 9.12b for the circuit of Fig. 9.52.

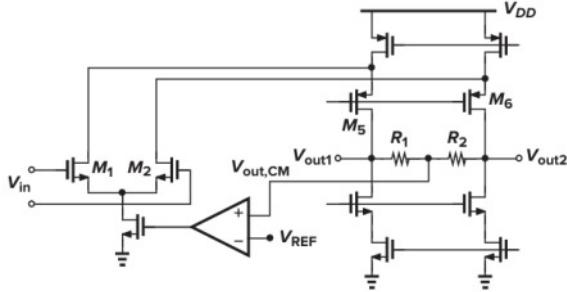


Figure 9.52 Alternative method of controlling output CM level.

$$\frac{V_x}{V_{test}} = g_{m13}(r_{o11}||r_{o13}) \frac{1}{2} g_{m15}[g_{m5}r_{o5}(r_{o9}||g_{m1}r_{o1}2r_{o15})]||g_{m5}r_{o5}r_{o3}]$$

9.14

In the circuit of Fig. 9.73(a), assume that $(W/L)_{1-4} = 100/0.5$, $C_1 = C_2 = 0.5\text{pF}$, and $I_{SS} = 1\text{mA}$.

(a) Calculate the small-signal time constant of the circuit.

(b) With a 1-V step at the input [Fig. 9.73(c)], how long does it take for I_{D2} to reach $0.1I_{SS}$?

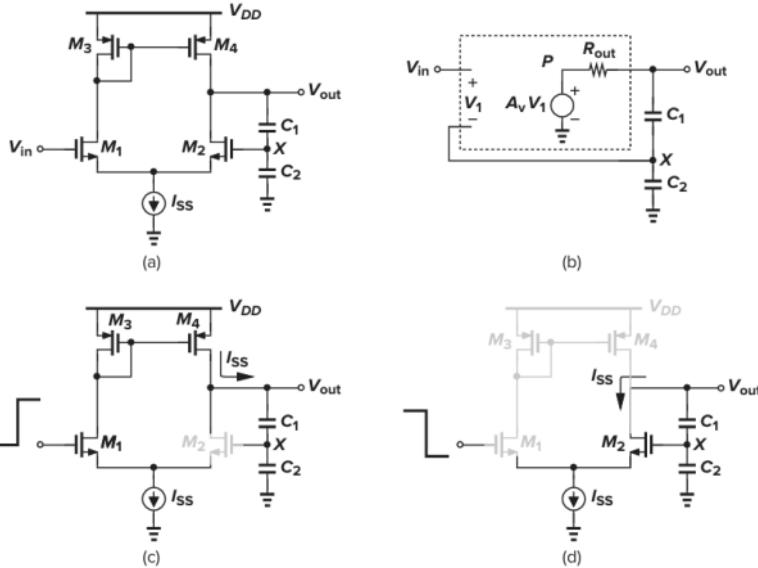


Figure 9.73

$$(a) A_{close} = \frac{A_{open}}{1 + BA_{open}}$$

$$B = \frac{C_1}{C_1 + C_2}$$

$$|A_{open}| = g_{m1}(r_{o2}||r_{o4}) \left(\frac{1}{sC_1} + \frac{1}{sC_2} \right) = g_{m1}(r_{o2}||r_{o4}) \frac{1}{1 + \frac{R_{out}}{C_1 + C_2}s}$$

$$\tau = \frac{\frac{R_{out}C_1C_2}{C_1+C_2}}{1 + A_v \frac{C_1}{C_1 + C_2}}$$

$$(b) \frac{I_{ss}t}{C_2} = \delta V_x$$

$$I_{d2} = 0.1I_{ss} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$$

$$V_{gs2} - V_{th} = 86\text{mV}$$

$$V_{gs1} - V_{th} = 258\text{mV}$$

$$\delta V_x = \delta V_{in} - V_{gs1} + V_{gs2} = 828\text{mV}$$

$$t = 414\text{ps}$$

9.15

It is possible to argue that the auxiliary amplifier in a gain-boosting stage reduces the output impedance. Consider the circuit as drawn in Fig. 9.89, where the drain voltage of M2 is changed by V to measure the output impedance. It seems that, since the feedback provided by A1 attempts to hold V_X constant, the change in the current through r_{O2} is much greater than in the original circuit, suggesting that $R_{out} \approx r_{O2}$. Explain the flaw in this argument.

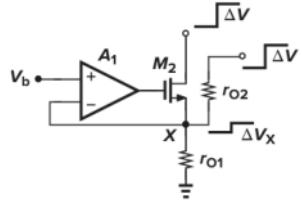


Figure 9.89

$$\delta I = \frac{\delta V_x}{r_{O1}} = \alpha \frac{\delta V}{r_{O1}} (\alpha \ll 1)$$

The current through r_{O1} is the real current we should consider rather than the current through r_{O2} .

9.16

Calculate the CMRR of the circuit shown in Fig. 9.73(a).

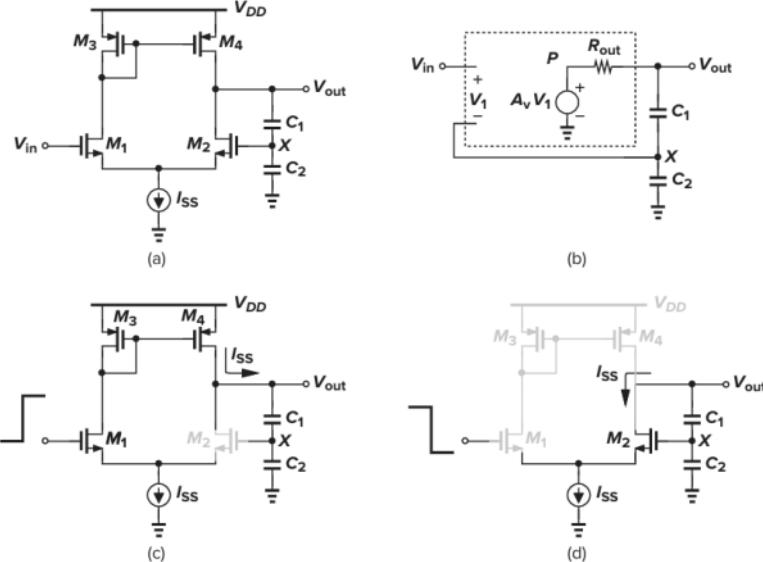
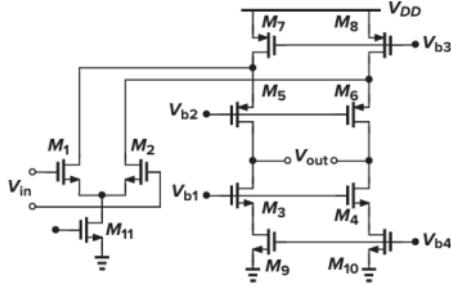


Figure 9.73

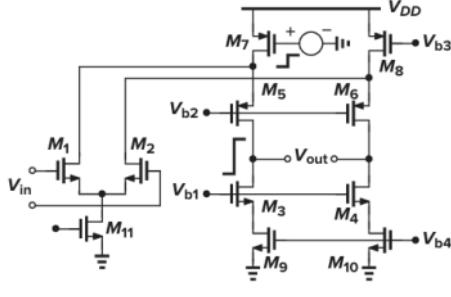
$$CMRR = \frac{A_{id}}{A_{ic}} = \frac{g_m(r_{o2}||r_{o4})}{\frac{g_{m1,2}}{(1+2g_{m1,2}R_{ss})g_{m3,4}}}$$

9.17

Calculate the input-referred flicker noise of the op amp shown in Fig. 9.85(a).



(a)



(b)

Figure 9.85 Noise in a folded-cascode op amp.

$$\overline{V_{n,in}^2} = 2 \left(\frac{K_n}{C_{ox}f(WL)_{1,2}} + \frac{K_p}{C_{ox}f(WL)_{7,8}} \frac{g_{m7}^2}{g_{m1}^2} + \frac{K_n}{C_{ox}f(WL)_{9,11}} \frac{g_{m9}^2}{g_{m1}^2} \right)$$

9.18

In this problem, we design a two-stage op amp based on the topology shown in Fig. 9.90. Assume a power budget of 6 mW, a required output swing of 2.5 V, and $L_{eff} = 0.5\mu\text{m}$ for all devices.

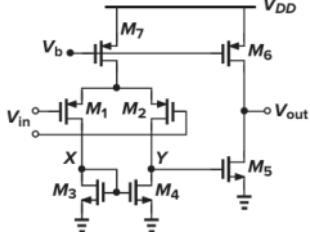


Figure 9.90

(a) Allocating a current of 1 mA to the output stage and roughly equal overdrive voltages to M5 and M6, determine $(W/L)_5$ and $(W/L)_6$. Note that the gate-source capacitance of M5 is in the signal path, whereas that of M6 is not. Thus, M6 can be quite a lot larger than M5.

(b) Calculate the small-signal gain of the output stage.

(c) With the remaining 1 mA flowing through M7, determine the aspect ratio of M3 (and M4) such that $V_{GS3} = V_{GS5}$. This is to guarantee that if $V_{in} = 0$ and hence $V_X = V_Y$, then M5 carries the expected current.

(d) Calculate the aspect ratios of M1 and M2 such that the overall voltage gain of the op amp is equal to 500.

$$(a) V_{od5,6} = 0.5(V_{DD} - 2.5V) = 0.25V$$

$$I_5 = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_5 V_{od}^2$$

$$\left(\frac{W}{L}\right)_5 = 238$$

$$\left(\frac{W}{L}\right)_6 = 834$$

$$(b) A_{v2} = g_{m5}(r_{o5} || r_{o6}) = \frac{2I_5}{V_{od}} \left(\frac{1}{\lambda_n I} || \frac{1}{\lambda_p I} \right) = 26.64$$

$$(c) I_3 = I_4 = \frac{1}{2}I_5 = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_3 V_{od}^2$$

$$\left(\frac{W}{L}\right)_3 = \frac{1}{2} \left(\frac{W}{L}\right)_5 = 119$$

$$(d) A_v = A_{v1}A_{v2}$$

$$A_{v1} = 18.75 = g_{m2}(r_{o2}||r_{o4})$$

$$g_{m2} = 2.8125mS = \sqrt{2\mu_p C_{ox}(\frac{W}{L})_{1,2} I_{1,2}}$$

$$(\frac{W}{L})_{1,2} = 206$$

9.19

Consider the op amp of Fig. 9.90, assuming that the second stage is to provide a voltage gain of 20 with a bias current of 1 mA.

- (a) Determine $(W/L)_5$ and $(W/L)_6$ such that M5 and M6 have equal overdrive voltages.
- (b) What is the small-signal gain of this stage if M6 is driven into the triode region by 50 mV?

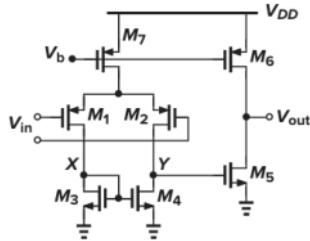


Figure 9.90

$$(a) A_{v2} = g_{m5}(r_{o5}||r_{o6})$$

$$V_{od5/6} = 0.33V$$

$$(\frac{W}{L})_5 = 134$$

$$(\frac{W}{L})_6 = 469$$

$$(b) I = \mu_p C_{ox}(\frac{W}{L})_6 [(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2]$$

$$r_{o6} = \frac{1}{\mu_p C_{ox}(\frac{W}{L})_6 (V_{gs} - V_{th} - V_{ds})} = 1.12k\Omega$$

$$A_{v2'} = 6$$

9.20

The op amp designed in Problem 9.18d is placed in unity-gain feedback. Assume that $|V_{GS7} - V_{TH7}| = 0.4V$.

- (a) What is the allowable input voltage range?
 - (b) At what input voltage are the input and output voltages exactly equal?
- (a) $g_{m1,2} = \frac{2I_1}{V_{od1}}$
 $V_{od1} = 0.35V$
 $V_{in,max} = 3 - 0.4 - 1.156 = 1.444V$
 $V_{out} \geq V_{od5} = 0.25V$
 $V_{in} \geq V_Y - |V_{thp}| = 0.15V$
- (b) $A(V_{in} - V_{out}) = V_{out}$ $I_5 = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_5 V_{od}^2 (1 + \lambda V_{ds})$
 $V_{ds} = 0.018V$

9.21

Calculate the input-referred noise of the op amp designed in Problem 9.18d.

$$\overline{V_{n,in}^2} = 2(4kT\gamma \frac{1}{g_{m1}} + 4kT\gamma \frac{g_{m3}}{g_{m1}^2}) + 4kT\gamma(g_{m5} + g_{m6}) \frac{1}{(g_{m1}(r_{o1}||r_{o4})g_{m5})^2}$$

9.22

It is possible to use the bulk terminal of PMOS devices as an input [10]. Consider the amplifier shown in Fig. 9.91 as an example.

- (a) Calculate the voltage gain.
- (b) What is the acceptable input common-mode range?
- (c) How does the small-signal gain vary with the input common-mode level?
- (d) Calculate the input-referred thermal noise voltage and compare the result with that of a regular

PMOS differential pair having NMOS current-source loads.

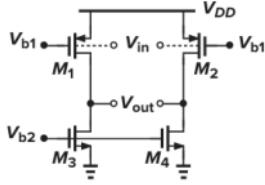


Figure 9.91

- (a) $A_v = g_{mb}(r_{o1} || r_{o3})$
- (b) $V_{in} > V_D - V_{junction}$
- (c) $g_{mb} = g_m \frac{\gamma}{2\sqrt{2|\phi_F| + |V_{sb}|}}$
- (d) $\overline{V_{n,in}^2} = 2(4kT\gamma(g_{m1} + g_{m3})R_{out}^2)/(A_v^2) = 2(4kT\gamma(g_{m1} + g_{m3}))/g_{mb}^2$

9.23

The idea of the active current mirror can be applied to the output stage of a two-stage op amp as well. That is, the load current source can become a function of the signal. Figure 9.92 shows an example [11]. Here, the first stage consists of M_1-M_4 , and the output is produced by M_5-M_8 . Transistors M_7 and M_8 operate as active current sources because their current varies with the signal voltage at nodes Y and X, respectively.

- (a) Calculate the differential voltage gain of the op amp.
- (b) Estimate the magnitude of the three major poles of the circuit.

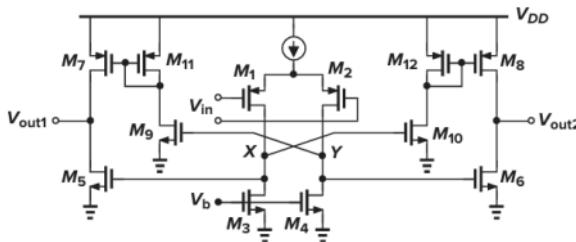


Figure 9.92

- (a) $A_v = g_{m1}(r_{o1} || r_{o3})2g_{m5,9}(r_{o5} || r_{o7})$ (b) X/Y, V_{out} , current mirror.
- At V_{out} , $w_{out} = \frac{1}{(r_{o5} || r_{o7})(C_{gd5} + C_{db5} + C_{gd7} + C_{db7})}$
- At X/Y, $w_{x,y} = \frac{1}{(r_{o1} || r_{o3})(C_{gd1} + C_{db1} + C_{dg3} + C_{db3} + C_{gs10} + C_{gd10}[1 + g_{m10}/g_{m12}] + C_{gs5} + C_{gd5}(1 + g_{m5}r_{o5} || r_{o7}))}$
- At current mirror point, $w_3 = \frac{1}{r_{o9} || r_{o11}(C_{gd9} + C_{gb9} + C_{db11} + C_{gs11} + C_{gs7} + C_{gd7}(1 + g_{m7}r_{o7} || r_{o5}))}$

9.24

The circuit of Fig.9.93 employs a fast path(M_1 and M_2)in parallel with the slow path. Calculate the differential voltage gain of the circuit. Which transistors typically limit the output swing?

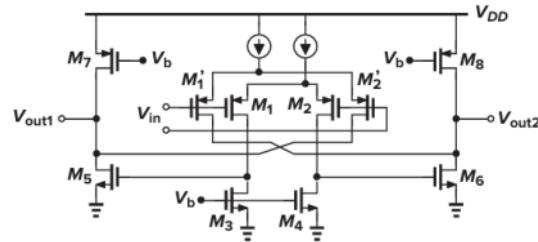


Figure 9.93

$$\begin{aligned} A_{v1} &= g'_{m1}r'_{o1}||r_{o8}||r_{o6} \\ A_{v2} &= g_{m2}(r_{o2}||r_{o4})g_{m6}(r'_{o1}||r_{o8}||r_{o6}) \\ M7, M5, M2' &\text{ will limit the output swing.} \end{aligned}$$

9.25

Calculate the input-referred thermal noise of the op amp in Fig. 9.93.

$$\overline{V_{in,n}^2} = \frac{V_{out,n}^2}{A_v^2} = \frac{i_{n,out}^2}{G_m^2} = \frac{2(i_{n5}^2 + i_{n7}^2 + i_{n2}^2) + 2[(i_{n1}^2 + i_{n3}^2)(r_{o1}||r_{o3})^2 g_{m5}^2]}{(g_{m2'} + g_{m1}(r_{o1}||r_{o3})g_{m5})^2}$$

9.26

Determine the slew rate of a fully-differential folded-cascode op amp.

$$SR = \frac{I_{ss}}{2C_L}$$

9.27

Calculate the slew rate in Fig. 9.75 if $I_{SS} > I_P$.

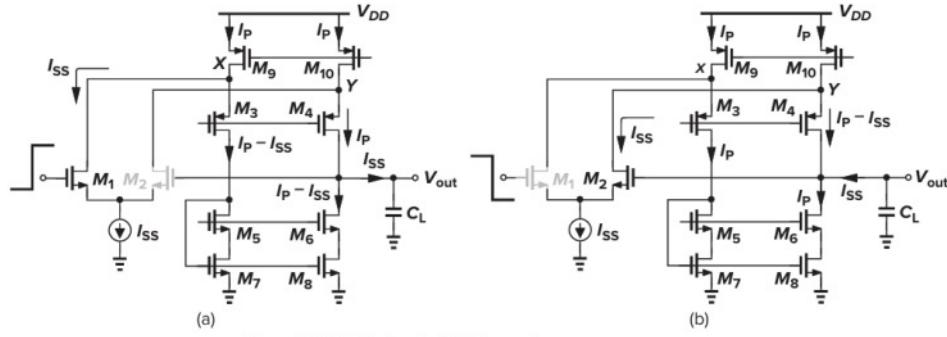


Figure 9.75 Slewing in folded-cascode op amp.

$$SR = \frac{2I_p - I_{ss}}{C_L}$$

10 Stability and Frequency Compensation

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3V$ where necessary. All device dimensions are effective values and in microns.

10.1

An amplifier with a forward gain of A_0 and two poles at 10 MHz and 500 MHz is placed in a unity-gain feedback loop. Calculate A_0 for a phase margin of 60° .

$$H(s) = \frac{A_0}{(1+\frac{s}{w_1})(1+\frac{s}{w_2})}$$

$$\frac{w}{w_2} = \tan(30^\circ) = \frac{1}{\sqrt{3}}$$

$$w = \frac{500}{\sqrt{3}} \text{ MHz} = 288.68 \text{ MHz}$$

$$\frac{288.68}{10} = 28.87$$

$$20 \times \log(28.87) = 29.21 \text{ dB}$$

10.2

An amplifier with a forward gain of A_0 has two coincident poles at w_p . Calculate the maximum value of A_0 for a 60° phase margin with a closed-loop gain of (a) unity and (b) 4.

$$A_0 = \frac{A_0}{(1+\frac{s}{w_p})^2}$$

$$A_{close} = \frac{A_0}{1+BA_0}$$

$$BA_0 = B \frac{A_0}{(1+\frac{s}{w_p})^2}$$

$$PM = 180^\circ - \arctan \frac{w}{w_p} - \arctan \frac{w}{w_p} = 60^\circ$$

$$\arctan(\frac{w}{w_p}) = 60^\circ$$

$$w = \sqrt{3}w_p$$

If phase margin is 60° , $B \frac{A_0}{(1+\frac{s}{w_p})^2} = 1$, $BA_0 = 4$

(a) As closed-loop gain is unity, $\frac{A_0}{1+BA_0} = 1$, $A_0 = 5$
(b) If closed-loop gain is 4, $A_0 = 20$

10.3

An amplifier has a forward gain of $A_0 = 1000$ and two poles at w_{p1} and w_{p2} . For $w_{p1} = 1 \text{ MHz}$, calculate the phase margin of a unity-gain feedback loop if (a) $w_{p2} = w_{p1}$ and (b) $w_{p2} = 4w_{p1}$.

(a) $BA = A = \frac{A_0}{(1+\frac{s}{w_{p1}})(1+\frac{s}{w_{p2}})}$

$$1000 = (1 + \frac{s}{w_{p1}})(1 + \frac{s}{w_{p2}})$$

$$w_{p1} = w_{p2} = \sqrt{999}w_p \quad PM = 180^\circ - 2 \times \arctan \frac{\sqrt{999}}{1} = 3.624^\circ$$

(b) $PM = 4.5^\circ$

10.4

A unity-gain closed-loop amplifier exhibits a frequency peaking of 50% in the vicinity of the gain crossover. What is the phase margin?

$$BA = e^{-j(180^\circ - PM)}$$

$$A_{closed} = \frac{A}{1+BA} = \frac{\frac{1}{B}e^{-j(180^\circ - PM)}}{1+e^{-j(180^\circ - PM)}} = \frac{1}{B}$$

$$PM = 39^\circ$$

10.5

Consider the transimpedance amplifier shown in Fig. 10.73, where $R_D = 1k\Omega$, $R_F = 10k\Omega$, $g_{m1} = g_{m2} = 1/(100\Omega)$, and $C_A = C_X = C_Y = 100fF$. Neglecting all other capacitances and assuming that $\lambda = \gamma = 0$, compute the phase margin of the circuit. (Hint: break the loop at node X.)

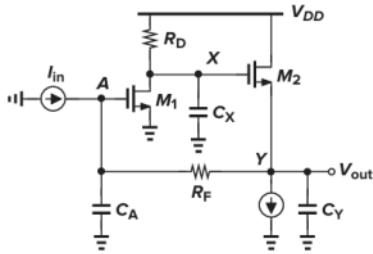


Figure 10.73

$$BA = \frac{g_m \frac{1}{sC_Y}}{1 + g_m \frac{1}{sC_Y}} \left(\frac{\frac{1}{sC_A}}{\frac{1}{sC_A} + R_F} \right) [-g_m 3(R_D || \frac{1}{sC_X})] = \frac{-g_m R_D}{(1 + \frac{s}{g_m 2})(1 + \frac{s}{C_A R_F})(1 + \frac{s}{R_D C_X})}$$

$$A_0 = g_m 1 R_D = 10$$

$$w_1 = \frac{g_m 2}{C_Y} = 10^{11} \text{ rad/s}$$

$$w_2 = \frac{1}{C_A R_F} = 10^9 \text{ rad/s}$$

$$w_3 = \frac{1}{R_D C_X} = 10^{10} \text{ rad/s}$$

$$PM = 45^\circ$$

10.6

In Problem 10.5, what is the phase margin if R_D is increased to $2k\Omega$?

$$A_0 = g_m 1 R_D = 20$$

$$w_1 = \frac{g_m 2}{C_Y} = 10^{11} \text{ rad/s}$$

$$w_2 = \frac{1}{C_A R_F} = 10^9 \text{ rad/s}$$

$$w_3 = \frac{1}{R_D C_X} = 5 \times 10^9 \text{ rad/s}$$

$$BA = 1$$

$$w/w_1 = 9.32$$

$$PM = 180^\circ - \arctan 9.32 - \arctan(9.32/5) = 34^\circ$$

10.7

If the phase margin required of the amplifier of Problem 10.5 is 45° , what is the maximum value of (a) C_Y , (b) C_A , and (c) C_X while the other two capacitances remain constant?

$$(a) C_Y \leq 100 \text{ fF.}$$

$$(b) C_A \leq 100 \text{ fF.}$$

$$(c) C_X \leq 100 \text{ fF.}$$

10.8

Prove that the zero of the circuit shown in Fig. 10.32 is given by Eq. (10.30). Apply the technique illustrated in Fig. 6.18.

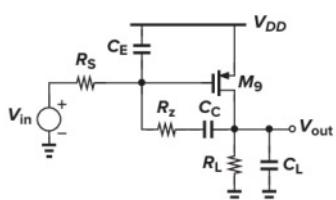


Figure 10.32 Addition of R_z to move the right-half-plane zero.

$$\frac{V_{in}}{R_z + \frac{1}{sC_c}} - g_m V_{in} = 0$$

$$s_z = \frac{g_m}{C_c(1 - g_m R_z)}$$

10.9

Consider the amplifier of Fig. 10.74, where $(W/L)_{1-4} = 50/0.5$ and $I_{SS} = I_1 = 0.5mA$.

(a) Estimate the poles at nodes X and Y by multiplying the small-signal resistance and capacitance to

ground. Assume that $C_X = C_Y = 0.5\text{pF}$. What is the phase margin for unity-gain feedback?

(b) If $C_X = 0.5\text{pF}$, what is the maximum tolerable value of C_Y that yields a phase margin of 60° for unity-gain feedback?

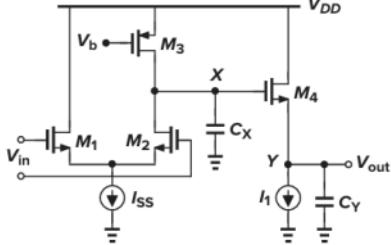


Figure 10.74

$$(a) BA = A = \frac{-1}{2} g_{m2}(r_{o2} || r_{o4} || \frac{1}{sC_4}) g_{m4}(\frac{1}{g_{m4}} || \frac{1}{sC_4})$$

$$w_1 = \frac{1}{C_x(r_{o2} || r_{o3})}$$

$$w_2 = \frac{1}{C_Y \frac{1}{g_{m4}}}$$

$$A_0 = \frac{1}{2} g_{m2}(r_{o2} || r_{o3}) = 17.27$$

$$w/w_1 = 16$$

$$PM = 75.35^\circ$$

$$(b) \arctan \frac{w}{g_{m4}/C_Y} = 30^\circ$$

10.10

Estimate the slew rate of the op amp of Problem 10.9 for both parts (a) and (b).

$$\text{slewrate} = \frac{0.5I_{ss}}{C_x} = 5 \times 10^8 \text{V/s}$$

10.11

In the two-stage op amp of Fig. 10.75, $W/L = 50/0.5$ for all transistors except for $M_{5,6}$, for which $W/L = 60/0.5$. Also, $I_{SS} = 0.25 \text{ mA}$ and each output branch is biased at 1 mA .

(a) Determine the CM level at nodes X and Y.

(b) Calculate the maximum output voltage swing.

(c) If each output is loaded by a 1-pF capacitor, compensate the op amp by Miller multiplication for a phase margin of 60° in unity-gain feedback. Calculate the pole and zero positions after compensation.

(d) Calculate the resistance that must be placed in series with the compensation capacitors to position the zero atop the nondominant pole.

(e) Determine the slew rate.

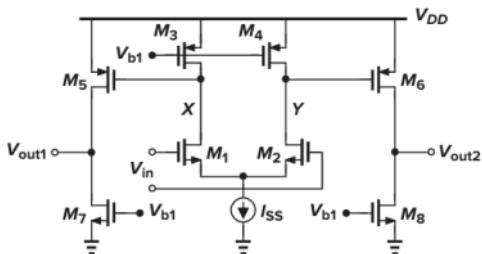


Figure 10.75

$$(a) I_5 = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_5 (V_{gs5} - V_{th})^2$$

$$V_{gs5} = 1.459V$$

$$V_{CM,X,Y} = 3 - 1.459 = 1.54V$$

$$(b) \text{swing} = 2(V_{max} - V_{min})$$

$$V_{max} = 3 - 0.659 = 2.341V$$

$$I_7 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_7 (V_{gs7} - V_{th})^2$$

$$V_{min} = V_{od7} = 0.386V$$

$$(c) A_{v1} = g_{m1}(r_{o1} || r_{o3})$$

$$A_{v2} = g_{m5}(r_{o5}) || r_{o7}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I}$$

$$A_v = 493.5 = 53.8dB$$

$$53.8/20 = 2.69$$

$$\frac{w_1}{w_d} = 10^{2.69} = 493$$

$$w_{nd} = \sqrt{3}w_1 = 855.2w_d$$

$$w_{nd} = \frac{1}{C_L \frac{1}{g_{m6}}} = 3 \times 10^9 rad/s$$

$$w_1 = \frac{1}{\sqrt{3}}w_{nd} = 1.75 \times 10^9 rad/s$$

$$w_d = 3.55 \times 10^9 rad/s$$

$$w_z = \frac{g_{m6}}{C_c}$$

$$(d) R_z = \frac{1}{g_m} \left(1 - \frac{C_L}{C_c}\right)$$

$$(e) \text{slew rate} = \frac{I_Y}{C_c}$$

10.12

In Problem 10.11, the pole-zero cancellation resistor is implemented with a PMOS device as in Fig. 10.34.

Calculate the dimensions of $M_{13}-M_{15}$ if $I_1 = 100\mu A$.

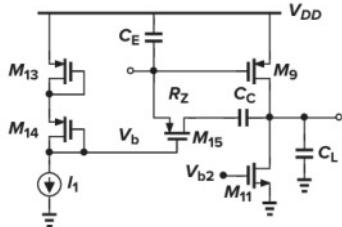


Figure 10.34 Generation of V_b for proper temperature and process tracking.

$$s_z = \frac{g_m}{C_c(1-g_m R_z)} = \frac{-g_m}{C_L}$$

$$R_z = \frac{C_L + C_c}{g_m C_c} = 646.5\Omega$$

$$R_{15} = \frac{1}{\mu_p C_{ox} (\frac{W}{L})_{15} (V_{gs} - V_{th})_{15}} = \frac{1}{\mu_p C_{ox} (\frac{W}{L})_{15} (V_{gs} - V_{th})_{14}} = \frac{(\frac{W}{L})_{14}}{(\frac{W}{L})_{15} g_{m14}}$$

$$(\frac{W}{L})_{13} = \frac{2I_{13}}{\mu_p C_{ox} (V_{gs} - V_{th})^2} = 12$$

$$V_{gs14} = 3 - 1.46 - 0.5 = 1.04V$$

$$(\frac{W}{L})_{15} = 168$$

$$(\frac{W}{L})_{14} = 90$$

10.13

Calculate the input-referred thermal noise voltage of the op amp shown in Fig. 10.75.

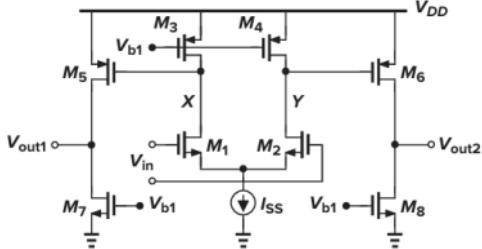


Figure 10.75

$$\overline{V_{n,in}^2} = 2 \times (4kT\gamma \frac{g_{m1}+g_{m3}}{g_{m1}^2} + 4kT\gamma \frac{g_{m5}+g_{m7}}{[g_{m1}(r_{o3}||r_{o1})g_{m5}]^2})$$

10.14

Figure 10.76 depicts a transimpedance amplifier employing voltage-current feedback. Note that the feedback factor may exceed unity because of M3. Assume that I_1-I_3 are ideal, $I_1 = I_2 = 1mA$, $I_3 = 10\mu A$, $(W/L)_{1,2} = 50/0.5$, and $(W/L)_3 = 5/0.5$.

(a) Breaking the loop at the gate of M3, estimate the poles of the open-loop transferfunction.

- (b) If the circuit is compensated by adding a capacitor C_c between the gate and the drain of M1, what value of CC achieves a phase margin of 60° ? Determine the poles after compensation.
(c) What resistance must be placed in series with CC to position the zero of the output stage atop the first nondominant pole?

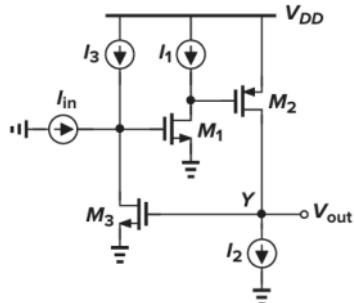


Figure 10.76

(a) For the node at the gate of M1,B, $C_{db3} + C_{dg3}(1 + \frac{1}{A_{v3}}) + C_{gs1} + C_{gd1}(1 + A_{v1})$

For the node at the gate of M2,A, $(1 + \frac{1}{A_{v1}})C_{gd1} + C_{db1} + (1 + A_{v2})C_{gd2} + C_{gs2}$

For Y, $C_{db2} + (1 + \frac{1}{A_{v2}})C_{gd2} + C_{gs3} + (1 + A_{v3})C_{gd3}$

$$C_{gd} = WC_{ov}$$

$$C_{gs} = WC_{ov} + \frac{2}{3}WLC_{ox}$$

$$C_{db} = C_jWE + C_{jw}2(W + E)$$

$$A_{v1} = g_{m1}r_{o1} = 51.8$$

$$A_{v2} = g_{m2}r_{o2} = 14$$

$$A_{v3} = g_{m3}r_{o3} = 164$$

$$w_B = \frac{1}{C_B r_{o3}} = 0.947 \times 10^6 \text{ rad/s}$$

$$w_A = \frac{1}{C_A r_{o1}} = 4.49 \times 10^8 \text{ rad/s}$$

$$w_Y = \frac{1}{C_Y r_{o2}} = 6.06 \times 10^8 \text{ rad/s}$$

$$BA = 101.41 \text{ dB}$$

$$\frac{w_1}{w_B} = 10^{101.4/20} = 1.17 \times 10^5$$

$$(b) w_d = \frac{1}{(A_{v1}C_c + C_B)r_{o3}}$$

$$w_{nd} = \frac{g_{m1}}{C_A} = 2.32 \times 10^{10} \text{ rad/s}$$

$$\frac{w_1}{w_{nd}} = \arctan(30^\circ) = \frac{1}{\sqrt{3}}$$

$$w_1 = 1.343 \times 10^{10} \text{ rad/s}$$

$$w_d = \frac{w_1}{10^5 \cdot 0.07} = 0.11 \times 10^6 \text{ rad/s}$$

$$C_c = 0.15 \text{ pF}$$

$$(c) \frac{V_{in}}{R_z + \frac{1}{sC_c}} = g_m V_{in}$$

10.15

Repeat Problem 10.14 if the output node is loaded by a 0.5-pF capacitor.

The capacitance at node Y changes. $w_Y = 2.4 \times 10^8 \text{ rad/s}$

$$w_1/w_Y = \frac{1}{\sqrt{3}}$$

$$w_d = 1.180 \times 10^3 \text{ rad/s}$$

$$C_c = 16.3 \text{ pF}$$

$$R_Z = 448 \Omega$$

10.16

Suppose that in the circuit of Fig. 10.76, a large negative input current is applied such that M1 turns off momentarily. What is the slew rate at the output?

$$\text{slew rate} = \frac{-I_2}{C_Y}$$

10.17

Explain why, in the circuit of Fig. 10.76, the compensation capacitor should not be placed between the gate and the drain of M2 or M3.

We add the compensation capacitor for pole splitting. Because the dominant pole is at the node of gate of M1 and the non-dominant pole is at the node of gate of M2.

10.18

Determine the input-referred noise current of the circuit shown in Fig. 10.76 and described in Problem 10.14. $A_{closed} = \frac{A_0}{1+BA_0}$

$$A_0 = r_{o3}g_{m1}r_{o1}g_{m2}r_{o2}$$

$$B = g_{m3}$$

$$A_{closed} = \frac{1}{g_{m3} + \frac{1}{r_{o3}g_{m1}r_{o1}g_{m2}r_{o2}}}$$

$$\overline{I_{n,in}^2} = \frac{V_{n,out}^2}{A_{closed}^2}$$

$$V_B = -r_{o3}(g_{m3}V_{n,out} + I_{n3})$$

$$V_A = -r_{o1}(g_{m1}V_B + I_1)$$

$$V_{n,out} = -r_{o2}(g_{m2}V_A + I_{n2})$$

$$\overline{V_{n,out}^2} = \frac{I_{n2}^2 + (g_{m2}r_{o1})^2 I_{n1}^2 + (g_{m1}g_{m2}r_{o1}r_{o3})^2 I_{n3}^2}{\frac{1}{(r_{o2})} + g_{m1}g_{m2}r_{o1}r_{o3}g_{m3}}^2$$

10.19

The cancellation of a pole by a zero, e.g., in a two-stage op-amp, entails an issue called the “doublet problem” [5,6]. If the pole and the zero do not exactly coincide, we say that they constitute a doublet. The step response of feedback circuits in the presence of doublets is of great interest. Suppose the open-loop transfer function of a two-stage op-amp is expressed as

$$H_{open}(s) = \frac{A_0(1+\frac{s}{w_z})}{(1+\frac{s}{w_{p1}})(1+\frac{s}{w_{p2}})}$$

Ideally, $w_z = w_{p2}$ and the feedback circuit exhibits a first-order behavior, i.e., its step response contains a single time constant and no overshoot.

(a) Prove that the transfer function of the amplifier in a unity-gain feedback loop is given by $H_{closed}(s) = \frac{A_0(1+\frac{s}{w_z})}{\frac{s^2}{w_{p1}w_{p2}} + (\frac{1}{w_{p1}} + \frac{1}{w_{p2}} + \frac{A_0}{w_z})s + A_0 + 1}$

(b) Determine the two poles of $H_{closed}(s)$, assuming they are widely spaced.

(c) Assuming $w_z = w_{p2}$ and $w_{p2} \ll (1+A_0)w_{p1}$, write $H_{closed}(s)$ in the form

$$H_{closed}(s) = \frac{A(1+\frac{s}{w_z})}{(1+\frac{s}{w_{pA}})(1+\frac{s}{w_{pB}})}$$

and determine the small-signal step response of the closed-loop amplifier.

(d) Prove that the step response contains an exponential term of the form $(1-w_z/w_{p2})\exp(-w_{p2}t)$. This is an important result, indicating that if the zero does not exactly cancel the pole, the step response exhibits an exponential with an amplitude proportional to $1-w_z/w_{p2}$ (which depends on the mismatch between w_z and w_{p2}) and a time constant of $1/w_z$.

$$(a) H_{closed} = \frac{A_0}{1+BA_0} = \frac{A_0}{1+A_0} = \frac{\frac{A_0(1+\frac{s}{w_z})}{(1+\frac{s}{w_{p1}})(1+\frac{s}{w_{p2}})}}{1 + \frac{A_0(1+\frac{s}{w_z})}{(1+\frac{s}{w_{p1}})(1+\frac{s}{w_{p2}})}} = \frac{A_0(1+\frac{s}{w_z})}{\frac{s^2}{w_{p1}w_{p2}} + (\frac{1}{w_{p1}} + \frac{1}{w_{p2}} + \frac{A_0}{w_z})s + A_0 + 1}$$

$$(b) \text{ When } s \text{ is small, } (\frac{1}{w_{p1}} + \frac{1}{w_{p2}} + \frac{A_0}{w_z})s + A_0 + 1 = 0, s = -\frac{A_0 + 1}{\frac{1}{w_{p1}} + \frac{1}{w_{p2}} + \frac{A_0}{w_z}}$$

$$\text{When } s \text{ is large, } \frac{s^2}{w_{p1}w_{p2}} + (\frac{1}{w_{p1}} + \frac{1}{w_{p2}} + \frac{A_0}{w_z})s = 0$$

$$s = -(w_{p1} + w_{p2} + \frac{w_{p1}w_{p2}}{w_z}A_0)$$

$$(c) w_{pA} = (1+A_0)w_{p1}$$

$$w_{pB} = w_{p2}$$

$$(d) Y(s) = \frac{1}{s}H_{closed} = \frac{1}{s} \frac{A(1+\frac{s}{w_z})}{(1+\frac{s}{w_{pA}})(1+\frac{s}{w_{pB}})}$$

Math Problem.

10.20

Using the results of the previous problem, determine the step response of the amplifier described in Problem 10.11 with (a) perfect pole-zero cancellation, and (b) 10% mismatch between the pole and the zero magnitudes.

- (a) $H(t) = A'_0 u(t)$
- (b) $H(t) = A'_0 (1 - 0.1e^{-w_p t})$

10.21

It is possible to raise the voltage gain of a folded-cascode op-amp by adding a secondary path. As shown in Fig. 10.77 (gray section), the input signal can also travel through a differential pair with current-source loads I_1 and I_2 , and drive the current sources in the original op-amp. Of course, nodes X and Y exhibit relatively high impedance, thus contributing a pole that significantly degrades the phase margin. (a) Neglecting channel-length modulation in I_1 and I_2 determine the low-frequency gain of the op-amp. (b) Considering only the capacitances at nodes X, Y, P, Q, and the output nodes, compute the overall transfer function. Is it possible for the zero to cancel one of the poles?

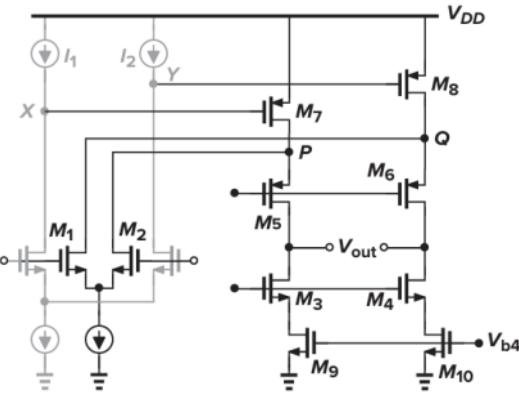


Figure 10.77

$$(a) A_v = g_{m1} R_{out}$$

$$(b) A_v = g_{m12} r_{o12} g_{m8} R_{out}$$

$$R_{out} = g_{m4} r_{o4} r_{o10} || g_{m6} r_{o6} (r_{o8} || r_{o1})$$

$$H(s) = \frac{A(1 + \frac{s}{w_z})}{(1 + \frac{s}{w_1})(1 + \frac{s}{w_2})(1 + \frac{s}{w_3})}$$

$$w_Q = \frac{1}{(r_{o11} || r_{o8} || r_o) C_p}$$

$$w_{out} = \frac{1}{(g_{m4} r_{o4} r_{o10}) || (g_{m6} r_{o6} r_{o8}) C_{out}}$$

$$w_Y = \frac{1}{r_{o12} A_{v8} C_{gss}}$$

$$g_{m12} V_{in} (r_{o12} || \frac{1}{s C_Y}) g_{m8} + g_{m1} V_{in} = 0$$

$$s_z = \frac{-g_{m12} r_{o12} g_{m8}}{g_{m1} r_{o1} C_Y}$$

10.22

Consider the circuit of Fig. 10.37(b) and assume that $I_{in} = I_{SS} u(t)$. Also, assume that a load capacitance of C_L is tied from the drain to ground. Write a KCL at the output node and derive a differential equation in terms of V_{out} . Taking the Laplace transform and using partial fractions, prove that $V_{out}(t) = \frac{I_{SS}}{C_F} t u(t) - \frac{I_{SS}}{g_m} (1 + \frac{C_L}{C_F}) u(t) - \frac{I_{SS}}{g_m} (1 + \frac{C_L}{C_F}) e^{-\frac{t}{\tau}} u(t)$

where $\tau = CL/gm$. Plot these three terms as a function of time and determine the time at which $V_{out}(t)$ reaches a minimum. This result indicates that the output initially falls and then assumes a ramp behavior.

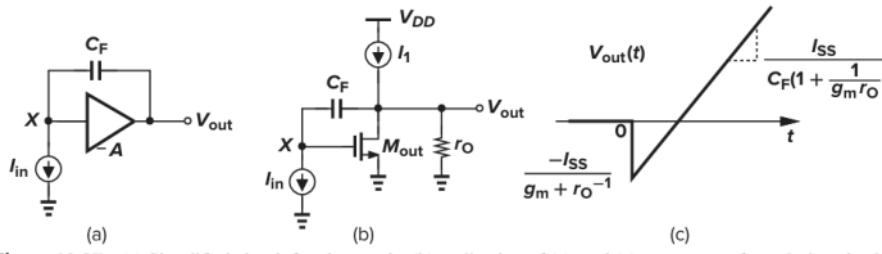


Figure 10.37 (a) Simplified circuit for slew study, (b) realization of (a), and (c) output waveform during slewing.

$$i + \frac{V_x - V_{out}}{\frac{1}{sC_F}} = 0$$

$$\frac{V_{out}}{r_o || \frac{1}{sC_L} + g_m V_x} = \frac{V_x - V_{out}}{\frac{1}{sC_F}}$$

Math problem.

10.23

A two-stage op amp is compensated for a phase margin of 60° with $\beta = 1$. If β is reduced to $\beta_1 < 1$, determine the new phase margin.

$$w_1/w_{nd} = B \frac{1}{\sqrt{3}}$$

11 Nanometer Design Studies

11.1

Consider the characteristics shown in Fig. 11.2. Estimate a λ value for $V_{GS} - V_{TH} = 350\text{mV}$ based on the slope from $V_{DS} = 0.2\text{V}$ to 1 V. [Hint: express the ratio of two currents at V_{DS1} and V_{DS2} as $(1 + \lambda V_{DS1})/(1 + \lambda V_{DS2})$]. Repeat this calculation for $V_{GS} - V_{TH} = 200\text{ mV}$, 250 mV, and 300 mV. What trend do you observe?

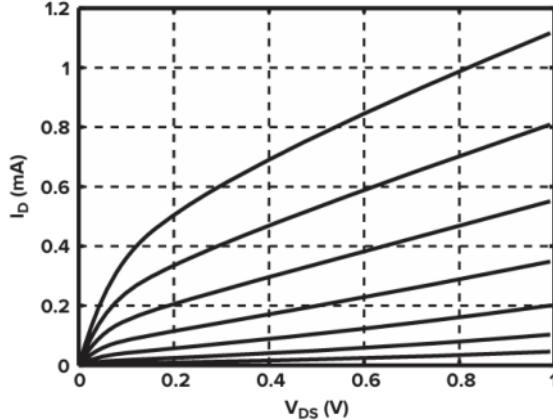


Figure 11.2 I-V characteristics of a 5- $\mu\text{m}/40\text{-nm}$ device for $V_{GS} - V_{TH} = 50, \dots, 350\text{ mV}$.

$$\begin{aligned}\frac{I_{D1}}{I_{D2}} &= \frac{1+\lambda V_{DS1}}{1+\lambda V_{DS2}} \\ \lambda &= \frac{I_{D2}-I_{D1}}{I_{D1}V_{DS2}-I_{D2}V_{DS1}} = 2.14 @ 350\text{ mV} \\ &= 3.57 @ 300\text{ mV} \\ &= 3.89 @ 250\text{ mV} \\ &= 8.33 @ 200\text{ mV}\end{aligned}$$

11.2

Explain why g_m falls in Fig. 11.6 as $V_{GS} - V_{TH}$ exceeds 0.5 V.

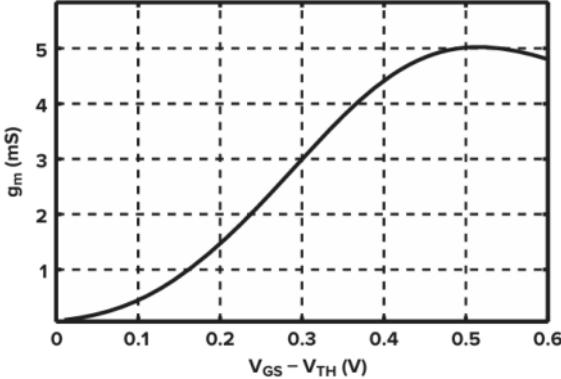


Figure 11.6 Transconductance as a function of overdrive voltage.

Because of mobility degradation with vertical field.

11.3

Suppose a hypothetical transistor exhibits a transconductance given by $g_m = B(V_{GS} - V_{TH})^2$.

(a) Find an expression for I_D as a function of $V_{GS} - V_{TH}$.

(b) Find two other expressions for g_m .

(a) $g_m = \frac{\delta I_D}{\delta V_{GS}} = B(V_{GS} - V_{th})^2$

$I_D = \int g_m = \frac{1}{3}B(V_{GS} - V_{th})^3$

(b) $g_m = \frac{3I_D}{(V_{GS} - V_{th})} = (3I_D)^{\frac{2}{3}} B^{\frac{1}{3}}$

11.4

Sketch the plots in Fig. 11.7 for the device introduced in the previous problem.

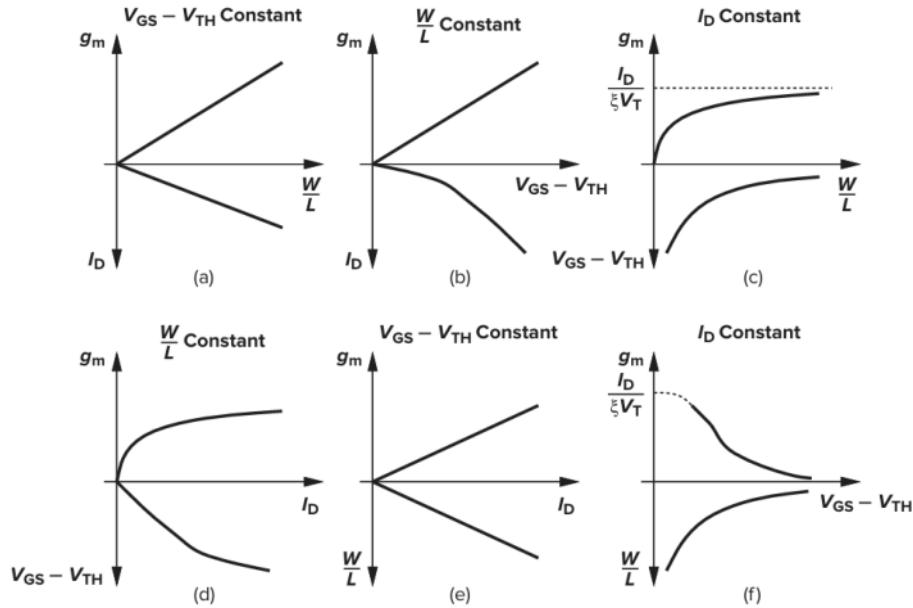


Figure 11.7 Dependence of (a) g_m and I_D upon W/L , (b) g_m and I_D upon $V_{GS} - V_{TH}$, (c) g_m and $V_{GS} - V_{TH}$ upon W/L , (d) g_m and $V_{GS} - V_{TH}$ upon I_D , (e) g_m and W/L upon I_D , and (f) g_m and W/L upon $V_{GS} - V_{TH}$.

Skip

11.5

We wish to bias a transistor with $L = 40\text{nm}$ at $I_D = 0.25\text{mA}$. Referring to Fig. 11.13, determine which case yields a higher output impedance: $W = 5\mu\text{m}$ or $W = 10\mu\text{m}$.

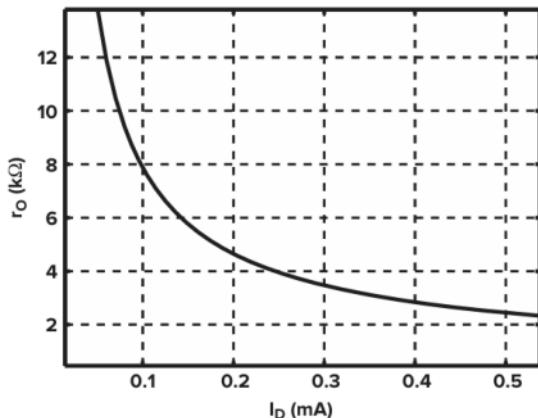


Figure 11.13 Output resistance of a $5\text{-}\mu\text{m}/40\text{-nm}$ NMOS device as a function of drain current.

$$r_o = 4\text{k}\Omega \text{ when } W = 5\mu\text{m}$$

$$r_o = \frac{1}{2}6 = 3\text{k}\Omega \text{ when } W = 10\mu\text{m}$$

11.6

Explain what happens to the unachievable region in Fig. 11.15 if ξ falls from 1.5 to 1.0. Assume that the behavior in strong inversion does not change.

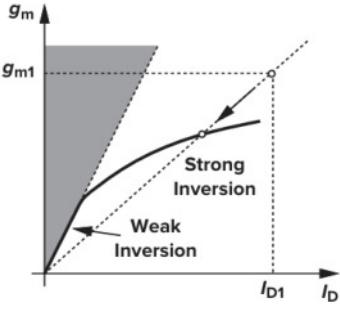


Figure 11.15 Unachievable g_m region.

$$g_m = \frac{I_D}{\xi V_T}$$

The unachievable region decreases if ξ falls from 1.5 to 1.0.

11.7

Modeling the thermal noise of M_6 in Fig. 11.21 by a voltage source in series with its gate, determine the gain that it sees as it reaches node Y. Use the exact expression for the gain of a degenerated CS stage. Compare this result with the thermal noise contributed by M_8 .

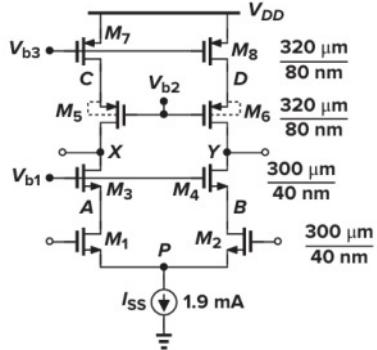


Figure 11.21 First design of telescopic-cascode op amp.

$$A_{v6} = \frac{g_{m6}}{1+g_{m6}r_{o8}} [(1 + g_{m6}r_{o6})r_{o8} || (1 + g_{m4}r_{o4})r_{o2}]$$

$$A_{v8} = g_{m8}R_{out}$$

11.8

Consider the arrangement shown in Fig. 11.24(b). How high can the input CM level be for M_{13} and M_{14} to remain in saturation? Does I_{D11}/I_{D12} increase or decrease beyond this point?

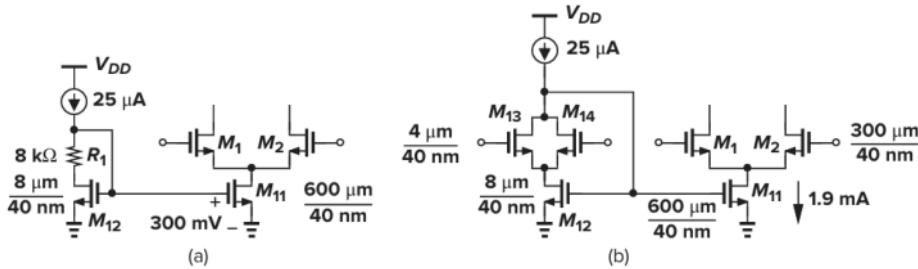


Figure 11.24 (a) Simple and (b) more accurate biasing for tail current source.

$$V_{CM,in} < V_{gs12} + V_{th13}$$

$$I_{D11}/I_{D12} \text{ increases.}$$

11.9

Suppose a closed-loop amplifier exhibits ringing at a frequency f_1 in its step response [as in Fig. 11.46(b)]. Does this provide any information about the phase response of the open-loop circuit?

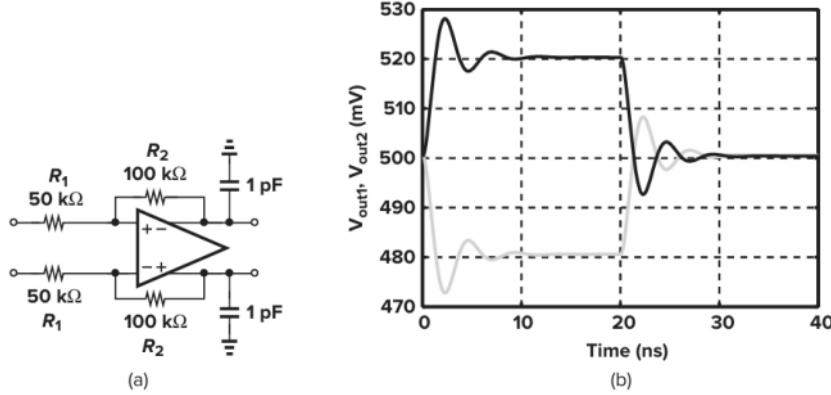


Figure 11.46 (a) Closed-loop amplifier and (b) its step response.

$PM < 60^\circ$

11.10

A two-stage op amp contains a nondominant pole, w_{p2} , at the output and is compensated for $PM = 45^\circ$ so that —BH— drops to unity at w_{p2} . Assume that the dominant pole is much lower than w_{p2} .

(a) Estimate the degradation in PM if the load capacitance seen at the output is doubled.

(b) How should the compensation be modified to ensure that $PM = 45^\circ$ again?

(a) $\arctan(\frac{GBW}{w_{nd}}) = 54.7^\circ$ (b) increase the C_c .

Add a resistor in series.

11.11

Estimate the closed-loop time constant in Fig.11.57 and see if it agrees with the open-loop dominant frequency of 1.7 MHz.

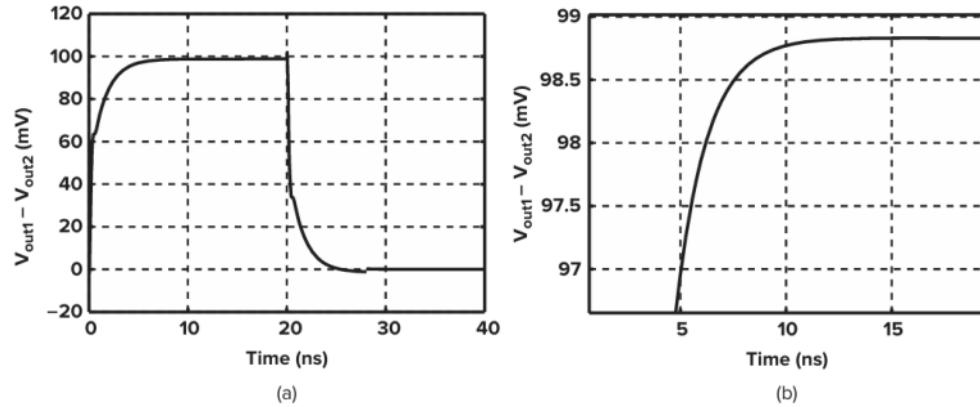


Figure 11.57 (a) Closed-loop step response and (b) close-up showing settling to 1% accuracy.

$$V = 0.1(1 - e^{-t/\tau})$$

$$\tau = \frac{-t}{\ln(1-10V)} = 1.786nS$$

$$f_d = \frac{1}{2\pi\tau} = 89.1MHz$$

11.12

Suppose that in Fig. 11.60, we scale an op amp up by a factor of a . If the load capacitance is constant, how much bandwidth improvement can be achieved?

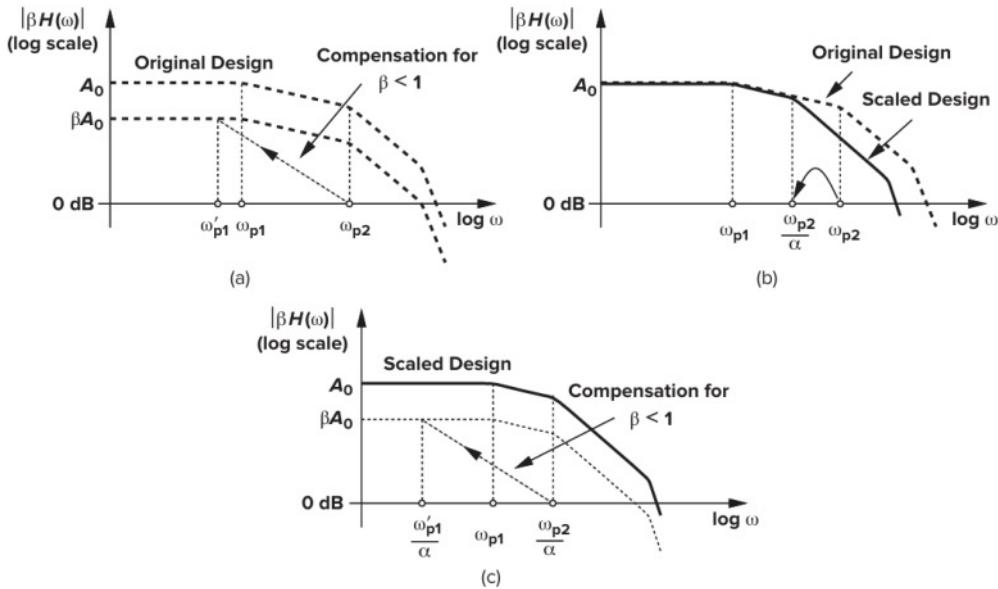
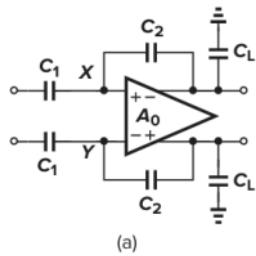


Figure 11.60 (a) Original op amp response and frequency compensation, (b) scaled op amp response, and (c) compensation of scaled op amp.

α

11.13

Modeling the op amp in Fig. 11.51(a) by a voltage-dependent current source equal to GmV_{XY} and an output resistance equal to R_{out} , calculate the zero of the closed-loop transfer function. (Hint: the output voltage is equal to zero at the zero frequency.)

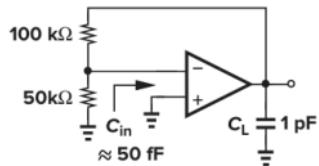


$$V_{xy} s 2C_2 - V_{xy} G_m = 0$$

$$s_z = \frac{G_m}{2C_2}$$

11.14

Consider the situation illustrated in Fig. 11.47(a). Suppose we place a capacitor, C_F , in parallel with the feedback resistor. Prove that C_F introduces a zero in the loop transmission and determine its value so as to cancel the pole created by C_{in} .



$$C_F = \frac{1}{2} C_{in}$$