EE599 ASSIGNMENT 1

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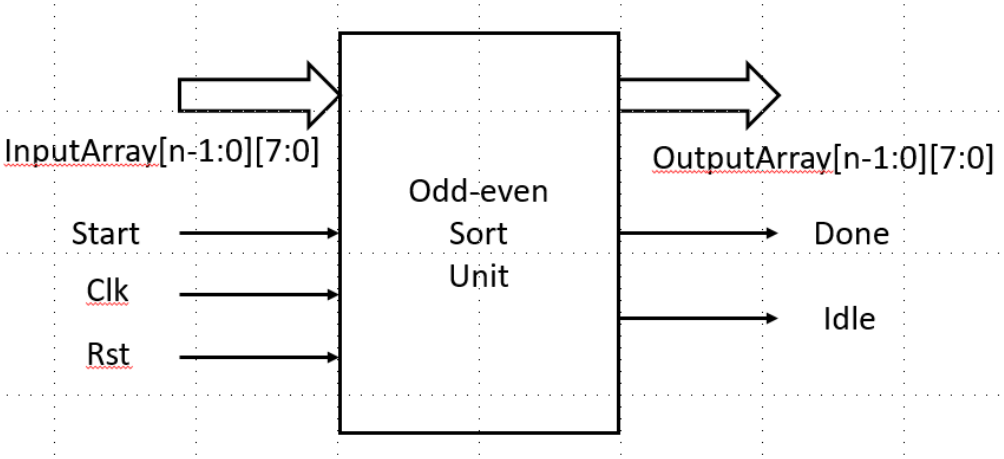
Github: https://github.com/zjjzby/EE599_bingyizh_6838451736

Odd-even transposition sort on FPGA

1. Hardware overview:



Signal	description	Signal	description
InputArray	Input array	OutputArray	Output array
Start	Start signal, assert to start the sort	Clk	Clock
Rst	reset	Done	Will be asserted when finish the sorting
Idle	Indicate whether the Unit is working or not		

2. Hardware parameters:

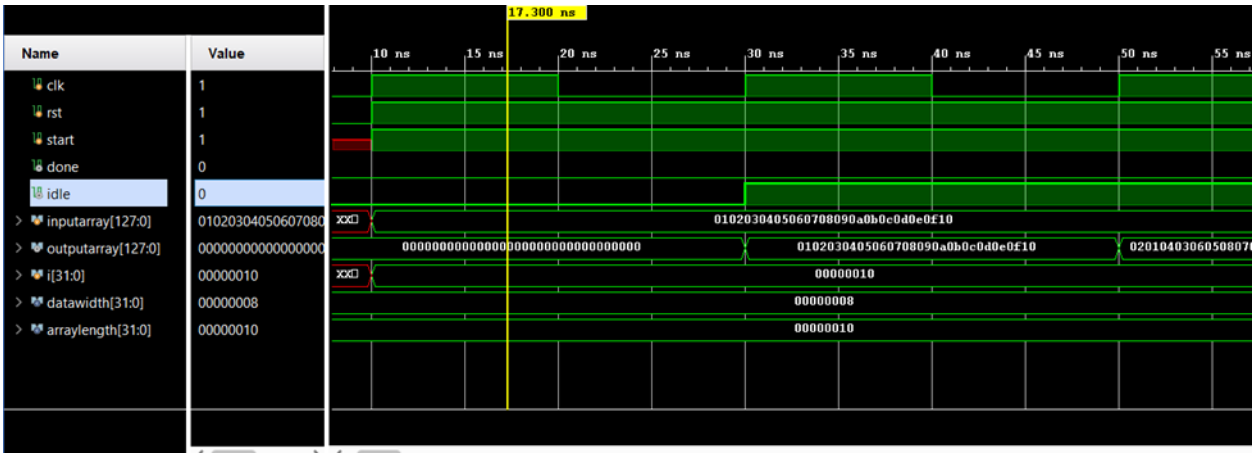
In the design, there are two hardware parameters—**datawidth** and **arraylength. Datawidth** is the width of each element in the array and **arraylength** is the size of the array.

3. Waveform:

DataWidth = 8, Arraylength = 16:

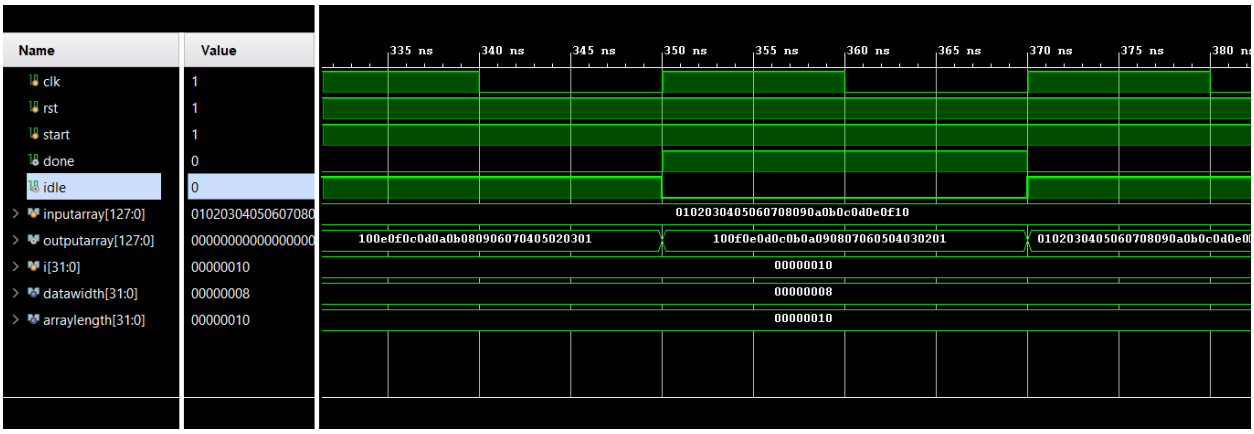
Start:

As indicated in the picture, when start is asserted, the inputarray(0x01_02_03_04-05_06_07_08_09_0c_0d_0e_0f_10) will be loaded to the outputarray(0x01_02_03_04-05_06_07_08_09_0c_0d_0e_0f_10).



Done:

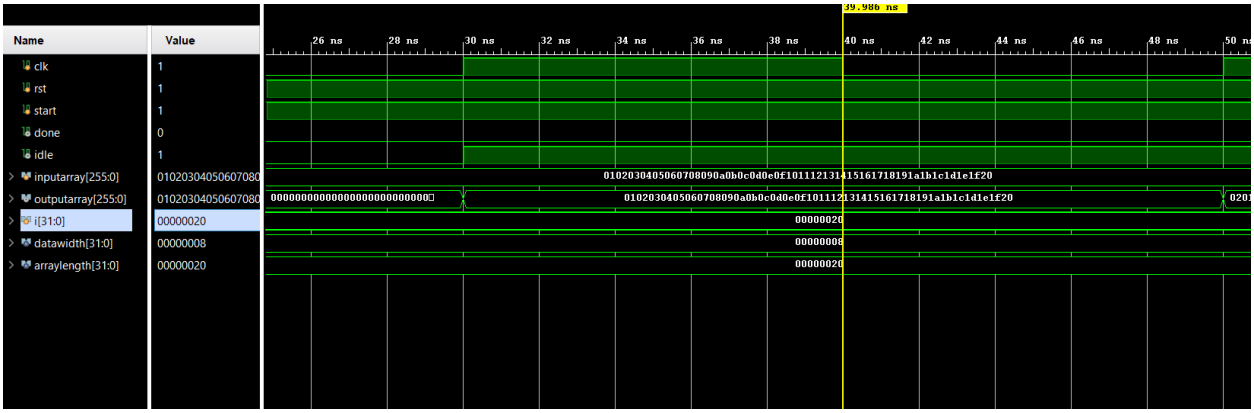
As indicated in the picture, when done is asserted, the sorting is finished. The outputarray contains the result of the sorting (0x10_0f_0e_0d_0c_09_08_07_06_05_04_03_02_01).



DataWidth = 8, Arraylength = 32:

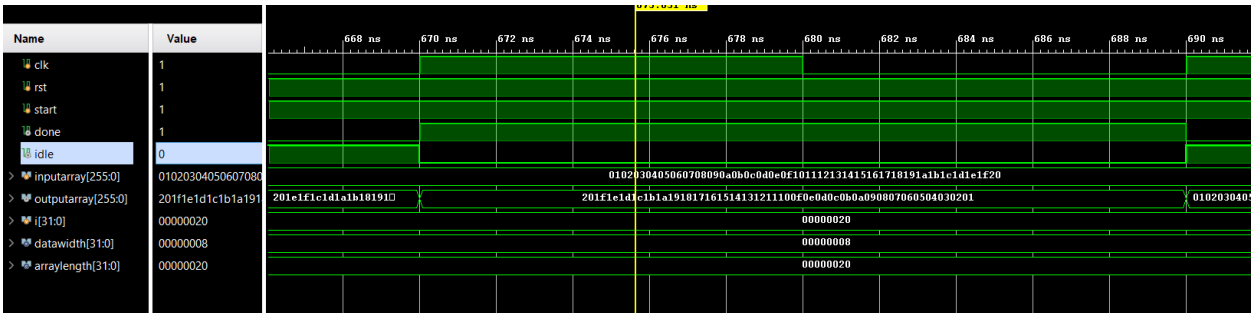
Start:

Explanation is similar to previous waveform.



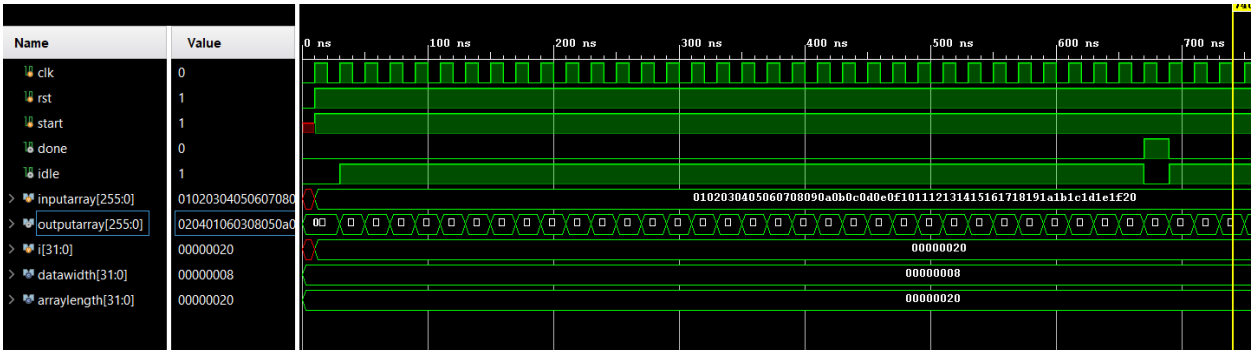
Done:

Explanation is similar to previous waveform.



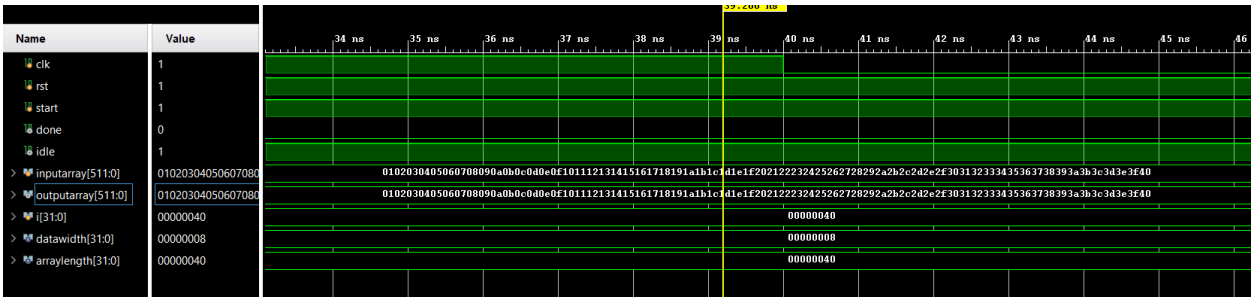
Global:

The waveform from start to done:

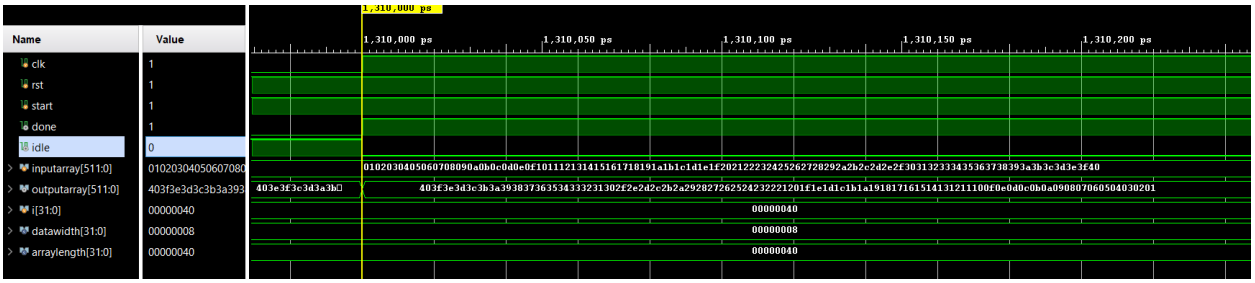


DataWidth = 8, Arraylength = 64:

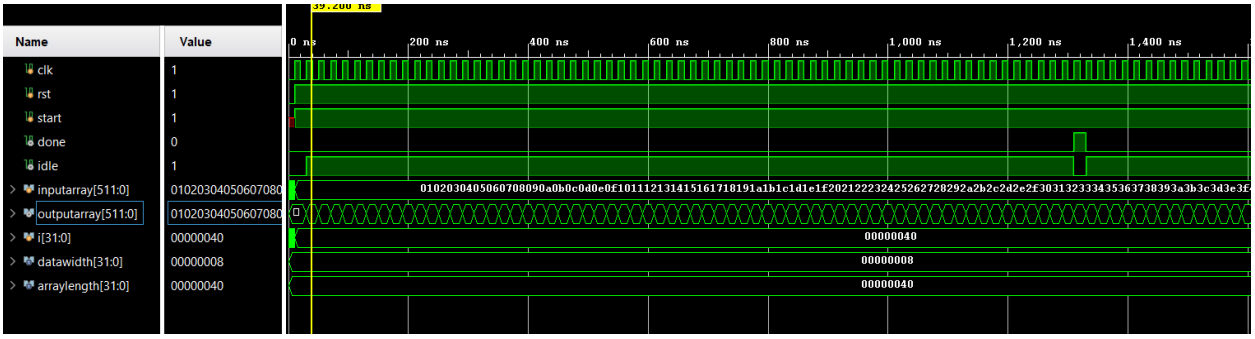
Start:



Done:

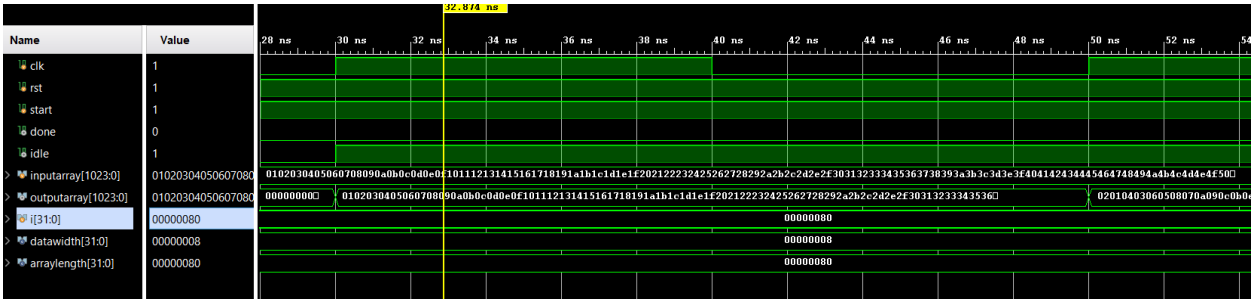


Global:

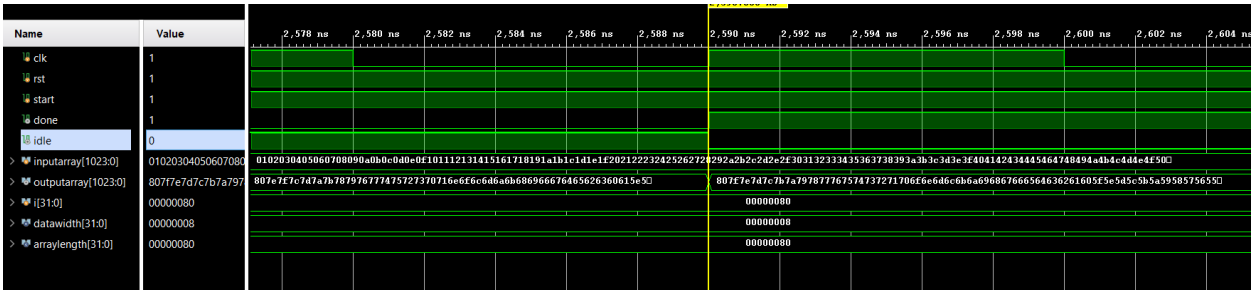


DataWidth = 8, Arraylength = 128:

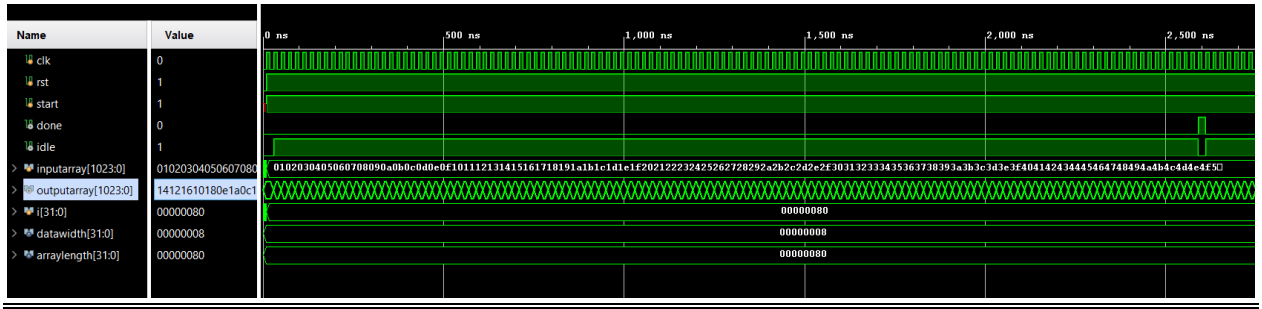
Start:



Done:



Global:



4. Frequency:

I list the maximum achievable frequency of my design. The target FPGA device is **xc7z007sclg225-2.**

Hardware configuration	Minimum Clock Period	Maximum Frequency
DataWidth = 8, Arraylength = 16	4.200 ns	238 MHZ
DataWidth = 8, Arraylength = 32	4.202 ns	238 MHZ
DataWidth = 8, Arraylength = 64	4.202 ns	238 MHZ
DataWidth = 8, Arraylength = 128	4.202 ns	238 MHZ

5. Resource:

The target FPGA device is **xc7z007sclg225-2**. In my design, only LUTs are consumed. So, I only list LUT usage here:

Hardware configuration	LUT usages
DataWidth = 8, Arraylength = 16	360 (3%)
DataWidth = 8, Arraylength = 32	960 (7%)
DataWidth = 8, Arraylength = 64	1800 (13%)
DataWidth = 8, Arraylength = 128	3611(25%)

6. Power:

The target FPGA device is **xc7z007sclg225-2**. The power reports consist of two parts—dynamic power and static power when FPGA achieve maximum frequency 238 MHZ.

Hardware configuration	Dynamic	Static	total
DataWidth = 8, Arraylength = 16	0.321 W	0.099 W	0.42 W
DataWidth = 8, Arraylength = 32	0.683 W	0.110 W	0.793 W
DataWidth = 8, Arraylength = 64	1.373 W	0.142 w	1.515 W
DataWidth = 8, Arraylength = 128	2.782 W	0.301 W	3.83

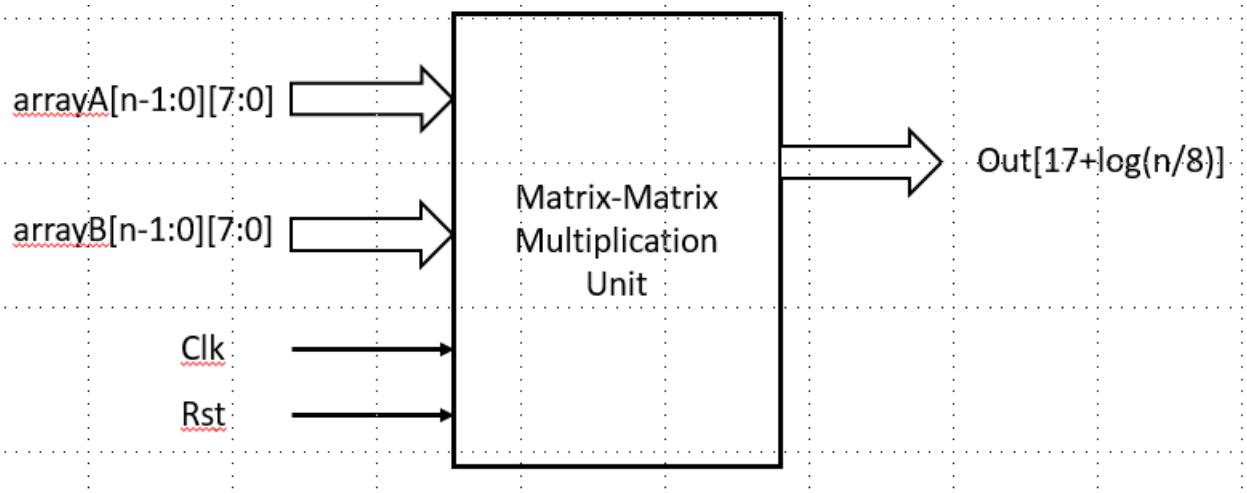
7. Schematic:

The Schematics are attached as pdf files:

Hardware configuration	File name
DataWidth = 8, Arraylength = 16	schematic-odd-even-arraysize16.pdf
DataWidth = 8, Arraylength = 32	schematic-odd-even-arraysize32.pdf
DataWidth = 8, Arraylength = 64	schematic-odd-even-arraysize64.pdf
DataWidth = 8, Arraylength = 128	schematic-odd-even-arraysize128.pdf

Dense Matrix-Matrix Multiplication on FPGA

1. Hardware Overview:



Signal	description	Signal	description
arrayA	Input A, each clock cycle, push a row of A	arrayB	Input B, each clock cycle, push a row of B
Out	Output, every clock cycle will produce a single result	Clk	Clock
Rst	reset		

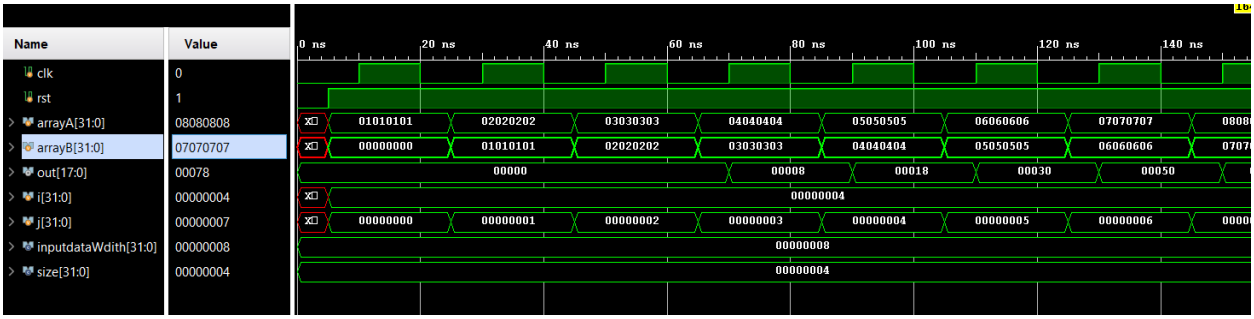
2. Hardware parameters:

In the design, there are two hardware parameters— **inputdataWdith** and **size. inputdataWdith** is the width of each element in the array and **size** is the size of the array.

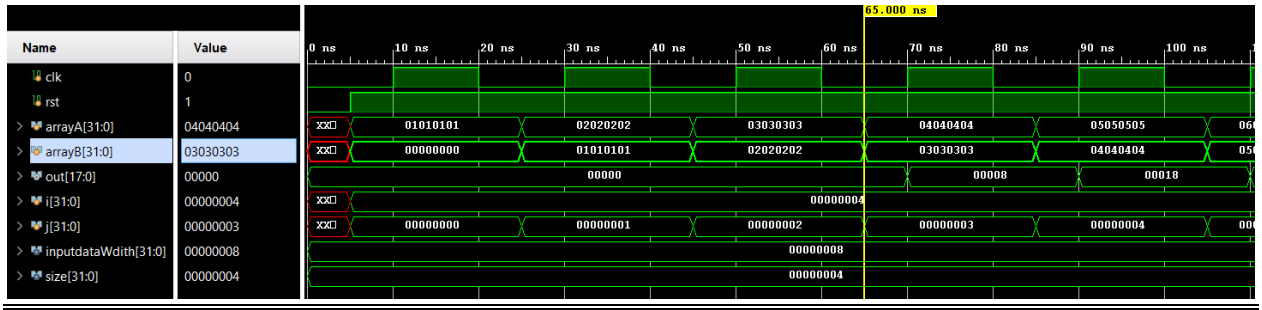
3. Waveform:

4x4 matrix-matrix multiplication:

Global:

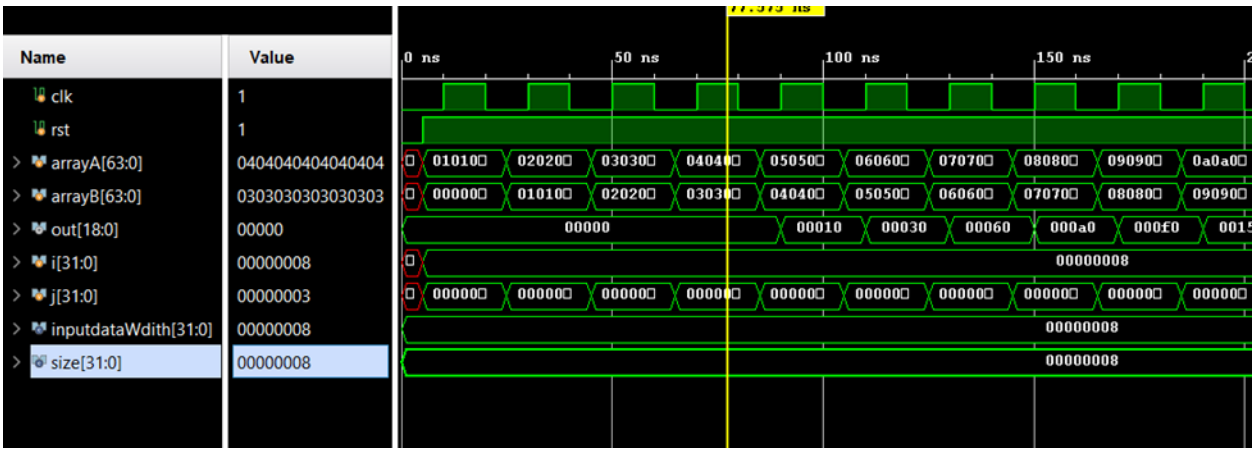


Detail:

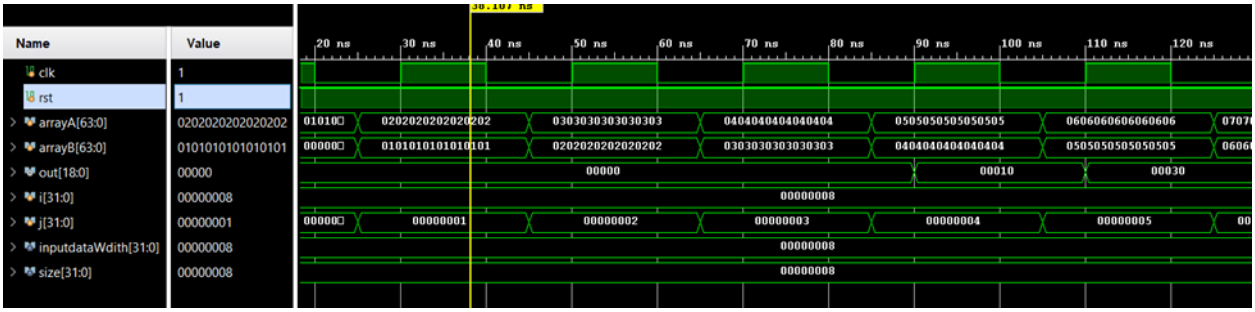


8x8 matrix-matrix multiplication:

Global:

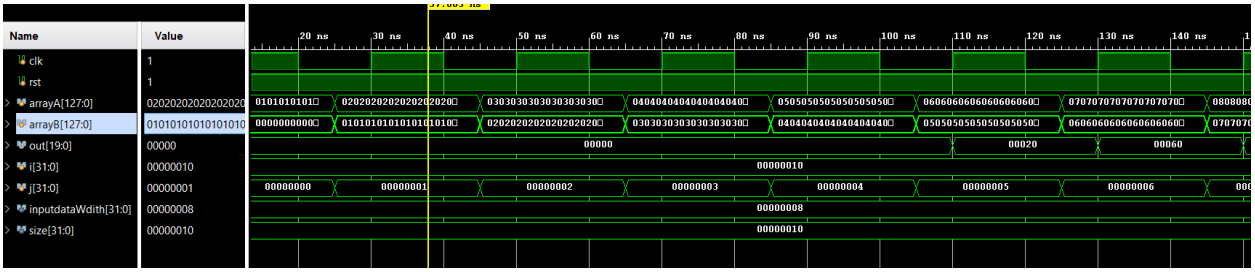


Detail:

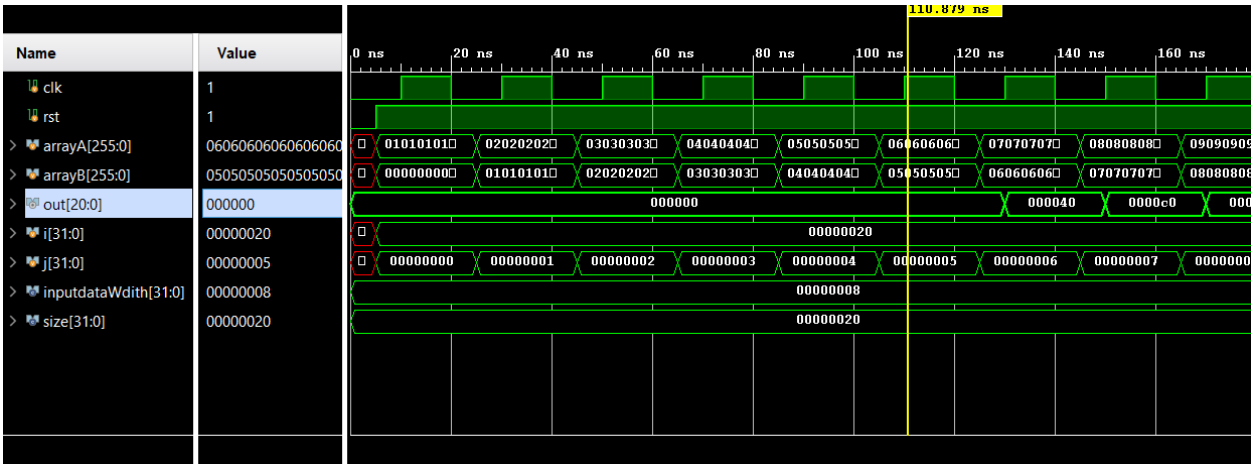


16x16 matrix-matrix multiplication:

Global:



32x32 matrix-matrix multiplication:



4. Frequency:

I list the maximum achievable frequency of my design. The target FPGA device is **xc7z007sclg225-2.**

Hardware configuration	Minimum Clock Period	Maximum Frequency
inputdataWdith = 8, size = 4	2.351 ns	425 MHZ

inputdataWdith = 8, size = 8	2.370 ns	422 MHZ
inputdataWdith = 8, size = 16	2.401 ns	416 MHZ
inputdataWdith = 8, size = 32	2.449 ns	408 MHZ

5. Resource:

The target FPGA device is **xc7z007sclg225-2**. In my design, only LUTs are consumed. So, I only list LUT usage here:

Hardware configuration	LUT usages
inputdataWdith = 8, size = 4	335 (2%)
inputdataWdith = 8, size = 8	686 (5%)
inputdataWdith = 8, size = 16	1388 (10%)
inputdataWdith = 8, size = 32	2796 (19%)

6. Power:

The target FPGA device is **xc7z007sclg225-2**. The power reports consist of two parts—dynamic power and static power when FPGA achieve maximum frequency 238 MHZ.

Hardware configuration	Dynamic	Static	total
inputdataWdith = 8, size = 4	0.122 W	0.093 W	0.215 W
inputdataWdith = 8, size = 8	0.165 W	0.093 W	0.258 W
inputdataWdith = 8, size = 16	0.237 W	0.094 w	0.331 W
inputdataWdith = 8, size = 32	0.400 W	0.096 W	0.496 W

7. Schematic:

The Schematics are attached as pdf files:

Hardware configuration	File name
inputdataWdith = 8, size = 4	schematic-MMM-size4x4.pdf
inputdataWdith = 8, size = 8	schematic-MMM-size8x8.pdf
inputdataWdith = 8, size = 16	schematic-MMM-size16x16.pdf
inputdataWdith = 8, size = 32	schematic-MMM-size32x32.pdf