EE599 ASSIGNMENT 2

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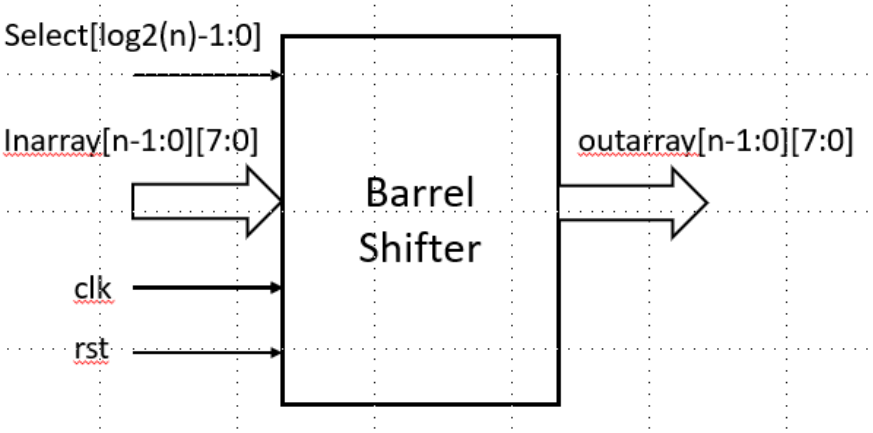
Github: https://github.com/zjjzby/EE599_bingyizh_6838451736

Barrel Shifter

1. Hardware overview:



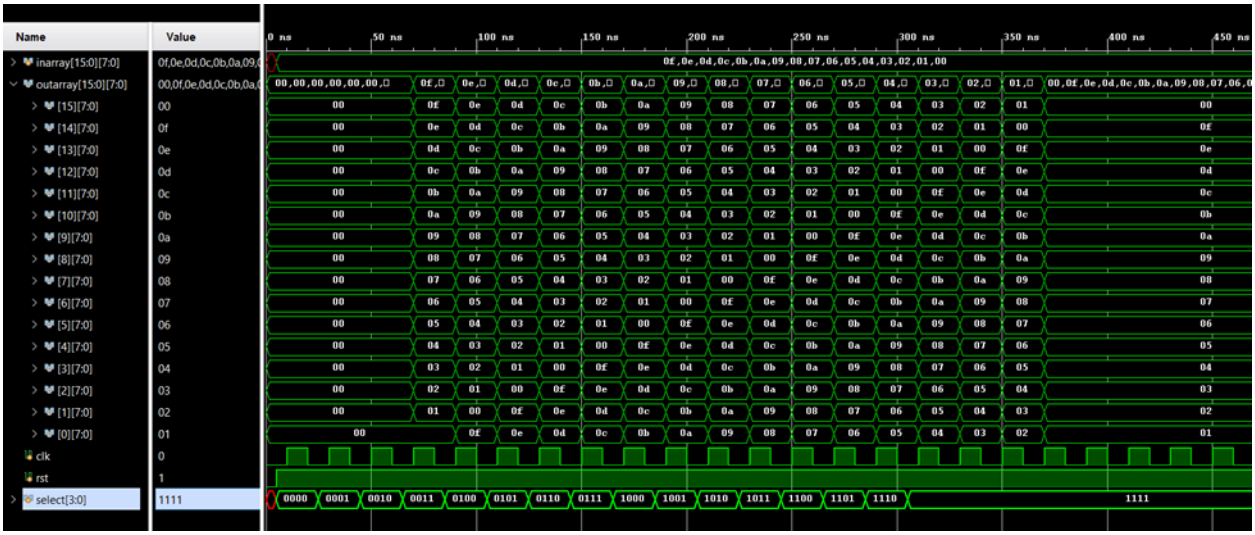
Signal	description	Signal	description
Inarray	Input array	outarray	Output array
Select	select signal, shift selection	Clk	Clock
Rst	reset		

Source file	description
barrel_shfiter/barrelshifer.v	Top module in the hardware design
barrel_shfiter/ mux.v	Two to one multiplexor
barrel_shfiter/ testbench.v	Testbench file

Hardware parameters	Description
size	The size of the input array
datawidth	The width of the element in the array

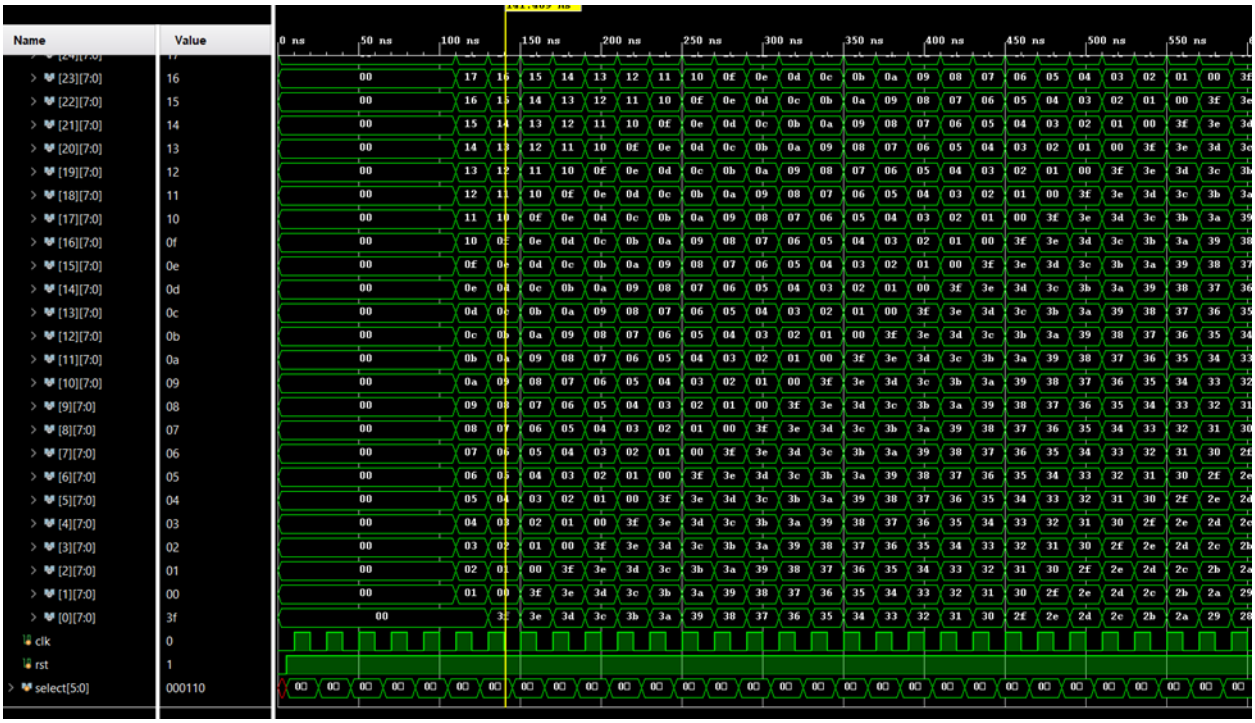
2. Ware form

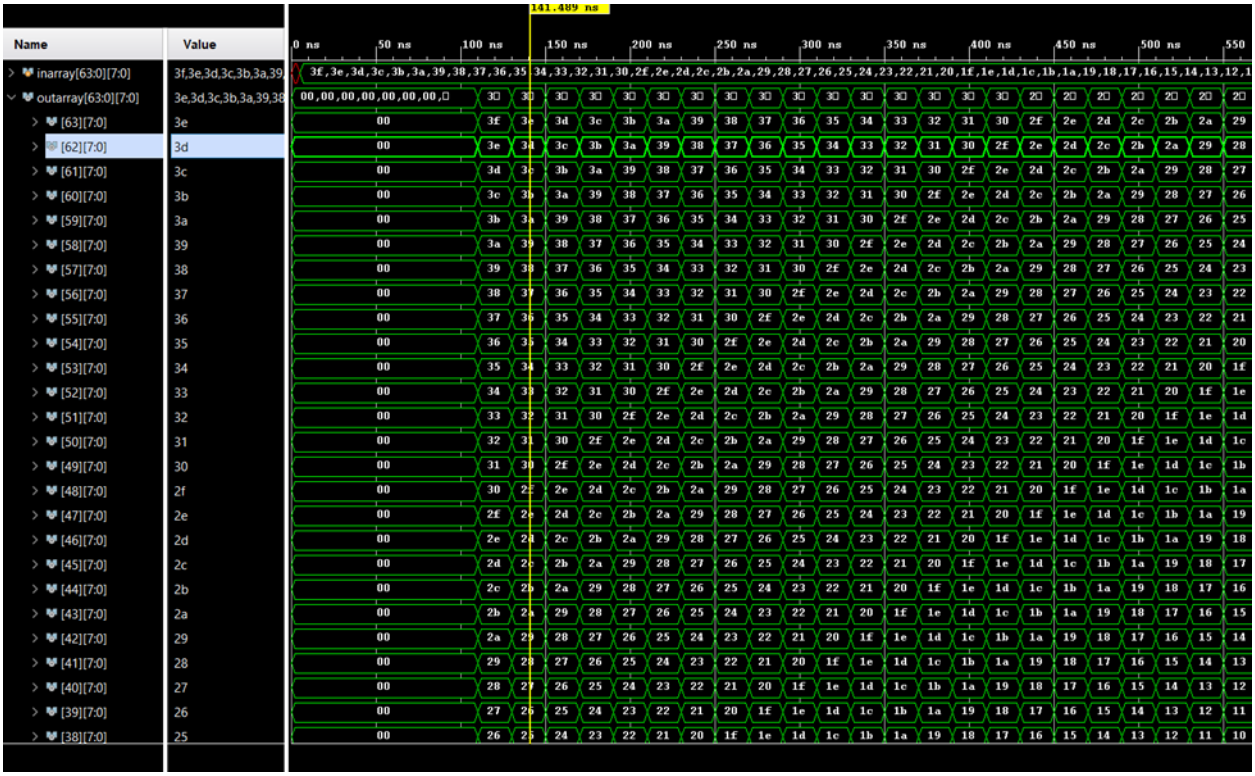
Size=16, datawidth=8



As indicated in the waveform, the input array is set to: $0f, 0e, 0d, 0c, 0b, 0a$, 09,08,07,06,05,04,03,02,01,00 For: $inarray[15], inarray[14] \ldots, inarray[2], inarray[1], inarray[0]$ Respectively. The select signal do one increments for every clock cycle. The output will shift for corresponding locations after 4 clock cycle delay.

Size=64, datawidth=8





3. Frequency:

I list the maximum achievable frequency of my design. The target FPGA device is **xc7z007sclg225-2.**

Hardware configuration	Minimum Clock Period	Maximum Frequency
Size=16, datawidth=8	1.391 ns	719 MHZ
Size=64, datawidth=8	1.435 ns	697 MHZ

4. Resource:

The target FPGA device is **xc7z007sclg225-2**. In my design, only LUTs are consumed. So, I only list LUT usage here:

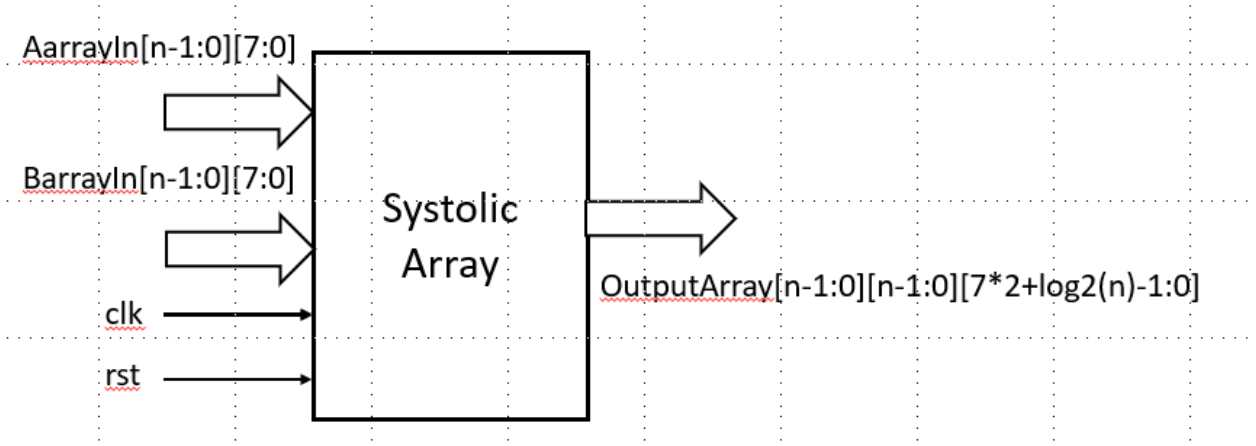
Hardware configuration	LUT usages
Size=16, datawidth=8	257 (2%)
Size=64, datawidth=8	1541 (11%)

5. schematic

Hardware configuration	File name
Size=16, datawidth=8	barrelShiftSchematicN16.pdf
Size=64, datawidth=8	barrelShiftSchematicN64

Systolic Array

6. Hardware overview



Signal	description	Signal	description
AarrayIn	Input array A	OutputArray	Output array
BarrayIn	Input array B	Clk	Clock
Rst	reset		

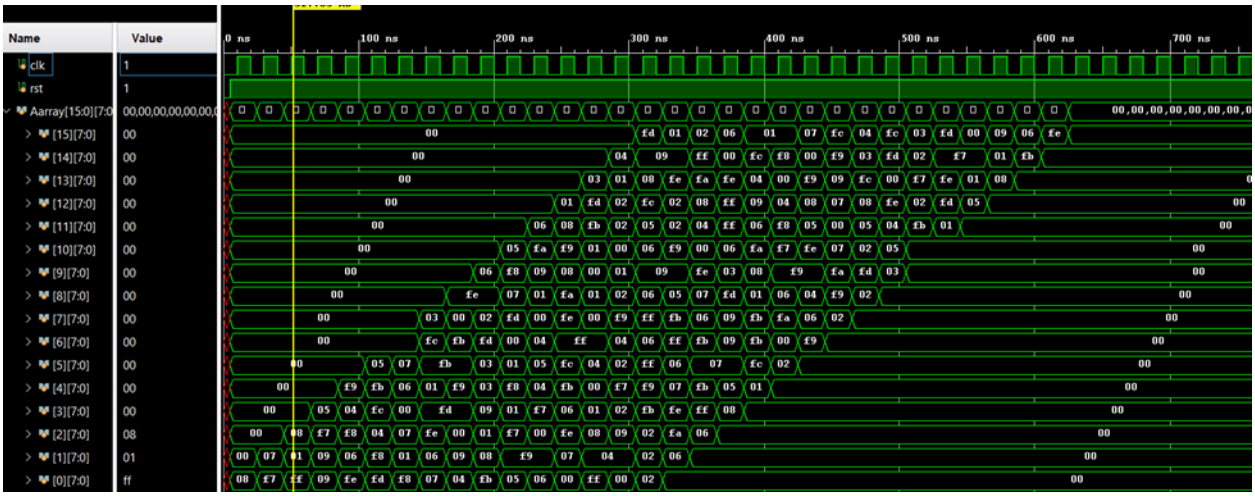
Source file	description
systolicArray/systolicArray.v	Top module in the hardware design
systolicArray/sysUnit.v	One processing element in systolic array
systolicArray/ testbench.v	Testbench file

Hardware parameters	Description
size	The size of the systolic array
datawidth	The width of the element in the array

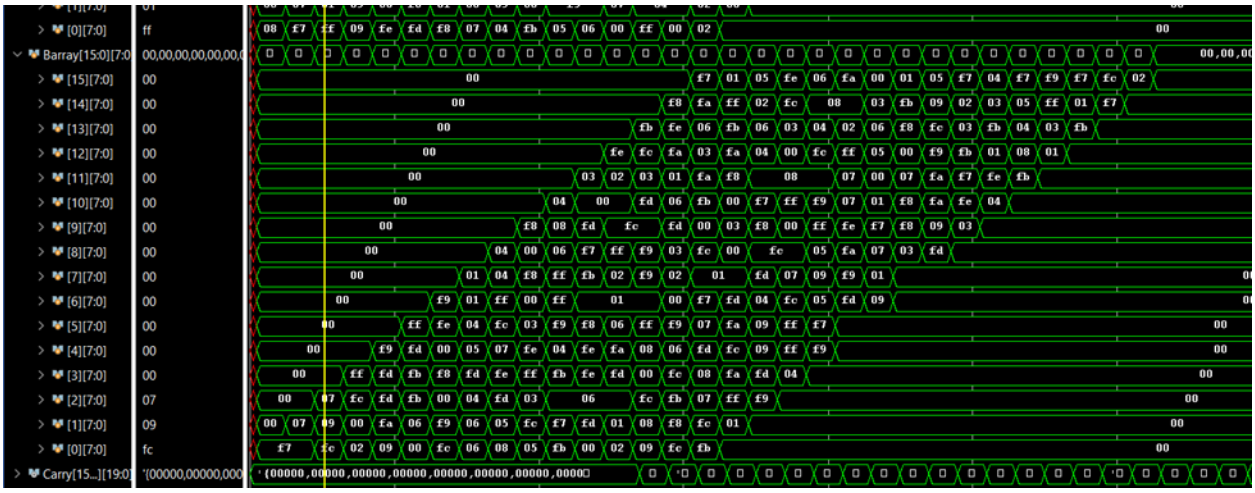
7. Ware form

Size=16, datawidth=8

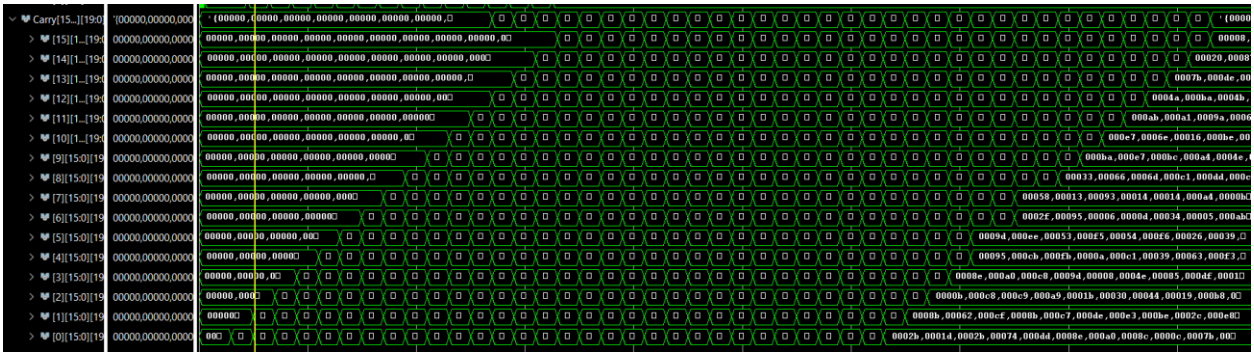
Input array A:

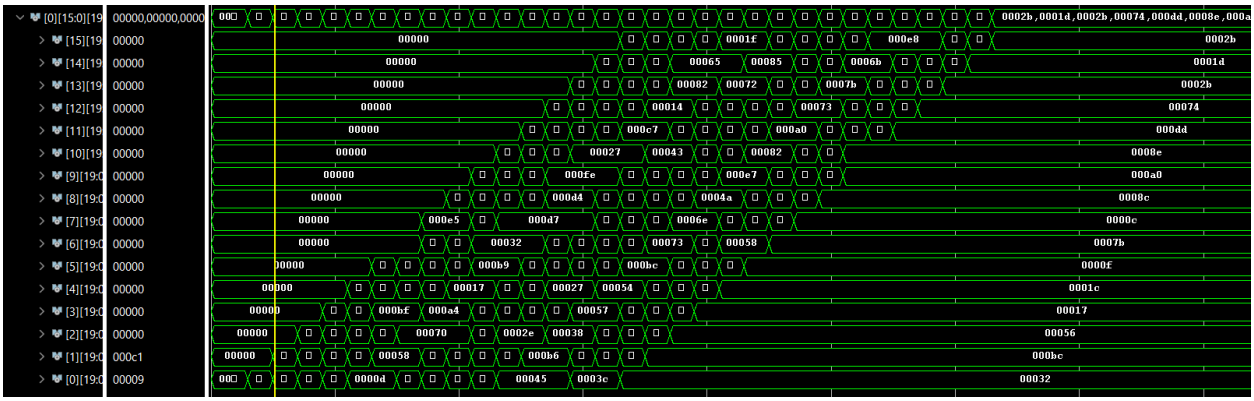


Input array B:



Output array C:





8. Frequency:

I list the maximum achievable frequency of my design. The target FPGA device is **xc7z007sclg225-2.**

Hardware configuration	Minimum Clock Period	Maximum Frequency
Size=16, datawidth=8	4.079 ns	245 MHZ
Size=64, datawidth=8	4.098 ns	244 MHZ

9. Resource:

The target FPGA device is **xc7z007sclg225-2**. In my design, only LUTs are consumed. So, I only list LUT usage here:

Hardware configuration	LUT usages
Size=16, datawidth=8	11008 (76%)
Size=64, datawidth=8	45056 (>100%)

10. schematic

Hardware configuration	File name
Size=16, datawidth=8	systolicArraySchematic16x16.pdf
Size=64, datawidth=8	systolicArraySchematic32x32.pdf