UIC COLLEGE OF ENGINEERING
UNIVERSITY OF ILLINOIS AT CHICAGO
Department of Electrical and Computer Engineering

# Advanced Digital System Design
# ECE 594 - Online Offering – Spring 2018
# Midterm Exam

Zainalabedin Navabi: navabi@uic.edu

**Detailed Description:**

1.A circuit has two 8-bit inputs a and b. A counter counts the number times that in more than 5 consecutive clock pulses a and b are different (for example if two inputs are different for 5+n consecutive cycles the counter should count n times). Design this circuit using a counter and basic logic gates and flip-flops. The counting is modulo-16 and it rolls back to 0 after it reaches 15. Provide an asynchronous reset input that resets the sequence detection and the counting. A. Show the complete datapath and controller state diagram of this circuit. B. Write VHDL code for the design. C. Write a comprehensive testbench and verify the circuit of Part B.

2. A circuit for finding address of a target value in memory blocks is to be designed (The memory has 8-bit address and 8-bit data). After a complete positive pulse appears on go, the circuit reads the 8-bit target value from its target input bus. The circuit starts searching for target data in the memory by starting from the first address until it reaches the target. When target data is reached address of corresponding memory block is put on 8-bit output of the circuit (address). A pulse on the done signal indicates that the output is ready. found output signal shows whether the target value was found or not (In other words it shows whether the address output is valid or not) A. Show the complete datapath and controller state diagram of this circuit. B. Write VHDL code for the design. C. Write a comprehensive testbench and verify the circuit of Part B.

3. In this part you are to design a frequency multiplier. A frequency multiplier takes an input signal (inSig with frequency f) and multiplies its frequency by a value determined by multiplication factor (MultFactor). The output is a signal (outSig) with a frequency equal to f*MultFactor. Multiplication factor is a power of two and could be shown as 2n, where n is between 2 and 5. Therefore, the circuit takes as the input value. For example if MultFactor is 8, the corresponding input value would be 3. f range is between 64 KHz and 1 MHz. A reference clock input is used for the reference working clock of this circuit and is provided via an input named RefClk, with a frequency of 64 MHz. The circuit has a valid output that is asserted when frequency multiplication is taking place and output is appearing on outSig. When a positive pulse appears on adjust, the circuit is informed of a new multiplication factor, and begins preparation for the multiplication process with this new factor. While this preparation is taking place, valid becomes 0 and remains 0 until preparation is complete, at which time the generated outSig signal frequency represents the multiplied frequency. A) Show the complete datapath, including the components and necessary internal signals. B) Draw a state diagram that shows

the behavior of your controller and issuance of control signals. C) Show wiring between the datapath and the controller.

Deliverables:

1. All VHDL codes

2. A complete report illustrating all your observations, simulation results, and required waveforms.