UIC COLLEGE OF ENGINEERING
UNIVERSITY OF ILLINOIS AT CHICAGO
Department of Electrical and Computer Engineering

Advanced Digital System Design
ECE 594-Online Offering-Spring 2018
Assignment3- Due date: March 5

In this assignment, you are to design a circuit that has two input ports: data (8-bit) and reset (1-bit) and one 4-bit output port. After a complete synchronous pulse on reset, in the next eight clocks, the circuit receives eight bytes of data on the data port on every rising edge of clock. There is a module which calculates number of 1s for each received input. The output of this circuit should be maximum number of 1s between all 8 inputs (As the maximum value of output is 8, 4 bits is enough for it).

A. Show the complete datapath and controller state diagram of this circuit.

B. Write VHDL code for the design.

C. Write a comprehensive testbench and verify the circuit of Part B

Deliverables:

1.All VHDL codes

2.A complete report illustrating all your observations, simulation results, and required waveforms.