UIC COLLEGE OF ENGINEERING
UNIVERSITY OF ILLINOIS AT CHICAGO
Department of Electrical and Computer Engineering

Advanced Digital System Design
ECE 594-Online Offering-Spring 2018
Assignment5- Due date: April 10

In this assignment you are to design an RTL circuit to calculate an arithmetic operation. This circuit should be able to calculate the approximate value of exp(x) based on its Tailor expansion. Taylor series is one of a well-known methods to compute mathematical functions. Series of this function is shown below.

$$e^x = \sum_{k=0}^{\infty} \frac{x^k}{k!}$$

The following algorithm can be used to approximate e^x :

```
e = 1;
a = 1;
for( i = 1; i  < n; i++ ) {
   a = a * x * ( 1  / i );
   e = e + a;
}
```

Figure 1 shows block diagram of a circuit that approximates e^x . Module exp accepts a 16-bit fixed-point value on x after start is asserted. After that, computation is started. During the computation, busy signal is asserted. After the completion of the computation the result is available on outputs which are 2-bit IntegerPart and 16-bit FractionalPart and busy is deactivated. Assume $0 \leq x < 1$. All numbers are represented as fixed-point numbers (Value 1 is approximated by 0.1111111111111111 in 16-bit fixed point format.). Moreover values of term (1/i) for $1 \leq i < n$ have been computed before and stored in a computational table.

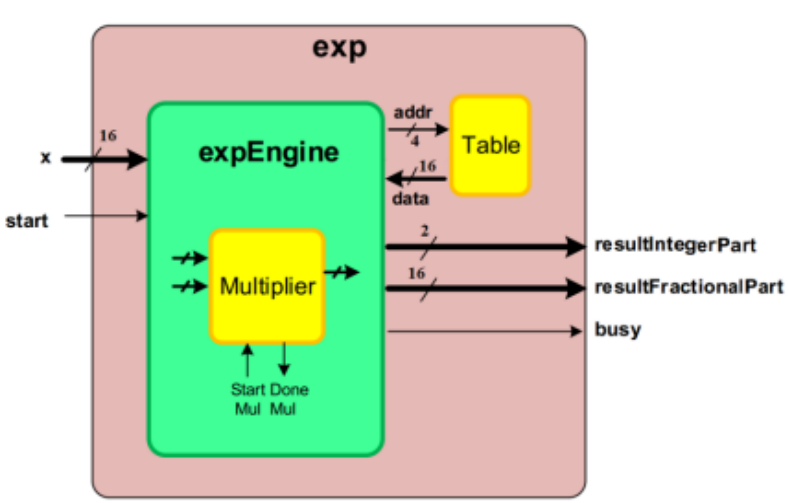

Figure 1. Block diagram of module *exp*

(A)Write an array multiplier that has a start and done signal to control its operation. You should use this multiplier in the exp module.

(B) Show datapath of Module exp(x).

(C) Show the state diagram of the controller of Module exp(x).

(D)Write a synthesizable VHDL description for module exp(x).

(E) Write a high-level VHDL description for Module Table (with 4-bit address and 16-bit data).

(F) Write a comprehensive testbench and verify the complete system.

Deliverables:

1. All VHDL codes.
2. A complete report illustrating all your observations, simulation results, and required waveforms.