**Final Exam**

1.

For solution, please see attached PDF “FinalProblem1ZP”, which includes the data path and state diagram on separate pages.

2.

A) Please see attached PDF “FinalProblem2ZP” page 1 for Data Path.

B) Please see attached PDF “FinalProblem2ZP” page 1 for control signals.

C) Please see attached PDF “FinalProblem2ZP” page 2 for state diagram.

D) Please see attached code for VHDL.

E) Please see attached test bench.

3.

This test is designed in such a way that we get an erroneous output at W given our input number.

