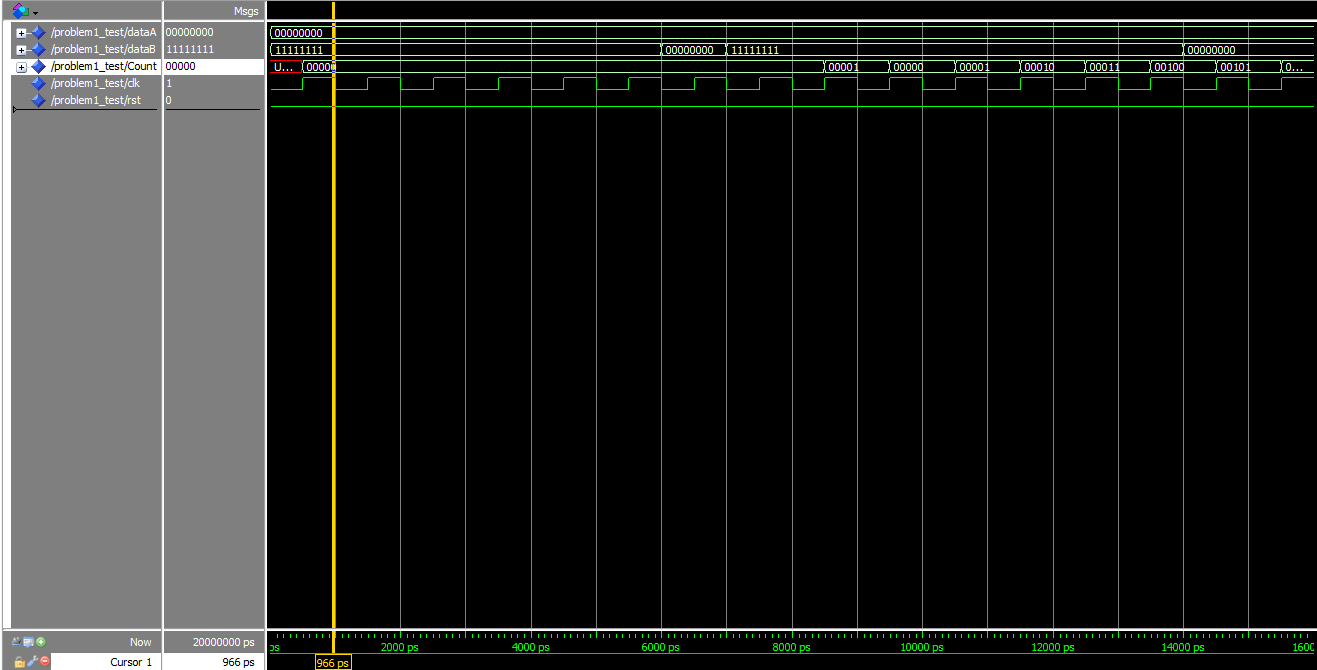
**Problem 1**

Data Path:





Simulated Waveform:



**Problem 2**

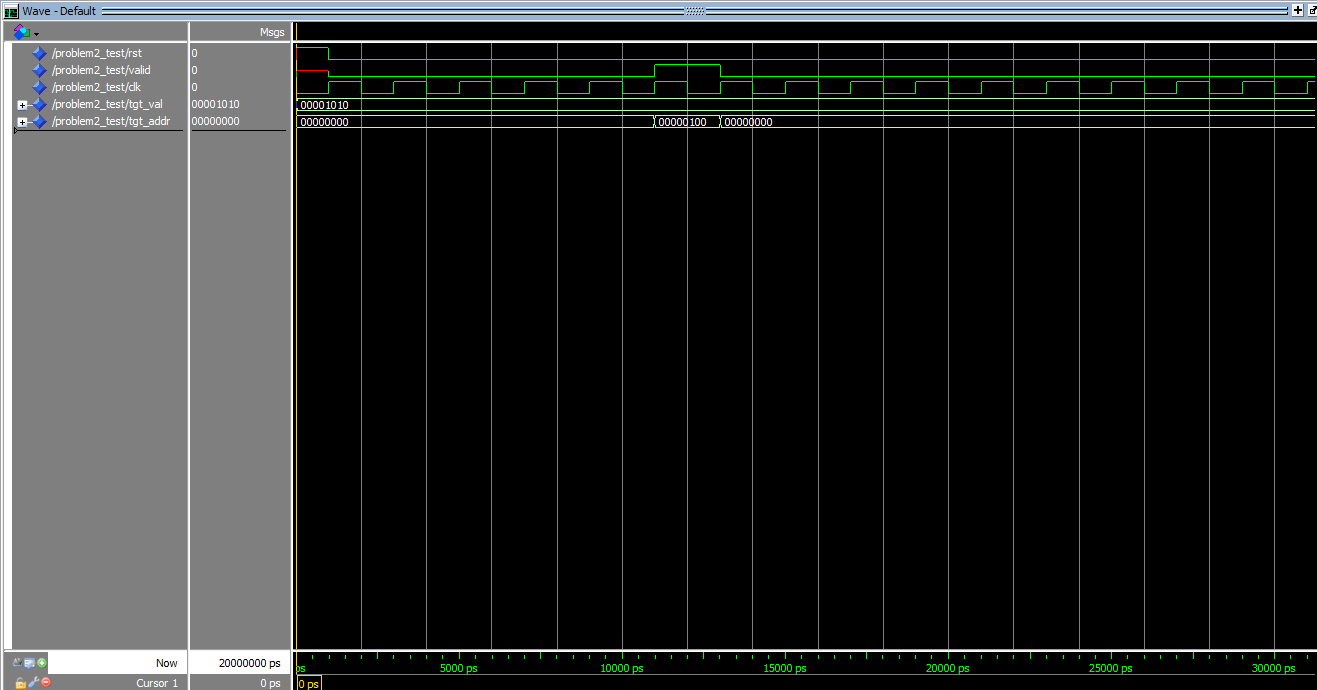
Data Path:



State Diagram:



Waveform output:



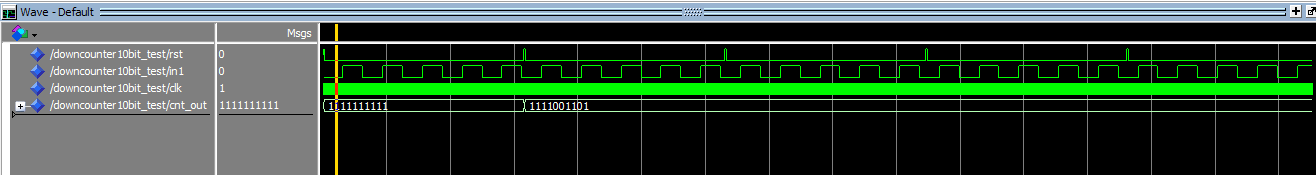
**Problem 3:**

Data Path:

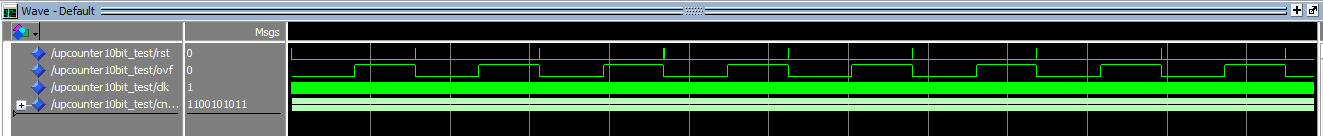


Despite my best efforts, I have been unable to make this problem come together. Each of my components functions the way I would expect, but then in the final design they don’t seem to work. Here is each part tested separately:

Down Counter (testing to see if output changes correctly on input freq change):

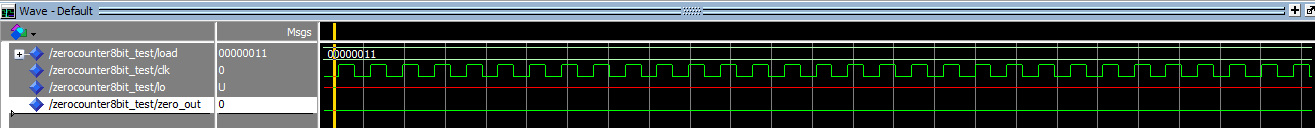


Up Counter (Testing to see correct timing loop and overflow output):



Zero Counter:

This counter is not feeding back properly. I have tried buffers, inout and various signal arrangements, but to no avail.



Problem 3:



Here we can see the first few parts working, but the zero counter never triggers and thus never outputs a freq.