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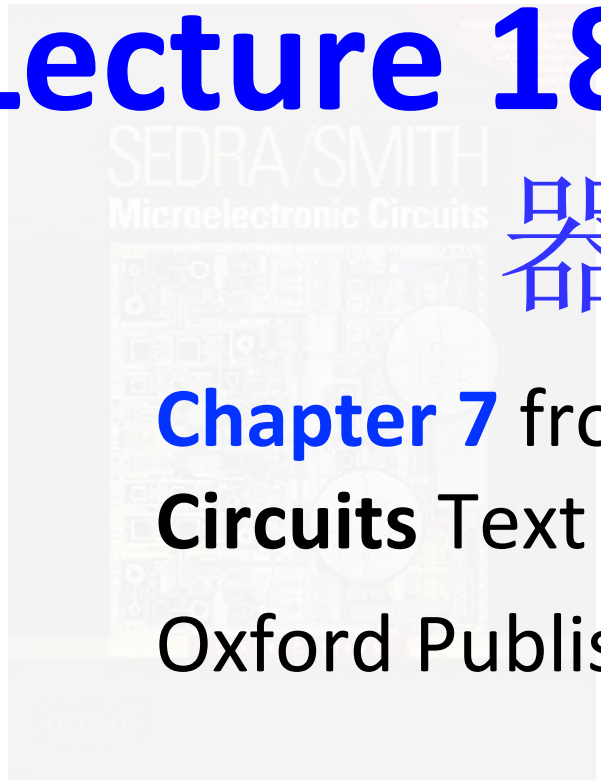
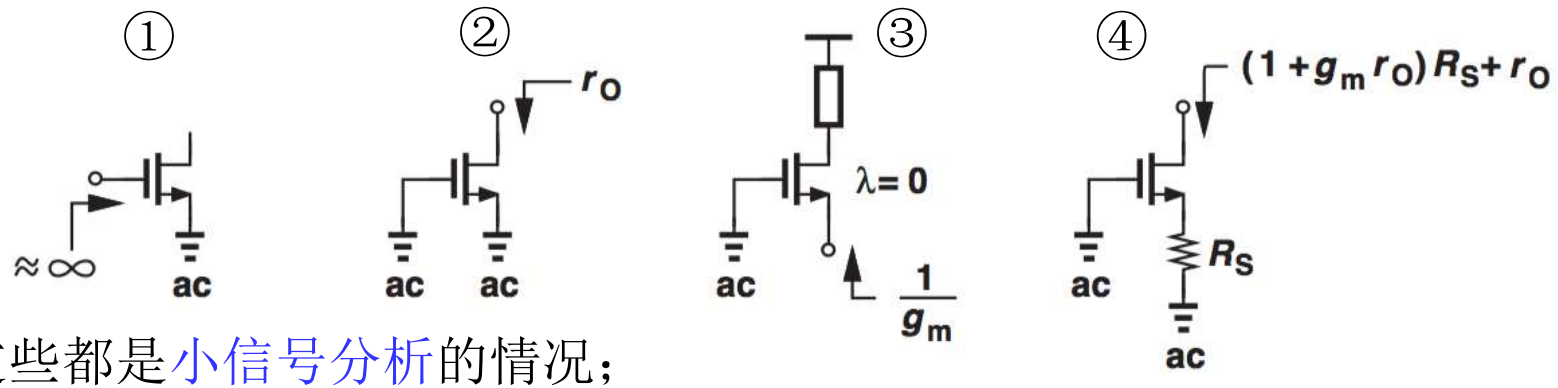
Lecture 18 – 晶体管放大器-part3



Chapter 7 from **Microelectronic Circuits** Text by Sedra and Smith

Oxford Publishing

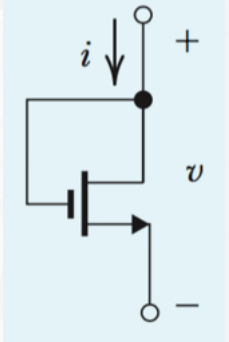
培养电路直觉的Building Blocks

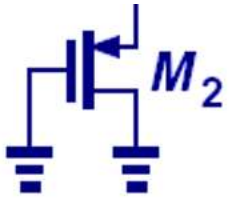


1. 这些都是小信号分析的情况；
2. 要逐渐习惯于从电路中某一点，向左、向右，或向上、向下看的阻抗
3. 计算输出阻抗时，输入信号 v_i 置零，所以图中的ac地，有可能是真正的ac地，也有可能是 v_i 输入端
4. ① 从 G 端向 MOS 管看的阻抗始终为∞；【因为有SiO_2绝缘, i_G=0】
5. ② G 和 S 都接地时，从 D 端向 MOS 管看的阻抗为 r_o；【因为信号都是从 G 或 S 端输入的（改变 v_{GS}），所以从 D 端向MOS管看阻抗时，均为计算电路的输出阻抗；计算输出阻抗时输入信号 v_i 要置零；所以②既适用于 CS（S 接地，v_i 接 G），也适用于 CG（G 接地，v_i 接 S）】
6. ③ G 端接地，从 S 端向MOS管看的阻抗为 $1/g_m$【与 D 端所接的负载无关; CG 的输入阻抗，或 CD，v_i 接 G 时，从 S 看向 MOS管的输出阻抗】
7. ④ Source degeneration 结构的主要作用：大幅提高输出阻抗→更接近于理想电流源，提高的增量为 S 端串接的电阻 R_S 放大（$1+g_m r_o$）倍；也可以看成 CG 结构（考虑信号源内阻时）的输出阻抗值

培养电路直觉的Building Blocks

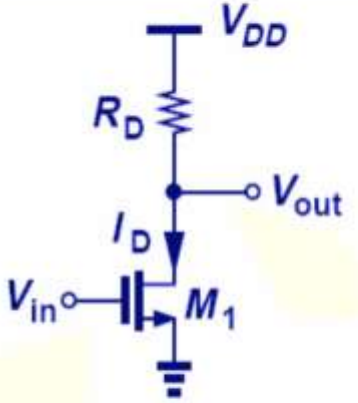
1. Diode-connected 结构（G 和 D 直接相连），小信号分析时等效为阻值 $1/g_m$ 的电阻；





培养电路直觉的Building Blocks

CS

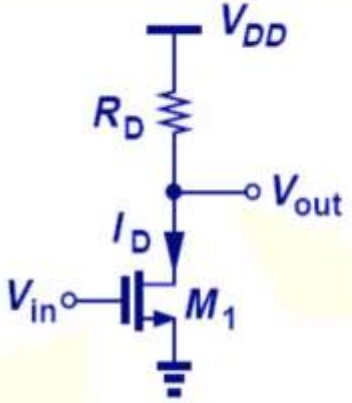
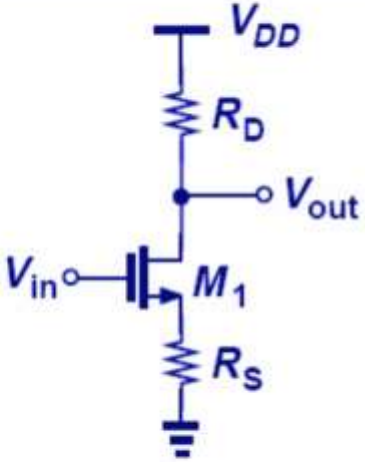


$$A_v = -g_m(R_D \| r_O)$$

$$R_{in} = \infty$$
$$R_{out} = R_D \| r_O$$

1. 输出阻抗：D 端到 ac 地的总电阻（向下看为 r_o 到地，向上看为 R_D 到地）
2. 增益：$-g_m \times$（D 端到 ac 地的总电阻）
3. 输入阻抗：∞

培养电路直觉的Building Blocks

CS	CS Deg
	
$A_v = -g_m(R_D \parallel r_O)$ $R_{in} = \infty$ $R_{out} = R_D \parallel r_O$	$A_v = -\dfrac{R_D}{\dfrac{1}{g_m} + R_S}$ $R_{in} = \infty$ $R_{out} = [(1 + g_m r_O)R_S + r_O] \square R_D$

1. 输出阻抗：D端到ac地的总电阻（向下看为 source degeneration 结构，到ac地的电阻为 $r_o + (1+g_m r_o) R_S$，向上看为 R_D 到地）

2. 增益：

$$A_v = -\frac{D\text{端到ac地的总电阻}}{\frac{1}{g_m} + R_S}$$

$$= -\frac{\text{res tied from “D” to ac GND}}{\frac{1}{g_m} + \text{res tied from “S” to ac GND}}$$

3. 输入阻抗：∞

培养电路直觉的Building Blocks

1. 输出阻抗：D 端到 ac 地的总电阻
   ①考虑信号源内阻R_S【向下看与 source degeneration 结构一致，到 ac 地的电阻为 $r_o+(1+g_m r_o)R_S$】
   ②不考虑信号源内阻R_S【向下看到 ac 地的电阻为 r_o】
   ③向上看均为 R_D 到地）

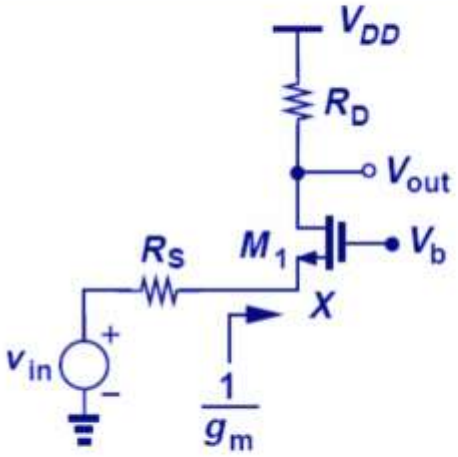
2. 增益：
   ①考虑信号源内阻R_S

$$A_v = \frac{D端到ac地的总电阻}{\frac{1}{g_m} + R_S}$$

   ②不考虑信号源内阻R_S，即**从X点到 V_{out}** 的电压增益
   g_m×（D 端到 ac 地的总电阻）

3. 输入阻抗：$1/g_m$

CG



$$A_v = \frac{R_D}{\frac{1}{g_m} + R_S}$$

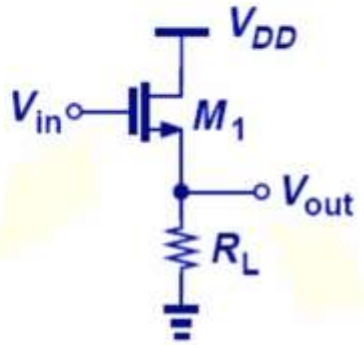
$$R_{in} = \frac{1}{g_m}$$

$$R_{out} = \left[(1+g_m r_O)R_S + r_O\right] \square R_D$$

培养电路直觉的Building Blocks

1. 输出阻抗，向上看为 $1/g_m \,||\, r_o$，向下看为R_L
2. 输入阻抗，无穷大
3. 增益，可看成是S端的分压，V_{in}和S之间是电阻$1/g_m$，S 和地之间是电阻 $R_L||r_o$

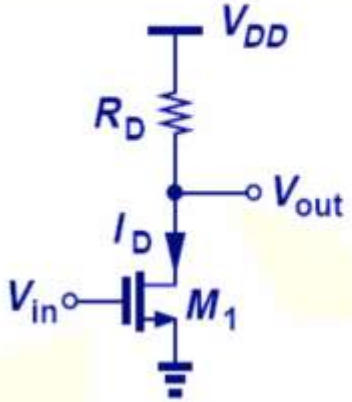
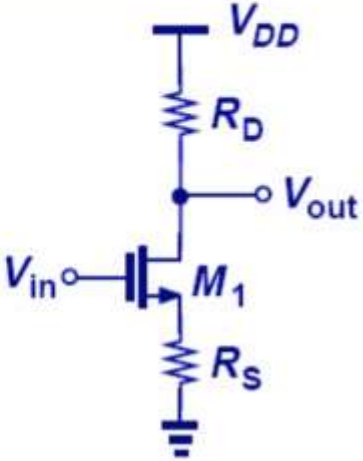
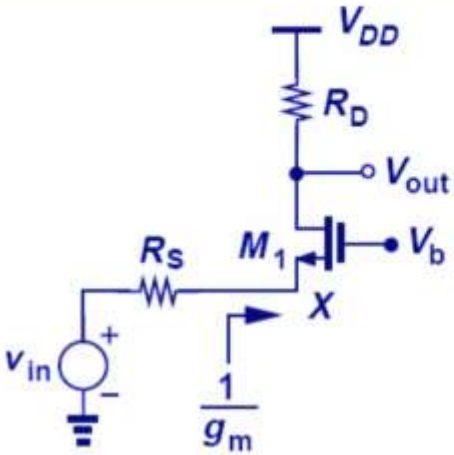
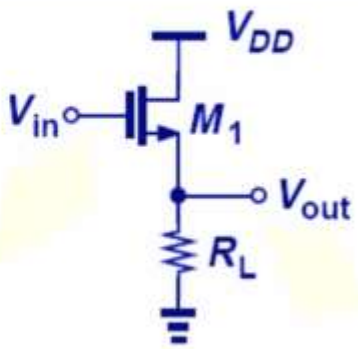
CD



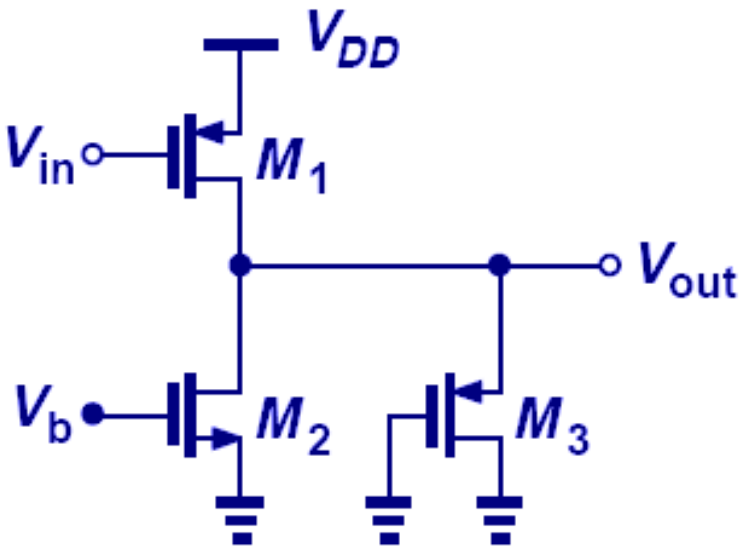
$$A_V = \frac{r_O \,||\, R_L}{\frac{1}{g_m} + r_O \,||\, R_L}$$

$$R_{in} = \infty$$

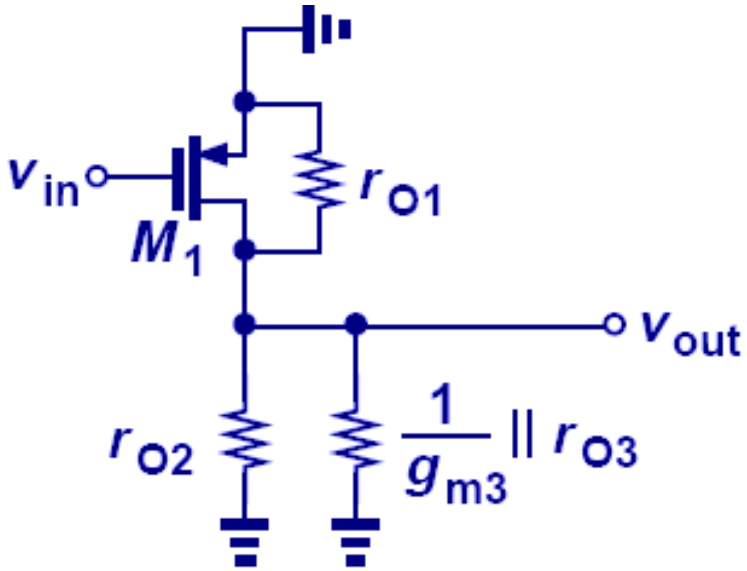
$$R_{out} = \frac{1}{g_m} \,||\, r_O \,||\, R_L$$

CS	CS Deg	CG	CD
			
$A_v = -g_m(R_D \parallel r_O)$ $R_{in} = \infty$ $R_{out} = R_D \parallel r_O$	$A_v = -\dfrac{R_D}{\dfrac{1}{g_m} + R_S}$ $R_{in} = \infty$ $R_{out} = [(1 + g_m r_O)R_S + r_O] \square R_D$	$A_v = \dfrac{R_D}{\dfrac{1}{g_m} + R_S}$ $R_{in} = \dfrac{1}{g_m}$ $R_{out} = [(1 + g_m r_O)R_S + r_O] \square R_D$	$A_v = \dfrac{r_O \parallel R_L}{\dfrac{1}{g_m} + r_O \parallel R_L}$ $R_{in} = \infty$ $R_{out} = \dfrac{1}{g_m} \parallel r_O \parallel R_L$
提供增益 一级或多级	牺牲增益，获得更 大的输出电阻	输入电阻可适配 更好的高频特性	Voltage Buffer 可驱动小电阻

综合实例 (I)



(a)

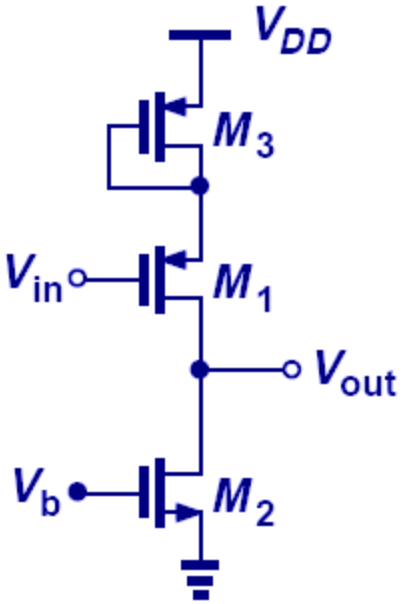


(b)

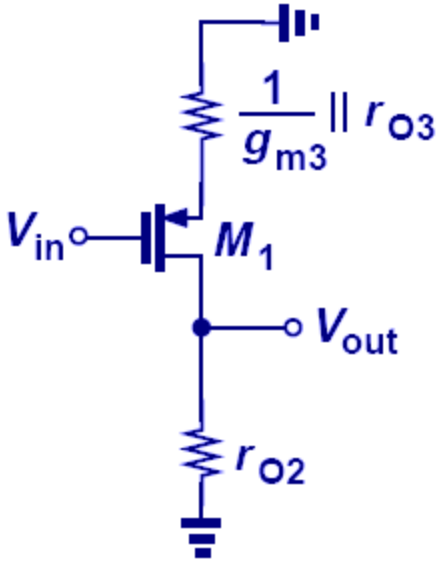
$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}\right)$$

$$R_{out} = \frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}$$

综合实例 (II)



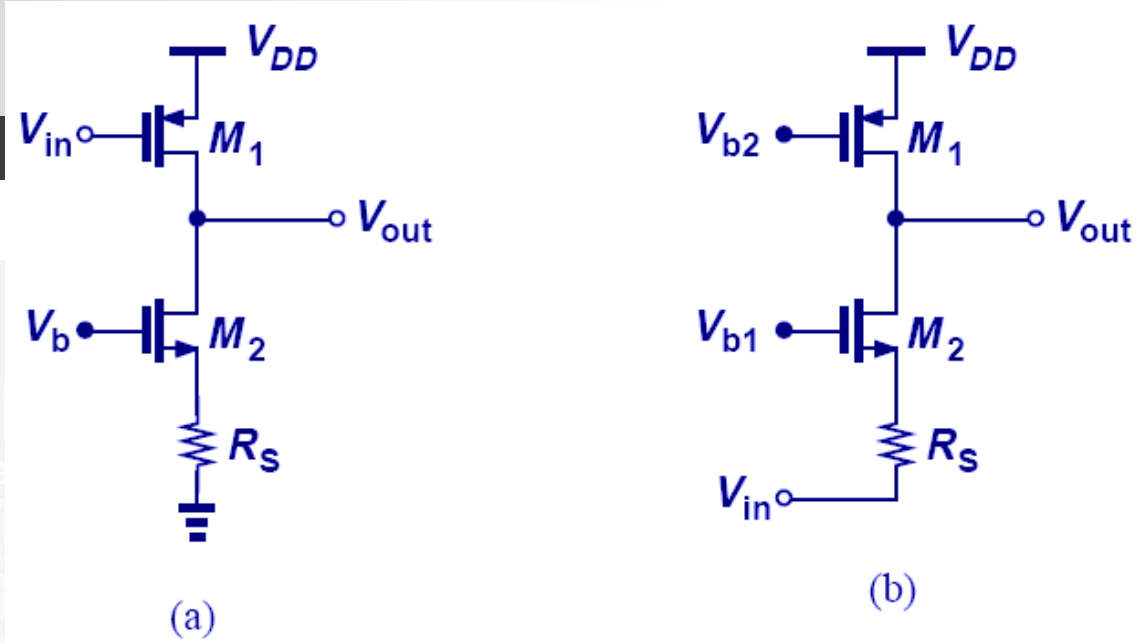
(a)



(b)

$$A_v = -\frac{r_{O2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}} \| r_{O3}}$$

综合实例 III

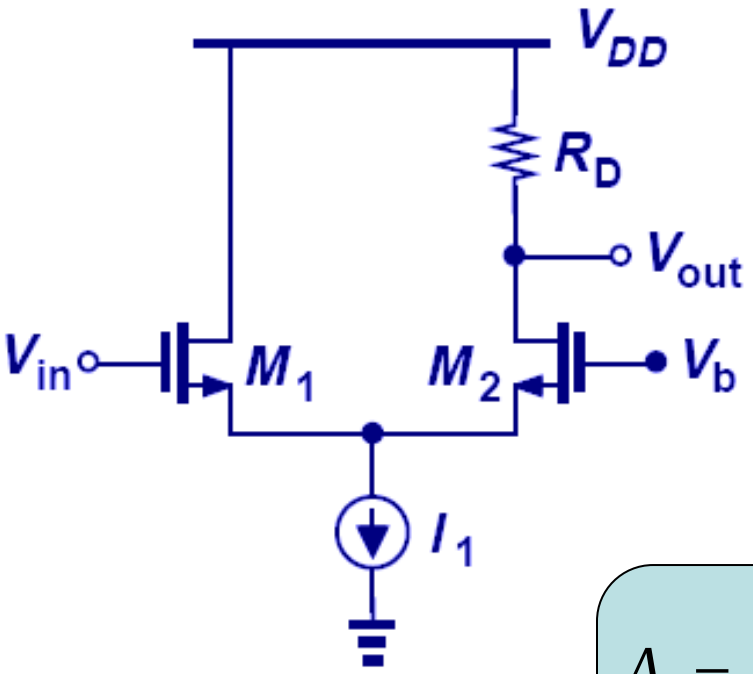


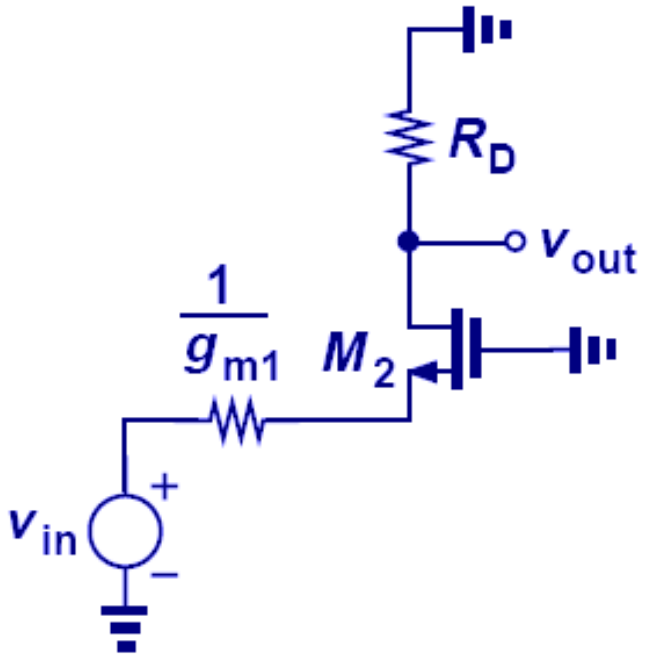
$$A_{v\_CS} = -g_{m1}\left[(1+g_{m2}r_{O2})R_S + r_{O2}\right] \| \, r_{O1}$$

$$A_{v\_CG} = \frac{r_{O1}}{\dfrac{1}{g_{m2}} + R_S}$$

- 同样的电路拓扑结构，若输入接在不同的地方，结果是完全不一样的

综合实例 (IV)

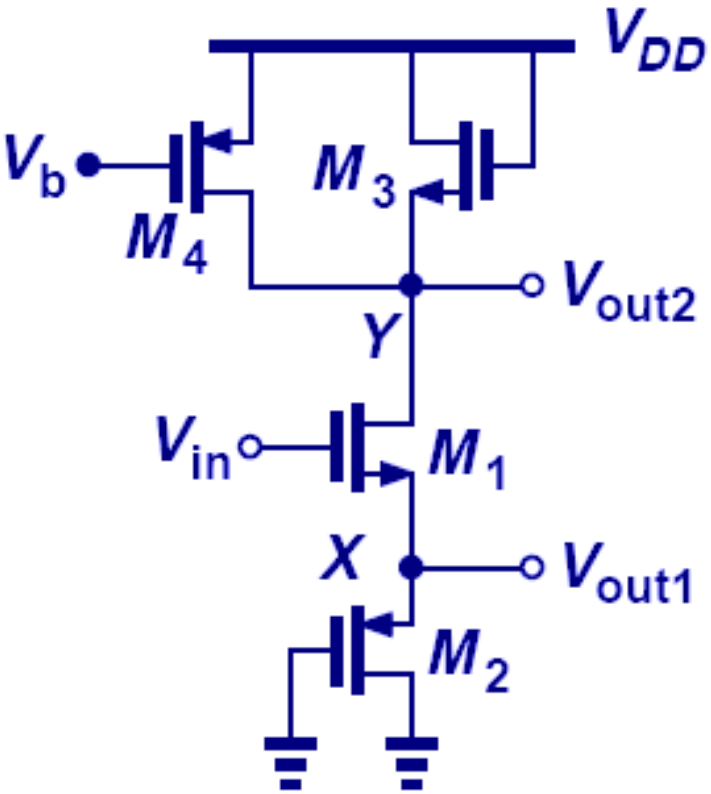




$$A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- 方法1： 左边用戴维南定理替代；
- 方法2： 级联计算

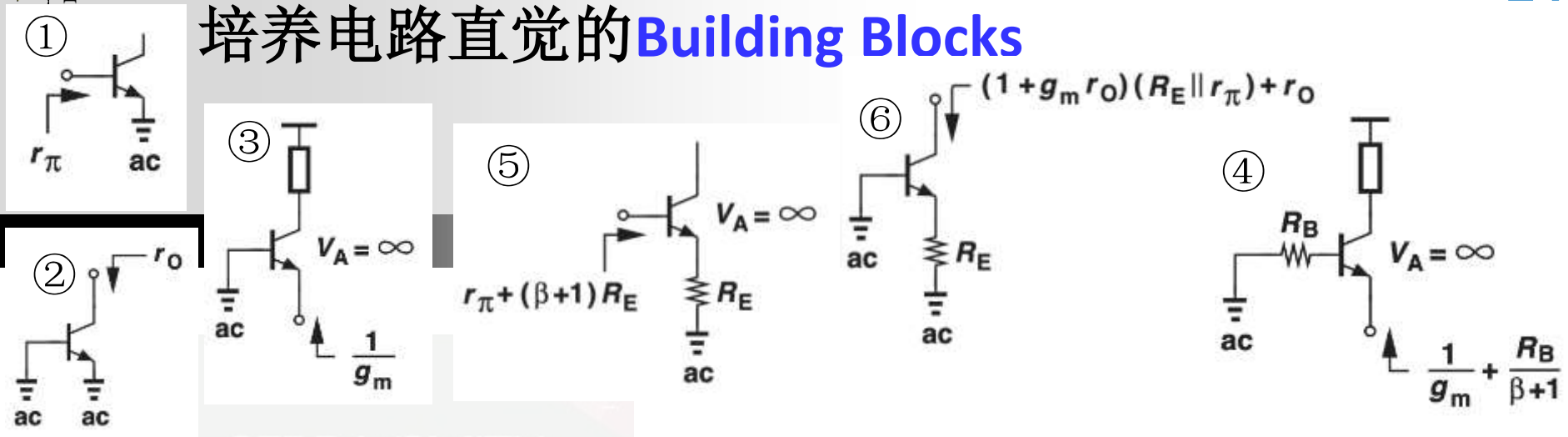
综合实例 (V)



$$\frac{v_{out2}}{v_{in}} = -\frac{\frac{1}{g_{m3}} \| r_{O3} \| r_{O4}}{\frac{1}{g_{m2}} \| r_{O2} + \frac{1}{g_{m1}}}$$

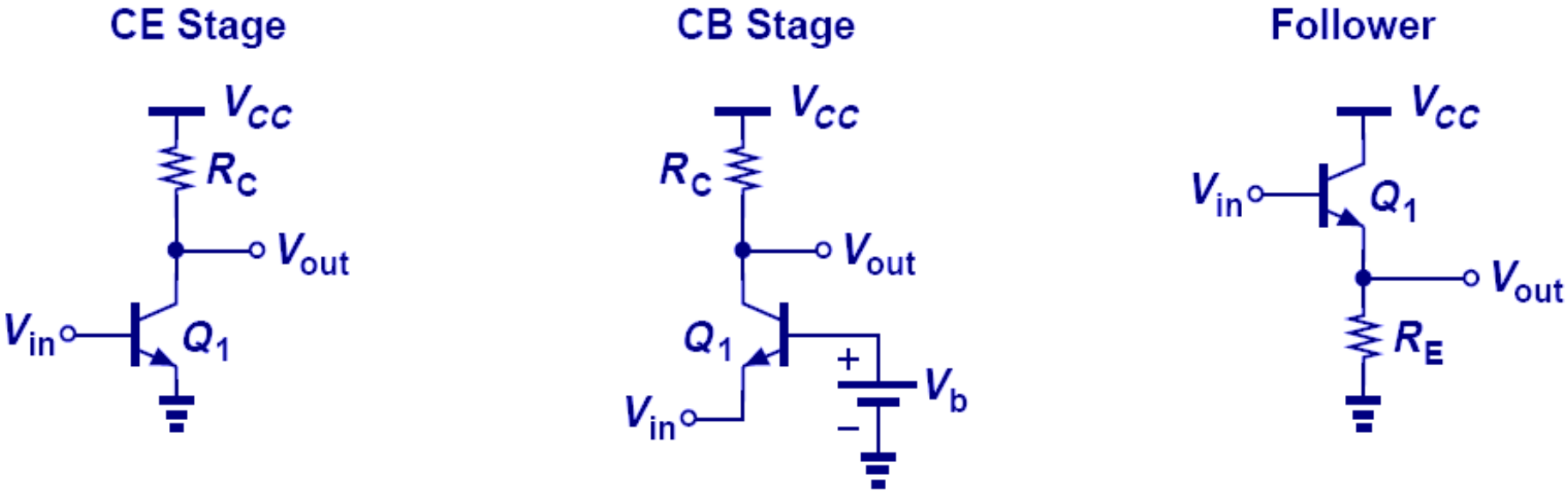
$$\frac{v_{out1}}{v_{in}} = \frac{\frac{1}{g_{m2}} || r_{O2}}{\frac{1}{g_{m2}} || r_{O2} + \frac{1}{g_{m1}}}$$

培养电路直觉的Building Blocks



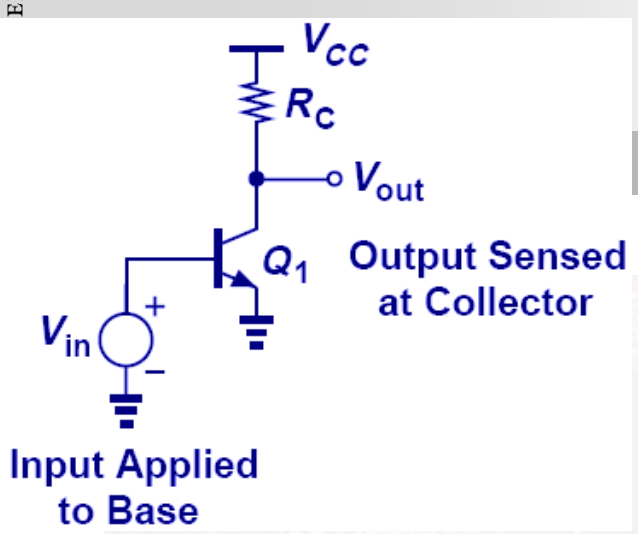
1. 计算输出阻抗时，输入信号 v_i 置零，所以图中的ac地，有可能是真正的ac地，也有可能是 v_i 输入端
2. 从B端看进去，E的电阻折算到B需乘以(1+β)；从E端看进去，B的电阻折算到E需除以(1+β)
3. ① r_π 或者 $r_e(1+\beta)$ ② r_o
4. ③B的ac可以是真正的ac地（CB输入电阻），也可以是v_i（CC输出电阻）
5. ④当B接有电阻R_B时，R_B除以(1+β)折算到E
6. ⑤从B看输入电阻，R_E乘以(1+β)折算到B
7. ⑥信号可以从B输入（发射极退化），也可以从E输入（CB,R_E可视为信号源内阻）；用混合π模型考虑，E到地的电阻是R_E和r_π并联
8. Emitter degeneration 结构的主要作用：大幅提高输出阻抗→更接近于理想电流源，提高的增量为 E 端串接的电阻 R_E ||r_π 放大（$1+g_m r_o$）倍

三极管放大电路总结

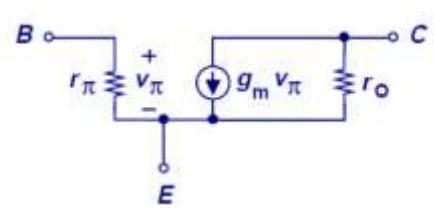


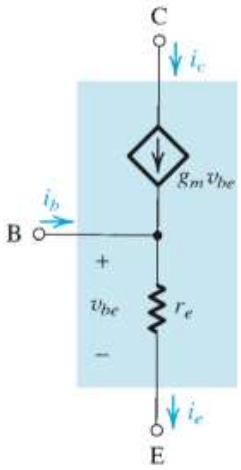
- 三种组态具有不同的特性→各有各的用途；
- CE和CB具有较大的电压增益，而射极跟随具有单位电压增益；
- CE是最常见的放大器结构；
- CB的输入阻抗具有$1/g_m$特性，适合于设计成50欧姆输入阻抗，因此在射频电路中有广泛应用；
- 射极跟随因具有较大输入阻抗、较小输出阻抗、单位电压增益等特性，往往作为Buffer使用；

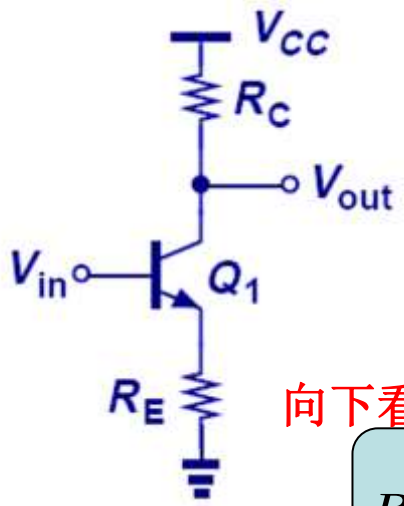
在理解的基础上熟记（CE）



$$A_v = -g_m(R_C \parallel r_O)$$
$$R_{out} = R_C \parallel r_O$$
$$R_{in} = r_\pi$$







$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$
$$R_{in} = r_\pi + (\beta+1)R_E$$
$$R_{out} = R_C$$

$i_c \approx i_e$

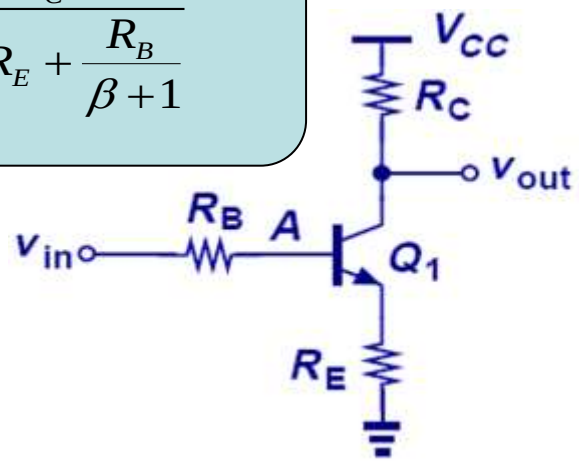
E折算到B

向下看

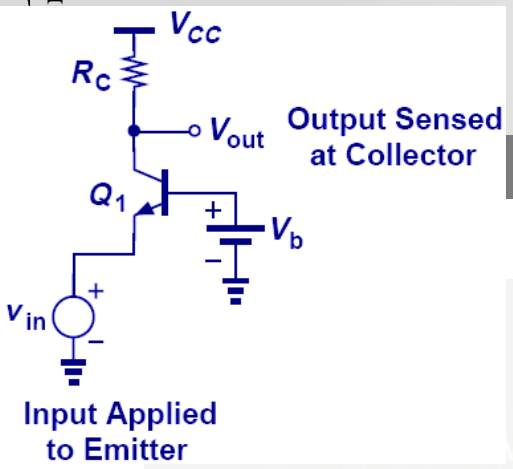
$$R_{out} = r_O + (g_m r_O + 1)(R_E \parallel r_\pi)$$

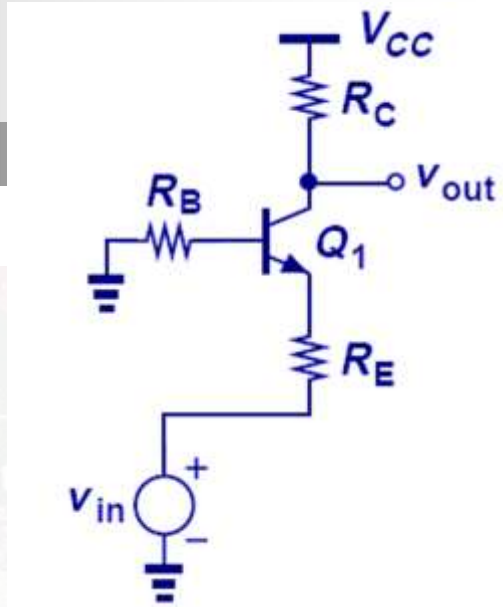
B折算到E

$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1}}$$



在理解的基础上熟记（CB）





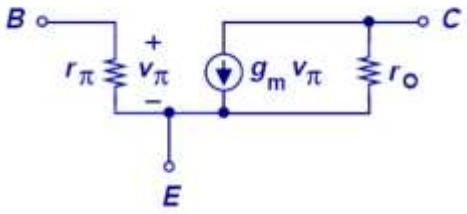
$i_c \approx i_e$　　B折算到E

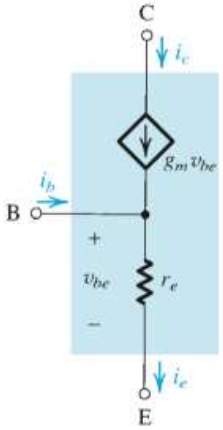
$$A_v \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

$$A_v = g_m(r_O \parallel R_C)$$

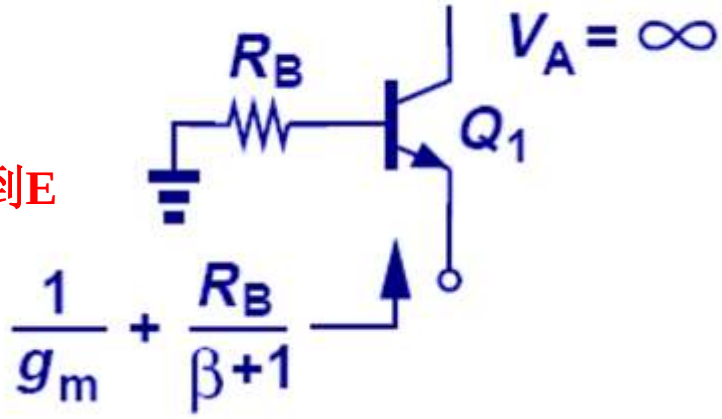
$$R_{in} = \frac{1}{g_m}$$

$$R_{out} = r_O \parallel R_C$$

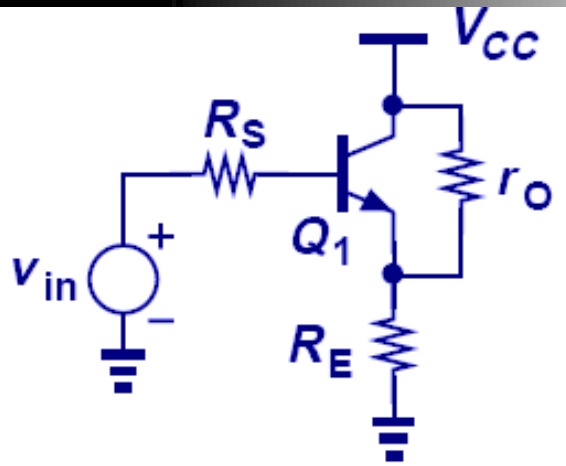




B折算到E



在理解的基础上熟记（射极跟随）



$$A_v = \frac{R_E \parallel r_O}{R_E \parallel r_O + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}}$$

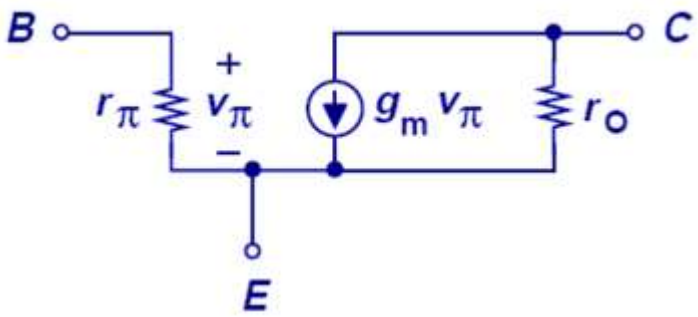
B折算到E

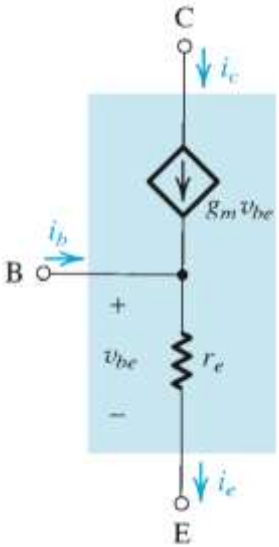
$$R_{in} = r_\pi + (\beta+1)(R_E \parallel r_O) + R_S$$

E折算到B

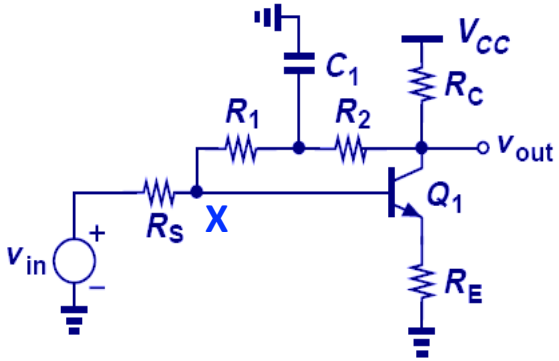
$$R_{out} = \left(\frac{R_s}{\beta+1} + \frac{1}{g_m}\right) \parallel R_E \parallel r_O$$

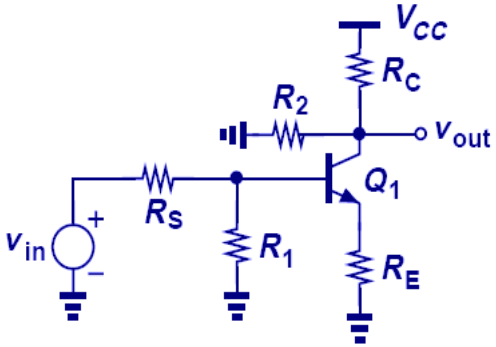
从E看进去，B要折算到E，再和r_o、R_E并联

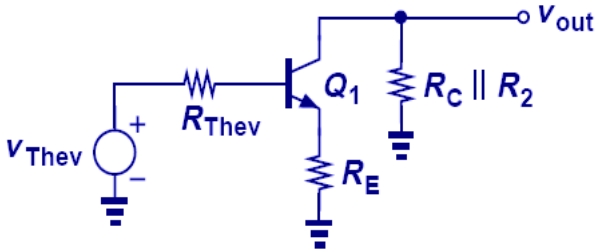




综合实例 I



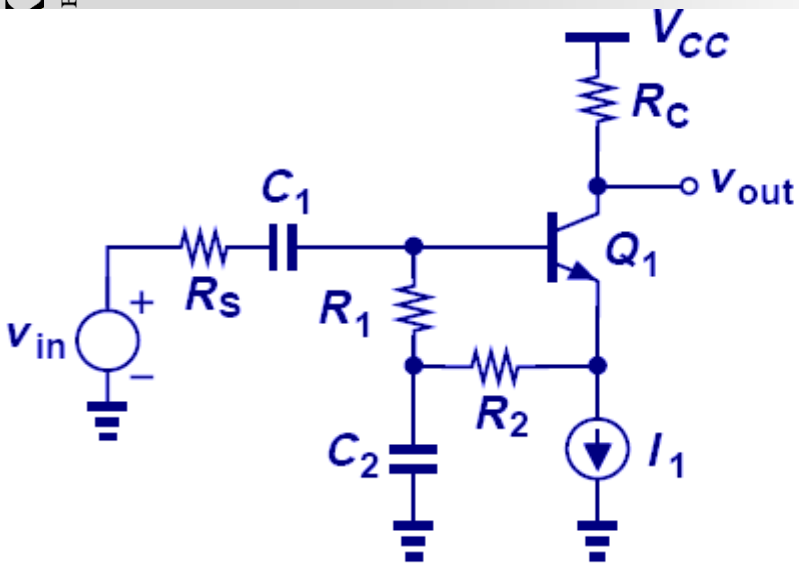


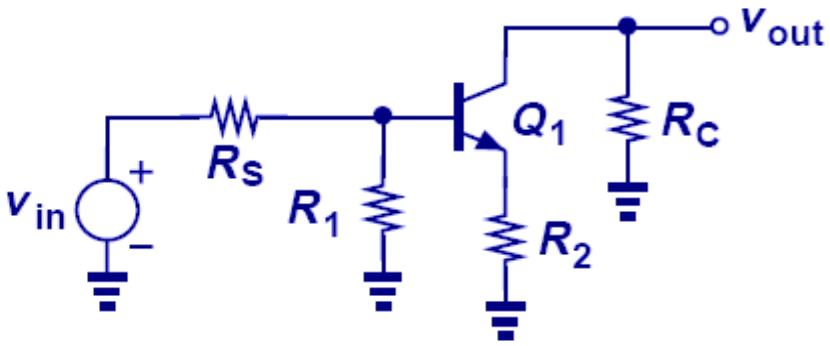


$$\frac{v_{out}}{v_{in}} = -\frac{R_2 \parallel R_C}{\dfrac{R_1 \parallel R_S}{\beta+1} + \dfrac{1}{g_m} + R_E} \cdot \frac{R_1}{R_1 + R_S}$$

通过X点级联，Q_1的输入电阻很大，与R_1并联时，可以忽略

综合实例 II





$$\frac{v_{out}}{v_{in}} = -\frac{R_C}{\frac{R_S \parallel R_1}{\beta+1} + \frac{1}{g_m} + R_2} \cdot \frac{R_1}{R_1 + R_S}$$

Example 5.50

Assuming $V_A = \infty$, compute the voltage gain and input impedance of the circuit shown in Fig. 5.99(a).

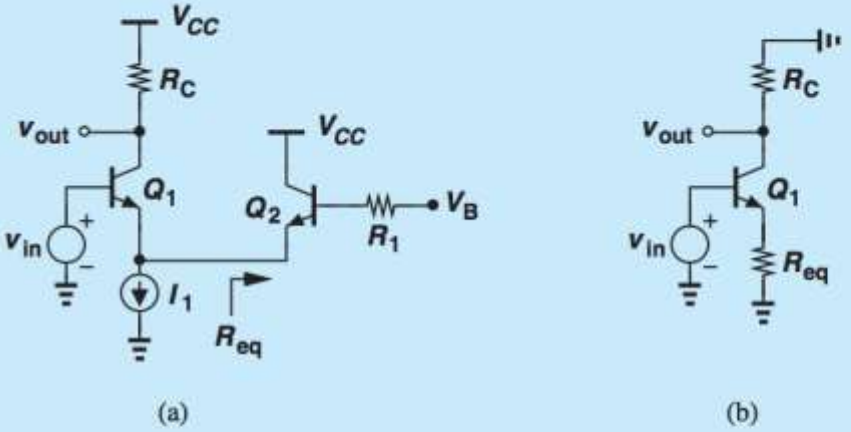


Figure 5.99 (a) Example of CE stage, (b) simplified circuit.

Solution The circuit resembles a CE stage (why?) degenerated by the impedance seen at the emitter of Q_2, R_{eq}. Recall from Fig. 5.75 that

$$R_{eq} = \frac{R_1}{\beta + 1} + \frac{1}{g_{m2}}. \tag{5.347}$$

The simplified model in Fig. 5.99(b) thus yields

$$A_v = \frac{-R_C}{\dfrac{1}{g_{m1}} + R_{eq}} \tag{5.348}$$

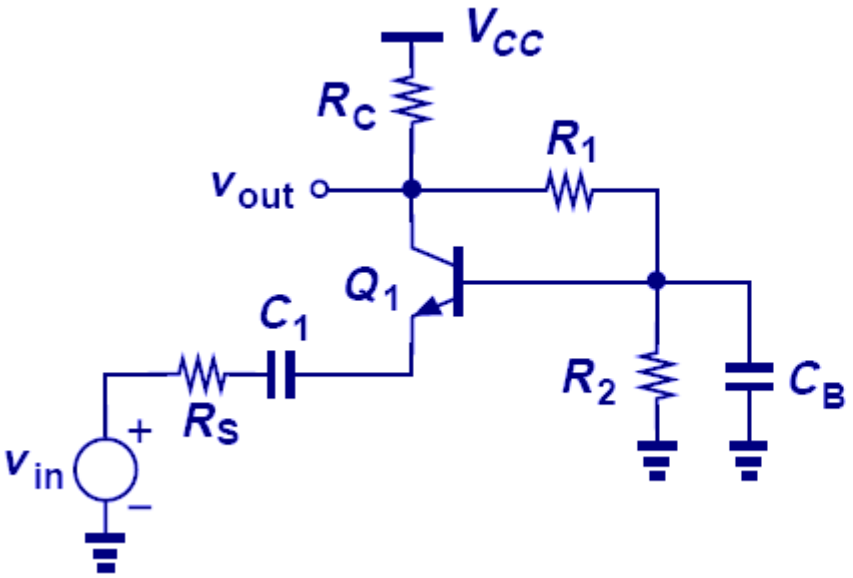
$$= \frac{-R_C}{\dfrac{1}{g_{m1}} + \dfrac{R_1}{\beta + 1} + \dfrac{1}{g_{m2}}}. \tag{5.349}$$

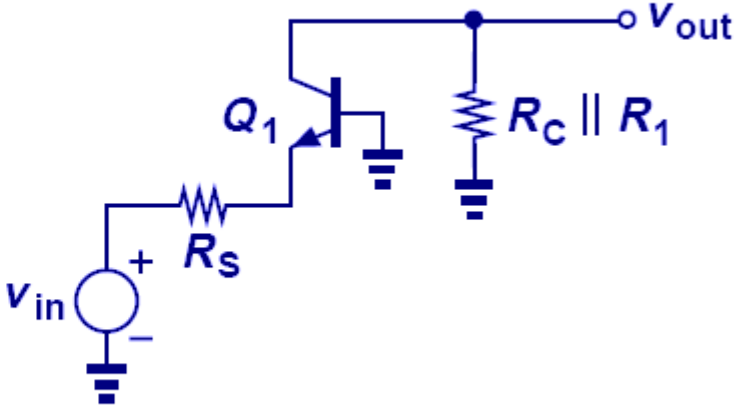
The input impedance is also obtained from Fig. 5.75:

$$R_{in} = r_{\pi 1} + (\beta + 1)R_{eq} \tag{5.350}$$

$$= r_{\pi 1} + R_1 + r_{\pi 2}. \tag{5.351}$$

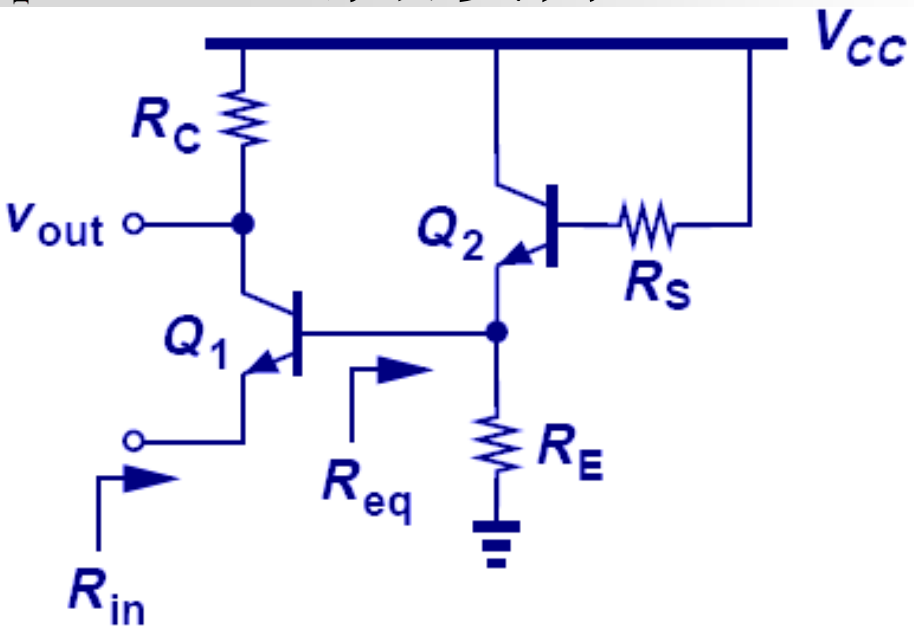
综合实例IV

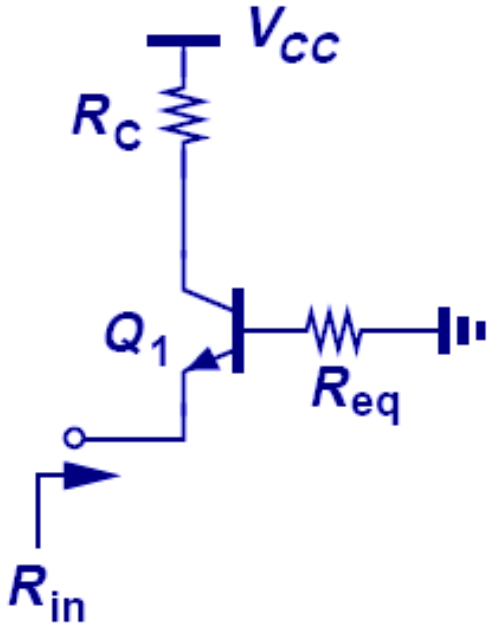




$$A_v = \frac{R_C \parallel R_1}{R_S + \dfrac{1}{g_m}}$$

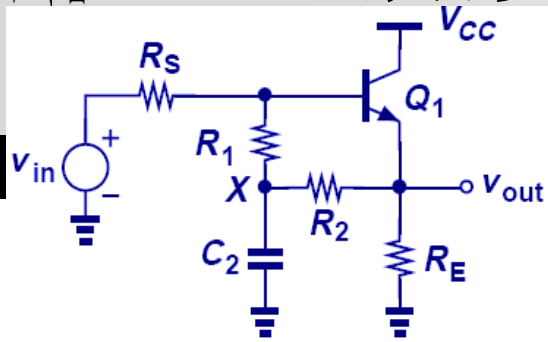
综合实例V



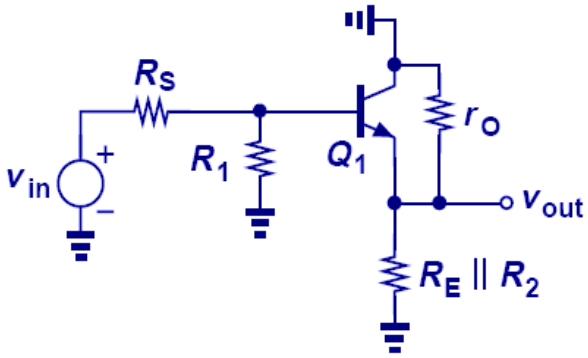


$$R_{in} = \frac{1}{\beta+1}\left[\left(\frac{R_S}{\beta+1}+\frac{1}{g_{m2}}\right)\| R_E\right]+\frac{1}{g_{m1}}$$

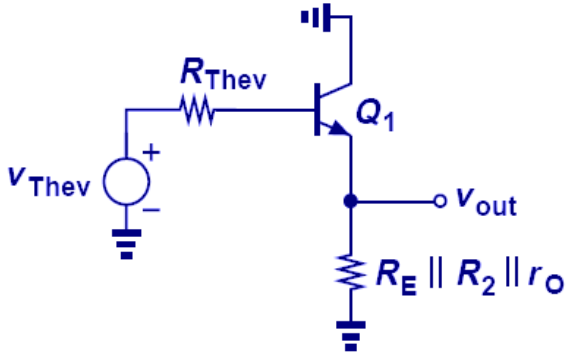
综合实例 VI



(a)



(b)

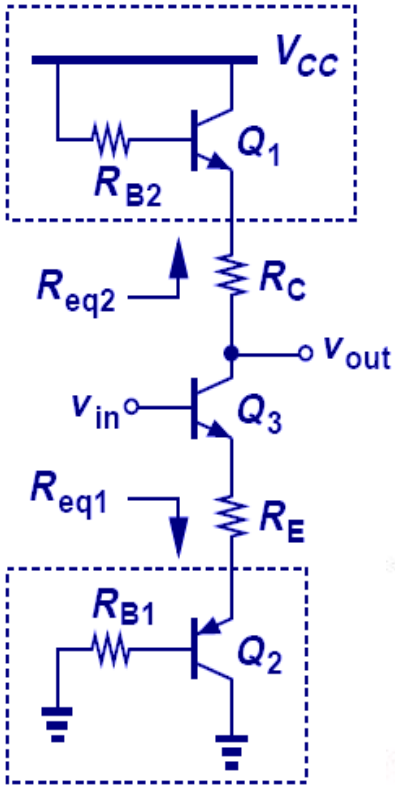


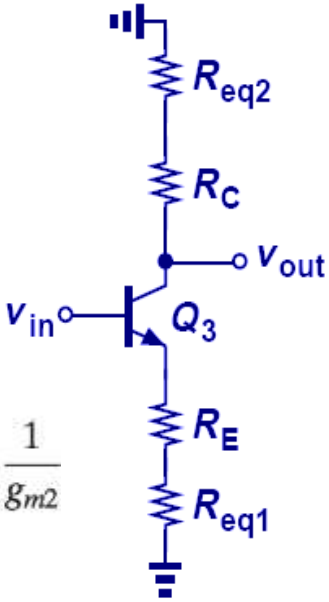
(c)

$$\frac{v_{out}}{v_{in}} = \frac{R_E \parallel R_2 \parallel r_O}{R_E \parallel R_2 \parallel r_O + \dfrac{1}{g_m} + \dfrac{R_S \parallel R_1}{\beta+1}} \cdot \frac{R_1}{R_1 + R_S}$$

$$R_{out} = \left(\frac{R_S \parallel R_1}{\beta+1} + \frac{1}{g_m} \right) \parallel R_E \parallel R_2 \parallel r_O$$

综合实例VII





$$R_{eq1} = \frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}}$$

$$R_{eq2} = \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m1}}$$

$$R_{in} = r_{\pi 3} + (\beta+1)\left(R_E + \frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}} \right)$$

$$R_{out} = R_C + \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m3}}$$

$$A_v = -\frac{R_C + \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m1}}}{\frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}} + \frac{1}{g_{m3}} + R_E}$$

偏置电路方案1，直接固定V_{GS}

Biasing by Fixing V_{GS}

Device 1 和 Device 2 为工艺、温度偏差导致的器件特性偏差

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

I_D受工艺、温度偏差的影响较大，不是好的偏置方案

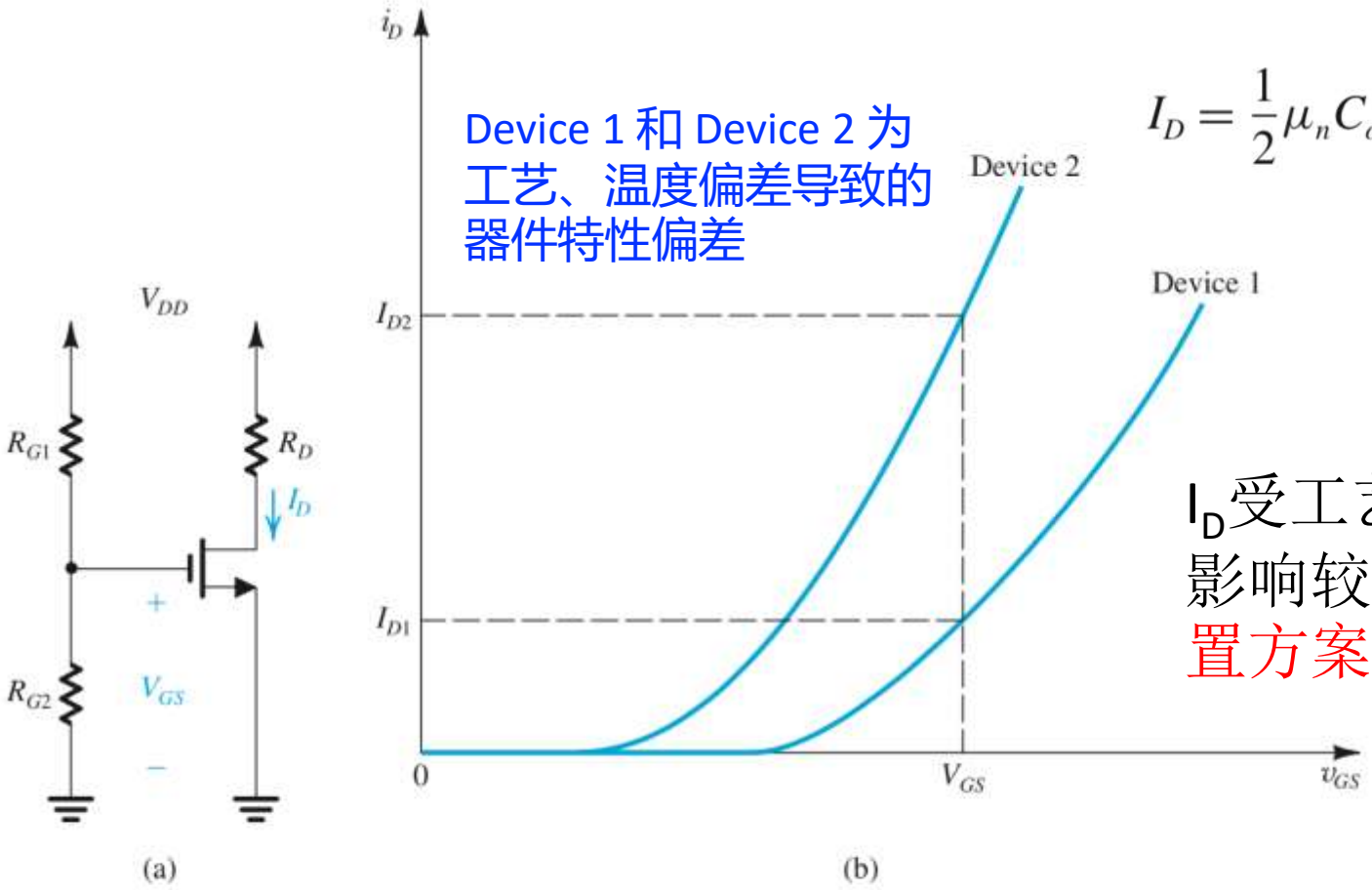
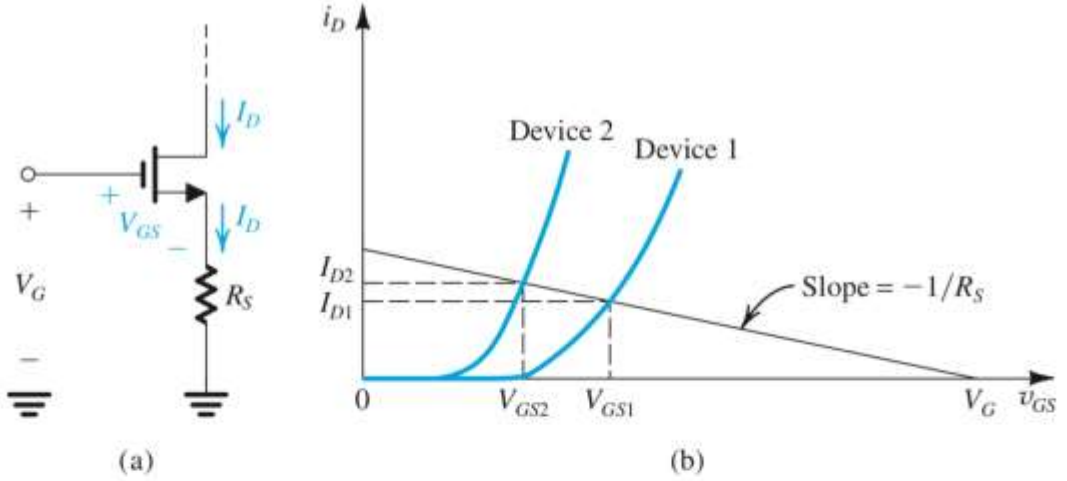


Figure 7.47 (a) Biasing the MOSFET with a constant V_{GS} generated from V_{DD} using a voltage divider (R_{G1},R_{G2}); (b) the use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.

偏置电路方案2，引入源极退化电阻，负反馈提高稳定性



$$V_G = V_{GS} + R_S I_D$$

可有效降低工艺、温度变化的影响(I_D变化较小)

单电源供电

双电源供电

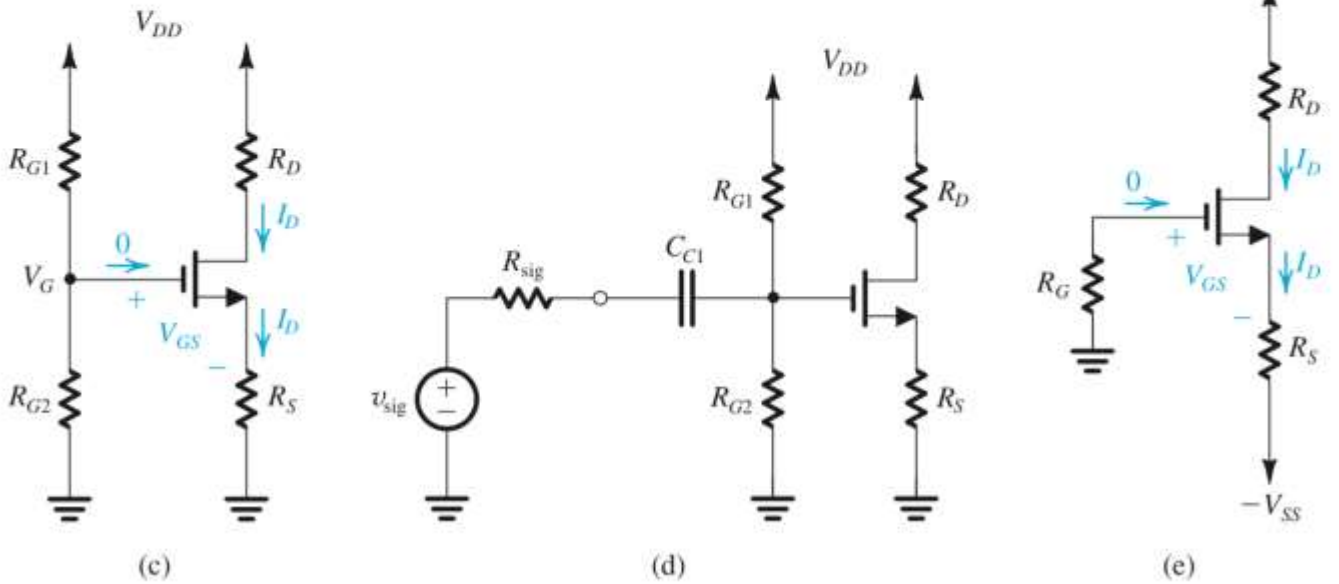
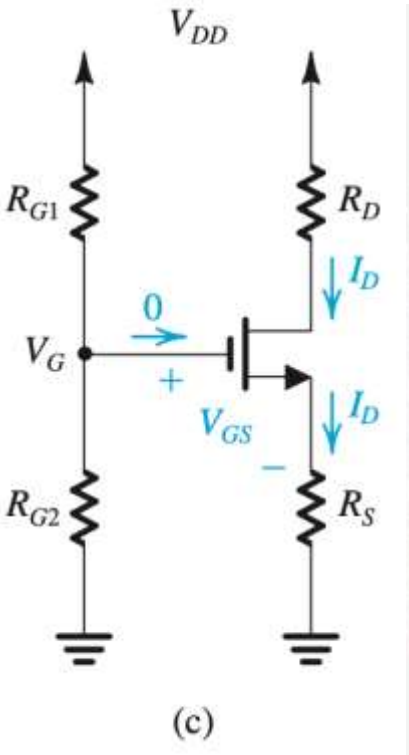


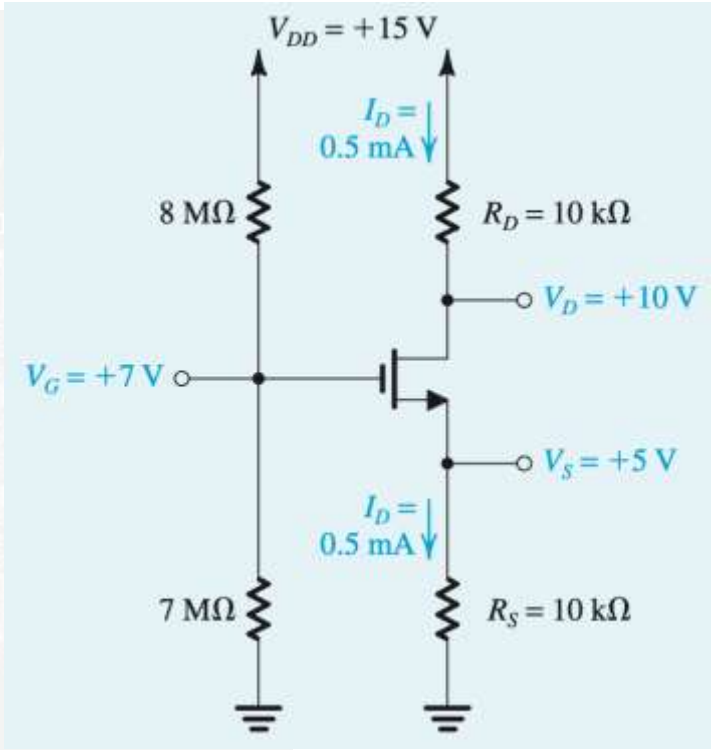
Figure 7.48 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D; **(c)** practical implementation using a single supply; **(d)** coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** practical implementation using two supplies.

Example 7.11

It is required to design the circuit of Fig. 7.48(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n' W/L = 1$ mA/V^2. For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n' W/L$ but $V_t = 1.5$ V.

一般直流分析时不考虑沟道调制效应





①为了使输出有最大可能的摆幅，一般设置V_D为V_{DD}的2/3，V_S为V_{DD}的1/3

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10\ \text{k}\Omega$$

$$R_S = \frac{V_S}{R_S} = \frac{5}{0.5} = 10\ \text{k}\Omega$$

②

$$I_D = \frac{1}{2} k_n' (W/L) V_{OV}^2 \Rightarrow V_{GS} = 2\ \text{V}$$

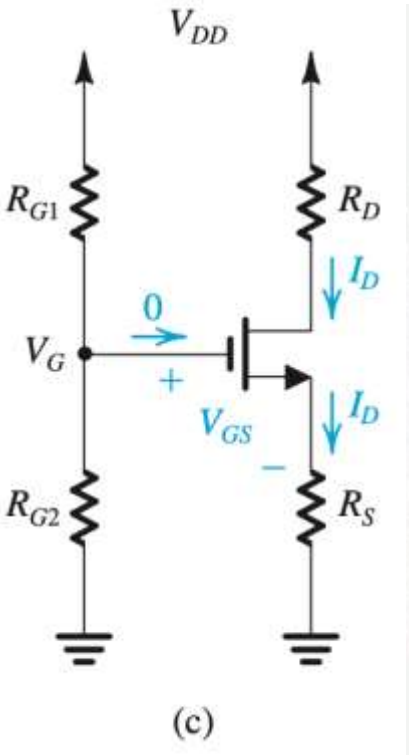
$$\Rightarrow V_G = V_S + V_{GS} = 5 + 2 = 7\ \text{V}$$

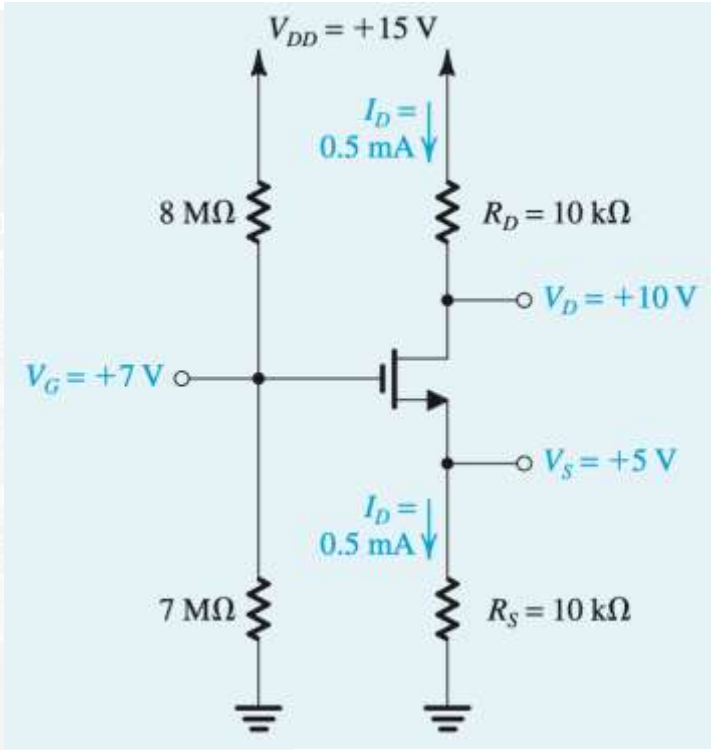
$\Rightarrow$ may select $R_{G1} = 8$ MΩ and $R_{G2} = 7$ MΩ

Example 7.11

It is required to design the circuit of Fig. 7.48(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n' W/L = 1$ mA/V^2. For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n' W/L$ but $V_t = 1.5$ V.

一般直流分析时不考虑沟道调制效应





如果 $V_t = 1.5$ V

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2$$

$$V_G = V_{GS} + I_D R_S$$

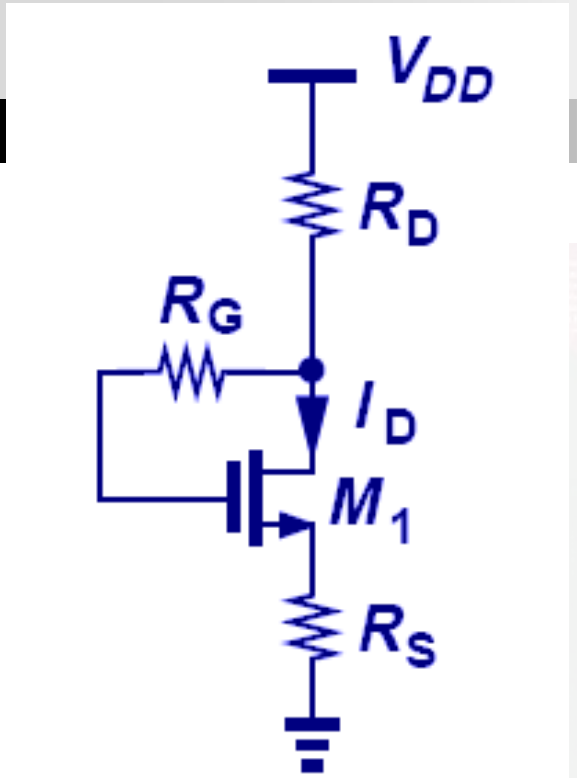
$$7 = V_{GS} + 10 I_D$$

$$I_D = 0.455 \text{ mA}$$

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

$$\frac{-0.045}{0.5} \times 100 = -9\% \text{ change.}$$

偏置电路方案3，自偏置：G和D连接一个较大电阻



- M1 始终处于饱和区；
- R_G 上面没有电压降

$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{DD} - (R_S + R_D)I_D - V_{TH}]^2$$

$$(R_S + R_D)^2 I_D^2 - 2\left[(V_{DD} - V_{TH})(R_S + R_D) + \frac{1}{\mu_n C_{ox}\frac{W}{L}}\right] I_D + (V_{DD} - V_{TH})^2 = 0. \quad (7.31)$$

Example 7.3

Calculate the drain current of M_1 in Fig. 7.3 if $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $\lambda = 0$. What value of R_D is necessary to reduce I_D by a factor of two?

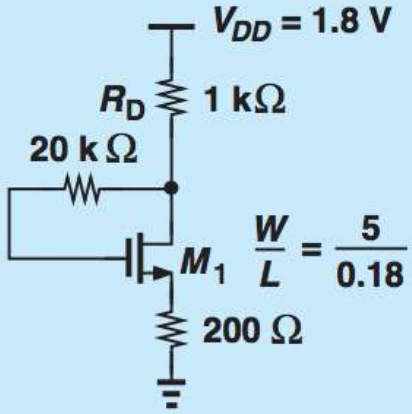


Figure 7.3 Example of self-biased MOS stage.

Solution Equation (7.31) gives

$$I_D = 556\,\mu\text{A}. \tag{7.32}$$

To reduce I_D to 278 μA, we solve Eq. (7.31) for R_D:

$$R_D = 2.867\,\text{k}\Omega. \tag{7.33}$$

偏置电路方案4，恒流源确定I_D：集成电路中常用的偏置方案

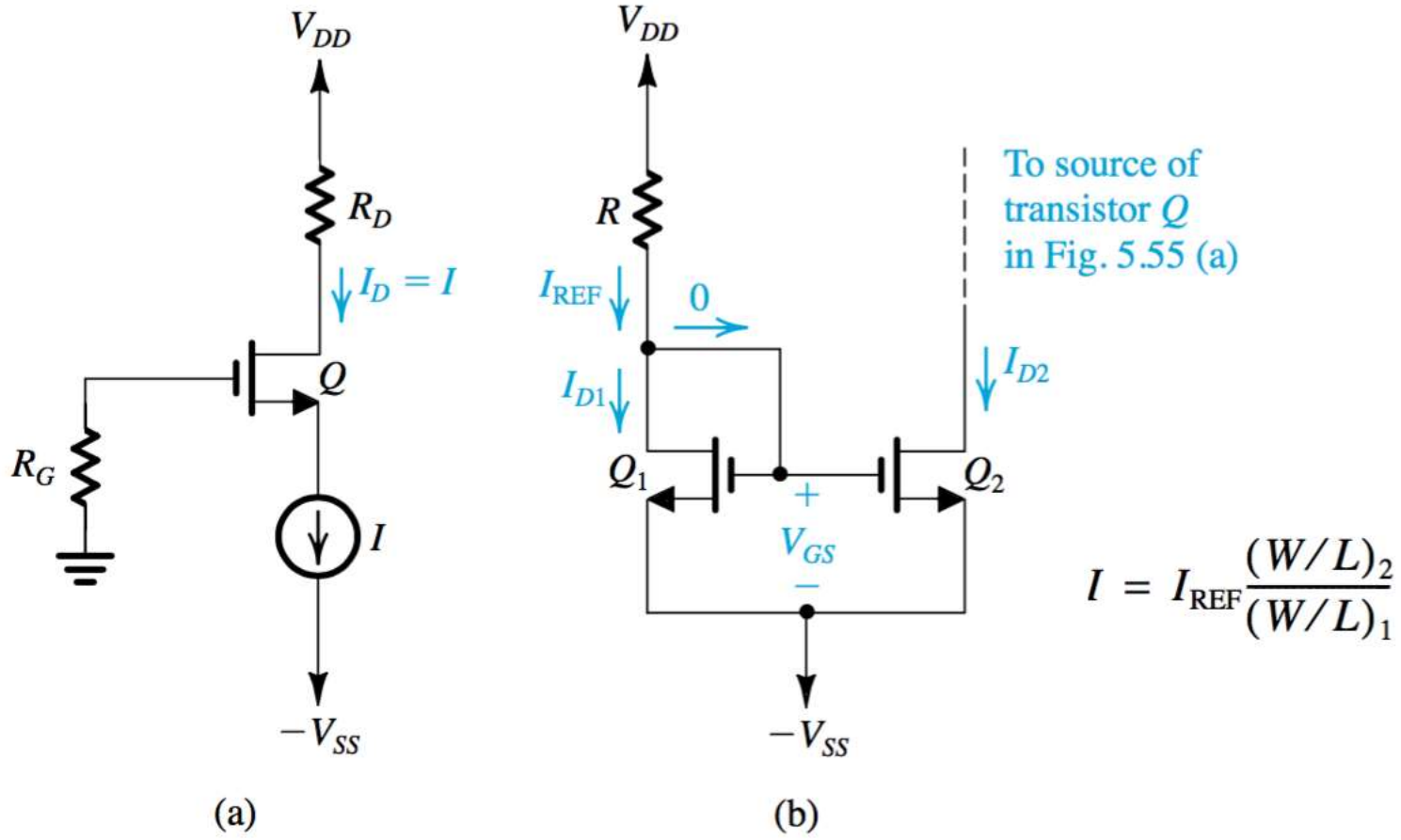
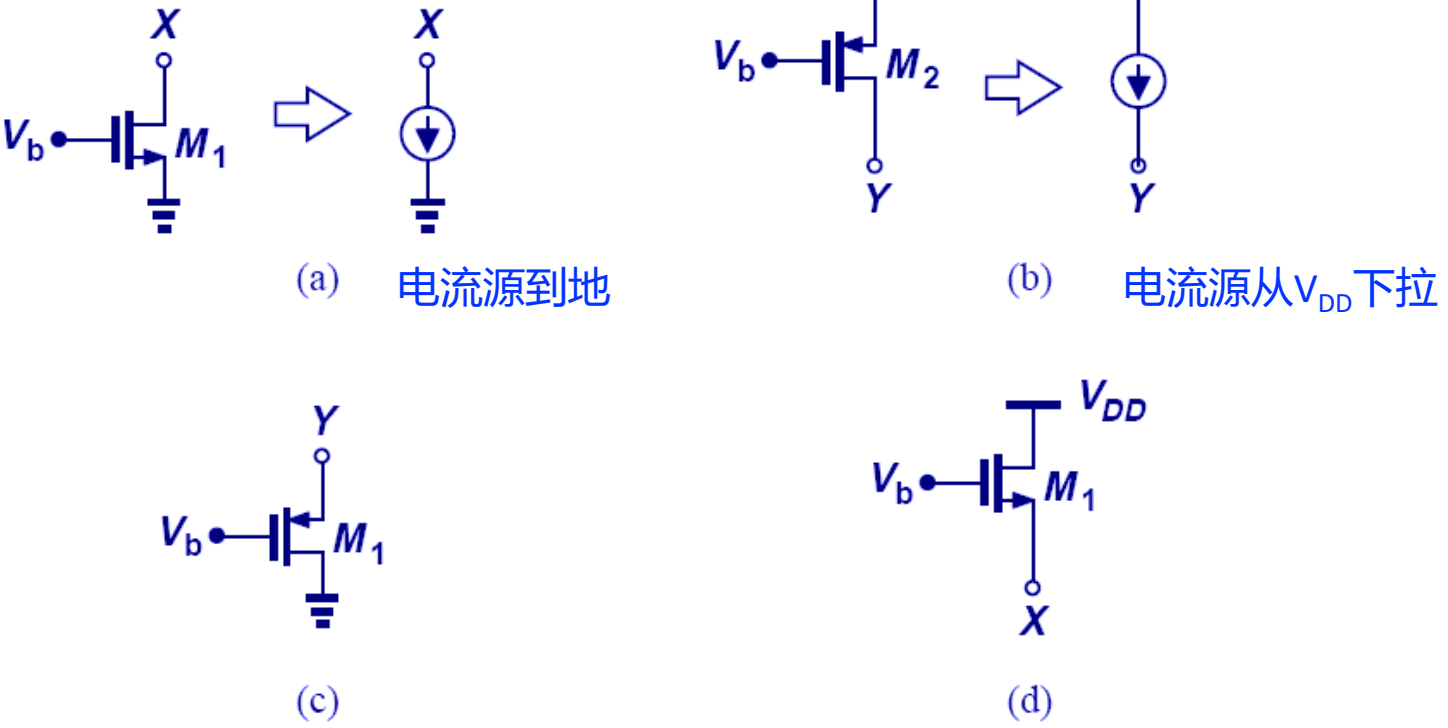


Figure 5.55 **(a)** Biasing the MOSFET using a constant-current source I. **(b)** Implementation of the constant-current source I using a current mirror.

电流源



- 工作在饱和区时，MOSFET 可以当做一个电流源；
- 思考：为何（c）和（d）不能当做电流源？ V_{GS}不固定

偏置电路方案1，直接固定 V_{BE} 或 I_B

I_C受工艺、温度偏差的影响较大，不是好的偏置方案

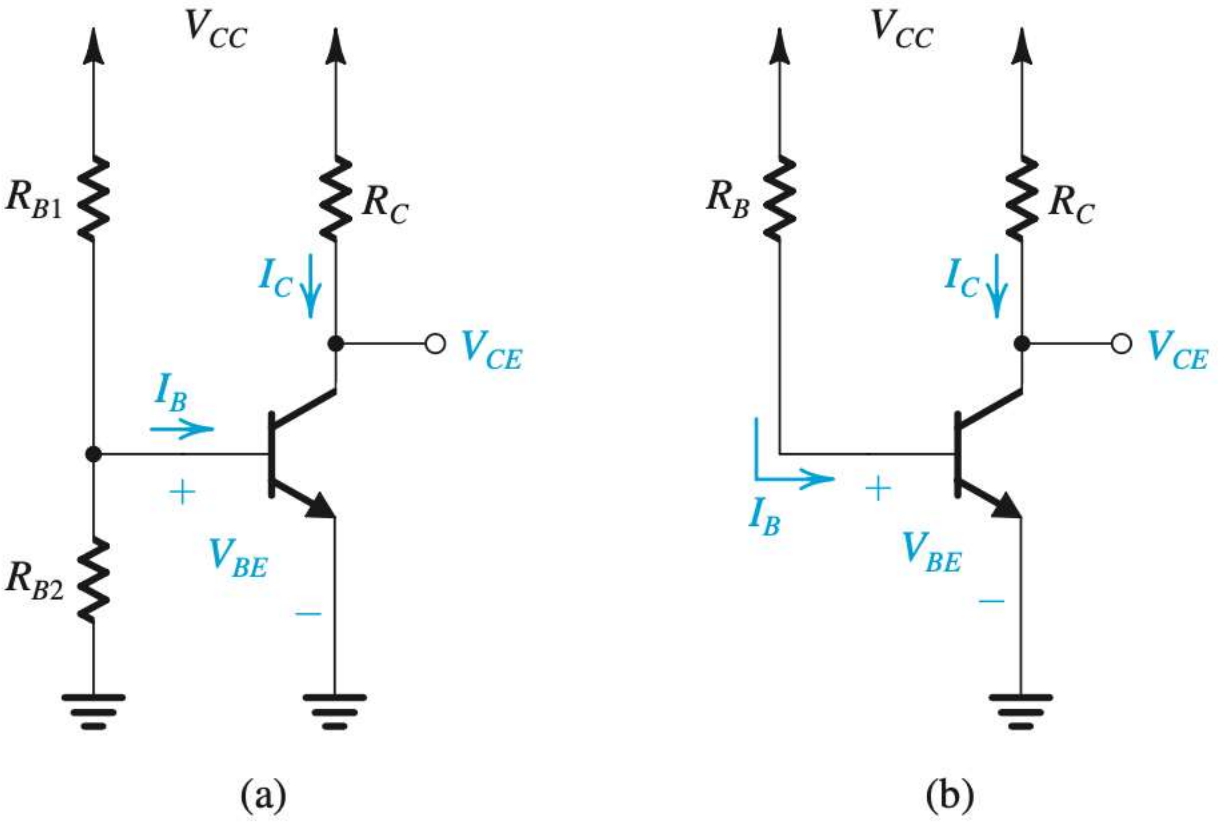


Figure 7.51 Two obvious schemes for biasing the BJT: (**a**) by fixing V_{BE}; (**b**) by fixing I_B. Both result in wide variations in I_C and hence in V_{CE} and therefore are considered to be "bad." Neither scheme is recommended.

偏置电路方案2，引入射极退化电阻，负反馈提高稳定性

①I_C（I_E）由I_B和β决定，为了减小β的影响：

$$V_{BB} \gg V_{BE}$$

$$R_E \gg \frac{R_B}{\beta + 1}$$

②为了使输出有较大的摆幅，V_{BB}一般设置为V_{CC}的1/3，V_C一般设置为V_{CC}的2/3

③I_B对V_B的影响要尽可能小→R_1R_2上的电流要比I_B大得多，一般选 I_E to $0.1I_E$

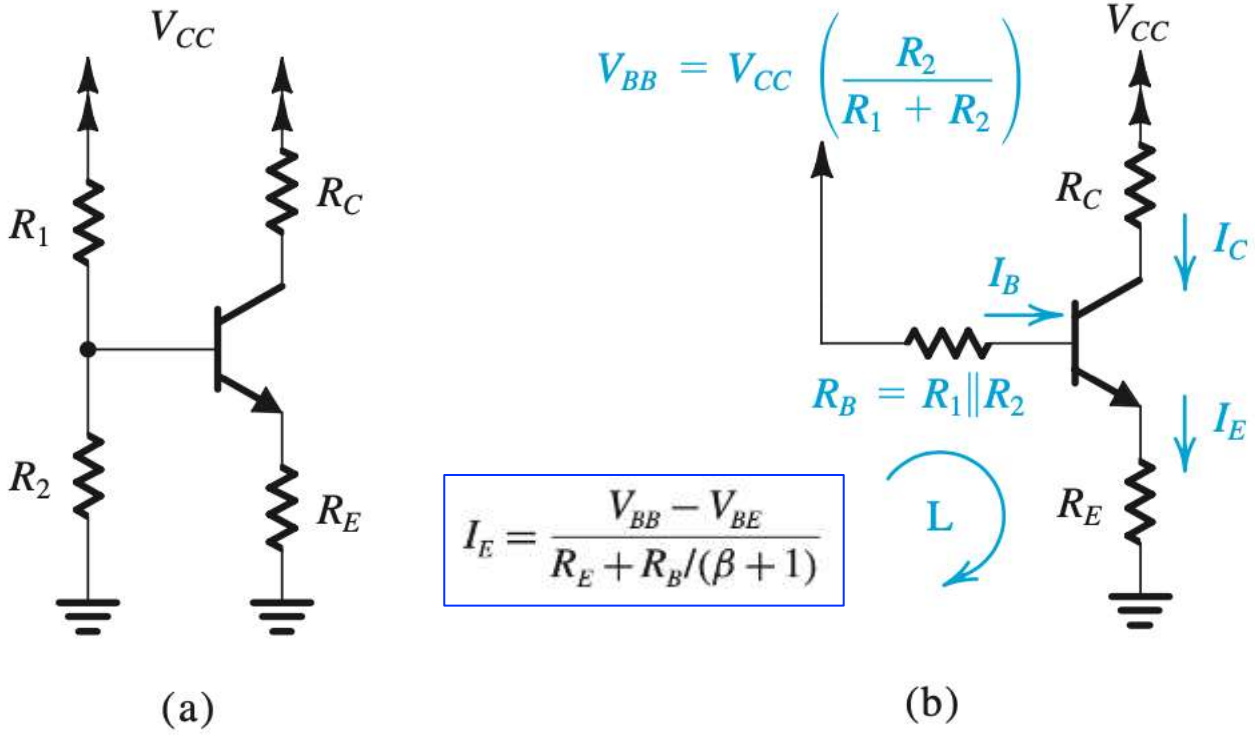
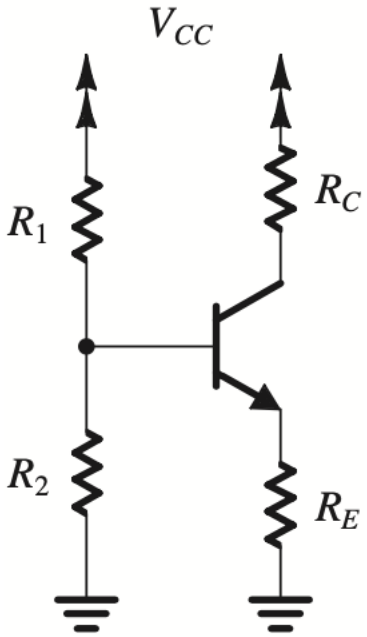


Figure 7.52 Classical biasing for BJTs using a single power supply: (**a**) circuit; (**b**) circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

We wish to design the bias network of the amplifier in Fig. 7.52 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.



(a)

①根据三分之一设计规则

$$V_B = +4\text{ V}$$
$$V_E = 4 - V_{BE} \simeq 3.3\text{ V}$$

$$R_E = \frac{V_E}{I_E} = \frac{3.3}{1} = 3.3\text{ k}\Omega$$

②根据R_1R_2电流设计规则

$$0.1I_E = 0.1 \times 1 = 0.1\text{ mA}$$

$$R_1 + R_2 = \frac{12}{0.1} = 120\text{ k}\Omega$$

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4\text{ V}$$

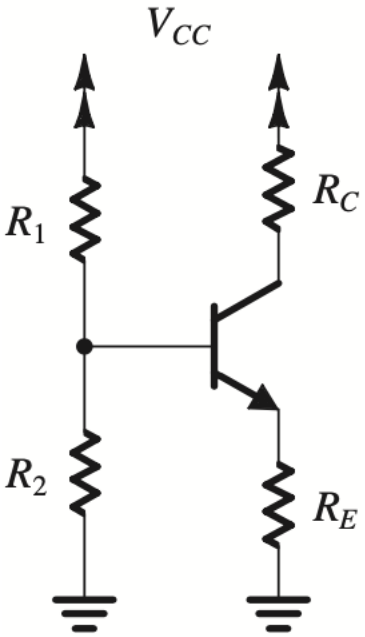
$$R_2 = 40\text{ k}\Omega \text{ and } R_1 = 80\text{ k}\Omega$$

③重新计算I_E，发现与设计值相比偏小了，可以通过减小R_E回到设计值

$$I_E = \frac{4 - 0.7}{3.3(\text{k}\Omega) + \frac{(80 \| 40)(\text{k}\Omega)}{101}} = 0.93\text{ mA}$$

原因是R_{BB}折算到E极后与R_E相比并非明显可忽略

We wish to design the bias network of the amplifier in Fig. 7.52 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.



(a)

④也可以重新选择R_1R_2设计规则，选择流过它们的电流为I_E，此时

$$R_1 + R_2 = \frac{12}{1} = 12 \text{ k}\Omega$$

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4 \text{ V}$$

$$R_1 = 8 \text{ k}\Omega \text{ and } R_2 = 4 \text{ k}\Omega$$

$$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \simeq 1 \text{ mA}$$

⑤计算R_C

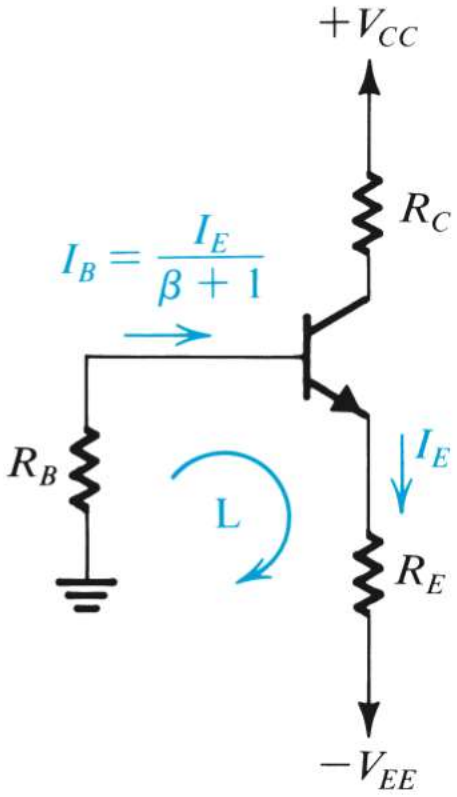
Finally, the value of R_C can be determined from

$$R_C = \frac{12 - V_C}{I_C}$$

Substituting $I_C = \alpha I_E = 0.99 \times 1 = 0.99 \text{ mA} \simeq 1 \text{ mA}$ results, for both designs, in

$$R_C = \frac{12 - 8}{1} = 4 \text{ k}\Omega$$

双电源供电情况



$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)}$$

Figure 7.53 Biasing the BJT using two power supplies. Resistor R_B is needed only if the signal is to be capacitively coupled to the base. Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total β-independence of the bias current.

偏置电路方案3，自偏置：B和C连接一个较大电阻

$$V_{CC} = I_E R_C + I_B R_B + V_{BE}$$
$$= I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE}$$

$$\Rightarrow \quad I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta + 1)}$$

为了降低对β的敏感度，选择

$$R_B/(\beta + 1) \ll R_C$$

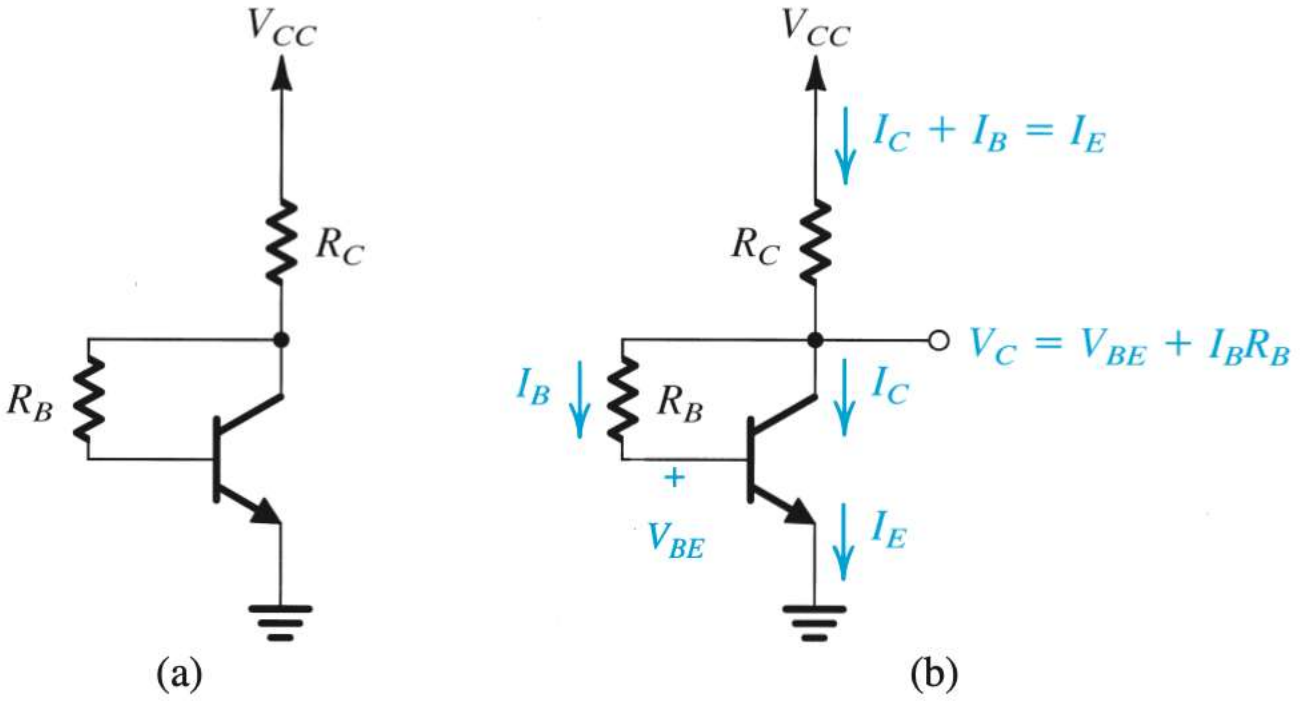
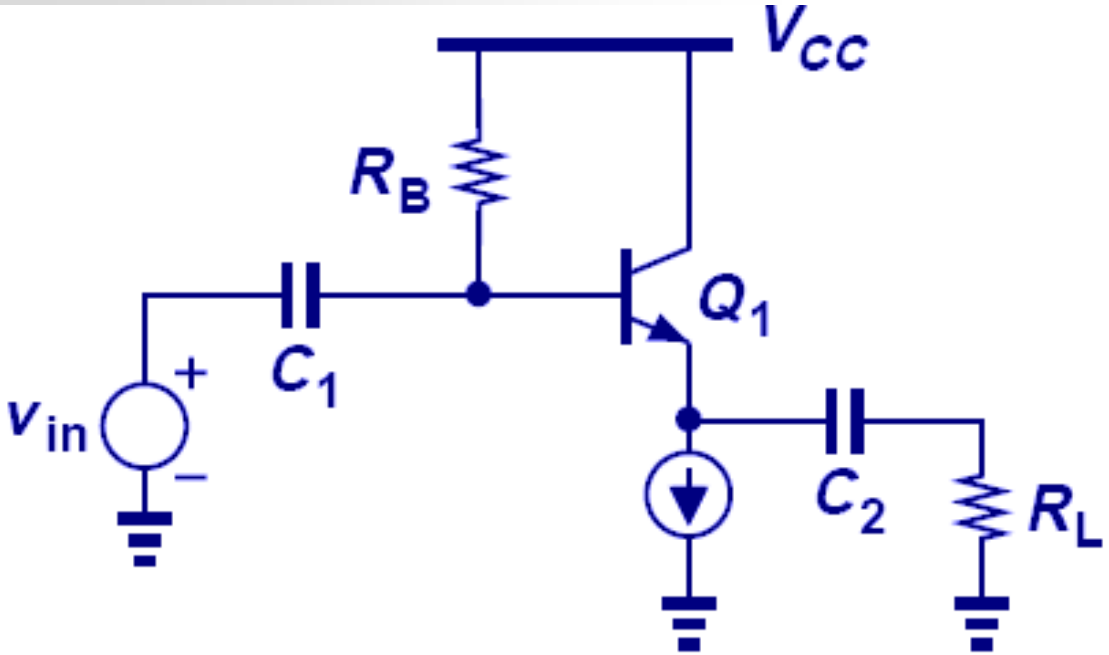


Figure 7.54 (**a**) A common-emitter transistor amplifier biased by a feedback resistor R_B. (**b**) Analysis of the circuit in (**a**).

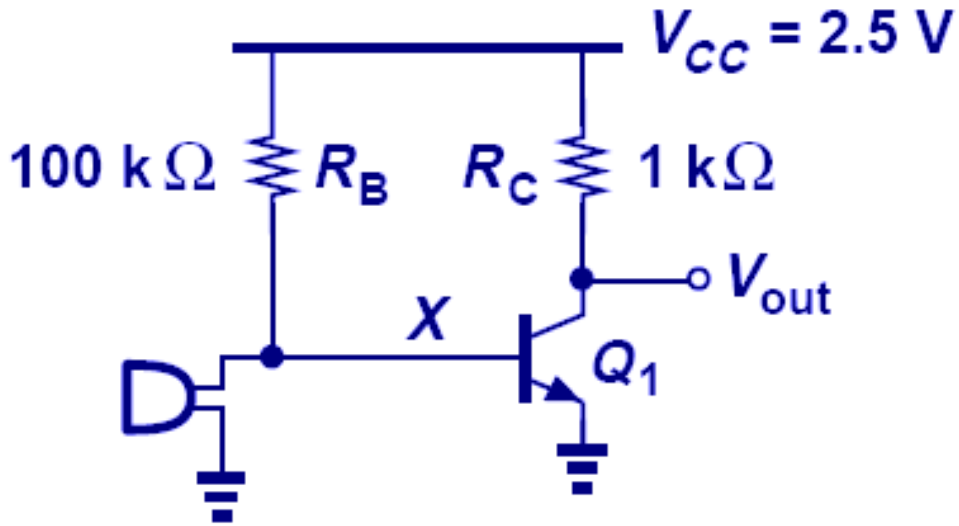
偏置电路方案4，恒流源确定I_C：集成电路中常用的偏置方案



- 也可通过在E极接一恒流源来偏置，此时 V_{BE}，I_BR_B 都有偏置恒流源决定，与供电电压V_{CC}无关.

完整PCB级电路分析（偏置电路 + 小信号放大电路）

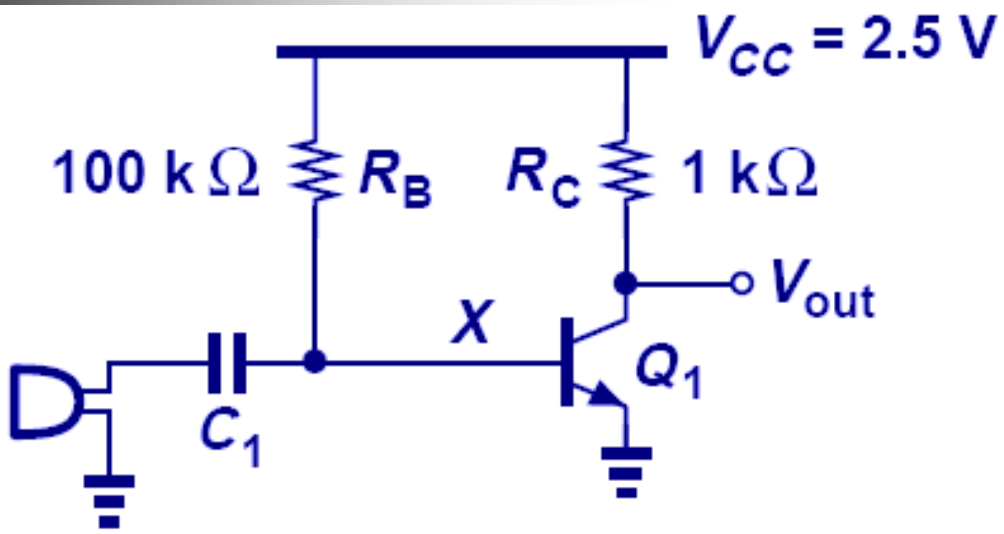
错误的输入连接



自偏置结构

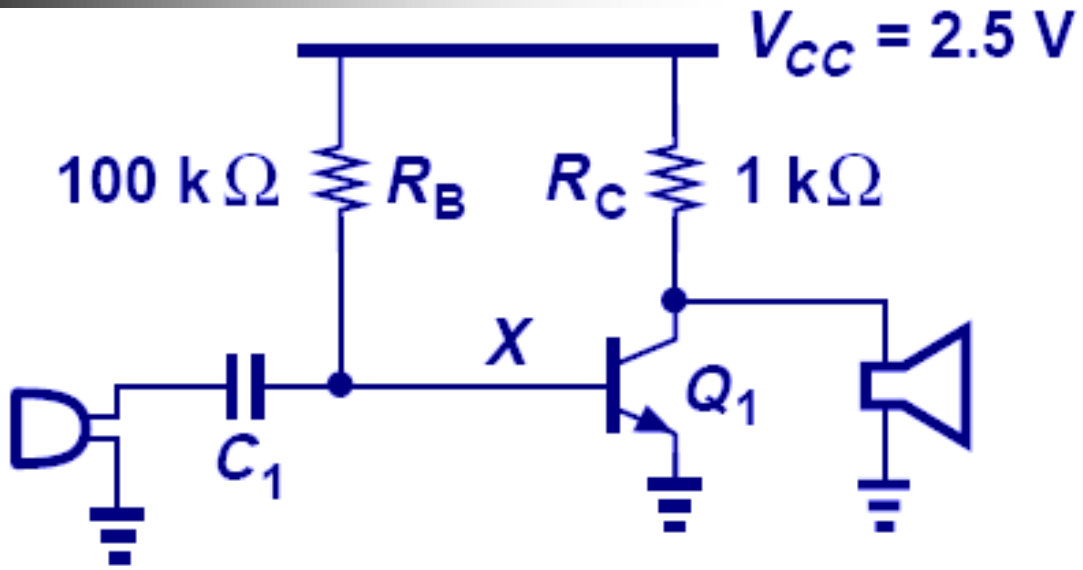
- 因为麦克风的阻抗很小，使得Q_1的B极经由一小电阻到地, 导致B极电压很小，从而不能正确偏置Q_1

使用耦合电容



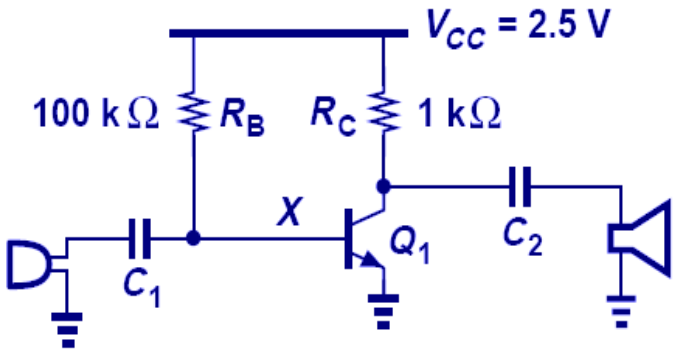
- DC：电容将偏置网络与麦克风相隔离；
- AC（交流小信号）：电容相当于短路，麦克风直接与放大电路相连；

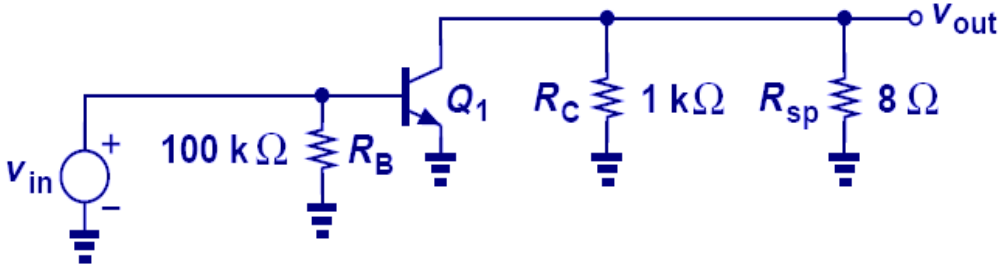
错误的输出连接



- 因为喇叭由螺线管（电感）构成，所以当其直接接到Q_1的C端时，将使C端短路，从而使三极管工作在深饱和区；

改进？

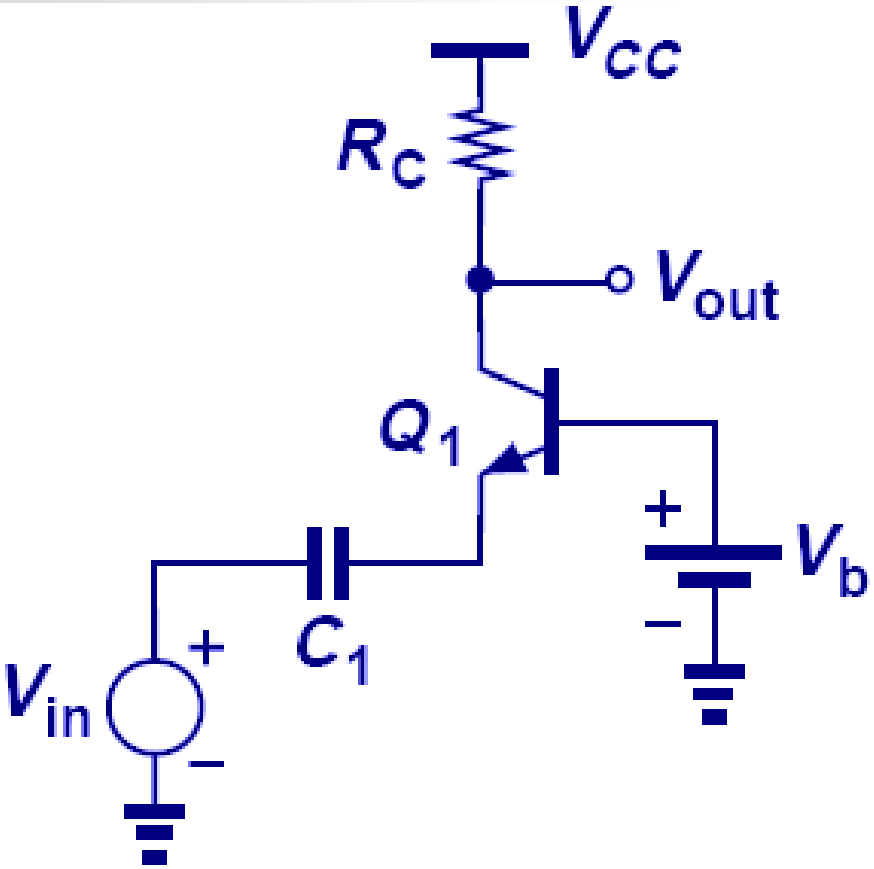




怎么解决？我们需要一个输入阻抗较大、输出阻抗较低的Buffer

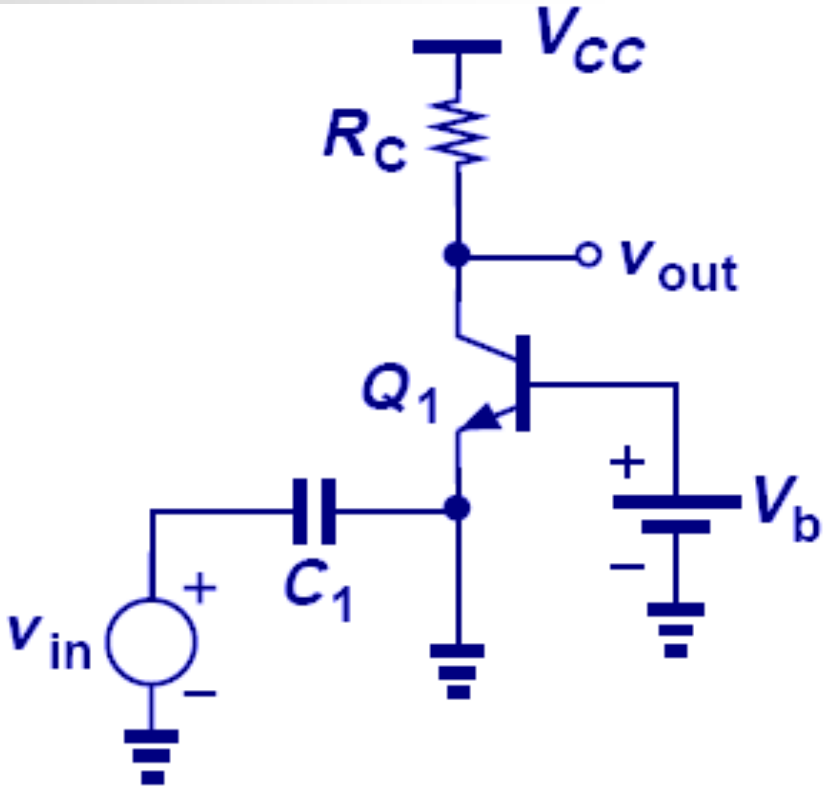
- 依旧没有增益：因为喇叭的输入阻抗很小，导致整体的电压增益很小；

错误的偏置网络



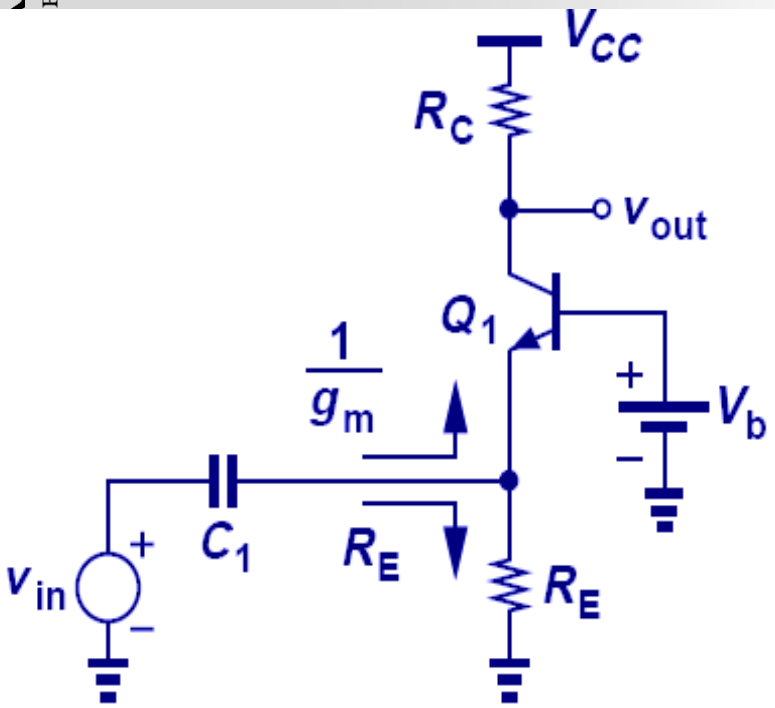
- E到GND没有直流通路

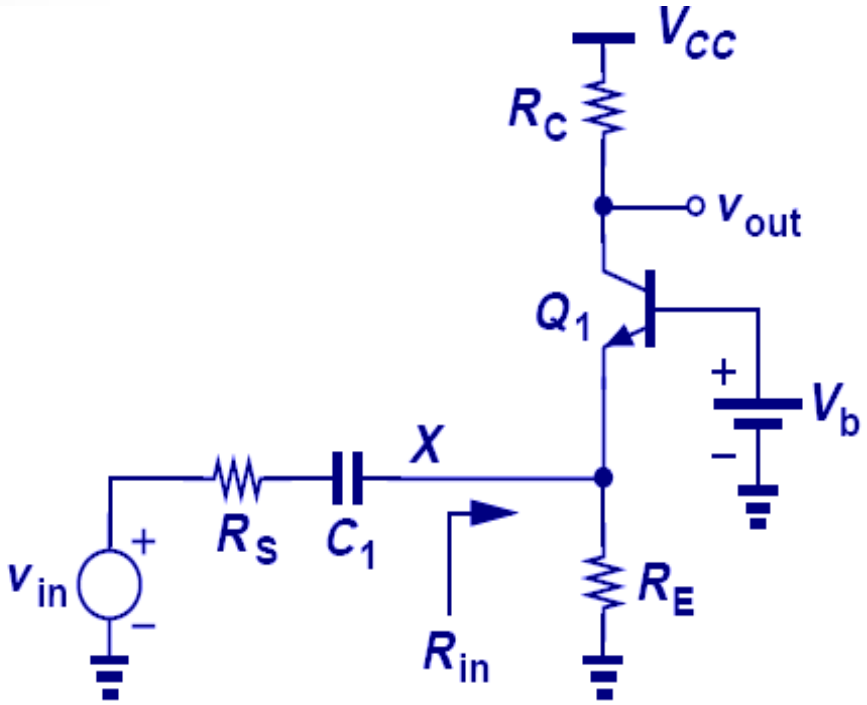
改进？



- 仍有问题。小信号分析时，输入信号被短路到GND；

合适的偏置网络





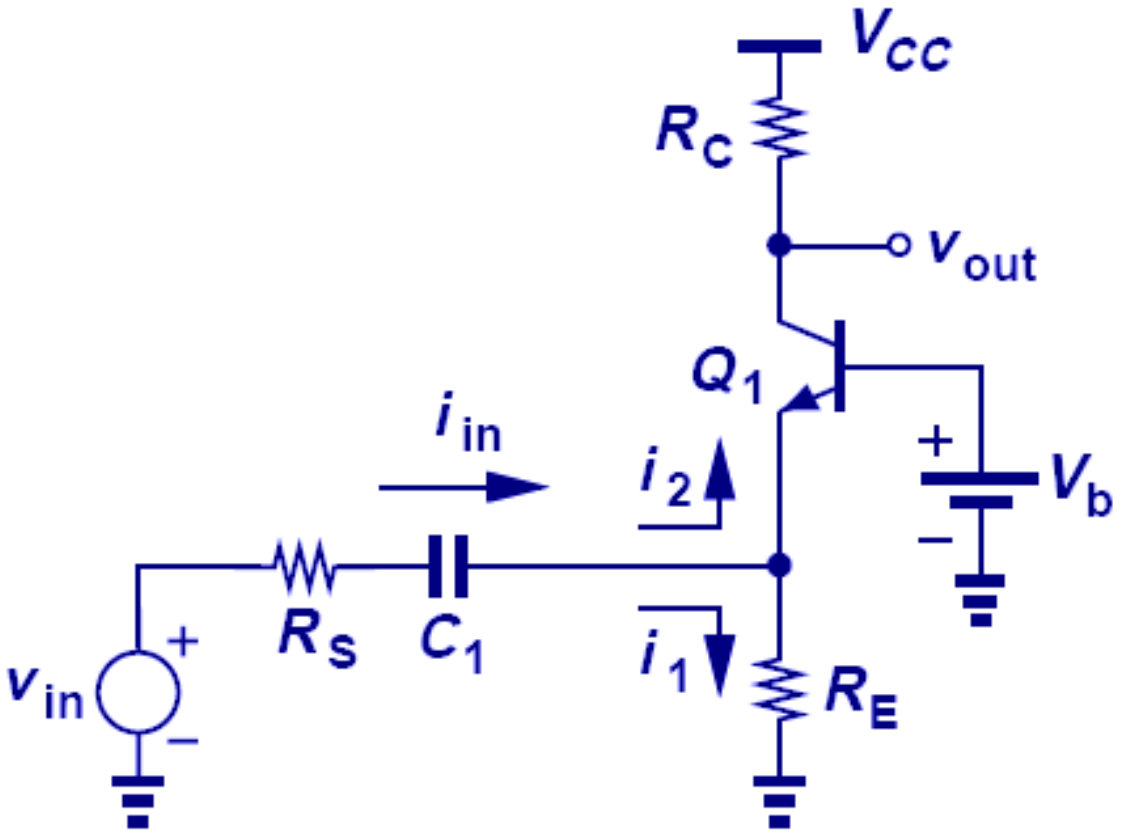
分级计算，v_{in}→X→v_{out}

$$R_{in} = \frac{1}{g_m} \| R_E$$

$$\frac{v_{out}}{v_{in}} = \frac{R_E}{R_E + (1 + g_m R_E) R_S} g_m R_C$$

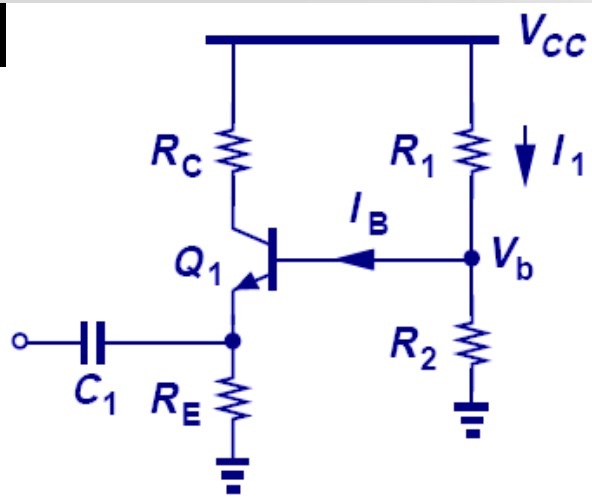
$$\frac{\frac{1}{g_m} || R_E}{\frac{1}{g_m} || R_E + R_S} \cdot g_m R_C$$

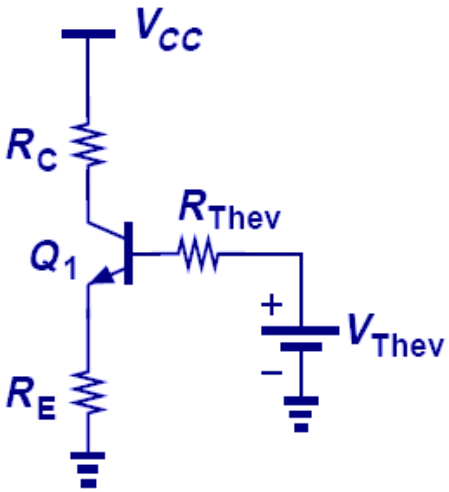
R_E导致输入阻抗的降低

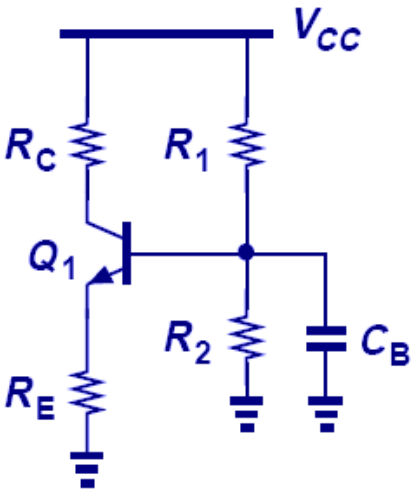


- R_E分流了部分电流到GND（这部分电流是浪费掉的）

如何获得V_b

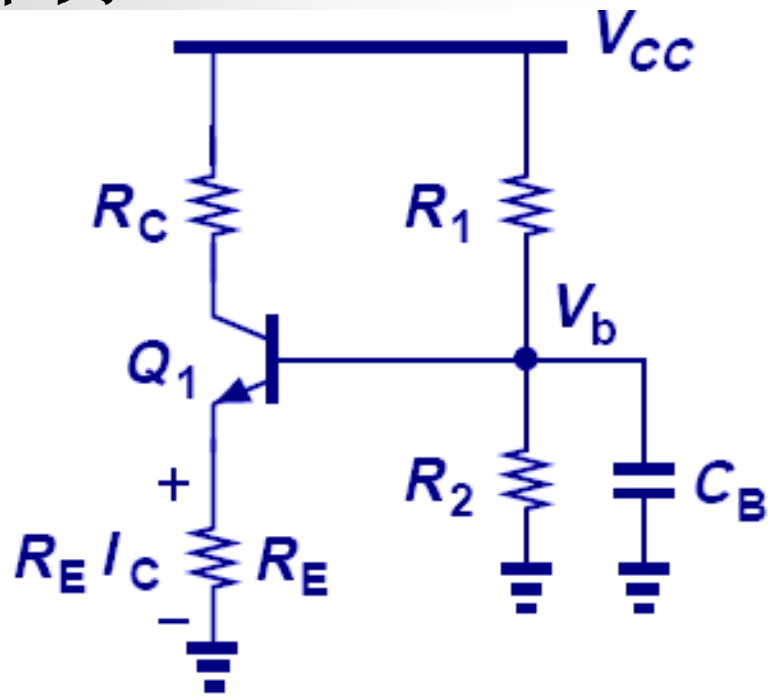






- 电阻分压：但降低了增益；
- 为了解决这个问题，可以在B极并联一电容C_B

举例



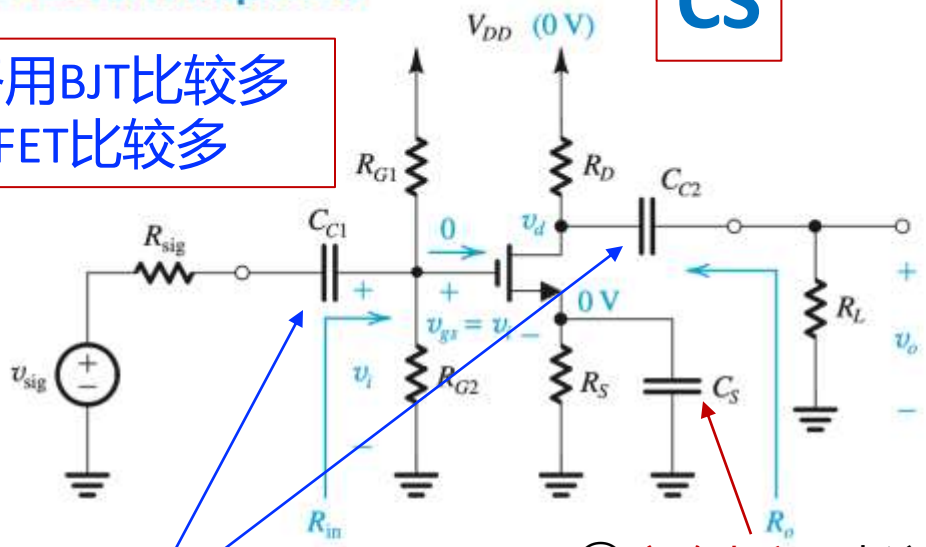
$$A_v \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

- 为了使R_E分流较小，需使$R_E >> 1/g_m$.
- R_1、R_2 分压获得 V_b，需保证流经R_1、R_2的电流远大于I_B;
- 电容如何选择？其折算到E之后的阻抗需远小于 $1/g_m$.

$$\frac{1}{\beta+1}\left|\frac{1}{C_B\omega}\right| = \frac{1}{20}\frac{1}{g_m}$$

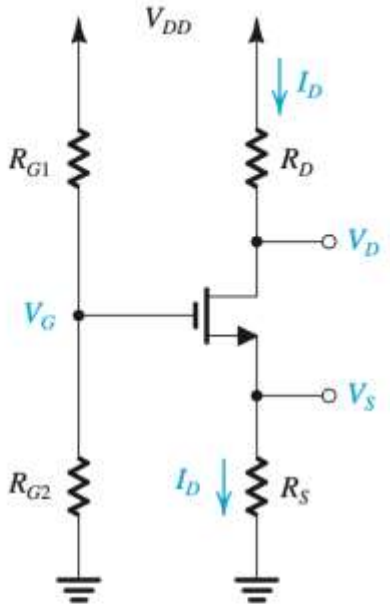
CS

分立电路用BJT比较多
IC用MOSFET比较多



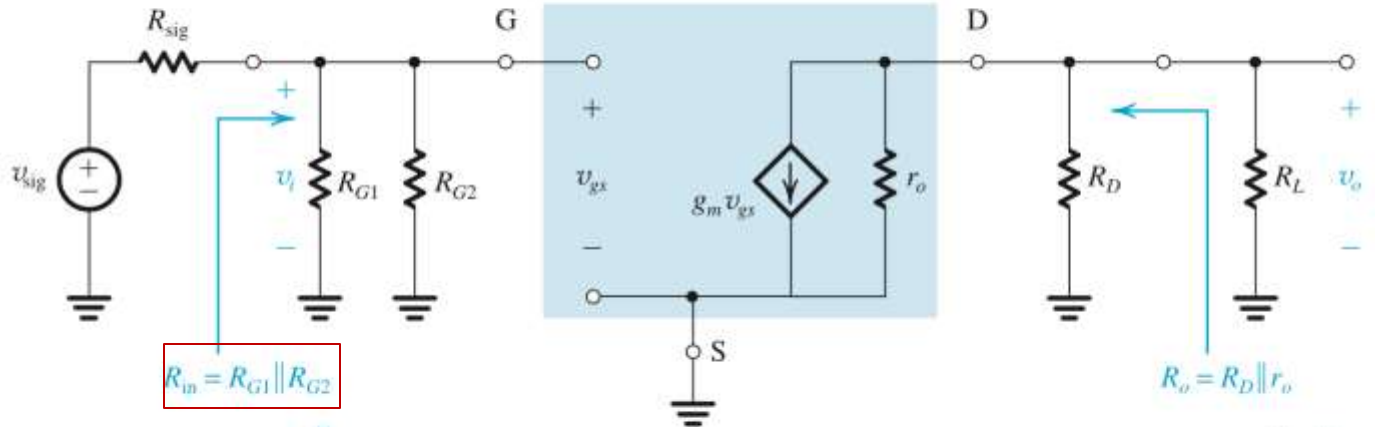
(a)

①隔直电容，隔离直流，通交流小信号



(b)

①旁路电容，直流开路
RS用来稳定直流工作点；
交流短路，CS结构

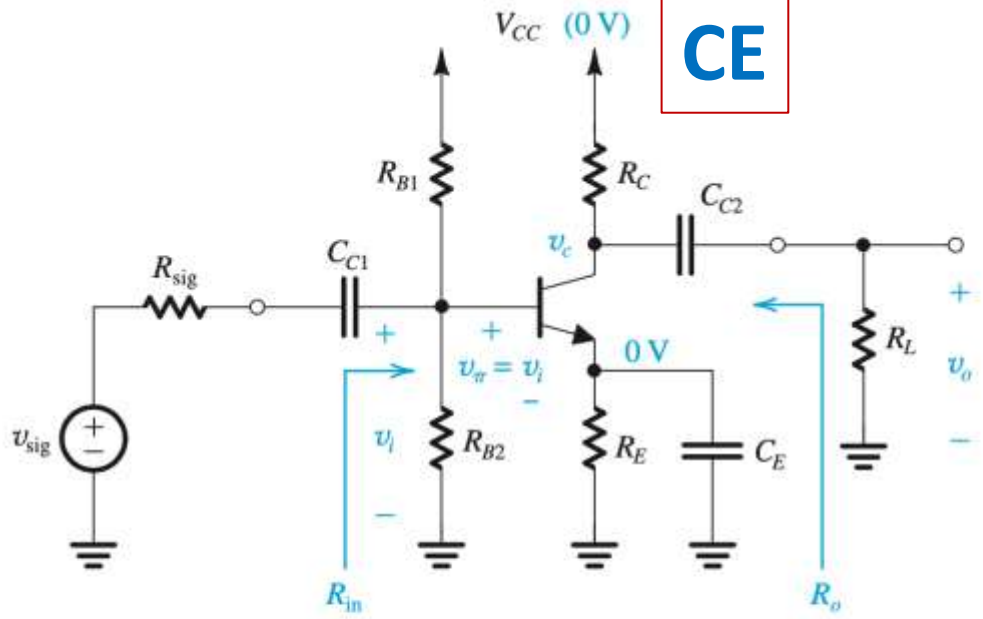


(c)

$$G_v = -\frac{R_{in}}{R_{in} + R_{sig}} g_m (R_D \| R_L \| r_o)$$

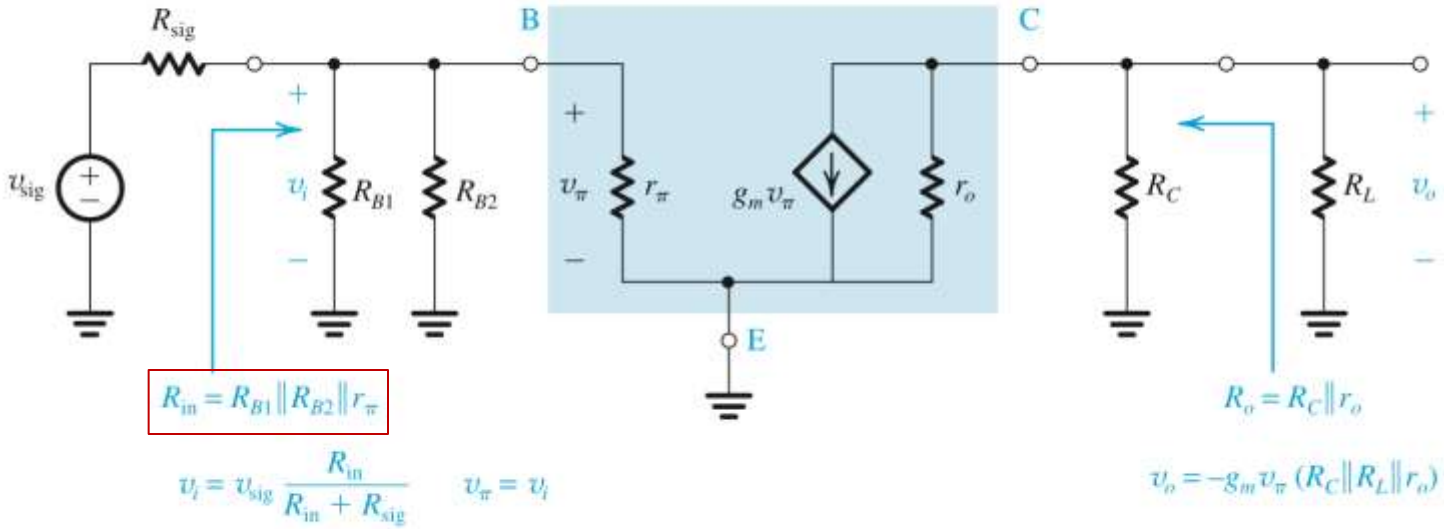
Figure 7.55 (a) A common-source amplifier using the classical biasing arrangement of Fig. 7.48(c). (b) Circuit for determining the bias point. (c) Equivalent circuit and analysis.

CE



(a)

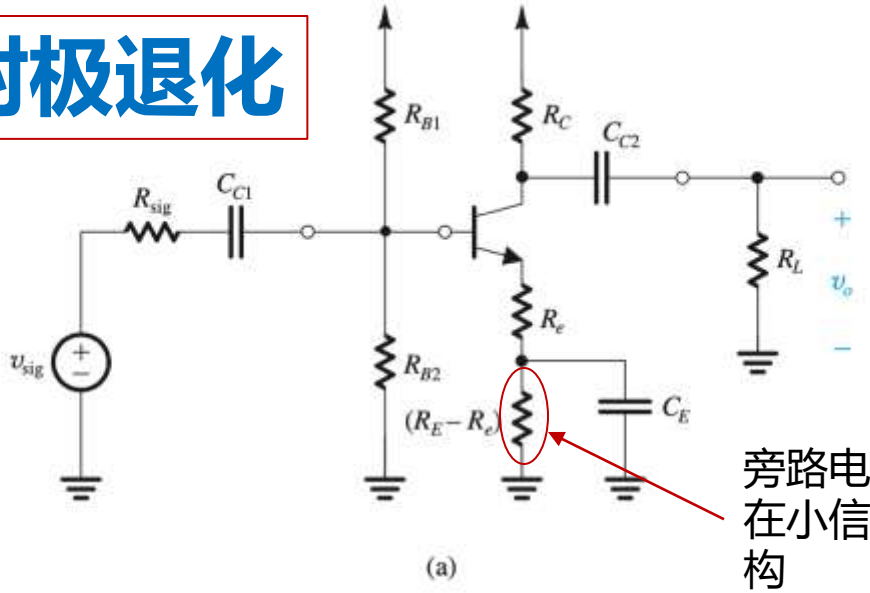
$$G_v = -\frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} g_m (R_C \| R_L \| r_o)$$



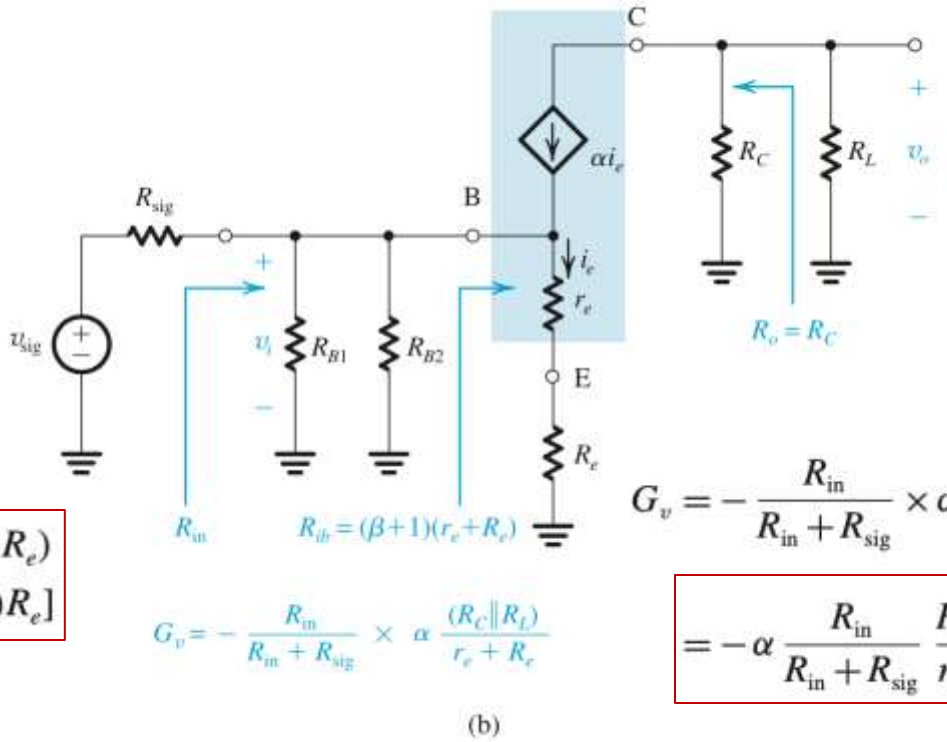
(b)

Figure 7.56 (**a**) A common-emitter amplifier using the classical biasing arrangement of Fig. 7.52(a). (**b**) Equivalent circuit and analysis.

射极退化



旁路电容只旁路部分反馈电阻，在小信号分析时，是射极退化结构

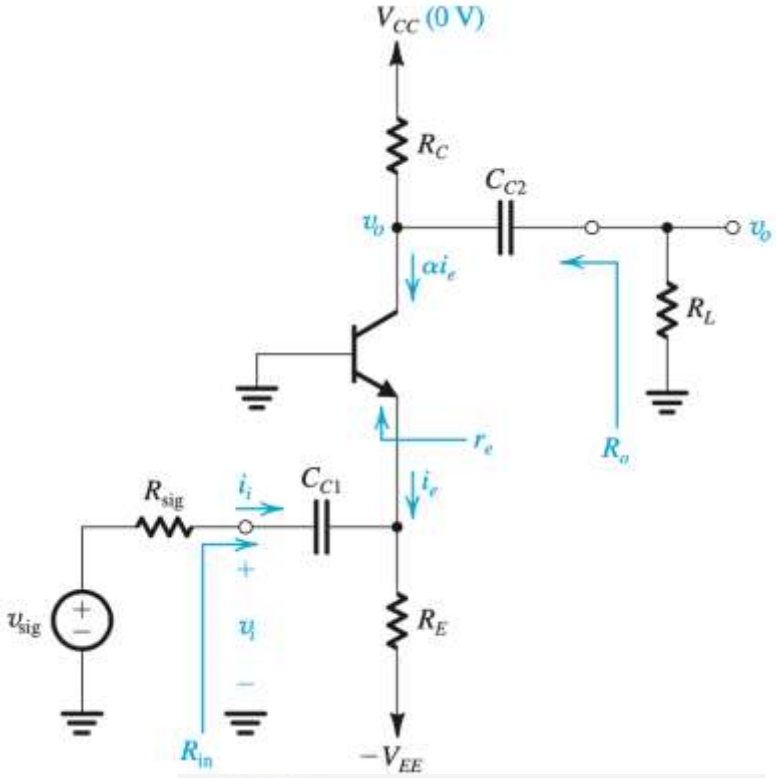


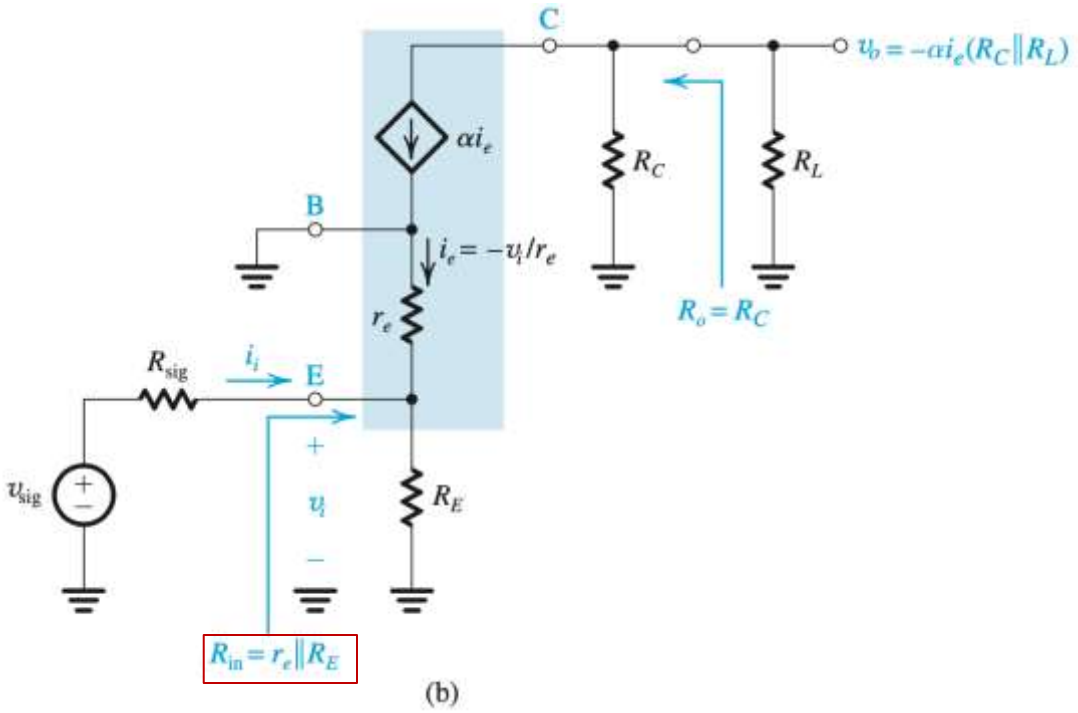
$$R_{in} = R_{B1} \| R_{B2} \| (\beta+1)(r_e+R_e)$$
$$= R_{B1} \| R_{B2} \| [r_\pi + (\beta+1)R_e]$$

$$G_v = -\frac{R_{in}}{R_{in}+R_{sig}} \times \alpha \frac{\text{Total resistance in collector}}{\text{Total resistance in emitter}}$$

$$= -\alpha \frac{R_{in}}{R_{in}+R_{sig}} \frac{R_C \| R_L}{r_e+R_e}$$

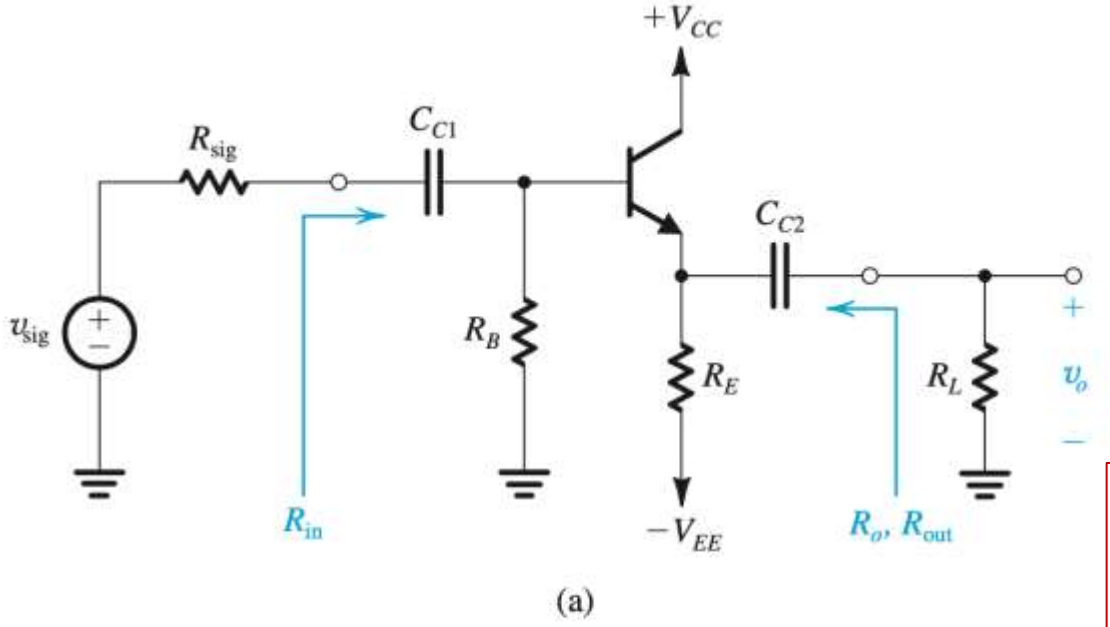
Figure 7.57 (**a**) A common-emitter amplifier with an unbiased emitter resistance R_e. (**b**) The amplifier small-signal model and analysis.





$$G_v = \alpha \frac{R_{in}}{R_{in} + R_{sig}} \frac{R_C \| R_L}{r_e} = \frac{R_{in}}{R_{in} + R_{sig}} g_m (R_C \| R_L)$$

射极跟随

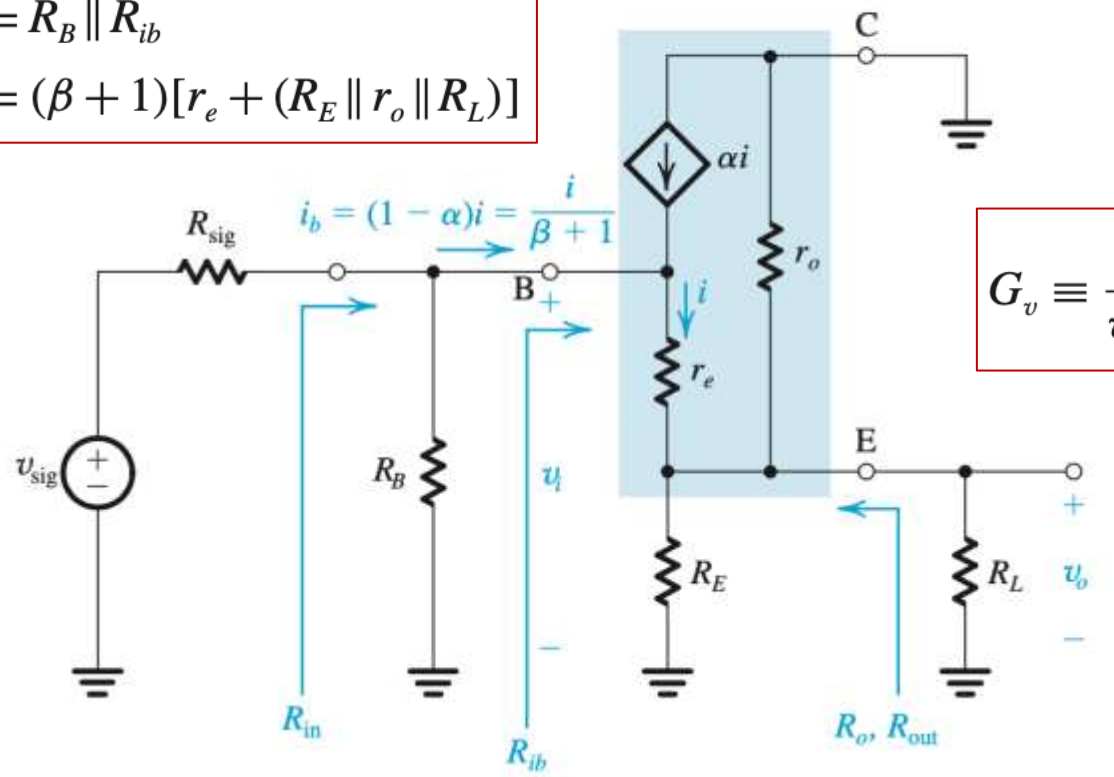


(a)

$$R_{\text{out}} = r_o \,\|\, R_E \,\|\, \left[r_e + \frac{R_B \,\|\, R_{\text{sig}}}{\beta + 1} \right]$$

$$R_{\text{in}} = R_B \,\|\, R_{ib}$$

$$R_{ib} = (\beta + 1)[r_e + (R_E \,\|\, r_o \,\|\, R_L)]$$



$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \frac{(R_E \,\|\, r_o \,\|\, R_L)}{r_e + (R_E \,\|\, r_o \,\|\, R_L)}$$

频率响应

信号频率较低时，隔直电容和旁路电容不能做理想化处理，会引起增益降低

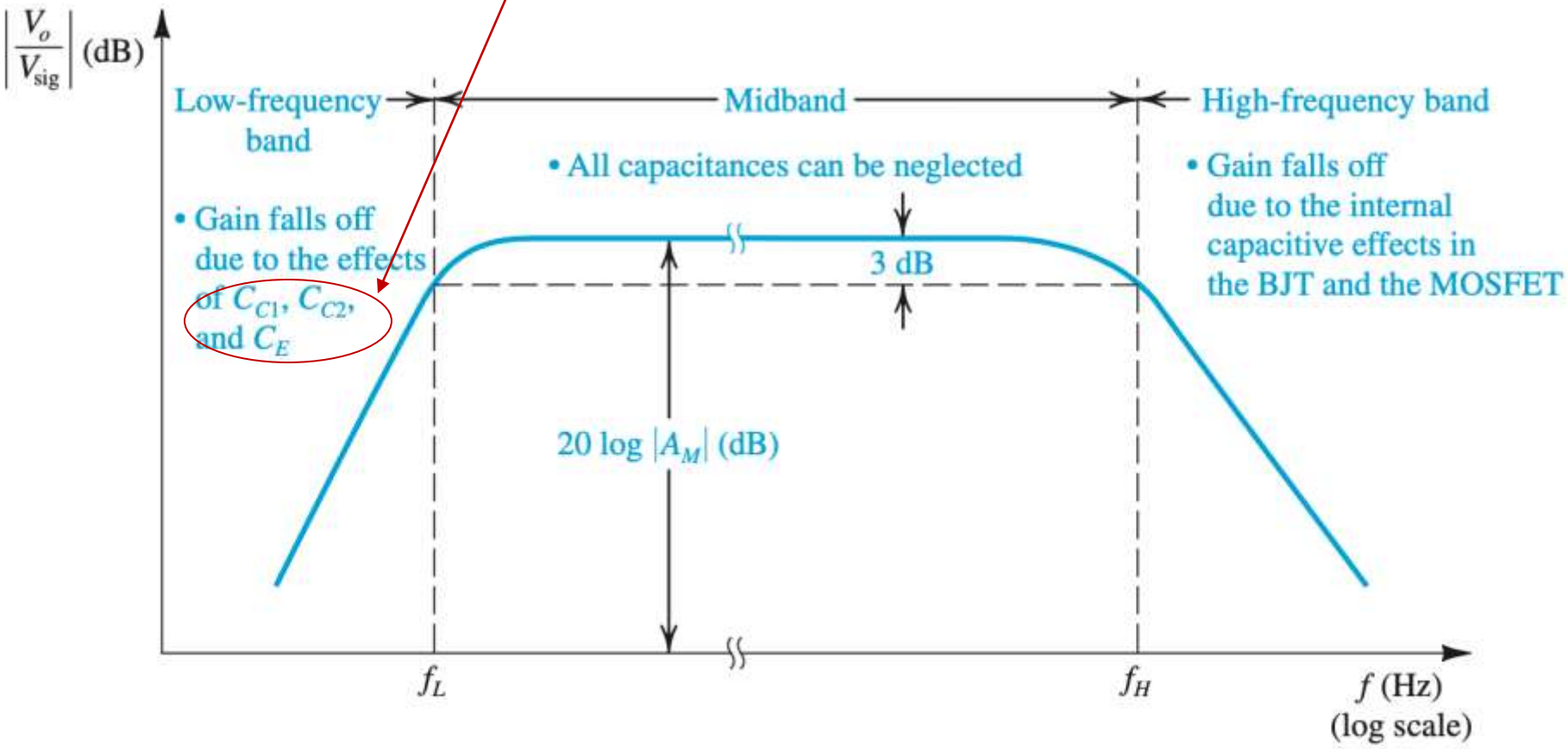
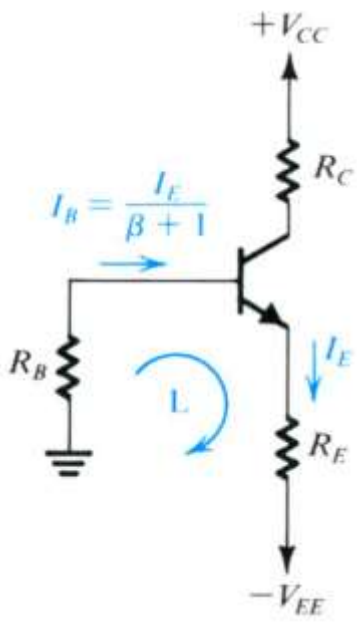


Figure 7.60 Sketch of the magnitude of the gain of a CE (Fig. 7.56) or CS (Fig. 7.55) amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency-response determination.

作业

D7.36 The bias arrangement of Fig. 7.55 is to be used for a common-base amplifier. Design the circuit to establish a dc emitter current of 1 mA and provide the highest possible voltage gain while allowing for a signal swing at the collector of ±2 V. Use +10-V and –5-V power supplies.

Ans. $R_B = 0$; $R_E = 4.3\ \text{k}\Omega$; $R_C = 8.4\ \text{k}\Omega$



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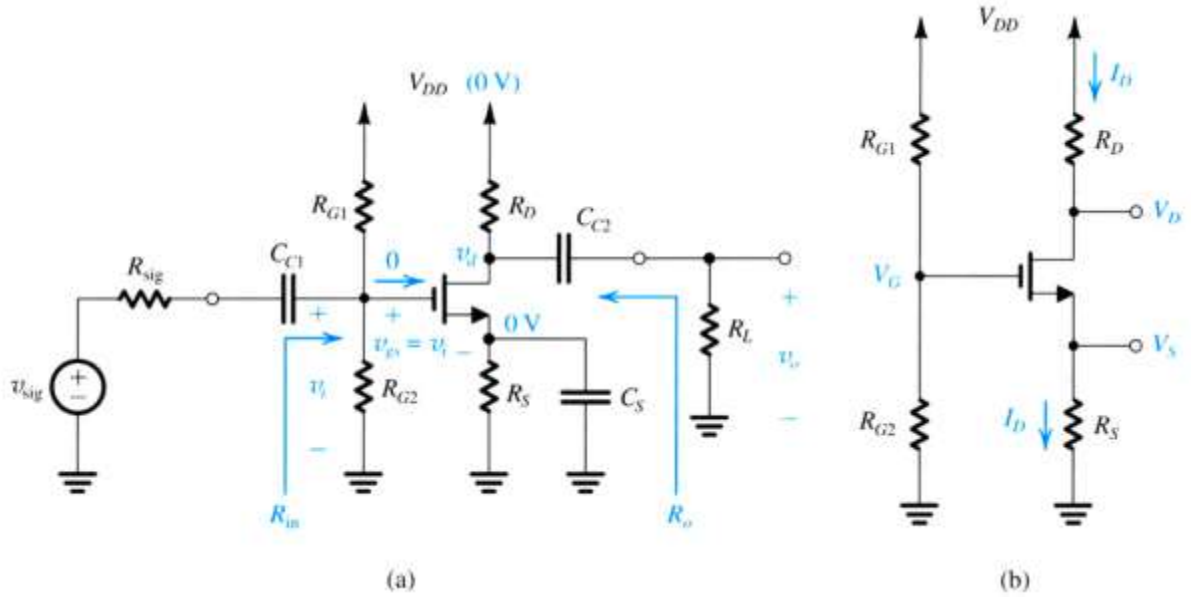
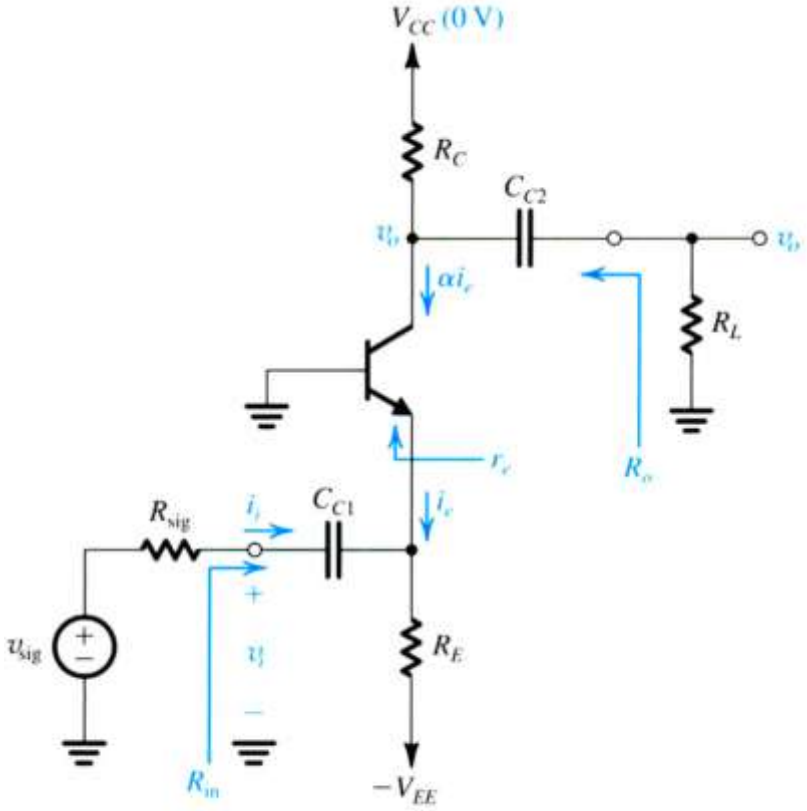
D7.38 Design the bias circuit in Fig.7.57(b) for the CS amplifier of Fig. 7.57(a). Assume the MOSFET is specified to have $V_t = 1$ V, $k_n = 4$ mA/V^2, and $V_A = 100$ V. Neglecting the Early effect, design for $I_D = 0.5$ mA, $V_S = 3.5$ V, and $V_D = 6$ V using a power-supply $V_{DD} = 15$ V. Specify the values of R_S and R_D. If a current of 2 μA is used in the voltage divider, specify the values of R_{G1} and R_{G2}. Give the values of the MOSFET parameters g_m and r_o at the bias point.

Ans. $R_S = 7$ kΩ; $R_D = 18$ kΩ; $R_{G1} = 5$ MΩ; $R_{G2} = 2.5$ MΩ; $g_m = 2$ mA/V; $r_o = 200$ kΩ



D7.44 Design the CB amplifier of Fig. 7.60(a) to provide an input resistance R_{in} that matches the source resistance of a cable with a characteristic resistance of 50 Ω. Assume that $R_E \gg r_e$. The available power supplies are ±5 V and $R_L = 8$ kΩ. Design for a dc collector voltage $V_C = +1$ V. Specify the values of R_C and R_E. What is the overall voltage gain? If v_{sig} is a sine wave with a peak amplitude of 10 mV, what is the peak amplitude of the output voltage? Let $\alpha \simeq 1$.

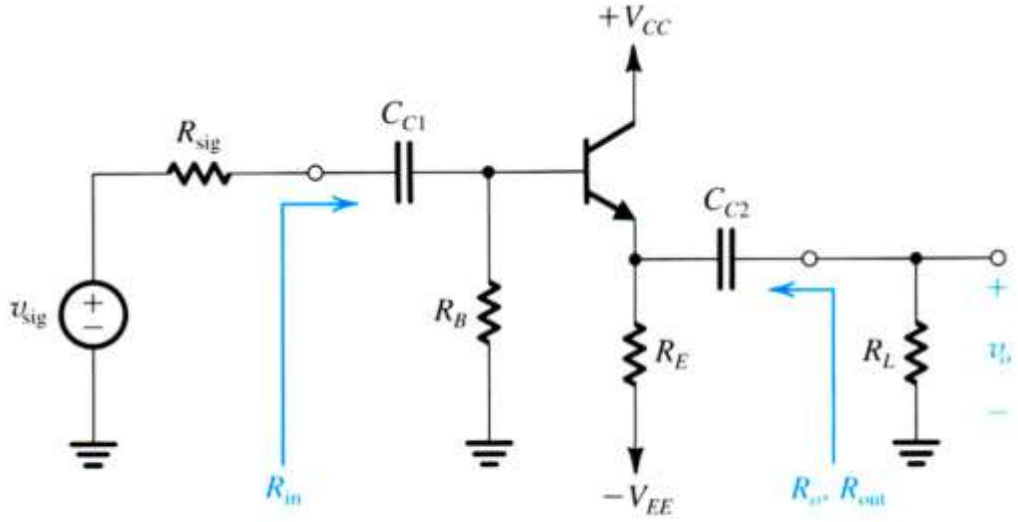
Ans. $R_C = 8$ kΩ; $R_E = 8.6$ kΩ; 40 V/V; 0.4 V



(a)

D7.45 Design the emitter follower of Fig. 7.61(a) to operate at a dc emitter current $I_E = 1$ mA. Allow a dc voltage drop across R_B of 1 V. The available power supplies are ± 5 V, $\beta = 100$, $V_{BE} = 0.7$ V, and $V_A = 100$ V. Specify the values required for R_B and R_E. If $R_{sig} = 50$ kΩ and $R_L = 1$ kΩ, find R_{in}, v_i/v_{sig}, v_o/v_i, G_v, and R_{out}. (*Note*: In the bias design, neglect the Early effect.)

Ans. $R_B = 100$ kΩ; $R_E = 3.3$ kΩ; 44.3 kΩ; 0.469 V/V; 0.968 V/V; 0.454 V/V; 320 Ω



(a)