

Lecture 17 – BJT-part2

Chapter 6 from **Microelectronic
Circuits** Text by Sedra and Smith
Oxford Publishing

BJT 电路直流分析

即求Q point

- 基于 BJT 的“电流电压”约束关系
- 基于基本电路原理与分析方法
- 为简单起见,
 - 若无明确说明, 一般我们不考虑厄雷效应
 - 开启时, $|V_{BE}| = 0.7 \text{ V}$
 - 饱和区 $|V_{CE}| = 0.2 \text{ V}$ 中间过渡区不用管
 - 放大区 $V_C > V_B - 0.4 \text{ V}$ (nnp) 或 $V_C < V_B + 0.4 \text{ V}$ (pnp)
- 假设-验证
 - 假设工作在放大区, 验证C点电压最低不得低于B点-0.4 (nnp) ; 或C点电压最高不得高于B点+0.4 (pnp)
 - 假设工作在饱和区, 验证 β 小于标称值 ($\beta_{\text{forced}} < \beta$) 饱和区 β 比较小

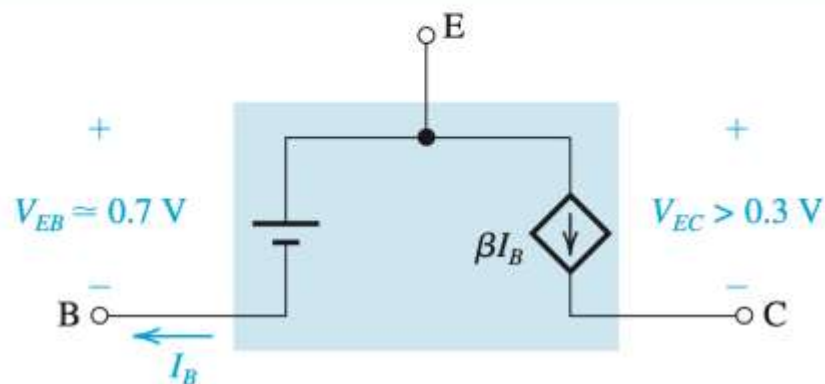
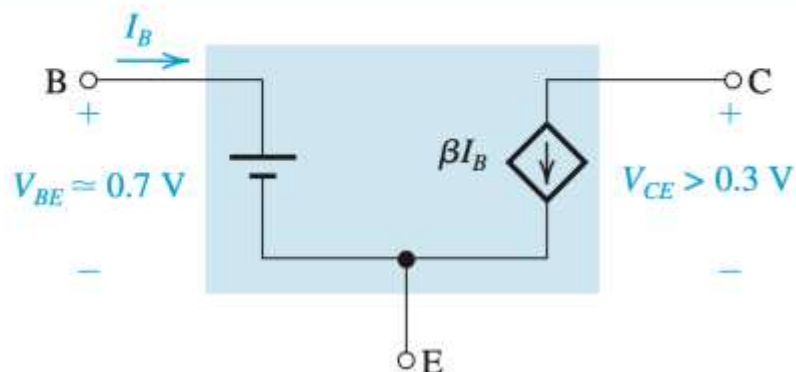
Table 6.3 Simplified Models for the Operation of the BJT in DC Circuits

nnp

pnnp

Active
EBJ:
Forward
Biased

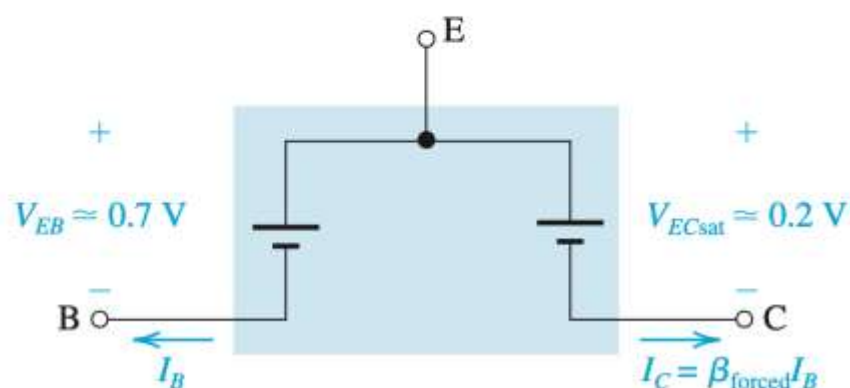
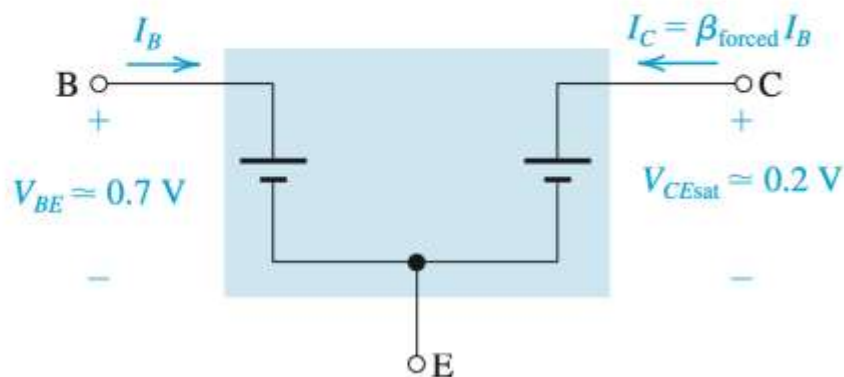
CBJ:
Reverse
Biased



这里当作电流控制电
流，实际上电压控制
也同理

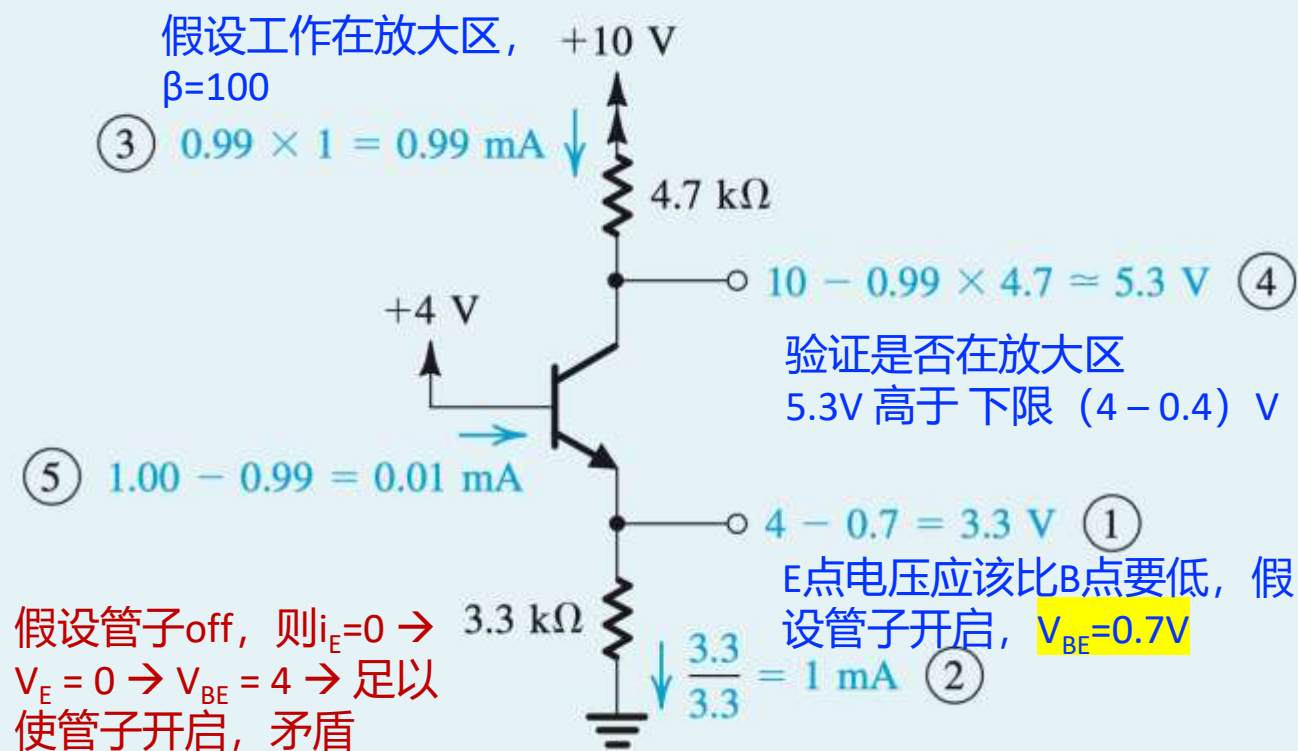
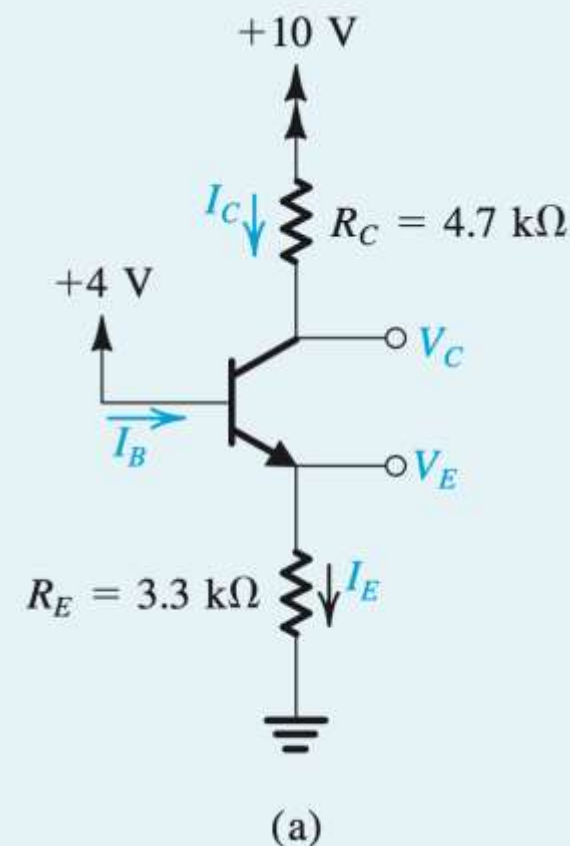
Saturation
EBJ:
Forward
Biased

CBJ:
Forward
Biased



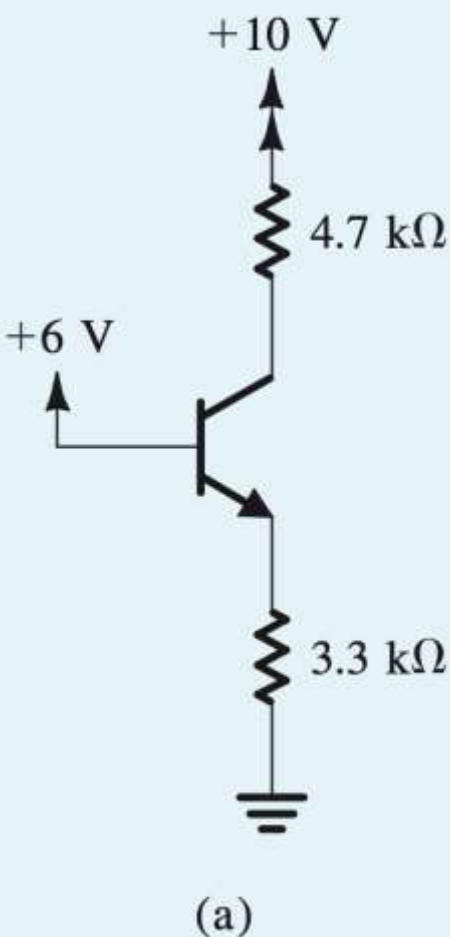
Example 6.4

Consider the circuit shown in Fig. 6.23(a), which is redrawn in Fig. 6.23(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that β is specified to be 100.



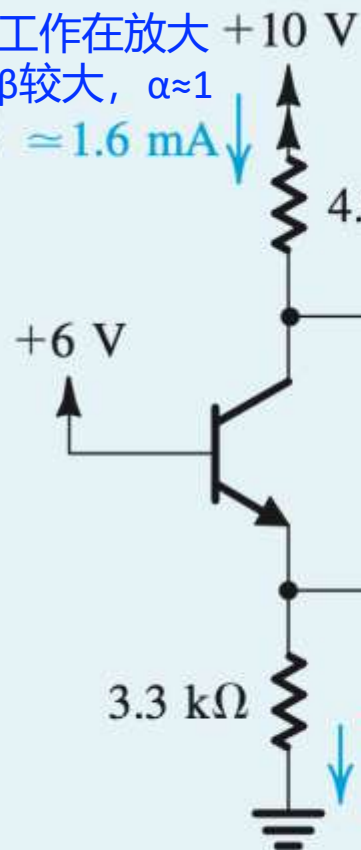
养成在电路图上直接进行分析的习惯

We wish to analyze the circuit of Fig. 6.24(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 6.23 except that the voltage at the base is now +6 V. Assume that the transistor β is specified to be *at least* 50.



假设工作在放大区, β 较大, $\alpha \approx 1$

③ $\approx 1.6 \text{ mA}$



验证是否在放大区 (c点电压最低不得低于6-0.4)

$$10 - 1.6 \times 4.7 = \cancel{2.48} \quad (4)$$

Impossible, not in active mode

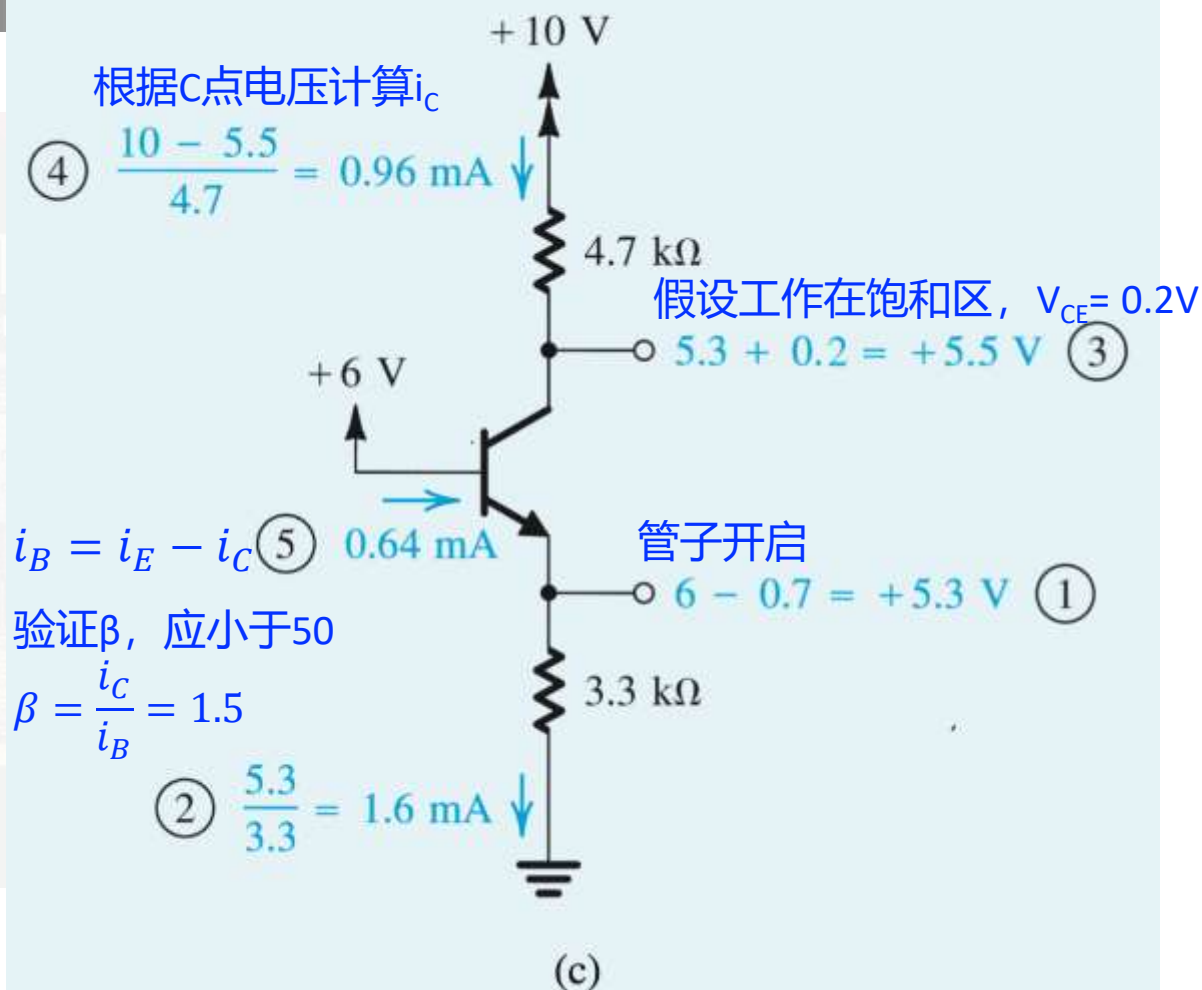
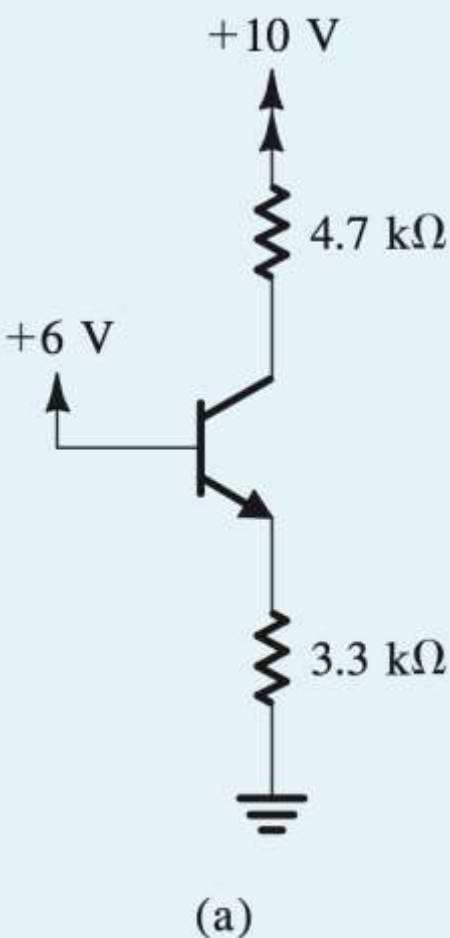
假设错误, 所以不是工作在放大区
→ 工作在饱和区

管子开启

$$6 - 0.7 = +5.3 \text{ V} \quad (1)$$

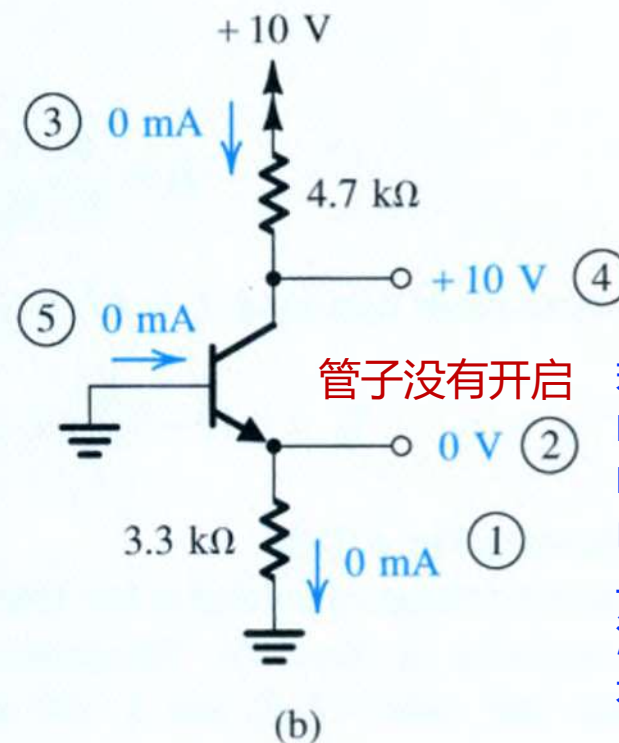
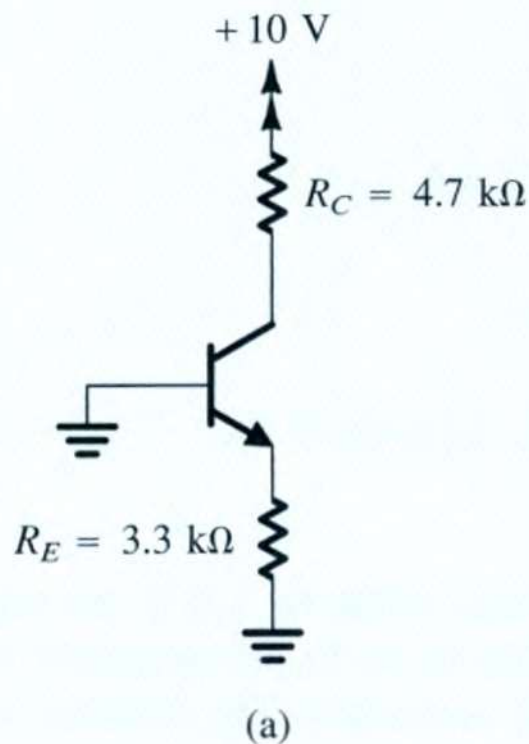
$$\frac{5.3}{3.3} = 1.6 \text{ mA} \quad (2)$$

We wish to analyze the circuit of Fig. 6.24(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 6.23 except that the voltage at the base is now +6 V. Assume that the transistor β is specified to be *at least* 50. 意思是放大区至少为50V



Example 6.6

We want to analyze the circuit in Fig. 6.25(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to the one considered in Examples 6.4 and 6.5 except that now the base voltage is zero.

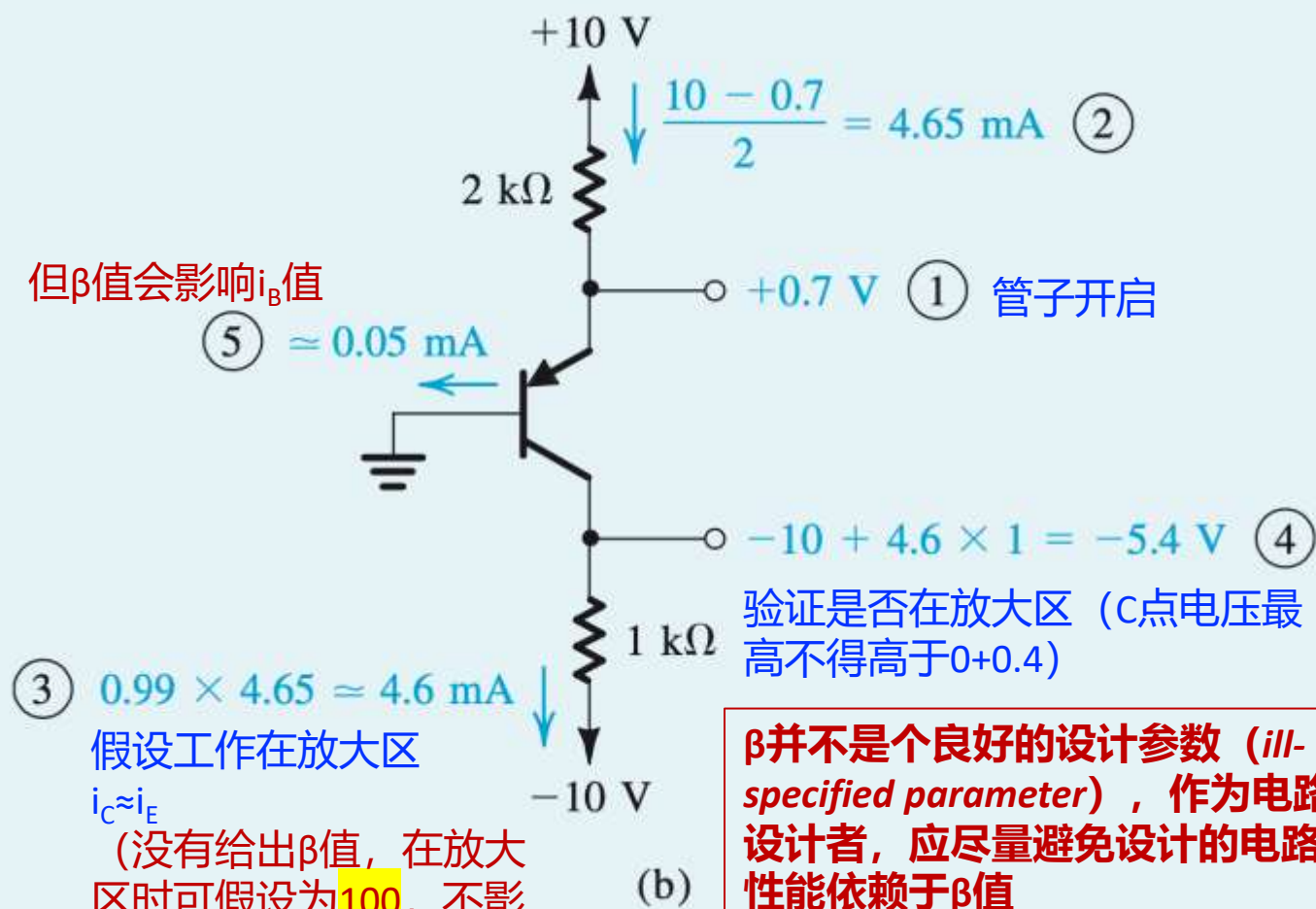
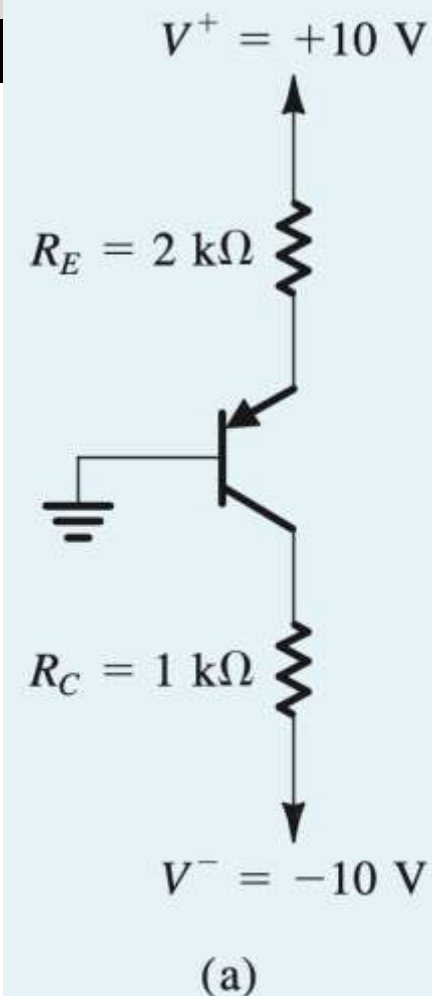


管子没有开启

若开启, E点电压-0.7V, 电流从地流到E, 再流到B, 与正偏pn结电流只能从p到n矛盾

Figure 6.25 Example 6.6: (a) circuit; (b) analysis, with the order of the analysis steps indicated by circled numbers.

We want to analyze the circuit of Fig. 6.26(a) to determine the voltages at all nodes and the currents through all branches.



(没有给出 β 值, 在放大区时可假设为100, 不影响C点电压, 即不影响管子是否在放大区的验证)

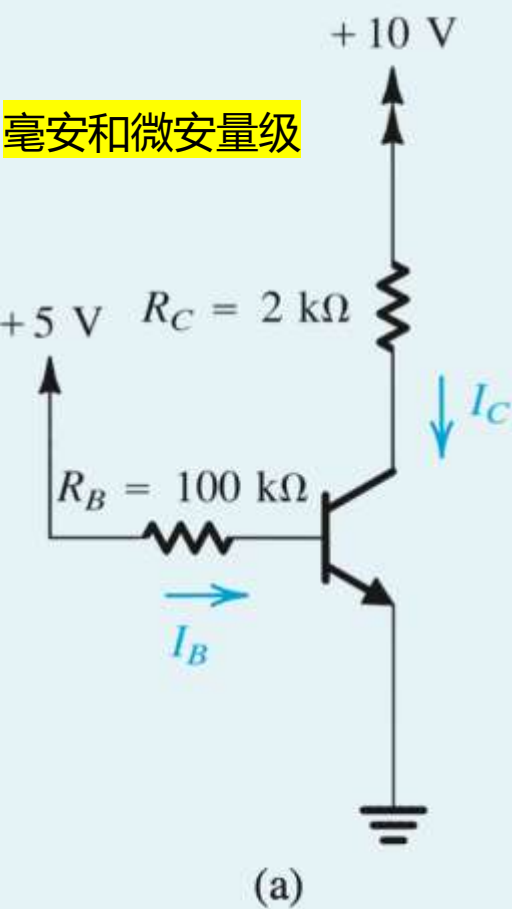
β 并不是个良好的设计参数 (*ill-specified parameter*), 作为电路设计者, 应尽量避免设计的电路性能依赖于 β 值

* 该电路, β 若变化15% $\rightarrow 115$, 不影响 i_C , 也不影响工作区域

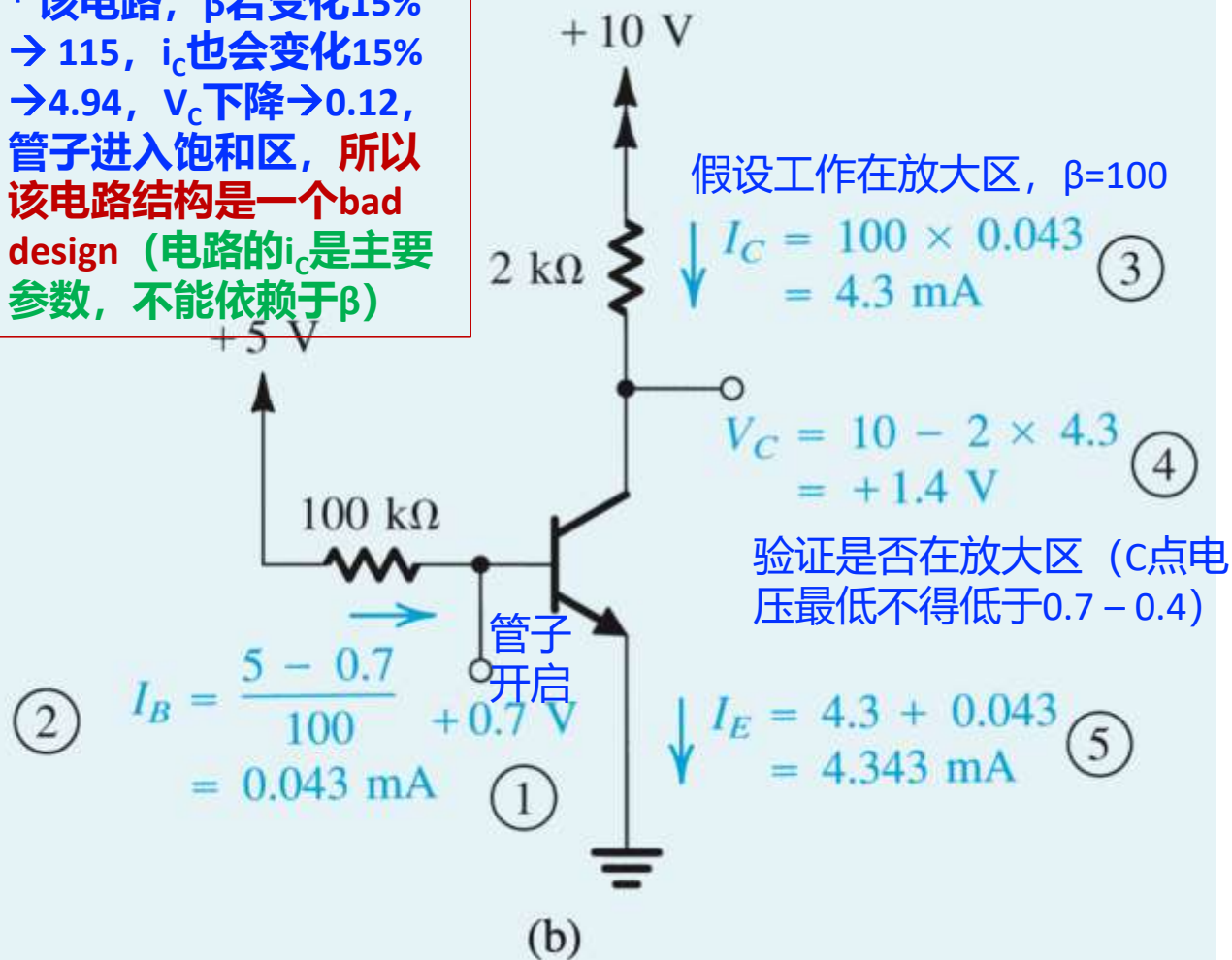
Example 6.8

We want to analyze the circuit in Fig. 6.27(a) to determine the voltages at all nodes and the currents in all branches. Assume $\beta = 100$.

毫安和微安量级

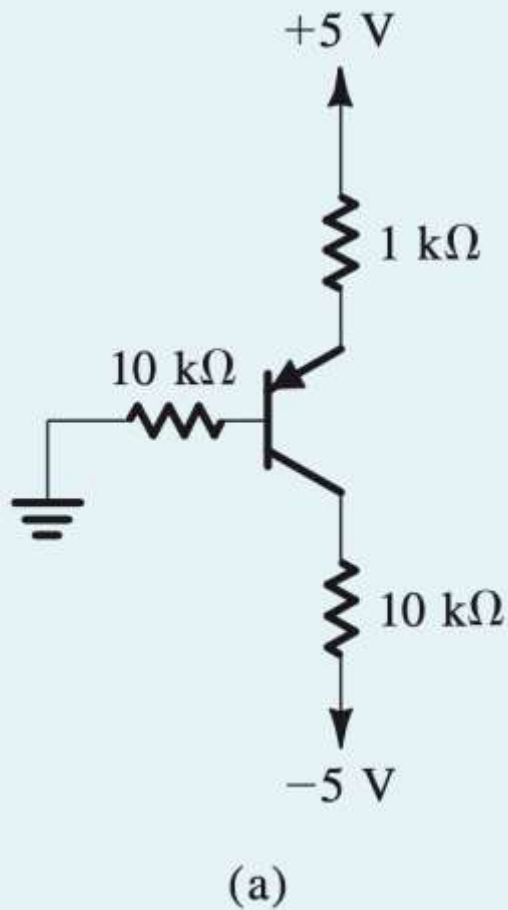


* 该电路, β 若变化15%
 $\rightarrow 115$, i_c 也会变化15%
 $\rightarrow 4.94$, V_C 下降 $\rightarrow 0.12$,
 管子进入饱和区, 所以
 该电路结构是一个bad
 design (电路的 i_c 是主要
 参数, 不能依赖于 β)



Example 6.9

We want to analyze the circuit of Fig. 6.28(a) to determine the voltages at all nodes and the currents through all branches. The minimum value of β is specified to be 30.



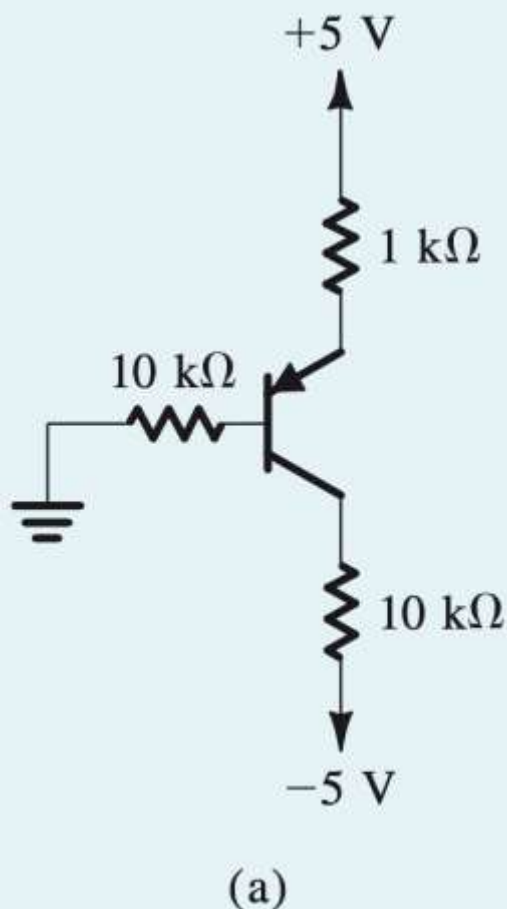
假设工作在放大区

B点电压略高于0V \rightarrow E点电压约等于0.7 V

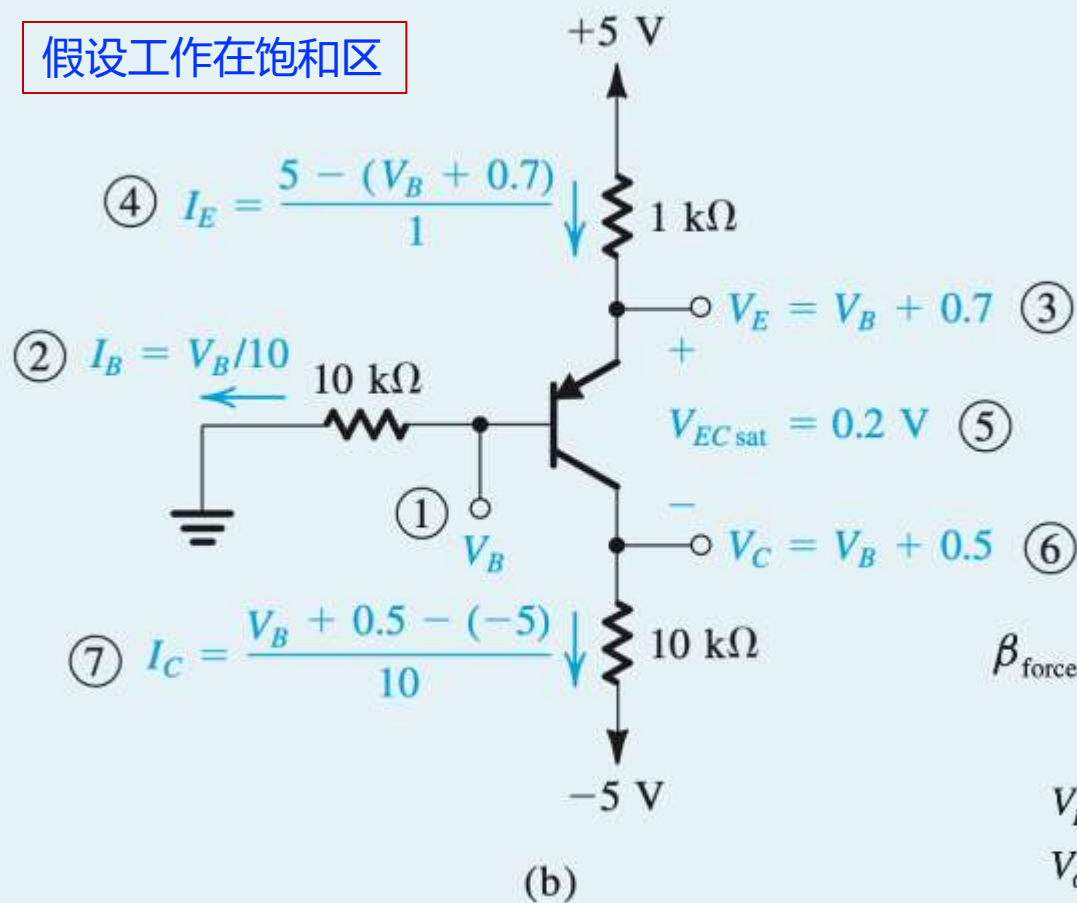
$\rightarrow i_E \approx 4.3 \text{ mA} \rightarrow i_C \approx 4.3 \text{ mA} \rightarrow V_C \approx -5 + 43 \text{ V}$ 不合理

Example 6.9

We want to analyze the circuit of Fig. 6.28(a) to determine the voltages at all nodes and the currents through all branches. The minimum value of β is specified to be 30.



假设工作在饱和区



< 30 合理

$$\beta_{\text{forced}} = \frac{0.86}{0.31} \simeq 2.8$$

$$V_E = 3.83 \text{ V}$$

$$V_C = 3.63 \text{ V}$$

$$I_E = 1.17 \text{ mA}$$

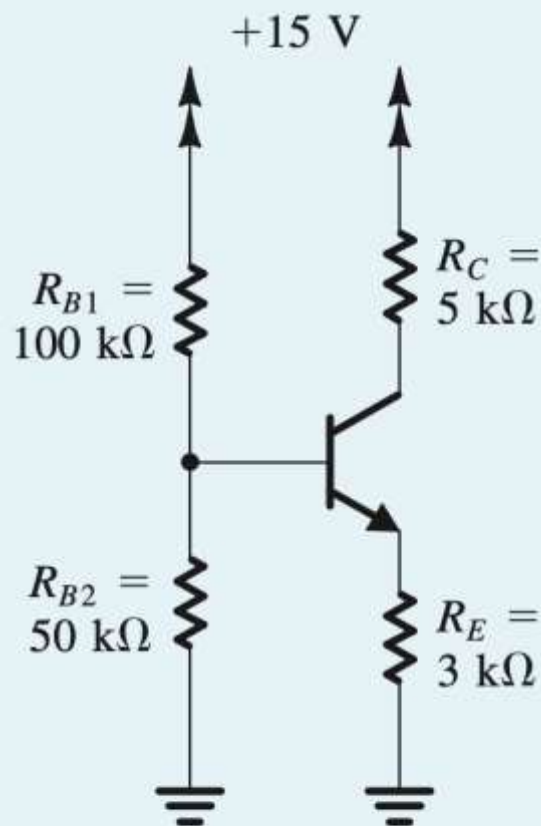
$$I_C = 0.86 \text{ mA}$$

$$I_B = 0.31 \text{ mA}$$

$$I_E = I_B + I_C \Rightarrow 4.3 - V_B = 0.1V_B + 0.1V_B + 0.55 \Rightarrow V_B = \frac{3.75}{1.2} \simeq 3.13 \text{ V}$$

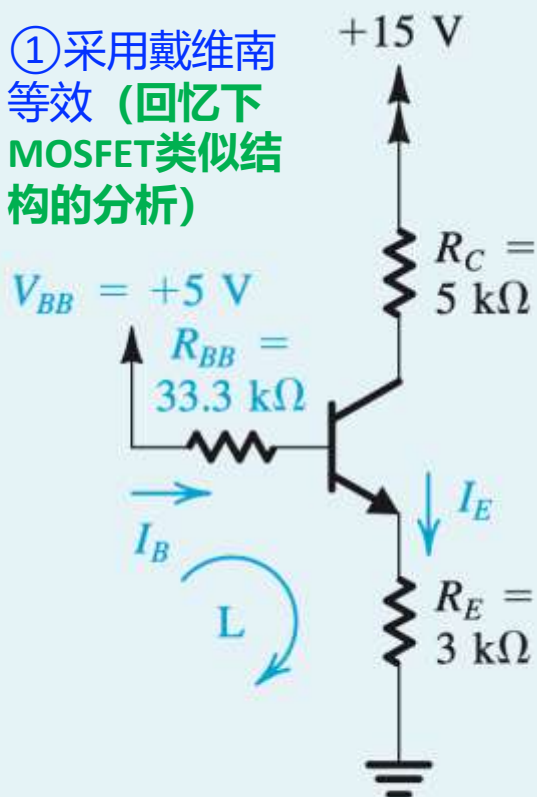
Example 6.10

We want to analyze the circuit of Fig. 6.29(a) to determine the voltages at all nodes and the currents through all branches. Assume $\beta = 100$.



(a)

①采用戴维南等效 (回忆下 MOSFET类似结构的分析)



(b)

②对loop L 写KVL方程 (注意流过 R_{BB} 的电流与流过 R_E 的电流不同)

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$$

③假设工作于放大区

$$I_B = \frac{I_E}{\beta + 1}$$

$$\Rightarrow I_E = \frac{V_{BB} - V_{BE}}{R_E + [R_{BB}/(\beta + 1)]} = 1.29 \text{ mA}$$

$$\Rightarrow I_B = 0.0128 \text{ mA}$$

$$I_C = \alpha I_E = 1.28 \text{ mA}$$

$$V_E = I_E \times R_E = 3.87 \text{ V}$$

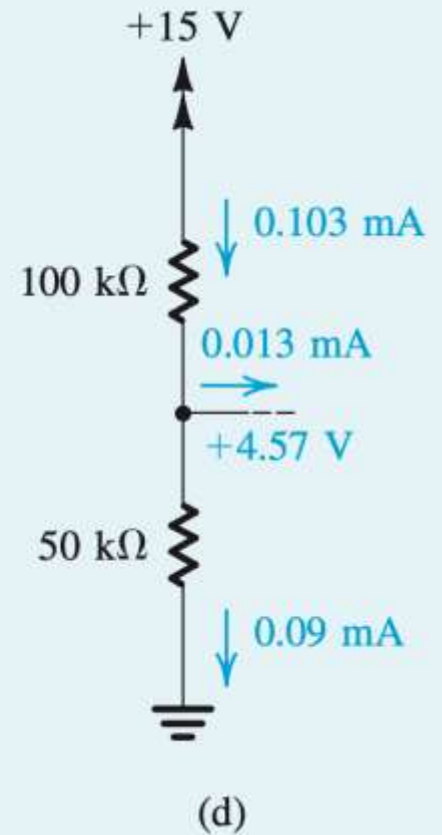
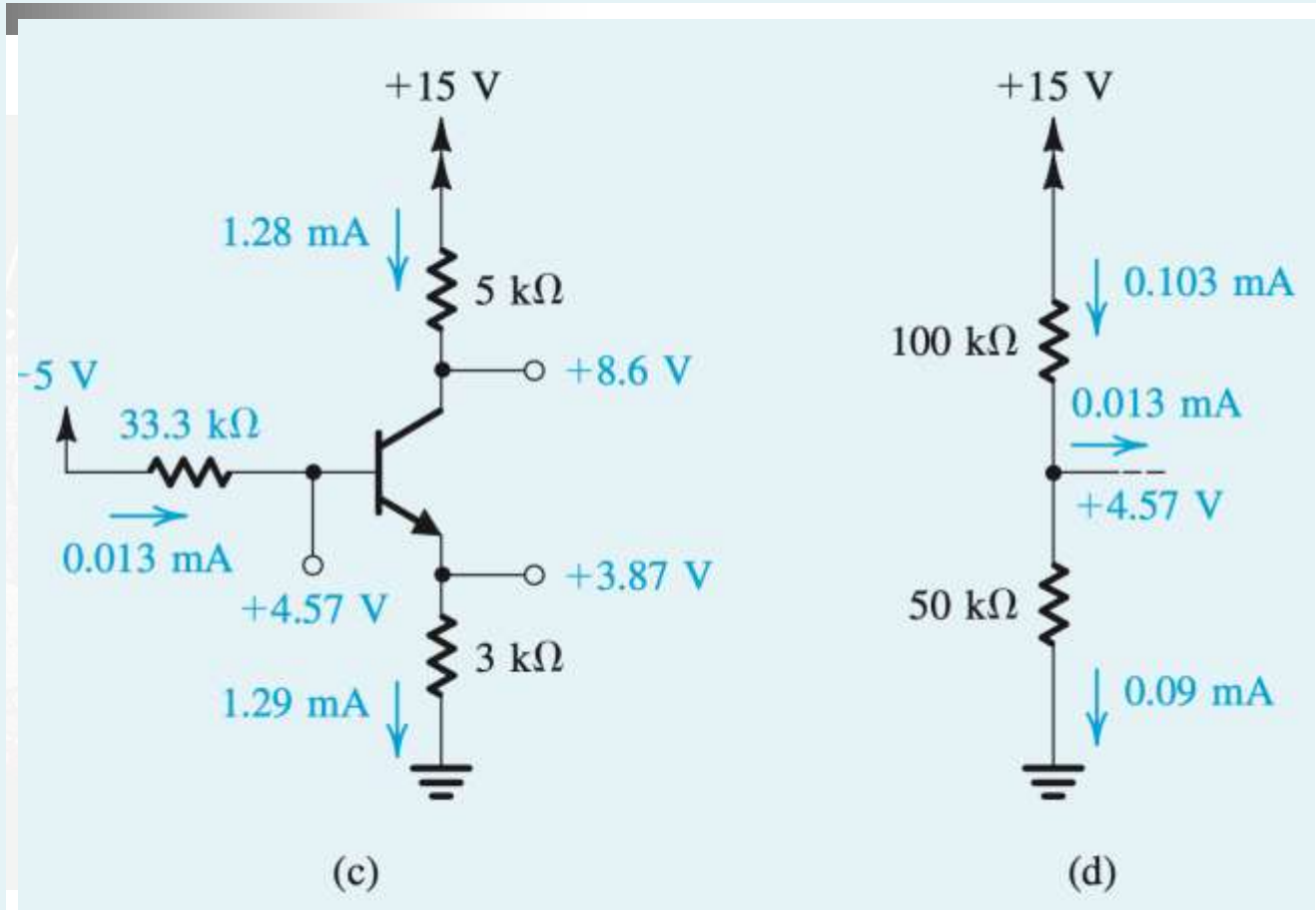
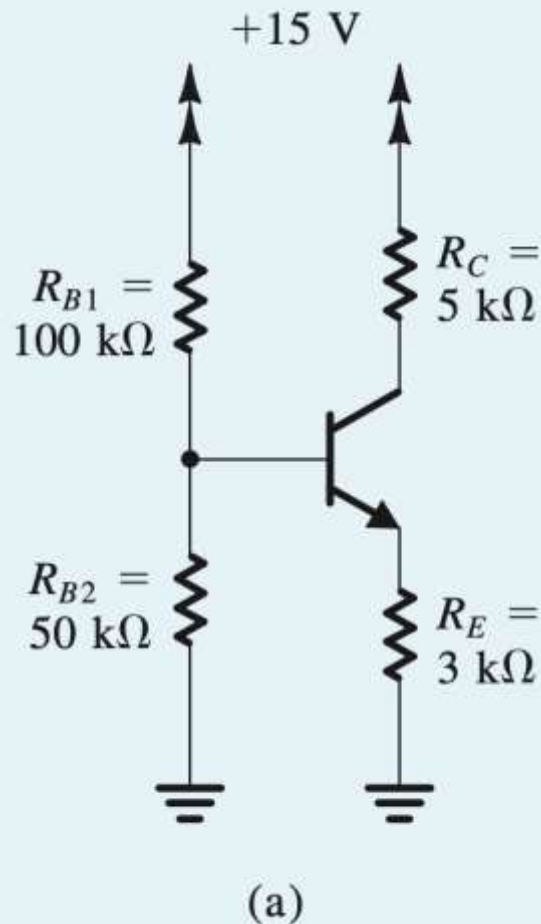
$$V_B = V_E + V_{BE} = 4.57 \text{ V}$$

$$V_C = +15 - I_C R_C = 8.6 \text{ V}$$

高于下限 (4.57 - 0.4) , 合理

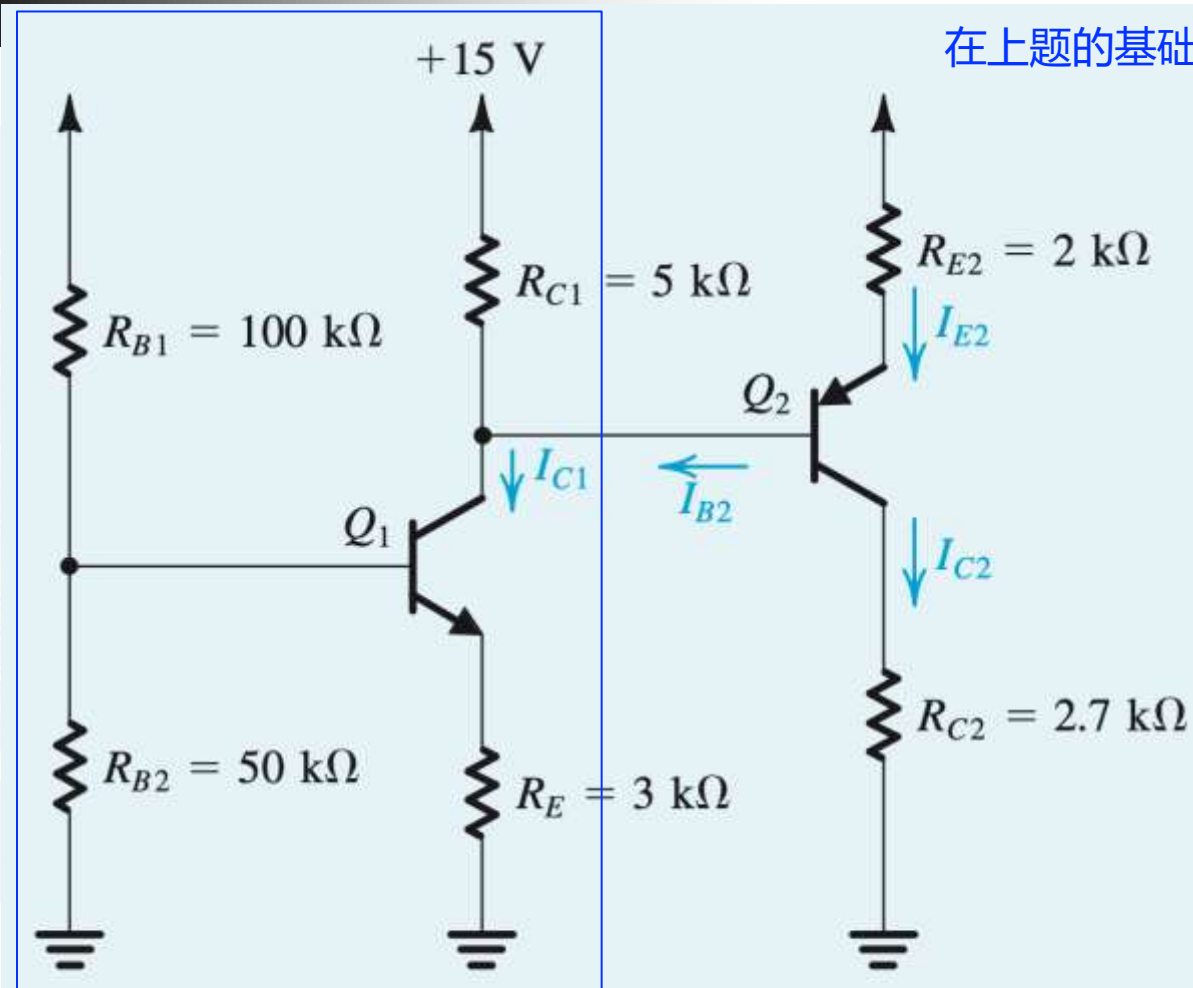
Example 6.10

We want to analyze the circuit of Fig. 6.29(a) to determine the voltages at all nodes and the currents through all branches. Assume $\beta = 100$.



④分析 R_{B1} 、 R_{B2} 分支的电压电流

We wish to analyze the circuit in Fig. 6.30(a) to determine the voltages at all nodes and the currents through all branches.

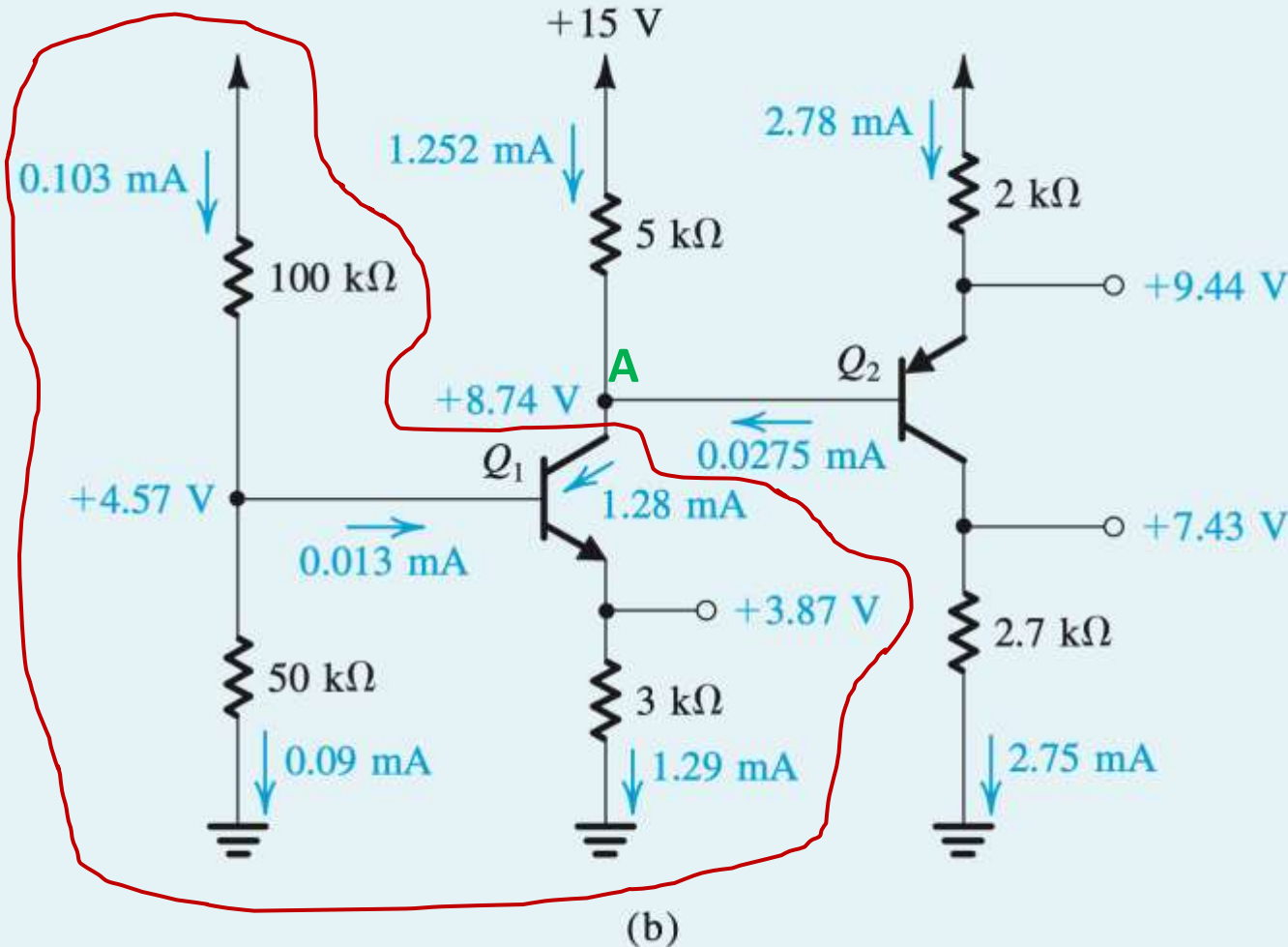


在上题的基础上再加了一个stage

(a)

Example 6.11

We wish to analyze the circuit in Fig. 6.30(a) to determine the voltages at all nodes and the currents through all branches.



① 假设Q1还是工作在放大区

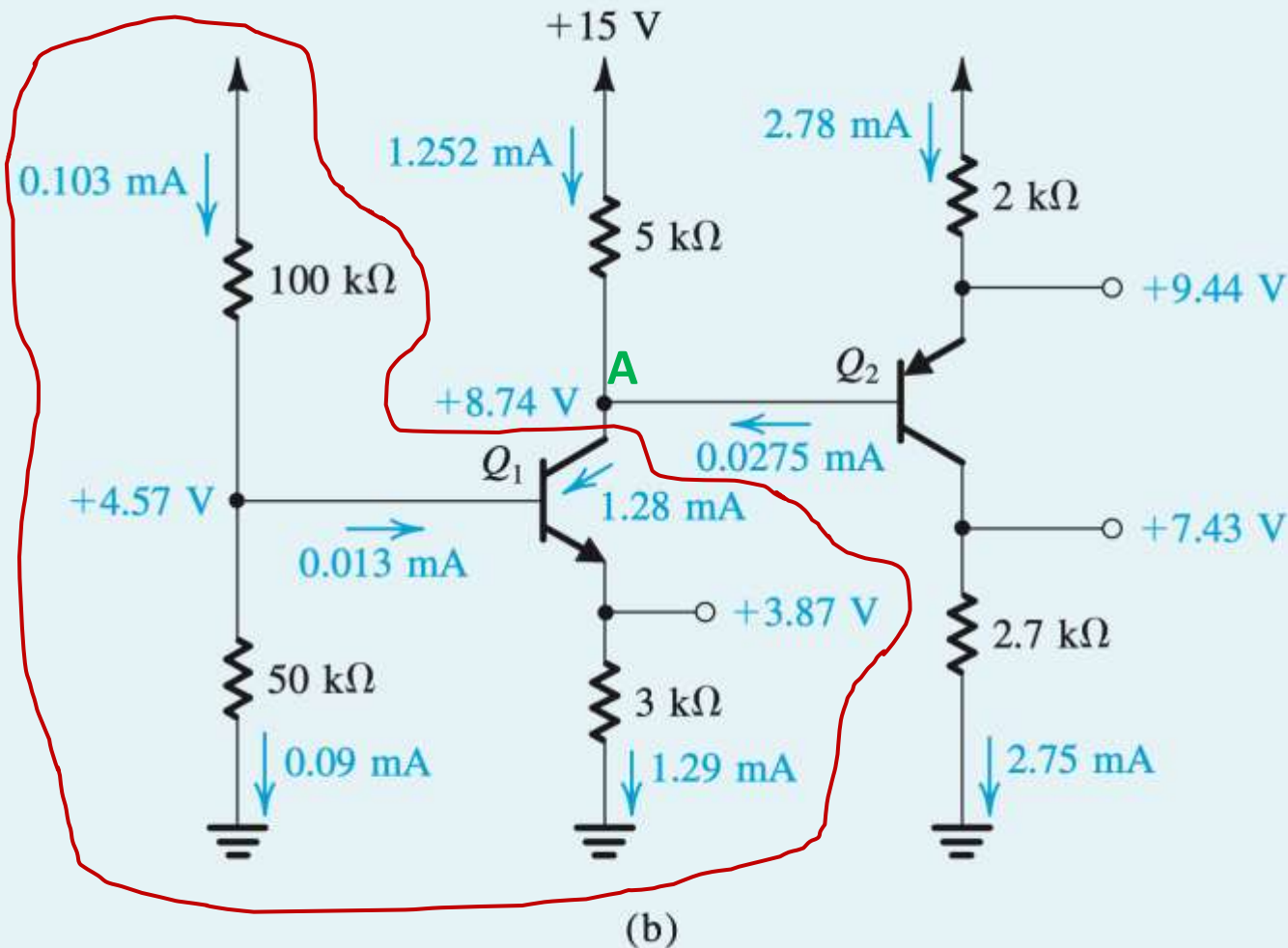
- 红色区域内的分析与上个例题一致
- 对A点应用KCL, Q1的 i_c 不变 (由 i_b 决定), 流过5kΩ的电流变小 (因Q2的 i_b 很小, 所以电流只有微小变化), A点电压略微上升, 更符合在放大区的要求。

② Q2的发射极通过2kΩ接到+15V, Q2开启

- 若不开启, 电流为0, 发射极电压为15V, 矛盾

Example 6.11

We wish to analyze the circuit in Fig. 6.30(a) to determine the voltages at all nodes and the currents through all branches.



③ 因为Q2的 i_B 很小，先做一阶近似，忽略Q2 i_B 的影响

$$V_{C1} \simeq +15 - I_{C1}R_{C1} \\ = 15 - 1.28 \times 5 = +8.6 \text{ V}$$

$$V_{E2} = V_{C1} + V_{EB}|_{Q_2} \\ \simeq 8.6 + 0.7 = +9.3 \text{ V}$$

$$I_{E2} = \frac{+15 - V_{E2}}{R_{E2}} \\ = \frac{15 - 9.3}{2} = 2.85 \text{ mA}$$

假设Q2工作在放大区

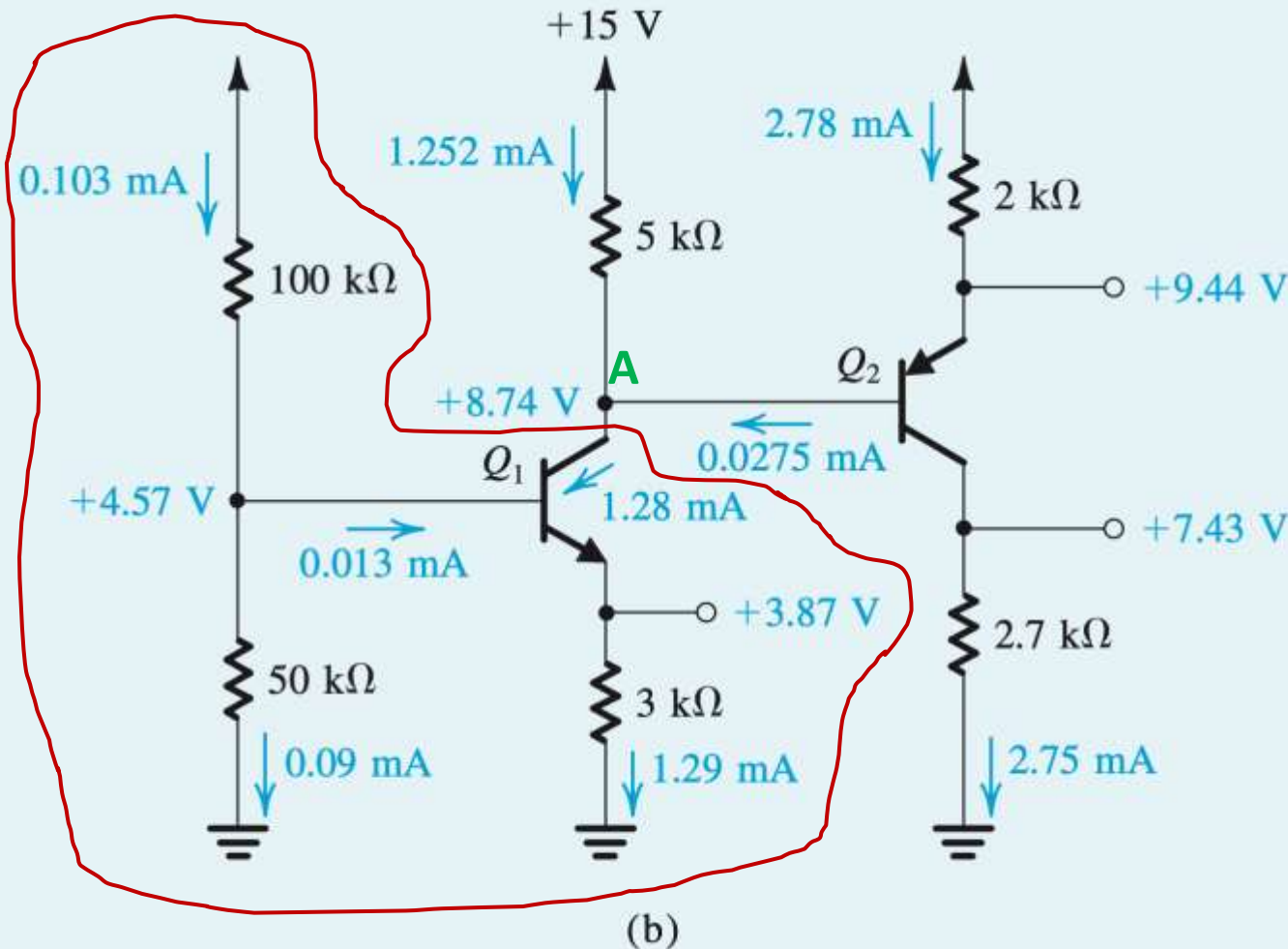
$$I_{C2} = \alpha_2 I_{E2} \quad (\text{assuming } \beta_2 = 100) \\ = 0.99 \times 2.85 = 2.82 \text{ mA}$$

$$V_{C2} = I_{C2}R_{C2} \\ = 2.82 \times 2.7 = 7.62 \text{ V}$$

$$7.62 < 8.6 + 0.4 \quad \checkmark$$

Example 6.11

We wish to analyze the circuit in Fig. 6.30(a) to determine the voltages at all nodes and the currents through all branches.



④ 忽略了 Q_2 的 i_B 导致了多少误差?

$$I_{B2} = \frac{I_{E2}}{\beta_2 + 1}$$

$$= \frac{2.85}{101} = 0.028 \text{ mA}$$

考虑 i_{B2} 的值, 重新进行迭代计算

$$\text{Current in } R_{C1} = I_{C1} - I_{B2}$$

$$= 1.28 - 0.028 = 1.252 \text{ mA}$$

$$V_{C1} = 15 - 5 \times 1.252 = 8.74 \text{ V}$$

$$V_{E2} = 8.74 + 0.7 = 9.44 \text{ V}$$

$$I_{E2} = \frac{15 - 9.44}{2} = 2.78 \text{ mA}$$

$$I_{C2} = 0.99 \times 2.78 = 2.75 \text{ mA}$$

$$V_{C2} = 2.75 \times 2.7 = 7.43 \text{ V}$$

$$I_{B2} = \frac{2.78}{101} = 0.0275 \text{ mA}$$

为了获得更精确的值, 可以再次进行迭代

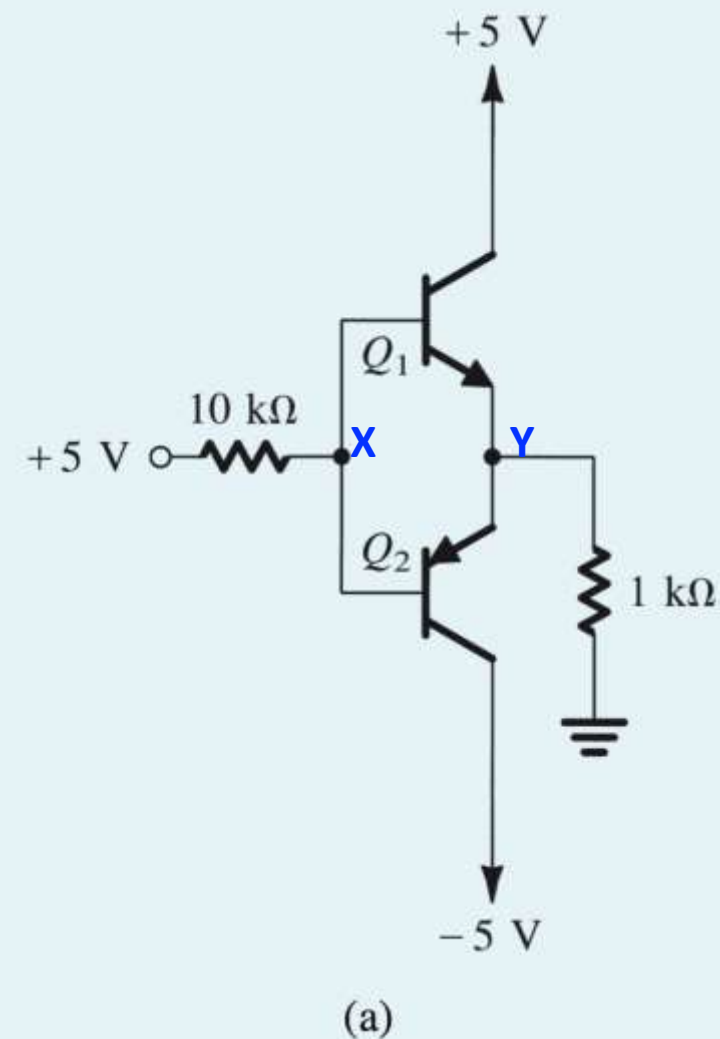


- 必要性不大

1. 快速计算
2. 培养对电路的直觉
3. 所以允许适当的误差

从估算的角度，工作在放大区的晶体管， α 可以用1近似， i_E 可用 i_C 近似

We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 6.31(a). Assume $\beta = 100$.



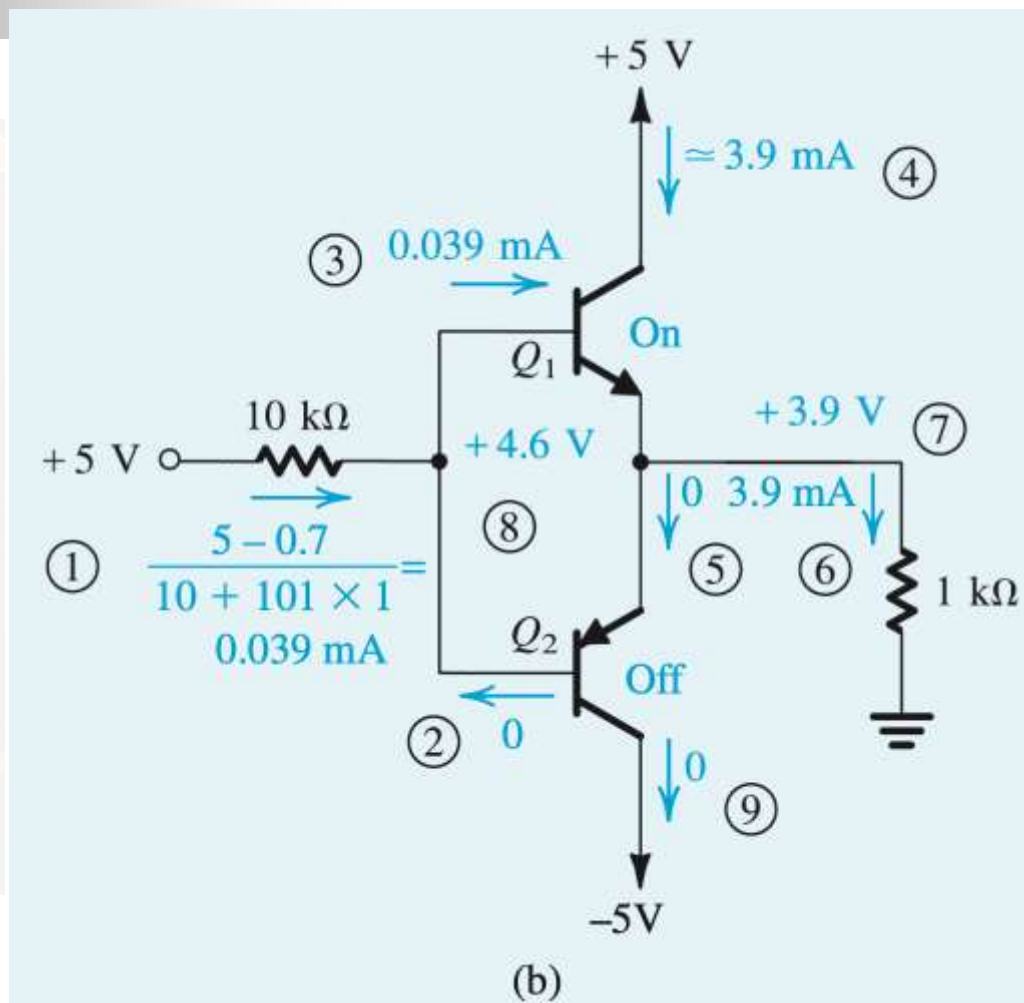
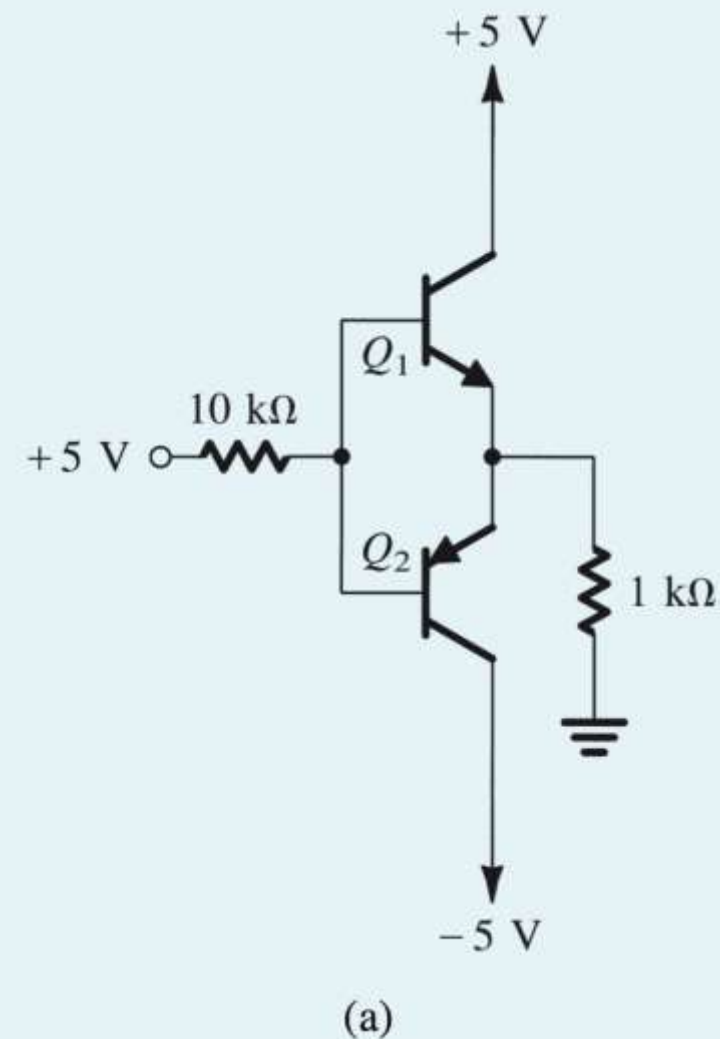
①分析两个晶体管是 on 还是 off

- **初步判断**, 基极接到 +5V, Y点电压不太可能高于X点电压, Q2 off, **进一步分析**如下:
- 若两个都off, $V_Y = 0$, $V_X = 5V \rightarrow Q1$ on, 矛盾
- 若两个都on, 从Q1看, $V_X > V_Y$, 从Q2看 $V_X < V_Y$, 矛盾
- 若Q1 off, Q2 on, $V_X < V_Y < 0V$, 电流从X流向5V, 矛盾
- **所以, 只能是Q1 on, Q2 off**

②分析Q1是工作在放大区还是饱和区?

- X点电压小于5V, 而Q1的C接在5V, 所以工作在放大区 (放大区的条件: C点电压的下限是B点-0.4V)

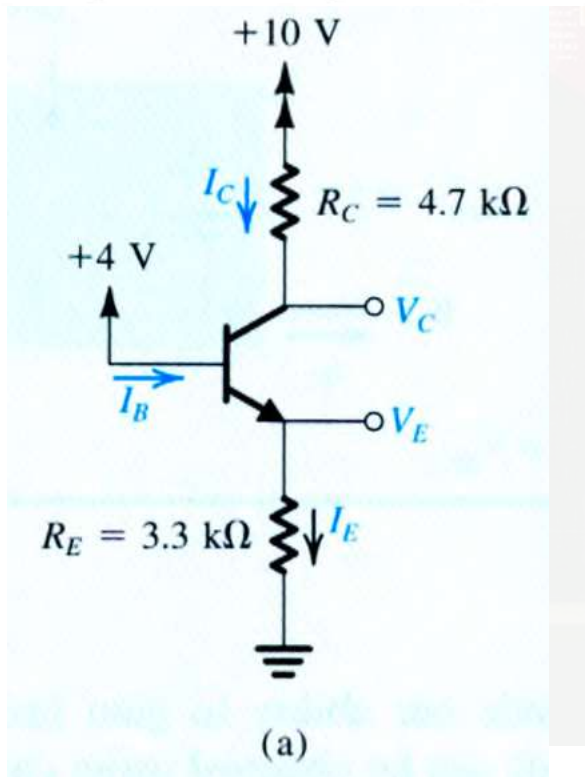
We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 6.31(a). Assume $\beta = 100$.



作业

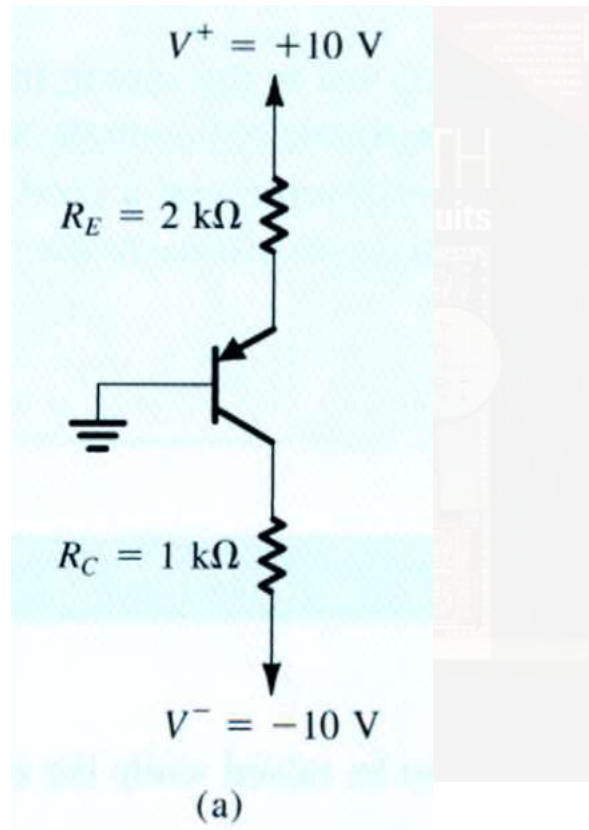
D6.23 Redesign the circuit of Fig. 6.23(a) (i.e., find new values for R_E and R_C) to establish a collector current of 0.5 mA and a reverse-bias voltage on the collector–base junction of 2 V. Assume $\alpha \simeq 1$.

Ans. $R_E = 6.6 \text{ k}\Omega$; $R_C = 8 \text{ k}\Omega$



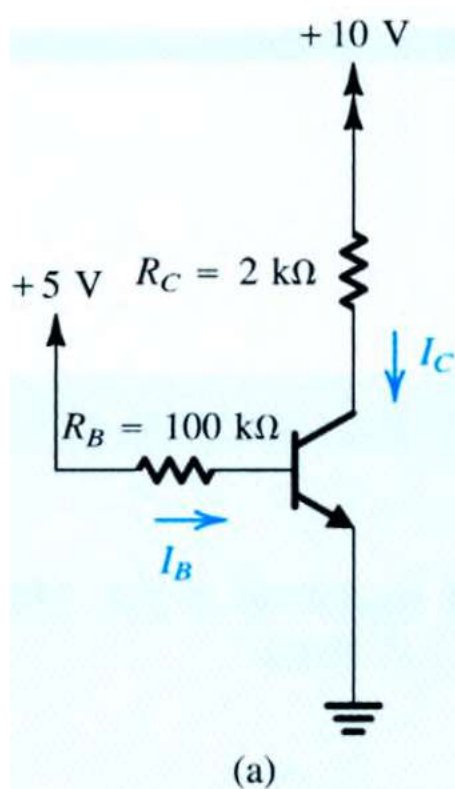
D6.25 For the circuit in Fig. 6.26(a), find the largest value to which R_C can be raised while the transistor remains in the active mode.

Ans. 2.24 k Ω



D6.27 The circuit of Fig. 6.27(a) is to be fabricated using a transistor type whose β is specified to be in the range of 50 to 150. That is, individual units of this same transistor type can have β values anywhere in this range. Redesign the circuit by selecting a new value for R_C so that all fabricated circuits are guaranteed to be in the active mode. What is the range of collector voltages that the fabricated circuits may exhibit?

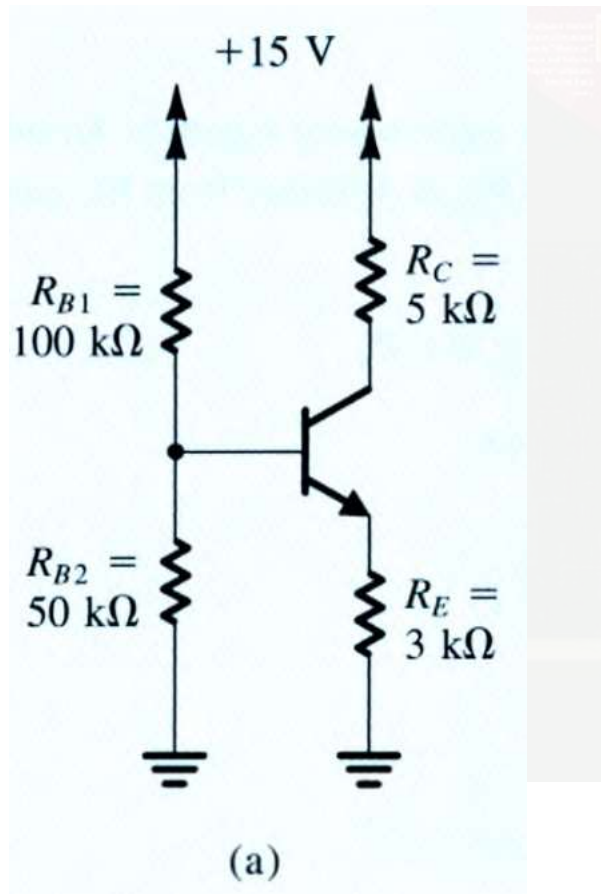
Ans. $R_C = 1.5 \text{ k}\Omega$; $V_C = 0.3 \text{ V}$ to 6.8 V



6.28 If the transistor in the circuit of Fig. 6.29(a) is replaced with another having half the value of β (i.e., $\beta = 50$), find the new value of I_C , and express the change in I_C as a percentage.

Ans. $I_C = 1.15 \text{ mA}$; -10%

$\beta = 100$ 时, $I_C = 1.28 \text{ mA}$



6.30 The circuit in Fig. E6.30 is to be connected to the circuit in Fig. 6.30(a) as indicated; specifically, the base of Q_3 is to be connected to the collector of Q_2 . If Q_3 has $\beta = 100$, find the new value of V_{C2} and the values of V_{E3} and I_{C3} .

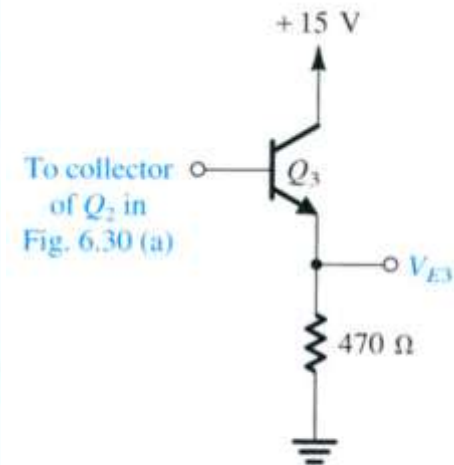
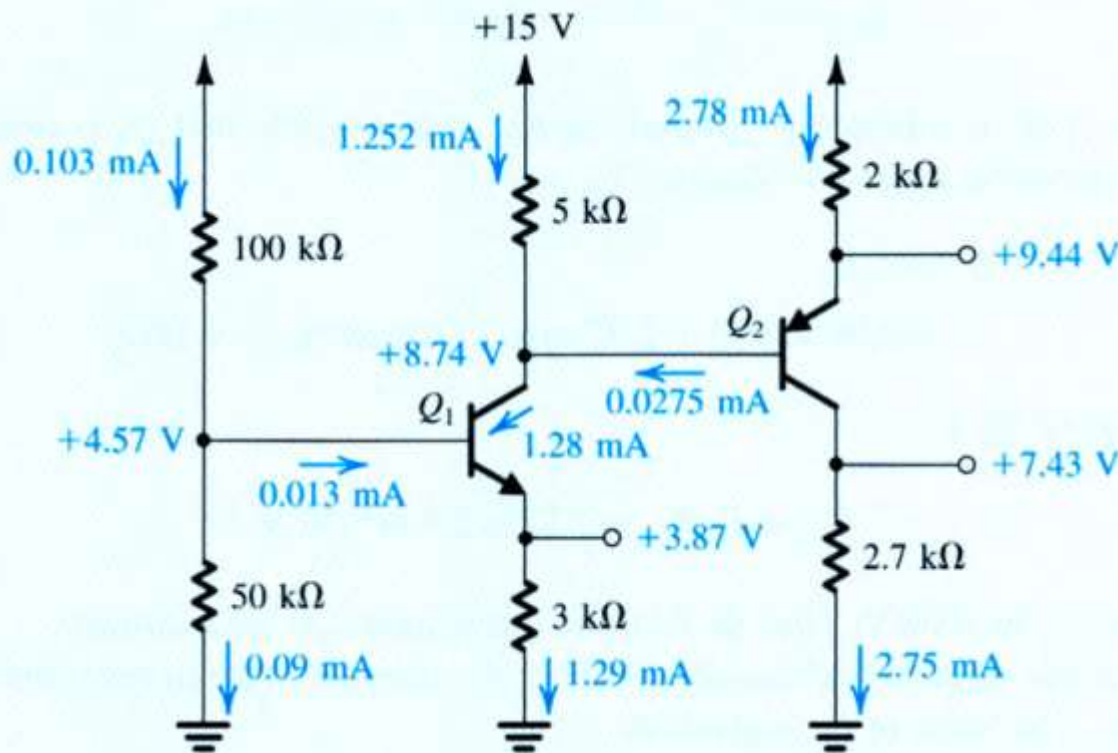


Figure E6.30

Ans. +7.06 V; +6.36 V; 13.4 mA

6.31 Solve the problem in Example 6.12 for the case of a voltage of -5 V feeding the bases. What voltage appears at the emitters?

Assume $\beta = 100$.

Ans. -3.9 V

