Lecture 21 – Active load, Cascode and Current Mirrors

- **Active load 有源负载**
- **Cascode**
- **Current Mirrors 电流镜**

教学大纲（对应英文教材第8章）

- 10. 差分和多级放大器
- 10.1 差分放大器的结构及其分析
- 10.1.1 BJT和MOS差分放大器的结构
- 10.1.2 大信号和小信号输入时的电路分析
- 10.1.3 差分放大器的非理想特性
- **10.2 镜像电流源的结构及其分析**
- **10.2.1 BJT和MOS基本镜像电流源**
- **10.2.1 改进型镜像电流源（包括Cascode、基极电流补偿、Wilson和Widlar）**
- **10.3 有源负载的作用及其应用**（包含有源负载的BJT和MOS差分放大器的分析）
- 10.4 多级放大器的分析
- 10.4.1 多级放大器的级联方式
- 10.4.2 多级放大器的增益计算

集成电路设计的特性

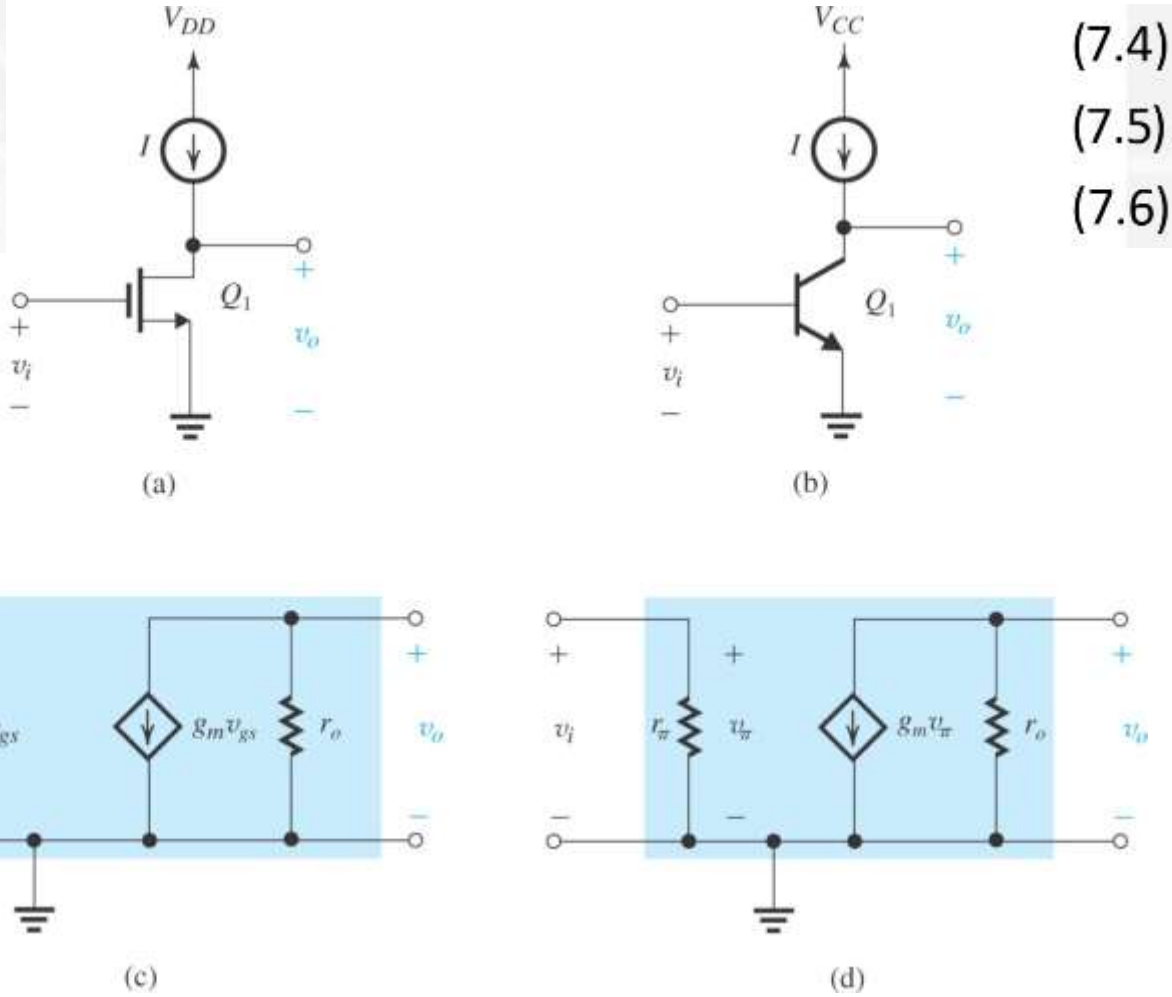
- **从本章开始，主要讲集成电路（IC，芯片）的设计；**

- **集成电路设计的特性**
  - 避免使用大电阻；
  - 大电容不可得；
  - 尽可能多使用MOSFET，少使用Bipolar；
  - 但Bipolar在少数的场合仍有其应用价值：
    - 高质量的运放；
    - 汽车电子（高输出电流、高可靠性要求）；
    - 射频功率放大器
    - …
  - 同时使用MOSFET和Bipolar的工艺——BiCMOS；

(7.1) $R_{in} = \infty$

(7.2) $A_{vo} = -g_m r_o$

(7.3) $R_o = r_o$



(7.4) $R_{in} = r_\pi$

(7.5) $A_{vo} = -g_m r_o$

(7.6) $R_o = r_o$

Figure 7.1 The basic gain cells of IC amplifiers: **(a)** current-source- or active-loaded common-source amplifier; **(b)** current-source- or active-loaded common-emitter amplifier; **(c)** small-signal equivalent circuit of **(a)**; and **(d)** small-signal equivalent circuit of **(b)**.

IC电路设计中，CS/CE 结构采用有源负载（电流源）来替代负载电阻R_L

7.2.2. The Intrinsic Gain

- **intrinsic gain $A_o = g_m r_o$**
- **Bipolar**

(7.7) $g_m = \frac{I_C}{V_T}$

(7.8) $r_o = \frac{V_A}{I_C}$

(7.9) intrinsic gain is: $A_0 = g_m r_o = \frac{V_A}{V_T}$

Bipolar：V_A工艺参数；

MOSFET：V_A'工艺参数；W、L、V_{OV}设计参数；

MOSFET

(7.10) $g_m = \frac{I_D}{V_{OV}/2}$

(7.11) $g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}}\sqrt{I_D}$

(7.12) $r_o = \frac{V_A}{I_D} = \frac{V_A' L}{I_D}$

(7.13) $A_0 = \frac{V_A}{V_{OV}/2}$

(7.14) $A_0 = \frac{2V_A' L}{V_{OV}}$

(7.14) $A_0 = \frac{V_A'\sqrt{2(\mu_n C_{ox})WL}}{\sqrt{I_D}}$

$$A_0 = \frac{V'_A \sqrt{2(\mu_n C_{ox})WL}}{\sqrt{I_D}}$$

偏置电流I_D越小，内在增益越大

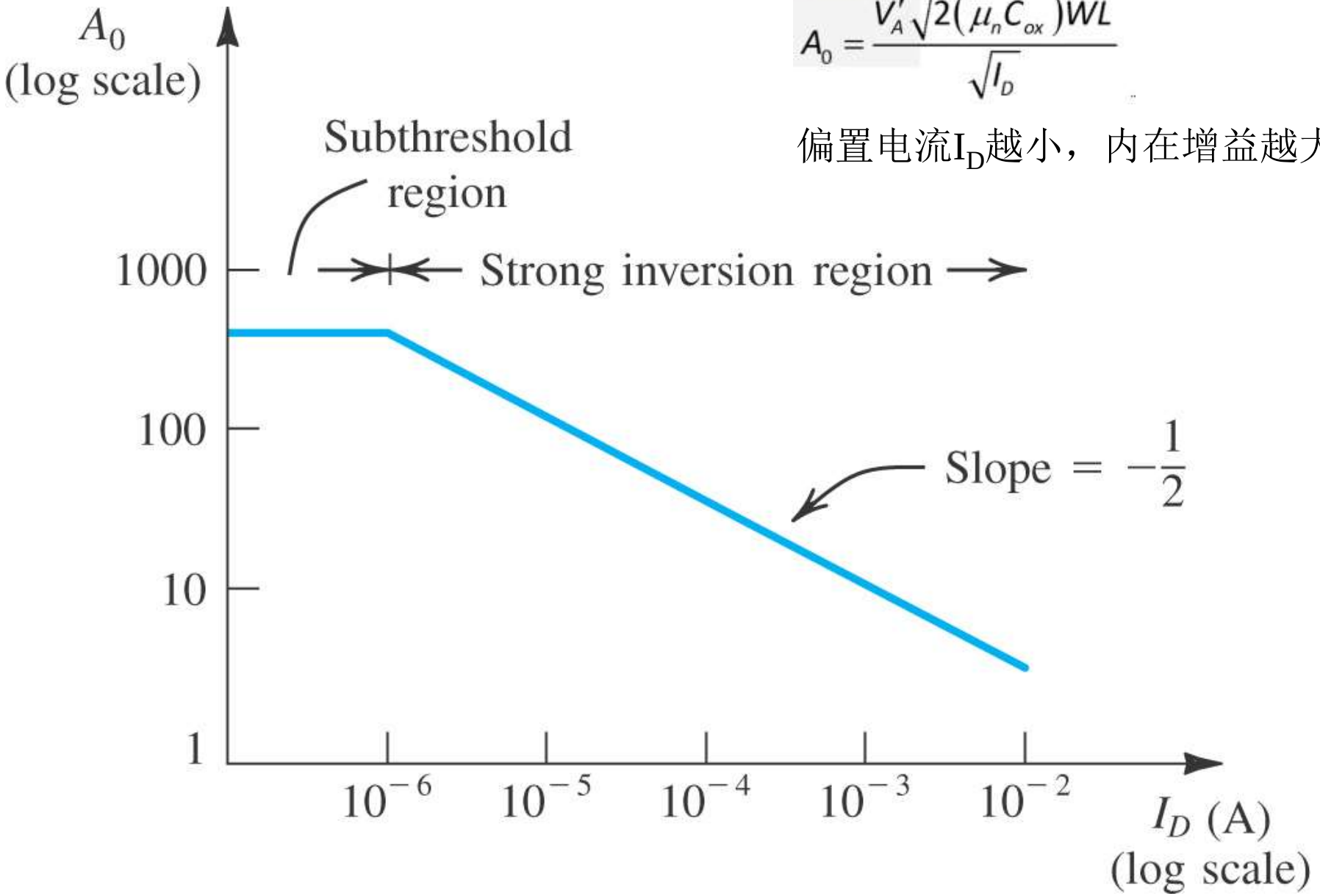


Figure 7.2 The intrinsic gain of the MOSFET versus bias current I_D. Outside the subthreshold region, this is a plot of $A_0 = V'A\ \sqrt{2\mu_n C_{ox} WL/I_D}$ for the case: $\mu_n C_{ox} = 20\ \mu A/V^2$, $V'A = 20$ V/μm, $L = 2$ μm, and $W = 20$ μm.

7.2.3. Effect of the Output Resistance of the Current-Source Load

- **The current-source load of the CS amplifier in Figure 7.1(a) can be implemented using a PMOS transistor biased in the saturation region to provide the required current *I*, as shown in Figure 7.3(a). 电流源用工作于饱和区的PMOS实现**

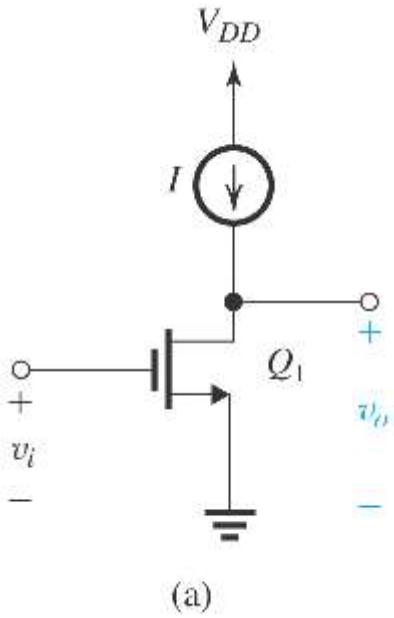


Figure 7.1(a)

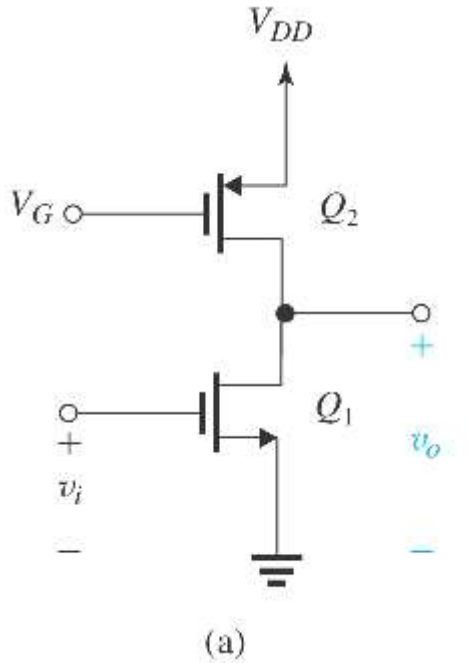
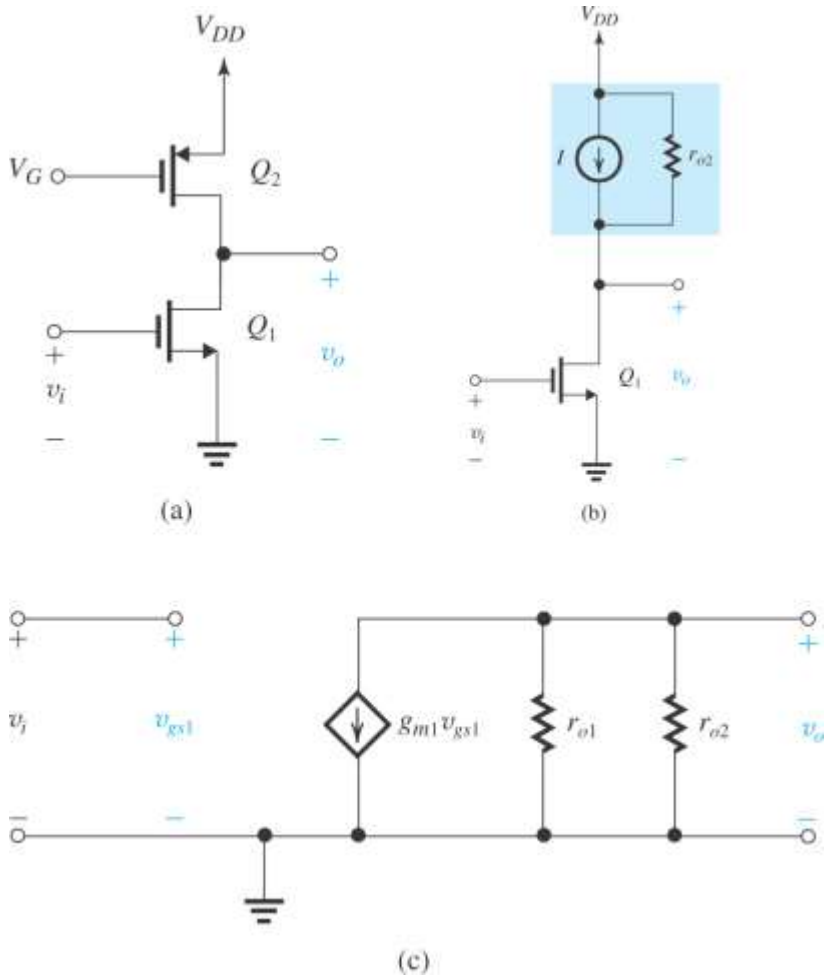
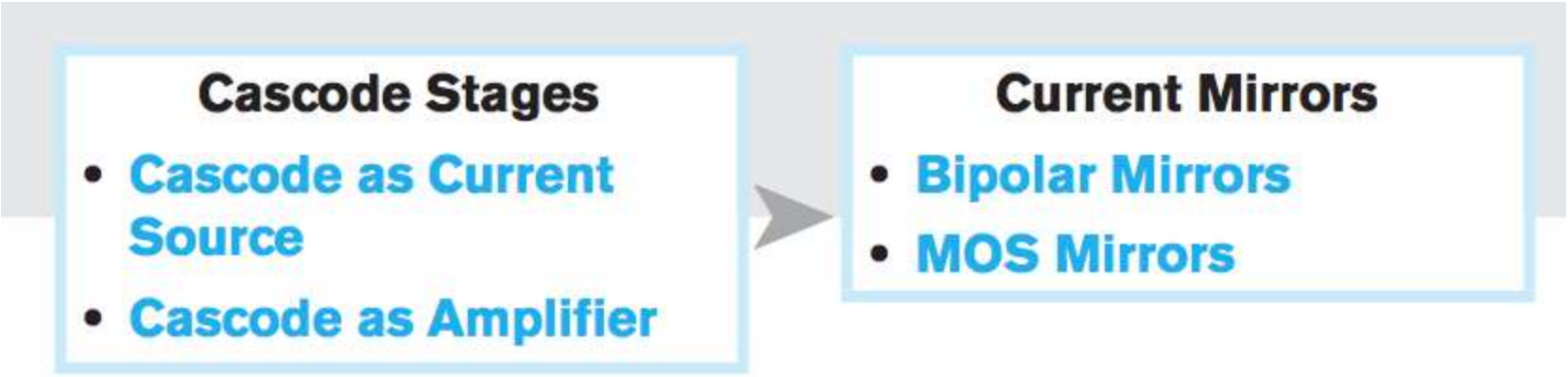


Figure 7.3(a)

有源负载

$$(7.18)\ A_v = \frac{v_o}{v_i} = -g_{m1}\left(r_{o1} \,||\, r_{o2}\right)$$

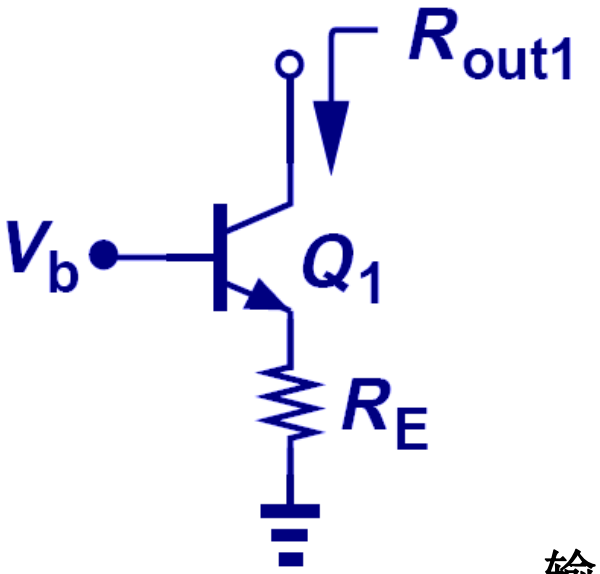


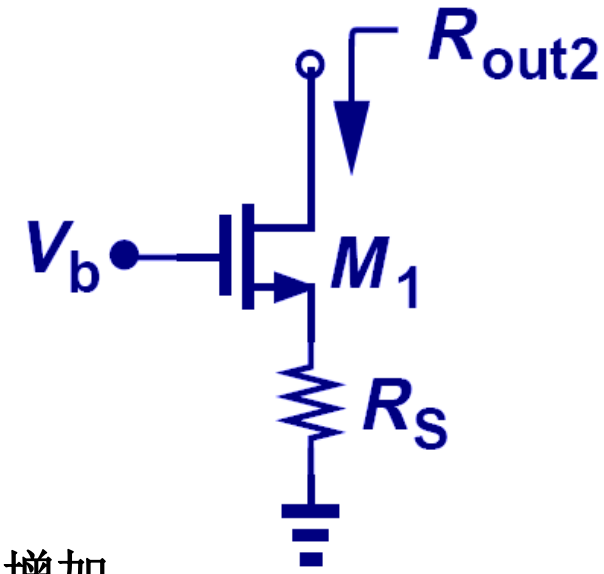


Cascode结构（高增益电路设计）
•Cascode结构作为电流源
•Cascode结构作为放大器

电流镜（广泛用于集成电路设计）
•三极管电流镜
•场效应管电流镜

发射极（源极）退化结构回顾





输出阻抗大幅增加

$$R_{out1} = r_O + (1 + g_m r_O)(R_E \| r_\pi)$$

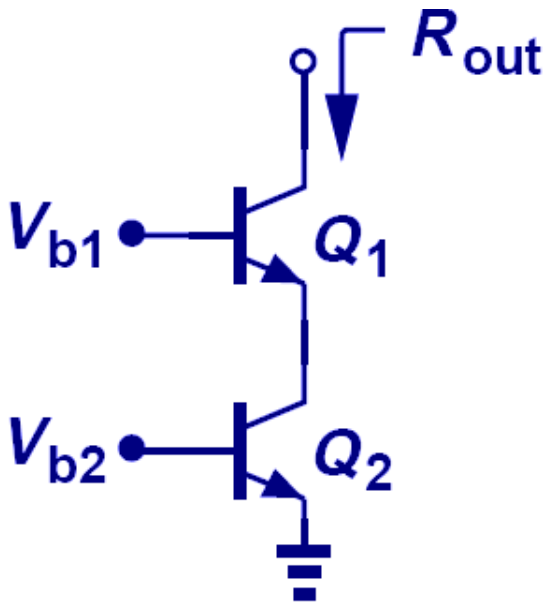
$$R_{out2} = r_O + (1 + g_m r_O) R_S$$

思考：集成电路中要避免使用大电阻，那么怎么办？

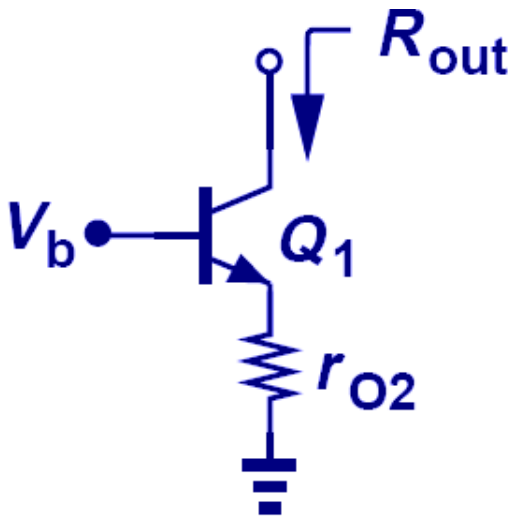
电流源结构可以提供大电阻 → R_E，R_S用电流源替代 → Cascode结构

Cascode结构做电流源用（需要大的输出阻抗）

三极管 Cascode 结构



(a)



(b)

$$R_{out} = r_{O1} + (1 + g_m r_{O1})(r_{O2} \parallel r_{\pi 1})$$

$$R_{out} \approx g_{m1} r_{O1} (r_{O2} \parallel r_{\pi 1})$$

例题

Example 9.1 If Q_1 and Q_2 in Fig. 9.2(a) are biased at a collector current of 1 mA, determine the output resistance. Assume $\beta = 100$ and $V_A = 5$ V for both transistors.

Solution Since Q_1 and Q_2 are identical and biased at the same current level, Eq. (9.7) can be simplified by noting that $g_m = I_C/V_T$, $r_O = V_A/I_C$, and $r_\pi = \beta V_T/I_C$: $R_{out} \approx g_{m1} r_{O1} (r_{O2} \| r_{\pi 1})$

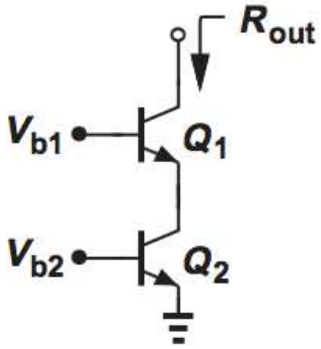
$$R_{out} \approx \frac{I_{C1}}{V_T} \cdot \frac{V_{A1}}{I_{C1}} \cdot \frac{\frac{V_{A2}}{I_{C2}} \cdot \frac{\beta V_T}{I_{C1}}}{\frac{V_{A2}}{I_{C2}} + \frac{\beta V_T}{I_{C1}}} \tag{9.8}$$

$$\approx \frac{1}{I_{C1}} \cdot \frac{V_A}{V_T} \cdot \frac{\beta V_A V_T}{V_A + \beta V_T}, \tag{9.9}$$

where $I_C = I_{C1} = I_{C2}$ and $V_A = V_{A1} = V_{A2}$. At room temperature, $V_T \approx 26$ mV and hence

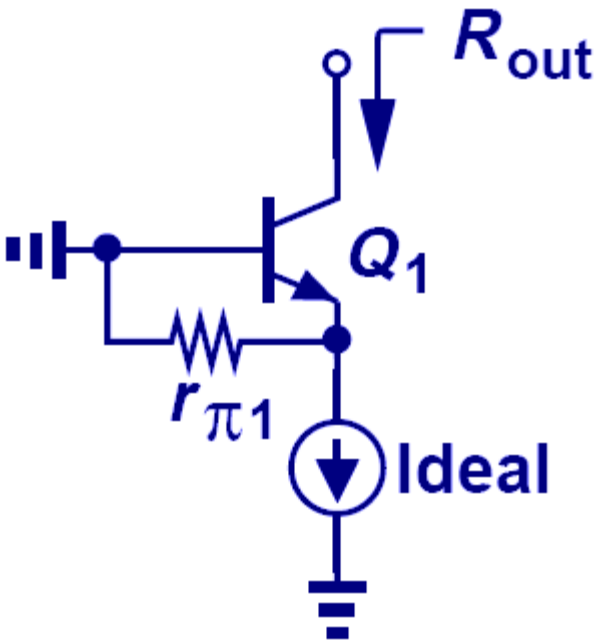
$$R_{out} \approx 328.9\,\text{k}\Omega. \tag{9.10}$$

By comparison, the output resistance of Q_1 with no degeneration would be equal to $r_{O1} = 5\,\text{k}\Omega$; i.e., "cascoding" has boosted R_{out} by a factor of 66 here. Note that r_{O2} and $r_{\pi 1}$ are comparable in this example.



(a)

三极管 Cascode 结构的最大输出阻抗



$$R_{out} \approx g_{m1} r_{O1} \left(r_{O2} \parallel r_{\pi 1} \right) < g_{m1} r_{O1} r_{\pi 1}$$

$$R_{out,\max} \approx g_{m1} r_{O1} r_{\pi 1}$$

$$R_{out,\max} \approx \beta_1 r_{O1}$$

- 发射极到GND的总电阻为$r_{\pi 1}$ 和r_{o2}的并联， $r_{\pi 1}$始终存在， r_{o2}最大可以为无穷大，所以三极管cascode结构的最大输出电阻为r_{o1}的β倍.

增加Q2的r_o，逼近最大输出阻抗值

Example 9.2 Suppose in Example 9.1, the Early voltage of Q_2 is equal to 50 V.[3] Compare the resulting output impedance of the cascode with the upper bound given by Eq. (9.12).

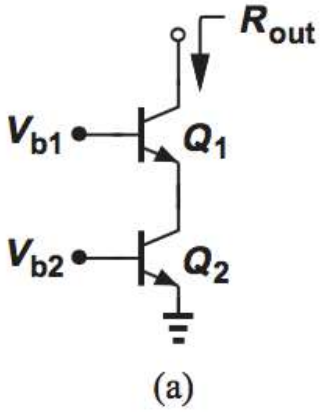
$I_C = 1$ mA, $\beta = 100$, $V_{A1} = 5$V, $V_{A2} = 50$V

Solution Since $g_{m1} = (26\,\Omega)^{-1}$, $r_{\pi 1} = 2.6\,\text{k}\Omega$, $r_{O1} = 5\,\text{k}\Omega$, and $r_{O2} = 50\,\text{k}\Omega$, we have

$$R_{out} \approx g_{m1} r_{O1} (r_{O2} || r_{\pi 1}) \tag{9.13}$$

$$\approx 475\,\text{k}\Omega. \tag{9.14}$$

The upper bound is equal to 500 kΩ, about 5% higher.



(a)

Example 9.3

We wish to increase the output resistance of the bipolar cascode of Fig. 9.2(a) by a factor of two through the use of resistive degeneration in the emitter of Q_2. Determine the required value of the degeneration resistor if Q_1 and Q_2 are identical.

Solution As illustrated in Fig. 9.4, we replace Q_2 and R_E with their equivalent resistance from Eq. (9.1):

$$R_{outA} = [1 + g_{m2}(R_E||r_{\pi 2})]r_{O2} + R_E||r_{\pi 2}. \tag{9.15}$$

It follows from Eq. (9.7) that

$$R_{out} \approx g_{m1}r_{O1}(R_{outA}||r_{\pi 1}). \tag{9.16}$$

We wish this value to be twice that given by Eq. (9.7):

$$R_{outA}||r_{\pi 1} = 2(r_{O2}||r_{\pi 1}). \tag{9.17}$$

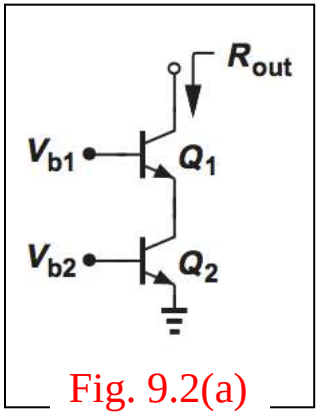
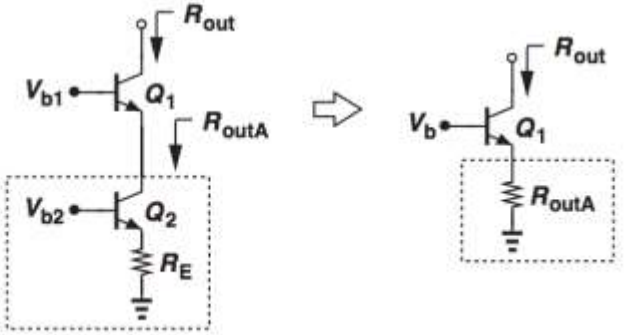


Fig. 9.2(a)

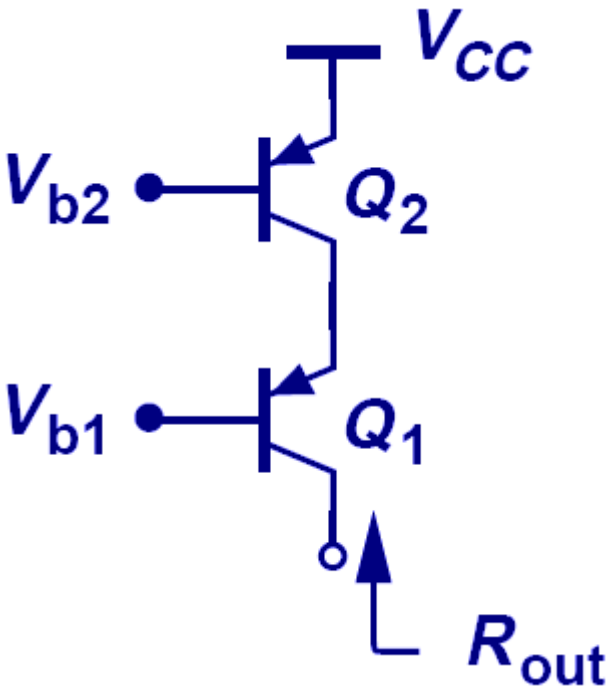


That is,

$$R_{outA} = \frac{2r_{O2}r_{\pi 1}}{r_{\pi 1} - r_{O2}}. \tag{9.18}$$

In practice, $r_{\pi 1}$ is typically *less* than r_{O2}, and no positive value of R_{outA} exists! In other words, it is impossible to double the output impedance of the cascode by emitter degeneration.

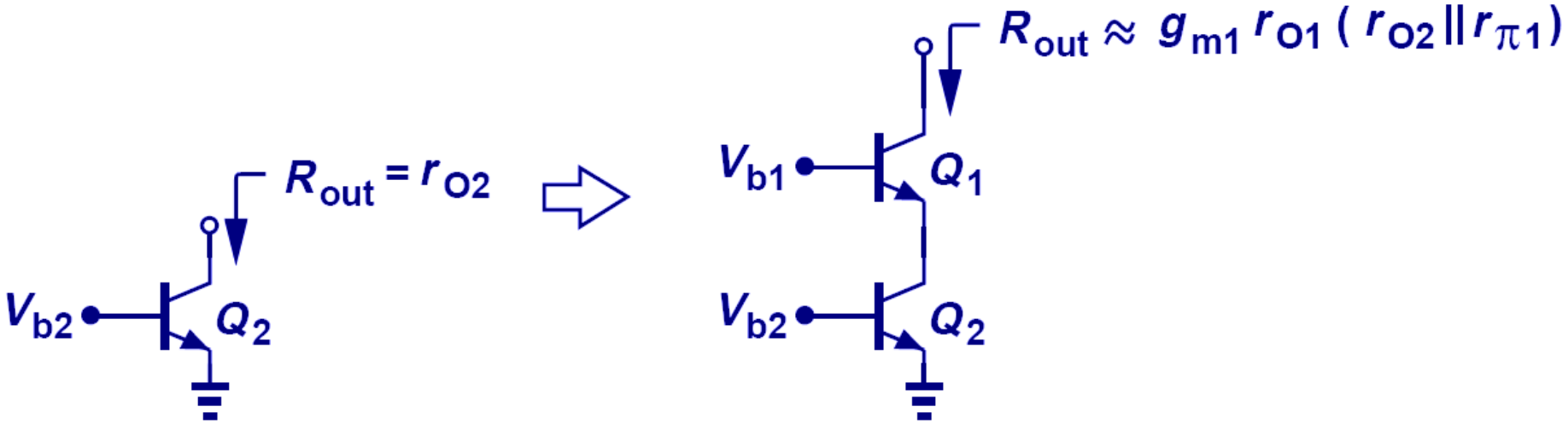
PNP Cascode 结构



$$R_{out} = r_{o1} + (1 + g_m r_{o1})(r_{o2} \,||\, r_{\pi 1})$$

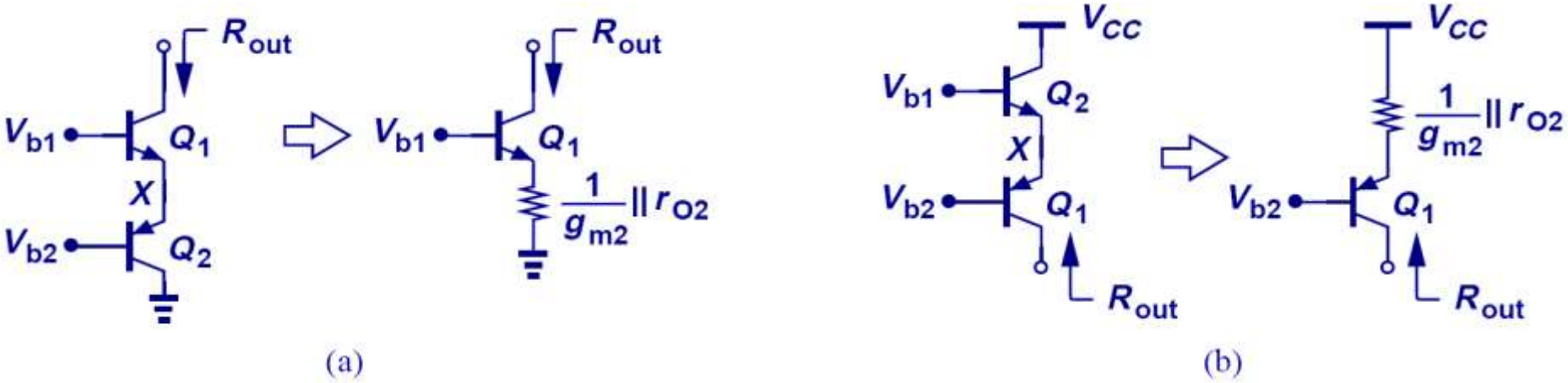
$$R_{out} \approx g_{m1} r_{o1} (r_{o2} \,||\, r_{\pi 1})$$

三极管 Cascode 结构的另一种解释



- 解释1：Q2是Q1的退化电阻；
- 解释2：Q1用来增强Q2的输出电阻。CB结构的Q1可看作电流Buffer（电流增益≈1，输出电阻大幅增加，与电压Buffer对偶）
- 【Instead of treating cascode as Q_2 degenerating Q_1, we can also think of it as Q_1 stacking on top of Q_2 (current source) to boost Q_2's output impedance. 】

这些是 Cascode 结构吗？



Solution Unlike the cascode of Fig. 9.2(a), the circuits of Fig. 9.7 connect the emitter of Q_1 to the *emitter* of Q_2. Transistor Q_2 now operates as a diode-connected device (rather than a current source), thereby presenting an impedance of $(1/g_{m2})||r_{O2}$ (rather than r_{O2}) at node X. Given by Eq. (9.1), the output impedance, R_{out}, is therefore considerably lower:

$$R_{out} = \left[1 + g_{m1}\left(\frac{1}{g_{m2}}||r_{O2}||r_{\pi 1}\right)\right]r_{O1} + \frac{1}{g_{m2}}||r_{O2}||r_{\pi 1}. \tag{9.19}$$

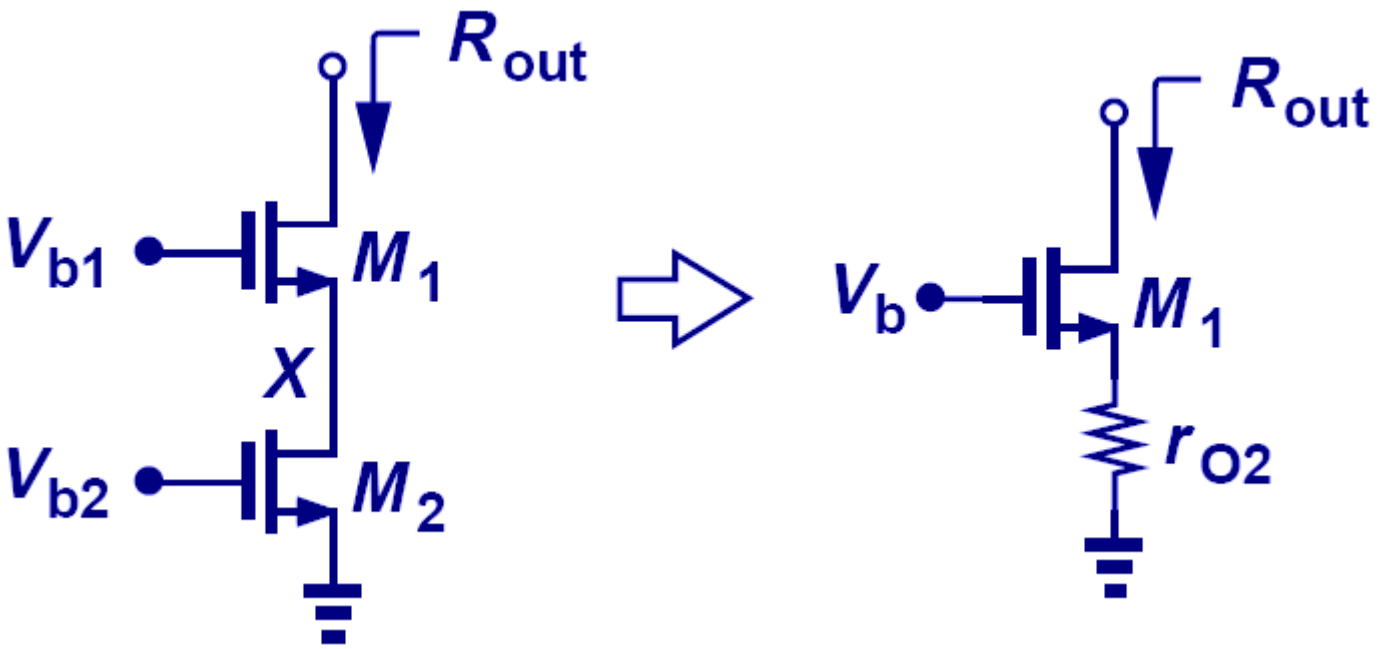
In fact, since $1/g_{m2} \ll r_{O2}, r_{\pi 1}$ and since $g_{m1} \approx g_{m2}$ (why?),

$$R_{out} \approx \left(1 + \frac{g_{m1}}{g_{m2}}\right)r_{O1} + \frac{1}{g_{m2}} \tag{9.20}$$

$$\approx 2r_{O1}. \tag{9.21}$$

The same observations apply to the topology of Fig. 9.7(b).

MOS Cascode 结构



$$R_{out} = (1 + g_{m1} r_{O2}) r_{O1} + r_{O2}$$

$$R_{out} \approx g_{m1} r_{O1} r_{O2}$$

例题

Example 9.5 Design an NMOS cascode for an output impedance of 500 kΩ and a current of 0.5 mA. For simplicity, assume M_1 and M_2 in Fig. 9.8 are identical (they need not be). Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$ and $\lambda = 0.1\,\text{V}^{-1}$.

Solution We must determine W/L for both transistors such that

$$g_{m1} r_{O1} r_{O2} = 500\,\text{k}\Omega. \tag{9.24}$$

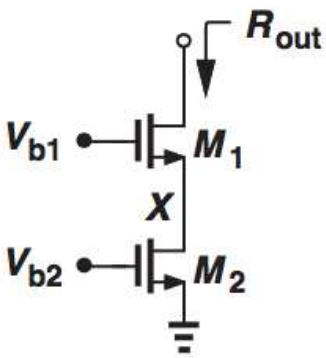
Since $r_{O1} = r_{O2} = (\lambda I_D)^{-1} = 20\,\text{k}\Omega$, we require that $g_{m1} = (800\,\Omega)^{-1}$ and hence

$$\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{1}{800\,\Omega}. \tag{9.25}$$

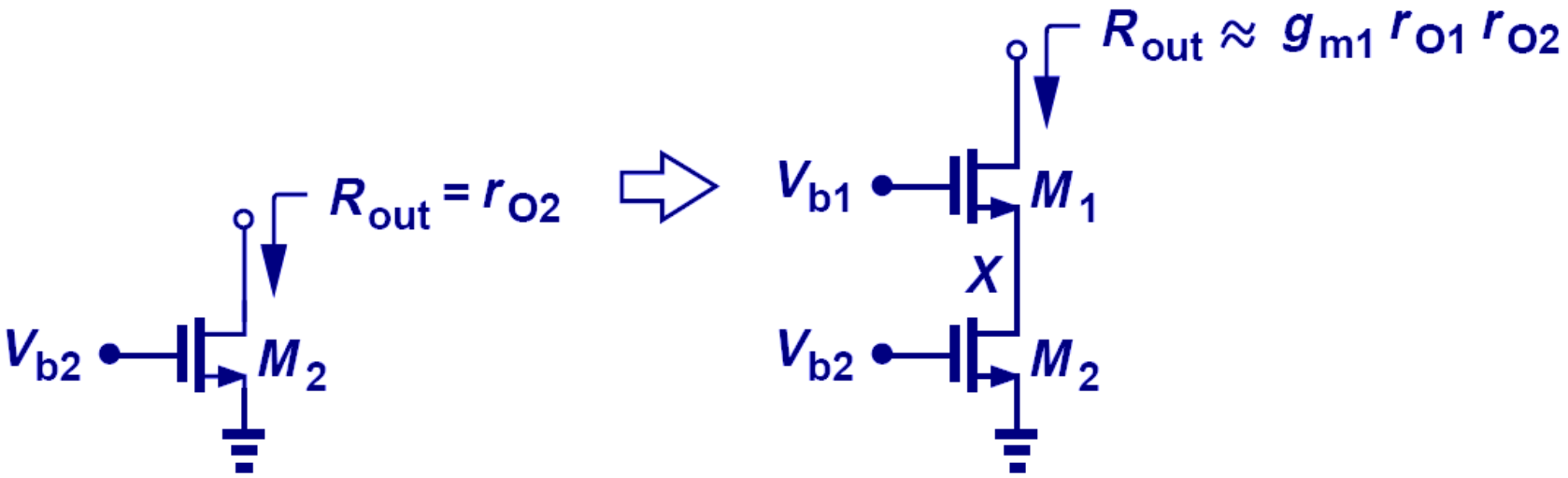
It follows that

$$\frac{W}{L} = 15.6. \tag{9.26}$$

We should also note that $g_{m1} r_{O1} = 25 \gg 1$.

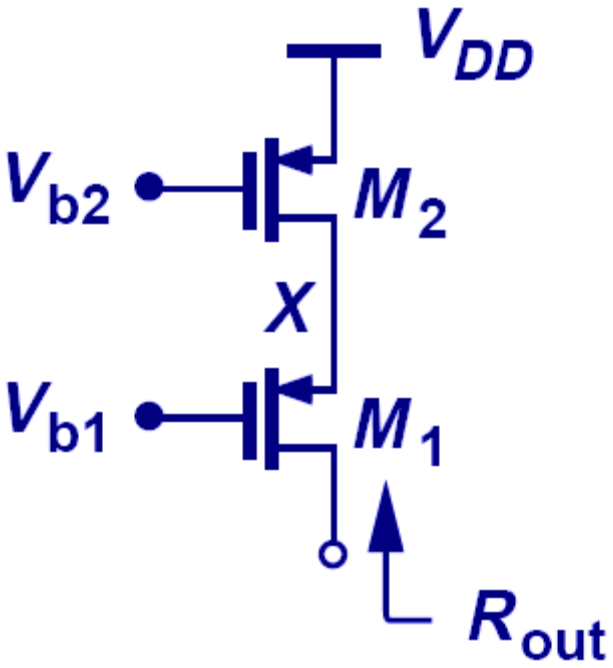


另一种解释



- 与三极管cascode一样，可以将M2看作是M1的退化电阻；也可以将M1看作是置于M2之上的，用来放大M2输出电阻用的MOS管；
- CG结构的M1可看作电流Buffer（电流增益=1，输出电阻大幅增加）
- 与三极管不同，三极管因为有r_π的存在，限制了最大输出电阻，而MOS管并无此限制

PMOS Cascode 结构



$$R_{out} = (1 + g_{m1} r_{O2}) r_{O1} + r_{O2}$$

$$R_{out} \approx g_{m1} r_{O1} r_{O2}$$

例题：寄生电阻的影响

Example 9.6

During manufacturing, a large parasitic resistor, R_P, has appeared in a cascode as shown in Fig. 9.11. Determine the output resistance.

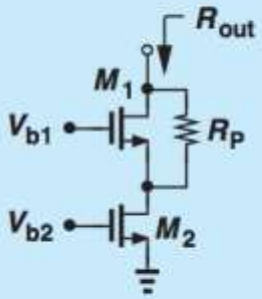


Figure 9.11

Solution We observe that R_P is in parallel with r_{O1}. It is therefore possible to rewrite Eq. (9.23) as

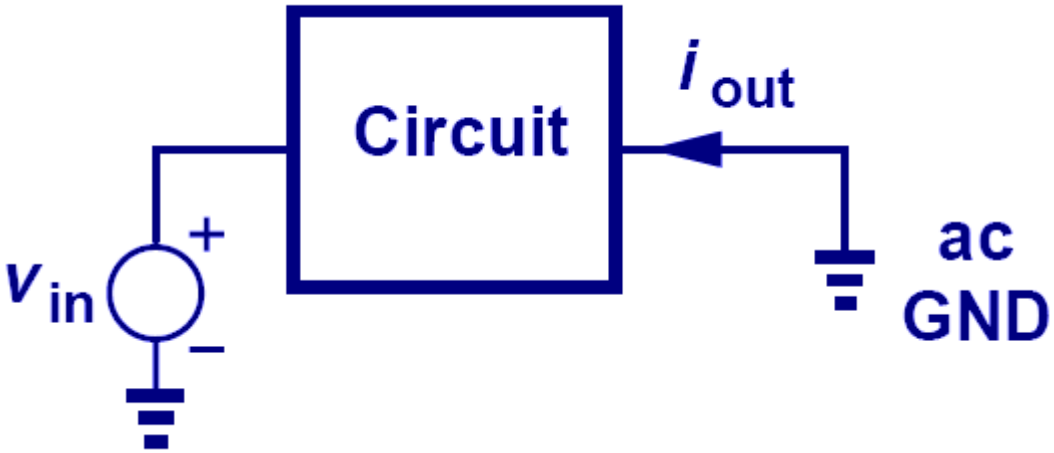
$$R_{out} = g_{m1}(r_{O1}||R_P)r_{O2}. \tag{9.27}$$

If $g_{m1}(r_{O1}||R_P)$ is not much greater than unity, we return to the original equation, (9.22), substituting $r_{O1}||R_P$ for r_{O1}:

$$R_{out} = (1 + g_{m1}r_{O2})(r_{O1}||R_P) + r_{O2}. \tag{9.28}$$

Cascode结构做放大器用（可提供大的电压增益）

电路跨导的定义



$$G_m = \left.\frac{i_{out}}{v_{in}}\right|_{v_{out}=0}$$

- 将电路的输出短路（交流地），计算输出电流与输入电压的比值，即为“电路跨导”，用大写的G_m表示（器件的跨导用小写的g_m表示）

例题

Example 9.7 Calculate the transconductance of the CS stage shown in Fig. 9.13(a).

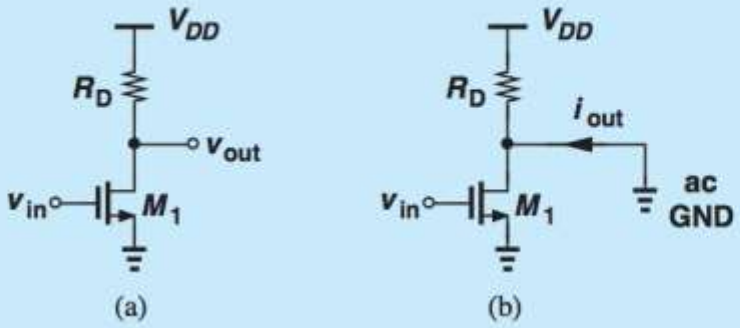


Figure 9.13

Solution As depicted in Fig. 9.13(b), we short the output node to ac ground and, noting that R_D carries no current (why?), write

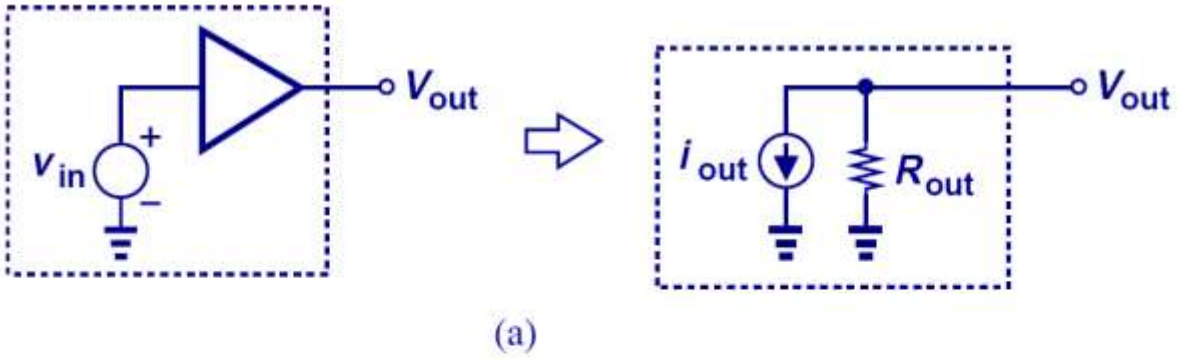
$$G_m = \frac{i_{out}}{v_{in}} \tag{9.30}$$

$$= \frac{i_{D1}}{v_{GS1}} \tag{9.31}$$

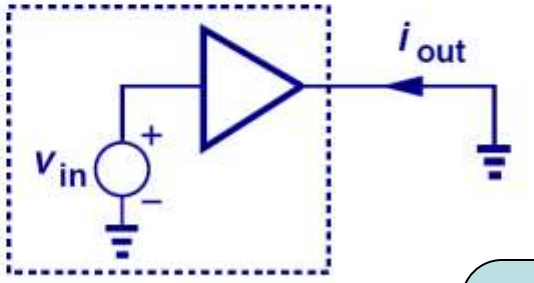
$$= g_{m1}. \tag{9.32}$$

Thus, in this case, the transconductance of the circuit is equal to that of the transistor.

电路的电压增益用“电路跨导”表示



(a)



(b)

诺顿定理

$$v_{out} = -i_{out} R_{out} = -G_m v_{in} R_{out}$$

$$v_{out} / v_{in} = -G_m R_{out}$$

电路的电压增益： —“电路跨导”×“输出电阻”

Example 9.8 Determine the voltage gain of the common-emitter stage shown in Fig. 9.15(a).

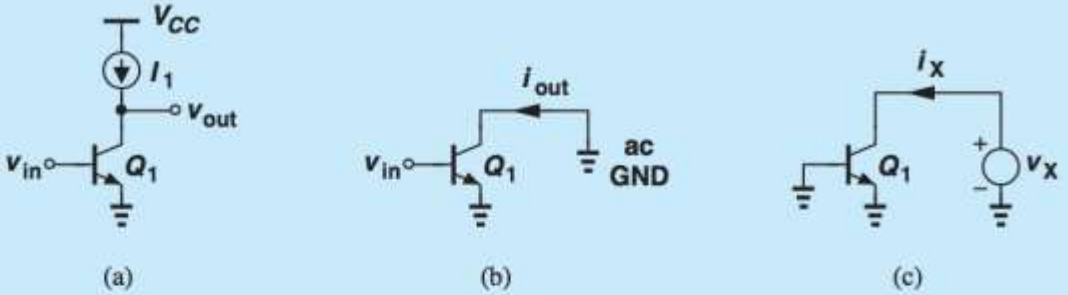


Figure 9.15

Solution To calculate the short-circuit transconductance of the circuit, we place an ac short from the output to ground and find the current through it [Fig. 9.15(b)]. In this case, i_{out} is simply equal to the collector current of Q_1, $g_{m1}v_{in}$, i.e.,

$$G_m = \frac{i_{out}}{v_{in}} \tag{9.37}$$

$$= g_{m1}. \tag{9.38}$$

Note that r_O does not carry a current in this test (why?). Next, we obtain the output resistance as depicted in Fig. 9.15(c):

$$R_{out} = \frac{v_X}{i_X} \tag{9.39}$$

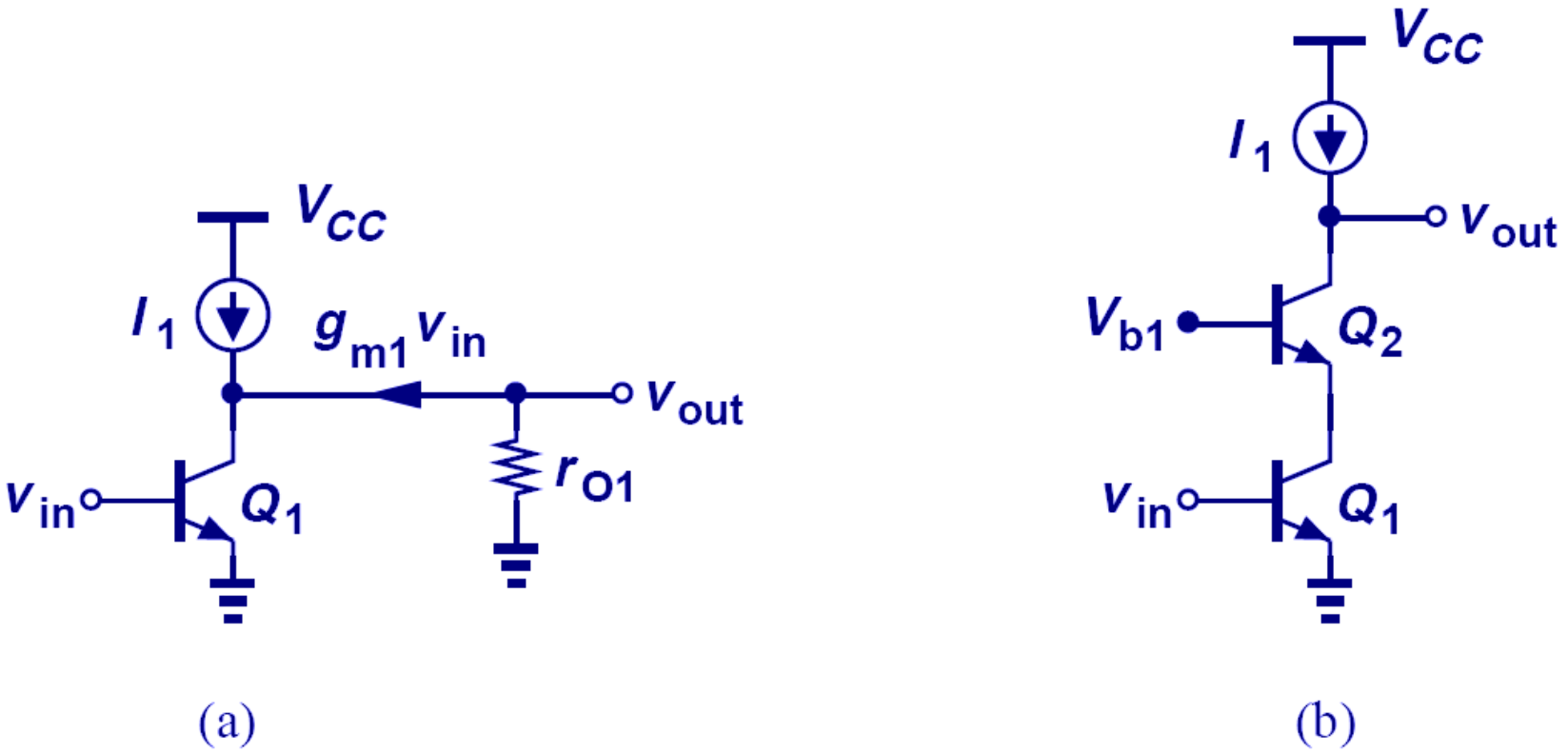
$$= r_{O1}. \tag{9.40}$$

It follows that

$$A_v = -G_m R_{out} \tag{9.41}$$

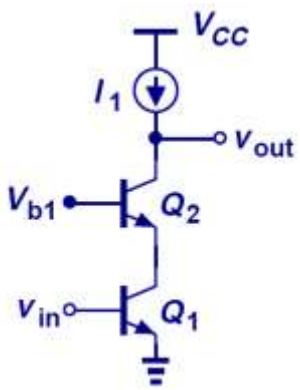
$$= -g_{m1} r_{O1}. \tag{9.42}$$

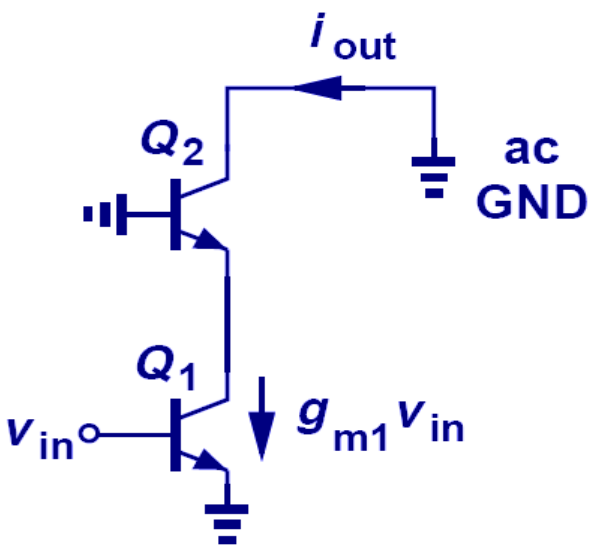
三极管 Cascode 和 CE 结构的比较



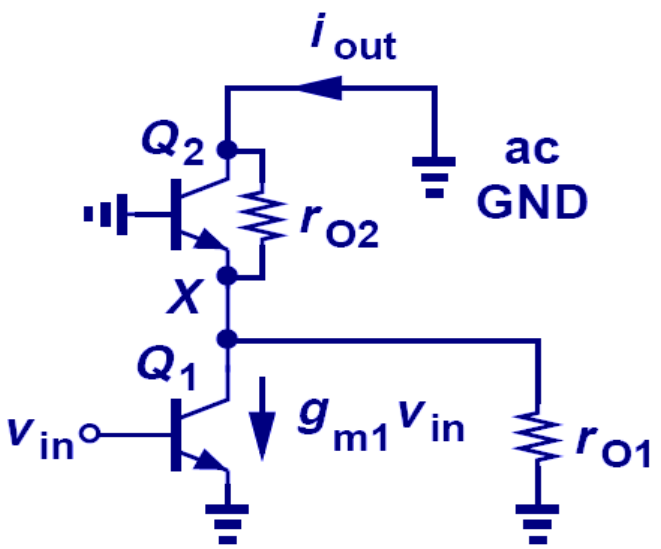
- 因为**cascode**的输出阻抗比**CE**要高很多，若两者G_m相当，则**cascode**结构的电压增益会高很多；

三极管 Cascode 电压增益的计算





(a)



(b)

$$G_m \approx g_{m1}$$

$$A_v \approx -g_{m1} r_{O2} g_{m2} (r_{O1} \| r_{\pi 2})$$

- 从X点向上看的阻抗是 $1/g_{m2}$,向右看的阻抗是r_{o1}，前者往往比后者小很多，所以 $i_{out} \approx g_{m1} v_{in}$.【输入电压→$Q_1$电流→$Q_2$电流】
- 因此，Q_2也被称为 Current Buffer（电流增益接近于1，输出阻抗大幅增加）【Voltage Buffer，电压增益接近于1，输出阻抗大幅降低】

例题

Example 9.9 The bipolar cascode of Fig. 9.16(b) is biased at a current of 1 mA. If $V_A = 5$ V and $\beta = 100$ for both transistors, determine the voltage gain. Assume the load is an ideal current source.

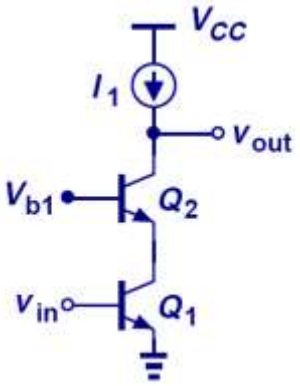
Solution We have $g_{m1} = (26\,\Omega)^{-1}$, $r_{\pi 1} \approx r_{\pi 2} \approx 2600\,\Omega$, $r_{O1} \approx r_{O2} = 5\,\text{k}\Omega$. Thus,

$$g_{m1}(r_{O1} \| r_{\pi 2}) = 65.8 \tag{9.54}$$

and from Eq. (9.53),

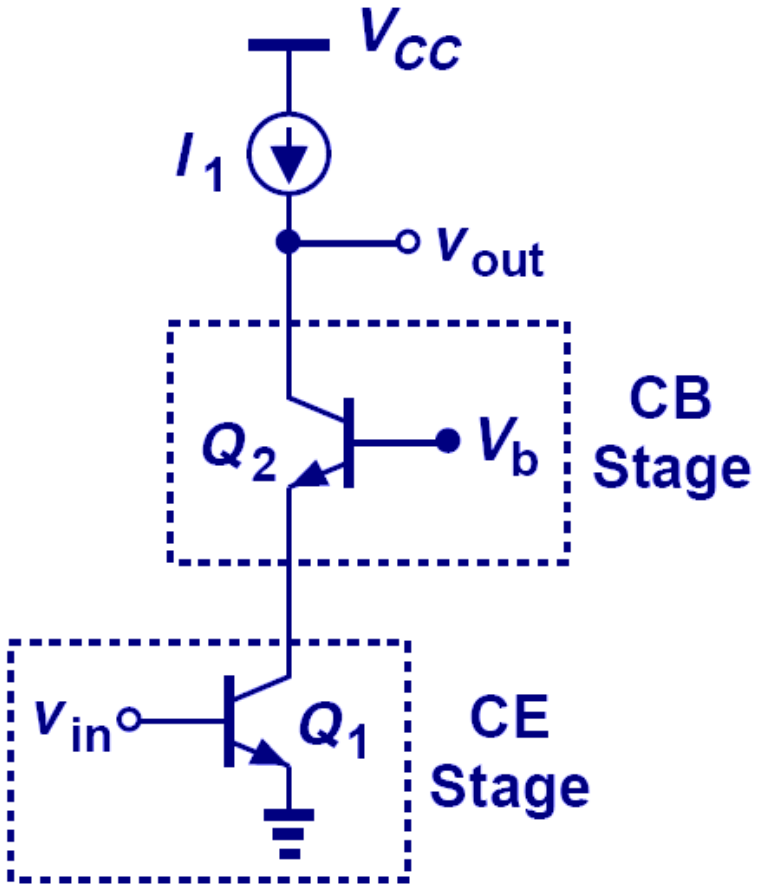
$$|A_v| = 12{,}654. \tag{9.55}$$

Cascoding thus raises the voltage gain by a factor of 65.8.



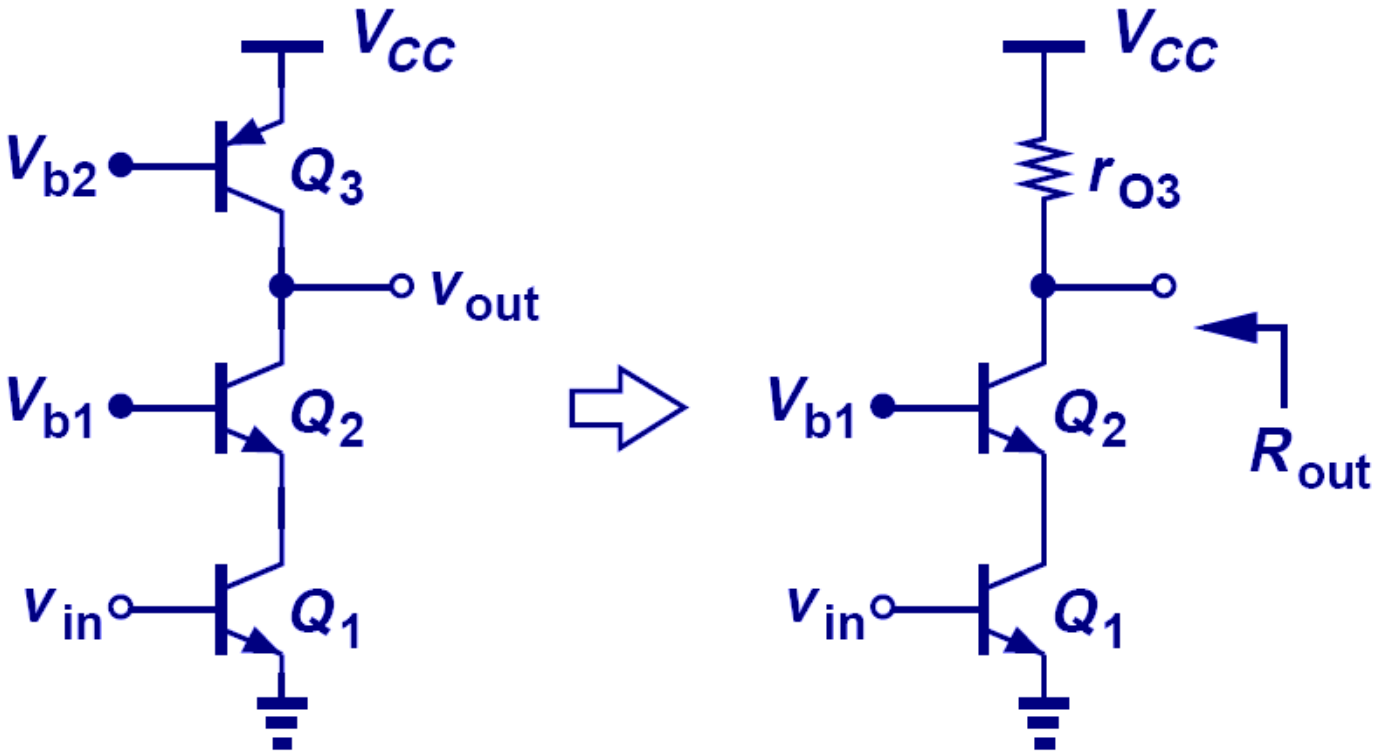
$$G_m \approx g_{m1}$$
$$A_v \approx -g_{m1} r_{O2} g_{m2} (r_{O1} \| r_{\pi 2})$$

Cascode 放大器的另一种解释



- Cascode 放大器也可以看作是CE和CB的串联；

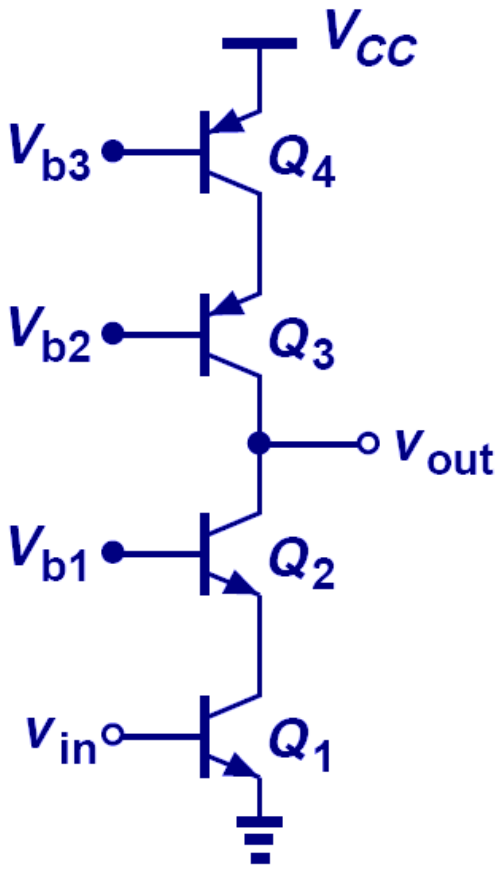
实用 Cascode 结构



$$R_{out} \approx r_{O3} \| g_{m2} r_{O2} (r_{O1} \| r_{\pi 2})$$

- 作为电流源负载的**Q3**也存在输出阻抗，所以会使整体电路的输出阻抗降低，从而降低电压增益；

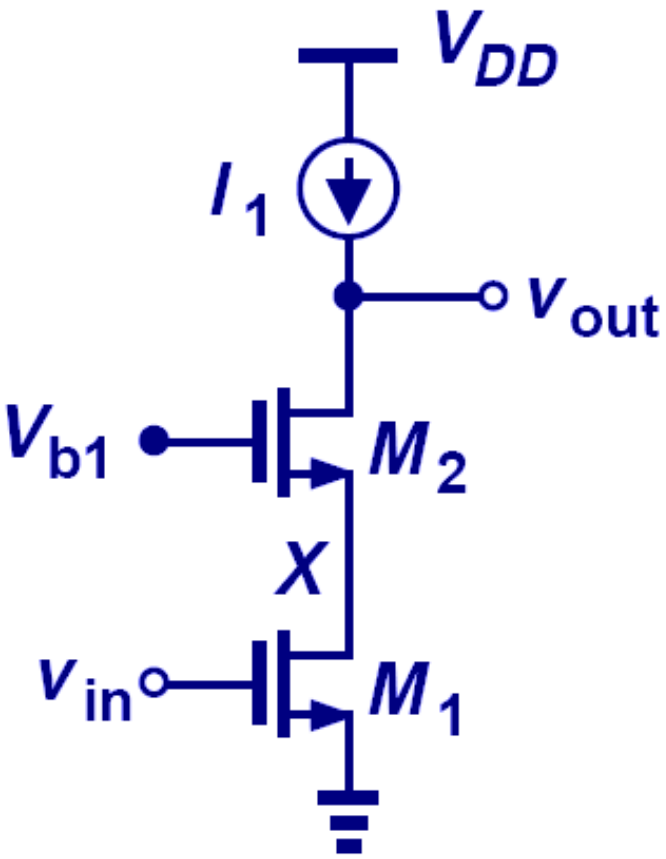
改进型 Cascode 结构



$$R_{out} \approx g_{m3} r_{O3} (r_{O4} \| r_{\pi 3}) \| g_{m2} r_{O2} (r_{O1} \| r_{\pi 2})$$

- 同样，我们可以采用 **cascode** 结构提高电流源负载的输出电阻

MOS Cascode 放大器

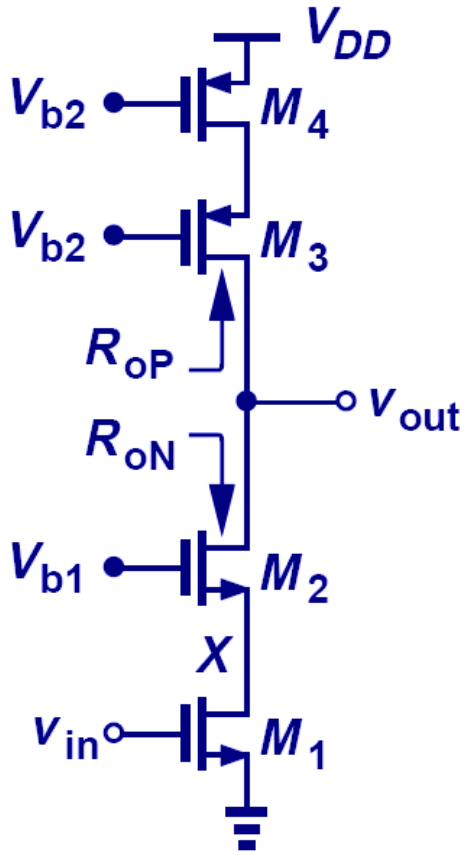


$$A_v = -G_m R_{out}$$

$$A_v \approx -g_{m1}\left[(1+g_{m2}r_{O2})r_{O1} + r_{O2}\right]$$

$$A_v \approx -g_{m1}r_{O1}g_{m2}r_{O2}$$

改进型 MOS Cascode 结构放大器



$$R_{on} \approx g_{m2} r_{O2} r_{O1}$$

$$R_{op} \approx g_{m3} r_{O3} r_{O4}$$

$$R_{out} = R_{on} \| R_{op}$$

- 与三极管电路类似， **MOS cascode** 放大器的输出阻抗也可以采用 **cascode** 结构的 **PMOS** 电流源负载来提高；

Example 9.11

The cascode amplifier of Fig. 9.20(b) incorporates the following device parameters: $(W/L)_{1,2} = 30$, $(W/L)_{3,4} = 40$, $I_{D1} = \cdots = I_{D4} = 0.5$ mA. If $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 50\,\mu\text{A/V}^2$, $\lambda_n = 0.1\,\text{V}^{-1}$ and $\lambda_p = 0.15\,\text{V}^{-1}$, determine the voltage gain.

Solution

With the particular choice of device parameters here, $g_{m1} = g_{m2}$, $r_{O1} = r_{O2}$, $g_{m3} = g_{m4}$, and $r_{O3} = r_{O4}$. We have

$$g_{m1,2} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2} I_{D1,2}} \tag{9.73}$$

$$= (577\,\Omega)^{-1} \tag{9.74}$$

and

$$g_{m3,4} = (707\,\Omega)^{-1}. \tag{9.75}$$

Also,

$$r_{O1,2} = \frac{1}{\lambda_n I_{D1,2}} \tag{9.76}$$

$$= 20\,\text{k}\Omega \tag{9.77}$$

and

$$r_{O3,4} = 13.3\,\text{k}\Omega. \tag{9.78}$$

Equations (9.70) and (9.71) thus respectively give

$$R_{on} \approx 693\,\text{k}\Omega \tag{9.79}$$

$$R_{op} \approx 250\,\text{k}\Omega \tag{9.80}$$

and

$$A_v = -g_{m1}(R_{on} || R_{op}) \tag{9.81}$$

$$\approx -318. \tag{9.82}$$

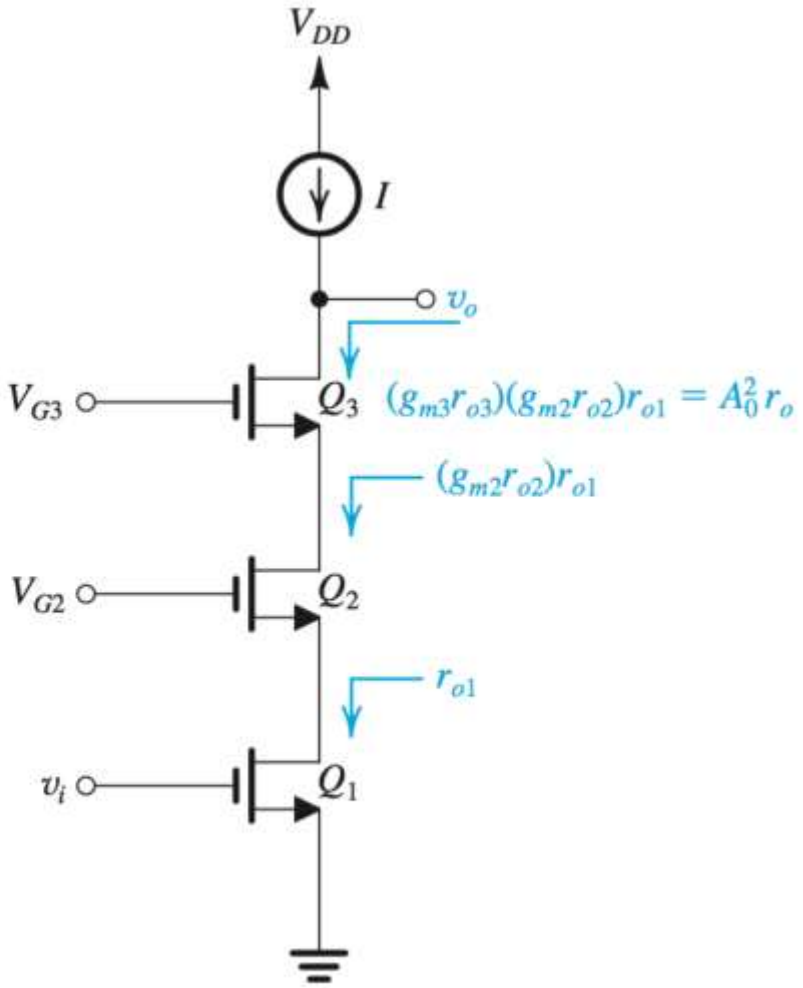


Figure 7.15 Double cascoding.

- 目的：获得更大的输出阻抗→更大的增益；
- 缺点：从V_{DD}到GND有太多的管子级联（①理想电流源也需要用Double Cascoding实现，导致有6个管子；②现代CMOS电路V_{DD}接近于1V，V_{OV}一般在0.1~0.2V；③每个管子必须工作在饱和区，v_{DS}至少需要v_{OV}）

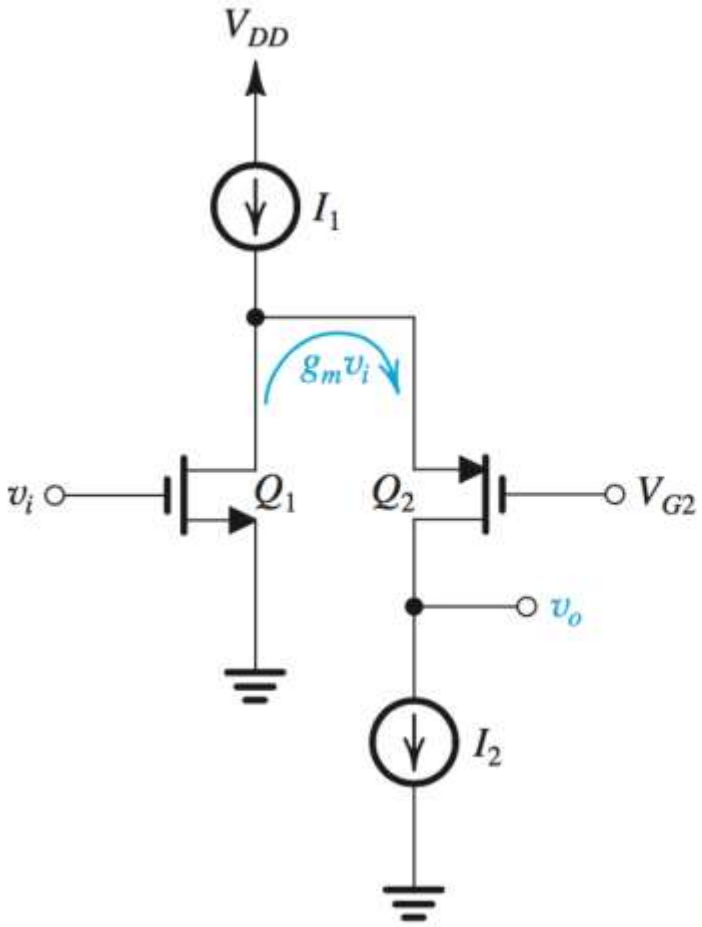


Figure 7.16 The folded cascode.

- Cascode结构中的CB用PMOS实现；
- Q_2的偏置电流为I_2；Q_1的偏置电流为I_1-I_2;
- 小信号分析呢？
- 该结构在现代CMOS电路设计中非常流行

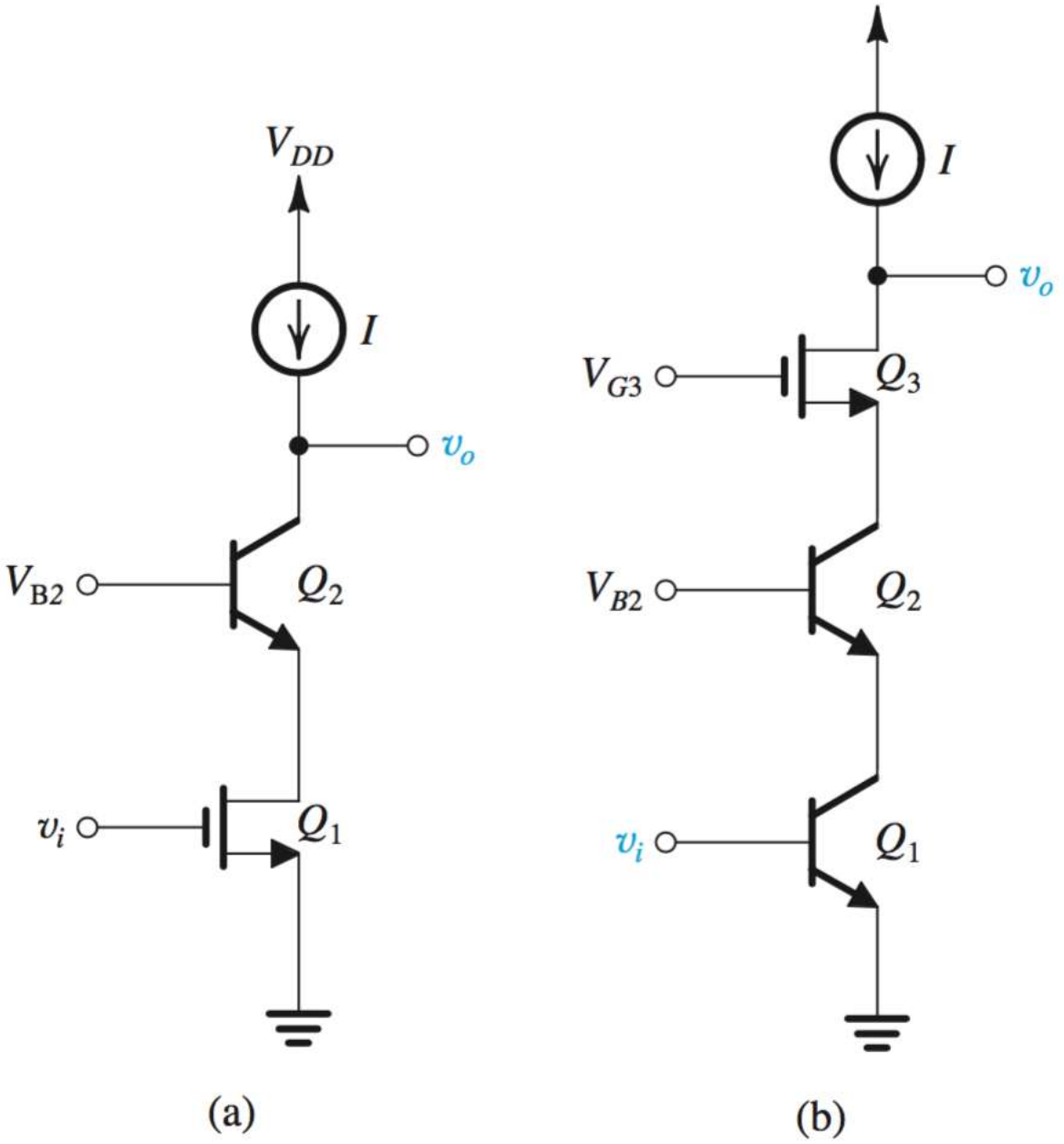
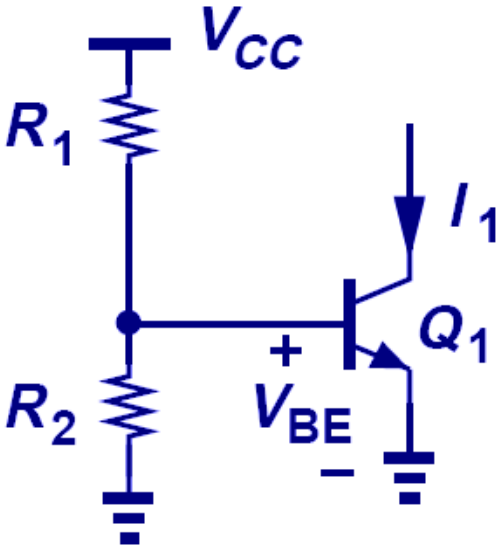


Figure 7.21 BiCMOS cascodes.

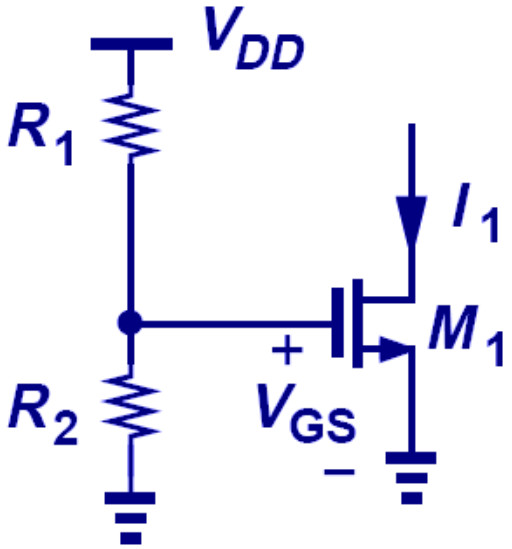
电流镜

偏置电流对温度、供电电压波动敏感



(a)

思考：我们的实际生活中，有什么例子是温度会波动？供电电压会波动？但我们的手机还是需要能正常工作



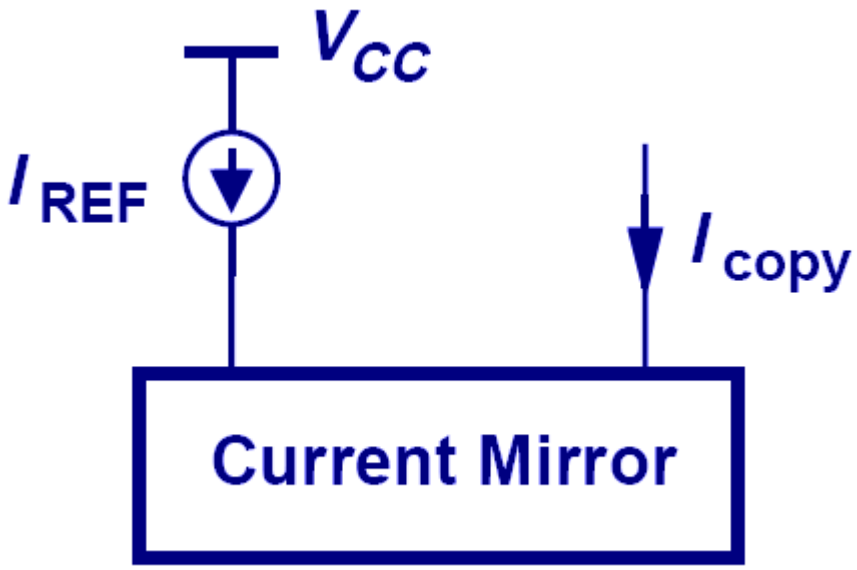
(b)

$$R_2 V_{CC}/(R_1+R_2) = V_T \ln(I_1/I_S)$$

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2$$

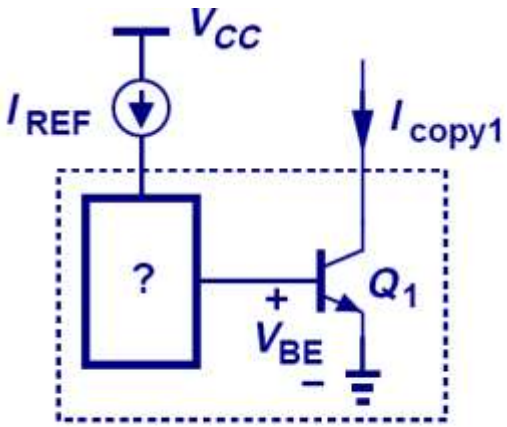
- 因为 V_T, I_S, μ_n, V_{TH} 等参数对温度敏感，所以电路中 I_1 会随温度和供电电压的波动而变化

Current Mirror （电流镜）的概念

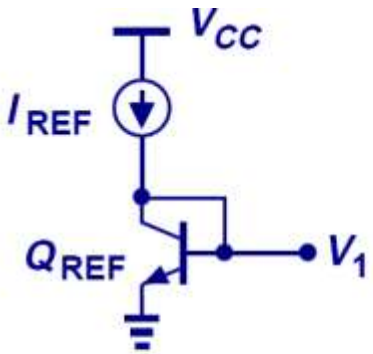


- 假如我们有一个完美的参考电流源（电流不随温度和供电电压的波动而变化），同时我们又有一套完美的“复制”工具，那么在电路中任意需要的地方我们都可以实现不随温度和供电电压波动的电流源；

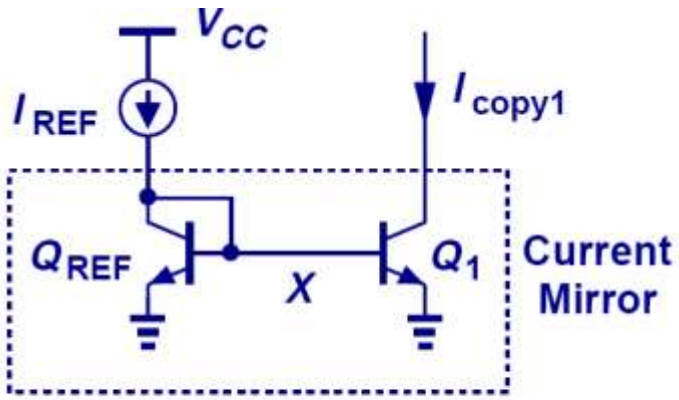
三极管电流镜实现



(a)



(b)



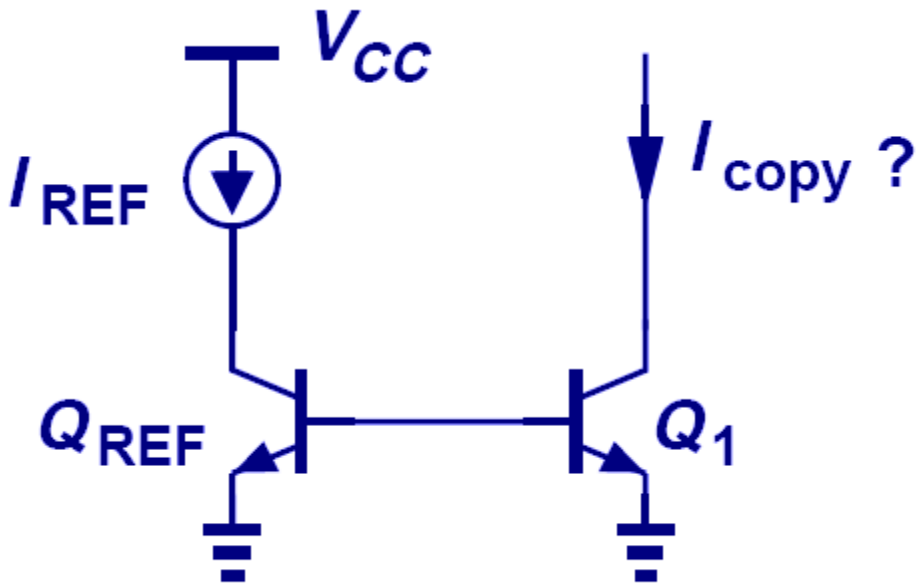
(c)

$$I_{REF} = I_{S,REF} \exp \frac{V_X}{V_T}$$

$$I_{copy} = I_{S1} \exp \frac{V_X}{V_T}$$

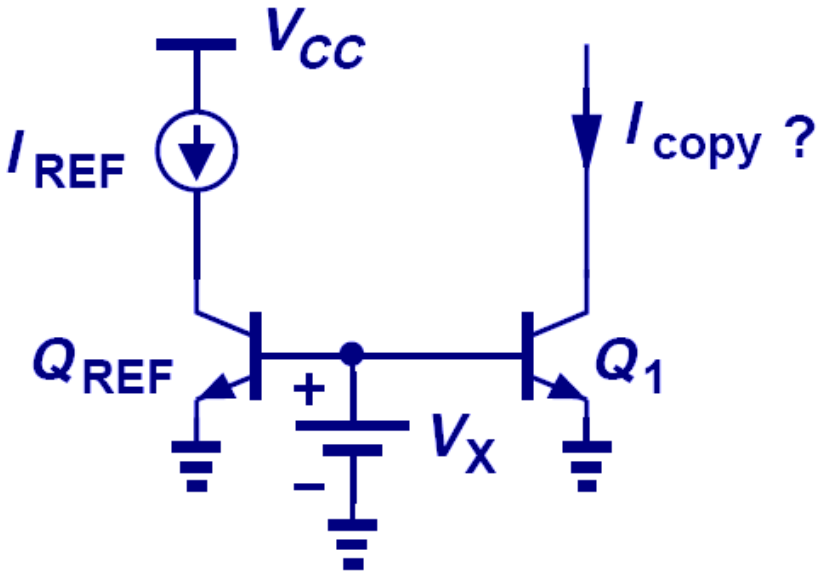
$$I_{copy} = \frac{I_{S1}}{I_{S,REF}} I_{REF}$$

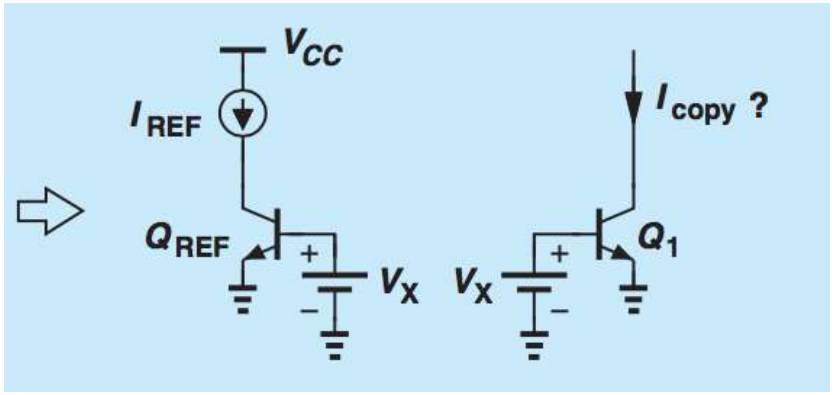
这样可以吗？



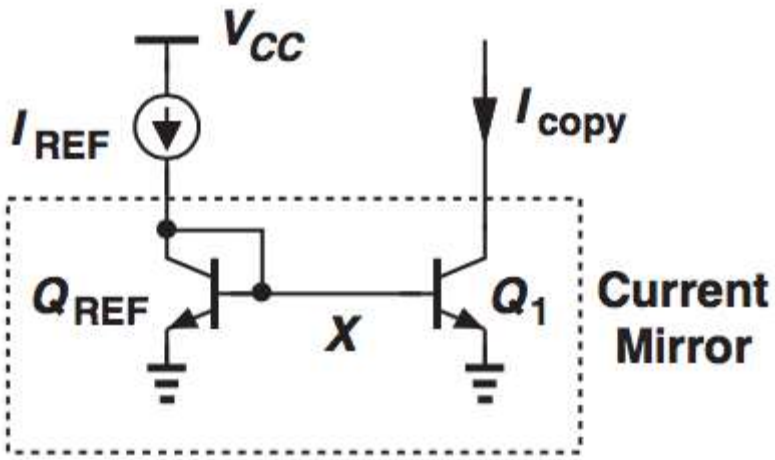
- 若Q_{REF}不是 diode-connected (C和B相连) 接法，则两个管子的基极电流没有通路，电路不能工作

那这么改进可以吗？





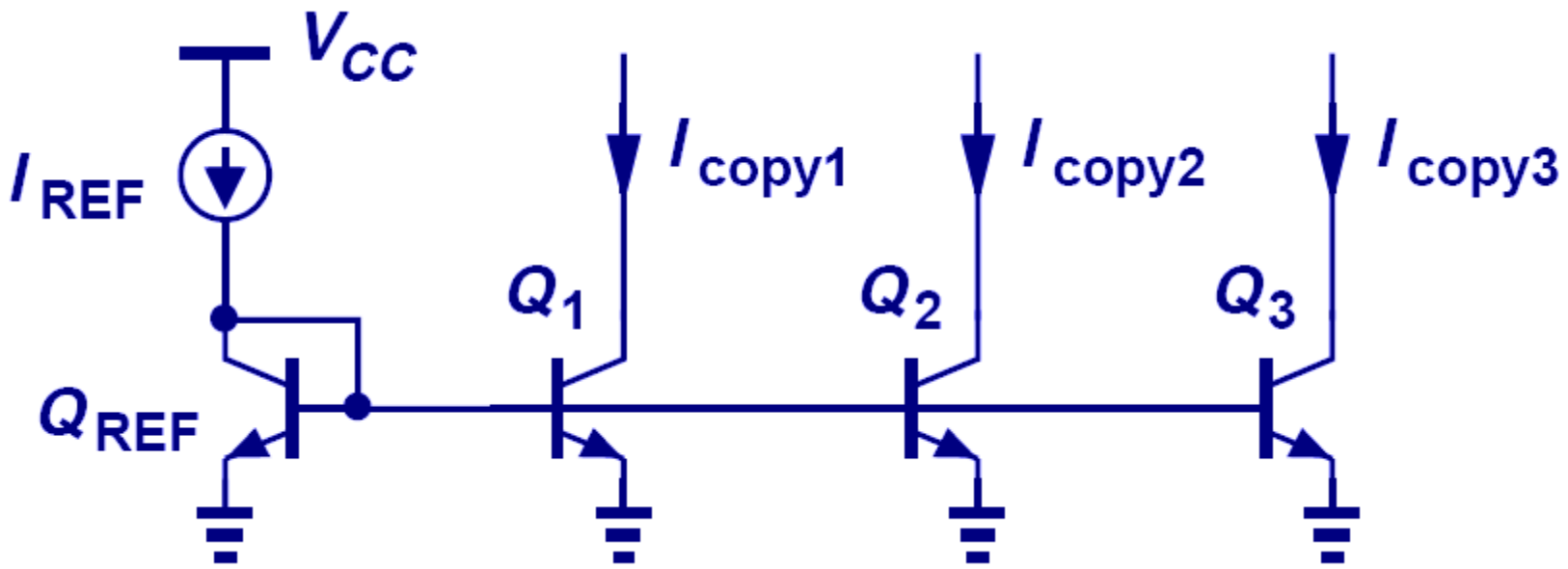
- Vx为基极电流提供了通路，但是Icopy变得与Iref无关了



(c)

- 因此，Q_{REF}必须为 diode-connected 接法！

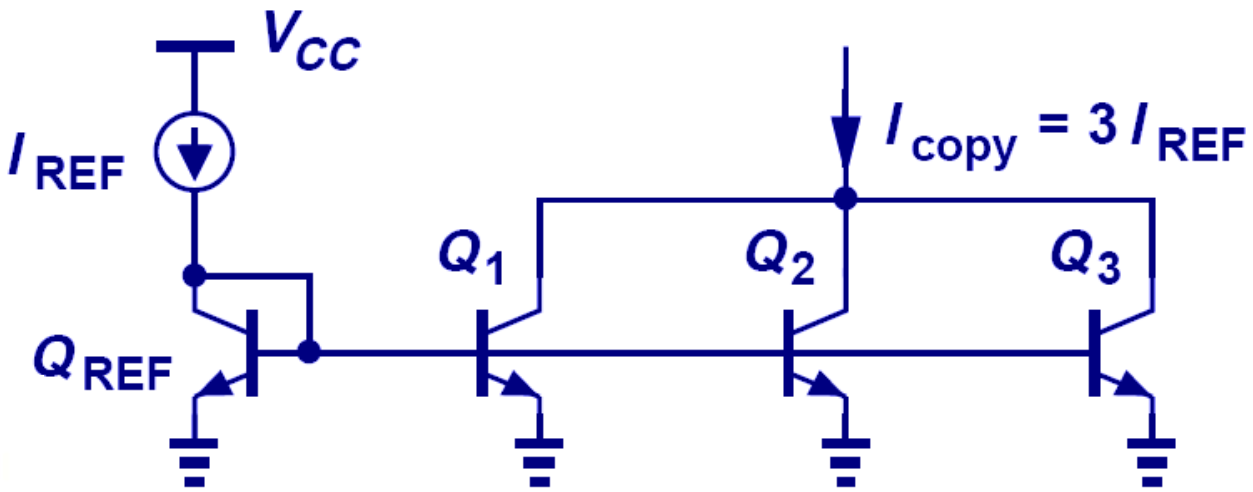
I_{REF} 可多次复制



$$I_{copy,j} = \frac{I_{S,j}}{I_{S,REF}} I_{REF}$$

- 电流镜的复制结构可多次使用，可方便地将I_{REF}复制到多个地方

成倍复制



$$I_C = I_S \exp \frac{V_{BE}}{V_T},$$

$$I_S = \frac{A_E q D_n n_i^2}{N_B W_B}.$$

$$I_{copy,j} = \frac{I_{S,j}}{I_{S,REF}} I_{REF}$$

$$I_{copy,j} = nI_{REF}$$

- 三极管的饱和电流I_S与面积成正比，若我们将 Q_j 的面积扩大为Q_{REF}的n倍，那么$I_{copy,j}$ 也将扩到到 I_{REF}的n倍.
- 将面积扩大到n倍等效于将相同面积的n个三极管并联；

例题

Example 9.14

A multistage amplifier incorporates two current sources of values 0.75 mA and 0.5 mA. Using a bandgap reference current of 0.25 mA, design the required current sources. Neglect the effect of the base current for now.

Solution Figure 9.27 illustrates the circuit. Here, all transistors are identical to ensure proper scaling of I_{REF}.

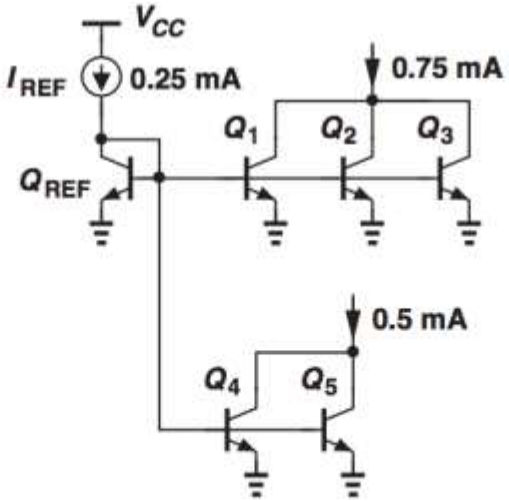
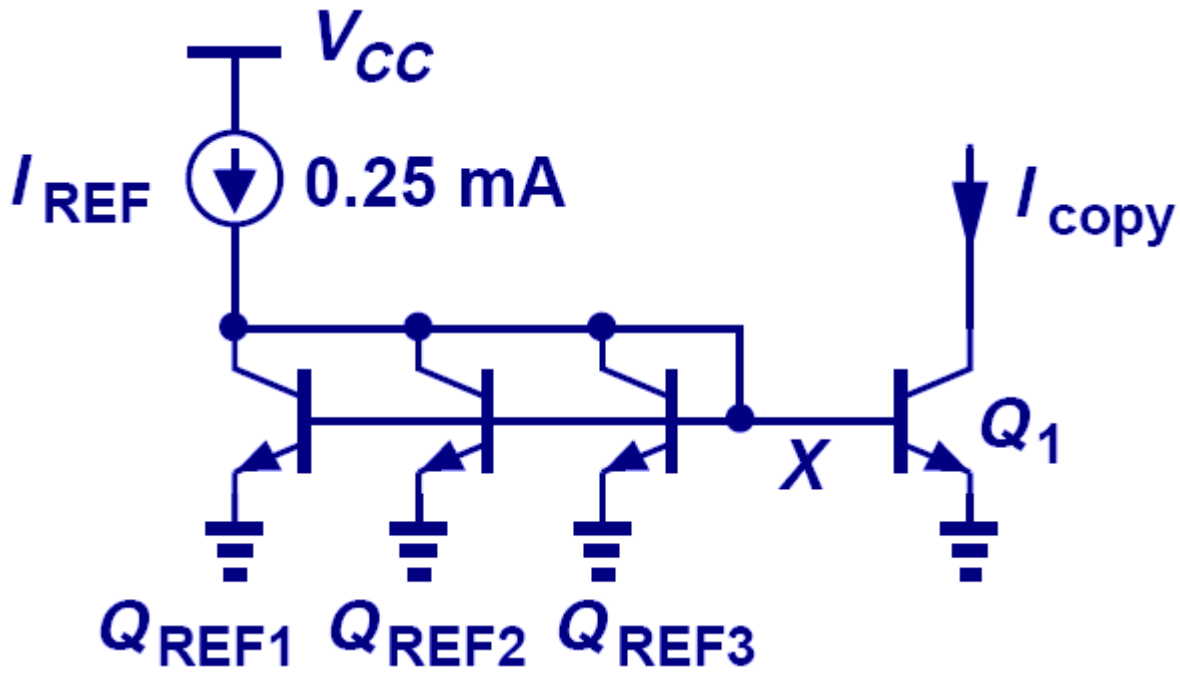


Figure 9.27

分数倍复制



$$I_{REF} = 3I_S \exp\frac{V_X}{V_T}$$

$$I_{copy} = I_S \exp\frac{V_X}{V_T}$$

$$\Rightarrow \quad I_{copy} = \frac{1}{3} I_{REF}$$

- 同样，我们若提高Q_{REF}的面积（或Q_{REF}由多个三极管并联），就可获得分数倍的复制电流

例题

Example 9.15 It is desired to generate two currents equal to 50 μA and 500 μA from a reference of 200 μA. Design the current mirror circuit.

Solution To produce the smaller current, we must employ four unit transistors for Q_{REF} such that each carries 50 μA. A unit transistor thus generates 50 μA (Fig. 9.29). The current of 500 μA requires 10 unit transistors, denoted by $10A_E$ for simplicity.

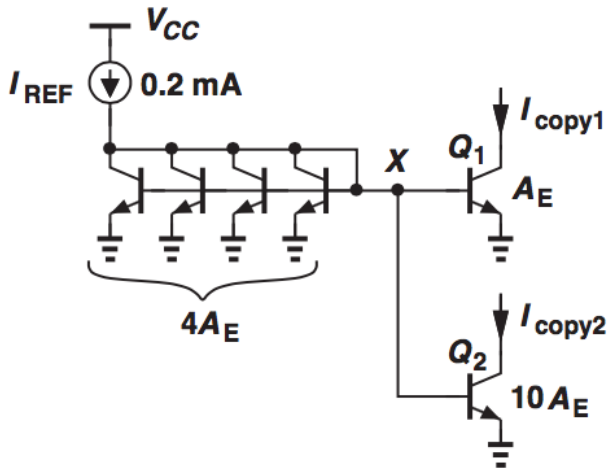
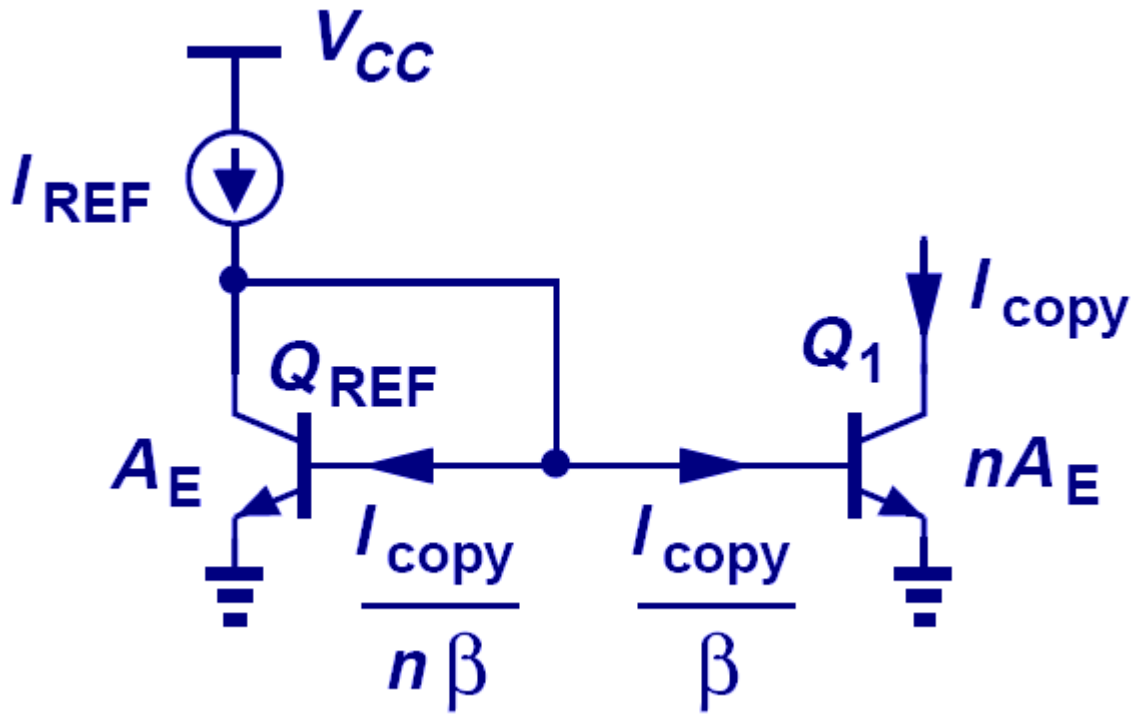


Figure 9.29

基极电流引起的误差

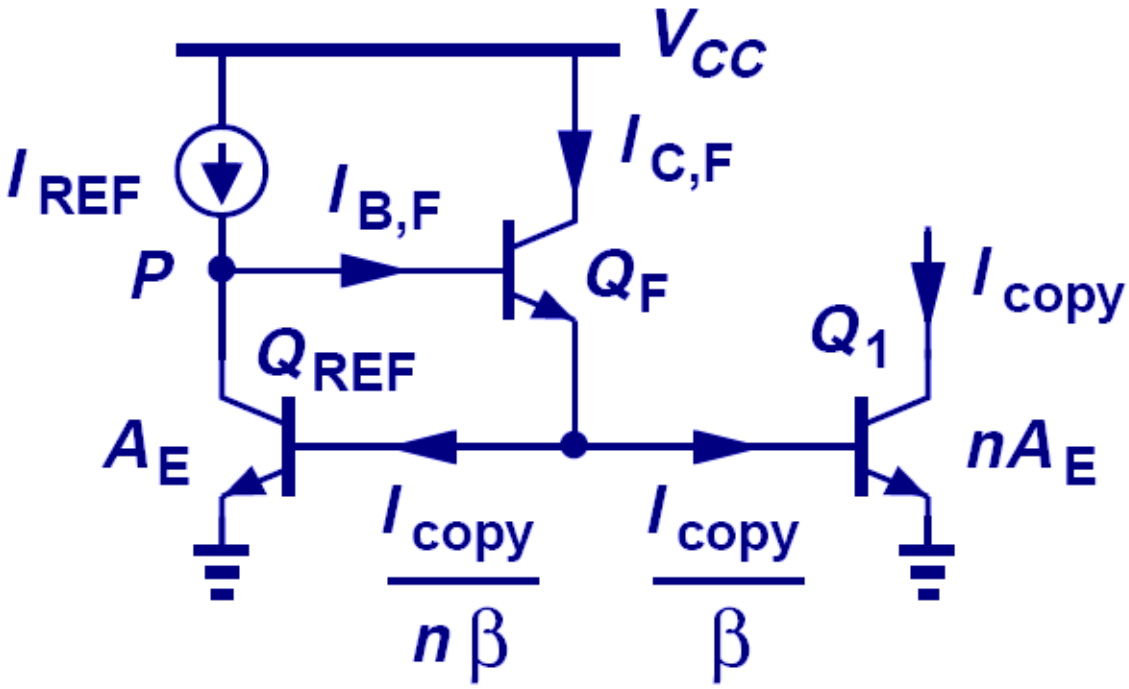


$$I_{REF} = I_{C,REF} + \frac{I_{copy}}{\beta} \cdot \frac{1}{n} + \frac{I_{copy}}{\beta}$$

$$I_{C,REF} = I_{copy}/n$$

$$I_{copy} = \frac{nI_{REF}}{1 + \frac{1}{\beta}(n+1)}$$

改进方法：基极电流补偿



$$I_{copy} = \frac{nI_{REF}}{1+\frac{1}{\beta^2}(n+1)}$$

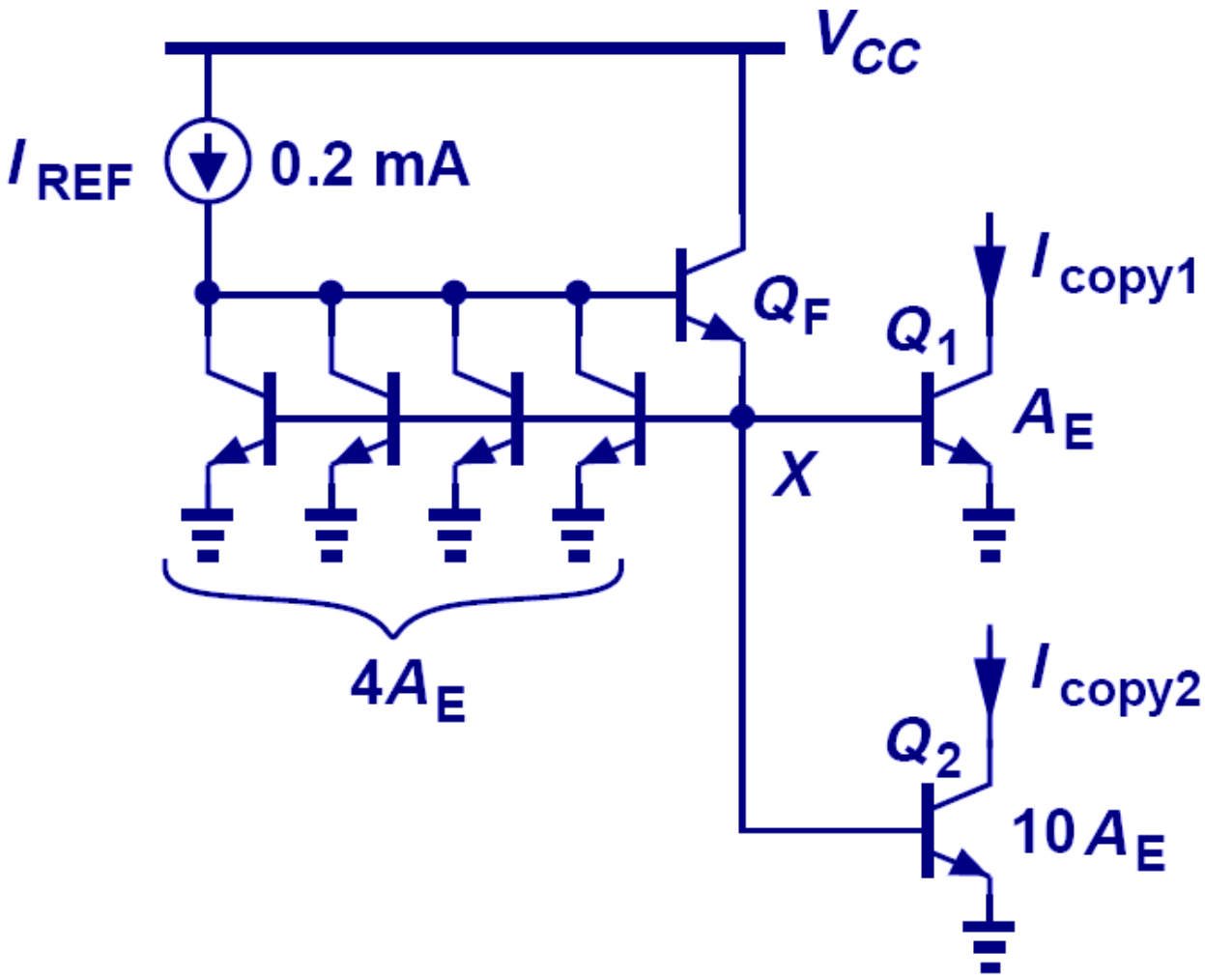
$$I_{C,F} = \frac{I_{copy}}{\beta} + \frac{I_{copy}}{\beta}\cdot\frac{1}{n},$$

$$I_{B,F} = \frac{I_{copy}}{\beta^2}\left(1+\frac{1}{n}\right).$$

$$I_{REF} = I_{B,F} + I_{C,REF}$$

$$= \frac{I_{copy}}{\beta^2}\left(1+\frac{1}{n}\right) + \frac{I_{copy}}{n}$$

思考，考虑基极电流（电流增益为β）

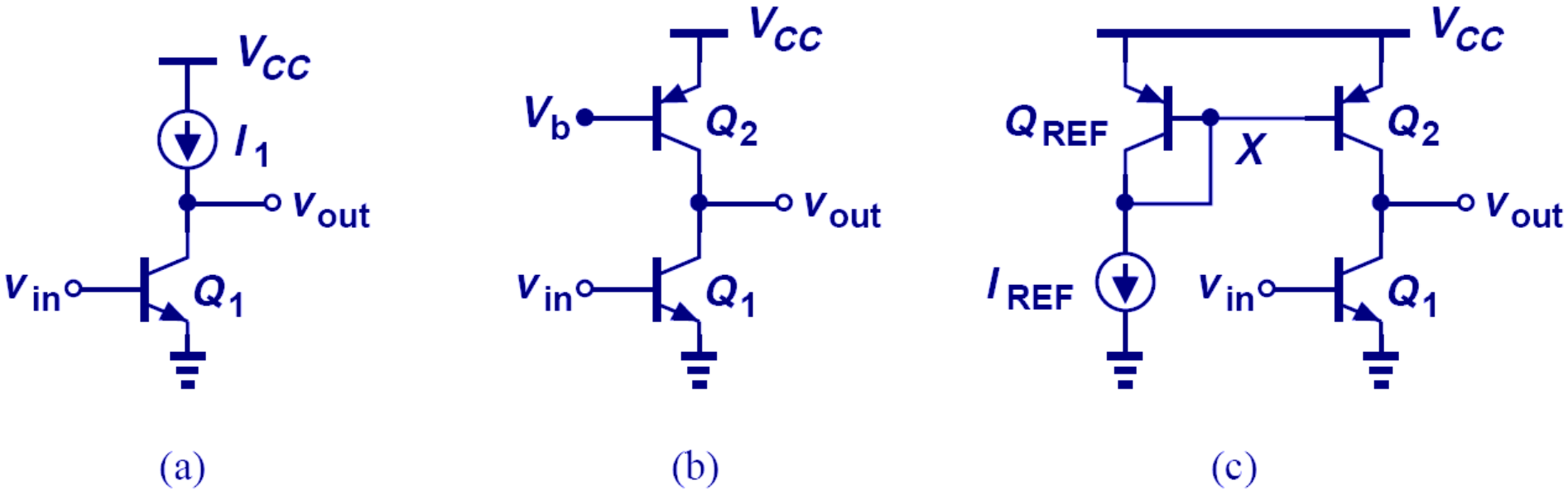


$$I_{copy1} = \frac{I_{REF}}{4 + \frac{15}{\beta^2}}$$

$$I_{copy2} = \frac{10 I_{REF}}{4 + \frac{15}{\beta^2}}$$

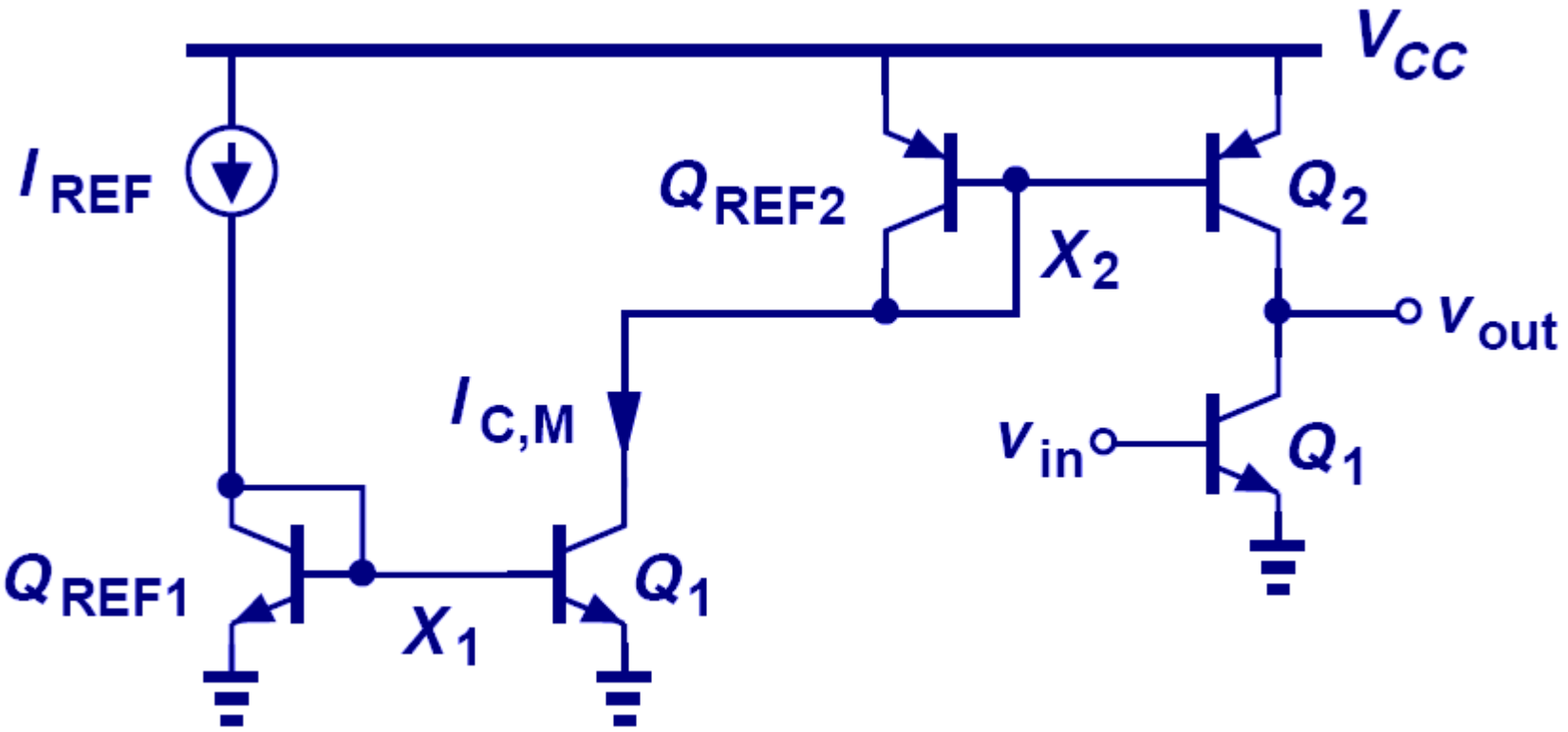
$$I_{REF} = 4I_{copy1} + \frac{I_{copy1}}{\beta^2} + \frac{10I_{copy1}}{\beta^2} + \frac{4I_{copy1}}{\beta^2}$$

PNP 电流镜

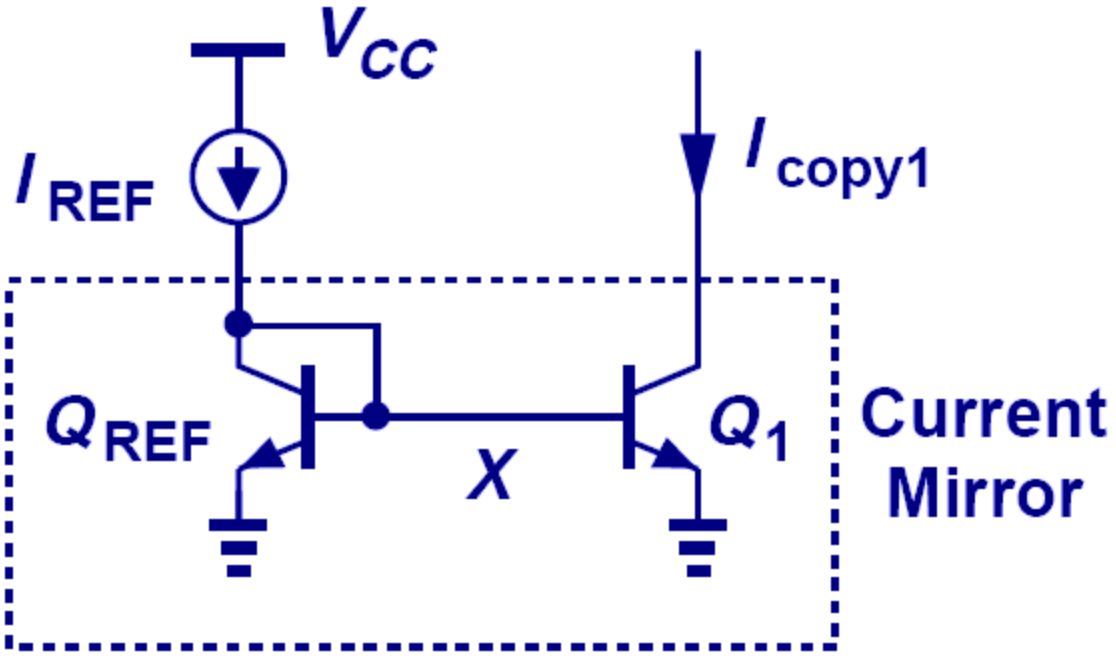


- 我们经常需要用到电流源作为负载，该电流源可以用**PNP**电流镜实现

PNP 电流镜参考电流的产生



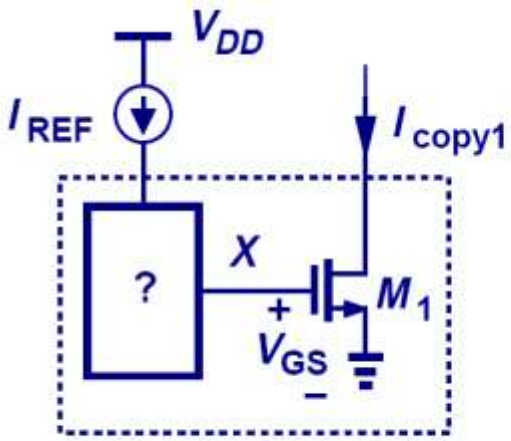
离散器件可以用来做电流镜吗？



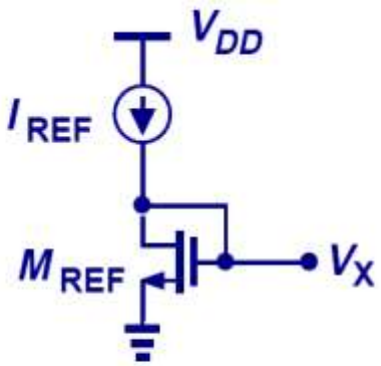
$$I_S = \frac{A_E q D_n n_i^2}{N_B W_B}.$$

- 若 Q_{REF} 和 Q_1 是离散的 NPN 器件（非集成电路内部的器件），同样尺寸的器件I_S的离散性会比较大，所以很少会用离散器件来搭建电流镜

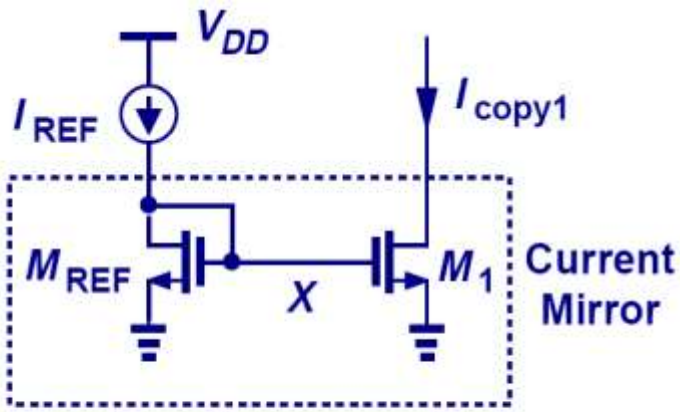
MOS 电流镜



(a)



(b)



(c)

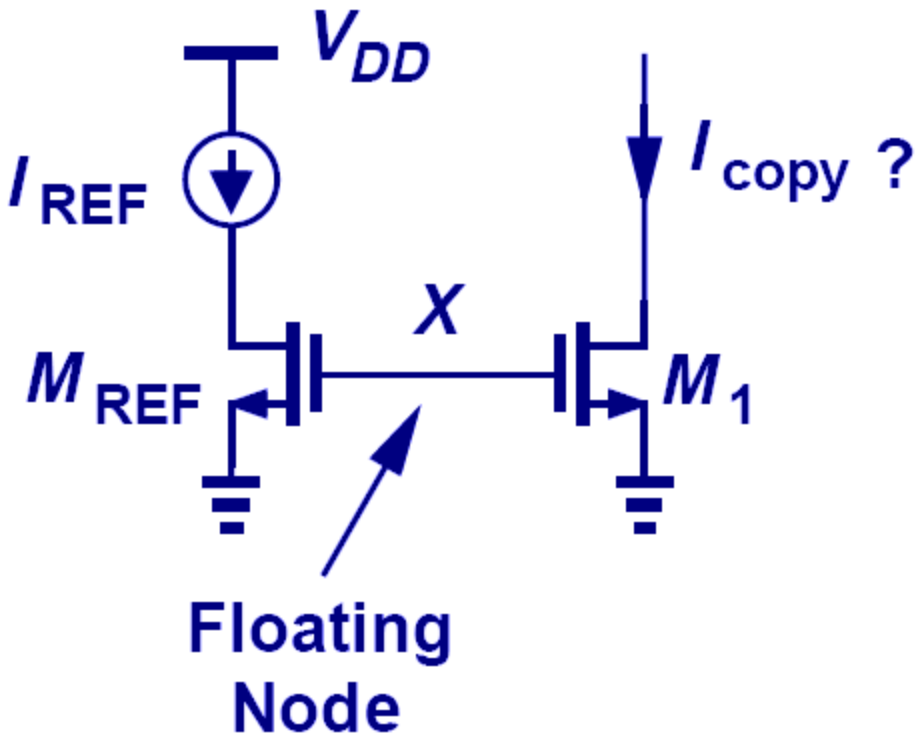
$$I_{D,REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{REF}(V_X - V_{TH})^2$$

$$I_{copy} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1(V_X - V_{TH})^2,$$

$$\Rightarrow \quad I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF},$$

- 同样，电流镜的思路和结构也可以用在MOS电路中

这样可以吗？



- 同样，参考MOS管也必须用“diode-connected”结构

成比例复制

Example 9.21

An integrated circuit employs the source follower and the common-source stage shown in Fig. 9.37(a). Design a current mirror that produces I_1 and I_2 from a 0.3-mA reference.

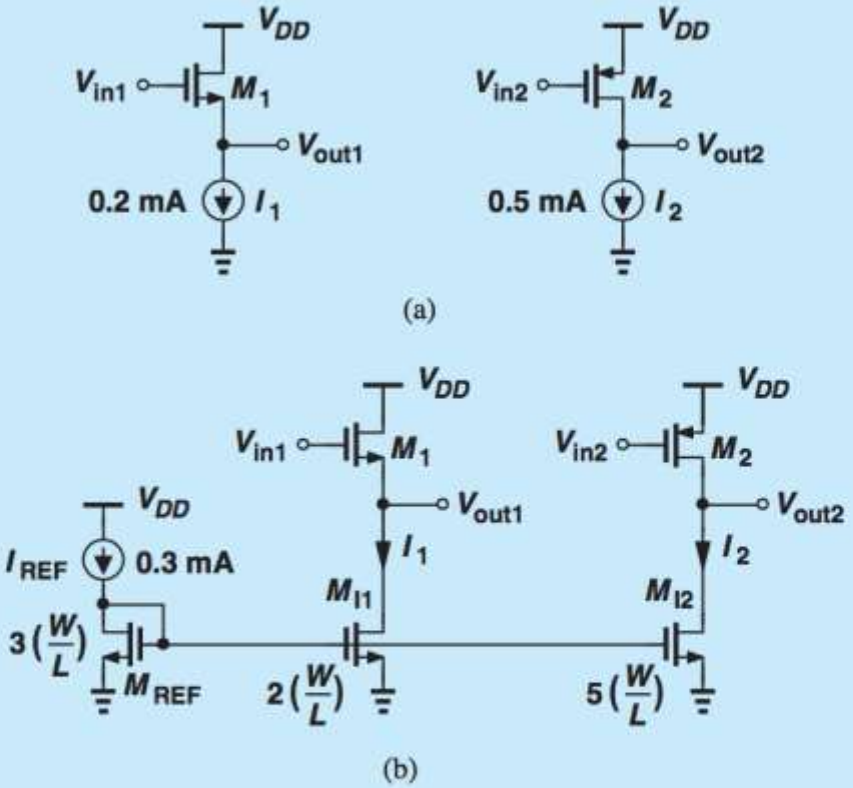
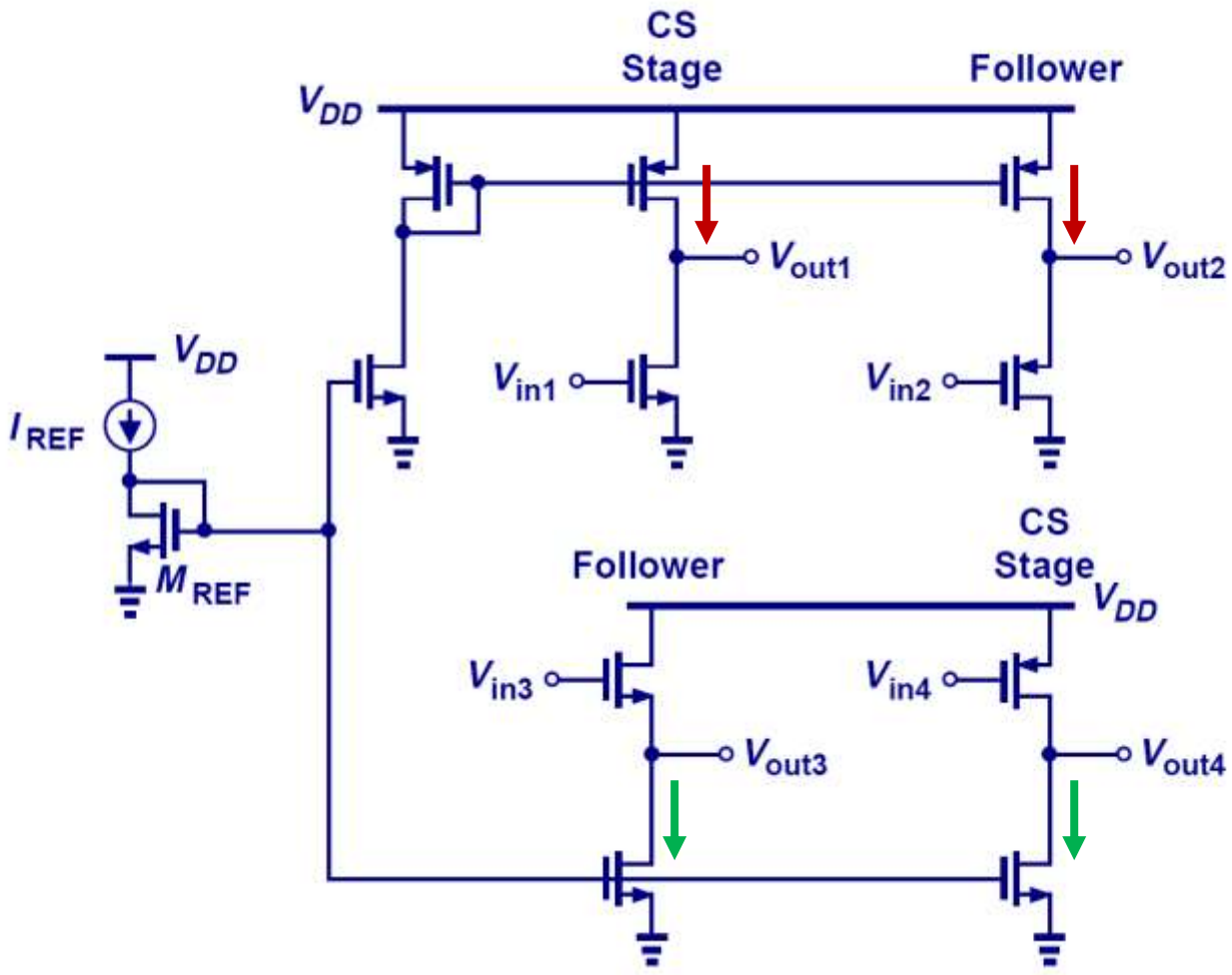


Figure 9.37

Solution Following the methods depicted in Figs. 9.28 and 9.29, we select an aspect ratio of $3(W/L)$ for the diode-connected device, $2(W/L)$ for M_{I1}, and $5(W/L)$ for M_{I2}. Figure 9.37(b) shows the overall circuit.

CMOS 电流镜

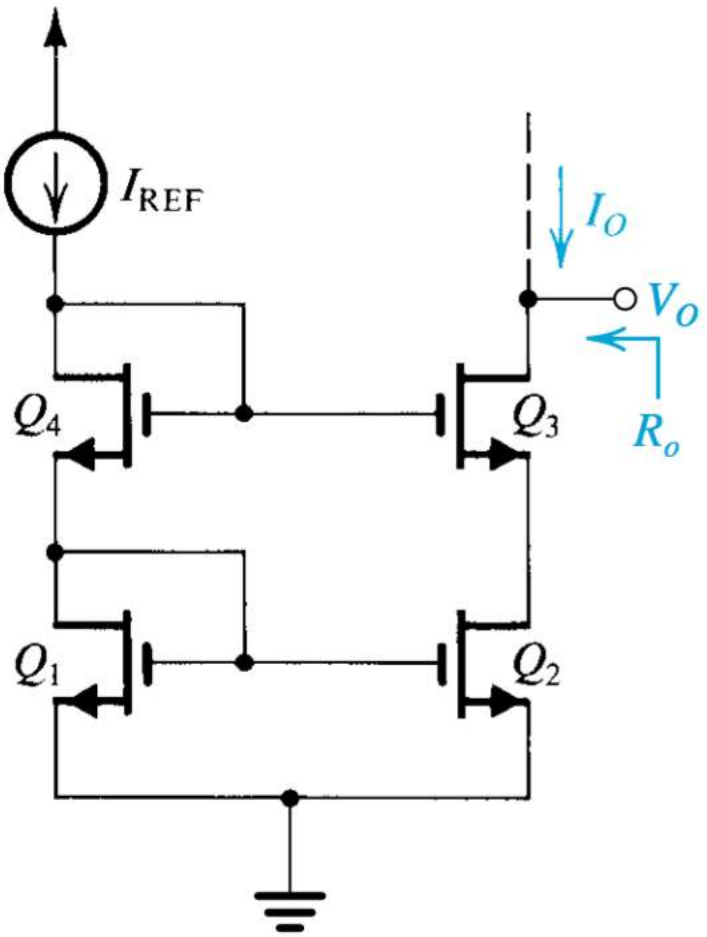


current source

current sink

- CMOS电路设计中最基本、最常用的模块

Cascode MOS Mirrors

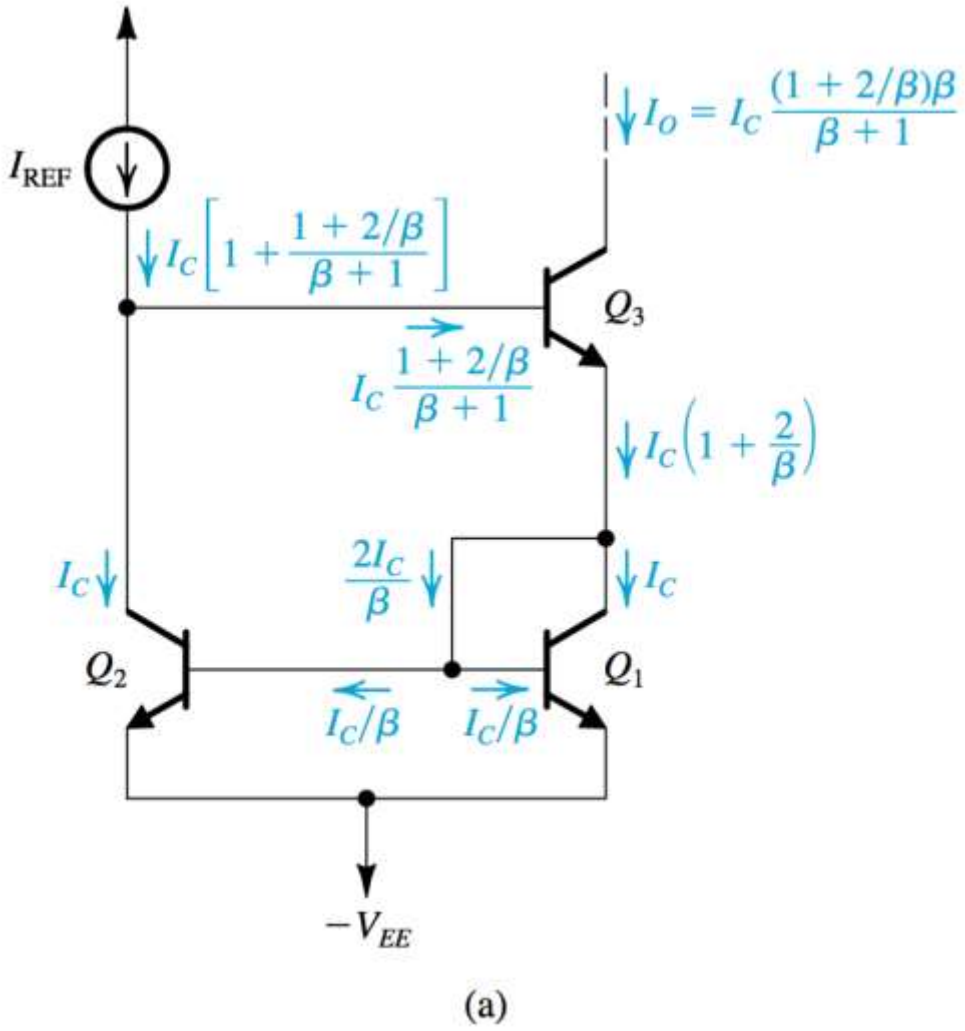


$$R_o \simeq g_{m3} r_{o3} r_{o2}$$

Figure 7.32 A cascode MOS current mirror.

- 提高电流源的输出阻抗
- 缺点是输出电压的摆幅减小（要保证Q2、Q3都工作在饱和区）

Wilson Current Mirror



(a)

$$\frac{I_O}{I_{REF}} = \frac{I_C\left(1+\frac{2}{\beta}\right)\beta/(\beta+1)}{I_C\left[1+\left(1+\frac{2}{\beta}\right)/(\beta+1)\right]}$$

$$= \frac{\beta+2}{\beta+1+\frac{\beta+2}{\beta}} = \frac{\beta+2}{\beta+2+\frac{2}{\beta}}$$

$$= \frac{1}{1+\frac{2}{\beta(\beta+2)}}$$

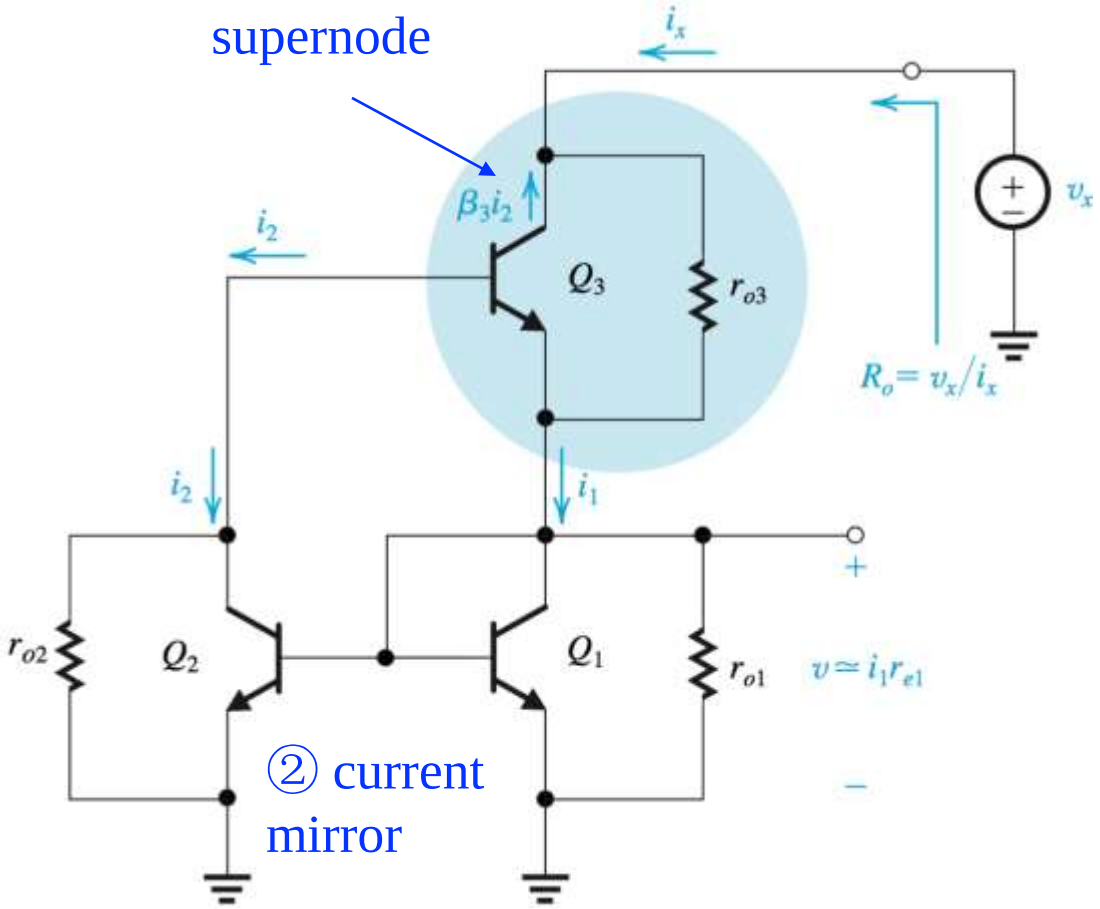
$$\simeq \frac{1}{1+2/\beta^2}$$

优点：1）降低β的影响；

输出阻抗计算

① $i_1 + i_2 = i_x$

① view as a supernode



② $i_2 \simeq i_1 = i_x/2$

③流过r_{o3}的电流： $i_x + \beta_3 i_2 = i_x + \beta_3 (i_x/2) = i_x(\beta_3/2 + 1)$

$$v_x = i_x\left(\frac{\beta_3}{2} + 1\right) r_{o3} + i_1 r_{e1}$$

$$= i_x\left(\frac{\beta_3}{2} + 1\right) r_{o3} + \left(\frac{i_x}{2}\right) r_{e1}$$

Since $r_o \gg r_e$ and $\beta_3 \gg 2$,

$$v_x \simeq i_x\left(\frac{\beta_3}{2}\right) r_{o3}$$

$$R_o = \beta_3 r_{o3}/2$$

优点：2）增加输出电阻

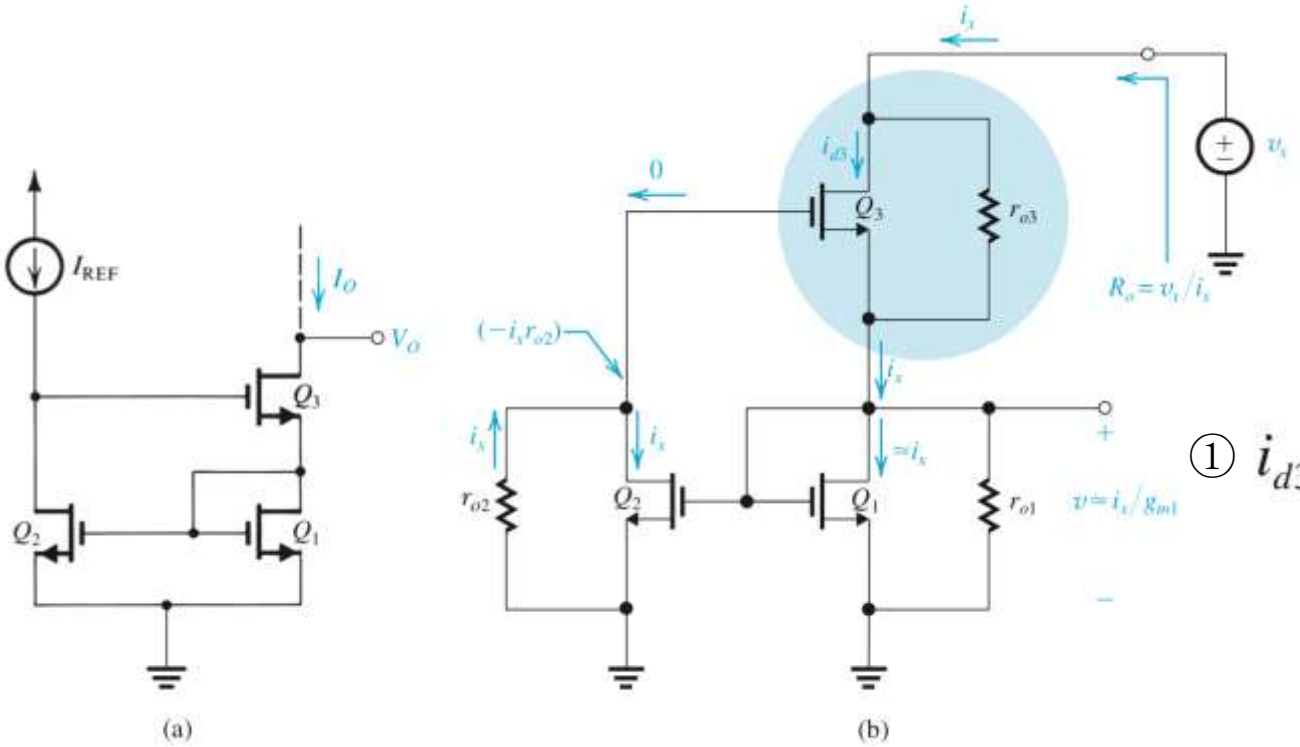


Figure 8.41 The Wilson MOS mirror: (**a**) circuit; (**b**) analysis to determine output resistance; (**c**) modified circuit.

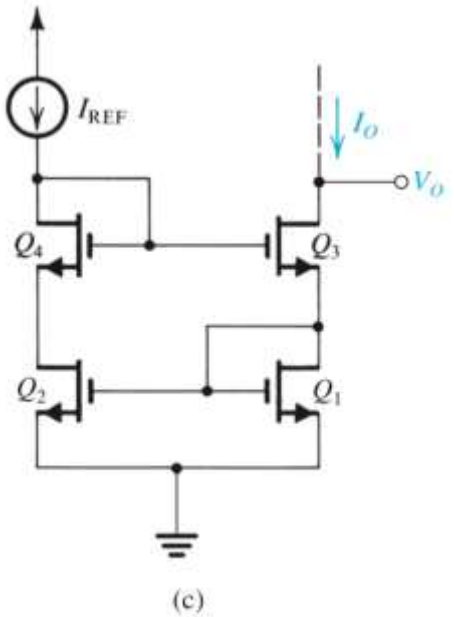
$I_o = I_{REF}$

① $$i_{d3} = g_{m3} v_{gs3}$$
$$= g_{m3}\left(v_{g3} - v_{s3}\right)$$
$$= g_{m3}\left(-i_x r_{o2} - i_x/g_{m1}\right)$$
$$\simeq -g_{m3} r_{o2} i_x$$

②流过r_{o3}的电流

$$(i_x - i_{d3}) = i_x + g_{m3} r_{o2} i_x \simeq g_{m3} r_{o2} i_x$$

③ $$v_x = g_{m3} r_{o2} i_x r_{o3} + v$$
$$= (g_{m3} r_{o3} r_{o2}) i_x + (i_x/g_{m1})$$
$$\simeq g_{m3} r_{o3} r_{o2} i_x$$



增加了对称性

$$R_o = \frac{v_x}{i_x} = (g_{m3} r_{o3}) r_{o2}$$

Widlar Current Source

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right) \tag{8.97}$$

and

$$V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right) \tag{8.98}$$

where we have assumed that Q_1 and Q_2 are matched devices. Combining Eqs. (8.97) and (8.98) gives

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \tag{8.99}$$

But from the circuit we see that

$$V_{BE1} = V_{BE2} + I_O R_E \tag{8.100}$$

Thus,

$$I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \tag{8.101}$$

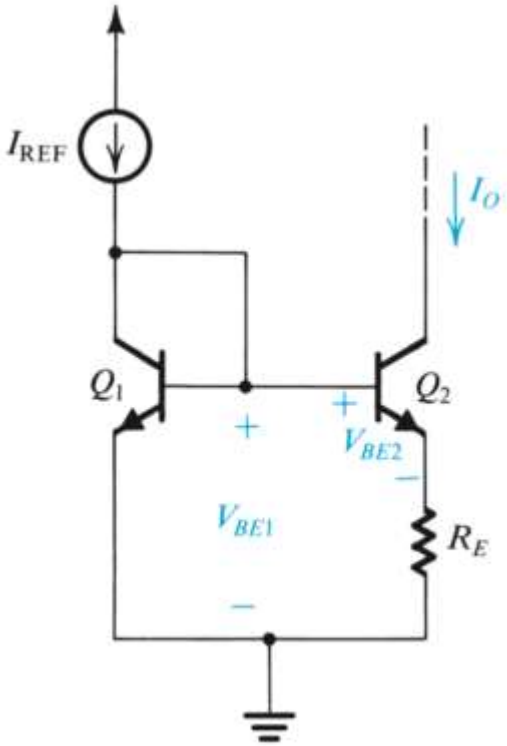


Figure 8.42 The Widlar current source.

The two circuits for generating a constant current $I_O = 10\,\mu A$ shown in Fig. 8.43 operate from a 10-V supply. Determine the values of the required resistors, assuming that V_{BE} is 0.7 V at a current of 1 mA and neglecting the effect of finite β.

Example 8.6

Solution

For the basic current-source circuit in Fig. 8.43(a) we choose a value for R_1 to result in $I_{REF} = 10\,\mu A$. At this current, the voltage drop across Q_1 will be

$$V_{BE1} = 0.7 + V_T \ln\left(\frac{10\,\mu A}{1\,mA}\right) = 0.58\ V$$

Thus,

$$R_1 = \frac{10 - 0.58}{0.01} = 942\ k\Omega$$

For the Widlar circuit in Fig. 8.43(b) we must first decide on a suitable value for I_{REF}. If we select $I_{REF} = 1$ mA, then $V_{BE1} = 0.7$ V and R_2 is given by

$$R_2 = \frac{10 - 0.7}{1} = 9.3\ k\Omega$$

The value of R_3 can be determined using Eq. (8.101) as follows:

$$10 \times 10^{-6} R_3 = 0.025 \ln\left(\frac{1\,mA}{10\,\mu A}\right)$$

$$R_3 = 11.5\ k\Omega$$

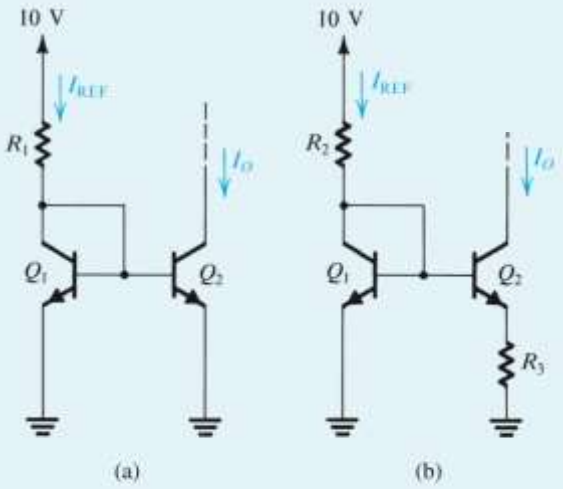


Figure 8.43 Circuits for Example 8.6.

- **Widlar 结构可用小电阻产生小电流；而基本电流镜结构产生小电流必须用大电阻；**

常用的晶体管组合：CC-CE, CD-CS, CD-CE Configurations

① CC使输入阻抗扩大（β+1）倍；
② 具有更大的带宽

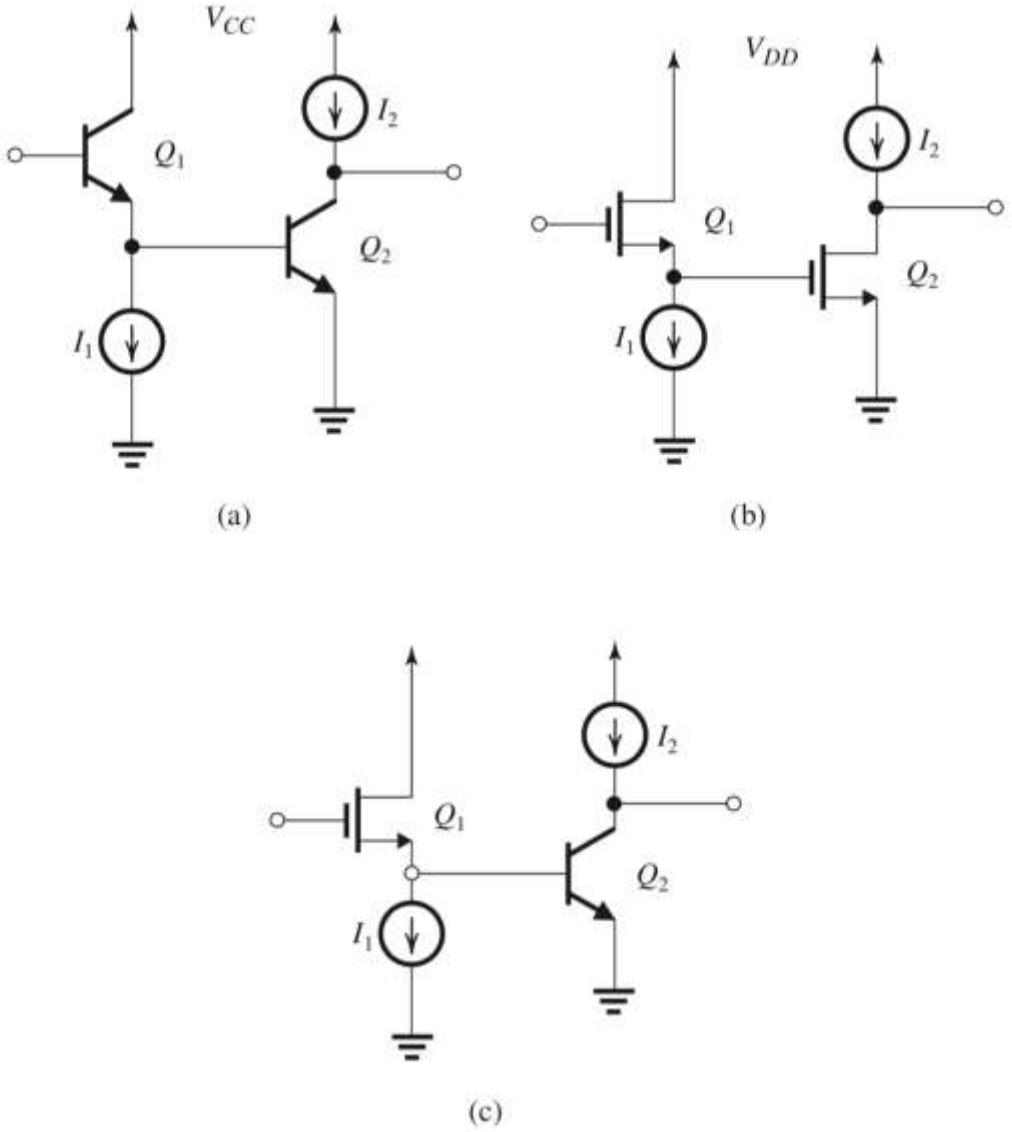
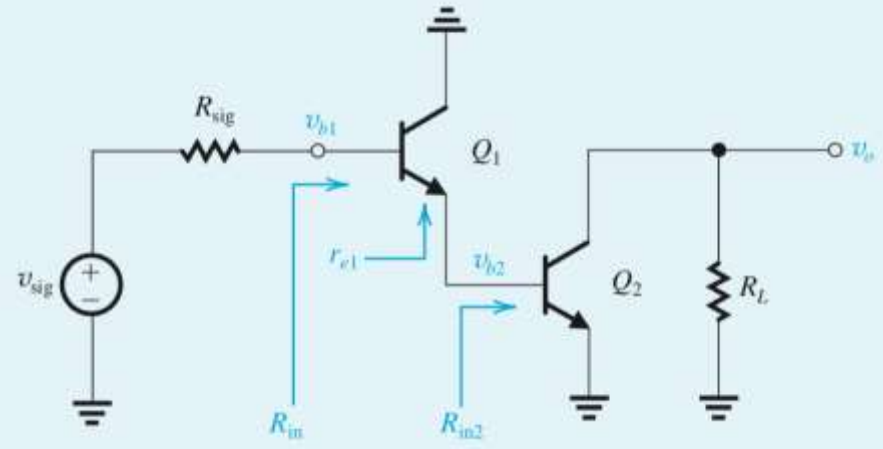


Figure 8.44 (a) CC–CE amplifier; (b) CD–CS amplifier; (c) CD–CE amplifier.

For the CC–CE amplifier in Fig. 8.44(a) let $I_1 = I_2 = 1$ mA and assume identical transistors with $\beta = 100$. Find the input resistance R_{in} and the overall voltage gain obtained when the amplifier is fed with a signal source having $R_{sig} = 4\,k\Omega$ and loaded with a resistance $R_L = 4\,k\Omega$. Compare the results with those obtained with a common-emitter amplifier operating under the same conditions. Ignore r_o.



At an emitter current of 1 mA, Q_1 and Q_2 have

$$g_m = 40\ \text{mA/V}$$

$$r_e = 25\,\Omega$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40} = 2.5\,k\Omega$$

$$R_{in2} = r_{\pi 2} = 2.5\,k\Omega$$

$$R_{in} = (\beta_1 + 1)(r_{e1} + R_{in2})$$

$$= 101(0.025 + 2.5) = 255\,k\Omega$$

$$\frac{v_{b1}}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{255}{255 + 4} = 0.98\ \text{V/V}$$

$$\frac{v_{b2}}{v_{b1}} = \frac{R_{in2}}{R_{in2} + r_{e1}} = \frac{2.5}{2.5 + 0.025} = 0.99\ \text{V/V}$$

$$\frac{v_o}{v_{b2}} = -g_{m2}R_L = -40 \times 4 = -160\ \text{V/V}$$

$$G_v = \frac{v_o}{v_{sig}} = -160 \times 0.99 \times 0.98 = -155\ \text{V/V}$$

a CE amplifier operating under the same conditions will have

$$R_{in} = r_\pi = 2.5\,k\Omega$$

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}}(-g_m R_L)$$

$$= \frac{2.5}{2.5 + 4}(-40 \times 4)$$

$$= -61.5\ \text{V/V}$$

Source Follower 的 IC 实现

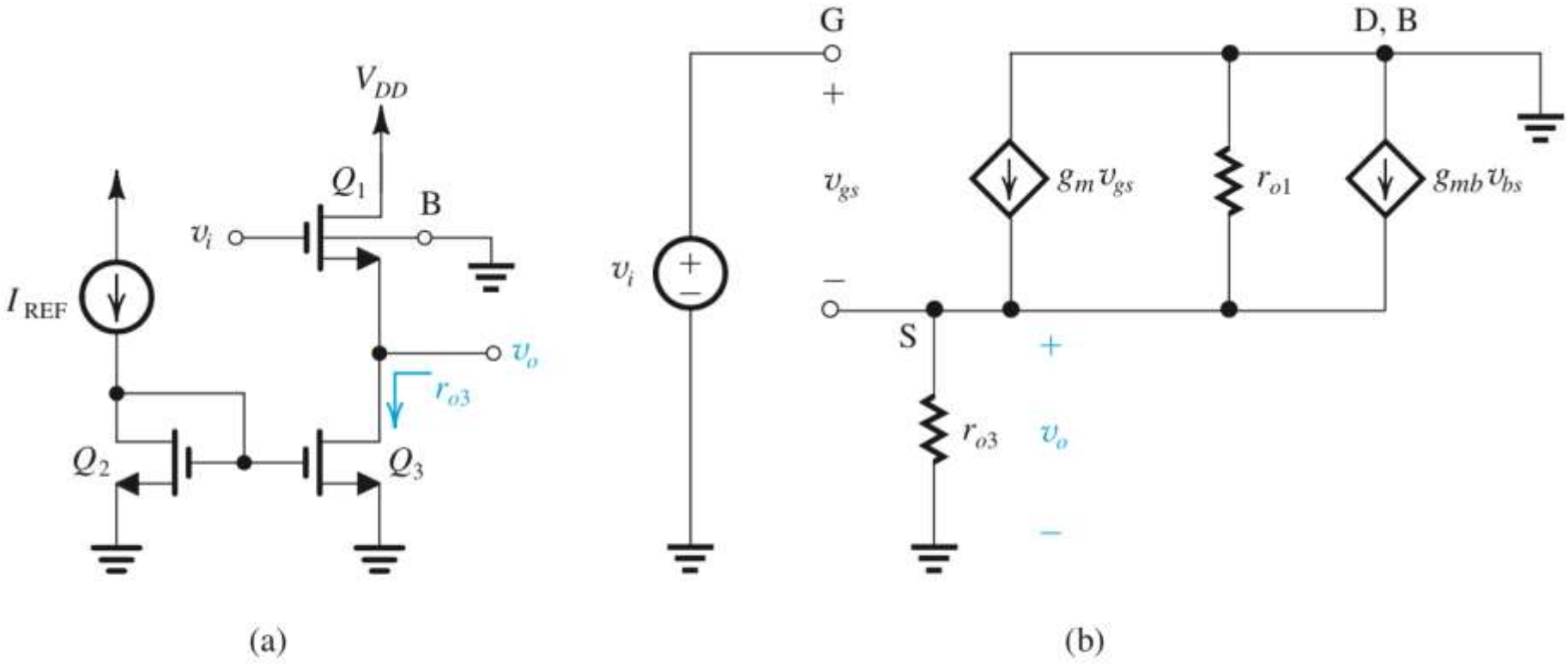
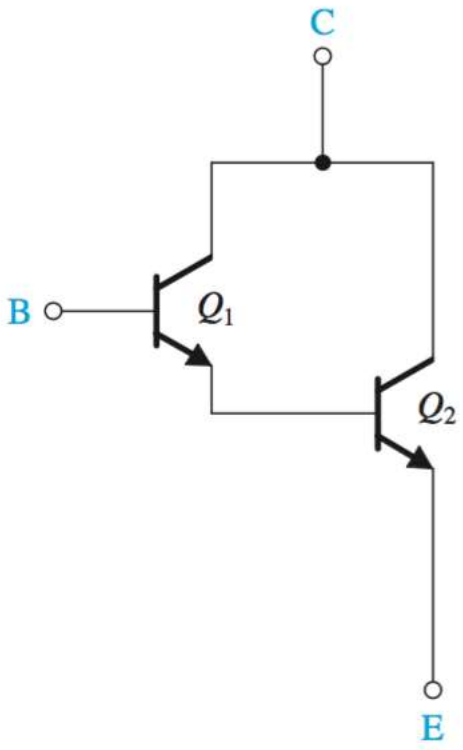
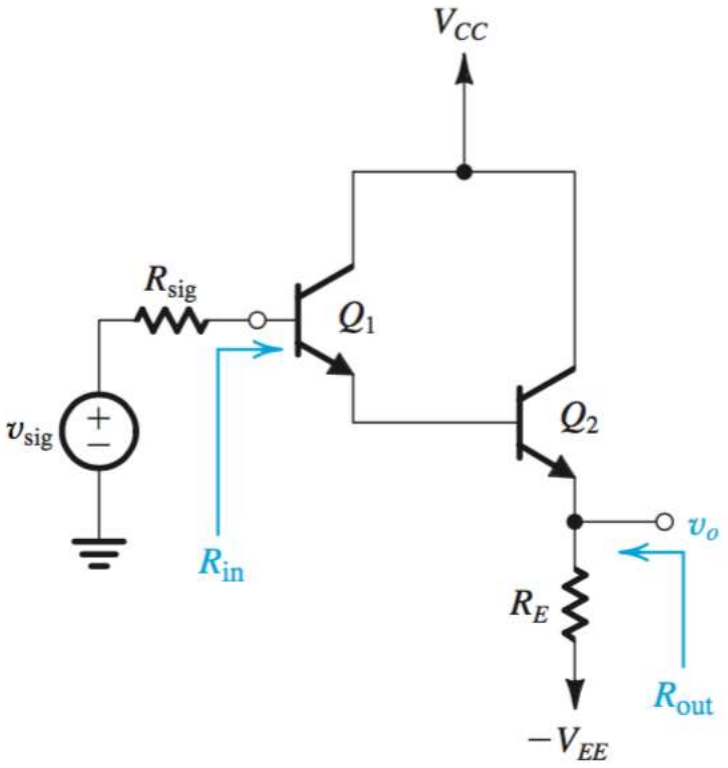


Figure 8.45 (**a**) A source follower biased with a current mirror Q_2–Q_3 and with the body terminal indicated. Note that the source cannot be connected to the body and thus the body effect should be taken into account. (**b**) Equivalent circuit.

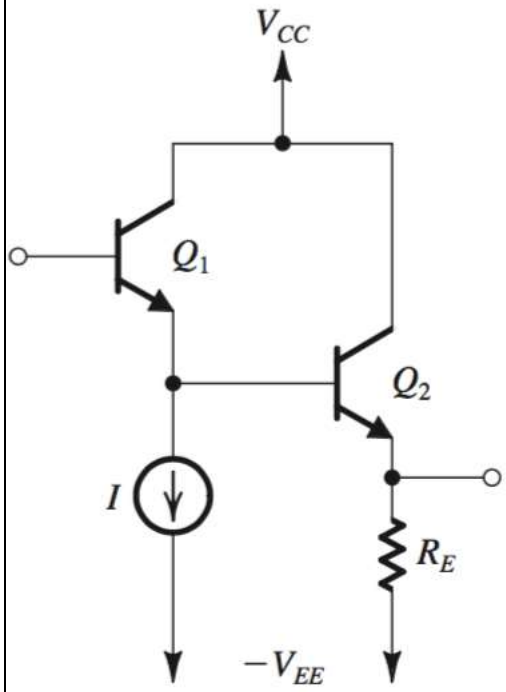
Darlington Configuration



(a)



(b)



(c)

Figure 8.47 **(a)** The Darlington c
(c) the Darlington follower with a bia

onfiguration;
.

$$R_{in} = (\beta_1 + 1)[r_{e1} + (\beta_2 + 1)(r_{e2} + R_E)]$$

$$R_{out} = R_E \| \left[r_{e2} + \frac{r_{e1} + [R_{sig}/(\beta_1 + 1)]}{\beta_2 + 1} \right]$$

$$\frac{v_o}{v_{sig}} = \frac{R_E}{R_E + r_{e2} + [r_{e1} + R_{sig}/(\beta_1 + 1)]/(\beta_2 + 1)}$$

可看成一个广义晶体管，其 $\beta=\beta_1\times\beta_2$

给Q_1单独偏置，保证β_1的值不会太小

CC-CB, CD-CG Configurations

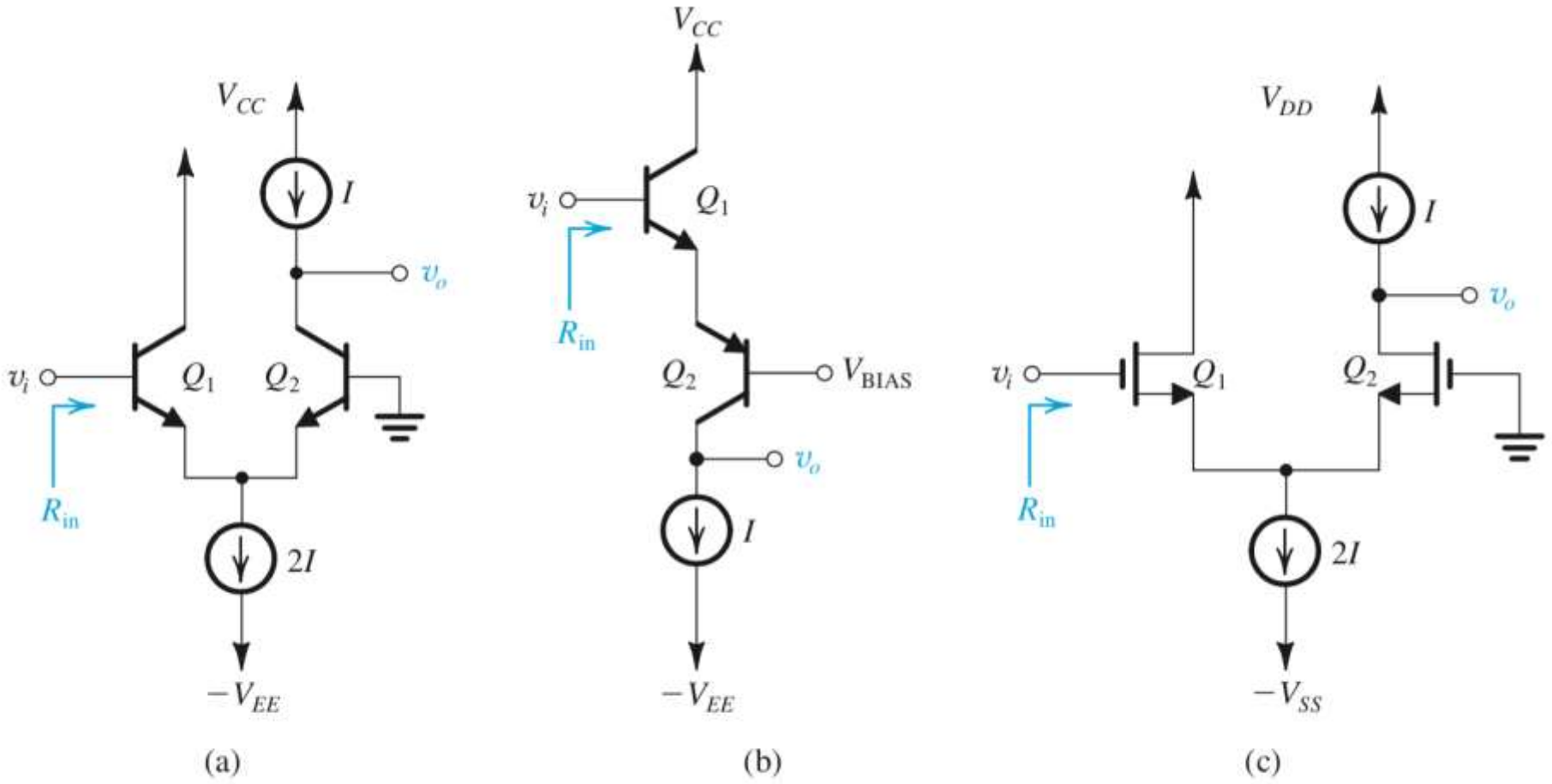
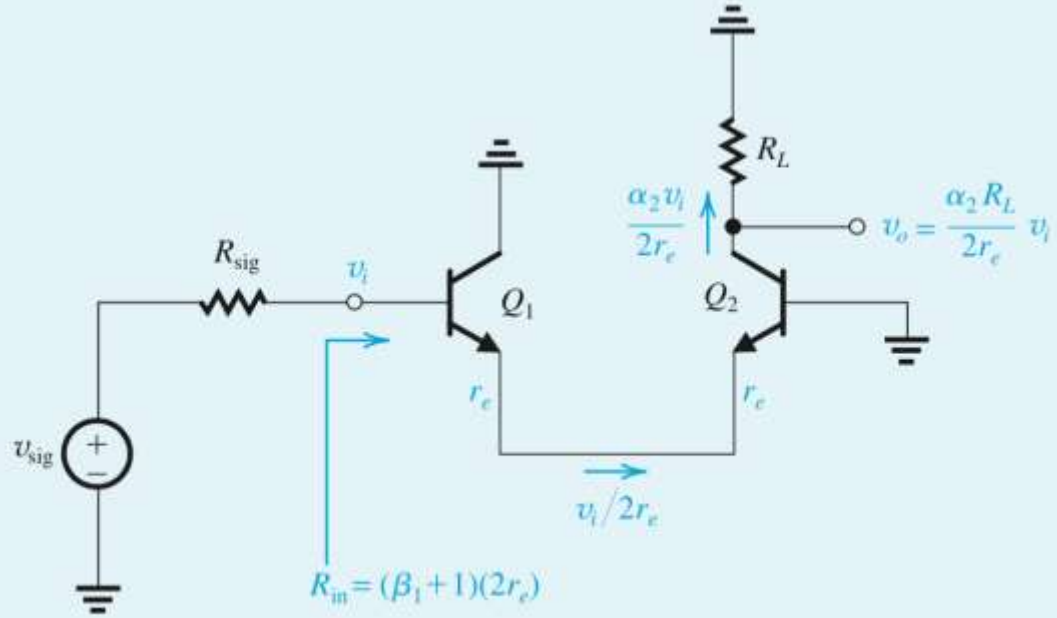


Figure 8.48 (**a**) A CC–CB amplifier. (**b**) Another version of the CC–CB circuit with Q_2 implemented using a *pnp* transistor. (**c**) The MOSFET version of the circuit in (**a**).

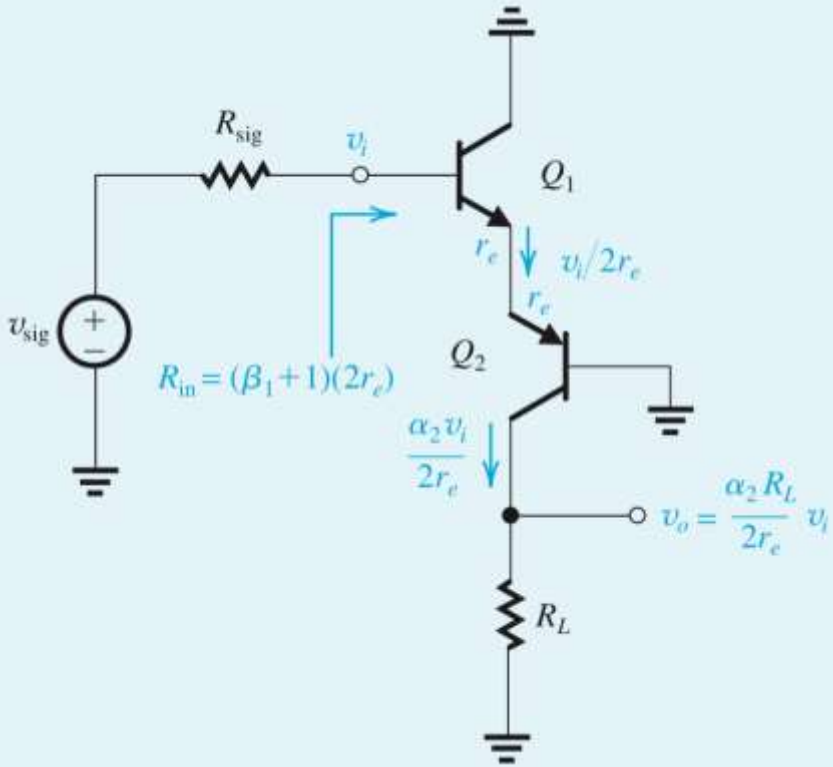
- **提供更大的输入阻抗（与CB比）；**
- **提供更大的带宽（与CE比）**

CB本身有较好的带宽特性，但缺点是输入阻抗小 → 通过前置一级CC加以解决

For the CC–CB amplifiers in Fig. 8.48(a) and (b), find R_{in}, v_o/v_i, and v_o/v_{sig} when each amplifier is fed with a signal source having a resistance R_{sig}, and a load resistance R_L is connected at the output. For simplicity, neglect r_o.



(a)

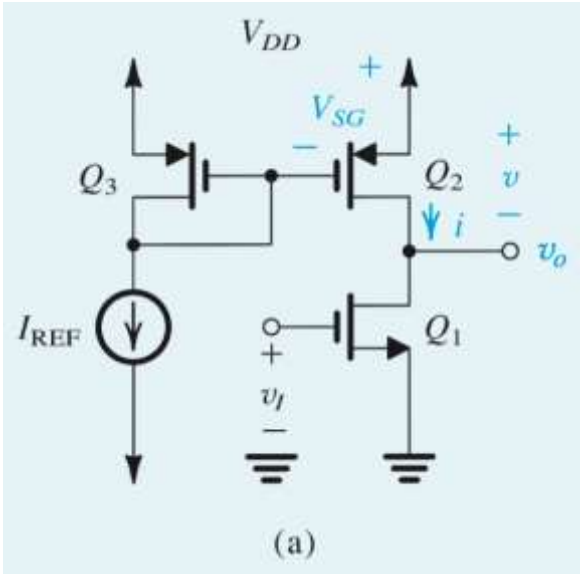


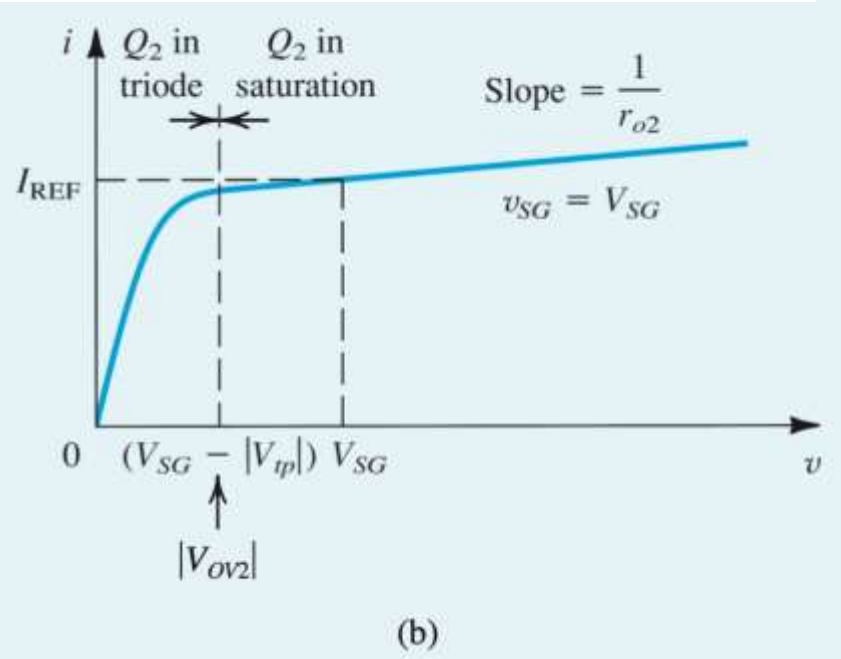
Solution

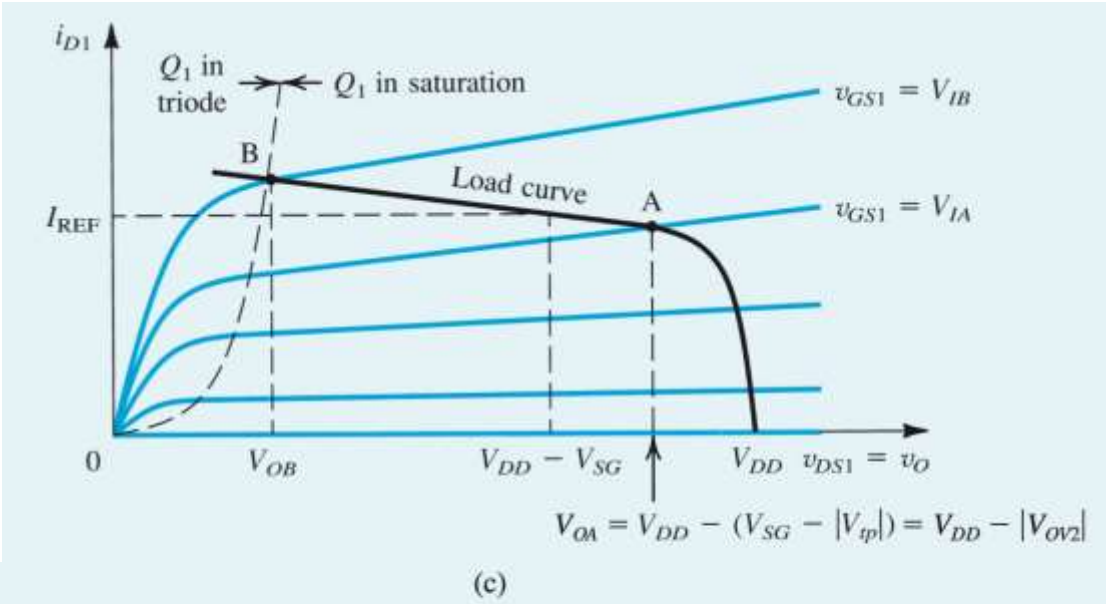
The analysis of both circuits is illustrated in Fig. 8.49. Observe that both amplifiers have the same R_{in} and v_o/v_i. The overall voltage gain v_o/v_{sig} can be found as

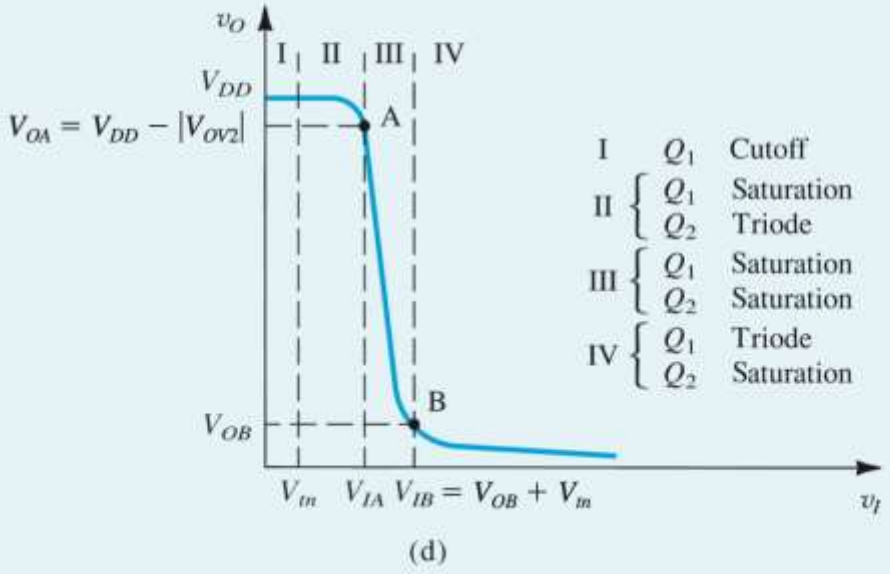
$$\frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} \frac{\alpha_2 R_L}{2r_e}$$

要保证所有管子都工作在饱和区（MOSFET） / 放大区（BJT）









小结

- 电流镜：1）Diode-connected结构；2）按比例复制；3）current source, current sink 两种形式；4）改进型结构的分析，目的1-增加输出电阻，目的2-减小β的影响
- 有源负载：用电流源替代电阻负载（IC设计中尽量少用电阻），增加内在增益，增加输出摆幅空间
- Cascode：提供大输出电阻，1）电流源应用：更好的恒流源；2）放大器应用：更大的内在增益；3）各管子都要工作在饱和区（MOSFET）/放大区（BJT），低电压供电设计时有压力
- 常用组合结构：1）Cascode是CS+CG，CG为CS提供current buffer，增加输出电阻；2）CC+CE，CC为CE增加输入电阻；3）Darlington结构，看成广义BJT， $\beta=\beta_1\times\beta_2$ 4）CD+CG，CD为CG增加输入电阻；5）CG具有优异的高频特性，其他结构与CG组合可提高带宽特性

作业

D8.2 For the circuit of Fig. 8.4, let $V_{DD} = V_{SS} = 1.5$ V, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, all channel lengths $= 1$ μm, $k_n' = 200$ μA/V^2, $k_p' = 80$ μA/V^2, and $\lambda = 0$. For $I_{REF} = 10$ μA, find the widths of all transistors to obtain $I_2 = 60$ μA, $I_3 = 20$ μA, and $I_5 = 80$ μA. It is further required that the voltage at the drain of Q_2 be allowed to go down to within 0.2 V of the negative supply and that the voltage at the drain of Q_5 be allowed to go up to within 0.2 V of the positive supply.

Ans. $W_1 = 2.5$ μm; $W_2 = 15$ μm; $W_3 = 5$ μm; $W_4 = 12.5$ μm; $W_5 = 50$ μm

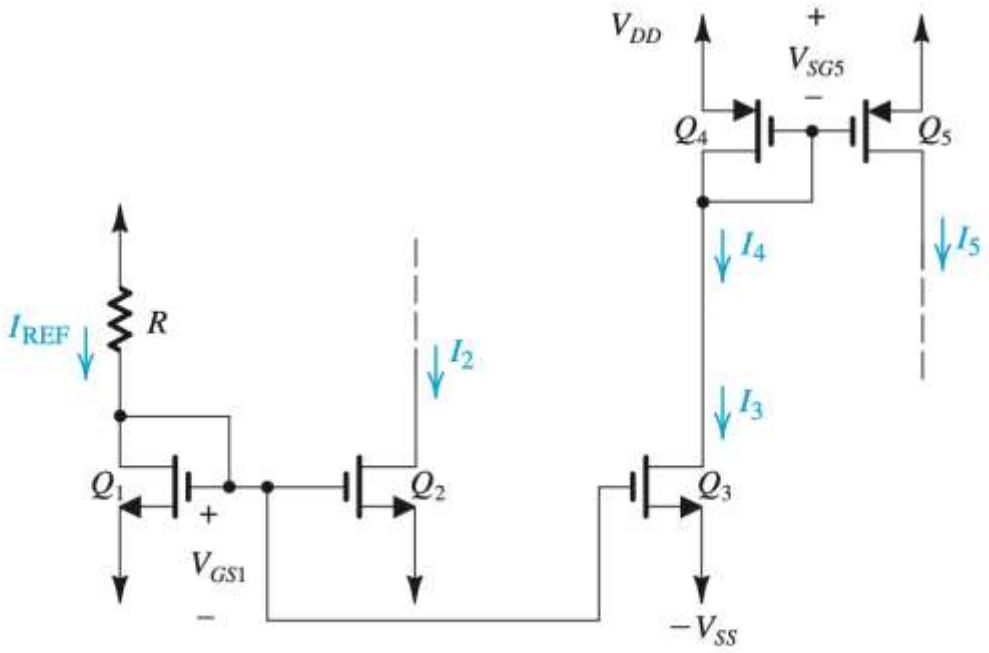


Figure 8.4 A current-steering circuit.

作业

8.5 Figure E8.5 shows an N-output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

$$I_1 = I_2 = \cdots = I_N = \frac{I_{\text{REF}}}{1 + (N+1)/\beta}$$

~~For $\beta = 100$, find the maximum number of outputs for an error not exceeding 10%.~~

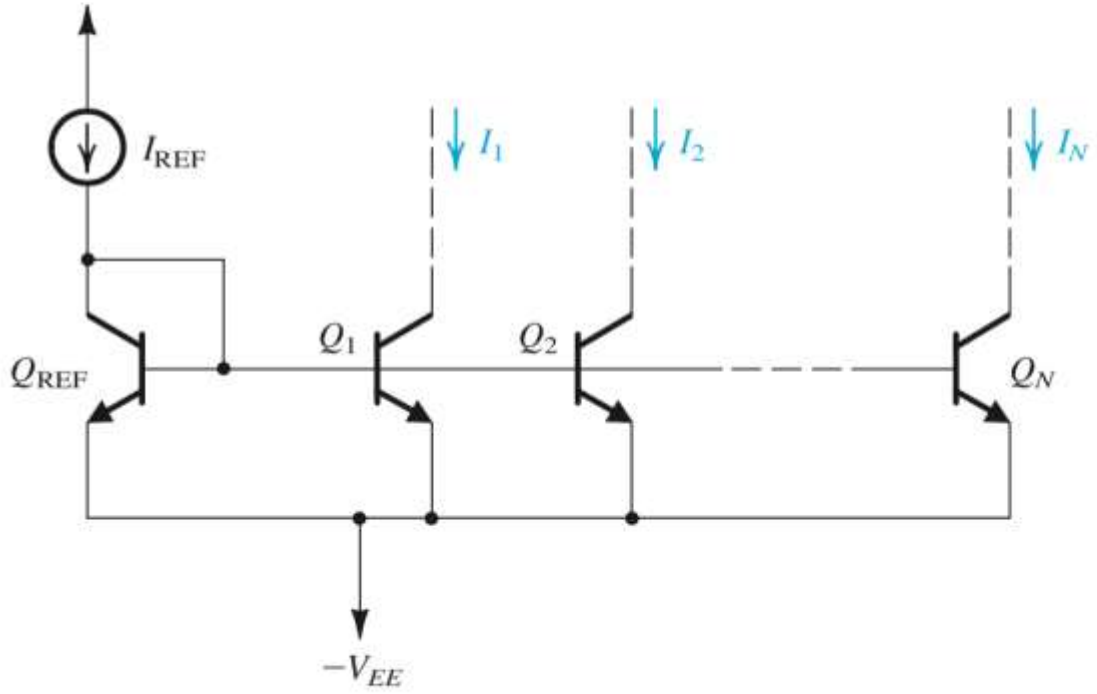
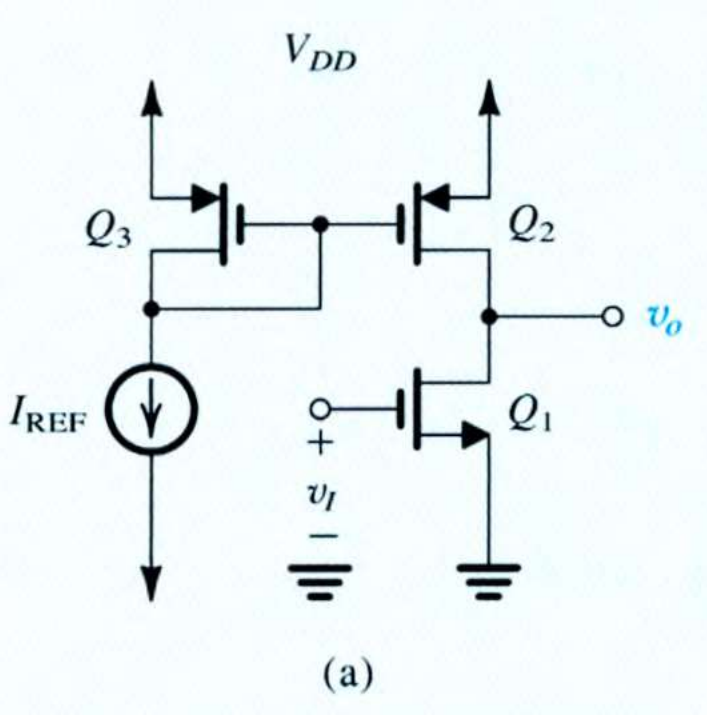


Figure E8.5

~~Ans. 9~~

8.8 A CMOS common-source amplifier such as that in Fig. 8.16(a), fabricated in a 0.18-μm technology, has $W/L = 7.2\ \mu m/0.36\ \mu m$ for all transistors, $k_n' = 387\ \mu A/V^2$, $k_p' = 86\ \mu A/V^2$, $I_{REF} = 100\ \mu A$, $V_{An}' = 5\ V/\mu m$, and $|V_{Ap}'| = 6\ V/\mu m$. Find g_{m1}, r_{o1}, r_{o2}, and the voltage gain.

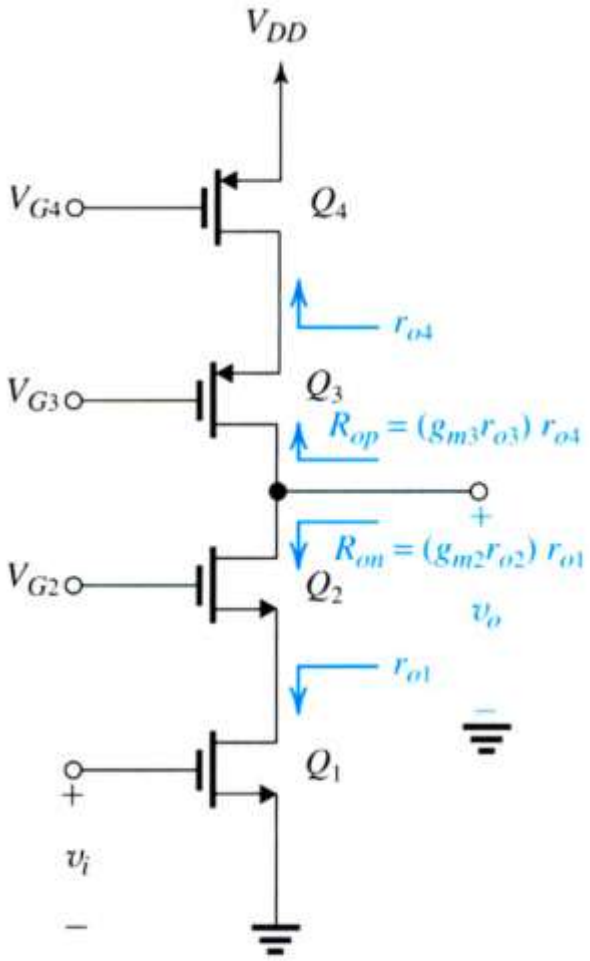
Ans. 1.24 mA/V; 18 kΩ; 21.6 kΩ; –12.2 V/V



(a)

8.20 Consider the cascode amplifier of Fig. 8.31 with the dc component at the input, $V_I = 0.7$ V, $V_{G2} = 1.0$ V, $V_{G3} = 0.8$ V, $V_{G4} = 1.1$ V, and $V_{DD} = 1.8$ V. If all devices are matched (i.e., if $k_{n1} = k_{n2} = k_{p3} = k_{p4}$), and have equal $|V_t|$ of 0.5 V, what is the overdrive voltage at which the four transistors are operating? What is the allowable voltage range at the output?

Ans. 0.2 V; 0.5 V to 1.3 V



(a)