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Chapter #2:
Operational Amplifiers
运算放大器 part1

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课程纲要

- 14.1 运算放大器的理想模型
- 14.2 运算放大器基本应用电路的设计分析
- 14.2.1 倒相和同相接法电路的分析
- 14.2.2 主要应用电路分析（包括加法电路、差分放大电路、仪表放大电路、积分电路、微分电路，以及单限和双限电压比较器，有源滤波器）
- 14.3 运算放大器性能参数及其对电路的影响
- 14.3.1 有限开环增益的影响
- 14.3.2 直流误差（输入失调电压和输入失调电流）
- 14.4 运算放大器的大信号分析（包括输出饱和、摆率和满功率带宽等基本概念）
- 14.5 典型运放内部电路结构及其分析（介绍741运放内部电路，包括电路结构、直流分析、交流分析和电路保护原理，不讲解具体定量计算过程）

Introduction

- **IN THIS CHAPTER YOU WILL LEARN**
  - The terminal characteristics of the ideal op-amp.理想运放的基本特性
  - How to analyze circuits containing op-amps, resistors, and capacitors. 基本运放电路的分析
  - How to use op-amps to design amplifiers having precise characteristics. 利用运放设计精确放大器

Introduction

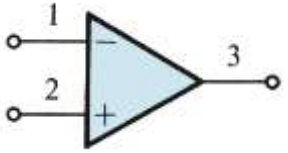
- **IN THIS CHAPTER YOU WILL LEARN**
  - How to design more sophisticated op-amp circuits, including summing amplifiers, instrumentation amplifiers, integrators, and differentiators.

    运放主要应用电路分析

2.1.1. The Op Amp Terminals

从信号角度讲，op amp 是一个三端元件（1、2、3），4和5是供电。

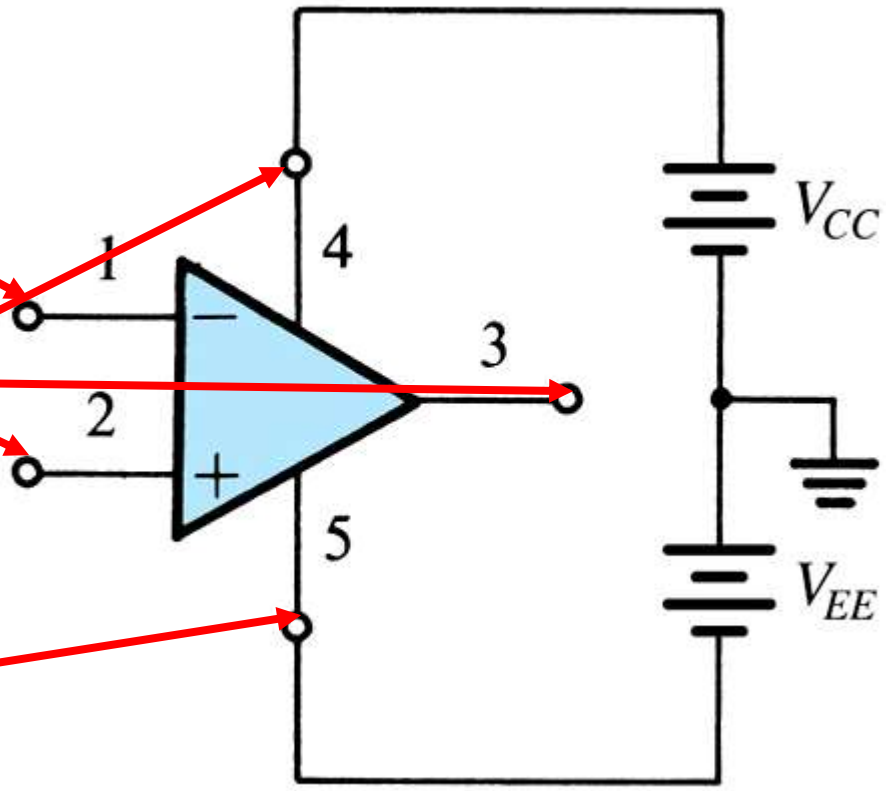
供电一般不画出



“电压电流约束关系”：

$$v_3 = A(v_2 - v_1)$$

- **terminal #1** 反相输入端
  - inverting input
- **terminal #2** 同相输入端
  - non-inverting input
- **terminal #3** 输出端
  - output
- **terminal #4** 供电电源（+）
  - positive supply V_{CC}
- **terminal #5** 供电电源（-）
  - negative supply V_{EE}



Op amp 也是一个基本的 building block，就如R、L、C

2.1 What is the minimum number of terminals required by a single op amp? What is the minimum number of terminals required on an integrated-circuit package containing four op amps (called a quad op amp)?

Ans. 5; 14

意思是供电可以共用

2.1.3. Differential & Common-Mode Signals

差分信号 & 共模信号

差分：$v_{di} = v_2 - v_1$
共模：$v_{cmi} = (v_2 + v_1)/2$

- **Q:** How is common-mode input (v_{cmi}) defined in terms of v_1 and v_2?

common-mode input

$$v_{cmi} = \frac{1}{2}(v_1 + v_2)$$

but also...

inverting input

$$v_1 = v_{cmi} - v_{di}/2$$

diff

$$v_2 = v_{cmi} + v_{di}/2$$

non-inverting input

任意两个信号v_1，v_2，都可以分解成共模信号（v_{cmi}）与差分信号（V_{di}）的叠加

common-mode input

$$v_{cmi} = \frac{1}{2}(v_1 + v_2)$$

but also...

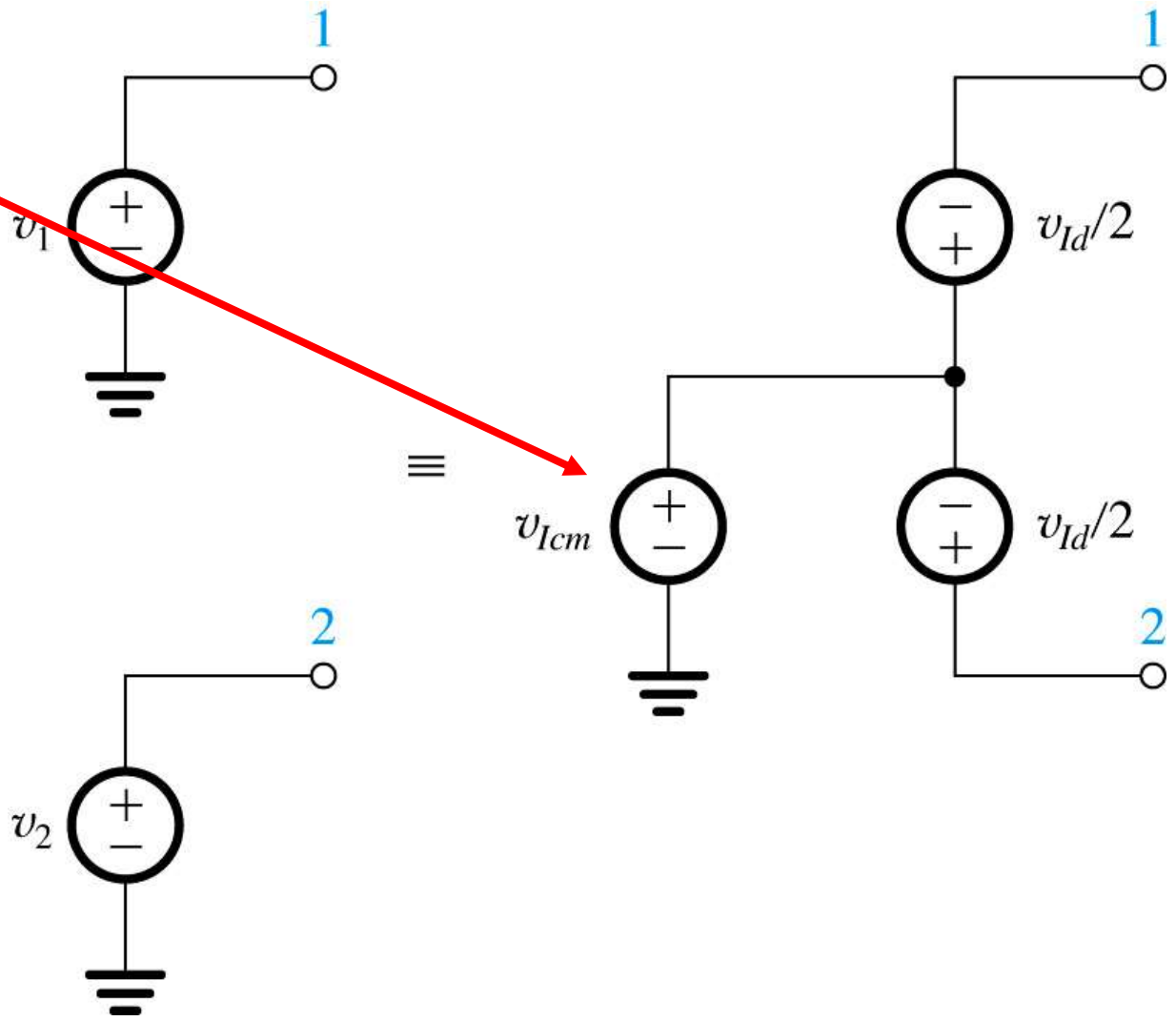
inverting input

$$v_1 = v_{cmi} - v_{di}/2$$

diff

$$v_2 = v_{cmi} + v_{di}/2$$

non-inverting input



理想运放的特性

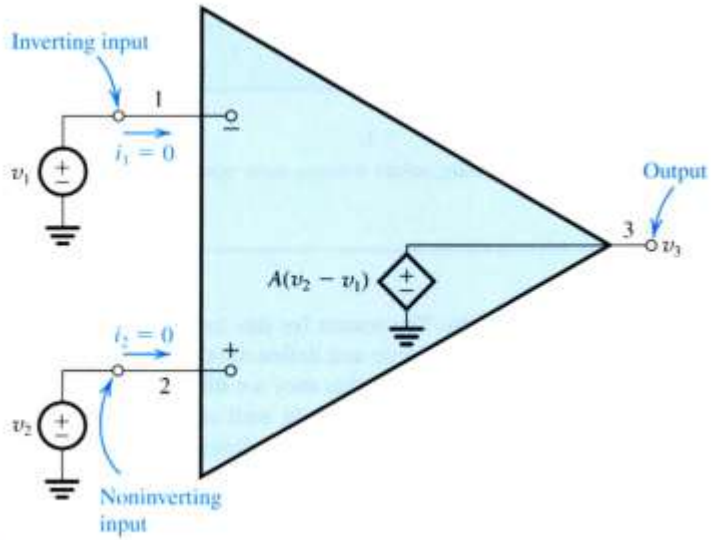


Figure 2.3 Equivalent circuit of the ideal op amp.

了解**理想运放**的基本特性，就如需要了解RLC元件的基本特性一样

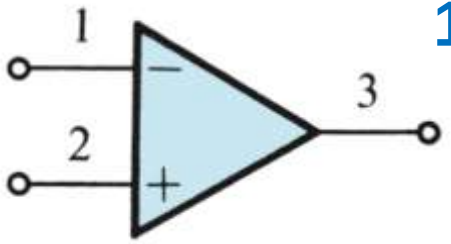
1. 电压关系： $v_3 = A(v_2 - v_1)$
2. 电流关系： $i_1 = i_2 = 0$

- ideal input characteristic is infinite impedance 输入阻抗=∞
- ideal output characteristic is zero impedance 输出阻抗=0
- differential gain (*A*) is infinite 差分电压增益=∞
- common mode gain is zero 共模电压增益=0
- bandwidth gain is constant from dc to high frequencies 带宽= ∞ 因为不考虑

理想运放不单独使用，输入输出需构成闭环再应用，所以A也称为开环增益（open-loop gain），相应的，构成闭环后的增益成为闭环增益（closed-loop gain）

Q: But, is an amplifier with infinite gain of any use?

简化 symbol，常用



$$v_3 = A(v_2 - v_1)$$

2.2 Consider an op amp that is ideal except that its open-loop gain $A = 10^3$. The op amp is used in a feedback circuit, and the voltages appearing at two of its three signal terminals are measured. In each of the following cases, use the measured values to find the expected value of the voltage at the third terminal. Also give the differential and common-mode input signals in each case. (a) $v_2 = 0$ V and $v_3 = 2$ V; (b) $v_2 = +5$ V and $v_3 = -10$ V; (c) $v_1 = 1.002$ V and $v_2 = 0.998$ V; (d) $v_1 = -3.6$ V and $v_3 = -3.6$ V.

Ans. (a) $v_1 = -0.002$ V, $v_{Id} = 2$ mV, $v_{Icm} = -1$ mV; (b) $v_1 = +5.01$ V, $v_{Id} = -10$ mV, $v_{Icm} = 5.005 \simeq 5$ V; (c) $v_3 = -4$ V, $v_{Id} = -4$ mV, $v_{Icm} = 1$ V; (d) $v_2 = -3.6036$ V, $v_{Id} = -3.6$ mV, $v_{Icm} \simeq -3.6$ V

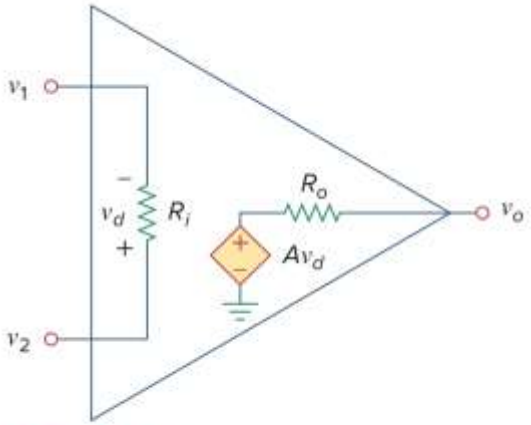


Figure 5.4
The equivalent circuit of the nonideal op amp.

理想运放的特性：

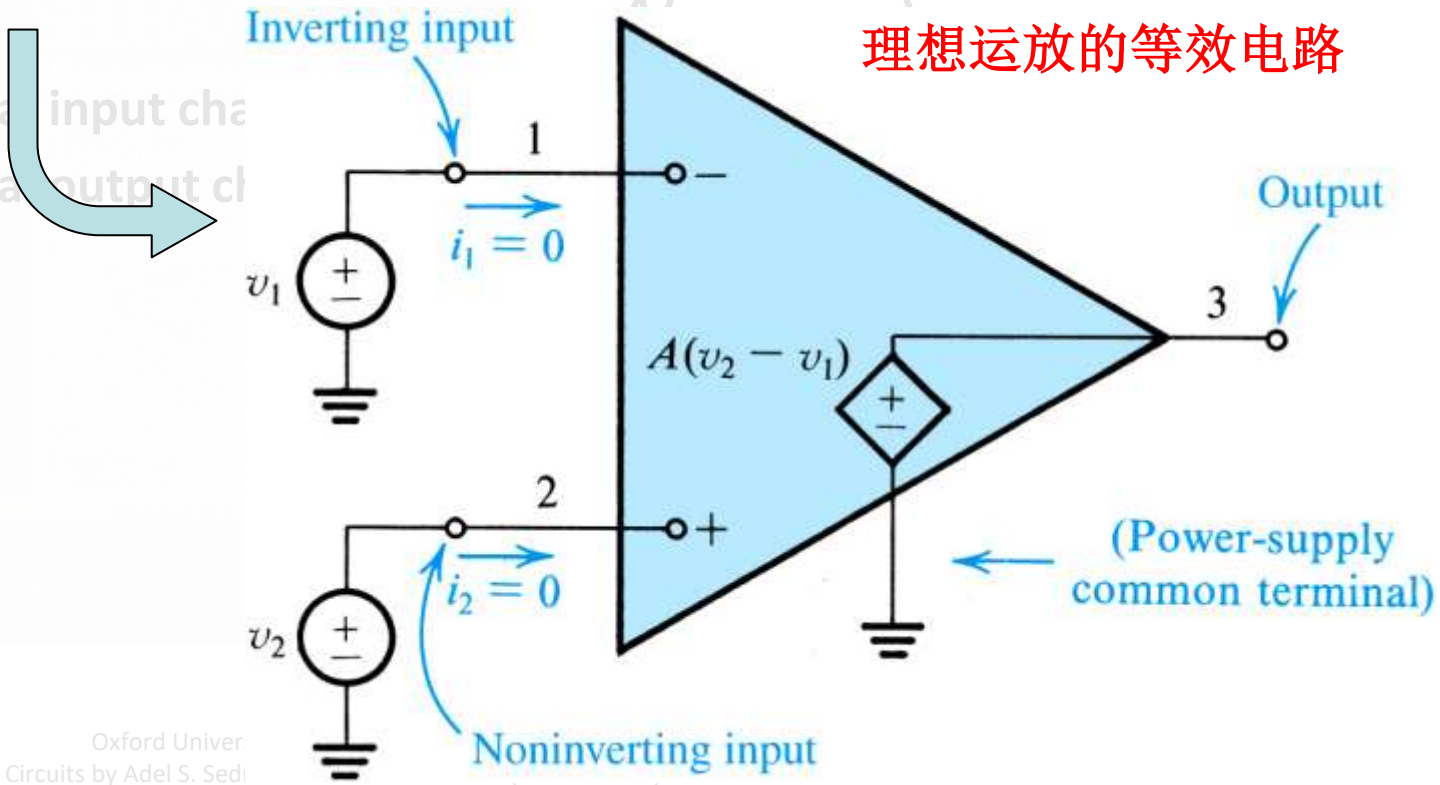
①输入阻抗=∞； → $i_1=i_2=0$ 虚断

②输出阻抗=0；

③只放大输入差分信号；

④差分电压增益=∞； → $v_1=v_2$ 虚短

⑤带宽=∞



理想运放的等效电路

2.1.2. Function and Characteristics of Ideal Op-Amp

运放的特性：
抑制共模信号、放大差分信号

- An amplifier's input is composed of two components…
  - **differential input** (v_{dfi}) – is difference between inputs at non-inverting and inverting terminals
  - **common-mode input** (v_{cmi}) – is input present at both inverting and non-inverting terminals
- Similarly, two components of gain exist…
  - **differential gain** (A) – gain applied to differential input ONLY
  - **common-mode gain** (A_{cm}) – gain applied to common-mode input ONLY

线性叠加原理

运放的增益也可看成两部分构成：差分增益+共模增益

$$v_O = A_d v_{Id} + A_{cm} v_{Icm}$$

2.1.2. Function and Characteristics of Ideal Op Amp

理想运放可以用集成运放（集成电路，而非分立元件实现运放）来近似实现

- This “Ideal” is only approached by IC op amps
- Z_i – usually high enough to ignore 输入阻抗往往够高 ∞
- Z_o – often higher than needed – follow by a low output impedance stage (emitter-follower) 输出阻抗往往不够低，需后接一级低输出阻抗的电路 0
- A_{cm} – usually quite good 共模增益往往够小 0
- A – usually high enough when not asking for too much gain with feedback 差分增益往往够高 ∞
- BW – needs to be evaluated in use. 需根据实际情况估算，≠∞ ∞

2.2. The Inverting Configuration

反相（倒相）接法

- **Q:** What are two basic closed-loop op-amp configurations which employ op-amp and resistors alone?
  - **A:** 1) inverting and 2) non-inverting op amp

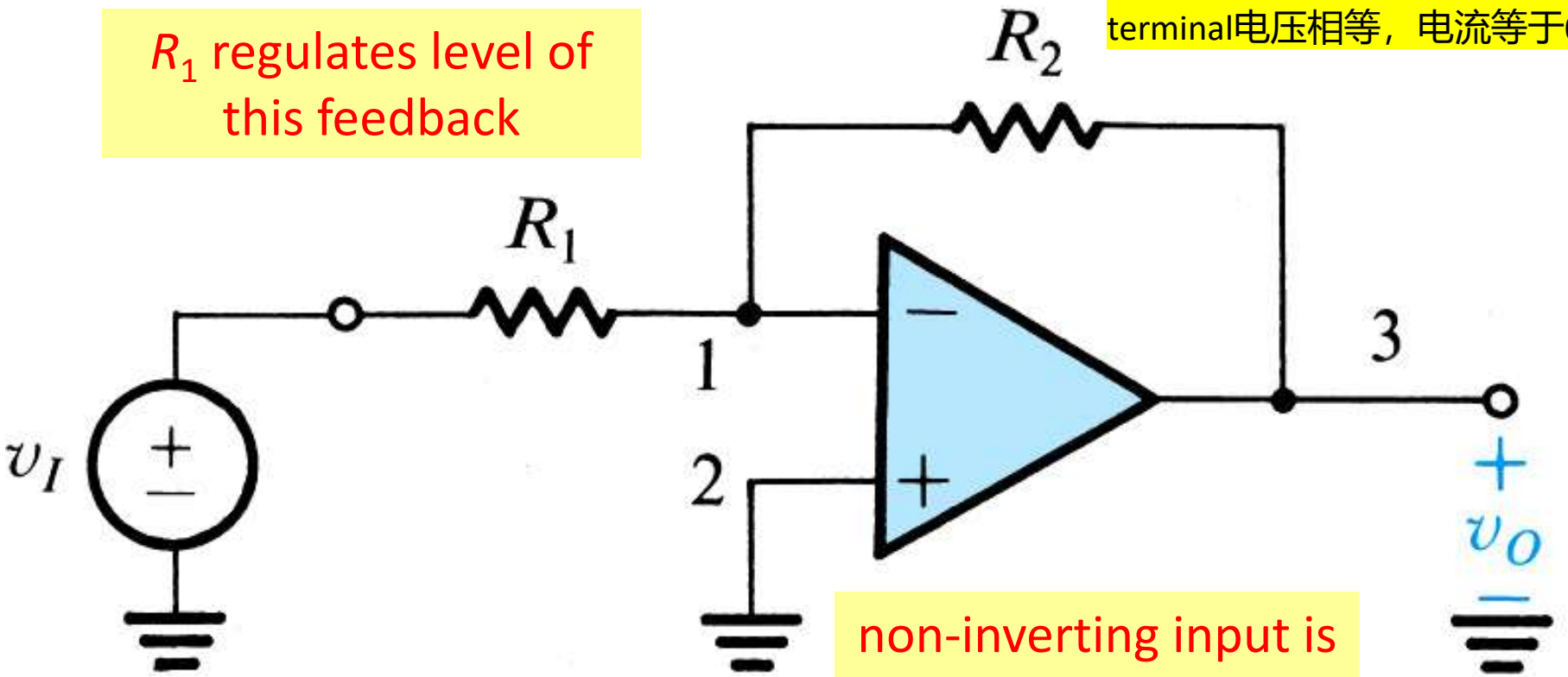
若仅可使用运放和电阻，那么有两种构成闭环的接法：①反相接法，输入在反相输入端；②同相接法，输入在同相输入端

Figure 2.5: The inverting closed-loop configuration.

R_2 facilitates "negative feedback"

terminal电压相等，电流等于0

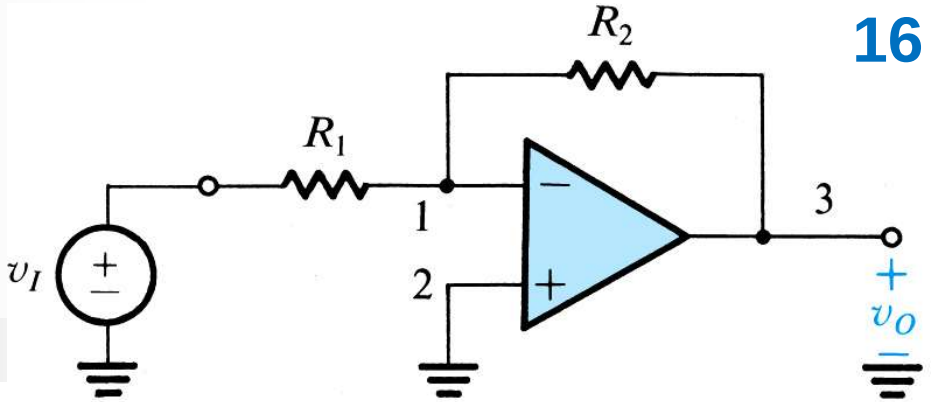
R_1 regulates level of this feedback



non-inverting input is grounded

source is applied to inverting input

2.2.1. Closed-Loop Gain



- **Q:** How does one analyze closed-loop gain for inverting configuration of an ideal op-amp?
  - **step #1: Begin at the output terminal**
  - **step #2: If v_{Out} is finite, then differential input must equal 0**
    - virtual short circuit between v_1 and v_2 1 和 2 之间电压相等，但实际物理上没有连接 → “虚短”
    - virtual ground exists at v_1 2的电压碰巧是0V，所以1称为“虚拟地”

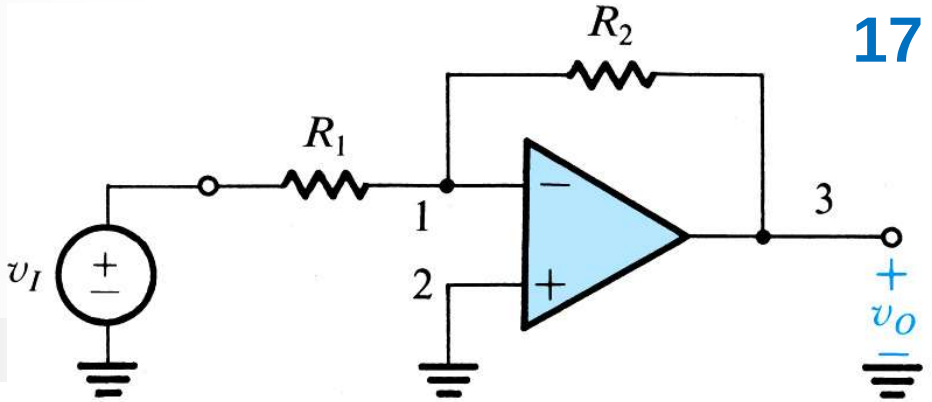
关键点：因为输出电压为有限值，所以输入必须为零（增益A为∞），也即 $v_2 = v_1$

because A in infinite

$$v_2 - v_1 = \frac{v_{Out}}{A} = 0$$

$A \to \infty$

2.2.1. Closed-Loop Gain

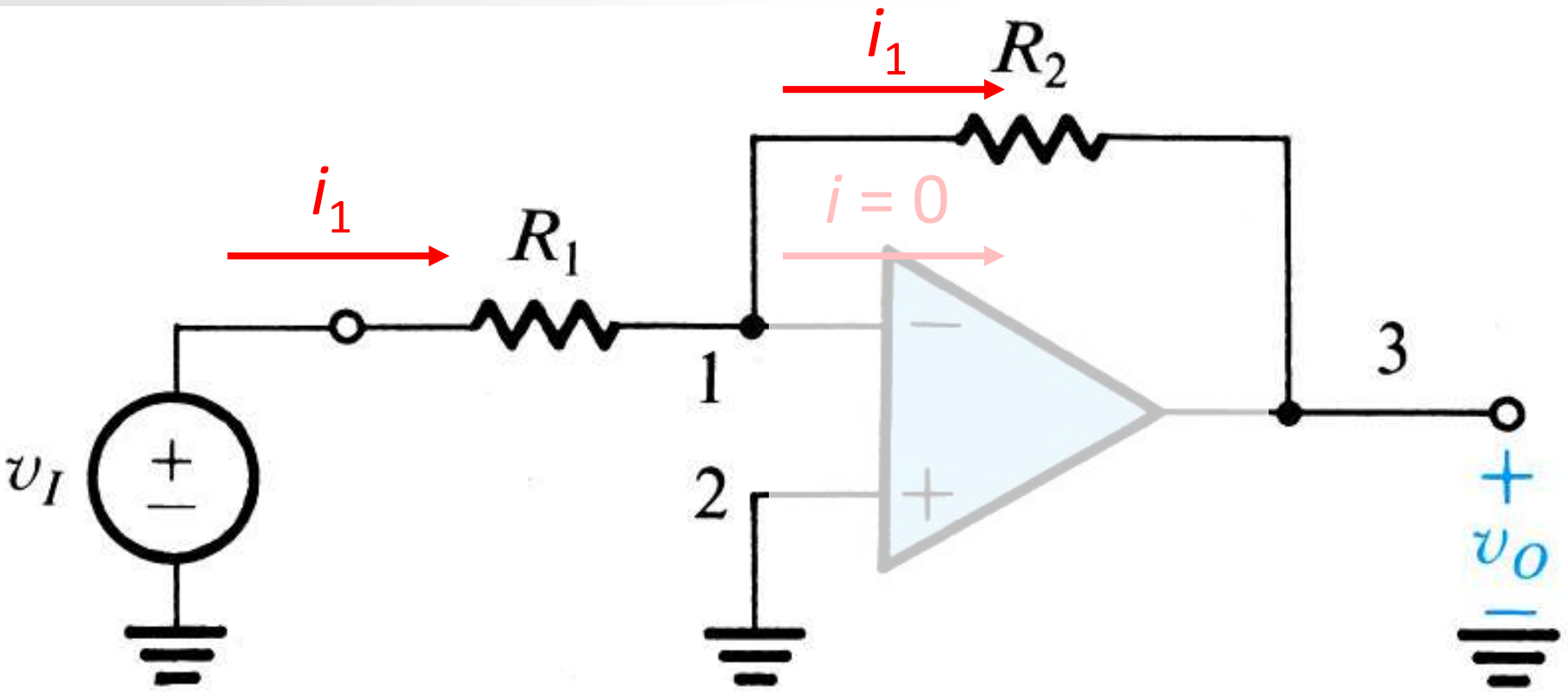


- **step #3:** Define current into inverting input (i_1).
- **step #4:** Determine where this current flows?
  - refer to following slide…

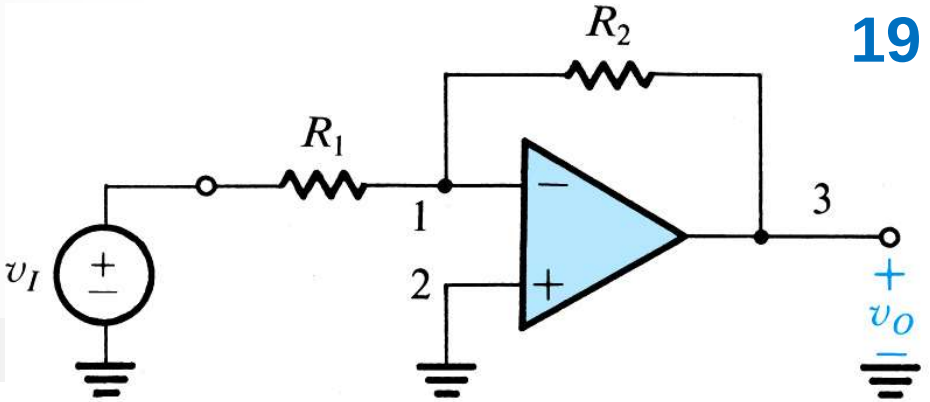
virtual ground

$$i_1 = \frac{(v_{In}) - (v_1)}{R_1} = \frac{v_{In} - 0}{R_1} = \frac{v_{In}}{R_1}$$

Figure 2.5: The inverting closed-loop configuration.



2.2.1. Closed-Loop Gain



- **step #5:** Define v_{Out} in terms of current flowing across R_2.
- **step #6:** Substitute v_{in} / R_1 for i_1.

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

virtual ground

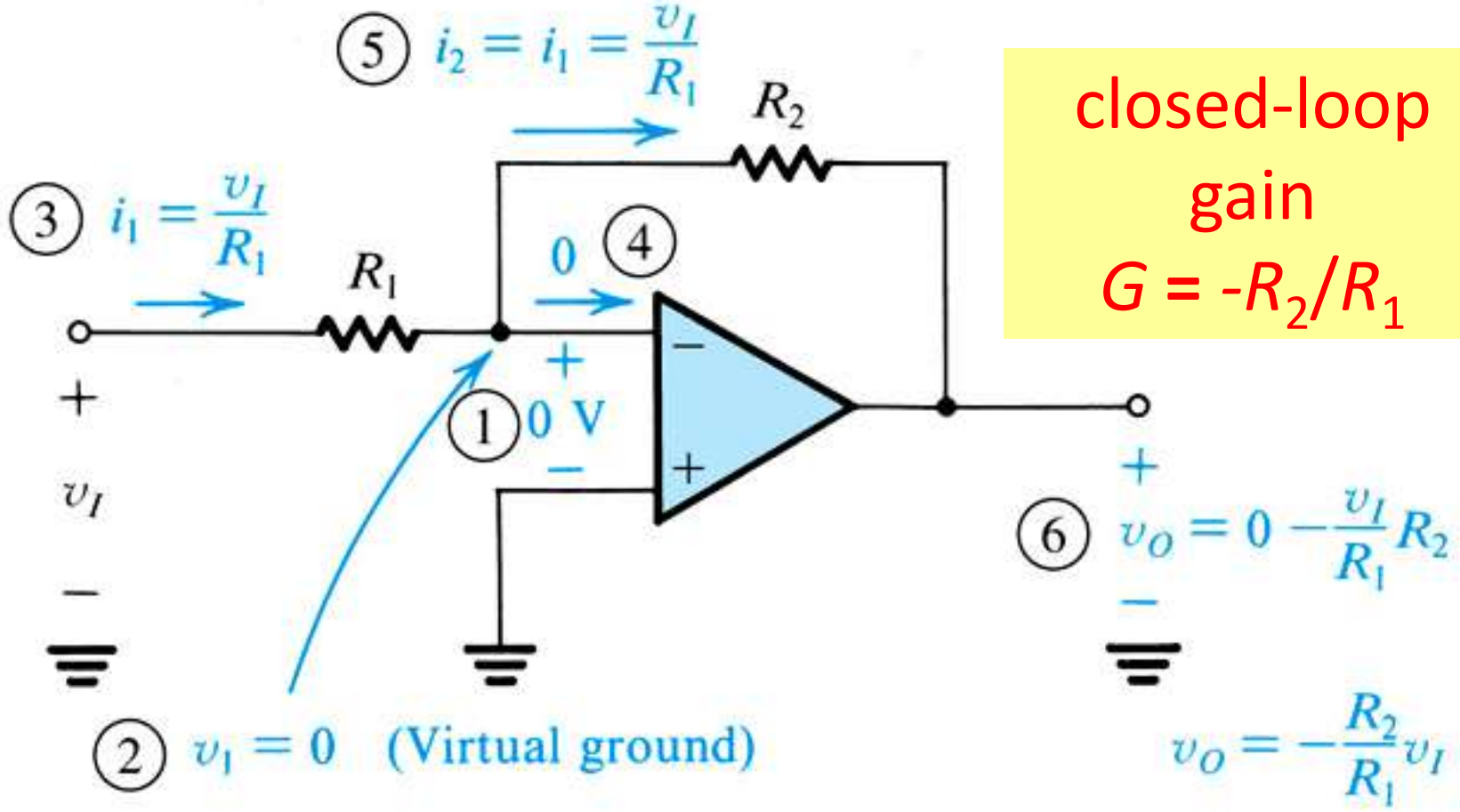
$$v_{Out} = (v_1) - (i_1 R_2) = -i_1 R_2$$

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}$$

solution

note: this expression is one of the fundamentals of electronics

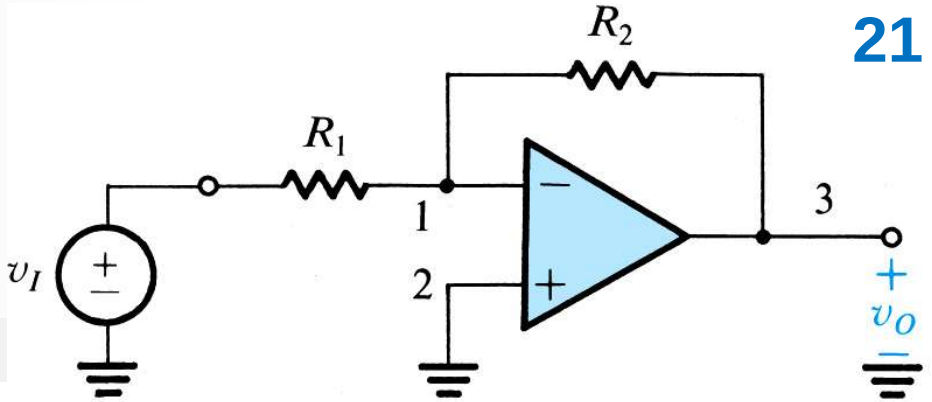
Figure 2.6: Analysis of the inverting configuration. The circled numbers indicate the order of the analysis steps.



closed-loop gain

$G = -R_2/R_1$

2.2.1. Effect of Finite Open-Loop Gain



若开环增益A≠∞，如何计算？

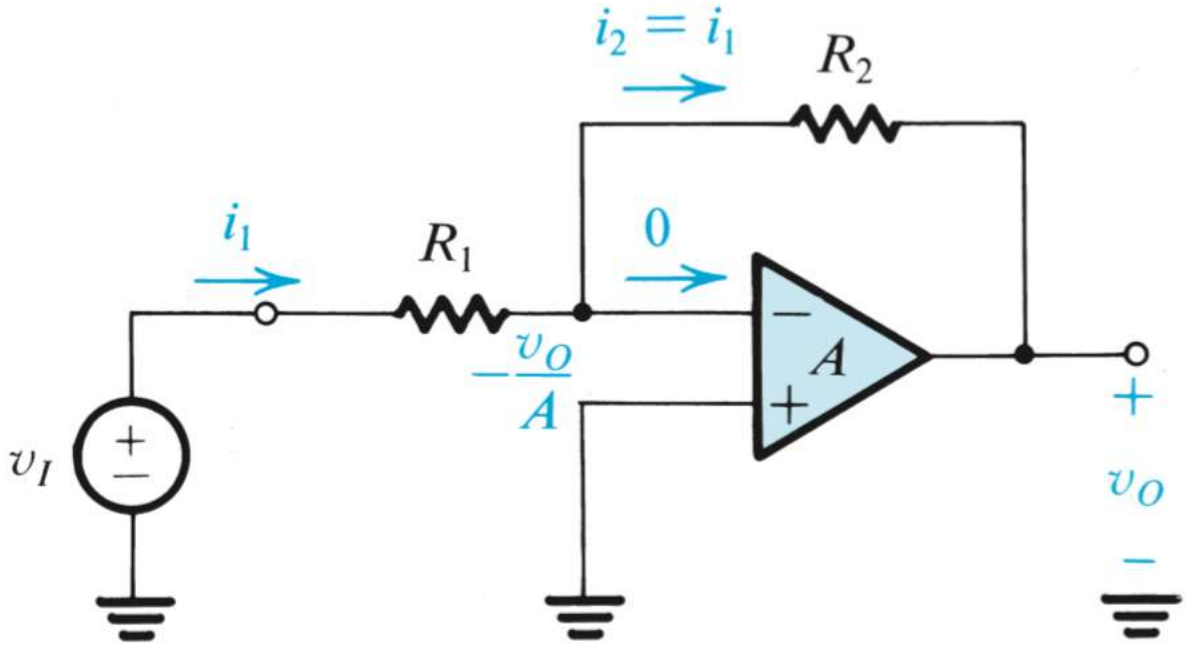
- **Q:** How does the gain expression change if open loop gain (*A*) is not assumed to be infinite?
  - **A:** One must employ analysis similar to the previous, result is presented below…

$$G_{A<\infty} = \frac{v_{Out}}{v_{In}} = \underbrace{\frac{-R_2/R_1}{1+\left(\frac{1+(R_2/R_1)}{A}\right)}}_{G_{A=\infty}} \neq -\frac{R_2}{R_1}$$

if $A=\infty$ then the previous gain expression is yielded

non-ideal gain

ideal gain



$$i_1 = \frac{v_I - (-v_O/A)}{R_1} = \frac{v_I + v_O/A}{R_1}$$

$$v_O = -\frac{v_O}{A} - i_1 R_2$$

$$= -\frac{v_O}{A} - \left(\frac{v_I + v_O/A}{R_1}\right) R_2$$

$$G \equiv \frac{v_O}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

2.2.1. Effect of Finite Open-Loop Gain

$$G_{A<\infty} = \frac{v_{Out}}{v_{In}} = \underbrace{\frac{-R_2/R_1}{1+\left(\frac{1+(R_2/R_1)}{A}\right)}}_{\text{if } A=\infty \text{ then the previous gain expression is yielded}} \neq -\frac{R_2}{R_1}$$

$G_{A=\infty}$

什么条件下G可近似等于 $-R_2/R_1$？

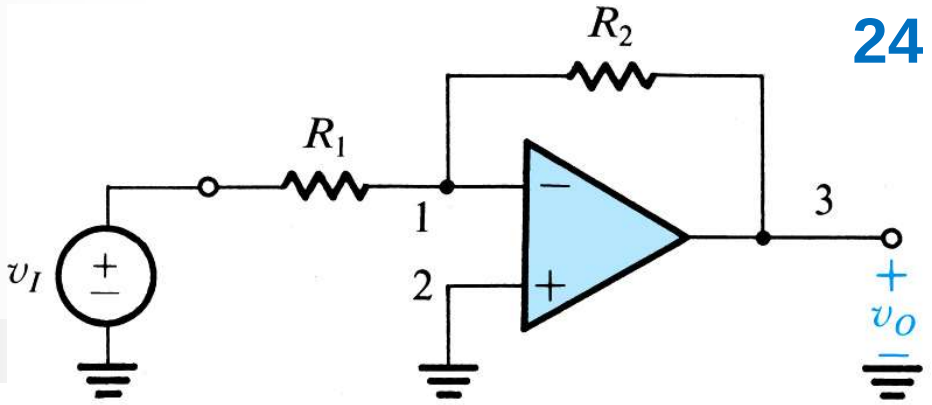
- **Q:** Under what condition can $G = -R_2 / R_1$ be employed over the more complex expression?
  - **A:** If $1 + (R_2/R_1) << A$, then simpler expression may be used.

$$\text{if } 1+\frac{R_2}{R_1} << A \text{ then } G_{A=\infty} = -\frac{R_2}{R_1} \text{ else } G_{A<\infty} = \frac{-R_2/R_1}{1+\left(\frac{1+(R_2/R_1)}{A}\right)}$$

ideal gain

non-ideal gain

Example 2.1: Simple Inverting Amplifier



- **Problem Statement:** Consider an inverting configuration with R_1 = 1*kOhm* and R_2 = 100*kOhm*.
- **Q(a):** Find the closed-loop gain (*G*) for the cases below. In each case, determine the percentage error in the magnitude of *G* relative to the ideal value.
  - cases are $A = 10^3, 10^4, 10^5$…
  - What is the voltage v_1 that appears at the inverting input terminal when v_{In} = 0.1*V*.
- **Q(b):** If the open loop gain (*A*) changes from 100*k* to 50*k*, what is percentage change in gain (*G*)?

$$G \equiv \frac{v_O}{v_I} = \frac{-R_2/R_1}{1+(1+R_2/R_1)/A} \tag{2.5}$$

Solution

(a) Substituting the given values in Eq. (2.5), we obtain the values given in the following table, where the percentage error ϵ is defined as

$$\epsilon \equiv \frac{|G| - (R_2/R_1)}{(R_2/R_1)} \times 100$$

The values of v_1 are obtained from $v_1 = -v_O/A = Gv_I/A$ with $v_I = -0.1$ V.

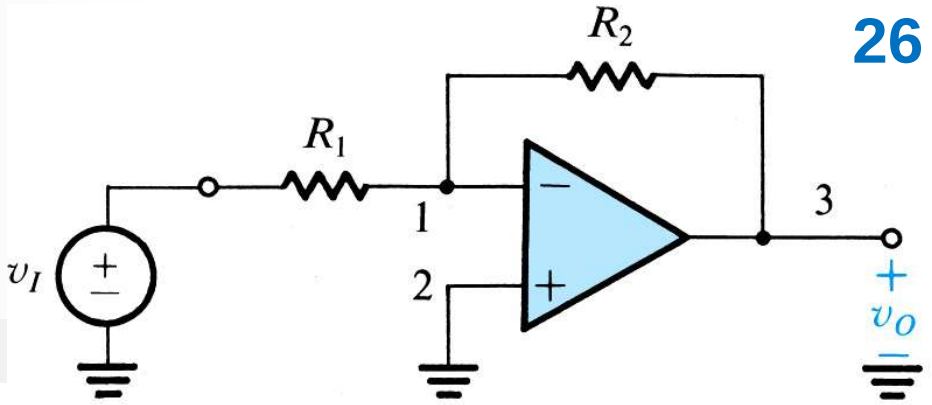
A	$\lvert G\rvert$	ϵ	v_1
10^3	90.83	−9.17%	−9.08 mV
10^4	99.00	−1.00%	−0.99 mV
10^5	99.90	−0.10%	−0.10 mV

(b) Using Eq. (2.5), we find that for $A = 50,000$, $|G| = 99.80$. Thus a −50% change in the open-loop gain results in a change in $|G|$ from 99.90 to 99.80, which is only −0.1%!

* Op amp 独自是不能用的，因为开环增益A为无穷大，必须外接电阻或电容等元件构成闭环反馈。Inverting configuration 是常见的一种构成闭环反馈的结构，其闭环电压增益仅与外接电阻有关。【**trade-off：trade gain for accuracy**】

2.2.3. Input and Output Resistances

输入电阻 & 输出电阻



- **Q:** What is input resistance for inverting op-amp? How is it defined mathematically?
  - **A:** R_1 (refer to math below)
- **Q:** What does this say?
  - **A:** That, for the combination of ideal op-amp and external resistors, input resistance will be finite…

关键点：$V_1=V_2=0$；

assumes ideal op-amp →

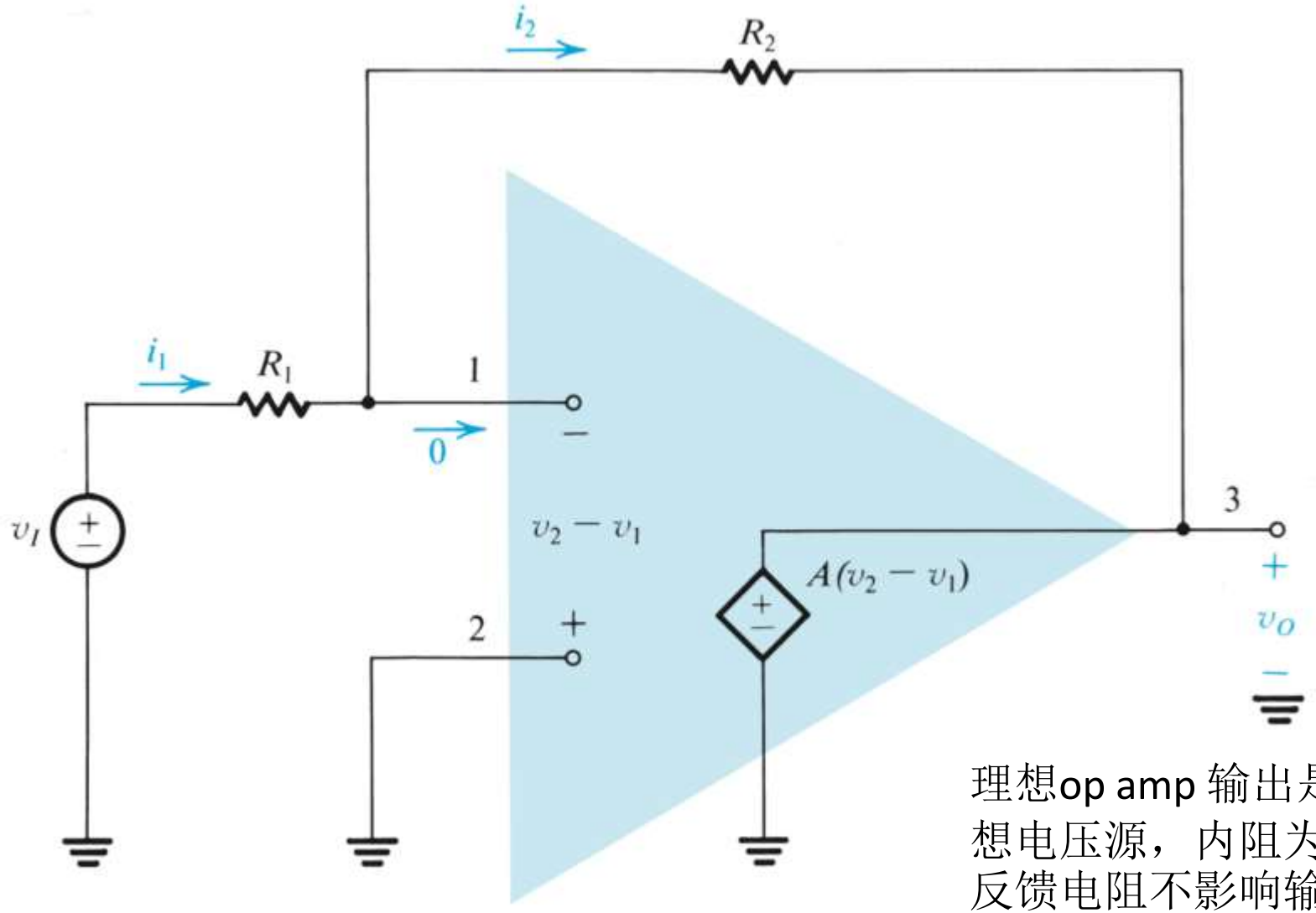
$$R_i = \frac{v_{In}}{i_{In}} = \frac{v_{In}}{(v_{In} - v_1)/R_1} = \frac{v_{In}}{v_{In}/R_1} = R_1$$

action: simplify — **action**: simplify

same as i_1

virtual ground $=0$

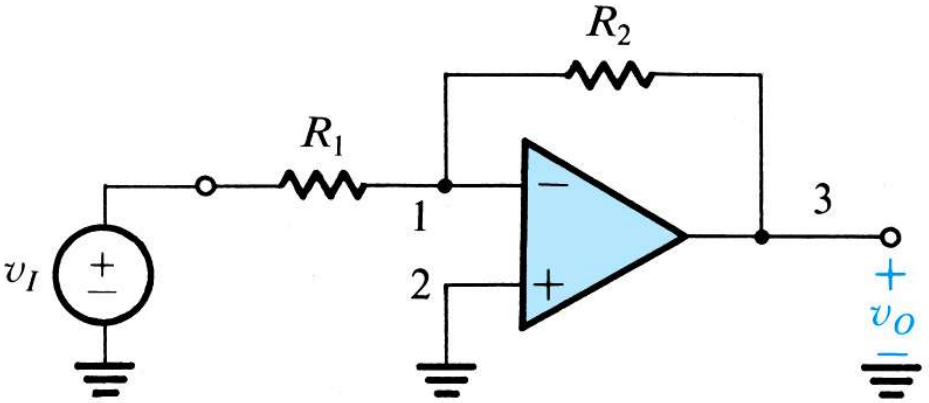
输出电阻呢？ 0



理想op amp 输出是一个理想电压源，内阻为零，外接反馈电阻不影响输出电阻

思考

- 理想的电压电压放大器，要求输入阻抗尽可能大 → 输入阻抗（R1）要尽可能大；
- 大的增益（-R2/R1） → R2的值会大得不切实际，如几MΩ等 → 只能牺牲R1，取较小的R1值
- 因此，常规反相连接运放电路存在输入阻抗较低的缺点



Example 2.2: Another Inverting Op-Amp

- **Problem Statement:** Consider the circuit below...
- **Q(a):** Derive an expression for the closed-loop gain v_{Out}/v_{In} of this circuit.
- **Q(b):** Use this circuit to design an inverting amplifier with gain of 100 and input resistance of 1*Mohm*.
  - Assume that one **cannot** use any resistor with resistance larger than 1*Mohm*.
- **Q(c):** Compare your design with that based on traditional inverting configuration.

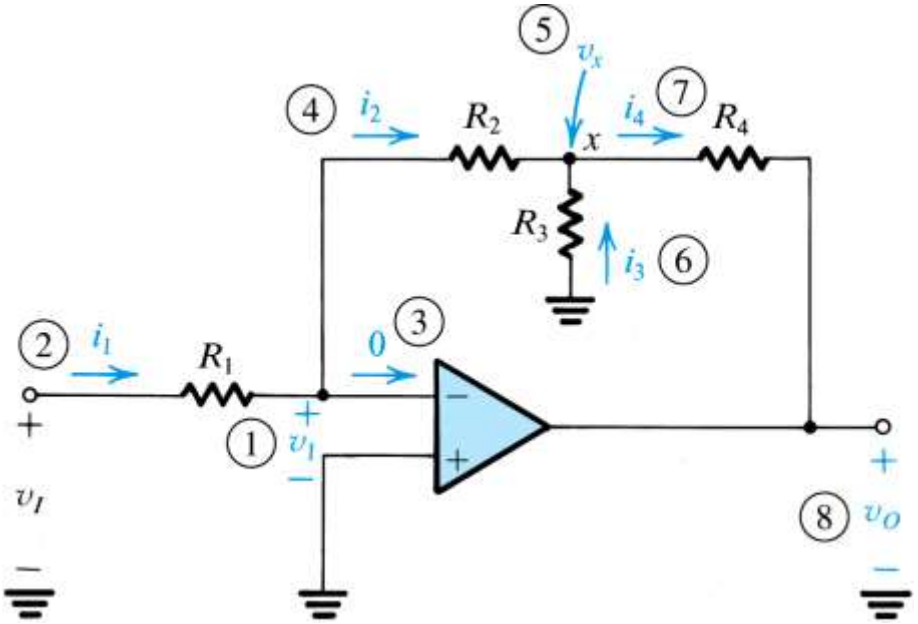
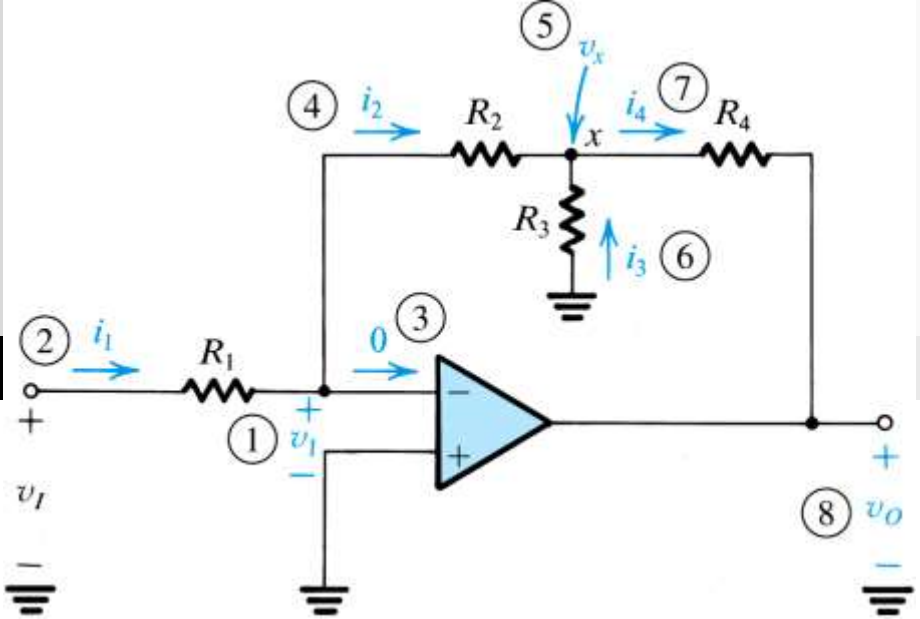


Figure 2.8: Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.



$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}\left(1 + \frac{R_4}{R_2} + \frac{R_4}{R_3}\right)$$

R1=1MΩ → R2=1MΩ →R4=1MΩ → R3用来实现增益 10.2kΩ

传统电路实现100的增益，
R2=100MΩ

① $$v_1 = \frac{-v_O}{A} = \frac{-v_O}{\infty} = 0$$

② $$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

④ $$i_2 = i_1 = \frac{v_I}{R_1}$$

⑤ $$v_x = v_1 - i_2 R_2 = 0 - \frac{v_I}{R_1} R_2 = -\frac{R_2}{R_1} v_I$$

⑥ $$i_3 = \frac{0 - v_x}{R_3} = \frac{R_2}{R_1 R_3} v_I$$

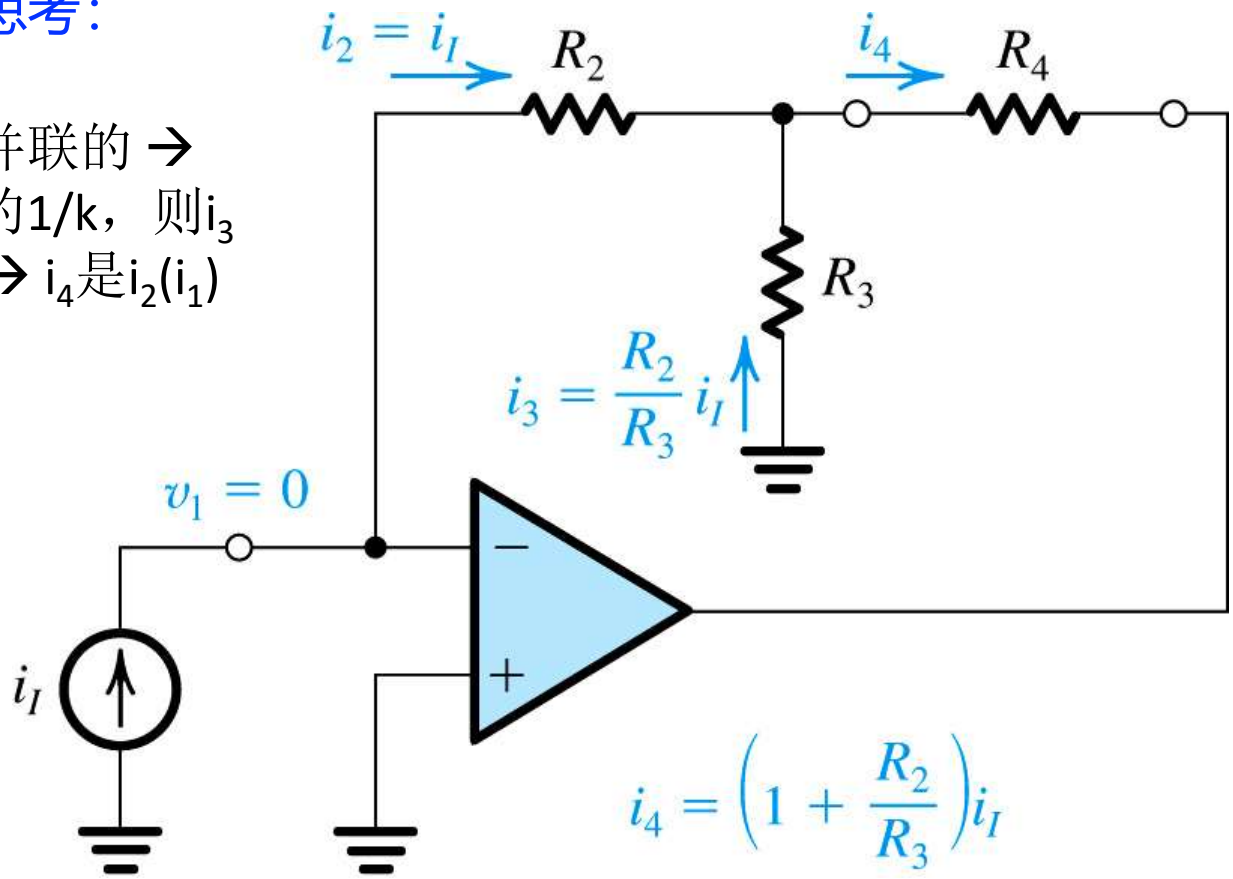
⑦ $$i_4 = i_2 + i_3 = \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I$$

⑧ $$v_O = v_x - i_4 R_4 = -\frac{R_2}{R_1} v_I - \left(\frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I\right) R_4$$

Figure 2.9: A current amplifier based on the circuit of Fig. 2.8. The amplifier delivers its output current to R_4. It has a current gain of (1 + R_2 /R_3)

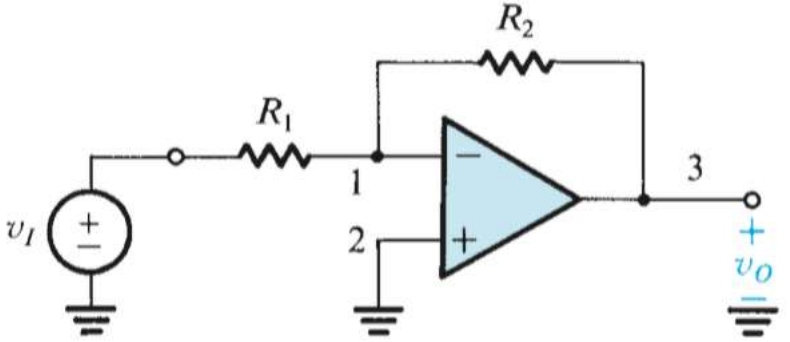
换个角度思考：
【Insight】

R2、R3是并联的 → 若R3为R2的1/k，则i_3是i_2的k倍 → i_4是i_2(i_1)的k+1倍



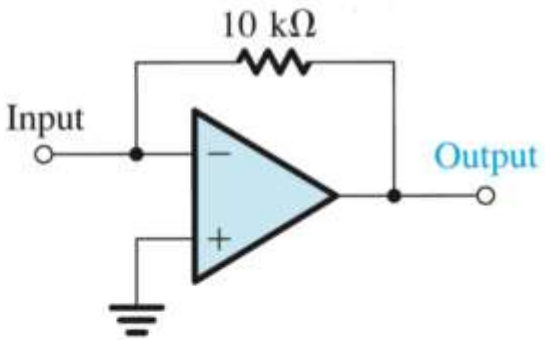
D2.4 Use the circuit of Fig. 2.5 to design an inverting amplifier having a gain of -10 and an input resistance of 100 kΩ. Give the values of R_1 and R_2.

Ans. $R_1 = 100\ \text{k}\Omega$; $R_2 = 1\ \text{M}\Omega$

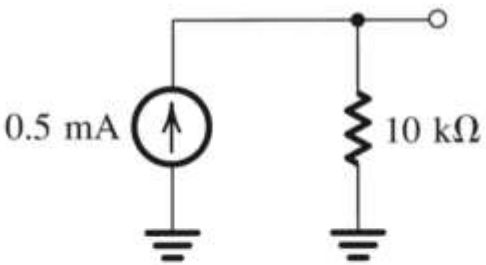


2.5 The circuit shown in Fig. E2.5(a) can be used to implement a transresistance amplifier (see Table 1.1 in Section 1.5). Find the value of the input resistance R_i, the transresistance R_m, and the output resistance R_o of the transresistance amplifier. If the signal source shown in Fig. E2.5(b) is connected to the input of the transresistance amplifier, find the amplifier output voltage.

Ans. $R_i = 0$; $R_m = -10\ \text{k}\Omega$; $R_o = 0$; $v_o = -5\ \text{V}$



(a)



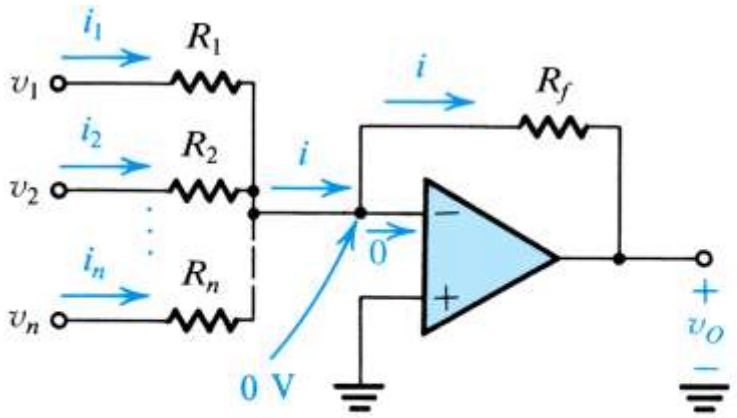
(b)

Figure E2.5

2.2.4. An Important Application – The Weighted Summer

加法器

- **weighted summer** - is a closed-loop amplifier configuration which provides an output voltage which is weighted sum of the inputs.



$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

Figure 2.10: A weighted summer.

$$v_{Out} = -[\,(R_f/R_{In1})v_{In1} + (R_f/R_{In2})v_{In2} + (R_f/R_{In3})v_{In3} + \ldots\,]$$

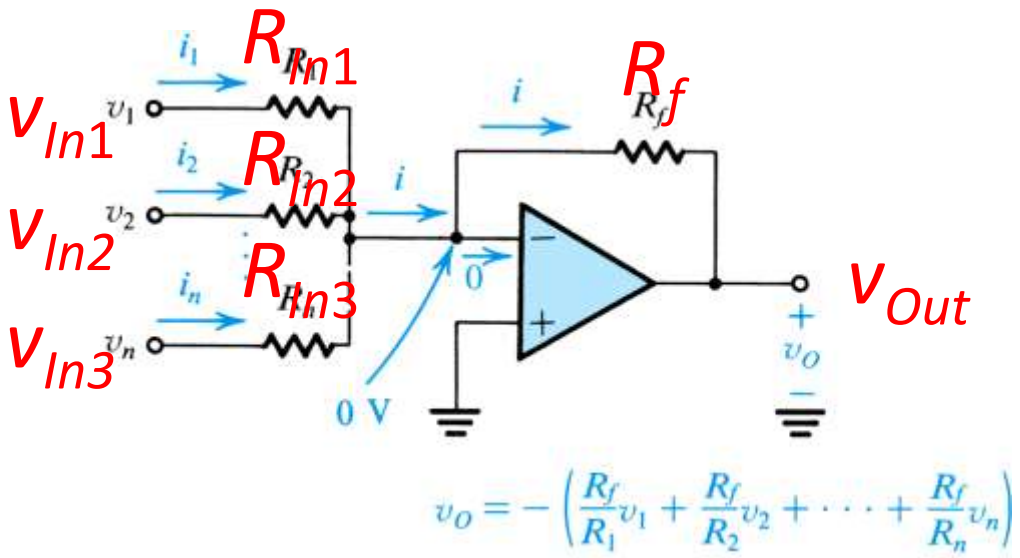


Figure 2.10: A weighted summer.

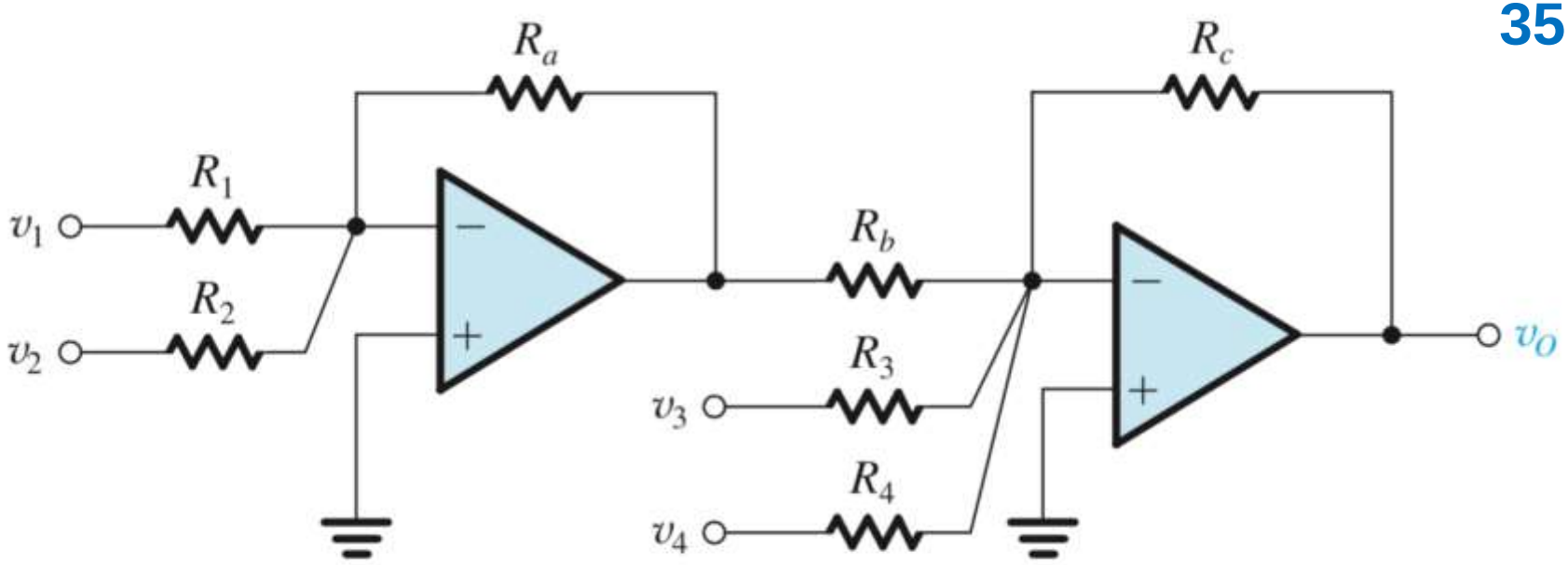


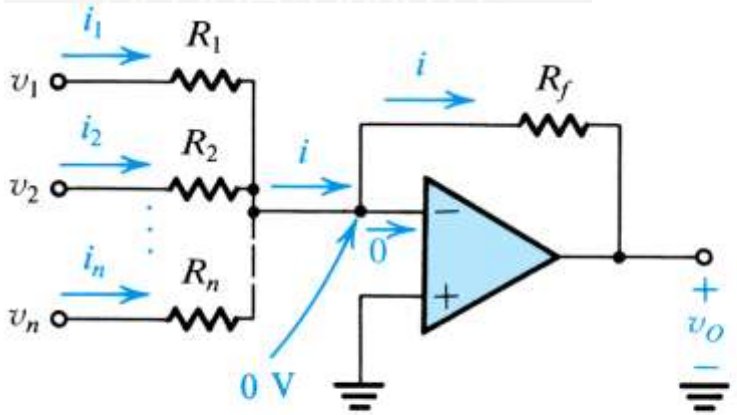
Figure 2.11 A weighted summer capable of implementing summing coefficients of both signs.

$$v_O = v_1\left(\frac{R_a}{R_1}\right)\left(\frac{R_c}{R_b}\right) + v_2\left(\frac{R_a}{R_2}\right)\left(\frac{R_c}{R_b}\right) - v_3\left(\frac{R_c}{R_3}\right) - v_4\left(\frac{R_c}{R_4}\right)$$

实现加减法

D2.7 Design an inverting op-amp circuit to form the weighted sum v_o of two inputs v_1 and v_2. It is required that $v_o = -(v_1 + 5v_2)$. Choose values for R_1, R_2, and R_f so that for a maximum output voltage of 10 V the current in the feedback resistor will not exceed 1 mA.

Ans. A possible choice: $R_1 = 10\ \text{k}\Omega, R_2 = 2\ \text{k}\Omega$, and $R_f = 10\ \text{k}\Omega$



$$v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

2.3. The Non-Inverting Configuration

同相接法

- **non-inverting op-amp configuration** – is one which utilizes external resistances (like the previous) to effect voltage gain. However, the polarity / phase of the output is same as input.

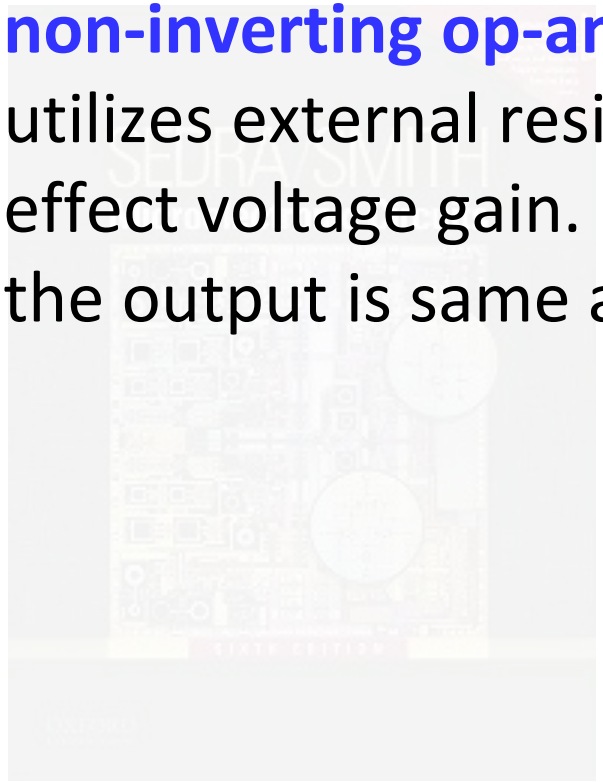
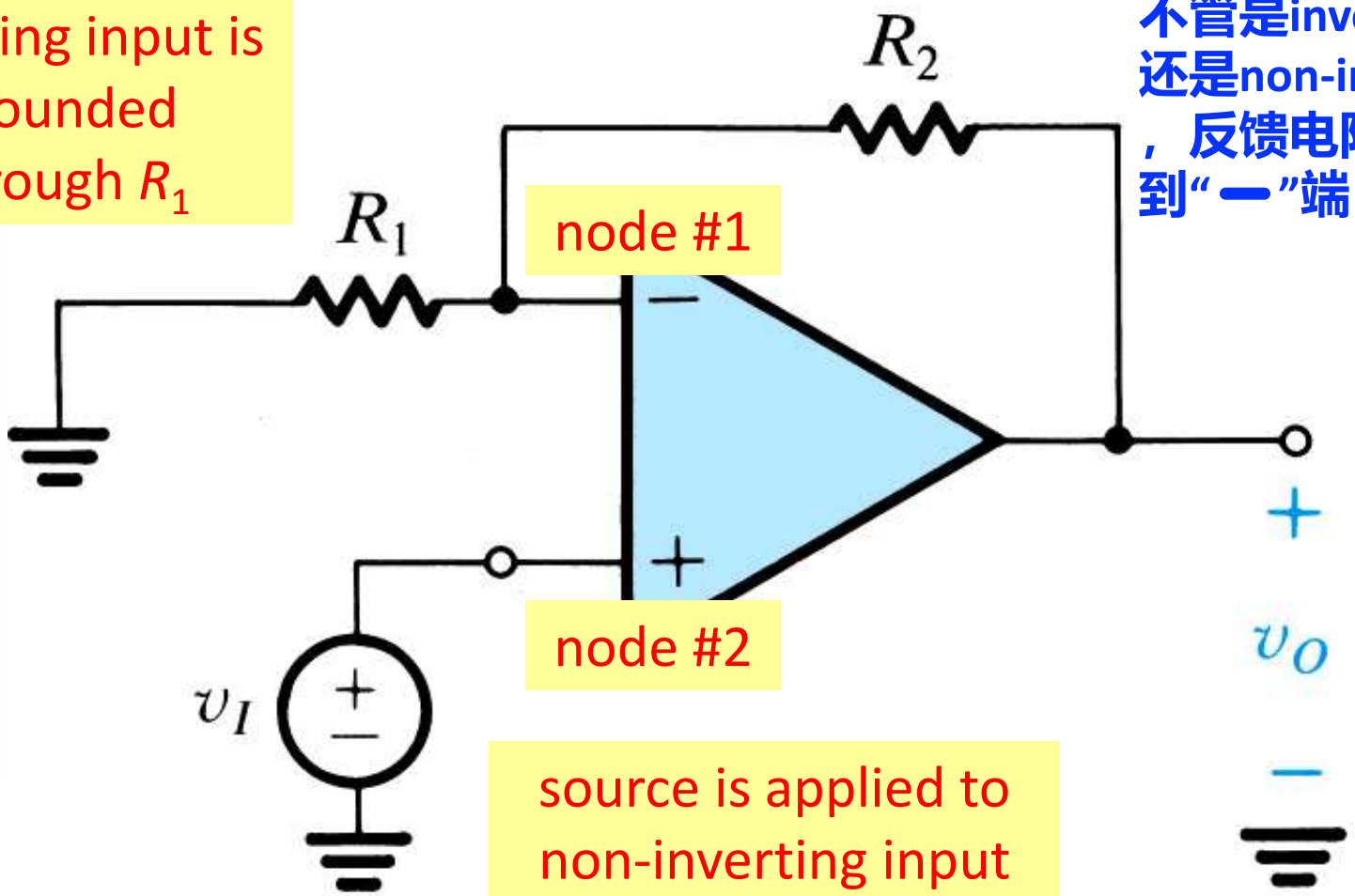


Figure 2.12: The non-inverting configuration.

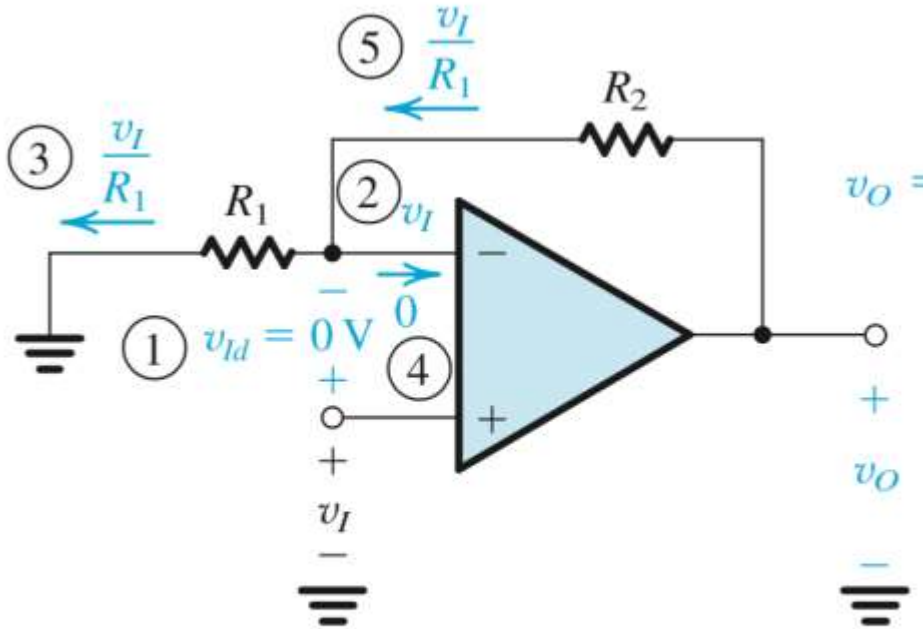
R_1 and R_2 act as voltage divider, regulating negative feedback to the inverting input

inverting input is grounded through R_1

不管是inverting，还是non-inverting，反馈电阻都是接到“－”端



source is applied to non-inverting input



$$v_O = v_I + \frac{v_I}{R_1}R_2 = v_I\left(1 + \frac{R_2}{R_1}\right) \quad ⑥$$

可以看成分压

Figure 2.13 Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

① $v_{Id} = \dfrac{v_O}{A} = 0 \qquad \text{for } A = \infty$

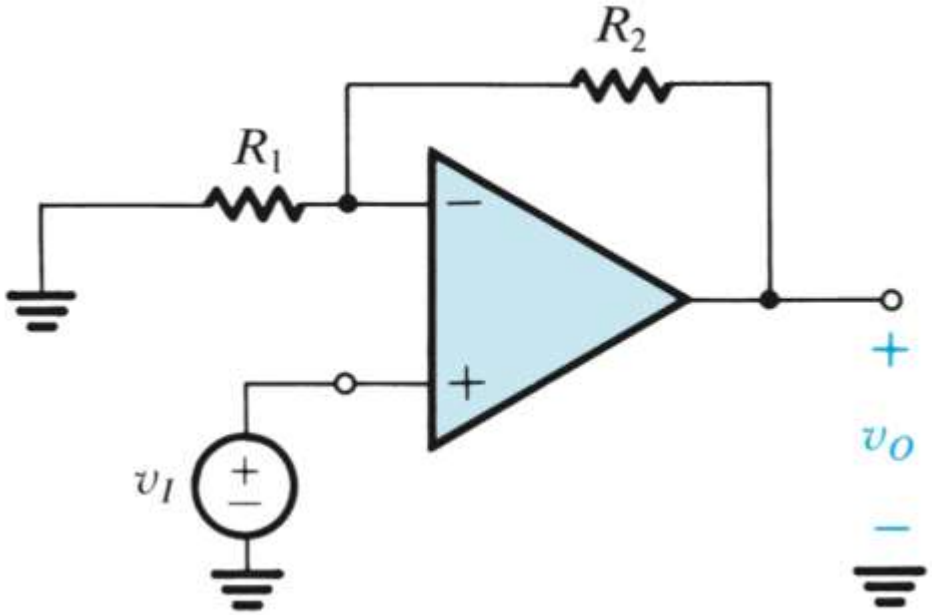
②

③ v_I/R_1.

④

⑤

⑥ $v_O = v_I + \left(\dfrac{v_I}{R_1}\right)R_2 \Rightarrow \boxed{\dfrac{v_O}{v_I} = 1 + \dfrac{R_2}{R_1}}$



- 若开环增益A不是无穷大，则如何计算？

v_2-v_1=v_o/A

$$G \equiv \frac{v_O}{v_I} = \frac{1 + (R_2/R_1)}{1 + \dfrac{1 + (R_2/R_1)}{A}}$$

同样，输入阻抗为∞，输出阻抗为0

Characteristics of Non-Inverting Op-Amp Configuration

ideal gain $\left(A >> 1 + \frac{R_2}{R_1} \right)$**:** $\frac{v_{Out}}{v_{In}}$

$$G_{A=\infty} = 1 + \frac{R_2}{R_1}$$

non - ideal gain :

$$G_{A<\infty} = \frac{1 + (R_2 / R_1)}{1 + \frac{1 + (R_2 / R_1)}{A}}$$

$\frac{v_{Out}}{v_{In}}$

percent gain error :

$$pge = 100 \left| \frac{1 + (R_2 / R_1)}{A + 1 + (R_2 / R_1)} \right|$$

inverting input potential :

$$v_1 = v_{Out} \left(\frac{R_1}{R_1 + R_2} \right)$$

Configuration and Characteristics of Buffer / Voltage-Follower Op-Amp Configuration

Buffer amp: 提供高输入阻抗、低输出阻抗，增益非主要考虑因素

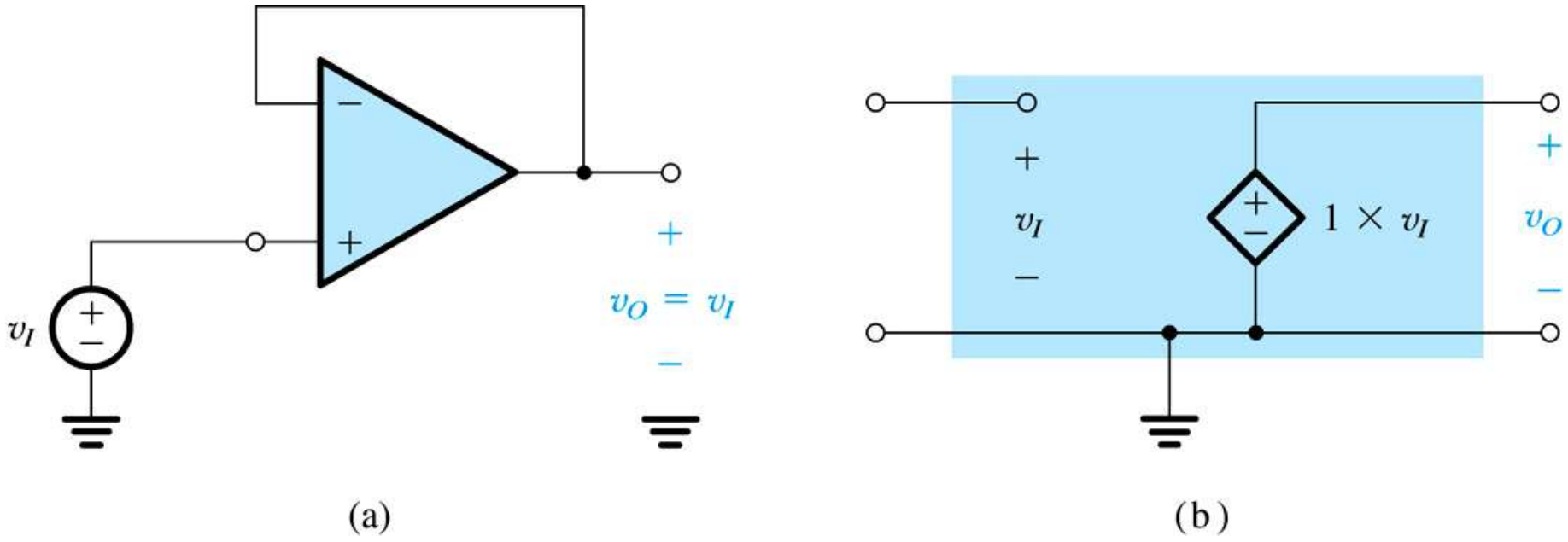


Figure 2.14: (**a**) The unity-gain buffer or follower amplifier. (**b**) Its equivalent circuit model.

Main point? For the buffer amp, output voltage is equal (in both magnitude and phase) to the input source. However, any current supplied to the load is drawn from amplifier supplies (V_{CC}, V_{EE}) and not the input source (v_I).

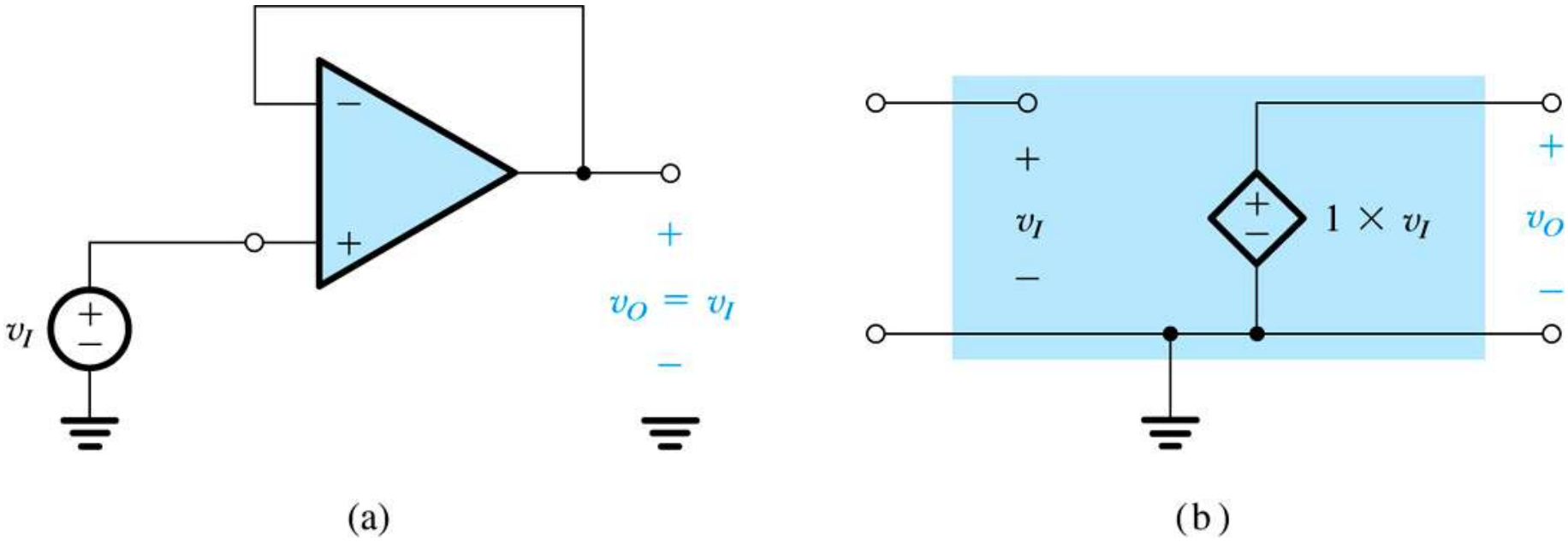
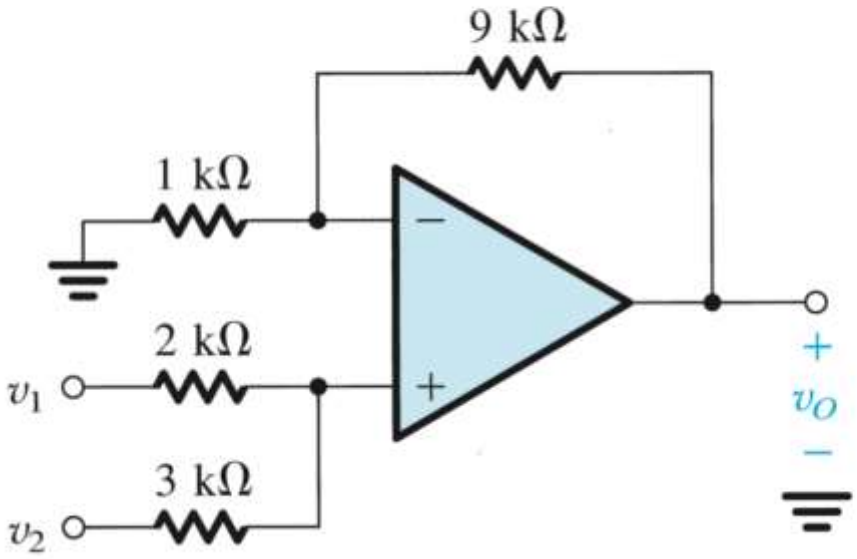


Figure 2.14: (**a**) The unity-gain buffer or follower amplifier. (**b**) Its equivalent circuit model.

2.9 Use the superposition principle to find the output voltage of the circuit shown in Fig. E2.9.

Ans. $v_o = 6v_1 + 4v_2$



对v1，v2应用叠加原理

Figure E2.9

2.10 If in the circuit of Fig. E2.9 the 1-kΩ resistor is disconnected from ground and connected to a third signal source v_3, use superposition to determine v_o in terms of v_1, v_2, and v_3.

Ans. $v_o = 6v_1 + 4v_2 - 9v_3$

2.13 For the circuit in Fig. E2.13 find the values of i_I, v_1, i_1, i_2, v_O, i_L, and i_O. Also find the voltage gain v_O/v_I, the current gain i_L/i_I, and the power gain P_L/P_I.

Ans. 0; 1 V; 1 mA; 1 mA; 10 V; 10 mA; 11 mA; 10 V/V (20 dB); ∞; ∞

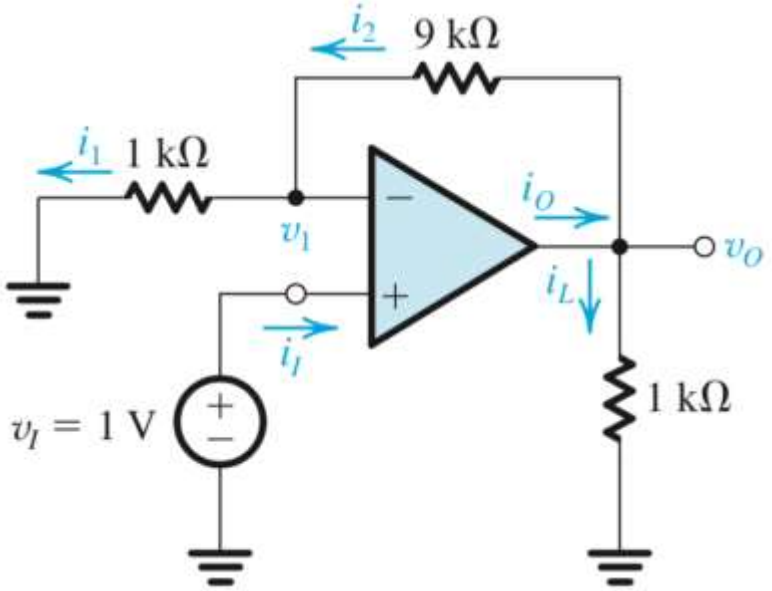


Figure E2.13

2.4. Difference Amplifiers 差分放大器

理想差分放大器，只放大输入的差分信号，对输入共模信号的增益为零

但实际上，会存在较小的共模增益

- **difference amplifier** – is a closed-loop configuration which responds to the difference between two signals applied at its input and ideally rejects signals that are common to the two.
  - Ideally, the amp will amplify only the differential signal (v_{dfi}) and reject completely the common-mode input signal (v_{cmi}). However, a practical circuit will behave as below…

$$v_{Out} = Av_{dfi} + A_{cm}v_{cmi}$$

2.4. Difference Amplifiers

common-mode input

common-mode gain

differential input

differential gain

$$v_{Out} = Av_{dfi} + A_{cm}v_{cmi}$$

2.4. Difference Amplifiers

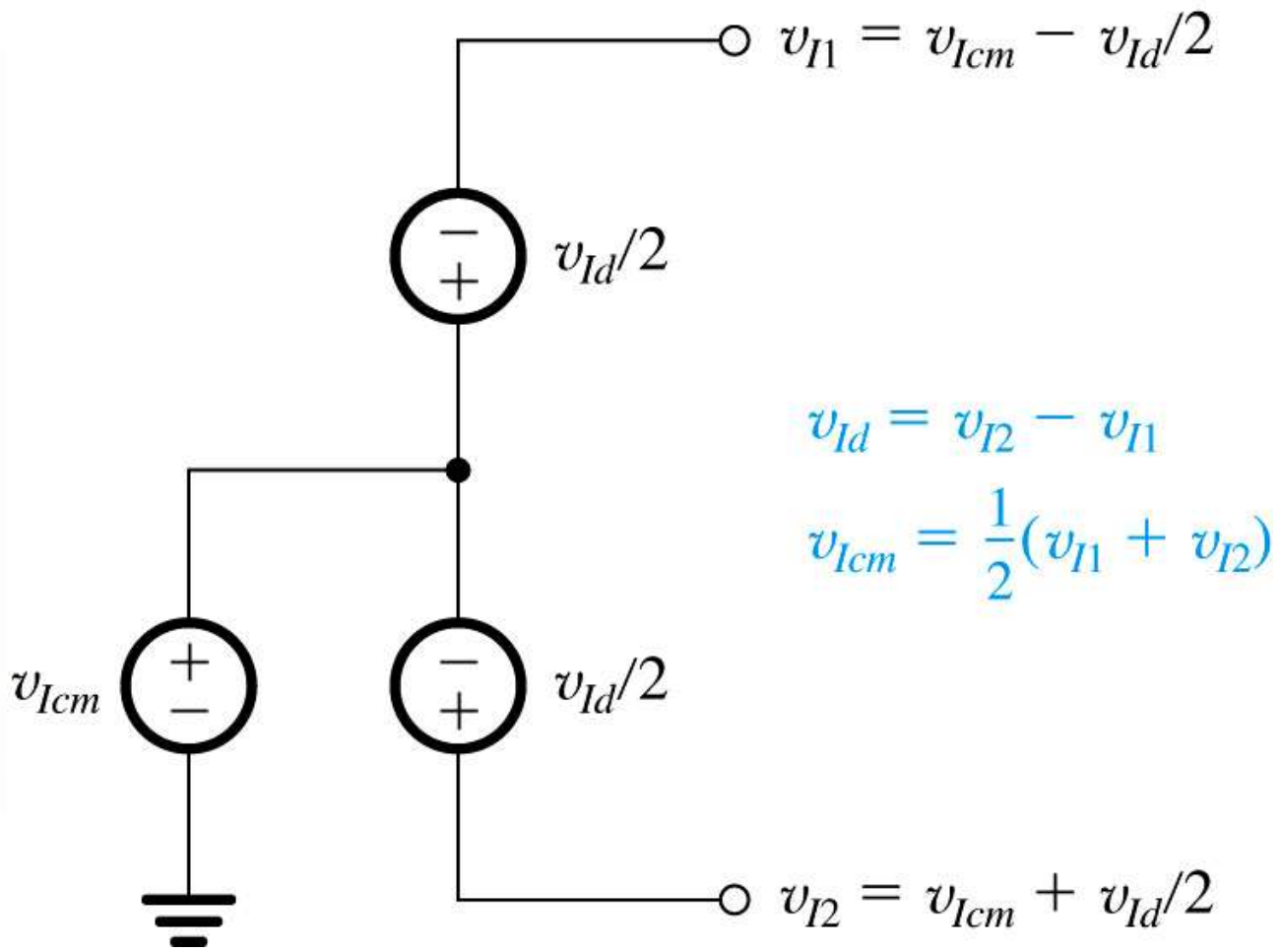
$$v_{Out} = Av_{dfi} + A_{cm}v_{cmi}$$

共模抑制比

- **common-mode rejection ratio** (CMRR) – is the degree to which a differential amplifier "rejects" the common-mode input.
  - Ideally, CMRR = *infinity*…

$$CMRR = 20\ \mathbf{log}_{10}\left|\frac{A}{A_{Cm}}\right|$$

Figure 2.15: Representing the input signals to a differential amplifier in terms of their differential and common-mode components.



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2.4. Difference Amplifiers

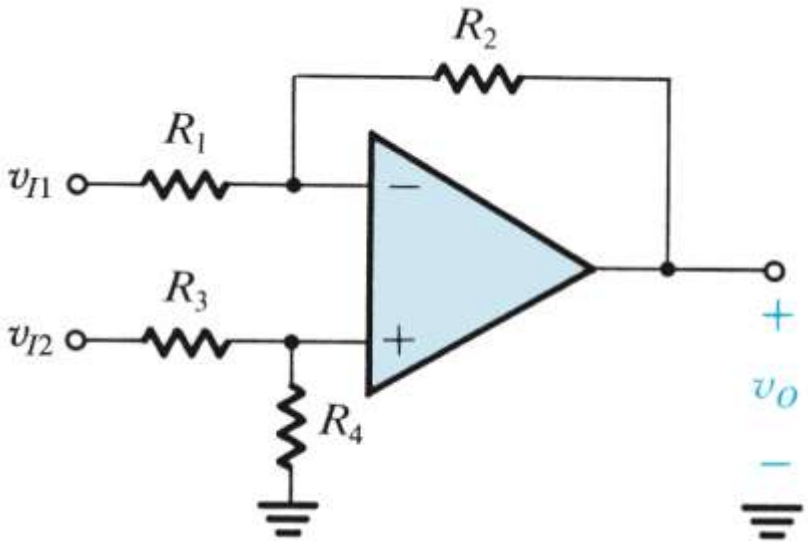
- **Q:** The op amp itself is differential in nature, why cannot it be used by itself? 运放本身就是差分输入的，为何不能直接用作差分放大器？
  - **A:** It has an infinite gain, and therefore cannot be used by itself. One must devise a closed-loop configuration which facilitates this operation.
  - 运放增益太大，且不稳定、不精确（一个很大的增益是做不到稳定和精确的）
  - 我们需要牺牲增益，来换取稳定性和精确性（**trade-off**，折衷）

【Insight】如何构建一个差分放大器?

noninverting amplifier configuration is positive, $(1 + R_2/R_1)$

inverting configuration is negative, $(-R_2/R_1)$

将noninverting configuration的输入适当衰减，使其总的增益等于R2/R1，则可构成一个差分放大器



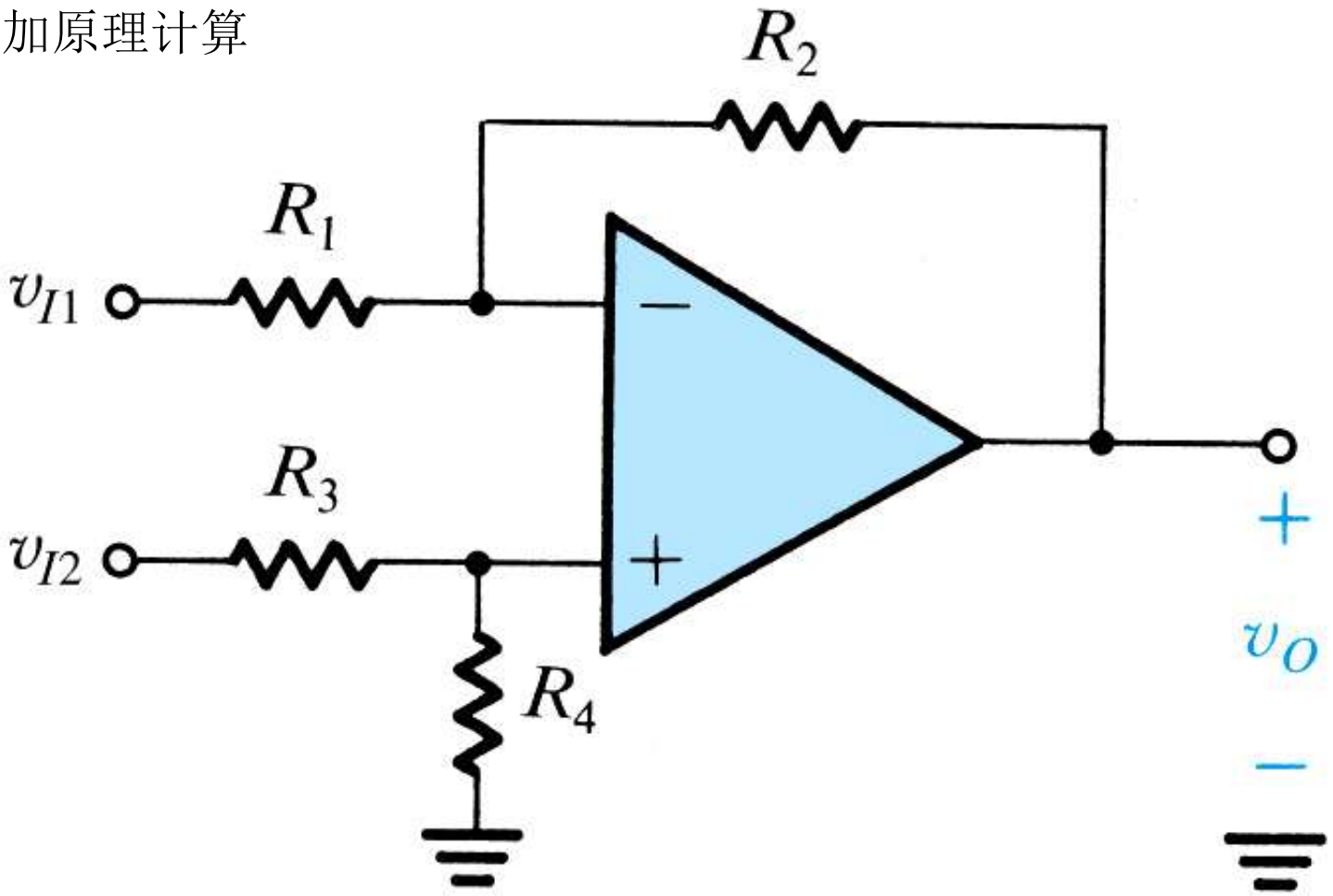
$$\frac{R_4}{R_4 + R_3}\left(1 + \frac{R_2}{R_1}\right) = \frac{R_2}{R_1}$$

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$

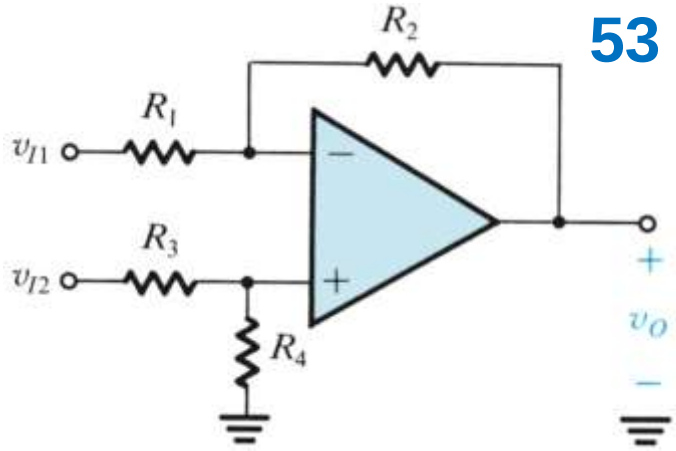
Figure 2.16 A difference amplifier.

Figure 2.16: A difference amplifier.

利用叠加原理计算



2.4.1. A Single Op-Amp Difference Amp



- **Q:** What are the characteristics of the difference amplifier?
  - **A:** Refer to following equations…

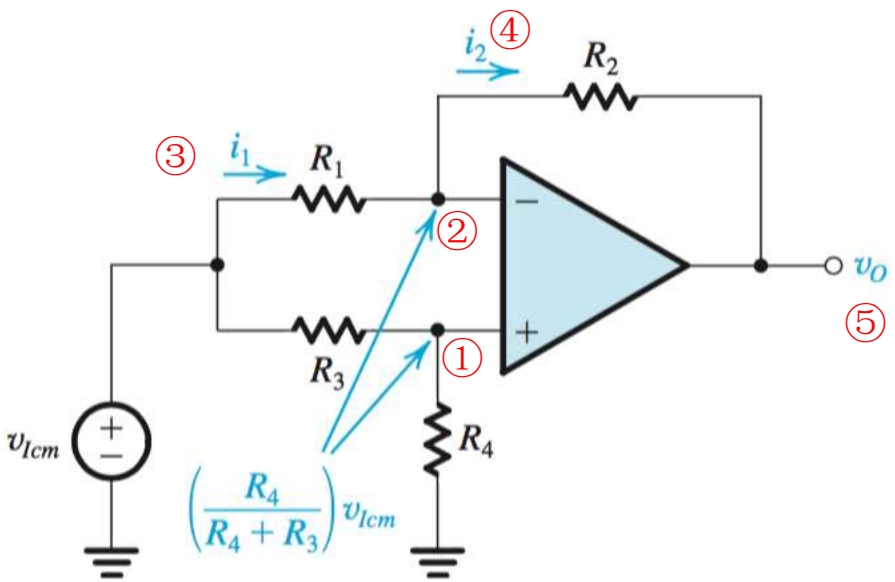
$$v_{Out} = \frac{(R_2 + R_1)R_4}{(R_4 + R_3)R_1} v_{In2} - \frac{R_2}{R_1} v_{In1}$$

$$A_d = \frac{R_2}{R_1}$$

but if $\begin{cases} R_1 = R_3 \\ R_2 = R_4 \end{cases}$ then $v_{Out} = \frac{R_2}{R_1}(v_{In2} - v_{In1})$

平衡条件

共模输入情况



① $\dfrac{R_4}{R_4+R_3}v_{Icm}$

②

③ $i_1 = \dfrac{1}{R_1}\left[v_{Icm} - \dfrac{R_4}{R_4+R_3}v_{Icm}\right]$

④ $= v_{Icm}\dfrac{R_3}{R_4+R_3}\dfrac{1}{R_1}$

⑤ $v_O = \dfrac{R_4}{R_4+R_3}v_{Icm} - i_2R_2$

$$v_O = \frac{R_4}{R_4+R_3}v_{Icm} - \frac{R_2}{R_1}\frac{R_3}{R_4+R_3}v_{Icm}$$

$$= \frac{R_4}{R_4+R_3}\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right)v_{Icm}$$

$$A_{cm} \equiv \frac{v_O}{v_{Icm}} = \left(\frac{R_4}{R_4+R_3}\right)\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right)$$

平衡时，$A_{cm}=0$；若不平衡，$A_{cm}\neq 0$

输入阻抗

存在的缺点：

差分放大器需要提供较大差分增益（R2/R1）→ R1要小 → 输入阻抗变小！

如何解决这一缺点？

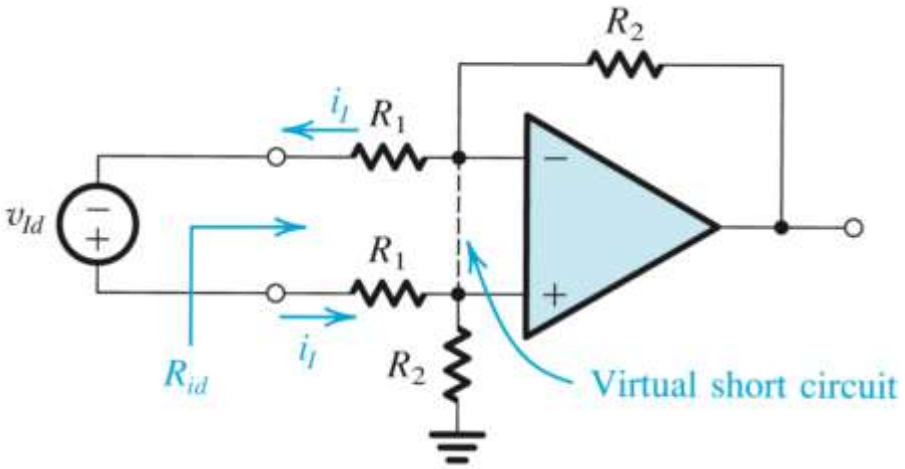


Figure 2.19 Finding the input resistance of the difference amplifier for the case $R_3 = R_1$ and $R_4 = R_2$.

① R_{id} 差分输入阻抗 $R_{id} \equiv \frac{v_{Id}}{i_I}$

② 考虑平衡情况 $v_{Id} = R_1 i_I + 0 + R_1 i_I$

$$R_{id} = 2R_1$$

2.15 Consider the difference-amplifier circuit of Fig. 2.16 for the case $R_1 = R_3 = 2\ \text{k}\Omega$ and $R_2 = R_4 = 200\ \text{k}\Omega$. (a) Find the value of the differential gain A_d. (b) Find the value of the differential input resistance R_{id} and the output resistance R_o. (c) If the resistors have 1% tolerance (i.e., each can be within ±1% of its nominal value), use Eq. (2.19) to find the worst-case common-mode gain A_{cm} and hence the corresponding value of CMRR.

Ans. (a) 100 V/V (40 dB); (b) 4 kΩ, 0 Ω; (c) 0.04 V/V, 68 dB

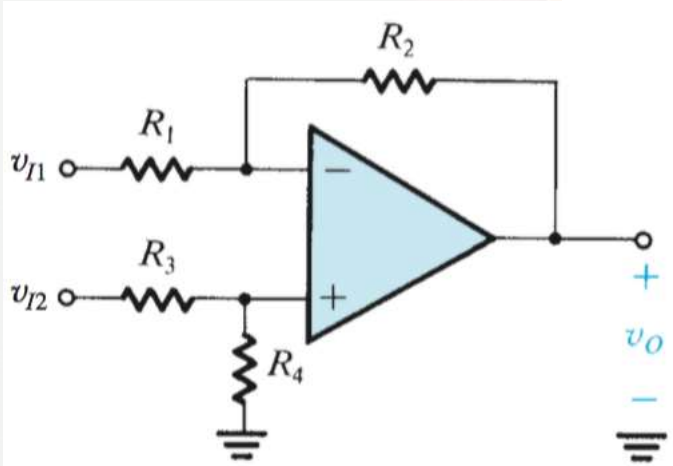
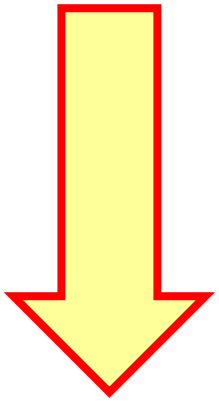


Figure 2.16 A difference amplifier.

$$A_{cm} \equiv \frac{v_O}{v_{Icm}} = \left(\frac{R_4}{R_4 + R_3}\right)\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right) \qquad (2.19)$$

A Shift in Notation



- Before this point…
  - The parameter *A* is used to represent open-loop gain of an op amp.
  - The parameter *G* is used to represent ideal / non-ideal closed-loop gain of an op amp.
- After this point…
  - The parameter *A* is used to represent ideal gain of an op amp in a given closed-loop configuration.
  - The parameter *G* is not used.

A代表理想运放的闭环增益

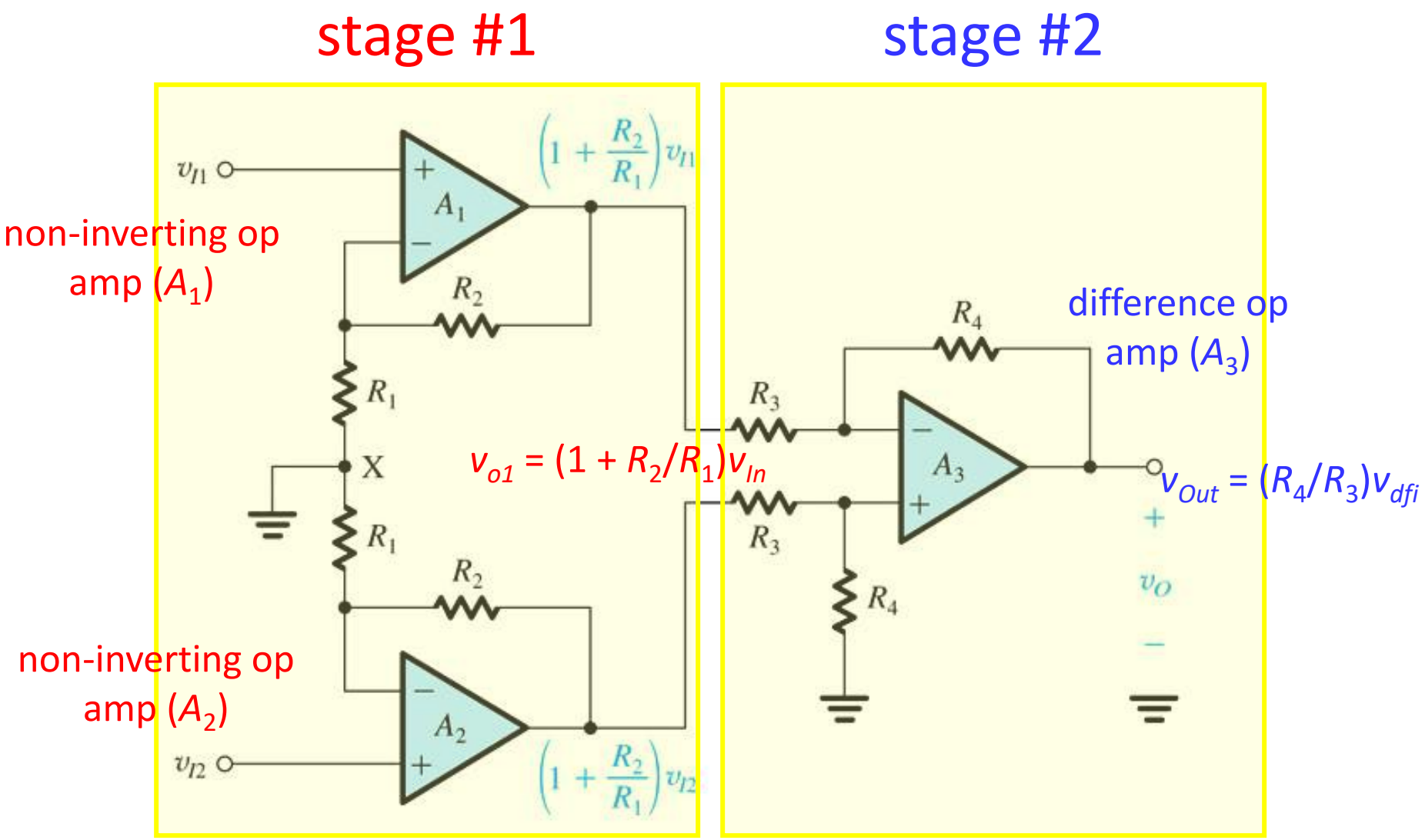
2.4.2. The Instrumentation Amplifier 仪表放大器

- **Q:** What is one problem associated with the difference amplifier? 差分放大器存在的缺点
  - **A:** Low input impedance. 输入阻抗低
- **Q:** And, what does this mean practically? 有什么影响
  - **A:** That source impedance will have an effect on gain. 输入端分压衰减 → 施加于放大器输入端的有效信号电压降低
- **Q:** What is the solution? 解决方法
  - **A:** Placement of two buffers at the input terminals, amplifiers which transmit the voltage level but draw minimal current. 在输入端插入buffer amp，提高R_{in}

2.4.2. The Instrumentation Amplifier

- **Q:** However, can one get "more" from these amps than simply impedance matching?
  - **A:** Yes, maybe additional voltage gain???
  - 在插入buffer amp，以提高输入阻抗的同时，还可以获得额外的增益

Figure 2.20: A popular circuit for an instrumentation amplifier.



2.4.2. The Instrumentation Amplifier

- **Q:** However, can one get "more" from these amps than simply impedance matching?
  - **A:** Yes, maybe additional voltage gain???

transfer function for instrumentation amplifier of figure 2.20.

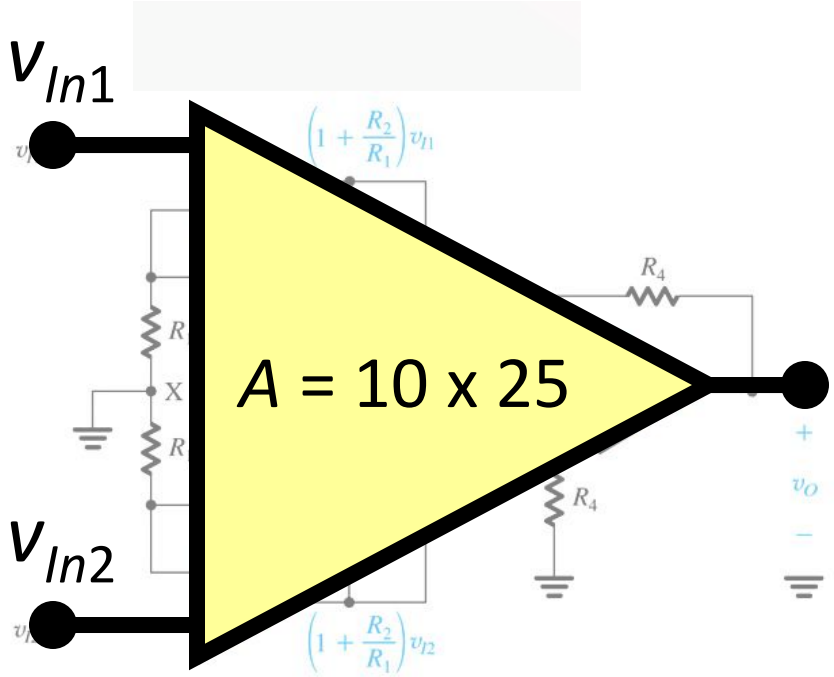
$$v_{Out} = \underbrace{\frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)}_{\mathbf{A}_{Inst}(R)} v_{dfi}$$

additional voltage gain

2.4.2. The Instrumentation Amplifier

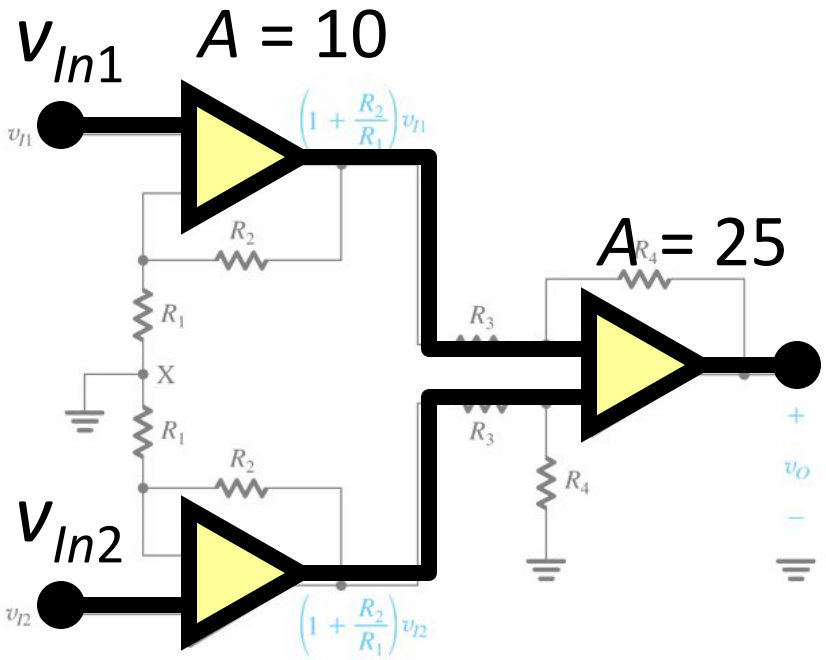
- **Advantages优点** of instrumentation amp
  - very high input resistance 输入阻抗很大
  - high differential gain 差分增益变大
  - symmetric gain (assuming that A_1 and A_2 are matched)
- **Disadvantages缺点** of instrumentation amp
  - A_{Di} and A_{Cm} are equal in first stage – meaning that the common-mode and differential inputs are amplified with equal gain… 第一级放大器对差分输入和共模输入进行了同样程度的放大！ → ①信号幅度过大容易使运放饱和；②第二级有更大的CMRR压力

What is problem with $A_{Cm} = A$?



differential gain >> common-mode gain

Case 1: 没有共模增益时

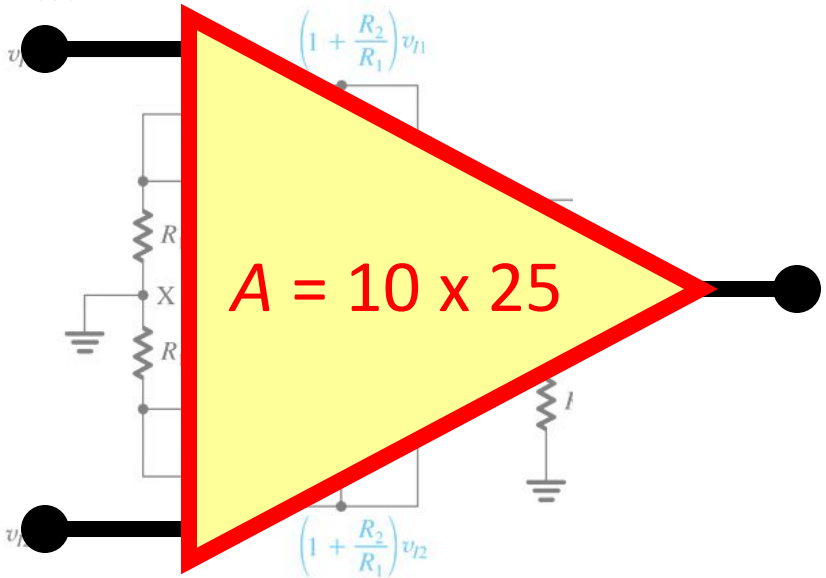


differential gain = common-mode gain

Case 2: 当第一级有共模增益时

differential gain >> common-mode gain

$v_{In1} = 10.02V$



$v_{In2} = 10.03V$

$v_{Out} = 250 \times (10.03 - 10.02)V$

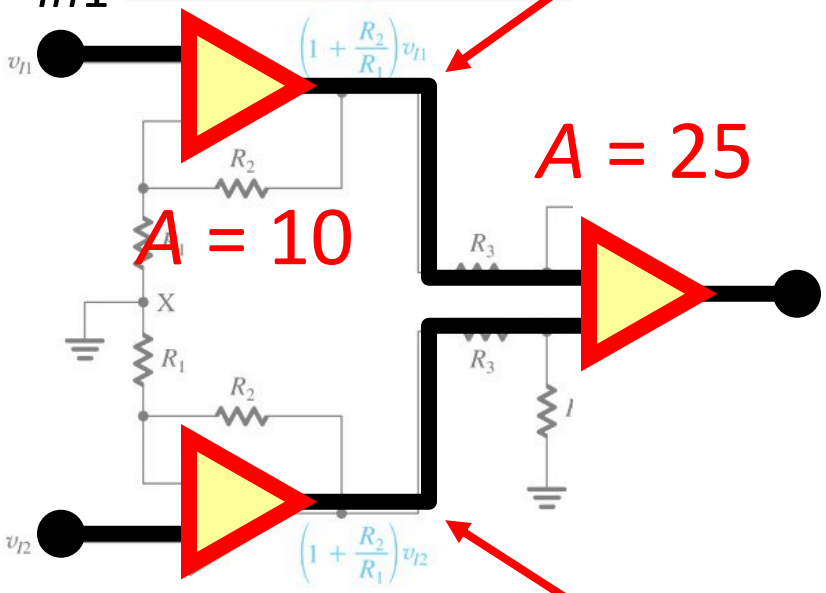
$v_{Out} = 2.5V$ **no problem!!!**

differential gain = common-mode gain

供电电源 ±15 V，限制了电路中最大允许的电压范围

$v_{In1} = 10.02V$

$v_{Out1} = 10 \times 10.02 = 15V$ saturation



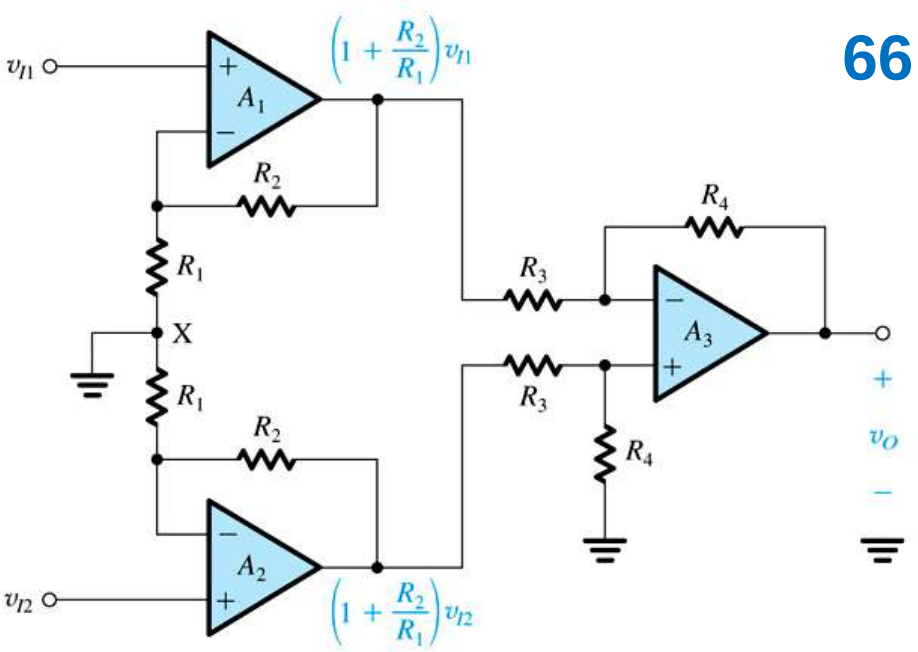
$v_{Out} = 25 \times (15-15)V$

$v_{Out} = 0V$ **problem!!!**

$v_{In2} = 10.03V$

$v_{Out2} = 10 \times 10.03 = 15V$ saturation

2.4.2. The Instrumentation Amplifier



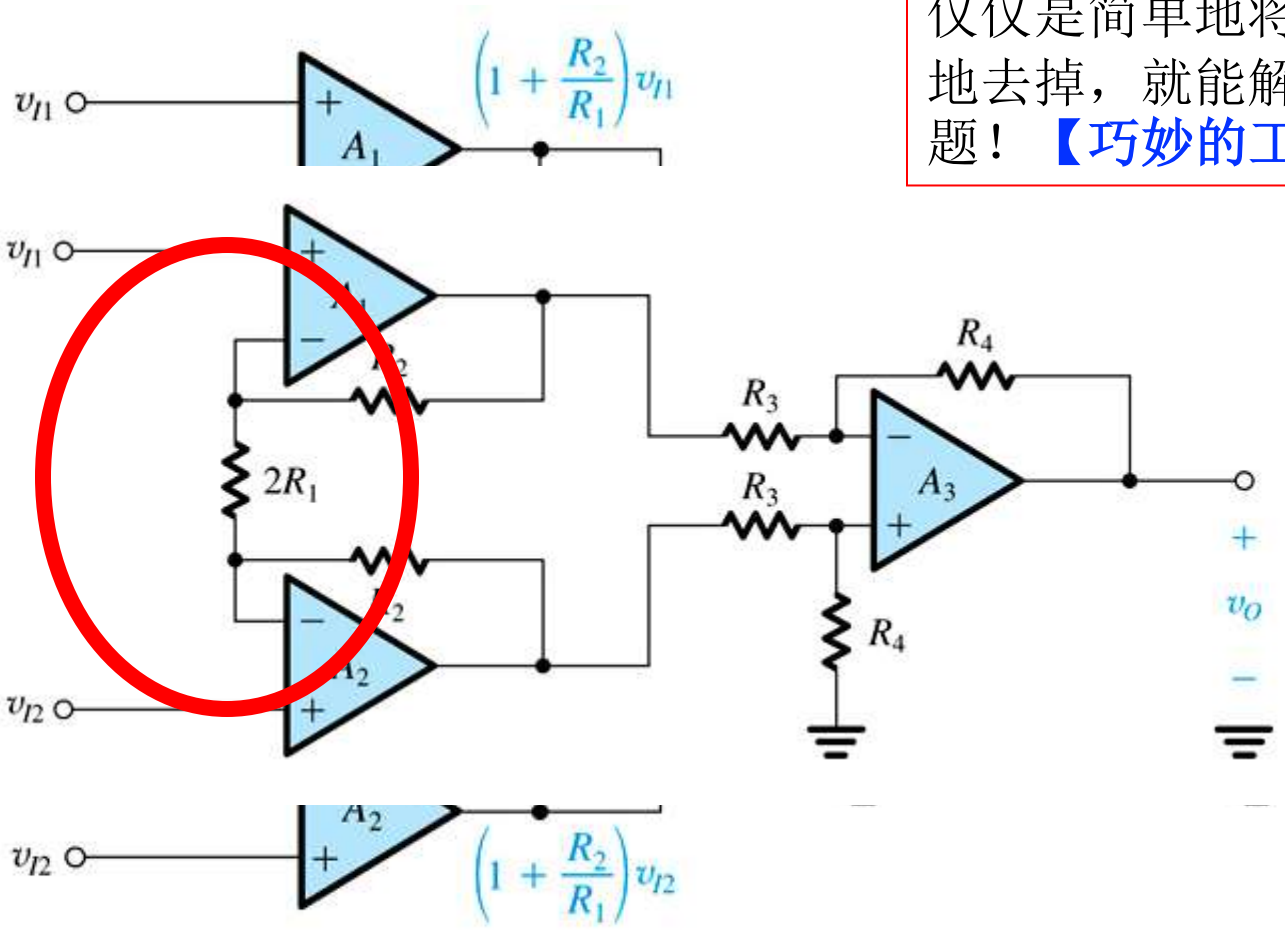
- **advantages** of instru. amp
  - **very high input resistance**
  - high differential gain
  - symmetric gain (assuming that A_1 and A_2 are matched)
- **disadvantages** of instrumentation amp
  - A_{Di} and A_{Cm} are equal in first stage – meaning that the common-mode and differential inputs are amplified with equal gain…
  - need for matching – if two op amps which comprise stage #1 are not perfectly matched, one will see unintended effects 如果第一级不完美匹配，那么将会对第二级的输入引入额外的差分信号

2.4.2. The Instrumentation Amplifier

- **Q:** How can one fix this (alleviate these disadvantages)?
  - **A:** Disconnect the two resistors (R_1) connected to node *X* from ground, making the configuration "floating" in nature…
  - **A:** Refer to following slide…

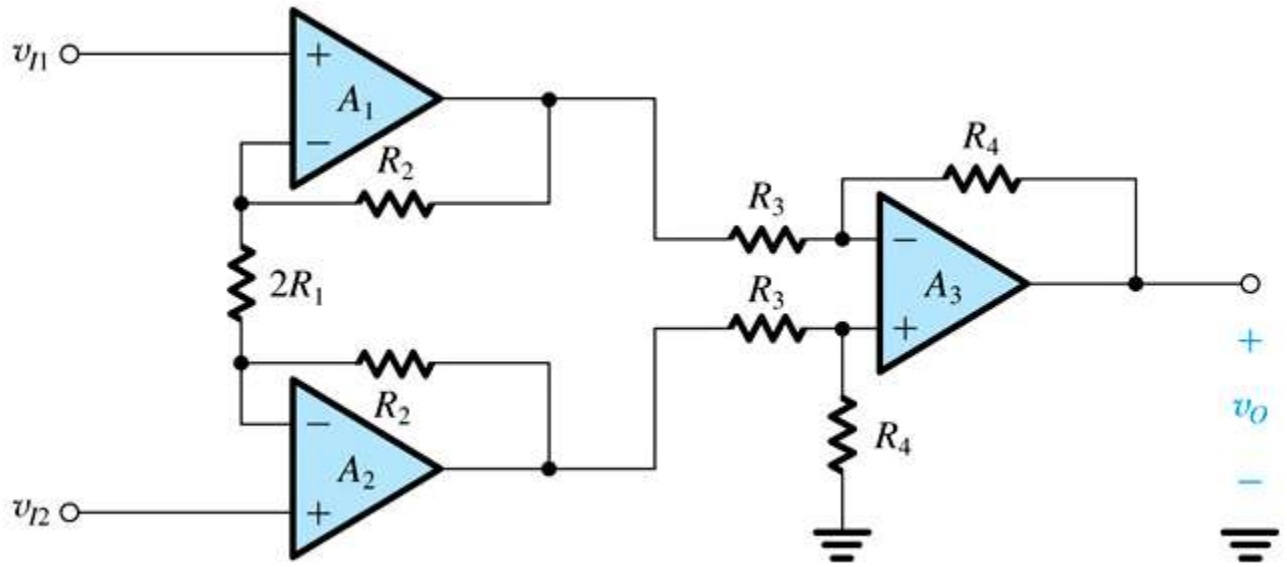
Figure 2.20: A popular circuit for an instrumentation amplifier. **(b)** The circuit in **(a)** with the connection between node X and ground removed and the two resistors R_1 and R_1 lumped together. This simple wiring change dramatically improves performance.

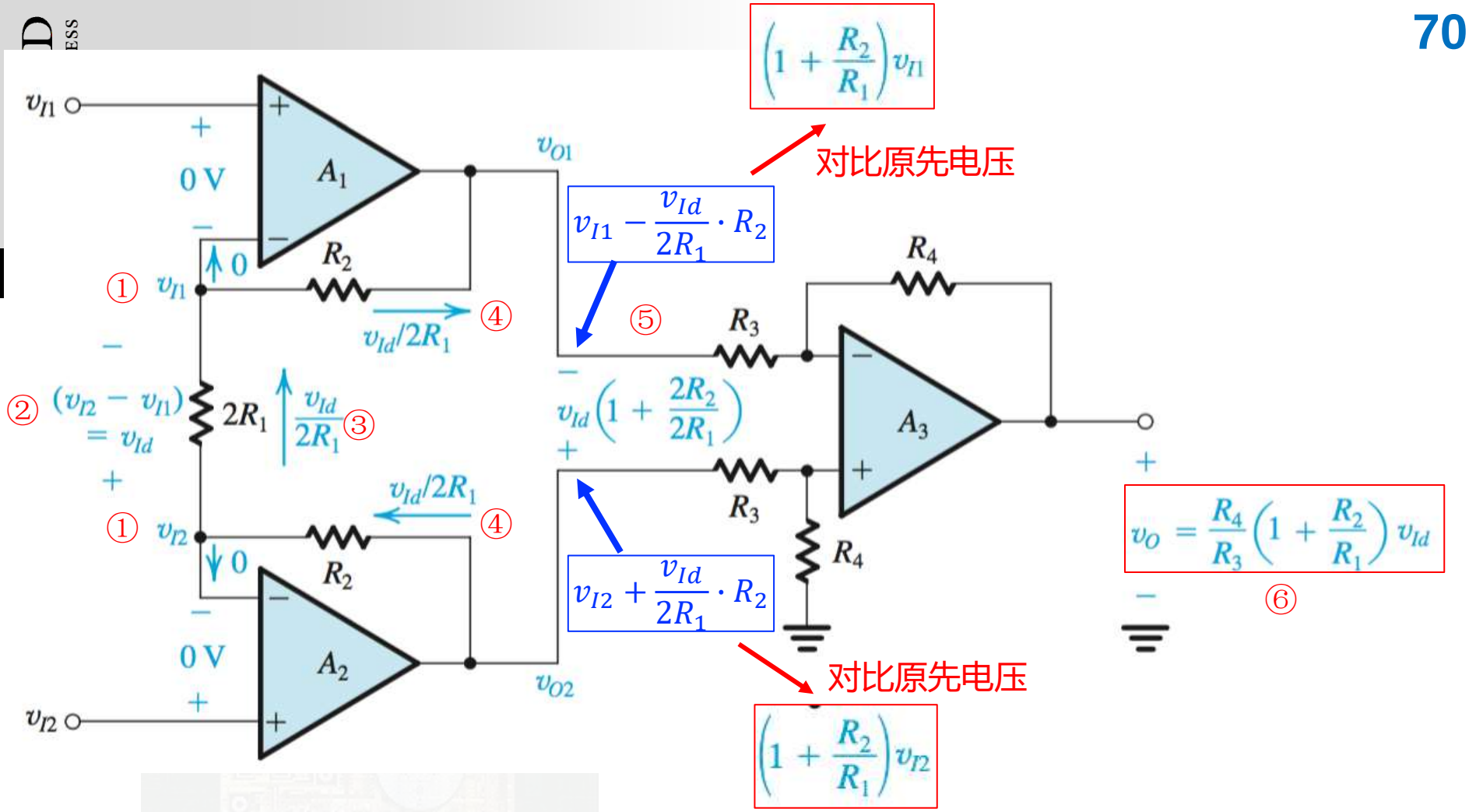
仅仅是简单地将X点的接地去掉，就能解决上述问题！【巧妙的工程实现】



2.4.2. The Instrumentation Amplifier

- **Q:** How can one analyze this circuit?





共模信号输入呢？

流经$2R_1$的电流为零 → 流经R_2的电流也为零 → A_1、A_2的输出电压即V_{I1}、V_{I2} → 第一级没有对共模信号进行放大！

Design the instrumentation amplifier circuit in Fig. 2.20(b) to provide a gain that can be varied over the range of 2 to 1000 utilizing a 100-kΩ variable resistance (a potentiometer, or "pot" for short).

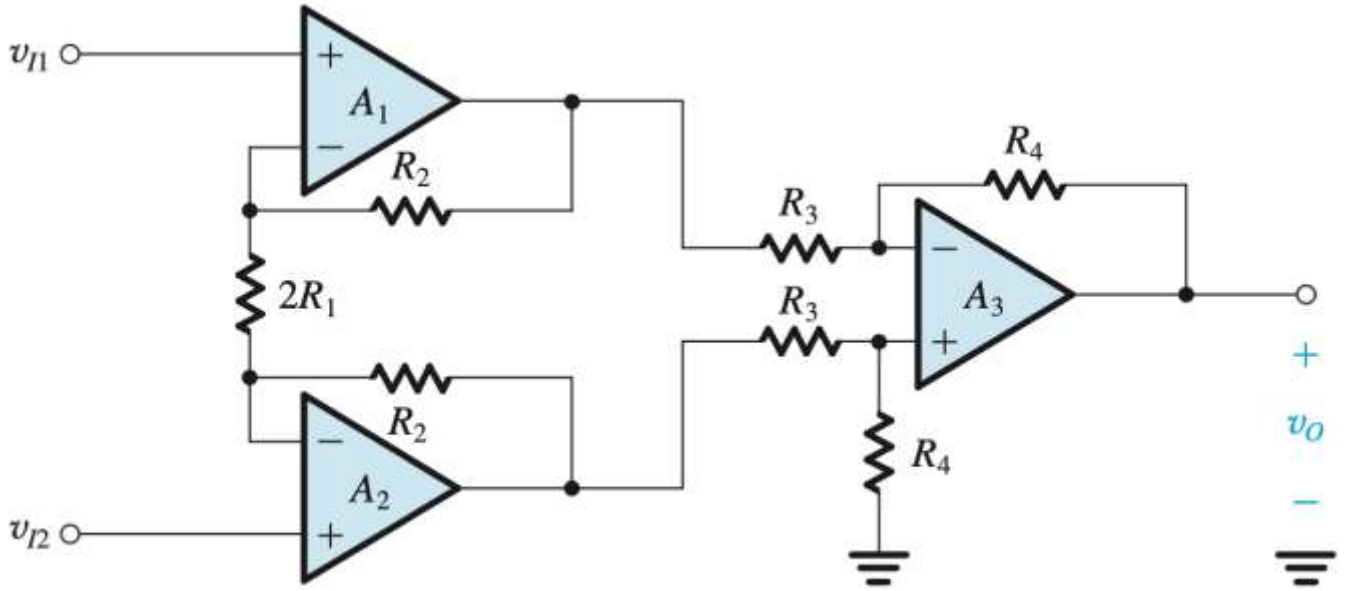
Solution

第一级实现增益

第一级实现共模抑制

It is usually preferable to obtain all the required gain in the first stage, leaving the second stage to perform the task of taking the difference between the outputs of the first stage and thereby rejecting the common-mode signal. In other words, the second stage is usually designed for a gain of 1. Adopting this approach, we select

把第二级增益设定为1



(b)

all the second-stage resistors to be equal to a practically convenient value, say 10 kΩ. The problem then reduces to designing the first stage to realize a gain adjustable over the range of 2 to 1000. Implementing $2R_1$ as the series combination of a fixed resistor R_{1f} and the variable resistor R_{1v} obtained using the 100-kΩ pot (Fig. 2.21), we can write

10 kΩ 是常用电阻

$$1+\frac{2R_2}{R_{1f}+R_{1v}}=2 \text{ to } 1000$$

Thus,

$$1+\frac{2R_2}{R_{1f}}=1000$$

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right)$$

and

$$1+\frac{2R_2}{R_{1f}+100\,\text{k}\Omega}=2$$

These two equations yield $R_{1f}=100.2\ \Omega$ and $R_2=50.050\ \text{k}\Omega$. Other practical values may be selected; for instance, $R_{1f}=100\ \Omega$ and $R_2=49.9\ \text{k}\Omega$ (both values are available as standard 1%-tolerance metal-film resistors; see Appendix J) results in a gain covering approximately the required range.

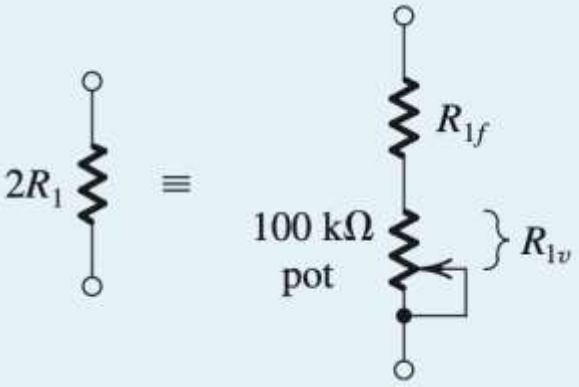


Figure 2.21 To make the gain of the circuit in Fig. 2.20(b) variable, $2R_1$ is implemented as the series combination of a fixed resistor R_{1f} and a variable resistor R_{1v}. Resistor R_{1f} ensures that the maximum available gain is limited.

2.5. Integrators and Differentiators 积分电路 & 微分电路

- **integrator / differentiator amplifier** – is one which outputs an integral or derivative of the input signal.

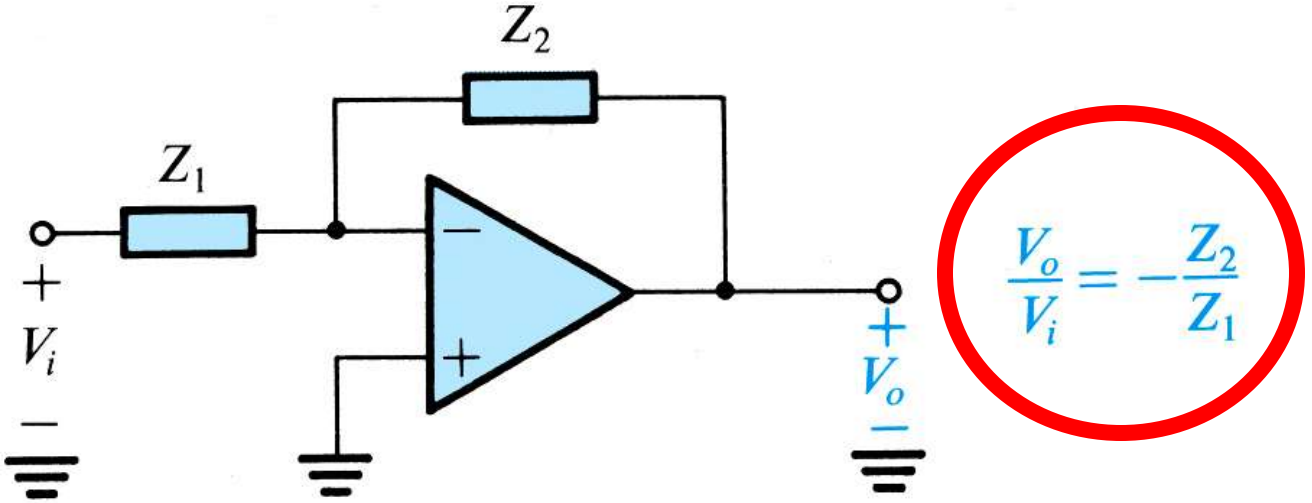
用模拟电路来实现积分、微分、加减法运算，这就是“运算”放大器名称的由来

In earlier days we use Analog computers using adders, integrators and multipliers.

Now Simulink (in MatLab) simulates an Analog computer using a digital computer.

2.5.1. The Inverting Configuration with General Impedances

- **Q:** Does the transfer function for the inverting op amp change if the feedback and input impedances are not purely resistive? 在反相接法中，若将电阻换成更普遍的阻抗，会如何？
  - **A:** 增益形式不变，只需将R替换成Z



一阶电路特性回顾

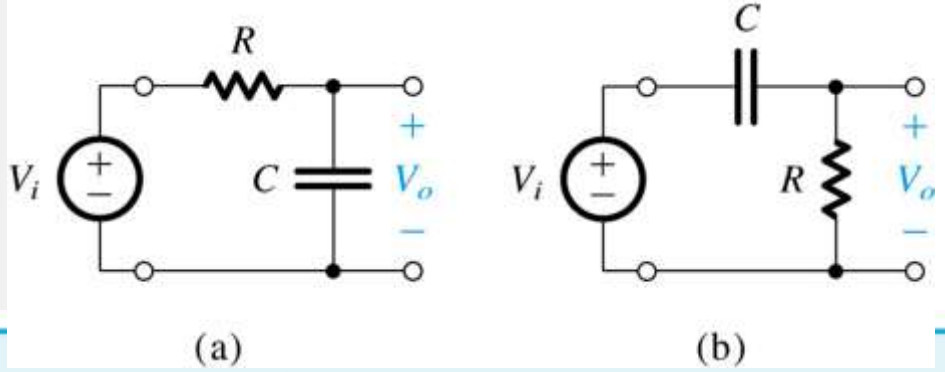


Table 1.2 Frequency Response of STC Networks

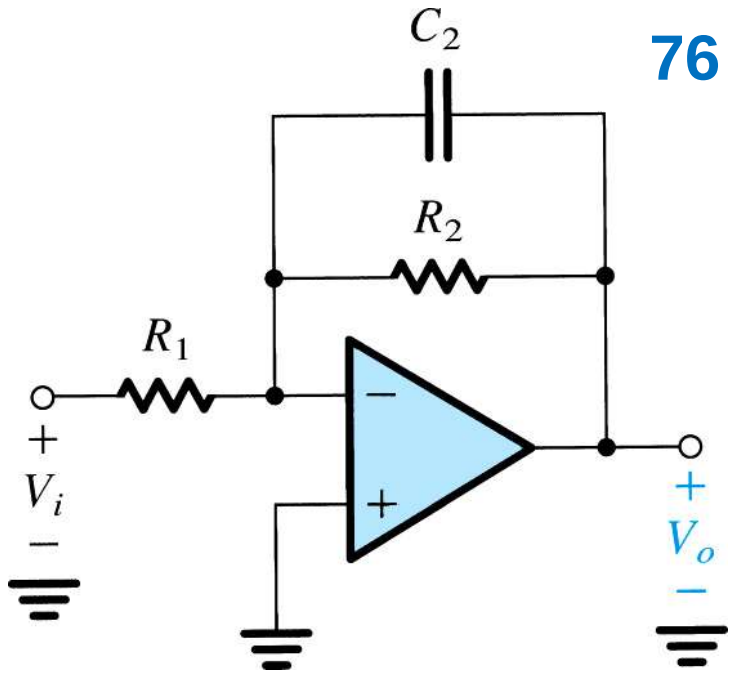
$s = j\omega$

	低通STC Low-Pass (LP)	高通STC High-Pass (HP)
Transfer Function $T(s)$ 传递函数标准形式	$\dfrac{K}{1+(s/\omega_0)}$	$\dfrac{Ks}{s+\omega_0}$
Transfer Function (for physical frequencies) $T(j\omega)$	$\dfrac{K}{1+j(\omega/\omega_0)}$	$\dfrac{K}{1-j(\omega_0/\omega)}$
Magnitude Response $\lvert T(j\omega)\rvert$	$\dfrac{\lvert K\rvert}{\sqrt{1+(\omega/\omega_0)^2}}$	$\dfrac{\lvert K\rvert}{\sqrt{1+(\omega_0/\omega)^2}}$
Phase Response $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega = 0$ (dc)	K	0
Transmission at $\omega = \infty$	0	K
3-dB Frequency	$\omega_0 = 1/\tau$; $\tau \equiv$ time constant $\tau = CR$ or L/R	
Bode Plots	in Fig. 1.23	in Fig. 1.24

$\dfrac{\dfrac{1}{j\omega C}}{R+\dfrac{1}{j\omega C}}$

$\dfrac{R}{R+\dfrac{1}{j\omega C}}$

Example 2.4: Other Op-Amp Configurations 例题



- 考虑右边的电路
- **Q(a):** Derive an expression for the transfer function v_{Out} / v_{In}. 求传输函数的表达式
- **Q(b):** Show that the transfer function is of a low-pass STC circuit. 验证传输函数是低通STC电路
- **Q(c):** By expressing the transfer function in standard form of Table 1.2, find the dc-gain and 3dB frequency. 用STC的标准表达式，计算直流增益和3dB频率

Example 2.4: Other Op-Amp Configurations

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{Z_1(s)Y_2(s)}$$

$Z_1 = R_1$ and $Y_2(s) = (1/R_2) + sC_2$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + sC_2R_2}$$

$$\frac{K}{1 + (s/\omega_0)} \qquad K = -\frac{R_2}{R_1} \qquad \omega_0 = \frac{1}{C_2R_2}$$

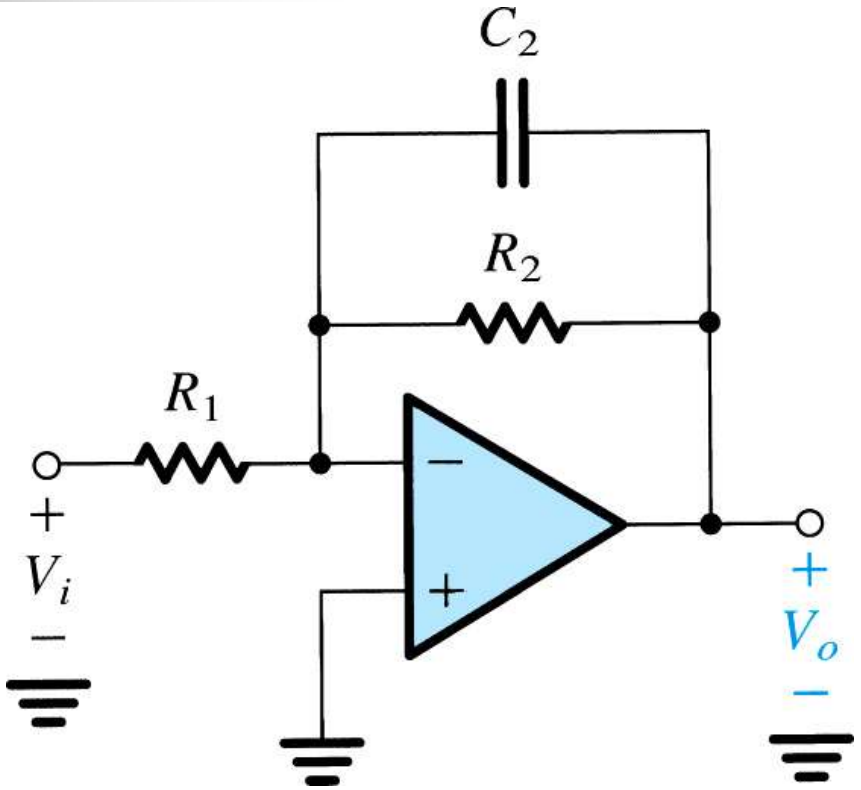
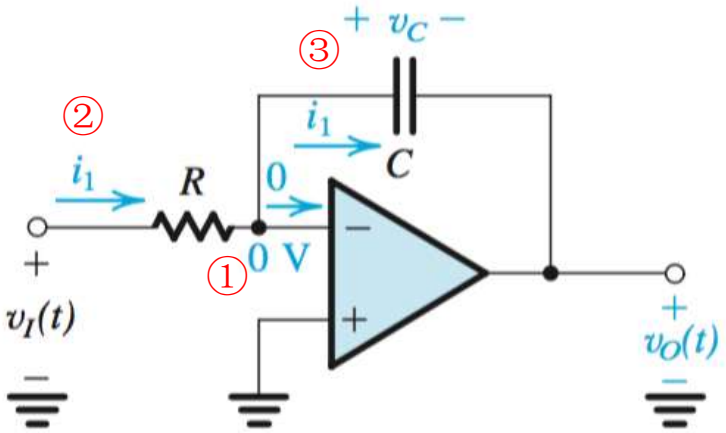


Figure 2.23: Circuit for Example 2.4.

2.5.2. The Inverting Integrator 反相积分电路

- **Q:** How can inverting op-amp be adapted to perform integration? 如何用反相接法的运放实现积分功能
  - **A:** Utilization of capacitor as feedback impedance.
  - 利用电容作为反馈阻抗



(a)

④

$$v_O(t) = -\frac{1}{CR}\int_0^t v_I(t)\,dt - V_C$$ 时域

$$\frac{V_o}{V_i} = -\frac{1}{sCR}$$ 频域

CR称为积分器的时间常数

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{sCR}$$

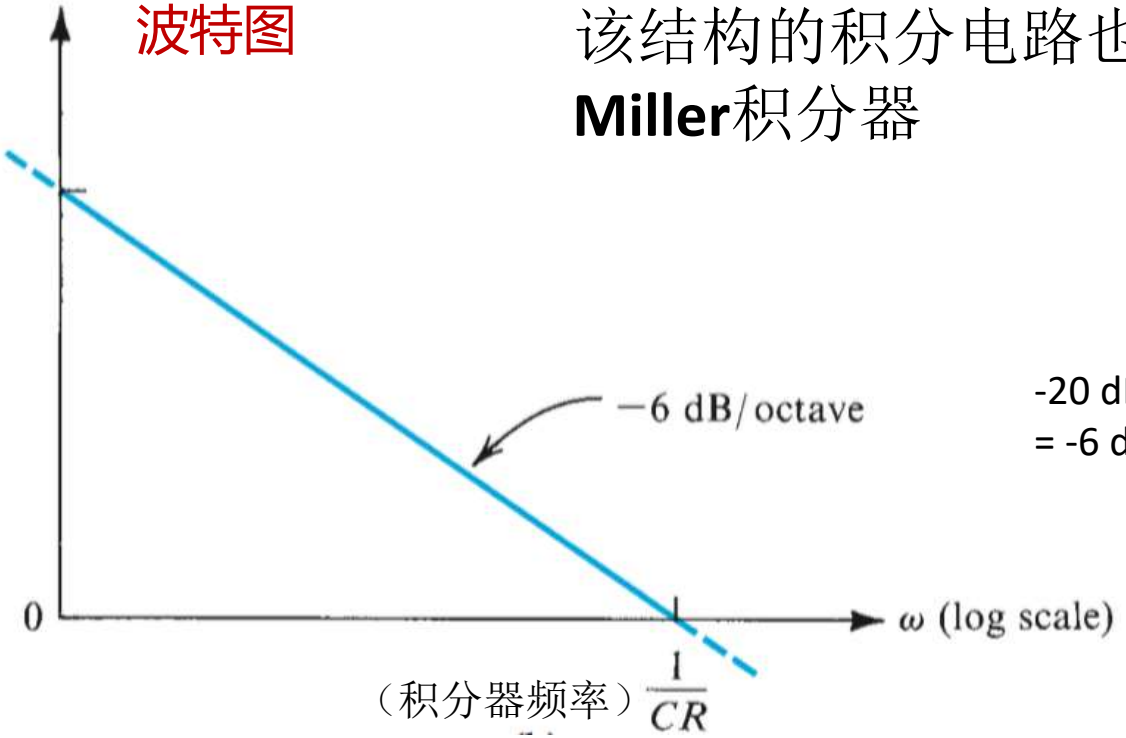
$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\omega CR}$$

$$\phi = +90°$$

$\left|\frac{V_o}{V_i}\right|$ (dB)

波特图



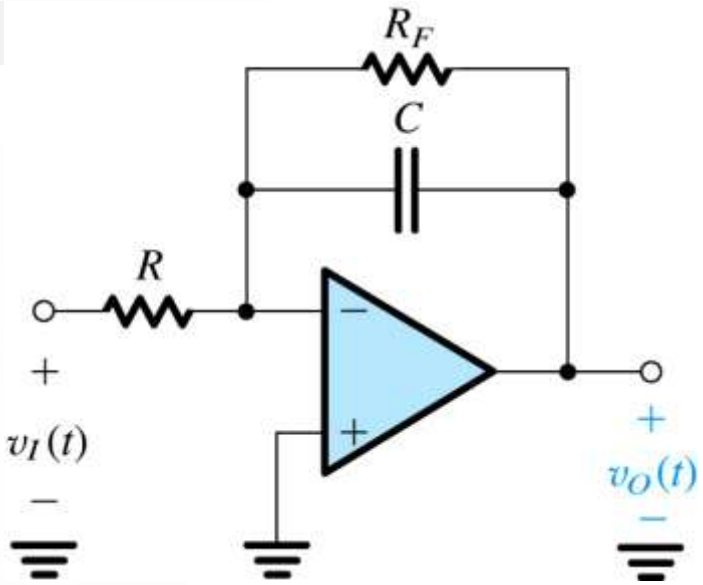
该结构的积分电路也被称为**Miller**积分器

-20 dB/十倍频
= -6 dB/两倍频

2.5.2. The Inverting Integrator

- **Q:** What is the problem with this configuration (related to dc gain)? 存在的问题
  - **A:** At dc frequency ($\omega = 0$), gain is infinite 低频增益∞
  - Gain = $1 / (\omega R_1 C_F)$
- **Q:** Solution? 解决的办法
  - **A:** By placing a very large resistor in parallel with the capacitor, negative feedback is employed to make dc gain "finite." 用一个大电阻并联反馈电容

Figure 2.25: The Miller integrator with a large resistance *RF* connected in parallel with *C* in order to provide negative feedback and hence finite gain at dc.



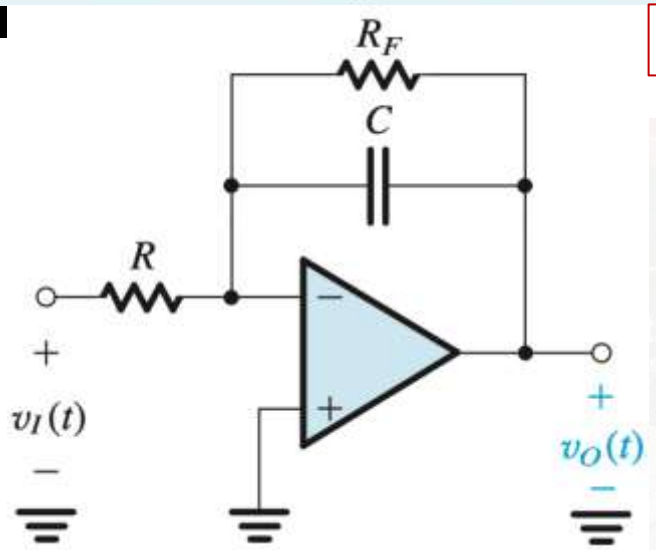
就是前面例题2.4的情况

$$\frac{V_o(s)}{V_i(s)} = -\frac{R_F/R}{1+sCR_F}$$

但引入R_F后，积分特性变得不完美了！

因此，R_F的取值需在**dc性能**和信号**积分性能**之间取trade-off

Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.26(a)]. Let $R = 10\,\text{k}\Omega$ and $C = 10\,\text{nF}$. If the integrator capacitor is shunted by a 1-MΩ resistor, how will the response be modified? The op amp is specified to saturate at ± 13 V. 假设电容初始电压为0



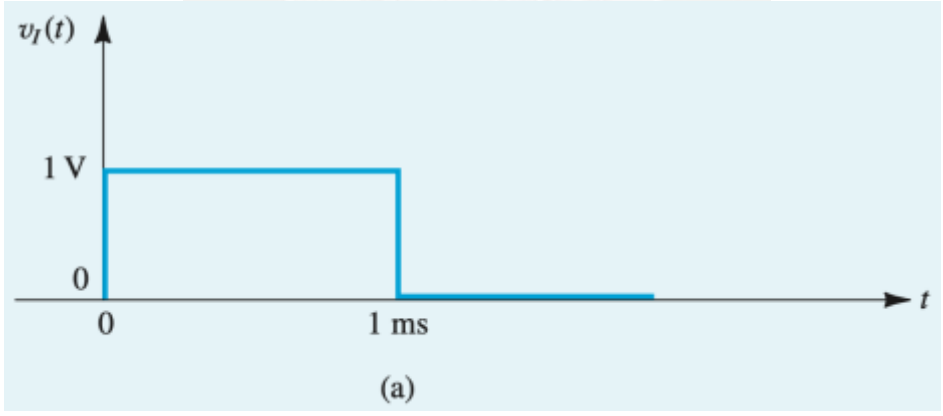
1. 没有 R_F 的情况

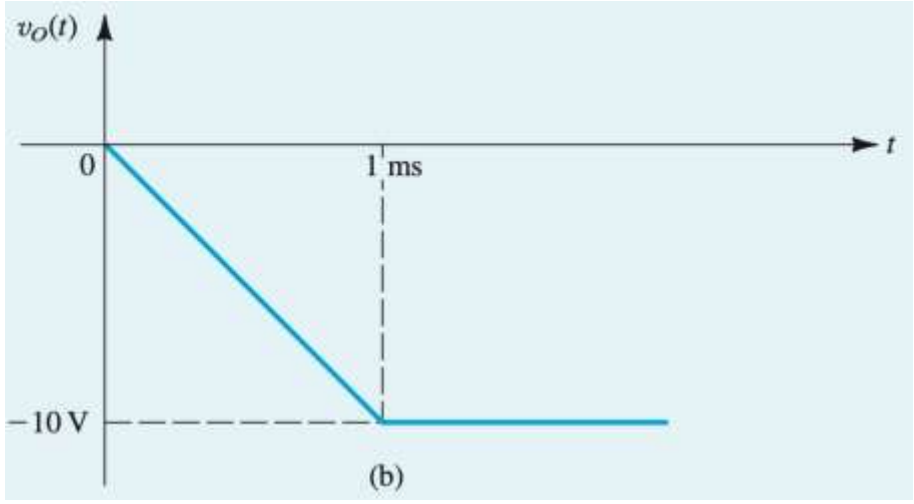
$$v_o(t) = -\frac{1}{CR}\int_0^t 1\,dt, \qquad 0 \le t \le 1\ \text{ms}$$

时间常数 ⇩ $CR = 0.1\ \text{ms}$

$$v_o(t) = -10t, \qquad 0 \le t \le 1\ \text{ms}$$

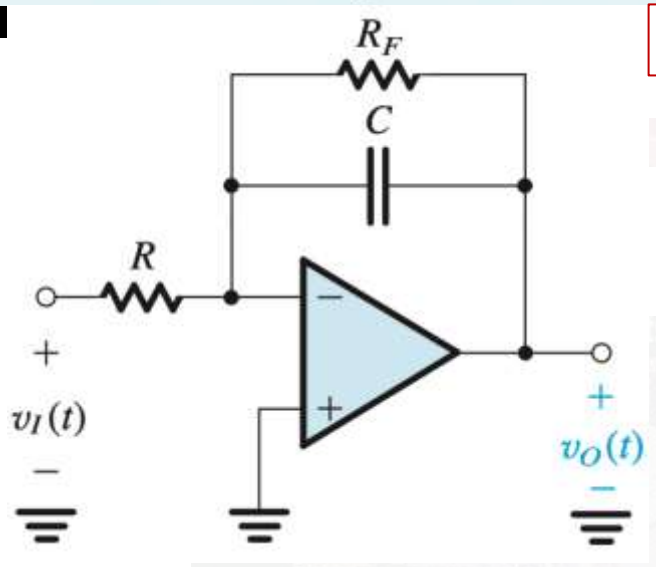
t 的单位是 ms





1 V 电压产生 0.1 mA 电流，对 C 进行充电

Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.26(a)]. Let $R = 10\,\text{k}\Omega$ and $C = 10\,\text{nF}$. If the integrator capacitor is shunted by a 1-MΩ resistor, how will the response be modified? The op amp is specified to saturate at ± 13 V. 假设电容初始电压为0



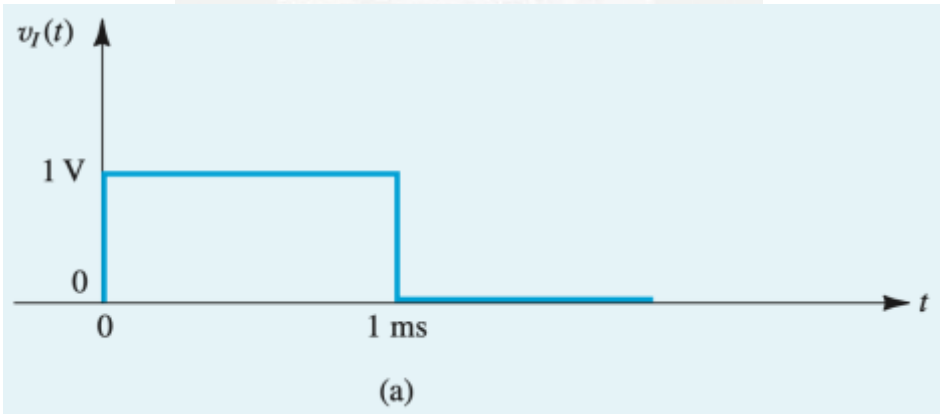
2. 有 R_F 的情况

1 V 电压产生 0.1 mA 电流，流入 C 和 R_F 网络

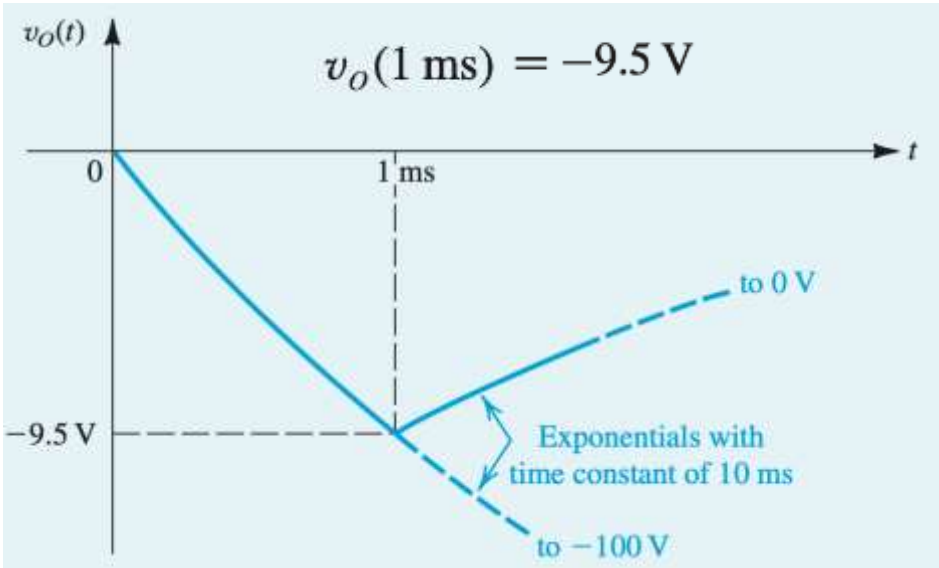
C的初始电压 0，稳态电压 0.1mA x R_F = 100 V，
时间常数 $\tau = R_F \times C = 10$ ms

$$v(t) = v(\infty) + [v(0) - v(\infty)]e^{-t/\tau}$$

$$v_o(t) = -100(1 - e^{-t/10}), \qquad 0 \le t \le 1\ \text{ms}$$



从方波产生三角波



2.5.3. The Op-Amp Differentiator 微分电路

- **Q:** How can one adapt integrator to perform differentiation? 如何构建微分电路呢？
  - **A:** Interchange locations of resistors and capacitors.
  - 将积分电路的R和C交换，即可实现微分电路

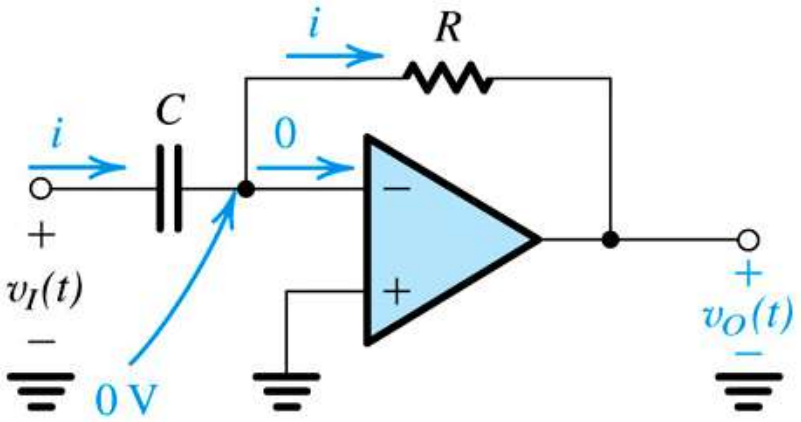
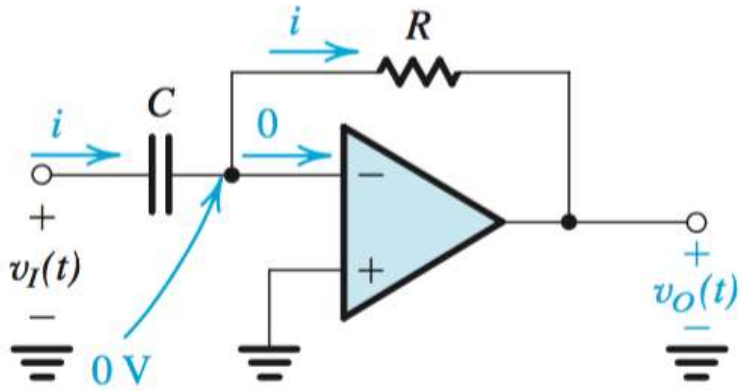


Figure 2.27: A differentiator.



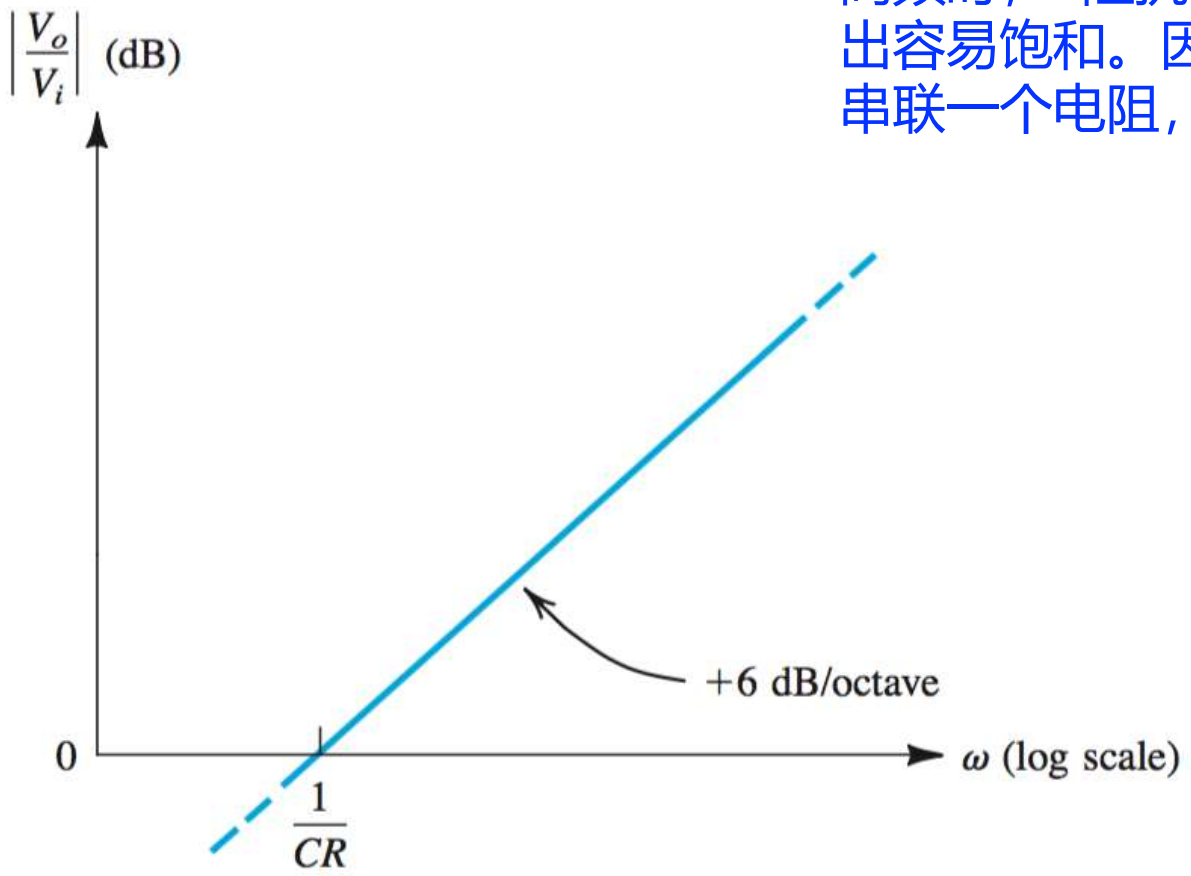
$$i(t) = C\frac{dv_I(t)}{dt}$$

$$v_O(t) = -CR\frac{dv_I(t)}{dt}$$

$$\frac{V_o}{V_i} = -sCR$$

(a)

高频时，C阻抗很小，增益很大，输出容易饱和。因此常常在输入端与C串联一个电阻，以抑制高频增益



2.5.3. The Op-Amp Differentiator

- filtering characteristic is high pass filter
- magnitude of transfer function is $|V_{Out} / V_{In}| = \omega R_F C_1$
- phase of transfer function is $\phi = -90^O$
- differentiator time-constant is frequency at which unity gain occurs and defined as $\omega = 1 / R_F C_1$
- **Q:** What is the problem with differentiator?
  - **A:** Differentiator acts as noise amplifier, exhibiting large changes in output from small (but fast) changes in input. As such, it is **rarely used in practice**.
  - 输入有突变，则输出无穷大

补充说明

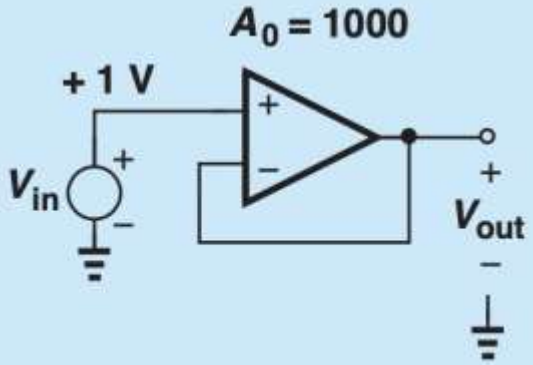
- Op amp 输入端电压相等只是在开环增益为无穷大的理想情况下成立，若开环增益为有限值，输入端电压差为“输出/开环增益”

The circuit shown in Fig. 8.3 is called a “unity-gain” buffer. Note that the output is tied to the inverting input. Determine the output voltage if $V_{in1} = +1$ V and $A_0 = 1000$.

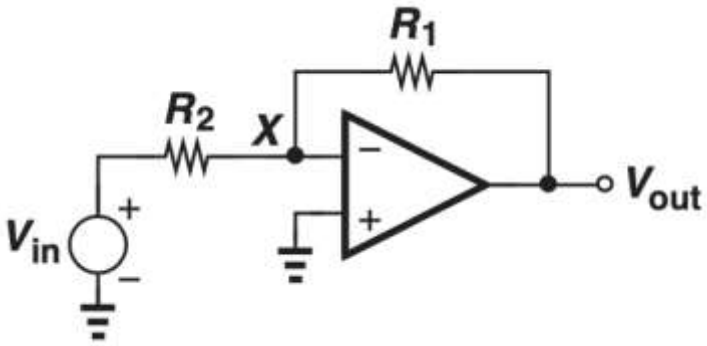
$$V_{out} = A_0(V_{in} - V_{out})$$

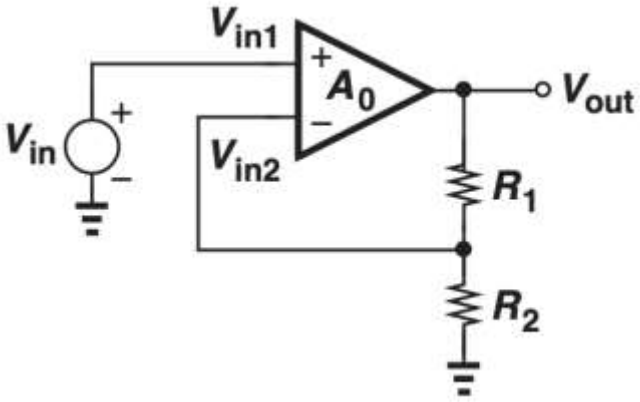
$$\Downarrow$$

$$V_{out} = 0.999 \text{ V}.$$



补充说明

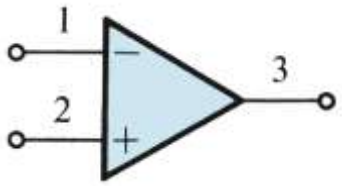




V_{in2} 看作 V_{out} 的分压

小结

- 运放的“电压电流约束关系”



$$v_3 = A(v_2 - v_1)$$

- 理想运放的特性

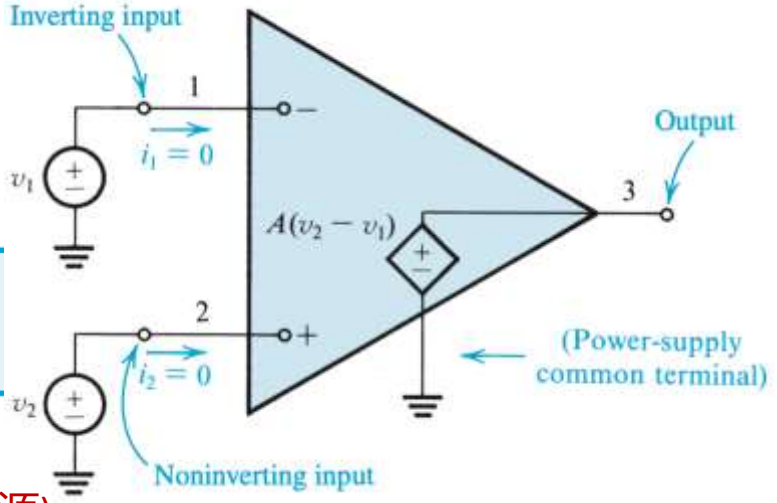
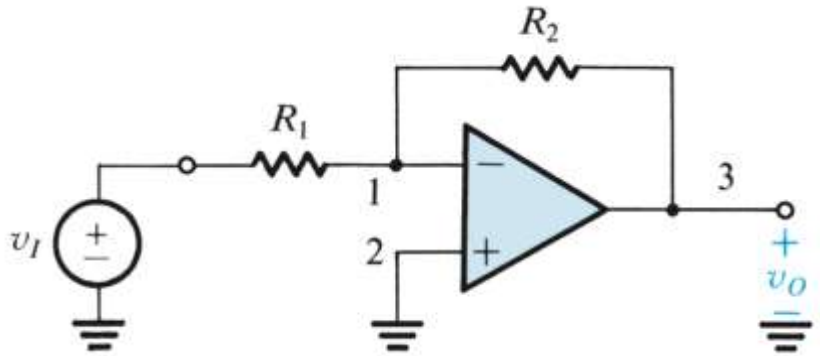


Table 2.1 Characteristics of the Ideal Op Amp

1. Infinite input impedance 输入阻抗无穷大
2. Zero output impedance 输出阻抗为0 (输出是理想电压源)
3. Zero common-mode gain or, equivalently, infinite common-mode rejection 共模增益为0
4. Infinite open-loop gain A 开环增益 A 无穷大
5. Infinite bandwidth 带宽无穷大

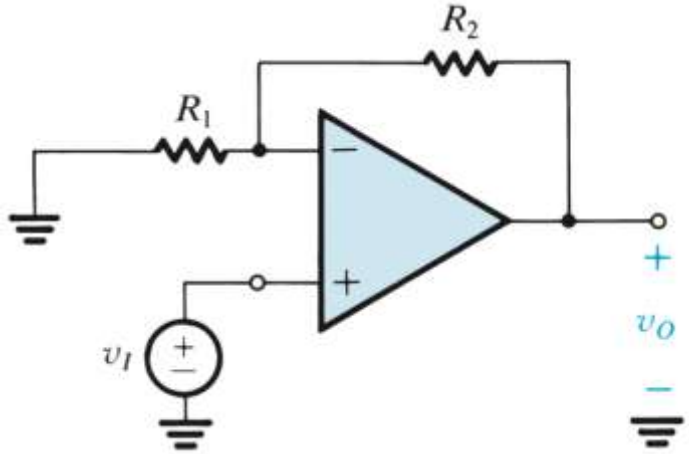
- **Inverting Configuration**



$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}$$

$$R_i \equiv \frac{v_I}{i_1} = \frac{v_I}{v_I/R_1} = R_1 \qquad R_o = 0$$

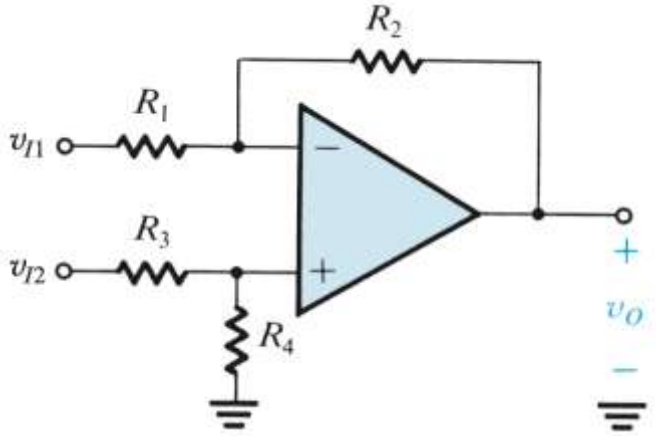
- **Noninverting Configuration**



$$\frac{v_O}{v_I} = 1 + \frac{R_2}{R_1}$$

$$R_i = \infty \qquad R_o = 0$$

- **差分放大器**

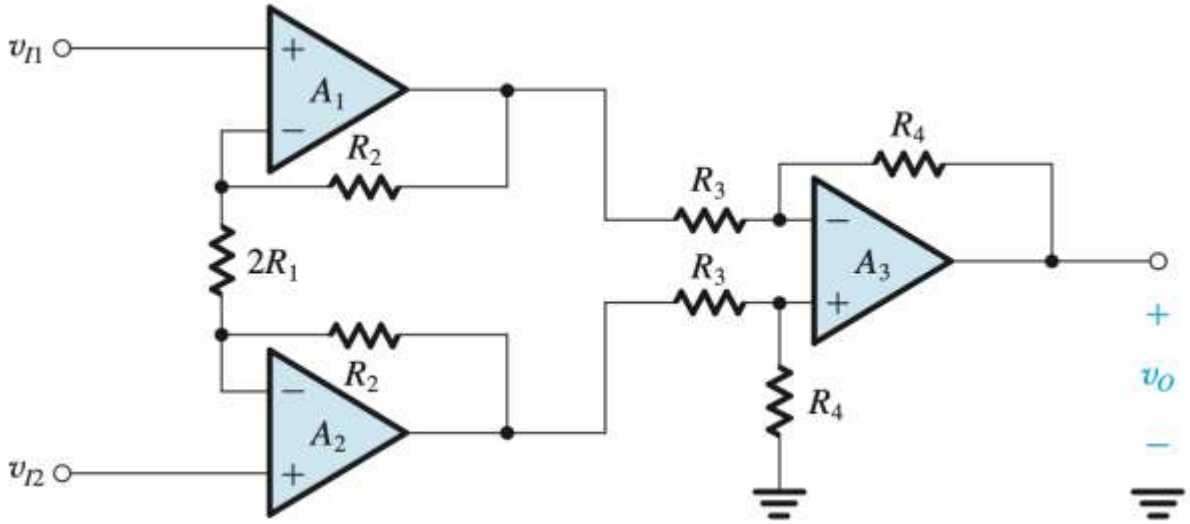


$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

$$A_d = \frac{R_2}{R_1}$$

$$R_{id} = 2R_1 \qquad R_o = 0$$

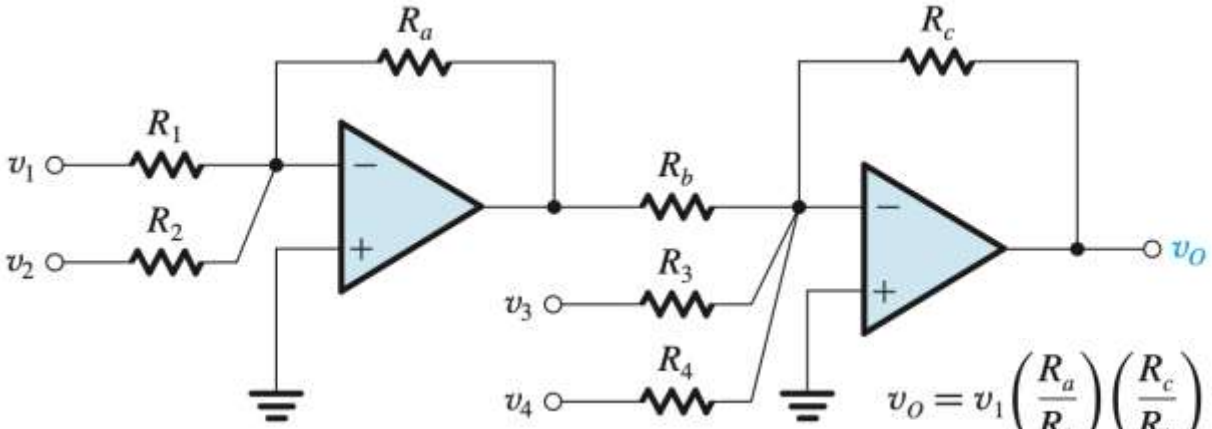
- **仪表放大器**



$$A_d = \left(\frac{R_4}{R_3}\right)\left(1 + \frac{R_2}{R_1}\right)$$

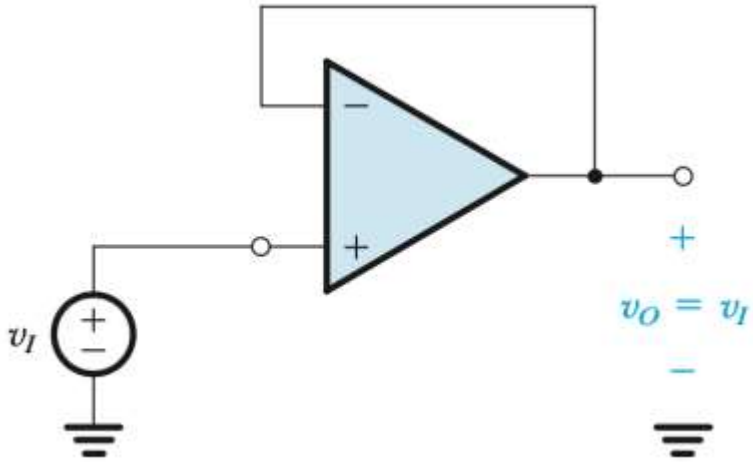
$$R_i = \infty \qquad R_o = 0$$

- **应用 1：加法**

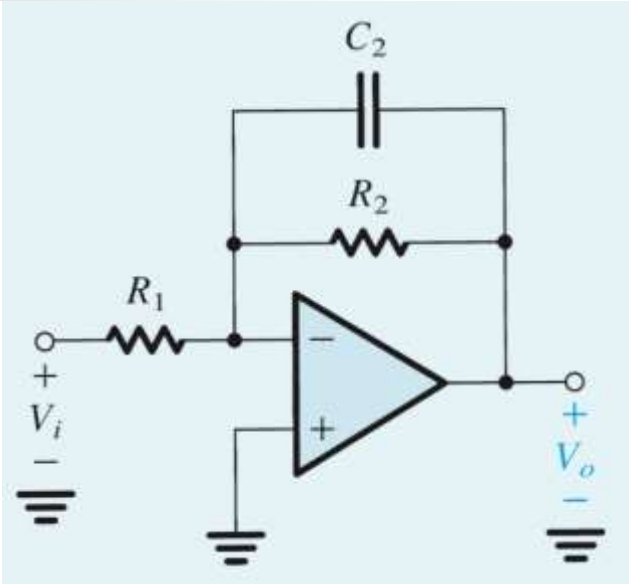


$$v_O = v_1\left(\frac{R_a}{R_1}\right)\left(\frac{R_c}{R_b}\right) + v_2\left(\frac{R_a}{R_2}\right)\left(\frac{R_c}{R_b}\right) - v_3\left(\frac{R_c}{R_3}\right) - v_4\left(\frac{R_c}{R_4}\right)$$

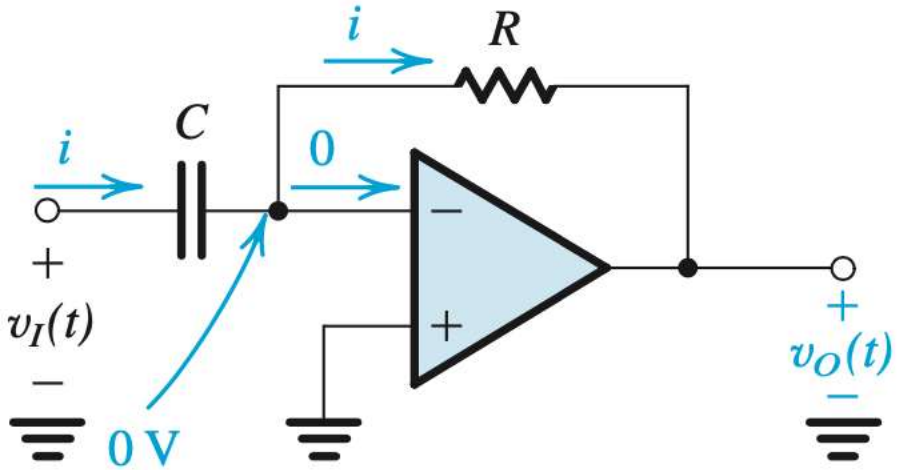
- **应用2：Buffer**



- **应用 3：积分**



- **应用4：微分**



$$i(t) = C\frac{dv_I(t)}{dt}$$

$$v_O(t) = -CR\frac{dv_I(t)}{dt}$$

$$\frac{V_o}{V_i} = -sCR$$

作业

EXERCISES

2.6 For the circuit in Fig. E2.6 determine the values of v_1, i_1, i_2, v_O, i_L, and i_O. Also determine the voltage gain v_O/v_I, current gain i_L/i_I, and power gain P_O/P_I.

Ans. 0 V; 2 mA; 2 mA; −10 V; −10 mA; −12 mA; −5 V/V (14 dB); −5 A/A (14 dB); 25 W/W (14 dB)

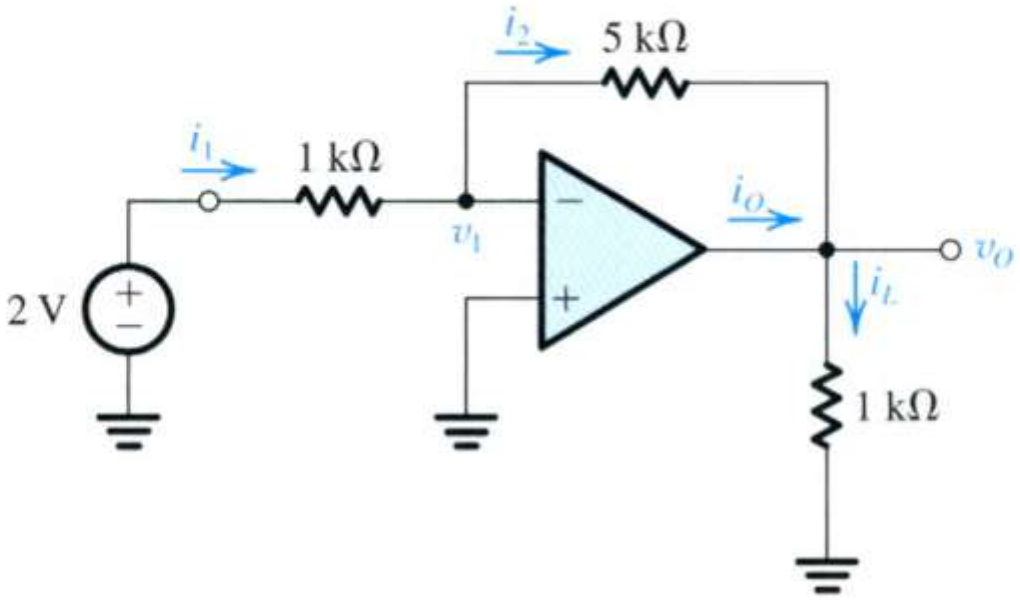


Figure E2.6

D2.8 Use the idea presented in Fig. 2.11 to design a weighted summer that provides

$$v_O = 2v_1 + v_2 - 4v_3$$

10 kΩ 是常用电阻

Ans. A possible choice: $R_1 = 5\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$, $R_a = 10\,\text{k}\Omega$, $R_b = 10\,\text{k}\Omega$, $R_3 = 2.5\,\text{k}\Omega$, $R_c = 10\,\text{k}\Omega$

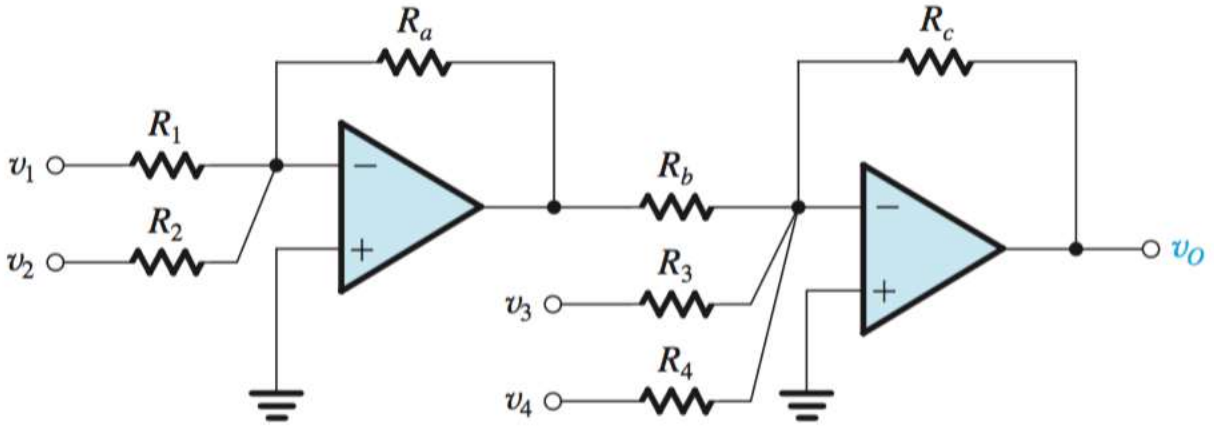


Figure 2.11 A weighted summer capable of implementing summing coefficients of both signs.

D2.11 Design a noninverting amplifier with a gain of 2. At the maximum output voltage of 10 V the current in the voltage divider is to be 10 μA.

Ans. $R_1 = R_2 = 0.5\ \text{M}\Omega$

D2.16 Find values for the resistances in the circuit of Fig. 2.16 so that the circuit behaves as a difference amplifier with an input resistance of 20 kΩ and a gain of 10.

Ans. $R_1 = R_3 = 10\ \text{k}\Omega$; $R_2 = R_4 = 100\ \text{k}\Omega$

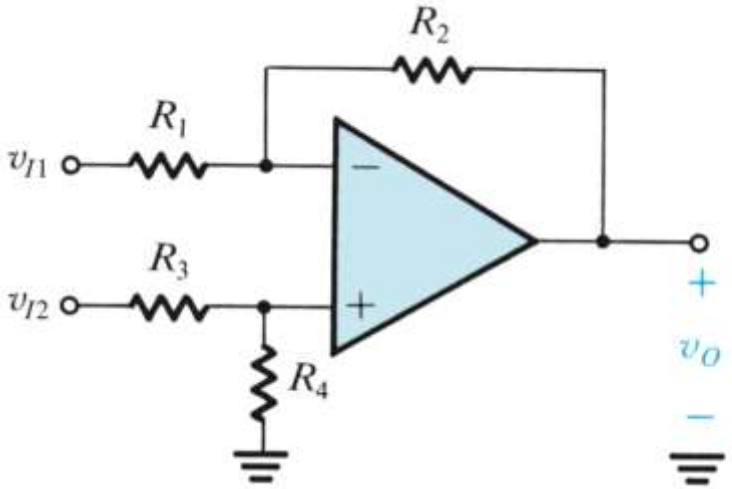
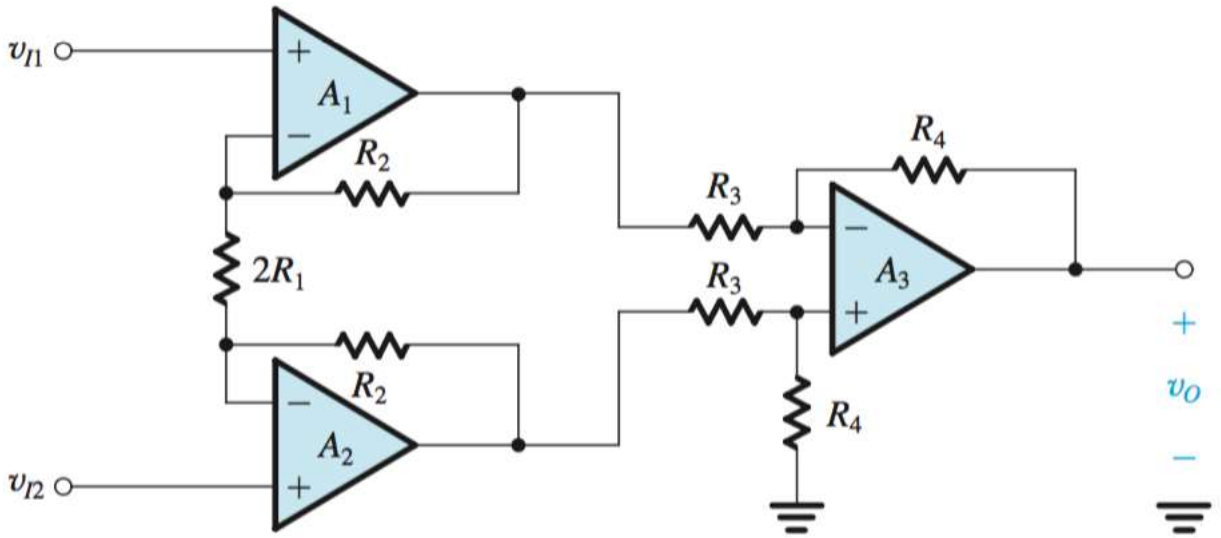


Figure 2.16 A difference amplifier.

2.17 Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of +5 V (dc) and a differential input signal of 10-mV-peak sine wave. Let $(2R_1) = 1\ \text{k}\Omega$, $R_2 = 0.5\ \text{M}\Omega$, and $R_3 = R_4 = 10\ \text{k}\Omega$. Find the voltage at every node in the circuit.

Ans. $v_{I1} = 5 - 0.005\sin\omega t$; $v_{I2} = 5 + 0.005\sin\omega t$; v_- (op amp A_1) $= 5 - 0.005\sin\omega t$; v_- (op amp A_2) $= 5 + 0.005\sin\omega t$; $v_{O1} = 5 - 5.005\sin\omega t$; $v_{O2} = 5 + 5.005\sin\omega t$; $v_-(A_3) = v_+(A_3) = 2.5 + 2.5025\sin\omega t$; $v_O = 10.01\sin\omega t$ (all in volts)



(b)

D2.19 Use an ideal op amp to design an inverting integrator with an input resistance of 10 kΩ and an integration time constant of 10^{-3} s. What is the gain magnitude and phase angle of this circuit at 10 rad/s and at 1 rad/s? What is the frequency at which the gain magnitude is unity?

Ans. $R = 10$ kΩ, $C = 0.1$ μF; at $\omega = 10$ rad/s: $|V_o/V_i| = 100$ V/V and $\phi = +90°$; at $\omega = 1$ rad/s: $|V_o/V_i| = 1000$ V/V and $\phi = +90°$; 1000 rad/s