Lecture 22 差分放大器

- 1 一般考虑
- 2 三极管差分对
- 3 MOS差分对
- 4 Cascode 差分放大器
- 5 共模抑制
- 6 差分对 with Active Load

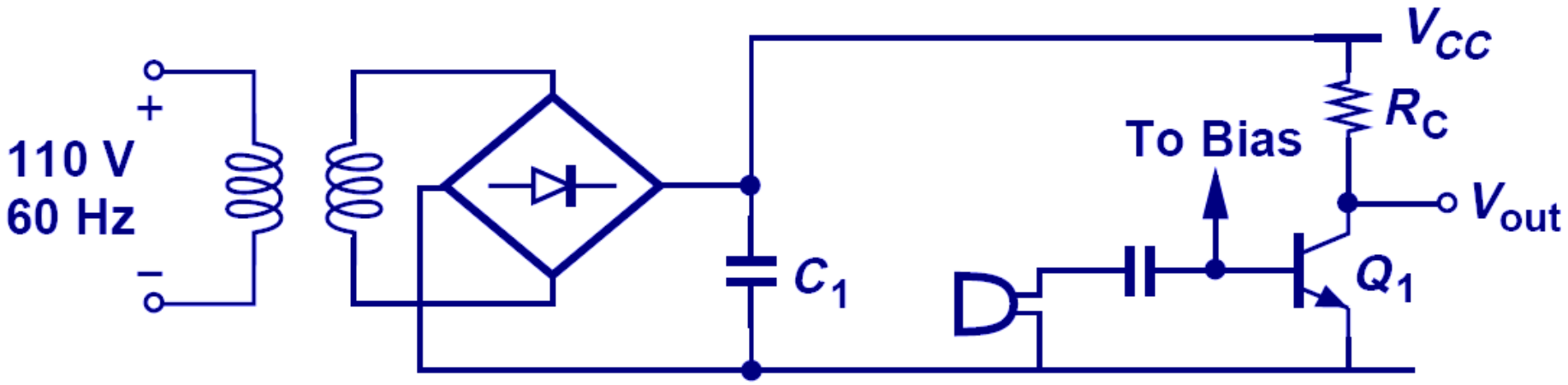
课程纲要

差分和多级放大器

- 差分放大器的结构及其分析
  - **10.1.1 BJT和MOS差分放大器的结构**
  - **10.1.2 大信号和小信号输入时的电路分析**
  - **10.1.3 差分放大器的非理想特性**
- 有源负载的作用及其应用（包含有源负载的**BJT和MOS**差分放大器的分析）
- 多级放大器的分析
  - **10.4.1 多级放大器的级联方式**
  - **10.4.2 多级放大器的增益计算**

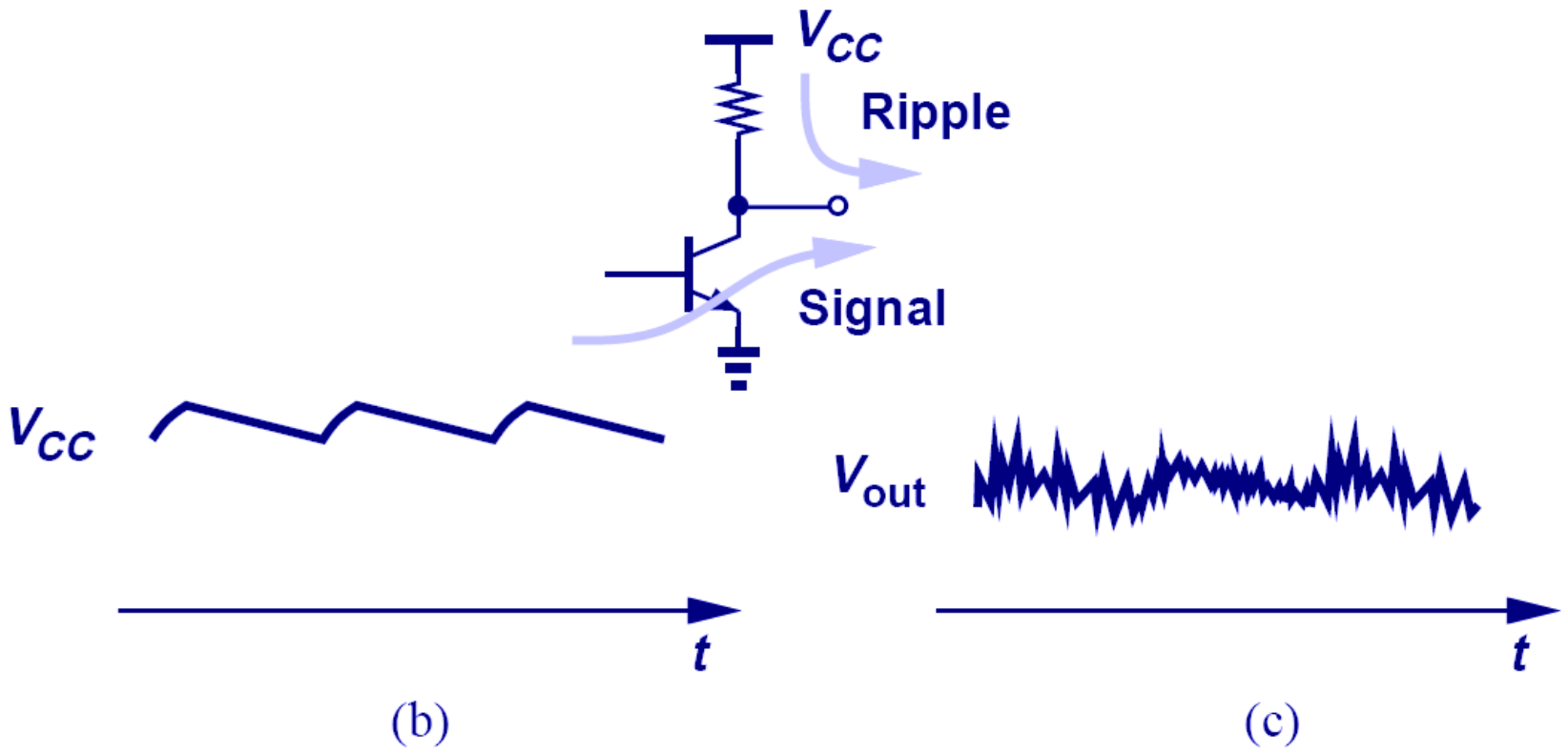
Audio Amplifier Example

Motivation:供电电压纹波



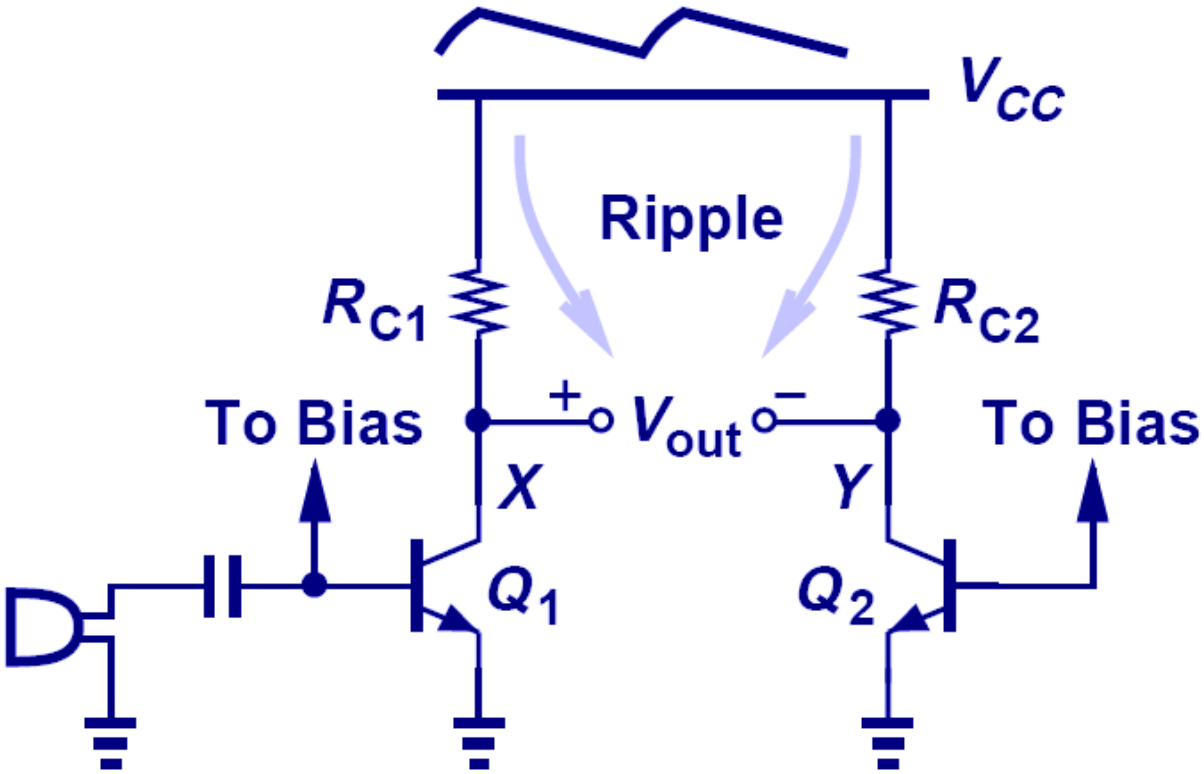
- 放大器的V_{CC}采用整流电路获得；
- 采用CE结构对麦克风的声音信号进行放大；

“Humming” Noise in Audio Amplifier Example



- 结果发现，输出信号有较强的“啸叫声”；
- 原因是二极管整流获得的 V_{CC} 具有ripple，而该ripple的频率为工频的两倍（100Hz），100Hz位于声音频带(20-20kHz)内，引起“啸叫声”；

Supply Ripple Rejection（供电电压波纹抑制）



小信号分析

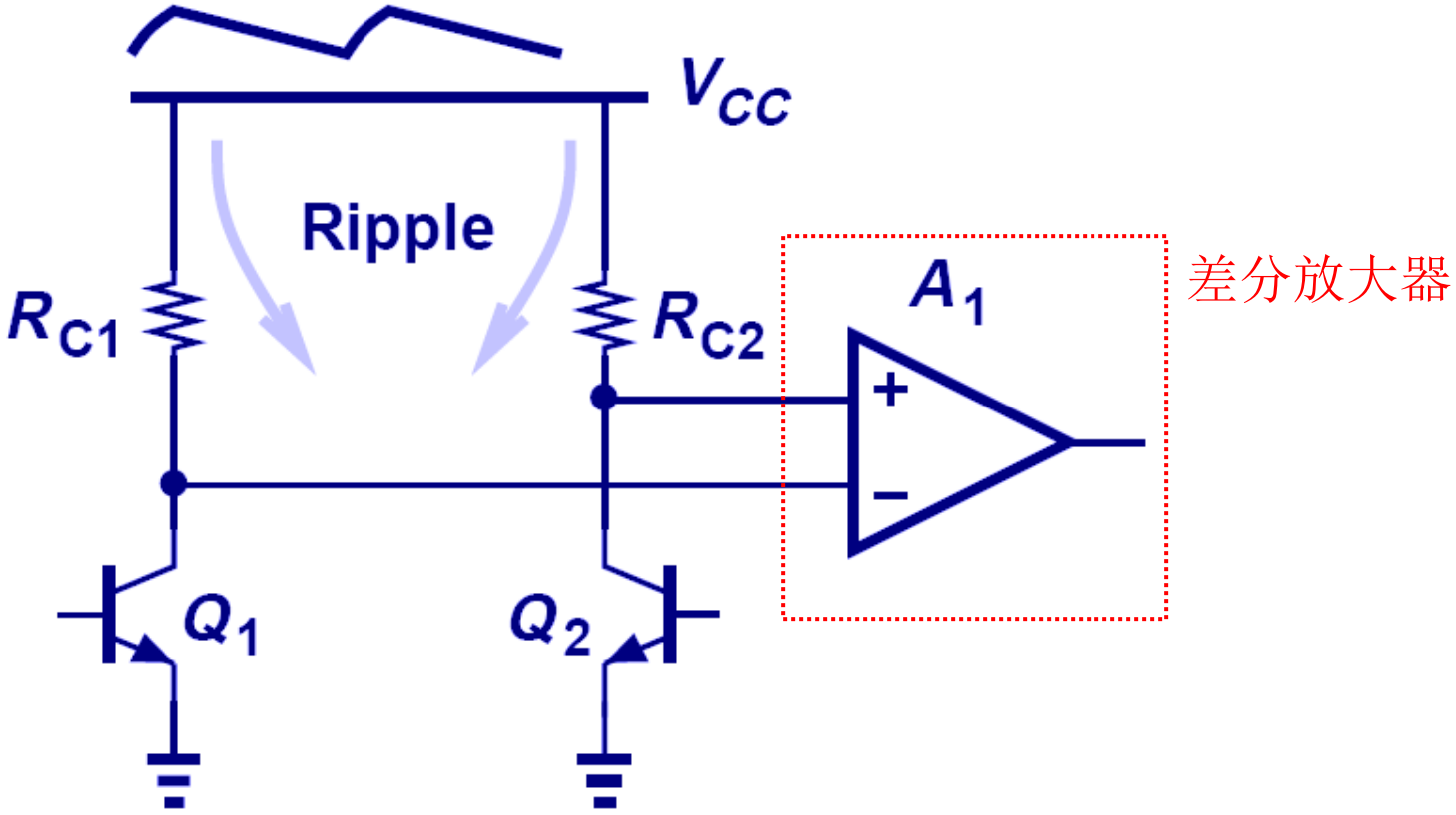
$$v_X = A_v v_{in} + v_r$$

$$v_Y = v_r$$

$$v_X - v_Y = A_v v_{in}$$

- 应用叠加原理，完整分析 = DC（供电电压无纹波） + 音频小信号 + 供电电压纹波（小信号）
- 虽然 X 点和 Y 点都受 V_{CC} 纹波（v_r）的影响，但 V_X-V_Y 与 V_{CC} 的纹波无关；

Ripple-Free Differential Output（无纹波的差分输出）

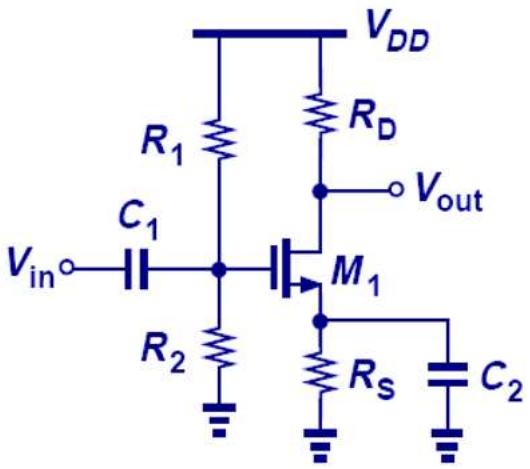


- 将两个结点的电压差作为信号（差分信号），因此，后续需要一个能对差分信号进行放大的放大器

Why Differential?

- **抗干扰强；**
  - 考虑两根靠得很近的差分信号线，外部干扰对它们的作用几乎是一样的（比如使两根线上的电压都增加Δv），而差分信号取两者之差，可以将干扰信号消除掉；

- **无需大电容（隔直电容 & 旁路电容）**



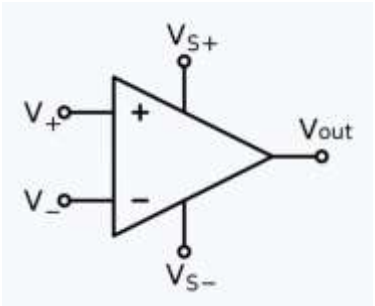
离散元件放大器电路中

1. 隔直电容C_1：直流开路（隔离前后级的直流偏置，使它们相互之间没有影响），交流短路（使信号可以无衰减地通过）
2. 旁路电容C_2：直流开路（直流偏置时Rs起作用，直流工作点更稳定），交流短路（小信号时Rs短路，保持CS的增益）

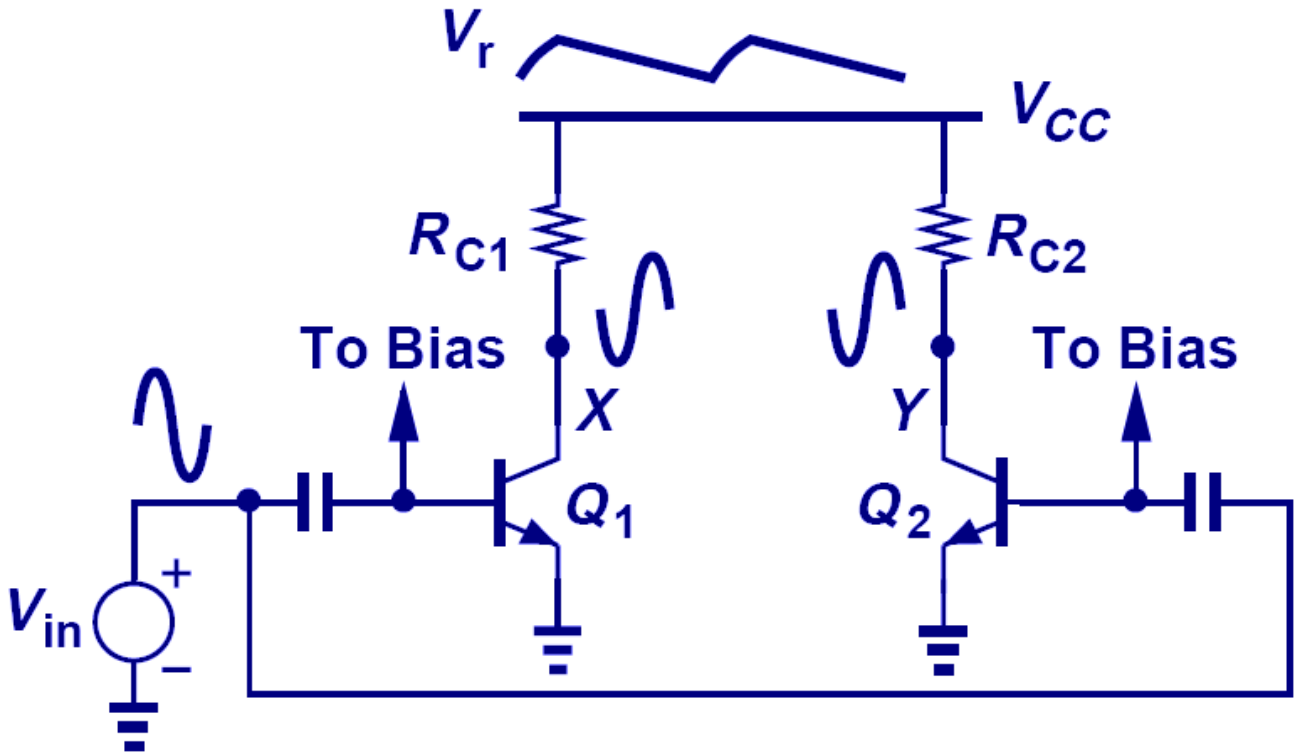
但集成电路中要尽量避免大电容 → 差分放大器

差分放大器尤其适合IC

- **差分放大器需要尽可能匹配**
  - 集成电路内部晶体管匹配的程度比分立电路晶体管要好很多（同一芯片内工艺参数变化较小）；
- **差分放大器元件的数量需要翻一倍**
  - 但集成电路中翻一倍的晶体管并不会增加多少成本
- **典型应用**
  - 运算放大器的输入级



差分放大器的共模输入



小信号分析

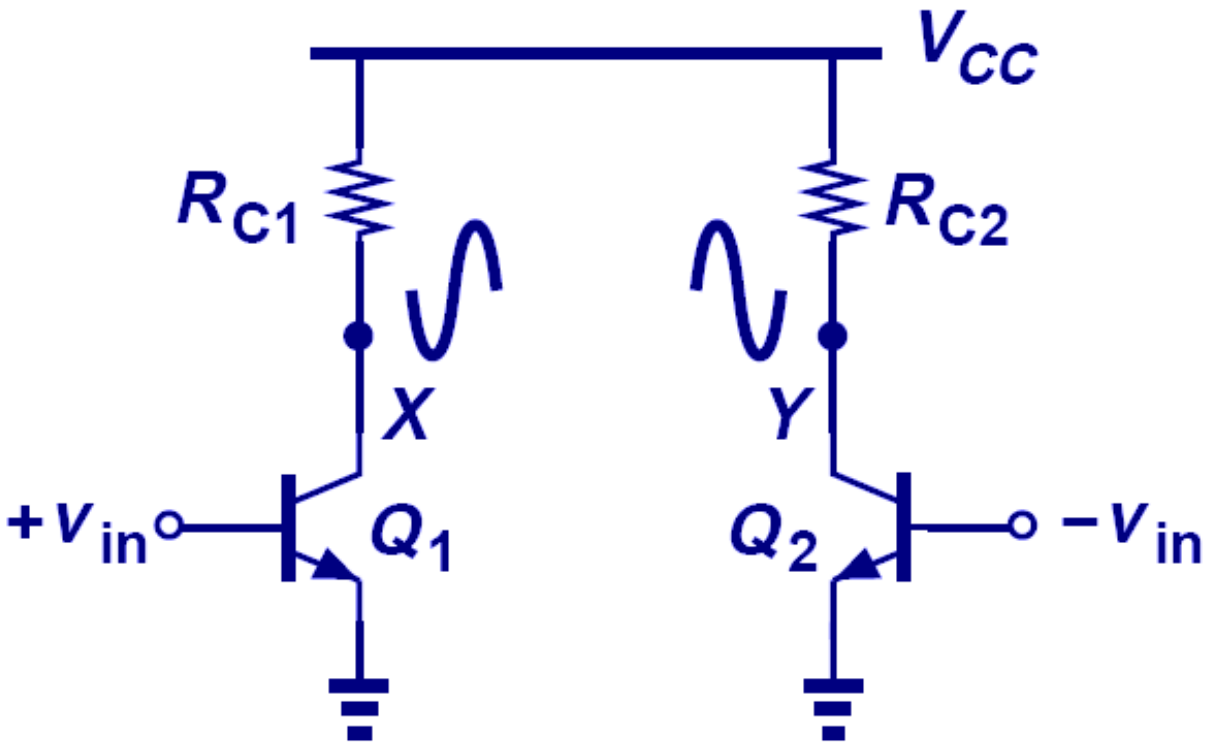
$$v_X = A_v v_{in} + v_r$$

$$v_Y = A_v v_{in} + v_r$$

$$v_X - v_Y = 0$$

- 若同幅同相的信号（共模信号）加到差分放大器的两个输入端，则在X和Y两个结点的信号也是同幅同相的， 也即没有差分输出；
- 共模输入 → 零差分输出，小信号时如此，大信号时也如此

差分放大器的差分输入



小信号分析

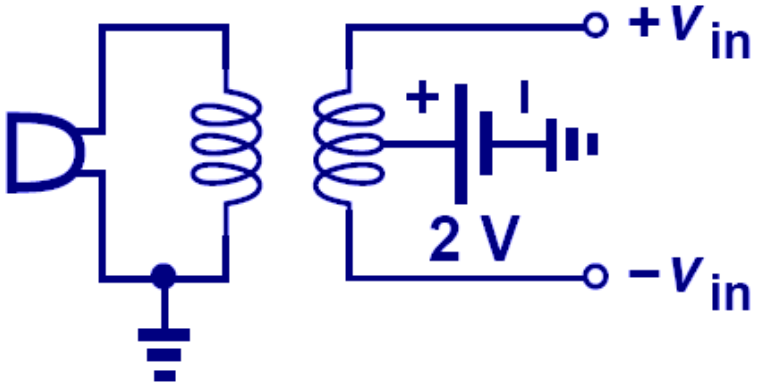
$$v_X = A_v v_{in} + v_r$$

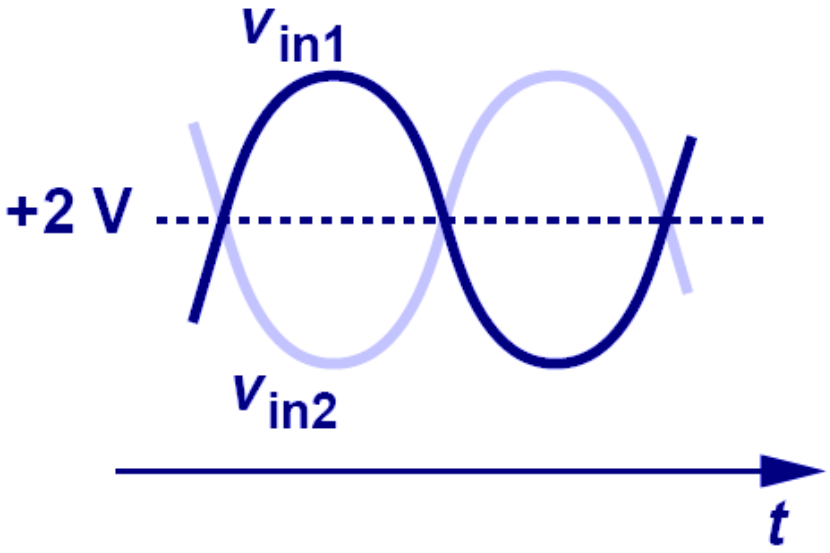
$$v_Y = -A_v v_{in} + v_r$$

$$v_X - v_Y = 2A_v v_{in}$$

- 若输入反相，则X、Y结点信号也反相 → （X – Y）或（ Y – X ）差分信号增强
- 若输入为“共模直流信号”+“小信号差分信号”，则输出只有增强了的差分信号

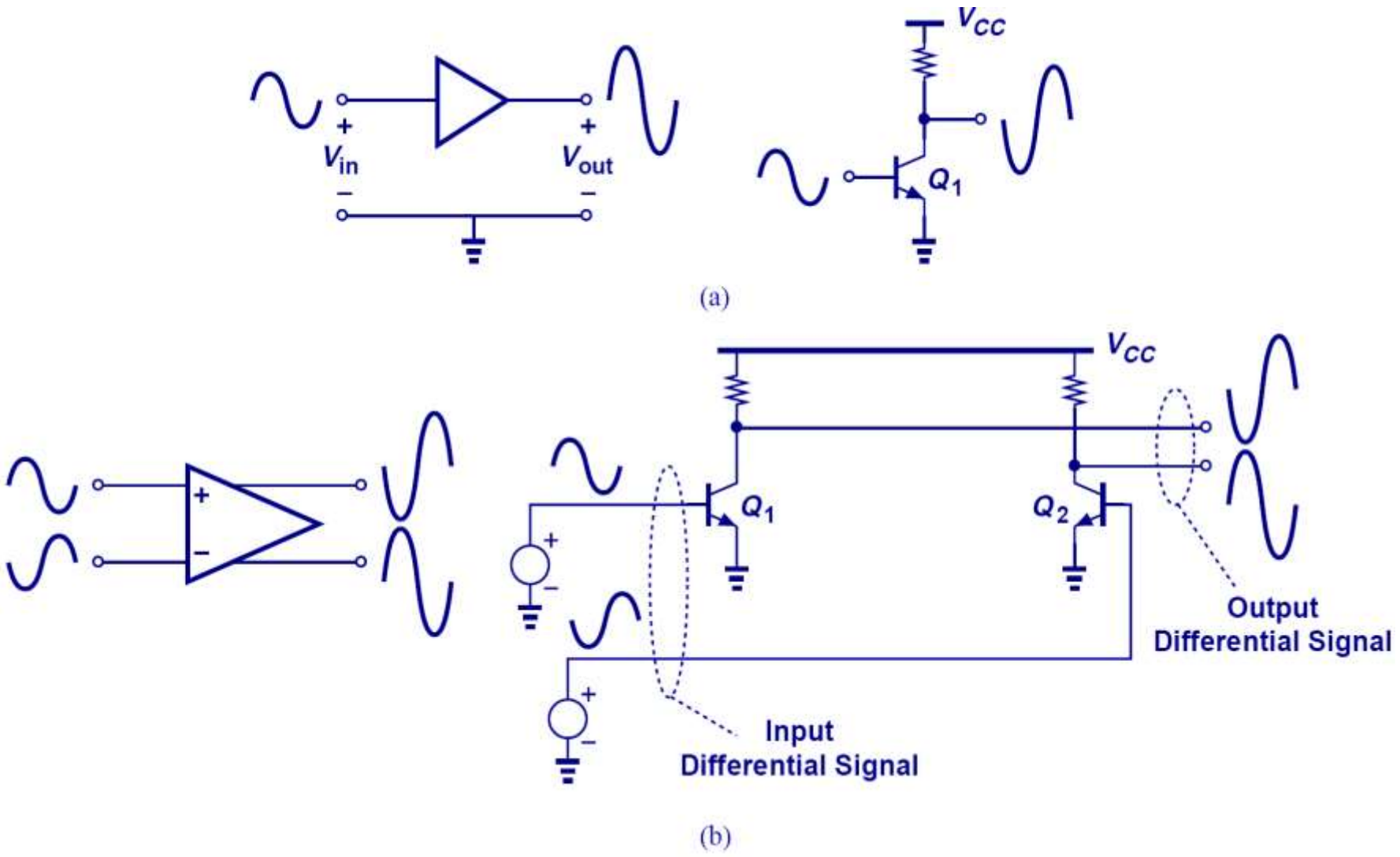
差分信号



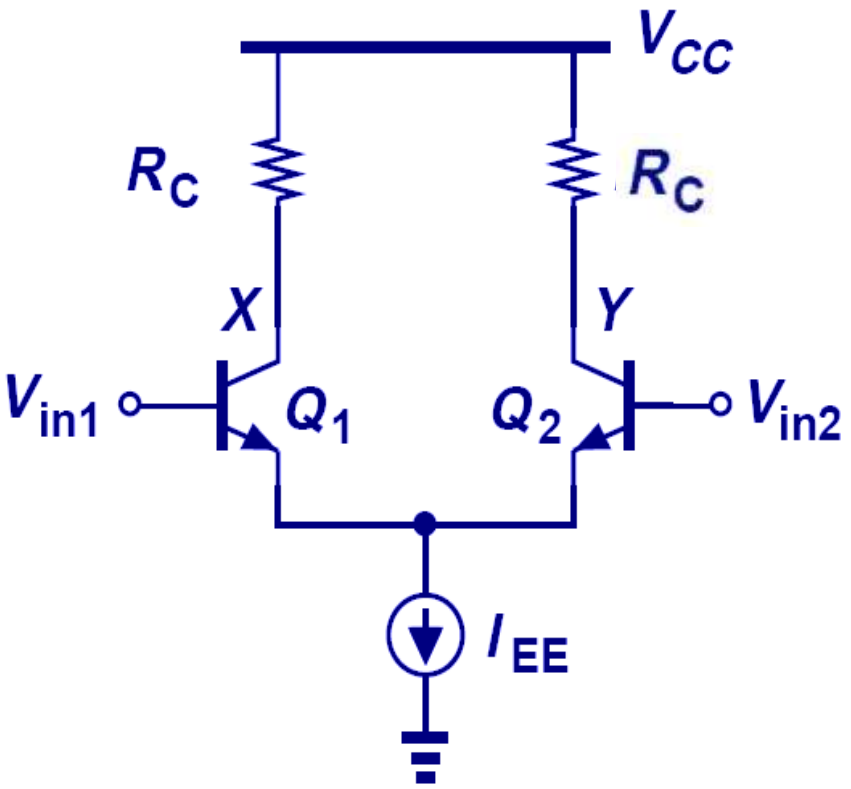


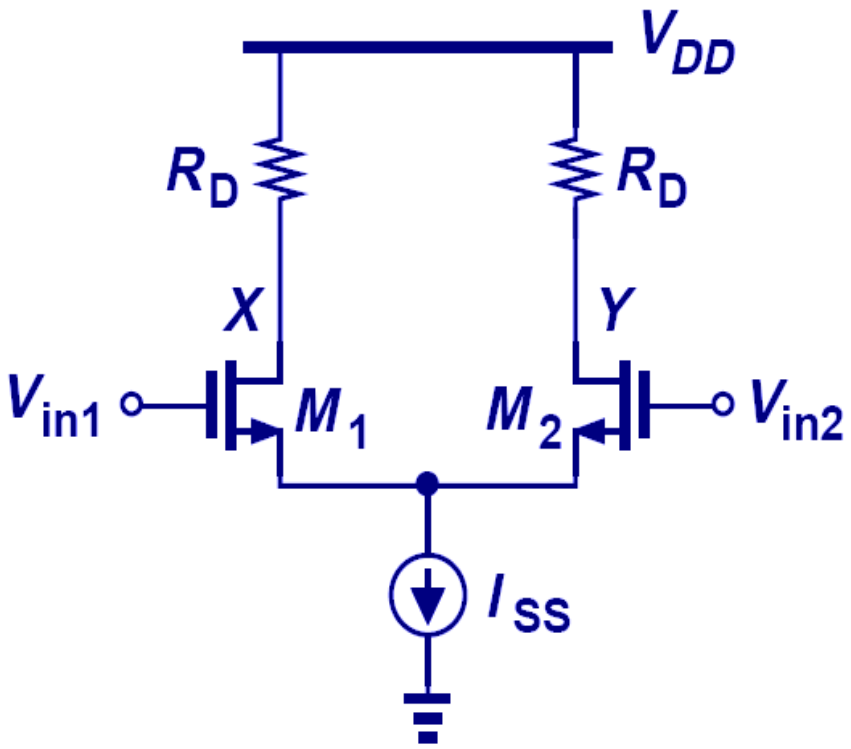
- 变压器可以产生差分信号；
- 差分信号的特性：①信号幅度相同，但相位相反；②信号平均值相等（该平均值即共模信号）

单端信号 vs. 差分信号


V_{in}
V_{out}
V_{CC}
Q_1
(a)
V_{CC}
Q_1
Q_2
Output
Differential Signal
Input
Differential Signal
(b)

差分对





- 如何优雅地构建差分对：采用如上结构的I_{EE}或I_{SS}尾电流（tail current source），对两个晶体管同时提供直流偏置；

The MOS Differential Pair

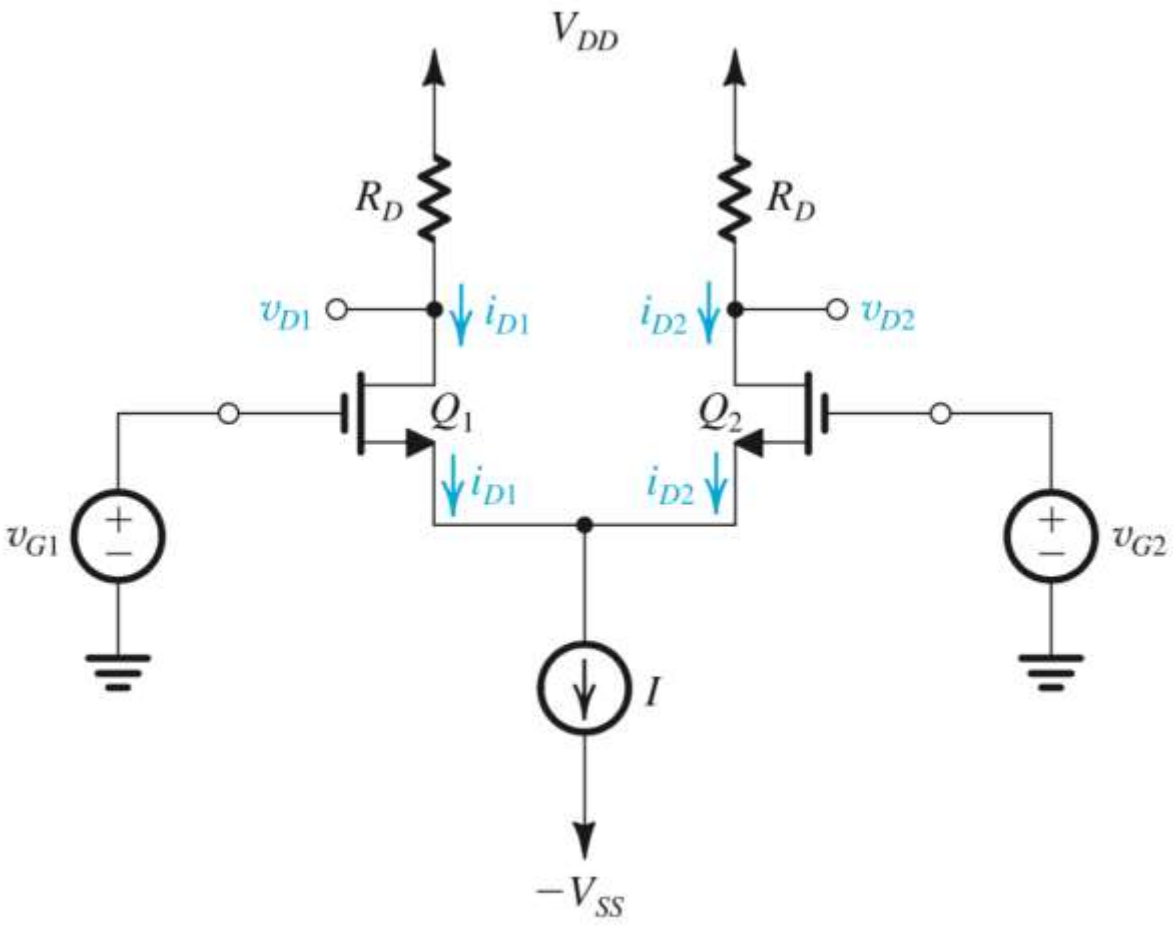
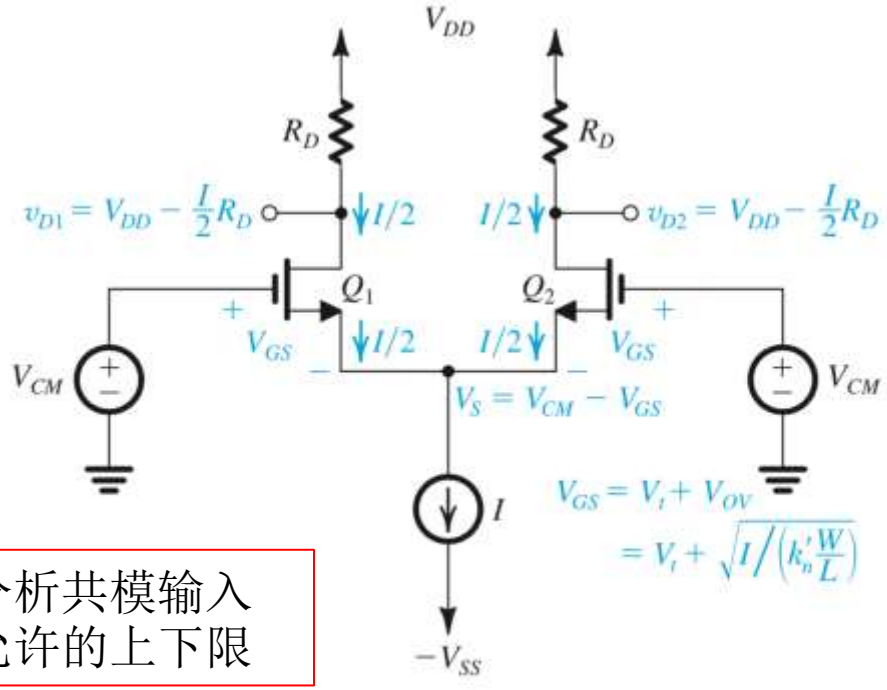


Figure 9.1 The basic MOS differential-pair configuration.

对称性

- Q_1，Q_2完全匹配（完全一致）
- 两个R_D完全一致
- 在大多数情况下，R_D可以用有源负载（电流源）替代
- 需保证Q_1、Q_2始终工作在饱和区

共模输入分析（Operation with a Common-Mode Input Voltage）



分析共模输入允许的上下限

Figure 9.2 The MOS differential pair with a common-mode input voltage V_{CM}

(8.2) $\frac{I}{2} = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2$

(8.3) $V_{OV} = V_{GS} - V_t$ ①由I_D可求出V_{GS}

(8.4) $\frac{I}{2} = \frac{1}{2}k_n'\frac{W}{L}V_{OV}^2$

注意，V_{OV}是I/2对应的有效电压

(8.5) $V_{OV} = \sqrt{I/\left(k_n'\frac{W}{L}\right)}$

(8.6) $v_{D1} = v_{D2} = V_{DD} - \frac{I}{2}R_D$ ②V_D固定→V_G的上限

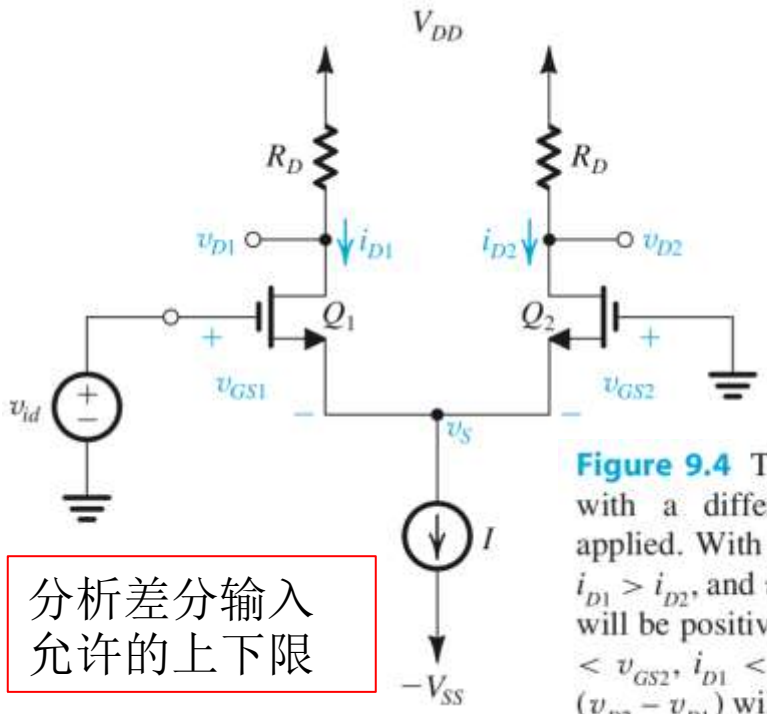
(8.7) $\max(V_{CM}) = V_t + V_{DD} - \frac{I}{2}R_D$

(8.8) $\min(V_{CM}) = -V_{SS} + V_{CS} + V_t + V_{OV}$

③V_S有最小值→V_G的下限

- $v_{G1} = v_{G2} = V_{CM}$, Q_1 and Q_2 are matched；电路完全对称
- 尾电流均分：$I_{D1} = I_{D2} = I/2$, $V_S = V_{CM} - V_{GS}$
- 为简化分析，得到直观的结果，先忽略沟道调制效应
- V_{CM}:上限~需保证管子工作在饱和区（8.7）；下限~V_S和-V_{SS}之间需具有一定的电压差（V_{CS}），以保证电流源能正常工作（8.8）
- V_{CM}有微小变化量（共模小信号）→尾电流仍均分→ v_{D1}- v_{D2}依旧=0（共模抑制）

差分输入分析（Operation with a Differential Input Voltage）



分析差分输入允许的上下限

Figure 9.4 The MOS differential pair with a differential input signal v_{id} applied. With v_{id} positive: $v_{GS1} > v_{GS2}$, $i_{D1} > i_{D2}$, and $v_{D1} < v_{D2}$; thus $(v_{D2} - v_{D1})$ will be positive. With v_{id} negative: $v_{GS1} < v_{GS2}$, $i_{D1} < i_{D2}$, and $v_{D1} > v_{D2}$; thus $(v_{D2} - v_{D1})$ will be negative.

①v_{id}上限：电流完全分配到Q_1时由I_{D1}可求出V_{GS1}，此时$I_{D2}=0$
→$V_{GS2}=V_t$

$$I = \frac{1}{2}\left(k_n' \frac{W}{L}\right)(v_{GS1} - V_t)^2$$

(8.9) $$v_{GS1} = V_t + \sqrt{2I/k_n'(W/L)}$$

(8.9) $$v_{GS1} = V_t + \sqrt{2}V_{OV}$$

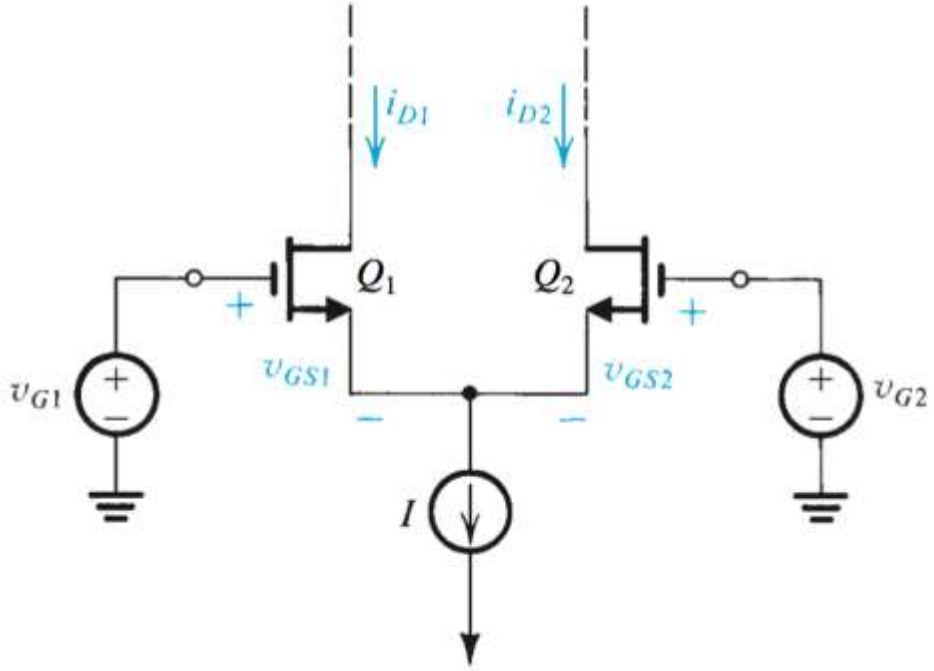
(8.10) $$\max(v_{id}) = V_{GS1} + v_S$$

(8.10) $$\max(v_{id}) = \sqrt{2}V_{OV}$$

- $v_{id} = v_{GS1} - v_{GS2}$；{ > 0 → $i_{D1} > i_{D2}$； < 0 → $i_{D1} < i_{D2}$；但$i_{D1}+i_{D2}$依旧=I }
- v_{id}的上限：使得尾电流完全被分配到Q_1，即$i_{D1}=I$，$i_{D2}=0$，见上面公式，其中V_{OV}为$i_{D1}=I/2$时的overdrive voltage
- v_{id}的下限：使得尾电流完全被分配到Q_2，即$i_{D1}=0$，$i_{D2}=I$；

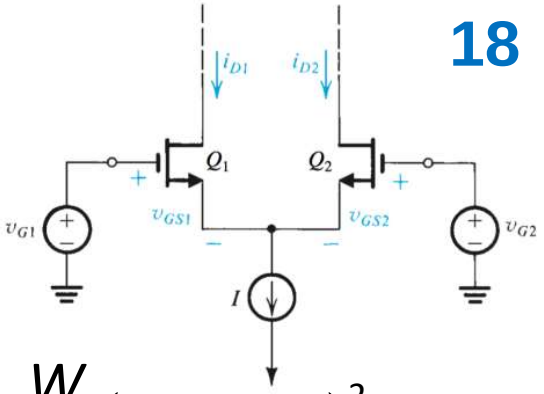
$$-\sqrt{2}V_{OV} \le v_{id} \le \sqrt{2}V_{OV}$$

差分大信号分析



- **Objective is to derive expressions for drain current i_{D1} and i_{D2} in terms of differential signal $v_{id} = v_{G1} - v_{G2}$.**
- **Assumptions:**
  - Perfectly Matched
  - Channel-length Modulation is Neglected
  - Work in Saturation Region

9.1.3. Large-Signal Operation



- **step #1: Expression drain currents for Q_1 and Q_2.**
- **step #2: Take the square roots of both sides of both (8.11) and (8.12)**
- **step #3: Subtract (8.14) from (8.13) and perform appropriate substitution.**
- **step #4: Note the constant-current bias constraint.**

(8.11) $i_{D1} = \frac{1}{2} k_n' \frac{W}{L} (v_{GS1} - V_t)^2$

约束方程1

(8.12) $i_{D2} = \frac{1}{2} k_n' \frac{W}{L} (v_{GS2} - V_t)^2$

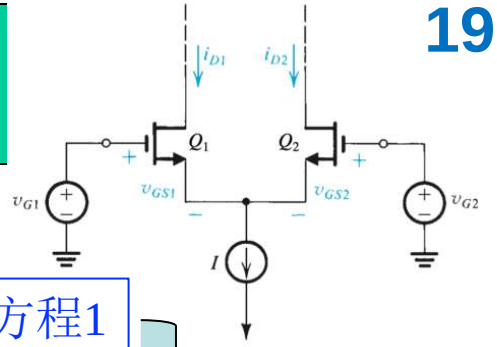
(8.13) $\sqrt{i_{D1}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} (v_{GS1} - V_t)$

(8.14) $\sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} (v_{GS2} - V_t)$

(8.15) $v_{GS1} - v_{GS2} = v_{G1} - v_{G2} = v_{id}$

(8.16) $\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} v_{id}$

9.1.3. **Large-Signal Operation**



$$(8.16)\quad \sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2}k_n'\frac{W}{L}}v_{id}$$ 约束方程1

$$(8.17)\quad i_{D1} + i_{D2} = I$$ 约束方程2

两个方程，两个未知数，可解

- **step #5: Simplify (8.15).**
- **step #6: Incorporate the constant-current bias.**
- **step #7: Solve (8.16) and (8.17) for the two unknowns – i_{D1} and i_{D2}.**
  - Refer to (8.23) and (8.24).

$$(8.17)\quad 2\sqrt{i_{D1}i_{D2}} = I - \frac{1}{2}k_n'\frac{W}{L}v_{id}^2$$

$$(8.23)\quad i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2}$$

$$(8.24)\quad i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2}$$

验证前面的极值 $-\sqrt{2}V_{OV} \le v_{id} \le \sqrt{2}V_{OV}$

但（8.23）、（8.24）包含了更多的信息

9.1.3. **Large-Signal Operation**

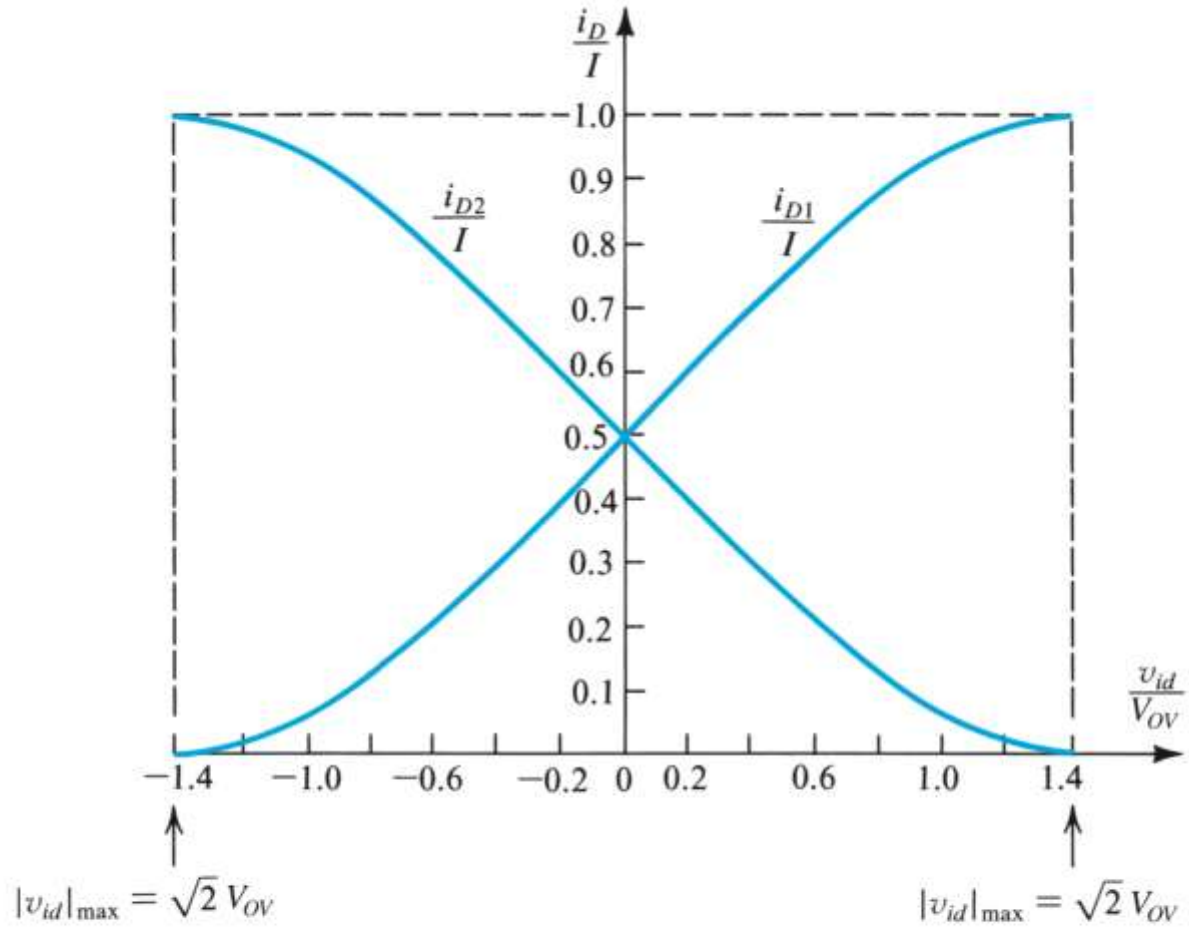


Figure 9.6 Normalized plots of the currents in a MOSFET differential pair. Note that V_{OV} is the overdrive voltage at which Q_1 and Q_2 operate when conducting drain currents equal to $I/2$, the equilibrium situation. Note that these graphs are universal and apply to any MOS differential pair.

9.1.3. Large-Signal Operation

$$i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1-\left(\frac{v_{id}/2}{V_{OV}}\right)^2}$$

$$i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1-\left(\frac{v_{id}/2}{V_{OV}}\right)^2}$$

Review 1：MOSFET小信号近似的前提？ $v_{gs} \ll 2V_{OV}$

小信号分析的前提

keep $(v_{id}/2)$ much smaller than V_{OV}

- **Transfer characteristics of (8.23) and (8.24) are nonlinear.** i_D与v_{id}的关系非线性
- **Linear amplification is desirable and v_{id} will be as small as possible.** 线性化需求
- **For a given value of V_{OV}, the only option is to keep $v_{id}/2$ much smaller than V_{OV}.**

希望输出（i_{D1}，i_{D2}）与输入（v_{id}）呈线性关系 → 根号里的两次项可忽略

small-signal approximation

$$(8.25)\quad i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\frac{v_{id}}{2}$$

$$(8.26)\quad i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\frac{v_{id}}{2}$$

单管电流变化

$$(8.27)\quad i_d \approx \left(\frac{I}{V_{OV}}\right)\frac{v_{id}}{2}$$

单管电压变化

Review 2：MOS管的g_m是多少？

$$g_m = \frac{I_D}{V_{OV}/2}$$

9.1.3. **Large-Signal Operation**

V_{OV}越大，线性范围越大，但跨导越小 → need trade-off

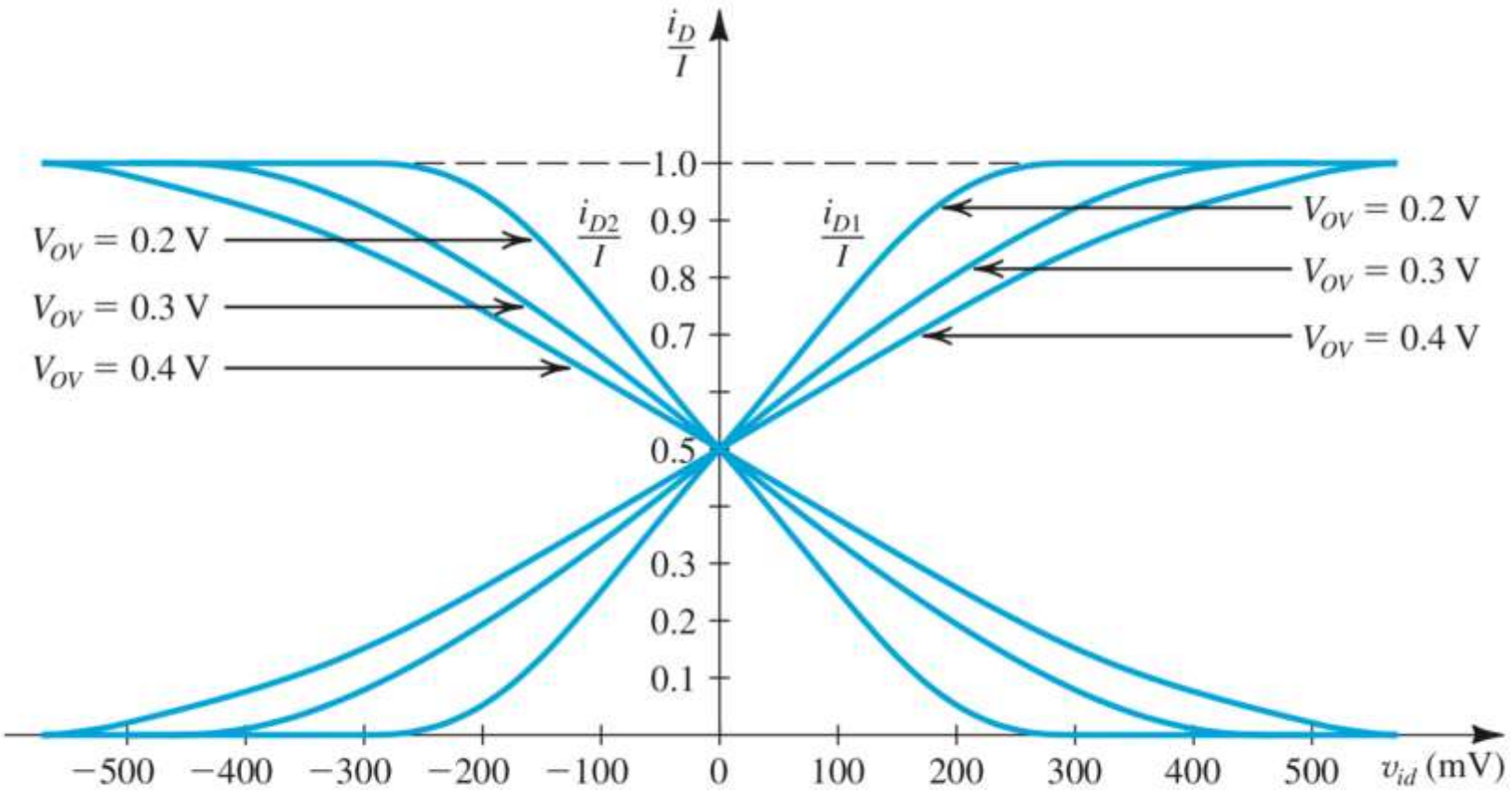
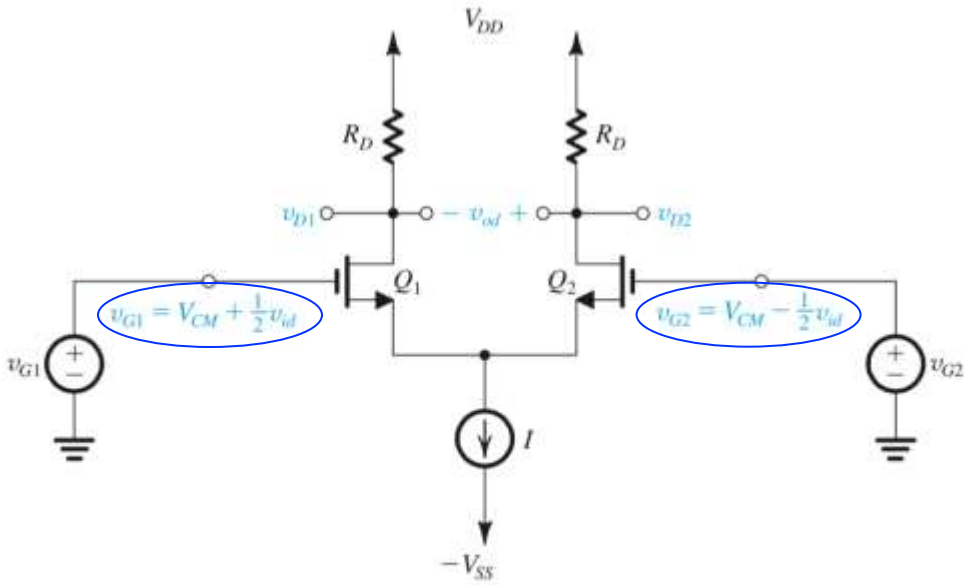
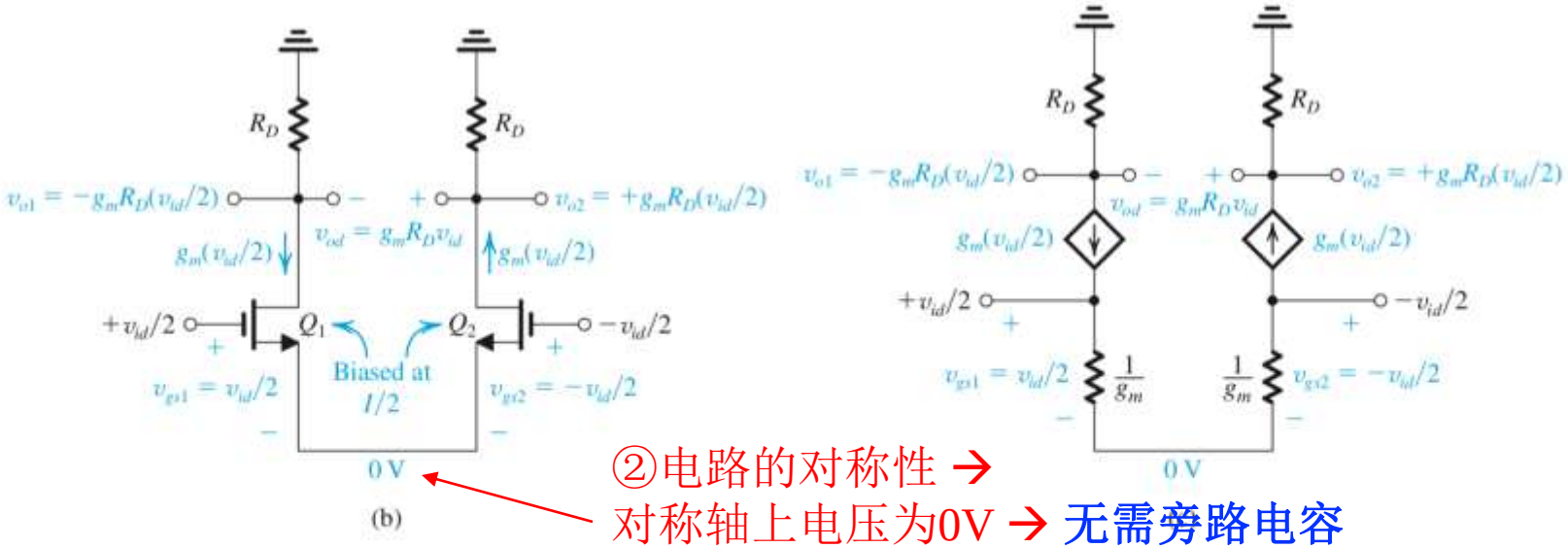


Figure 9.7 The linear range of operation of the MOS differential pair can be extended by operating the transistor at a higher value of V_{OV}.



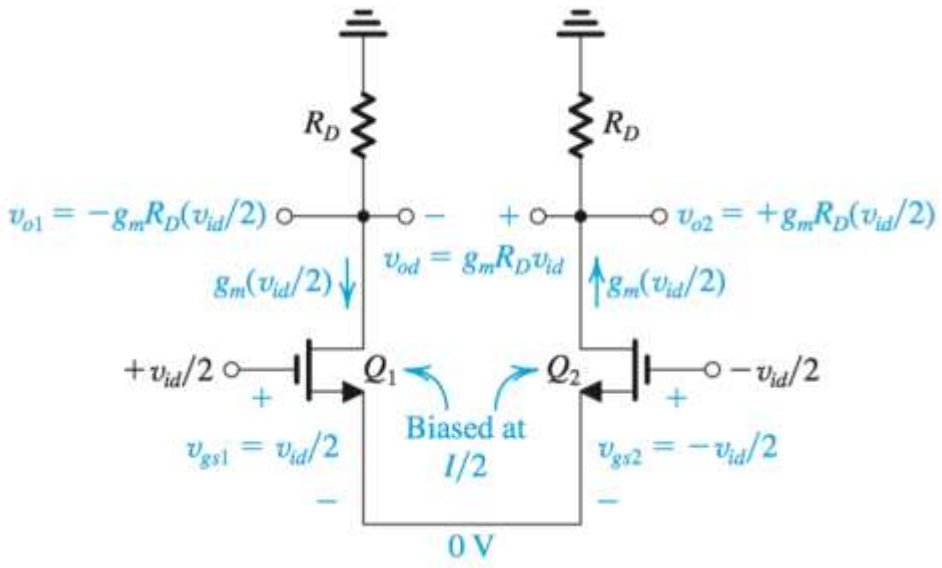
① V_{CM}一般取值在供电电源的中间电压位置，即$(V_{DD}+V_{SS})/2 \approx 0$ V



②电路的对称性 → 对称轴上电压为0V → 无需旁路电容

Figure 9.8 Small-signal analysis of the MOS differential amplifier. (**a**) The circuit with a common-mode voltage applied to set the dc bias voltage at the gates and with v_{id} applied in a complementary (or balanced) manner. (**b**) The circuit prepared for small-signal analysis. (**c**) The circuit in (**b**), with the MOSFETs replaced with T models.

9.1.4. **Differential Gain**



(8.28) $v_{G1} = V_{CM} + \frac{1}{2} v_{id}$

(8.29) $v_{G2} = V_{CM} - \frac{1}{2} v_{id}$

(8.30) $g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}}$

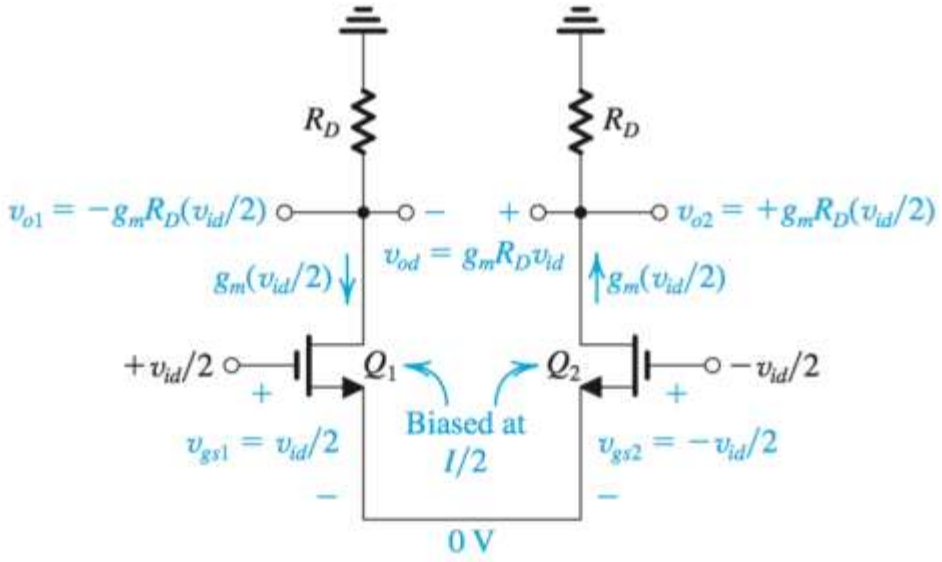
(8.31) $v_{o1} = -g_m \frac{v_{id}}{2} R_D$

(8.32) $v_{o2} = +g_m \frac{v_{id}}{2} R_D$

(8.35) $A_d \equiv \frac{v_{od}}{v_{id}} = g_m R_D$

9.1.4. **Differential Gain**

(8.28) $v_{G1} = V_{CM} + \frac{1}{2}v_{id}$



(8.29) $v_{G2} = V_{CM} - \frac{1}{2}v_{id}$

(8.30) $g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}}$

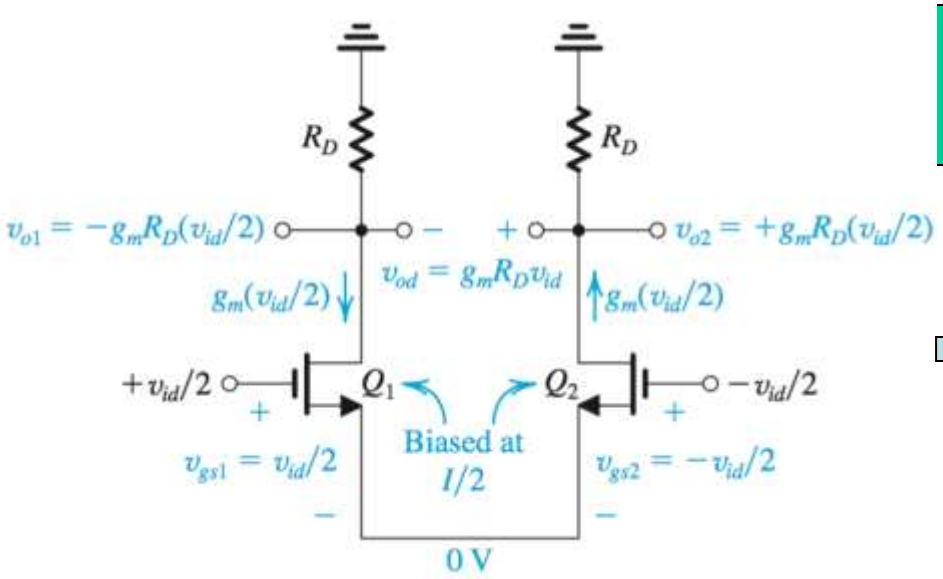
- **For MOS pair, each device operates with drain current I/2 and corresponding overdrive voltage (V_{OV}).**
- **MOS: $g_m = I/V_{OV}$**
- **BJT: $g_m = \alpha I/2V_T$**
- **MOS & BJT: $r_o = |V_A|/(I/2)$.**

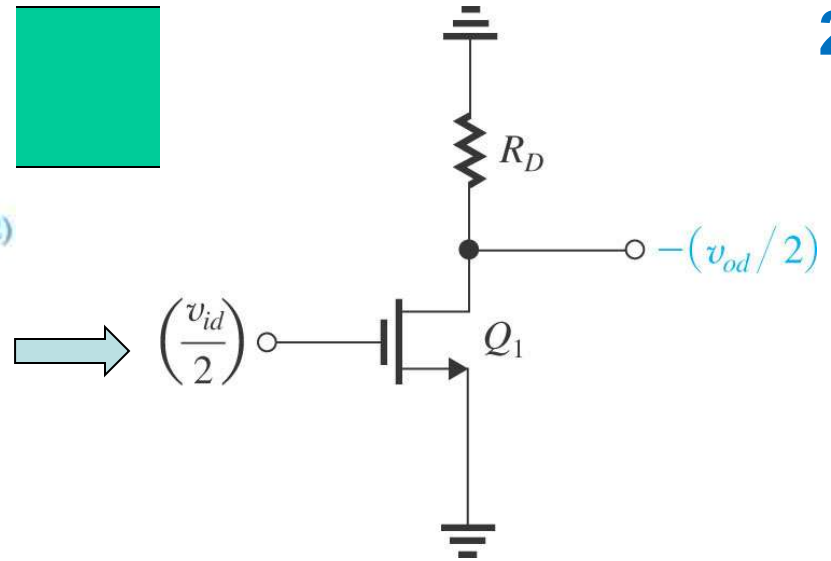
$$g_m = \frac{I_D}{V_{OV}/2}$$

(8.31) $v_{o1} = -g_m \frac{v_{id}}{2} R_D$

(8.32) $v_{o2} = +g_m \frac{v_{id}}{2} R_D$

(8.35) $A_d \equiv \frac{v_{od}}{v_{id}} = g_m R_D$



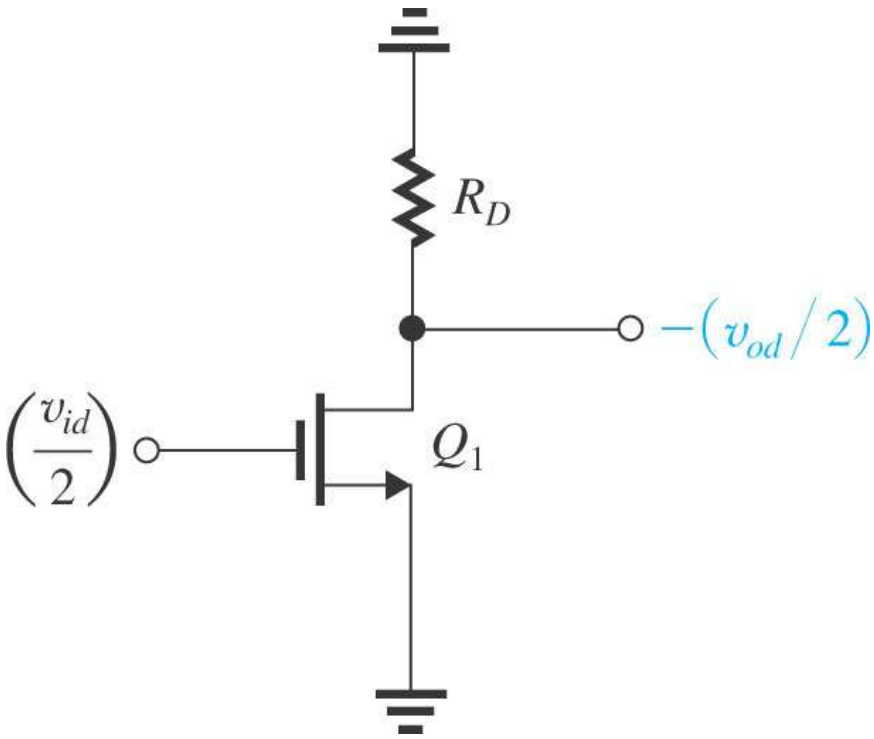


- $v_{i1} = V_{CM} + v_{id}/2$ and $v_{i2} = V_{CM} - v_{id}/2$ causes a virtual signal ground to appear on the common-source (common-emitter) connection
- Current in Q_1 increases by $g_m v_{id}/2$ and the current in Q_2 decreases by $g_m v_{id}/2$.
- Voltage signals of $g_m(R_D \| r_o) v_{id}/2$ develop at the two drains (collectors, with R_D replaced by R_C).

9.1.4 The Differential Half-Circuit

- **Figure 8.9 (right): The equivalent differential half-circuit of the differential amplifier of Figure 8.8.**
- **Here Q_1 is biased at $I/2$ and is operating at V_{OV}.**
- **This circuit may be used to determine the differential voltage gain of the differential amplifier $A_d = v_{od}/v_{id}$.**

- 差分电路的增益和半电路的增益完全一样！（负号是因为差分输出的正负极定义引起的）



$$(8.35)\quad A_d \equiv \frac{v_{od}}{v_{id}} = g_m R_D$$

Example 9.2

Give the differential half-circuit of the differential amplifier shown in Fig. 9.11(a). Assume that Q_1 and Q_2 are perfectly matched. Neglecting r_o, determine the differential voltage gain $A_d \equiv v_{od}/v_{id}$.

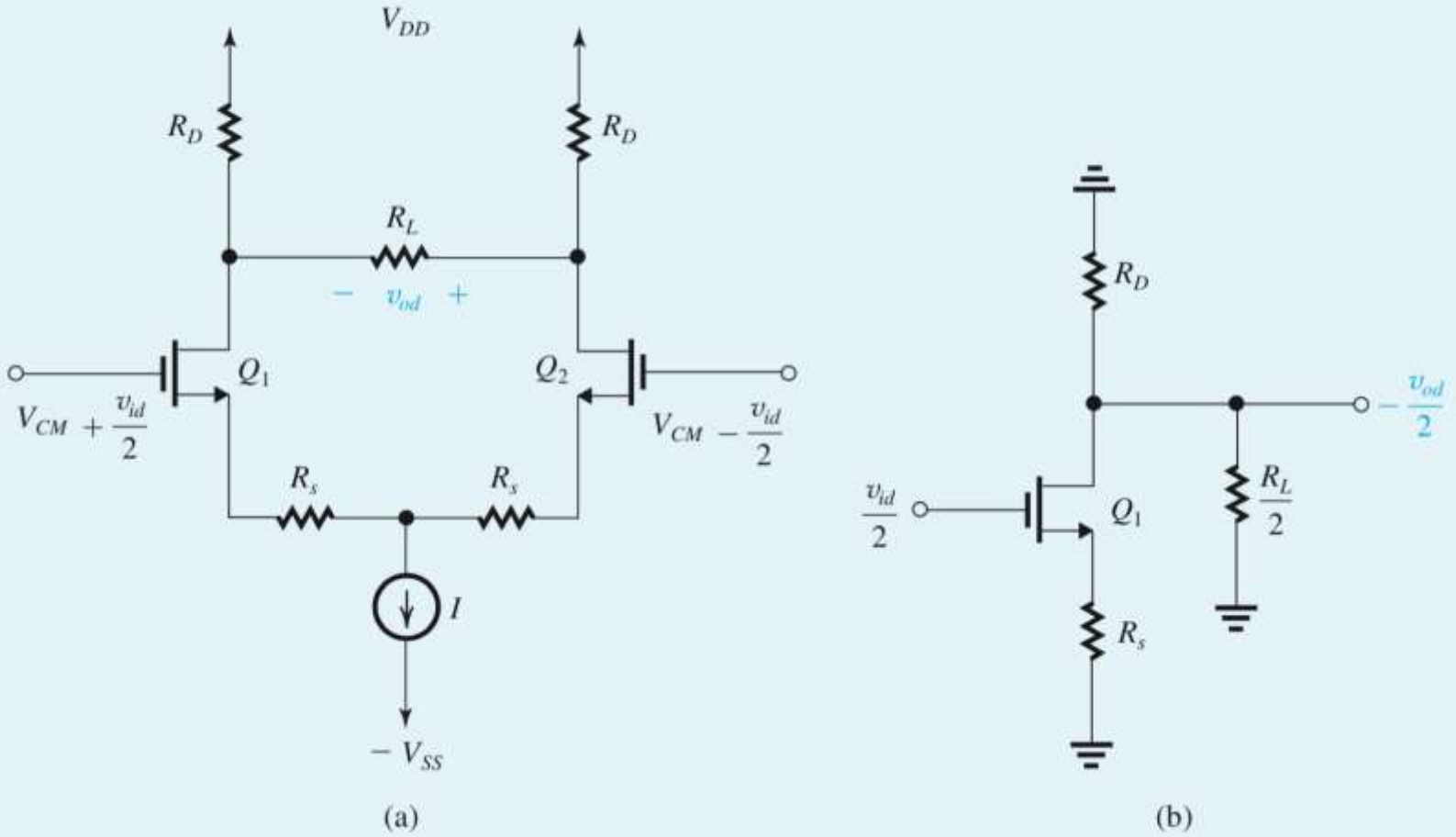


Figure 9.11 (**a**) Differential amplifier for Example 9.2. (**b**) Differential half-circuit.

$$\frac{-v_{od}/2}{v_{id}/2} = -\frac{R_D \parallel (R_L/2)}{1/g_m + R_s} \quad \Rightarrow \quad A_d \equiv \frac{v_{od}}{v_{id}} = \frac{R_D \parallel (R_L/2)}{1/g_m + R_s}$$

注意：此处差分对的增益是正的（v_{od}的极性定义），CS-deg的增益是负的

9.1.5. The Differential Amplifier with Current-Source Loads

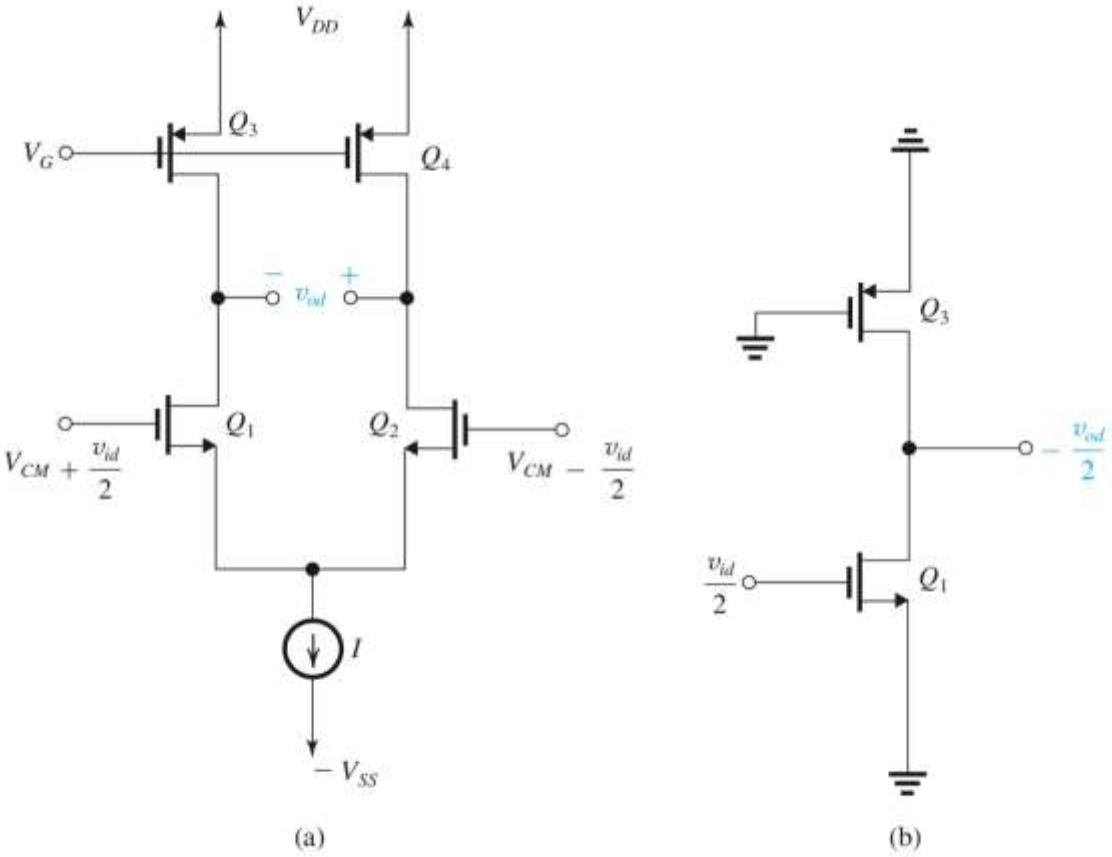


Figure 9.12 (**a**) Differential amplifier with current-source loads formed by Q_3 and Q_4. (**b**) Differential half-circuit of the amplifier in (**a**).

- **To obtain higher gain, the passive resistances (R_D) can be replaced with current sources.**
- $A_d = g_{m1}(r_{o1} \| r_{o3})$

9.1.6. **Cascode Differential Amplifier**

- **Gain can be increased via cascode configuration – discussed in Section 7.3.**
  - $A_d = g_{m1}(R_{on} \| R_{op})$
  - $R_{on} = (g_{m3}r_{o3})r_{o1}$
  - $R_{op} = (g_{m5}r_{o5})r_{o7}$

注意：只有当退化电阻阻值较大时（r_o, cascode 结构）才可以作此近似。若退化电阻为diode-connected 结构，可这样近似吗？

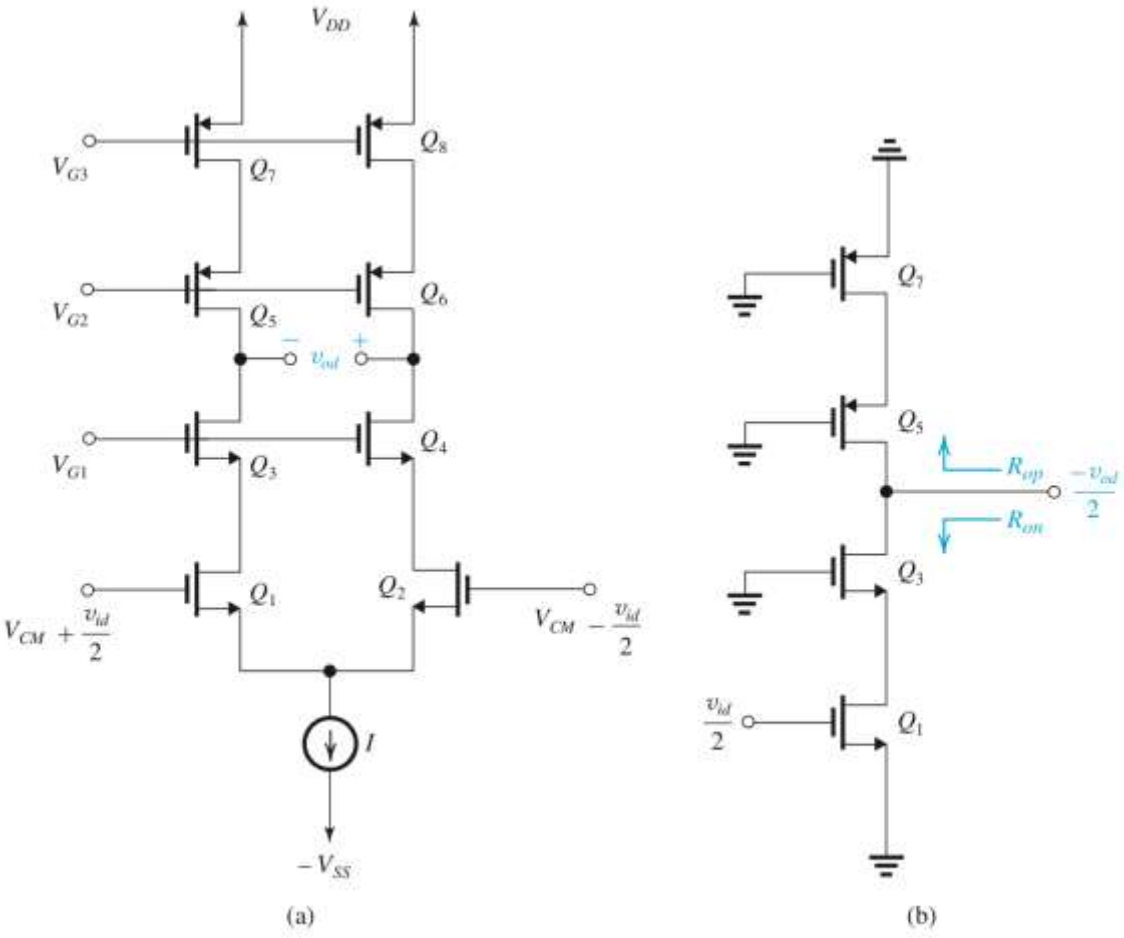
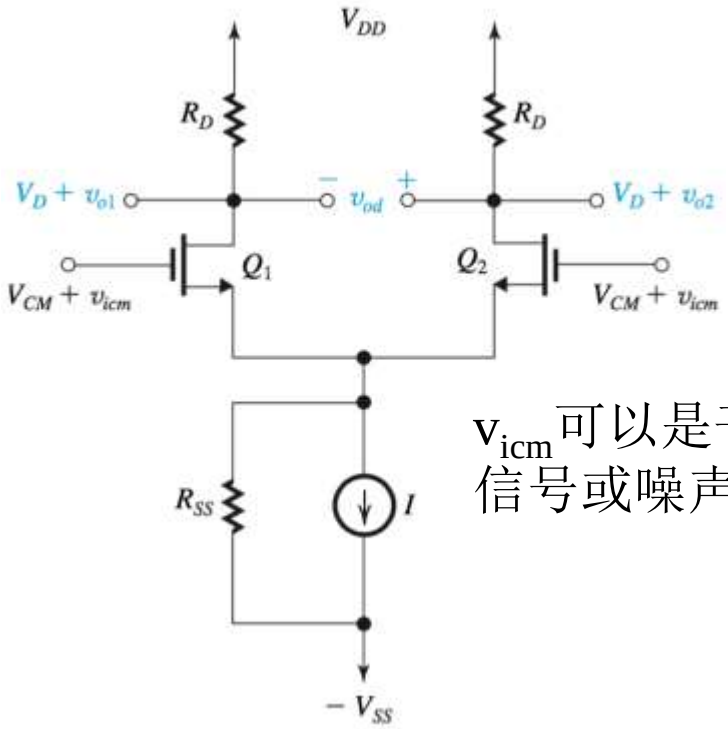


Figure 9.13 (a) Cascode differential amplifier; and (b) its differential half-circuit.

9.3.1. Common-Mode Gain and Common-Mode Rejection ratio (CMRR) 共模增益 & 共模抑制比



v_{icm}可以是干扰信号或噪声

- 如前所述，共模信号有微小变化时，无差分输出（共模小信号增益为零）。但若尾电流是非理想电流源呢？R_{SS}可看成两个$2R_{SS}$并联
- **Equation (8.43) describes effect of common-mode signal (v_{icm}) on v_{o1} and v_{o2}.**

(8.41) $$v_{icm} = \frac{i}{g_m} + 2iR_{SS}$$ 用T等效模型，i为单路的小信号电流

(8.42) $$i = \frac{v_{icm}}{1/g_m + 2R_{SS}}$$

(8.43) $$v_{o1} \approx v_{o2} \approx -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm}$$

(8.44) $$v_{o1} \approx v_{o2} \approx -\frac{v_{icm} R_D}{2R_{SS}}$$

(8.45) $$v_{od} = v_{o2} - v_{o1} = 0$$

完美匹配时依旧无差分输出

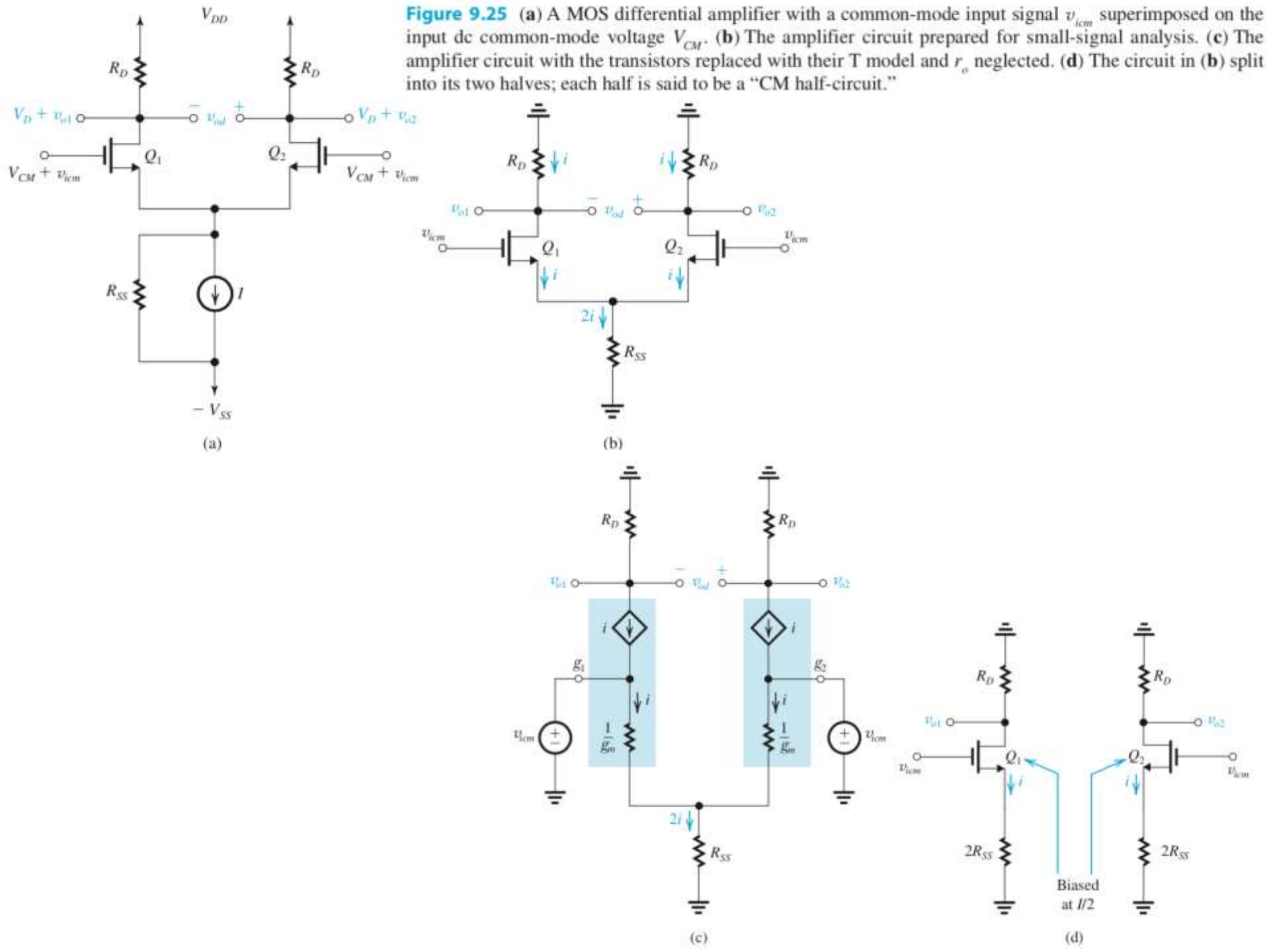


Figure 9.25 (**a**) A MOS differential amplifier with a common-mode input signal v_{icm} superimposed on the input dc common-mode voltage V_{CM}. (**b**) The amplifier circuit prepared for small-signal analysis. (**c**) The amplifier circuit with the transistors replaced with their T model and r_o neglected. (**d**) The circuit in (**b**) split into its two halves; each half is said to be a "CM half-circuit."

9.3.1. Common-Mode Gain and Common-Mode Rejection ratio (CMRR)

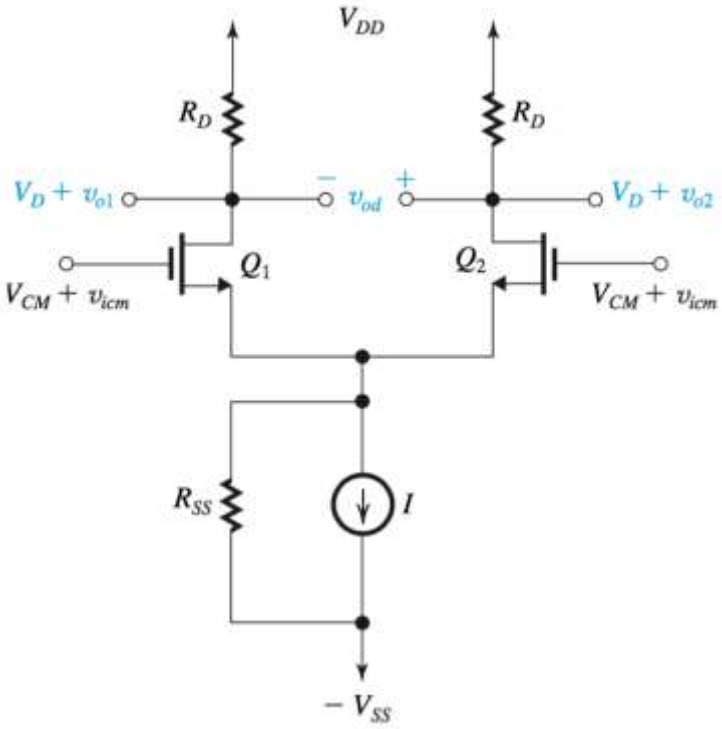
assumed that $2R_{SS} \gg 1/g_m$

(8.46) $$v_{o1} = -\frac{R_D}{2R_{SS}} v_{icm}$$

RD's are mismatched

(8.47) $$v_{o2} = -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$$

- 若R_D有mismatch呢？
- 若g_m有mismatch呢？



(8.48) $$v_{od} = v_{o2} - v_{o1} = \frac{-\Delta R_D}{2R_{SS}} v_{icm}$$

共模增益：共模小信号输入体现到差分输出的增益

(8.49) $$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = \frac{-\Delta R_D}{2R_{SS}} = \left(\frac{-R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right)$$

共模抑制比：差分增益/共模增益

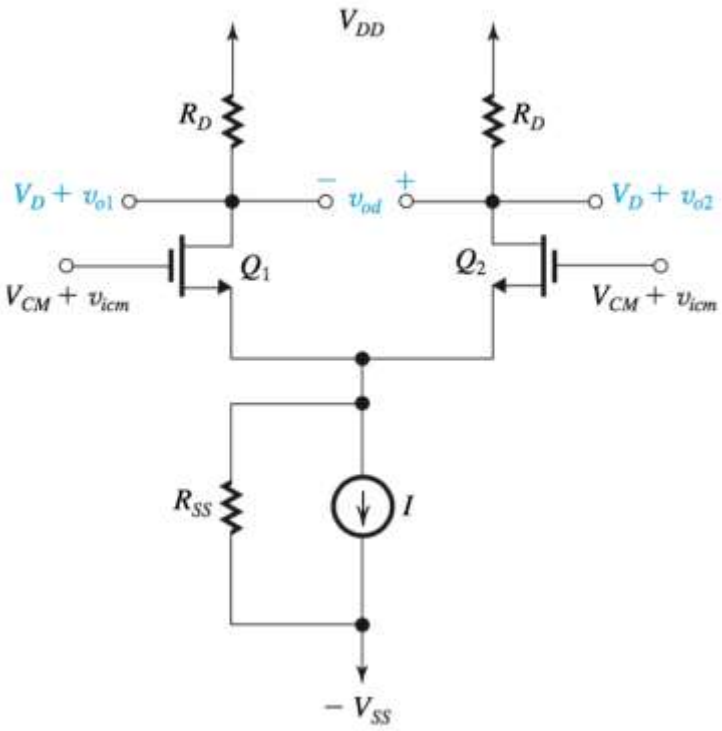
(8.50) $$CMRR \equiv \frac{|A_d|}{|A_{cm}|}$$ ← $g_m R_D$

$$\text{CMRR} = (2g_m R_{SS}) \Big/ (\Delta R_D / R_D)$$

9.3.1. Common-Mode Gain and Common-Mode Rejection ratio (CMRR)

g_m mismatch的可能原因：W/L的 mismatch

- 若R_D有mismatch呢？ $\mathrm{CMRR}=(2g_mR_{SS})/(\Delta R_D/R_D)$
- 若g_m有mismatch呢？



$$g_{m1}=g_m+\frac{1}{2}\Delta g_m$$

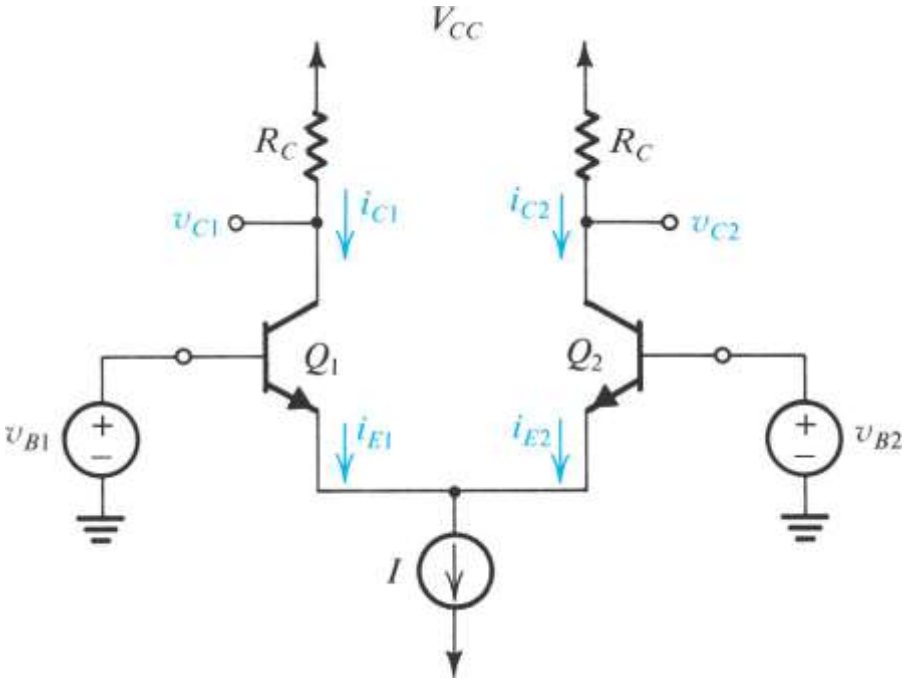
$$g_{m2}=g_m-\frac{1}{2}\Delta g_m$$

$$g_{m1}-g_{m2}=\Delta g_m$$

对称性破坏，需代入T等效电路模型计算，给出结果如下：

$$\mathrm{CMRR}=(2g_mR_{SS})\Big/\left(\frac{\Delta g_m}{g_m}\right)$$

The BJT Differential Pair



$$(8.66)\ \mathbf{max}\left(V_{CM}\right) \approx V_C + 0.4 = V_{CC} - \alpha \frac{I}{2} R_C + 0.4$$

$$(8.67)\ \mathbf{min}\left(V_{CM}\right) = -V_{EE} + V_{CS} + V_{BE}$$

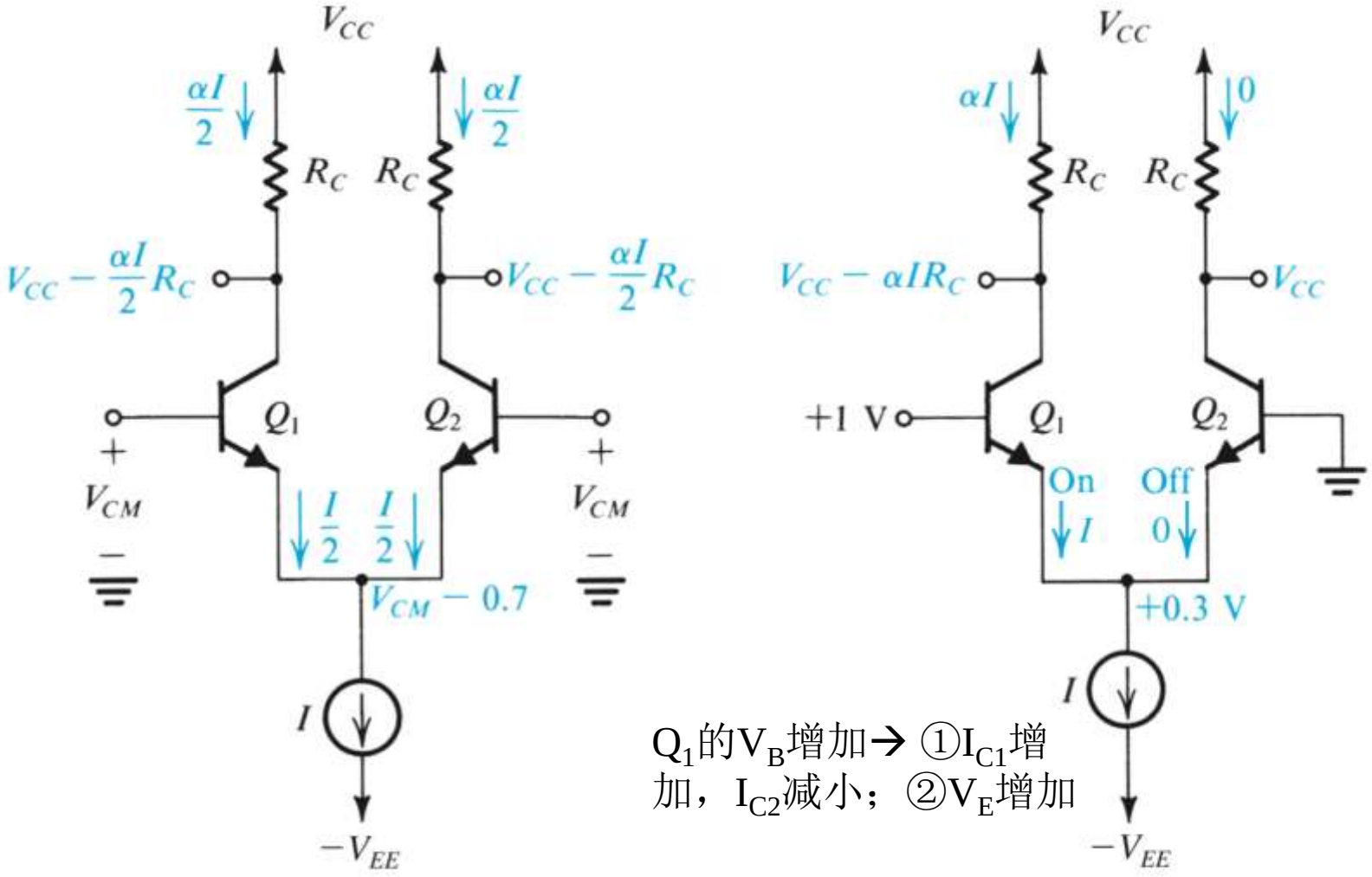
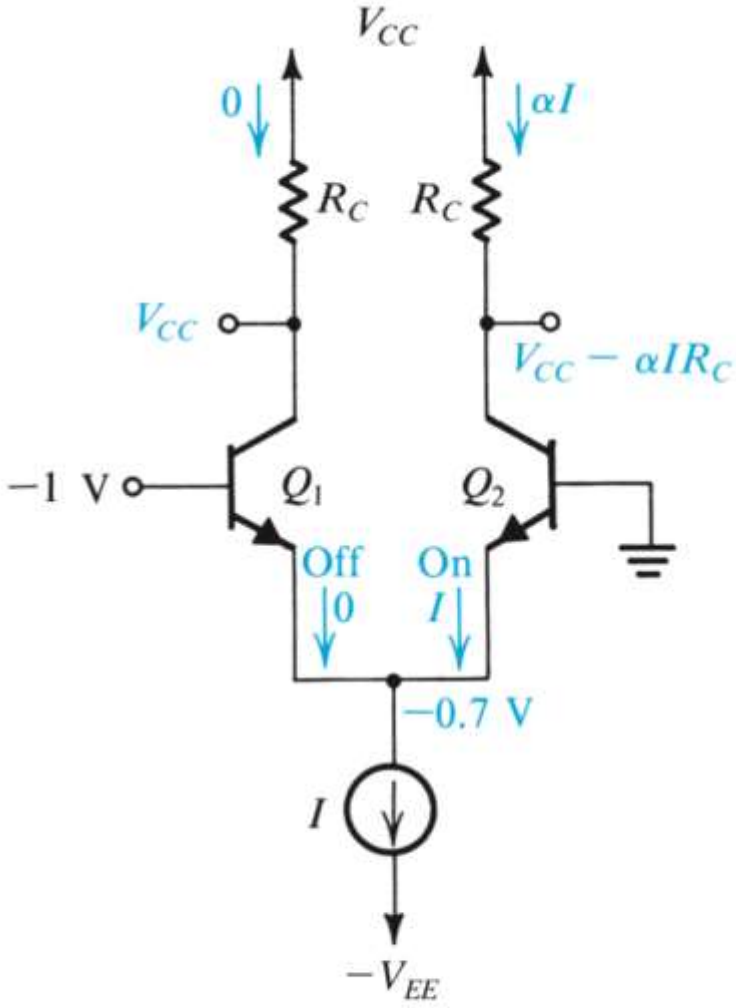
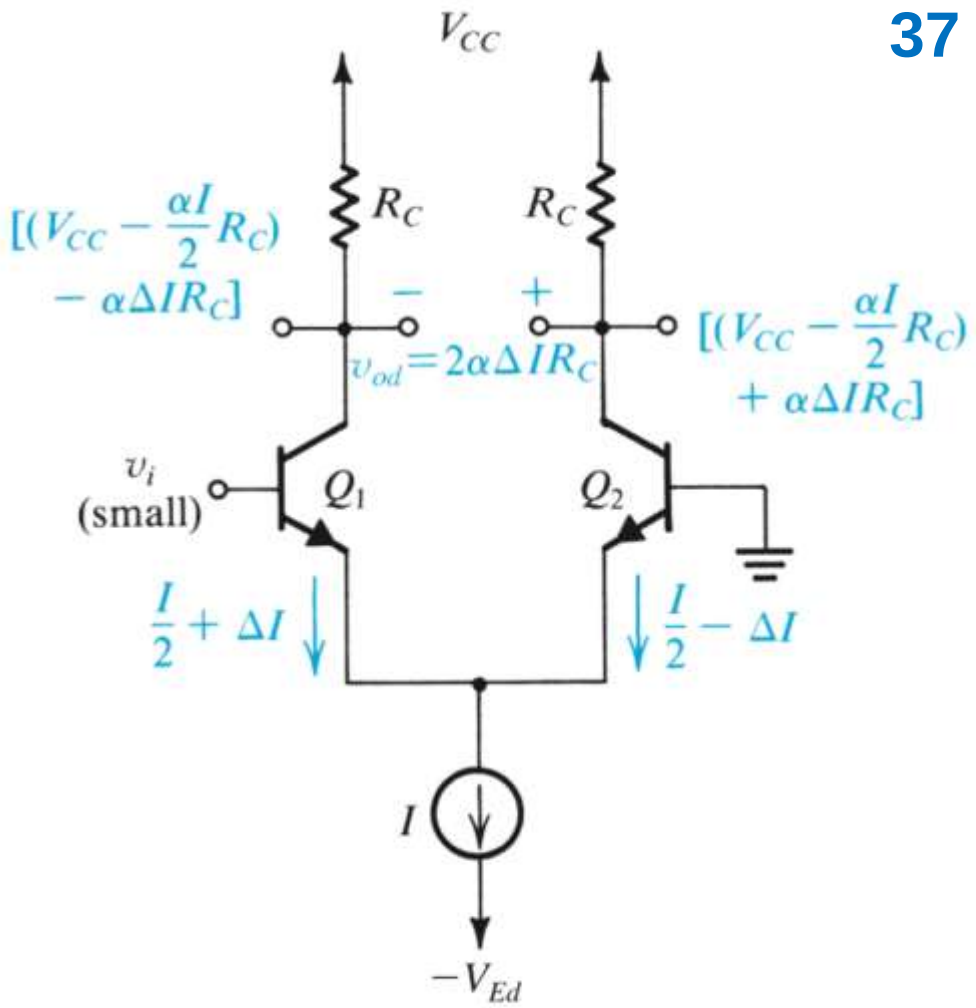


Figure 9.15 Different modes of operation of the BJT differential pair: **(a)** the differential pair with a common-mode input voltage V_{CM}; **(b)** the differential pair with a "large" differential input signal; **(c)** the differential pair with a large differential input signal of polarity opposite to that in **(b)**; **(d)** the differential pair with a small differential input signal v_i. Note that we have assumed the bias current source I to be ideal (i.e., it has an infinite output resistance) and thus I remains constant with the change in the voltage across it.

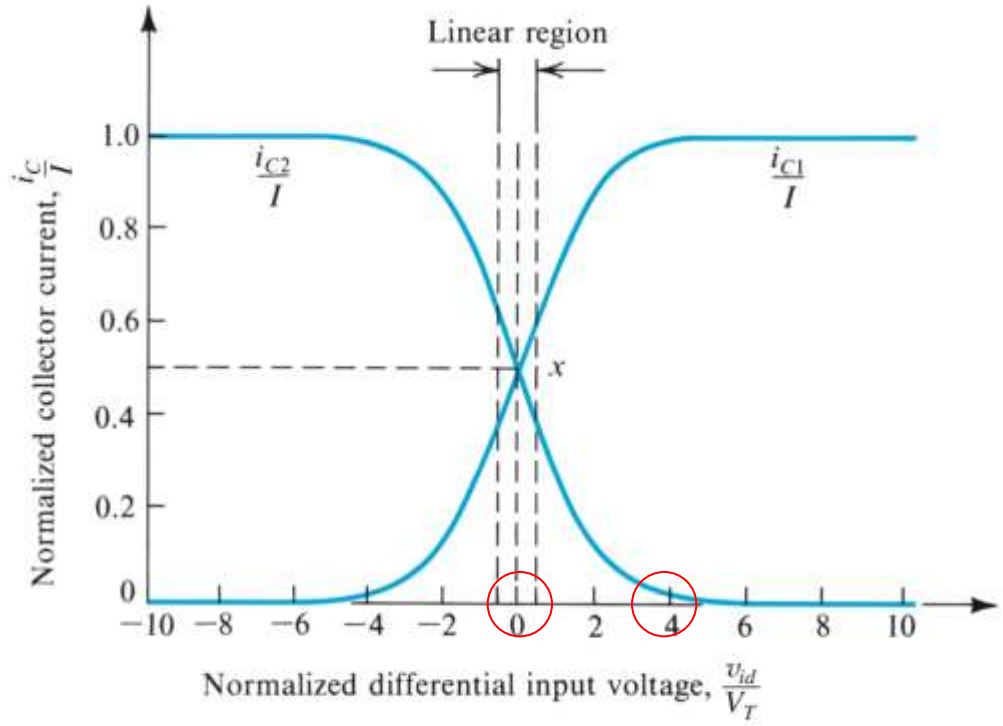


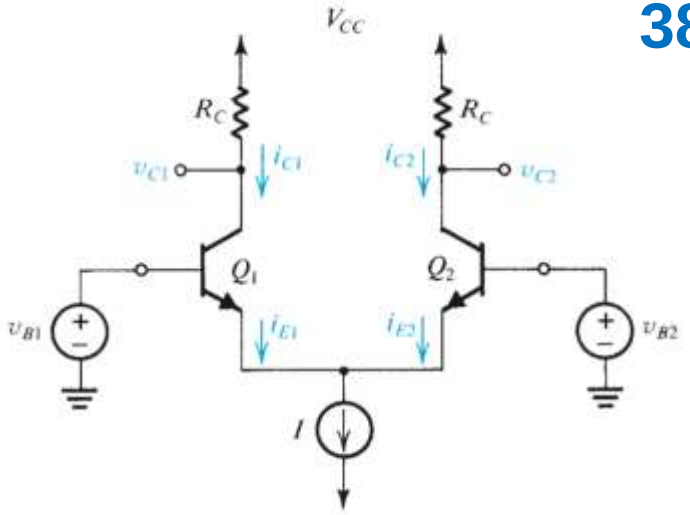
(c) 差分大信号输入（极性相反）



(d) 差分小信号输入

Figure 9.15 Different modes of operation of the BJT differential pair: **(a)** the differential pair with a common-mode input voltage V_{CM}; **(b)** the differential pair with a "large" differential input signal; **(c)** the differential pair with a large differential input signal of polarity opposite to that in **(b)**; **(d)** the differential pair with a small differential input signal v_i. Note that we have assumed the bias current source I to be ideal (i.e., it has an infinite output resistance) and thus I remains constant with the change in the voltage across it.





大信号特性：

① $4V_T$（≈100 mV）完全切换电流（对比MOS $\sqrt{2}\,V_{OV}$ ）

②小信号限制在$0.5V_T$范围内

Figure 9.16 Transfer characteristics of the BJT differential pair of Fig. 9.14 assuming $\alpha \simeq 1$.

$$i_{E1} = \frac{I_S}{\alpha} e^{(v_{B1}-v_E)/V_T}$$

$$i_{E2} = \frac{I_S}{\alpha} e^{(v_{B2}-v_E)/V_T}$$

$$\frac{i_{E1}}{i_{E2}} = e^{(v_{B1}-v_{B2})/V_T}$$

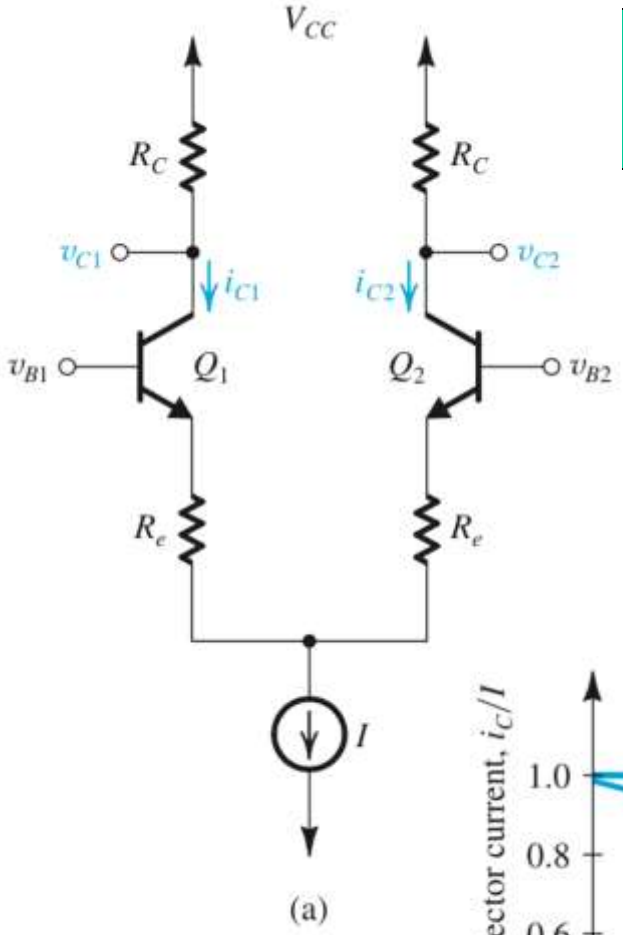
$$i_{E1} + i_{E2} = I$$

$$i_{E1} = \frac{I}{1+e^{-v_{id}/V_T}}$$

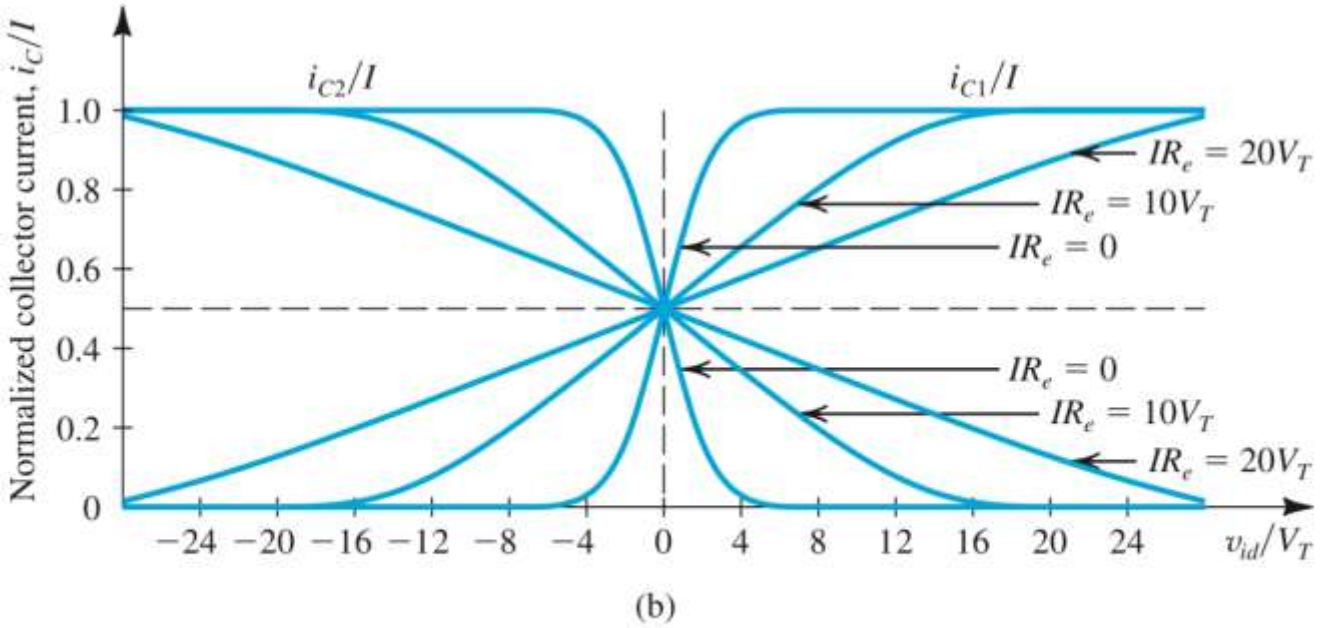
$$i_{E2} = \frac{I}{1+e^{v_{id}/V_T}}$$

两个方程，两个未知数，可解

发射极退化电阻可增加线性工作范围



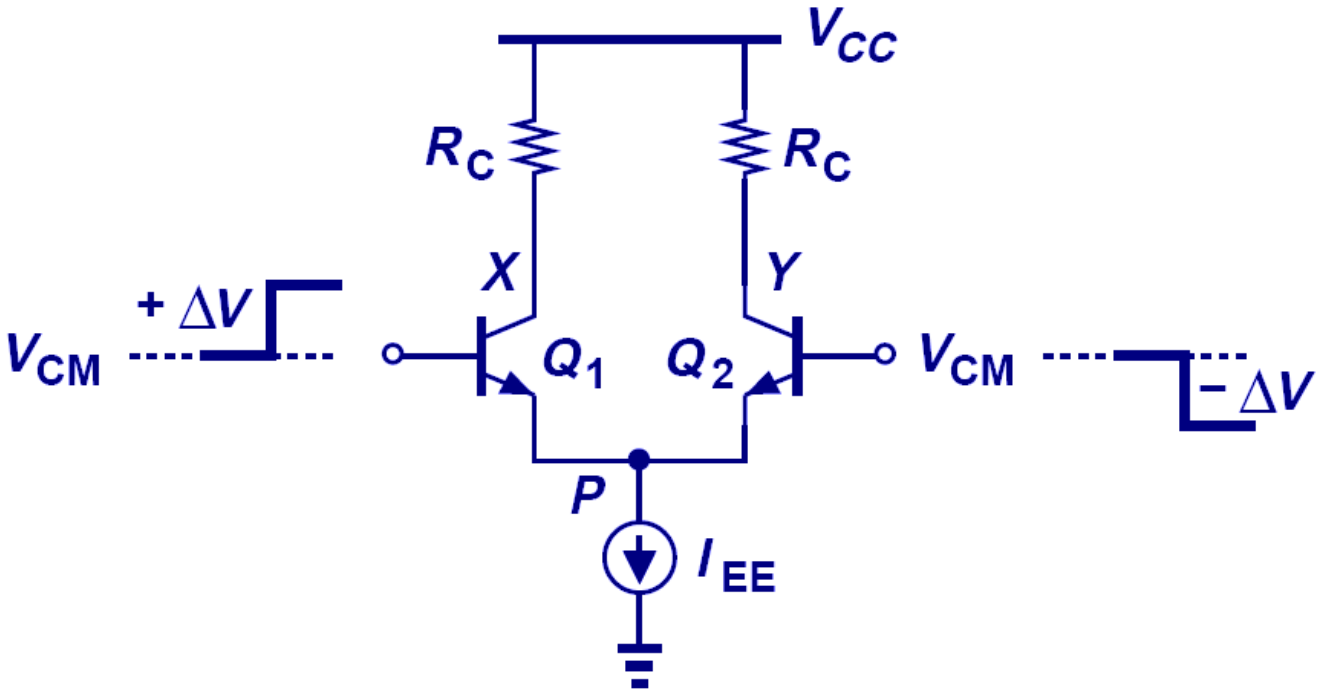
(a)



(b)

Figure 9.17 The transfer characteristics of the BJT differential pair **(a)** can be linearized **(b)** (i.e., the linear range of operation can be extended) by including resistances in the emitters.

小信号分析

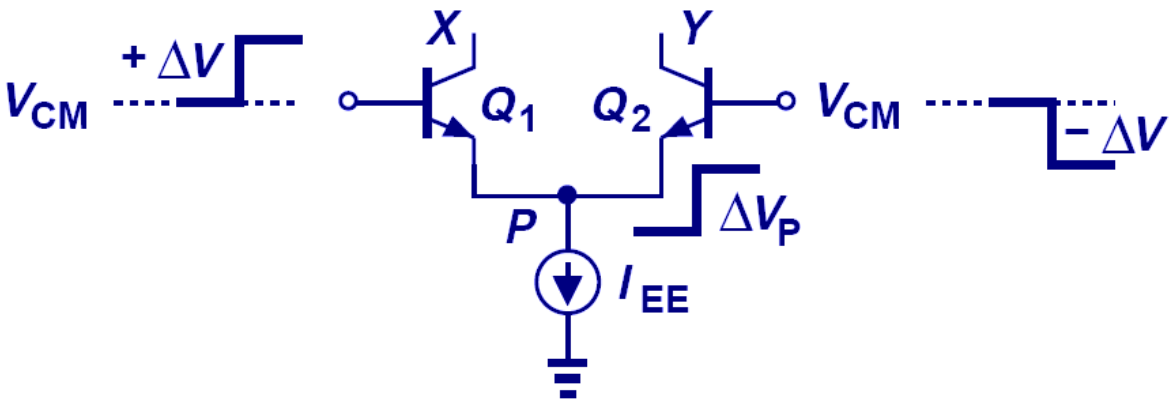


$$I_{C1} = \frac{I_{EE}}{2} + \Delta I$$

$$I_{C2} = \frac{I_{EE}}{2} - \Delta I$$

- I_{C1} 和 I_{C2}的和是固定值（I_{EE}），所以 I_{C1}的增加等于I_{C2}的减小；

“虚拟地”



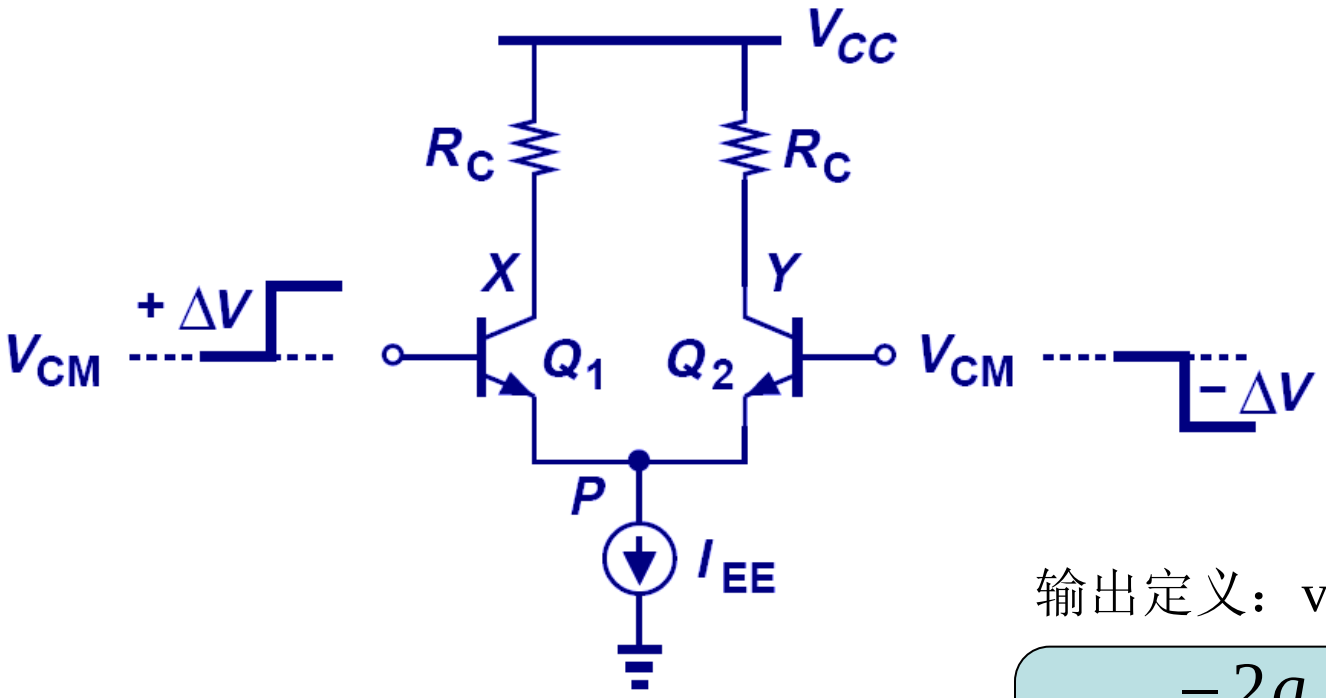
$$\Delta V_P = 0$$

$$\Delta I_{C1} = g_m \Delta V$$

$$\Delta I_{C2} = -g_m \Delta V$$

- 因对称性，P点可以看作交流地，但其实际是不接地的，所以也称为“虚拟地”

小信号差分增益



输出定义：v_X-v_Y 也可以是：v_Y-v_X

$$A_v = \frac{-2g_m \Delta V R_C}{2\Delta V} = -g_m R_C$$

- 增益与CE半电路一样，但功耗加倍

例题

Example 10.6 Design a bipolar differential pair for a gain of 10 and a power budget of 1 mW with a supply voltage of 2 V.

①根据功耗要求及V_{CC}，算出I_{EE}，进一步算出管子I_C

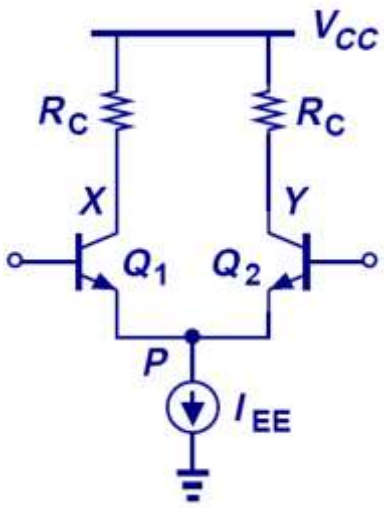
Solution With $V_{CC} = 2$ V, the power budget translates to a tail current of 0.5 mA. Each transistor thus carries a current of 0.25 mA near equilibrium, providing a transconductance of $0.25\,\text{mA}/26\,\text{mV} = (104\,\Omega)^{-1}$. It follows that

②根据I_C，算出g_m

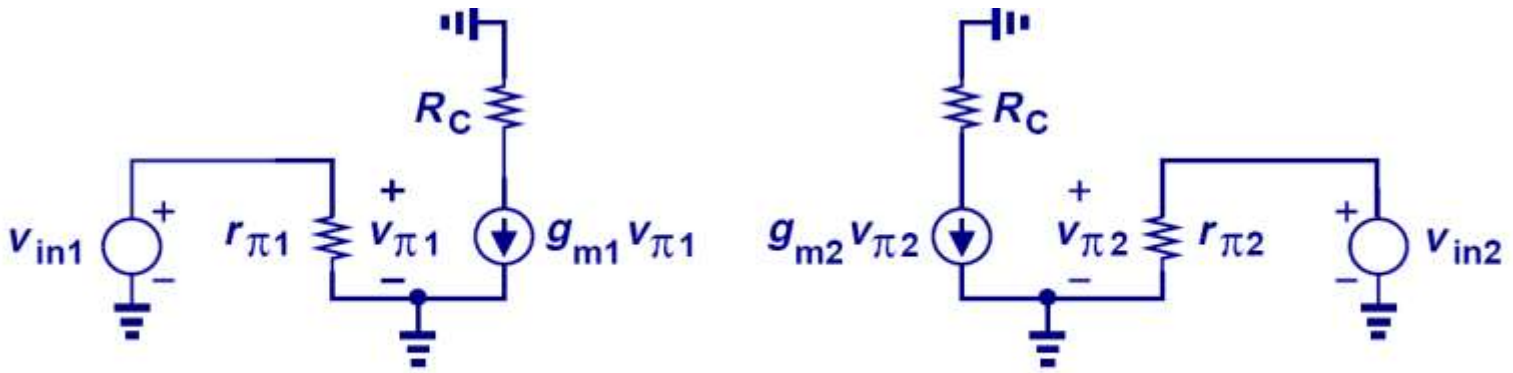
$$R_C = \frac{|A_v|}{g_m} \tag{10.41}$$

$$= 1040\,\Omega. \tag{10.42}$$

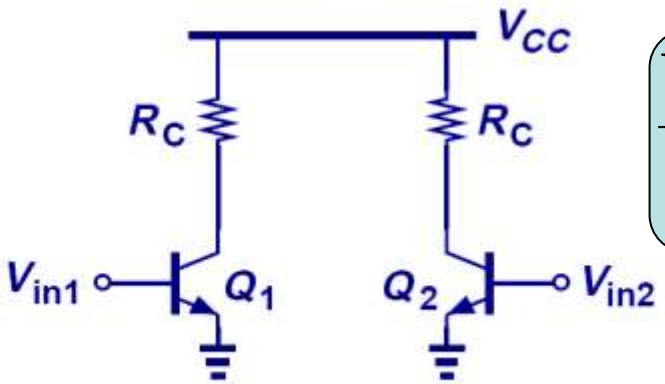
③根据增益要求和g_m，算出R_C



Half Circuits



(b)



(c)

$$\frac{v_{out1}-v_{out2}}{v_{in1}-v_{in2}}=-g_m R_C$$

- 因为 V_P 是虚拟地, 我们可以将差分对看作两个 CE 结构的电路（“half circuits”）；

$$v_{out1}=-g_m R_C v_{in1}$$
$$v_{out2}=-g_m R_C v_{in2}.$$

例题

Example 10.10

Compute the differential gain of the circuit shown in Fig. 10.16(a), where ideal current sources are used as loads to maximize the gain.

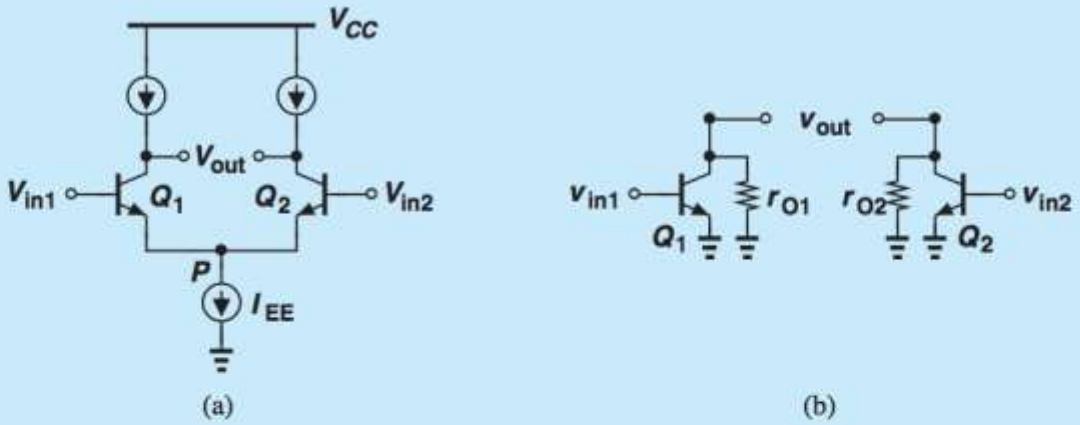


Figure 10.16

Solution With ideal current sources, the Early effect in Q_1 and Q_2 cannot be neglected, and the half circuits must be visualized as depicted in Fig. 10.16(b). Thus,

$$v_{out1} = -g_m r_O v_{in1} \tag{10.90}$$

$$v_{out2} = -g_m r_O v_{in2} \tag{10.91}$$

and hence

$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m r_O. \tag{10.92}$$

注意和我们教材中正负号的区别！

例题

Example 10.11 Figure 10.17(a) illustrates an implementation of the topology shown in Fig. 10.16(a). Calculate the differential voltage gain.

Solution Noting that each *pnp* device introduces a resistance of r_{OP} at the output nodes and drawing the half circuit as in Fig. 10.17(b), we have

$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m(r_{ON} || r_{OP}), \tag{10.93}$$

where r_{ON} denotes the output impedance of the *npn* transistors.

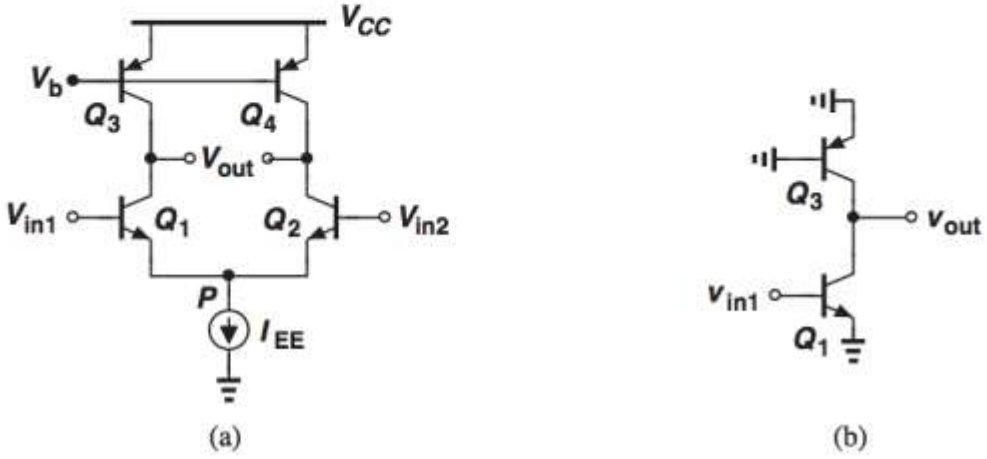
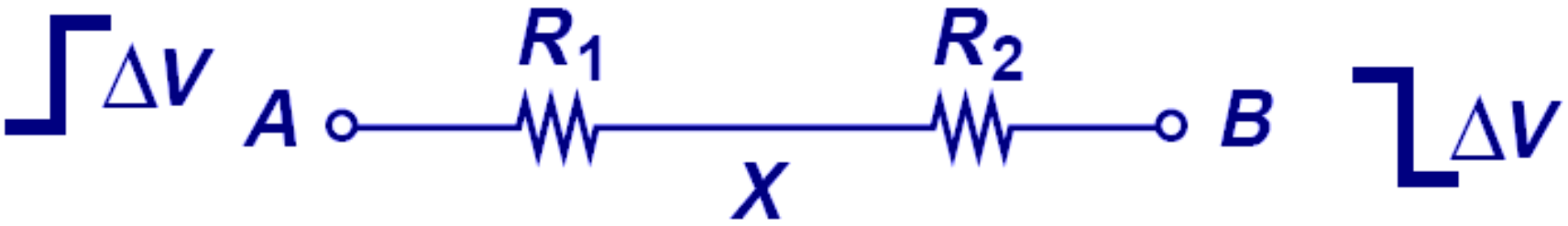


Figure 10.17

“虚拟地”的扩展



$$V_X = 0$$

- 如果 $R_1 = R_2$, 并且 V_A 的上升（下降）幅度与V_B的下降（上升）幅度一样, 那么 V_X 不变，也即小信号分析时X点为虚拟地.
- 对于对称结构的电路，若输入为差分信号，那么“对称轴上的所有结点都是虚拟地”

例题

Example 10.12 Determine the differential gain of the circuit in Fig. 10.19(a) if $V_A < \infty$ and the circuit is symmetric.

Drawing one of the half circuits as shown in Fig. 10.19(b), we express the total resistance seen at the collector of Q_1 as

$$R_{out} = r_{O1} || r_{O3} || R_1. \tag{10.94}$$

Thus, the voltage gain is equal to

$$A_v = -g_{m1}(r_{O1} || r_{O3} || R_1).$$

结构对称，且R_1=R_2

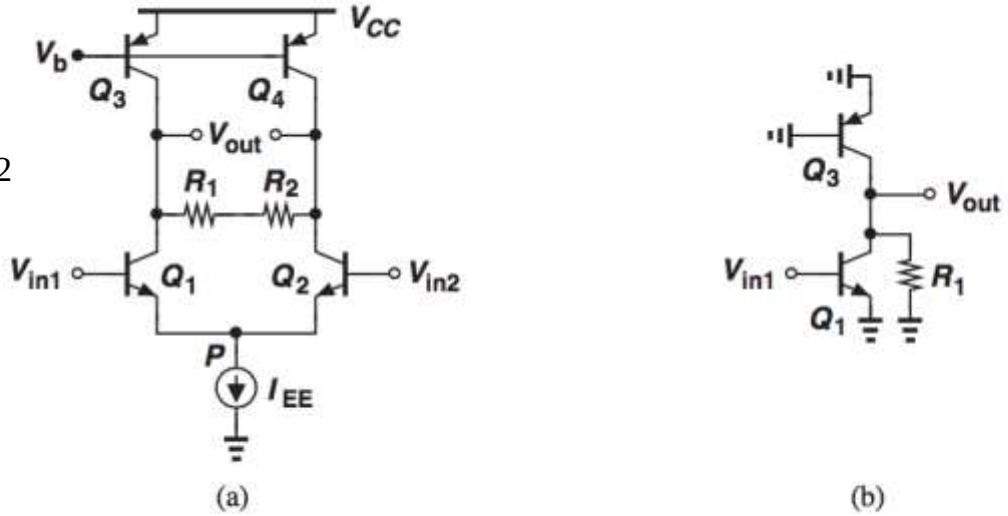


Figure 10.19

例题

Example 10.13

Calculate the differential gain of the circuit illustrated in Fig. 10.20(a) if $V_A < \infty$.

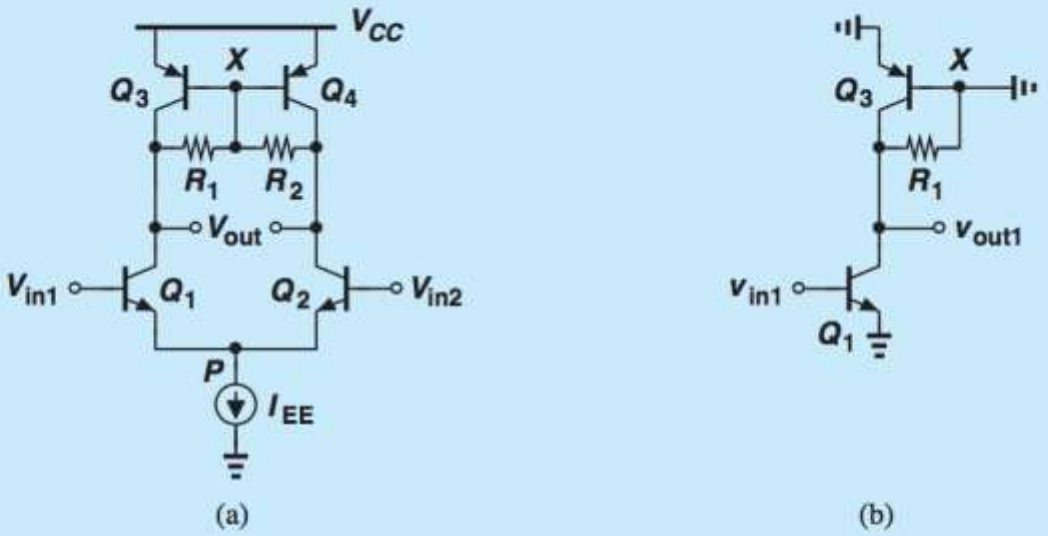


Figure 10.20

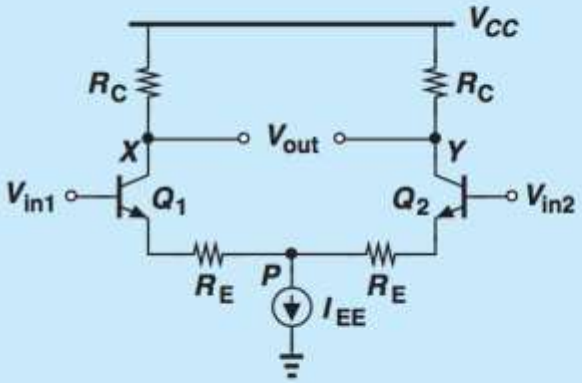
Solution For small differential inputs and outputs, V_X remains constant, leading to the conceptual half circuit shown in Fig. 10.20(b)—the same as that in the above example. This is because Q_3 and Q_4 experience a *constant* base-emitter voltage in both cases, thereby serving as current sources and exhibiting only an output resistance. It follows that

$$A_v = -g_{m1}(r_{O1} || r_{O3} || R_1). \tag{10.96}$$

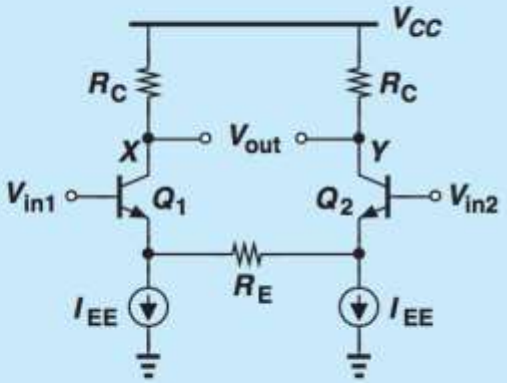
例题

Example 10.14

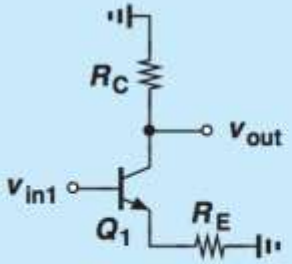
Determine the gain of the degenerated differential pairs shown in Figs. 10.21(a) and (b). Assume $V_A = \infty$.



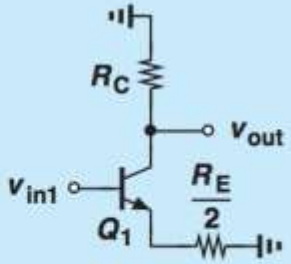
(a)



(b)



(c)

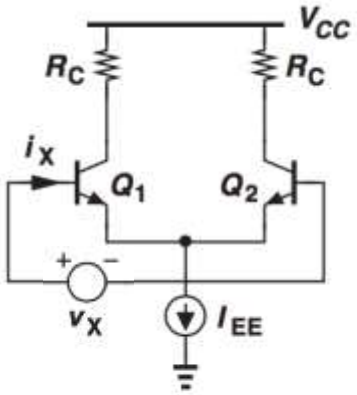


(d)

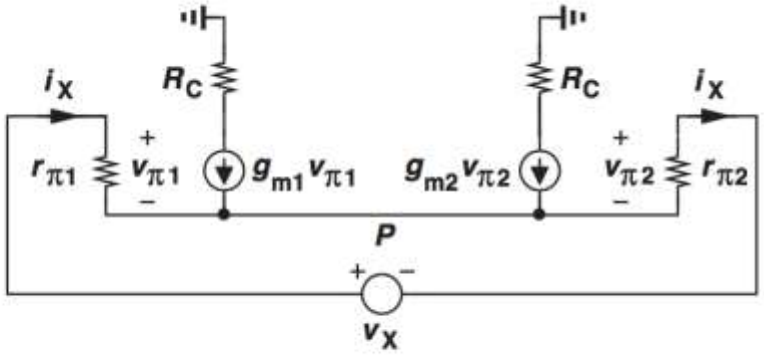
$$A_v = -\frac{R_C}{R_E + \dfrac{1}{g_m}}. \qquad A_v = -\frac{R_C}{\dfrac{R_E}{2} + \dfrac{1}{g_m}}.$$

输入输出阻抗

“differential input impedance”



(a)



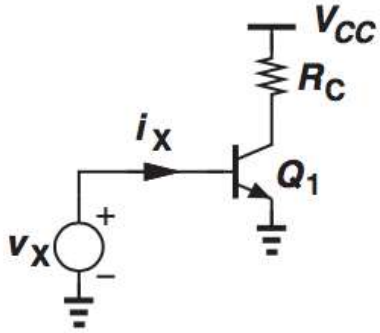
(b)

$$v_X = v_{\pi 1} - v_{\pi 2}$$

$$= 2r_{\pi 1} i_X .$$

$$\frac{v_X}{i_X} = 2r_{\pi 1},$$

“single-ended input impedance”



$$\frac{v_X}{i_X} = r_{\pi 1}.$$

In a manner similar to the foregoing development, the reader can show that the differential and single-ended output impedances are equal to $2R_C$ and R_C, respectively.

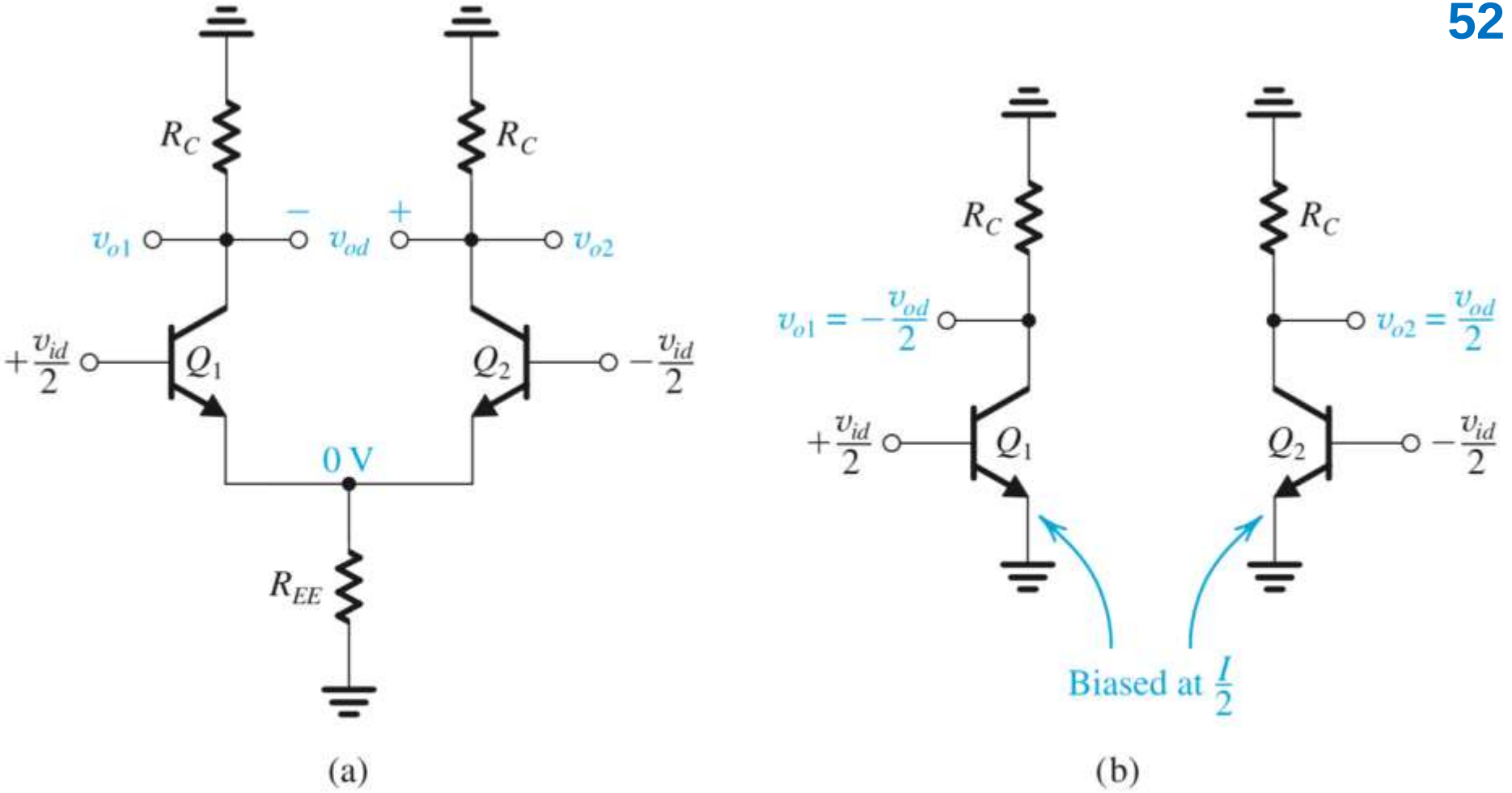


Figure 9.21 Equivalence of the BJT differential amplifier in **(a)** to the two common-emitter amplifiers in **(b).** This equivalence applies only for differential input signals. Either of the two common-emitter amplifiers in **(b)** can be used to find the differential gain, differential input resistance, frequency response, and so on, of the differential amplifier.

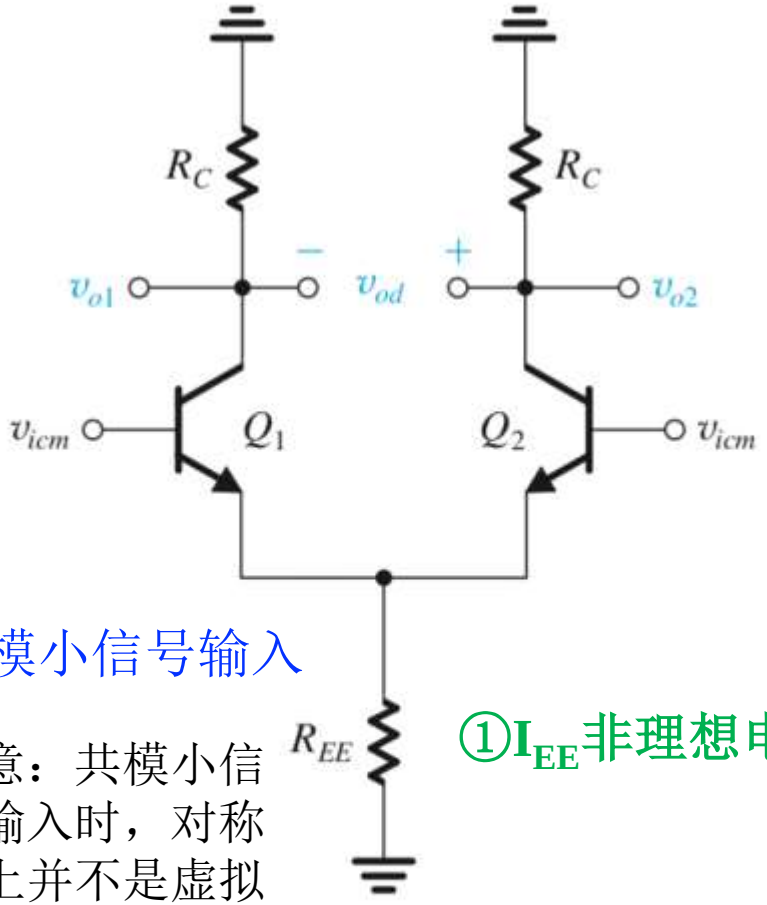
- **尾电流源的输出电阻R_{EE}对差分小信号分析无影响**

9.3.2. Common-Mode Gain and Common-Mode Rejection ratio (CMRR) 共模增益 & 共模抑制比

$$v_{o1} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \qquad v_{o2} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm}$$

$$v_{od} = v_{o2} - v_{o1} = 0$$

完美匹配时依旧无差分输出

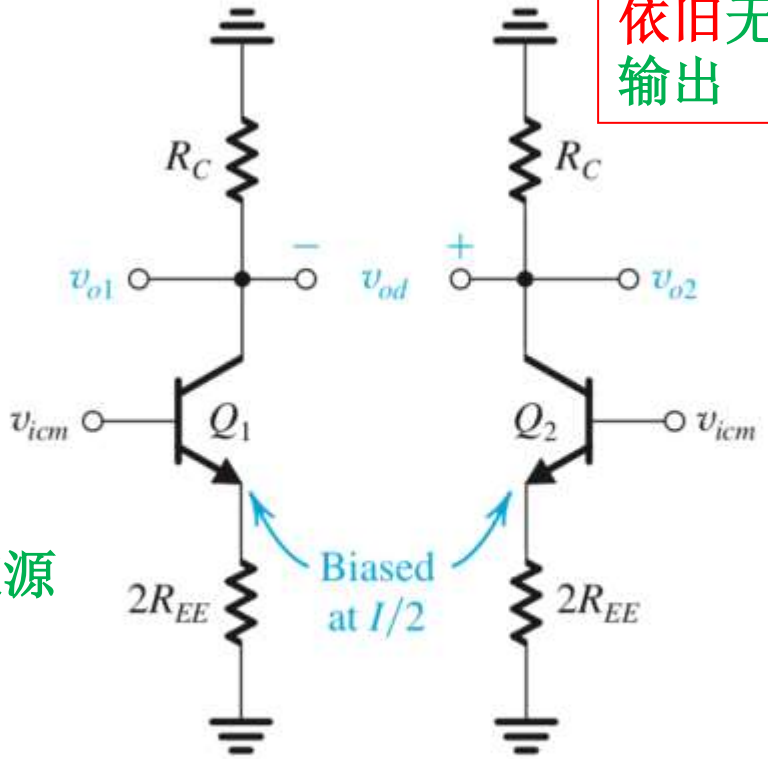


共模小信号输入

注意：共模小信号输入时，对称轴上并不是虚拟地，因为两端非跷跷板结构

①I_{EE}非理想电流源

(a)



(b)

Figure 9.26 (a) The differential amplifier fed by a common-mode input signal v_{icm}. (b) Equivalent "half-circuits" for common-mode calculations.

计算共模增益（共模小信号输入时，差分小信号的输出）

② mismatch ΔR_C ⟹

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = -\frac{\alpha \Delta R_C}{2R_{EE} + r_e}$$

Since $\alpha \simeq 1$, $r_e \ll 2R_{EE}$,

$$A_{cm} \simeq -\left(\frac{R_C}{2R_{EE}}\right)\left(\frac{\Delta R_C}{R_C}\right)$$

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|} = (2g_m R_{EE}) \Big/ \left(\frac{\Delta R_C}{R_C}\right)$$

要获得大的共模抑制比，我们可以：①提高尾电流源的输出电阻R_{EE}；②减小R_C的匹配误差

例题

Example 10.22

Determine the voltage gain of the circuit shown in Fig. 10.34(a). Assume $\lambda \neq 0$.

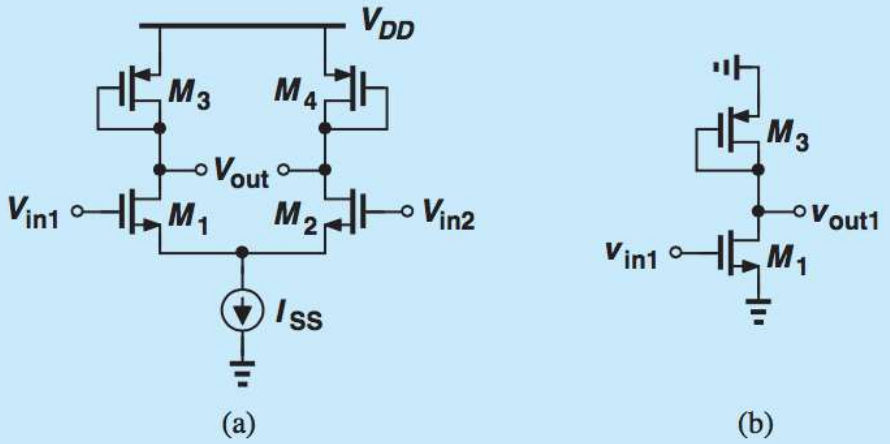


Figure 10.34

Solution Drawing the half circuit as in Fig. 10.34(b), we note that the total resistance seen at the drain of M_1 is equal to $(1/g_{m3})||r_{O3}||r_{O1}$. The voltage gain is therefore equal to

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}}||r_{O3}||r_{O1}\right). \tag{10.163}$$

例题

Example 10.23

Assuming $\lambda = 0$, compute the voltage gain of the circuit illustrated in Fig. 10.35(a).

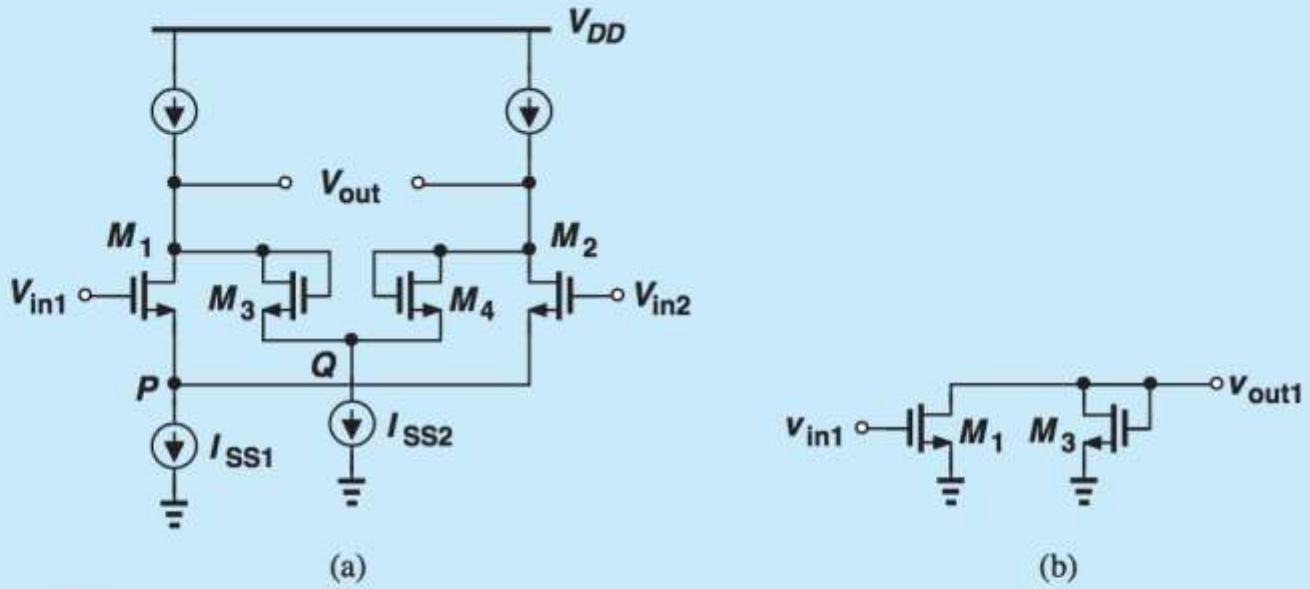


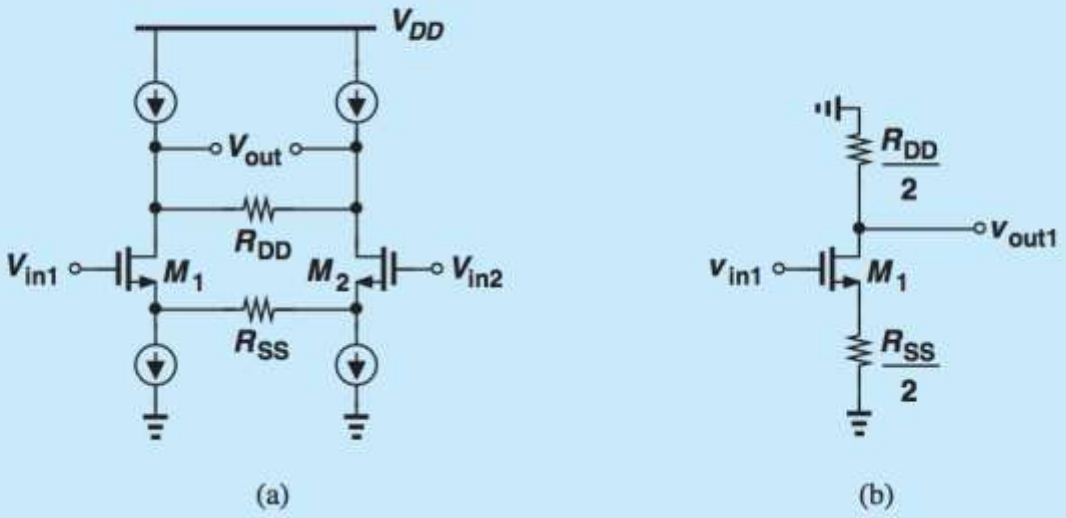
Figure 10.35

Solution Identifying both nodes P and Q as virtual grounds, we construct the half circuit shown in Fig. 10.35(b), and write

$$A_v = -\frac{g_{m1}}{g_{m3}}. \tag{10.164}$$

例题

Example 10.24 Assuming $\lambda = 0$, calculate the voltage gain of the topology shown in Fig. 10.36(a).

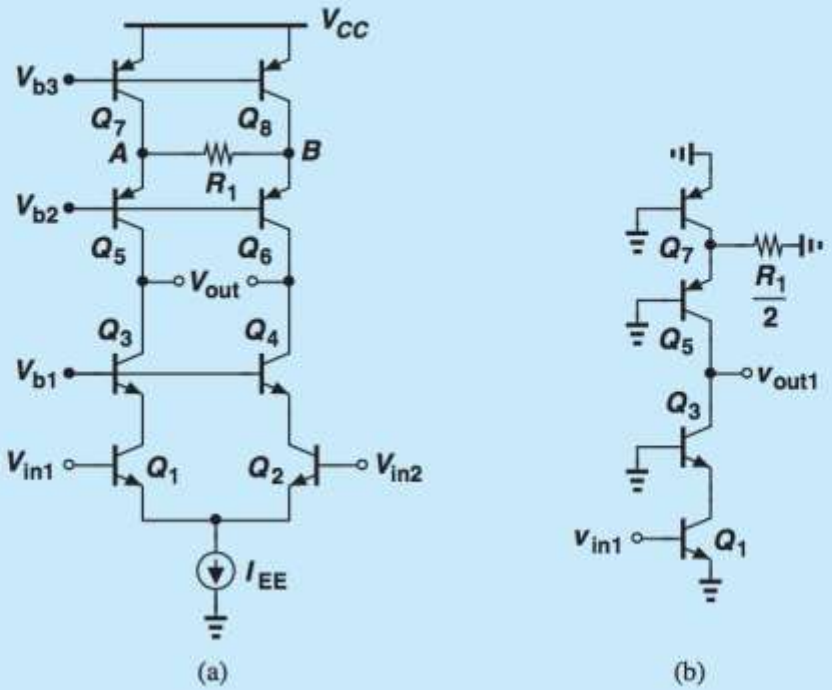


Solution Grounding the midpoint of R_{SS} and R_{DD}, we obtain the half circuit in Fig. 10.36(b), where

$$A_v = -\frac{\frac{R_{DD}}{2}}{\frac{R_{SS}}{2} + \frac{1}{g_m}}. \tag{10.165}$$

Example 10.25

Due to a manufacturing defect, a parasitic resistance has appeared between nodes A and B in the circuit of Fig. 10.39(a). Determine the voltage gain of the circuit.



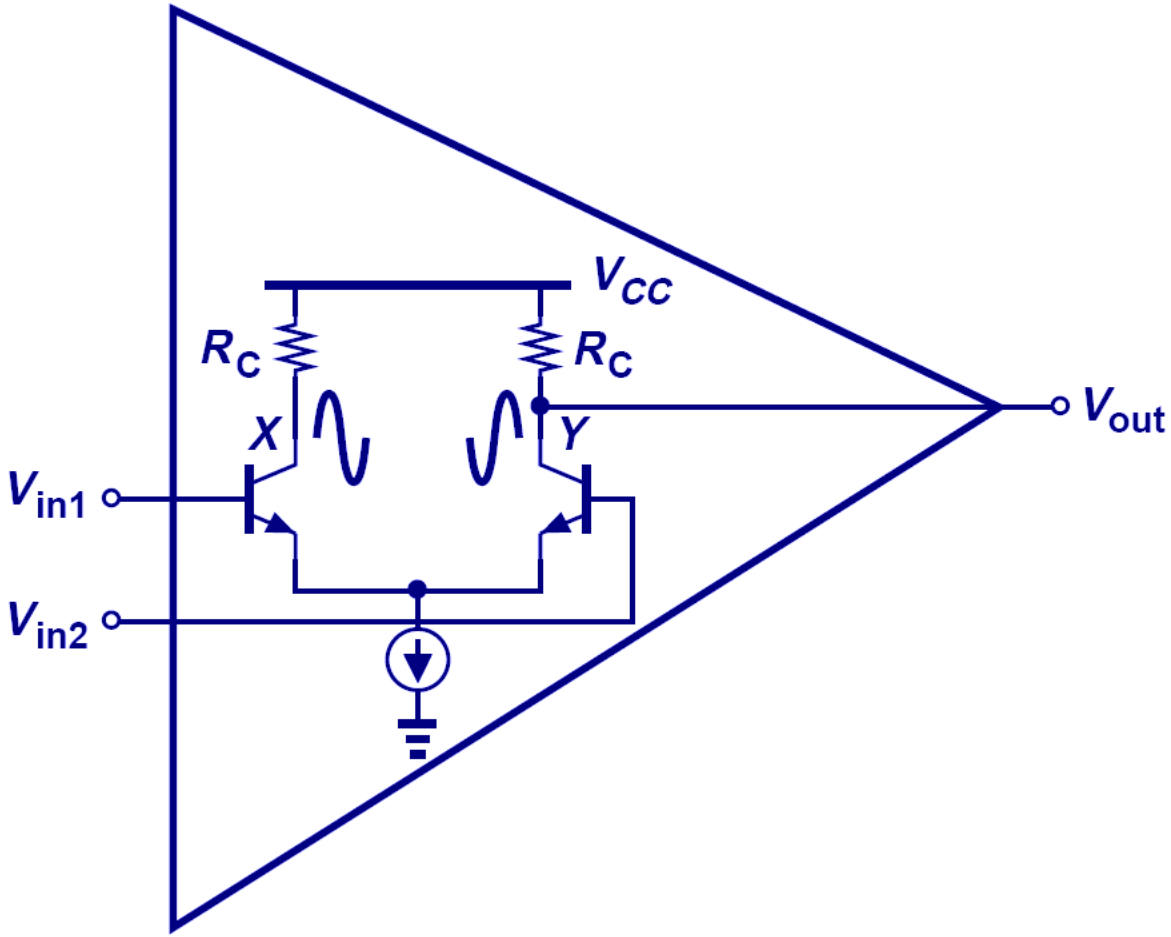
Solution The symmetry of the circuit implies that the midpoint of R_1 is a virtual ground, leading to the half circuit shown in Fig. 10.39(b). Thus, $R_1/2$ appears in parallel with r_{O7}, lowering the output impedance of the *pnp* cascode. Since the value of R_1 is not given, we cannot make approximations and must return to the original expression for the cascode output impedance, Eq. (9.1):

$$R_{op} = \left[1 + g_{m5}\left(r_{O7}||r_{\pi 5}||\frac{R_1}{2}\right)\right]r_{O5} + r_{O7}||r_{\pi 5}||\frac{R_1}{2}. \tag{10.168}$$

The resistance seen looking down into the *npn* cascode remains unchanged and approximately equal to $g_{m3}r_{O3}(r_{O1}||r_{\pi 3})$. The voltage gain is therefore equal to

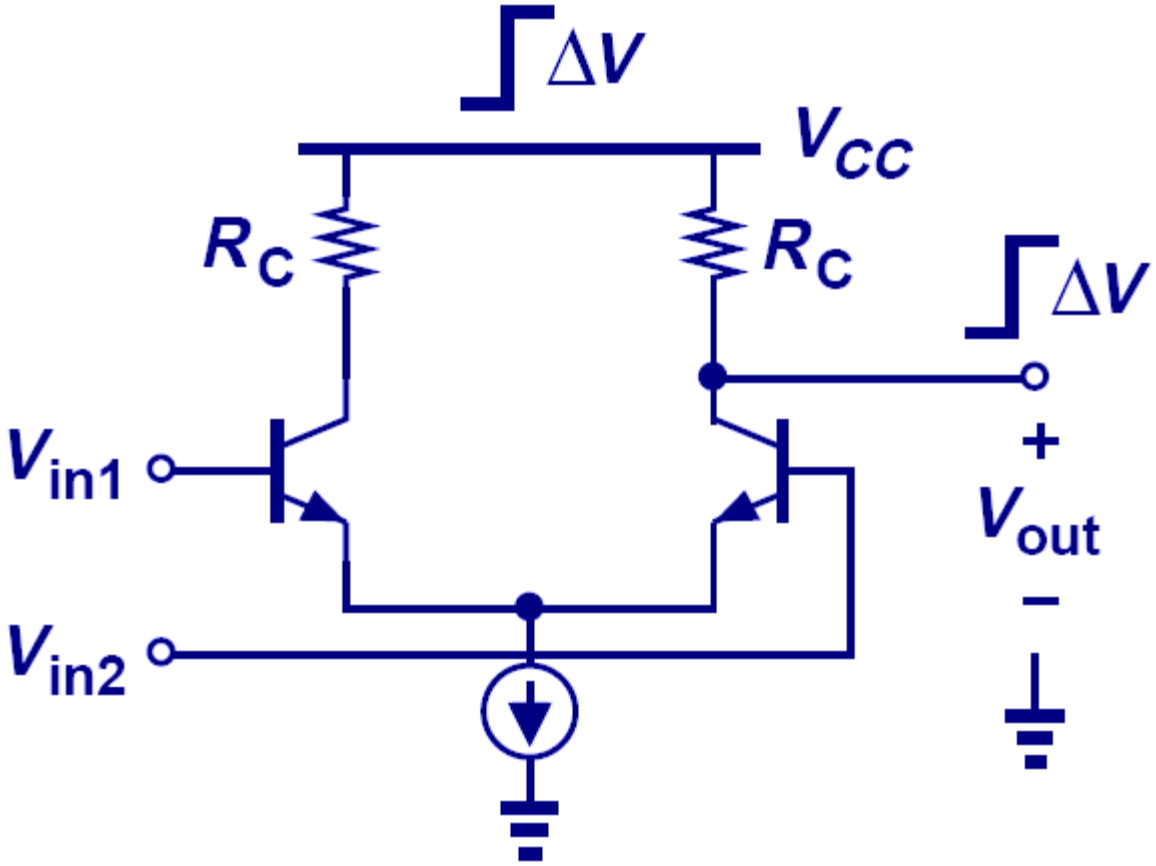
$$A_v = -g_{m1}[g_{m3}r_{O3}(r_{O1}||r_{\pi 3})]||R_{op}. \tag{10.169}$$

“差分-单端” 转换



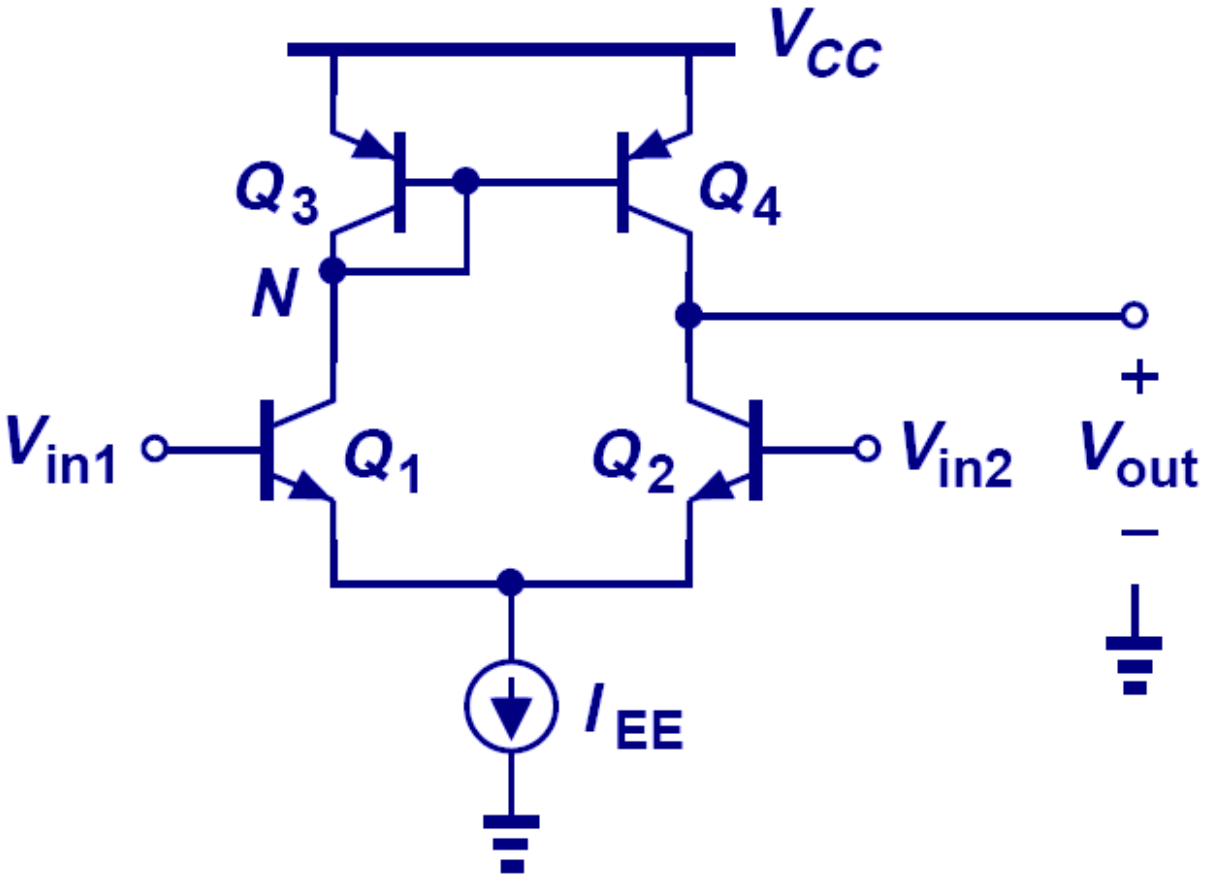
- 实际应用中，很多电路需要输入信号为差分形式，而输出信号为单端形式，如运算放大器等.

供电电压噪声的影响

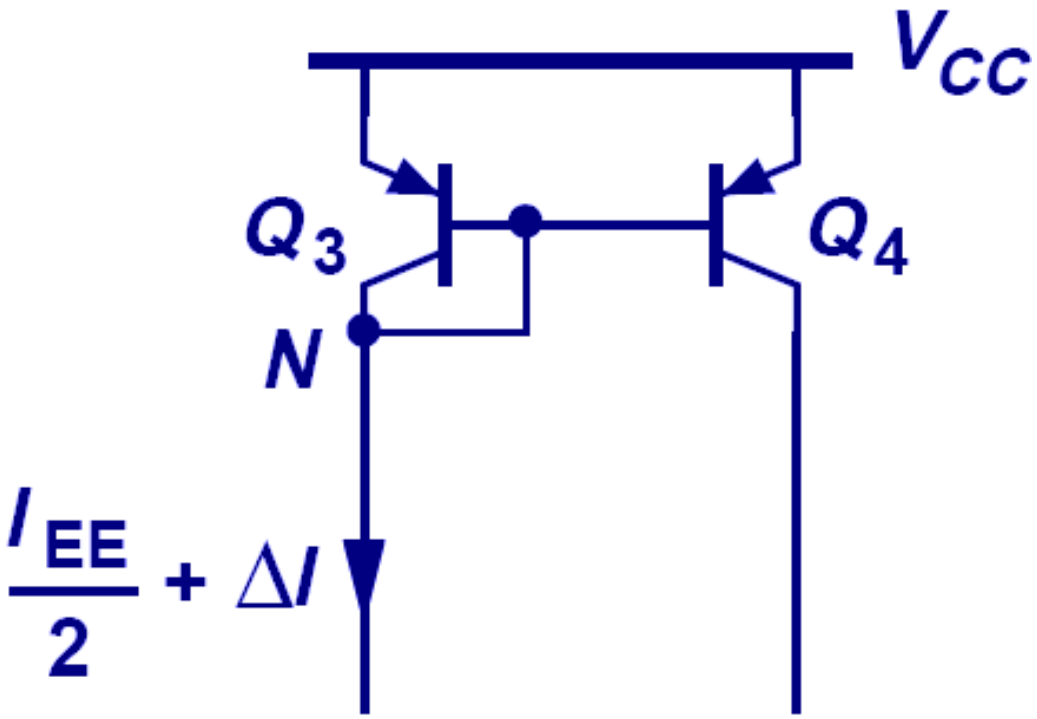


- 该结构存在的问题有：①V_{CC}的噪声将直接体现到V_{out}；②左边支路没有充分利用，对增益无贡献；

更好的结构

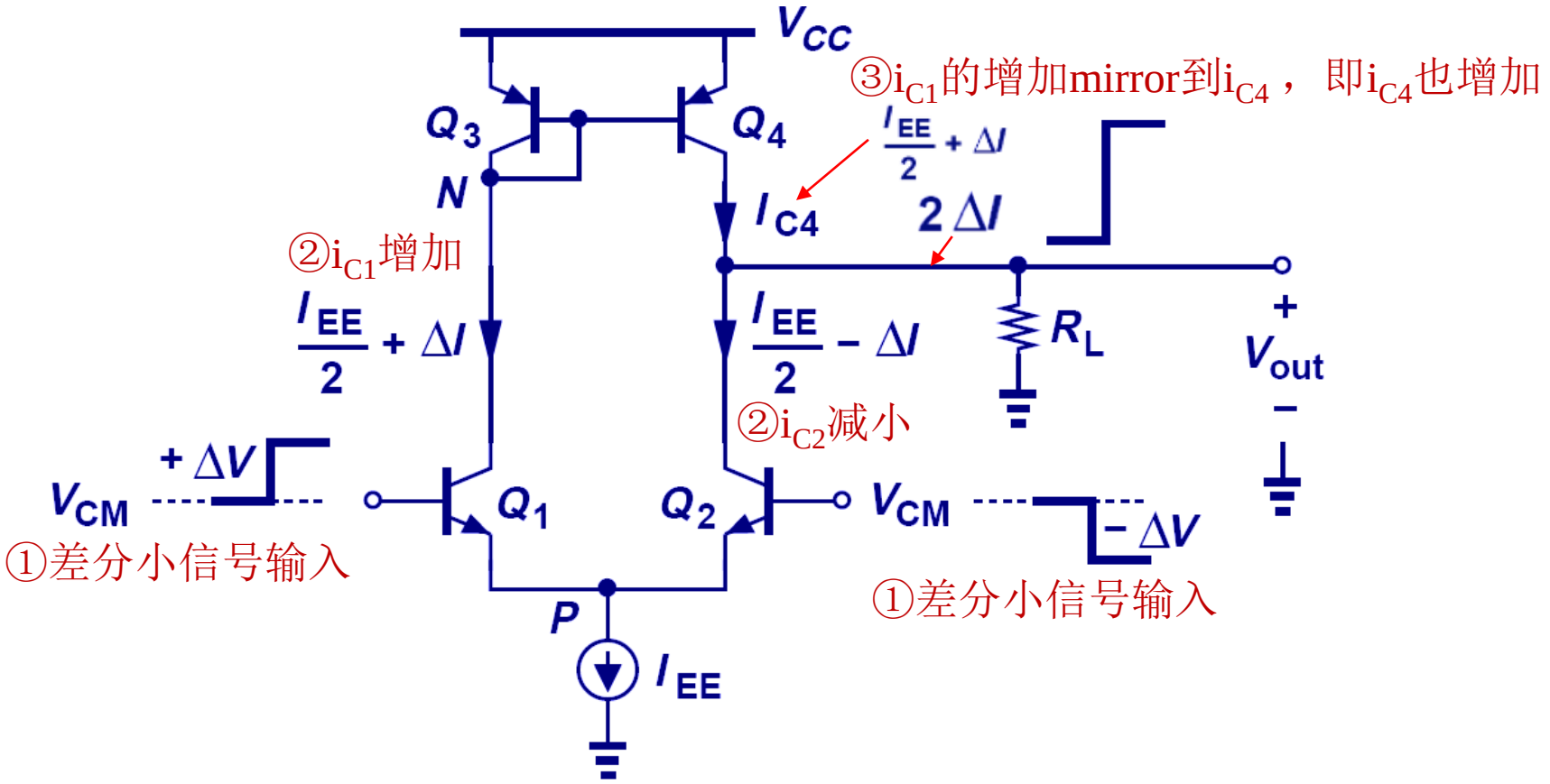


电流镜作为负载



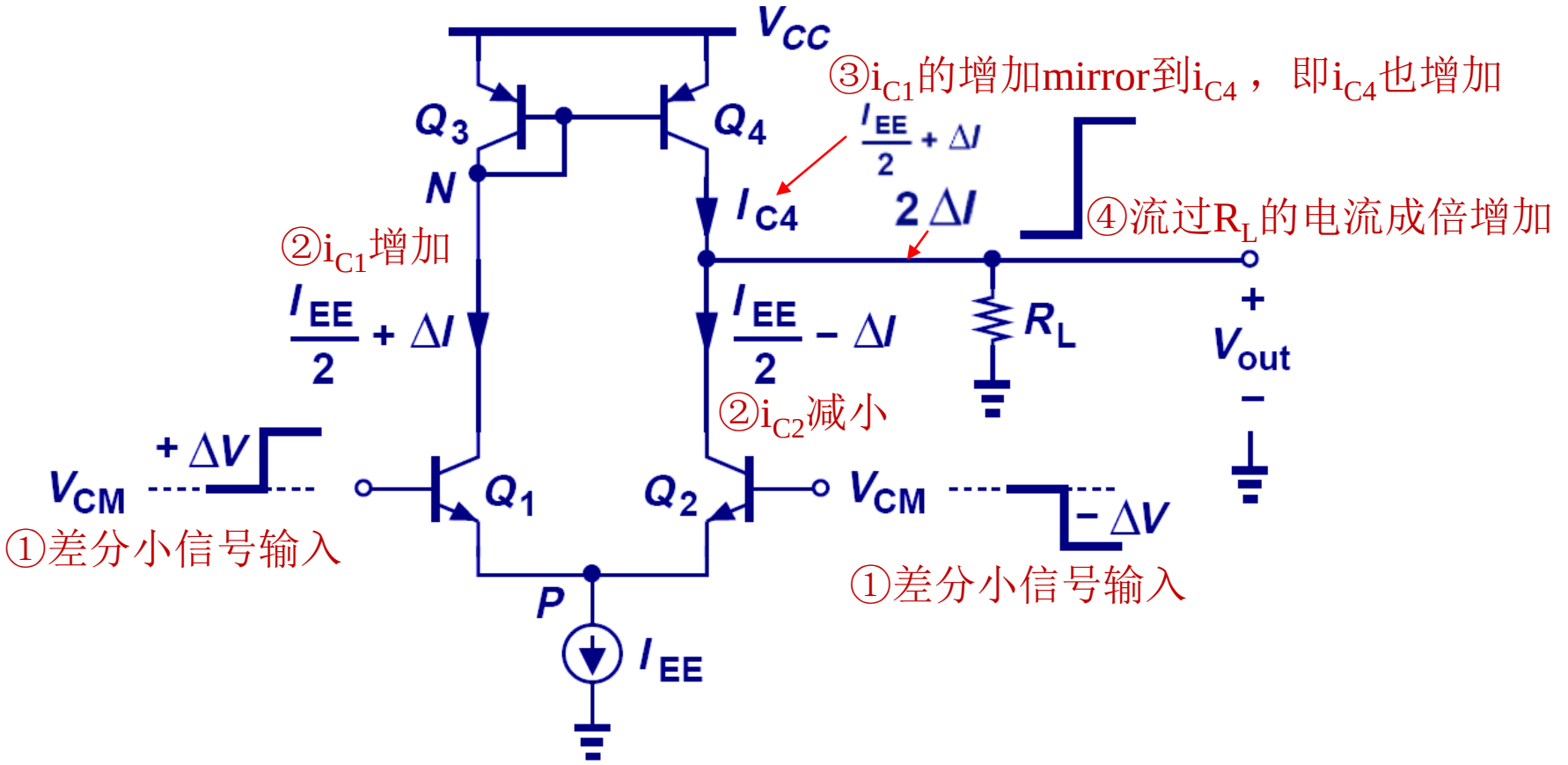
- With current mirror used as the load, the signal current produced by the Q_1 can be replicated onto Q_4.

Differential Pair with Current-Mirror Load



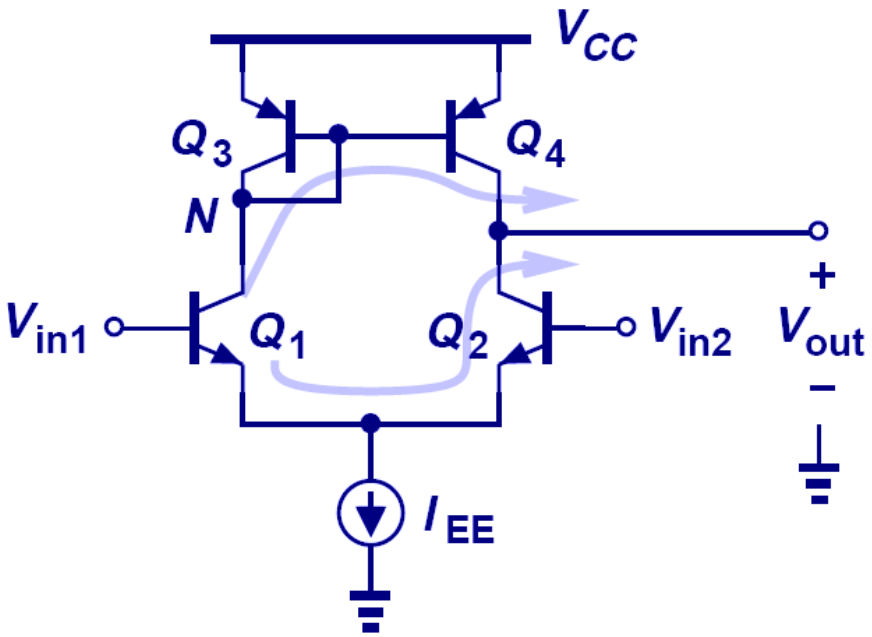
- **The input differential pair decreases the current drawn from R_L by ΔI and the active load pushes an extra ΔI into R_L by current mirror action; these effects enhance each other.**

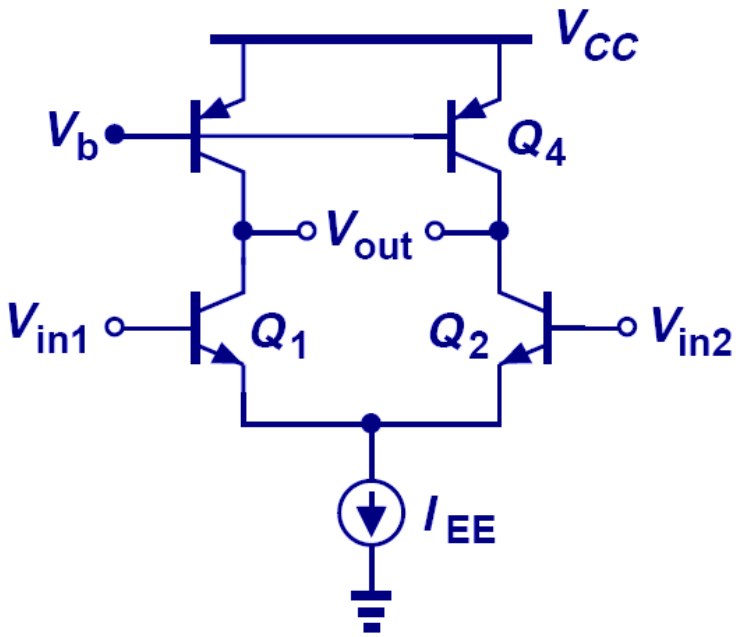
Differential Pair with Current-Mirror Load



- **The input differential pair decreases the current drawn from R_L by ΔI and the active load pushes an extra ΔI into R_L by current mirror action; these effects enhance each other.**

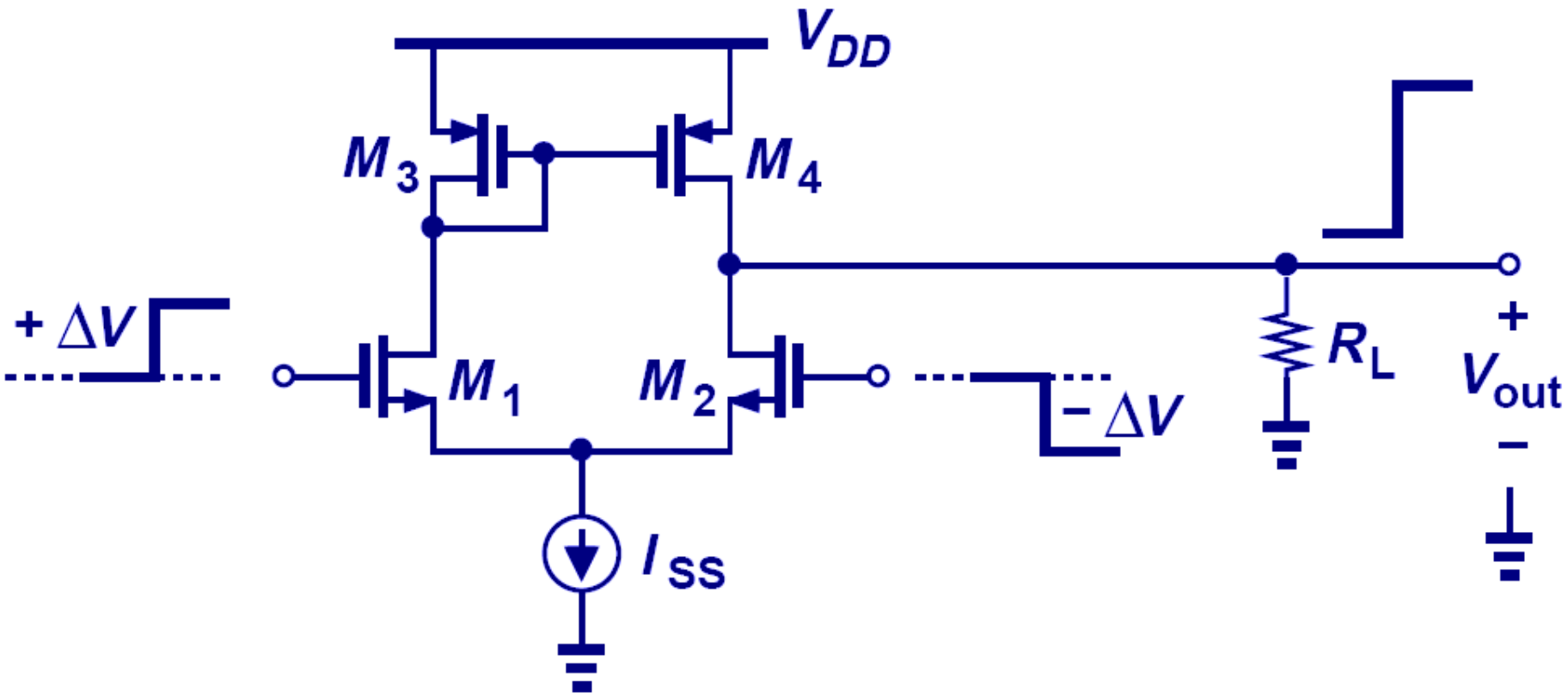
Current-Mirror Load





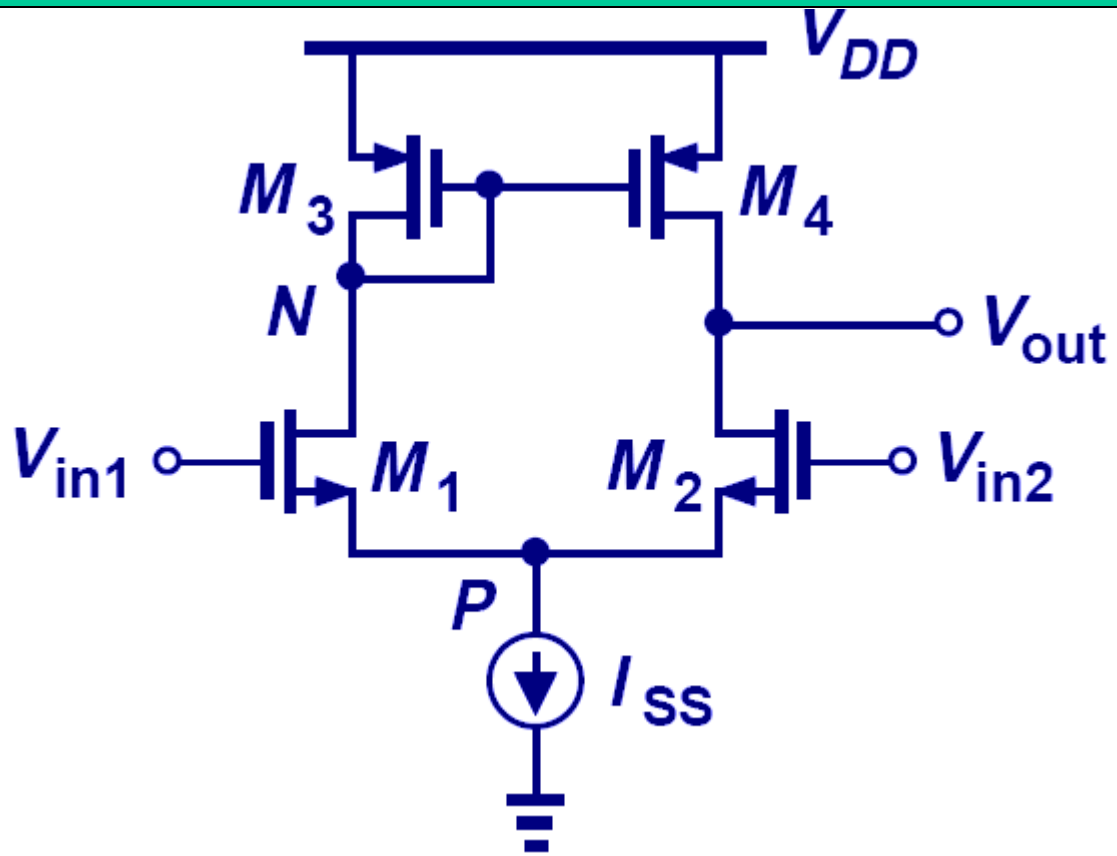
- **Current-Mirror Load:** 两路信号增强；

MOS Differential Pair with Current-Mirror Load



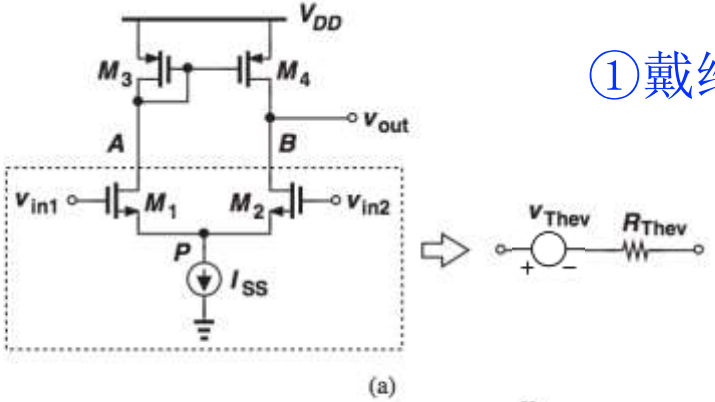
- 与三极管类似， **MOS** 差分对也可以使用 **current-mirror load** 来增强单端信号的输出.

非对称性



- 因为 **current-mirror load** 导致了电路的非对称，所以**P**点将不再是虚拟地；
- 同时因为**N**点的输出电阻比V_{out}点要小（$1/g_m$），所以**N**点的电压摆幅比V_{out}也要小

分析方法

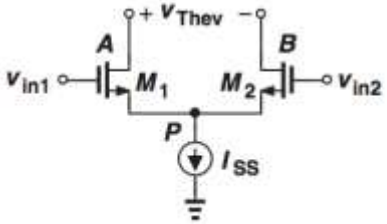


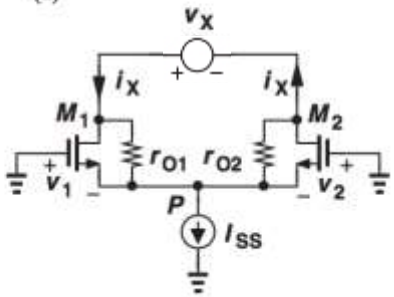
①戴维南等效

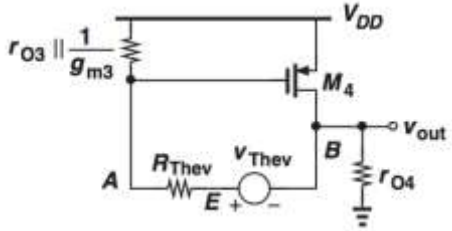
$$v_{Thev} = -g_{mN} r_{ON} (v_{in1} - v_{in2}).$$

$$(i_X - g_{m1} v_1) r_{O1} + (i_X + g_{m2} v_2) r_{O2} = v_X$$

$$R_{Thev} = 2 r_{ON}.$$







V_{GS4}

②对B点写KCL

$$\left(g_{m4} \frac{\frac{1}{g_{m3}} \Big\| r_{O3}}{\frac{1}{g_{m3}} \Big\| r_{O3} + R_{Thev}} + \frac{1}{\frac{1}{g_{m3}} \Big\| r_{O3} + R_{Thev}} \right) (v_{out} + v_{Thev}) + \frac{v_{out}}{r_{O4}} = 0. \quad (10.206)$$

$$v_A = \frac{\frac{1}{g_{m3}} \Big\| r_{O3}}{\frac{1}{g_{m3}} \Big\| r_{O3} + R_{Thev}} (v_{out} + v_{Thev})$$

$$g_{m4} v_A + \frac{v_{out}}{r_{O4}} + \frac{v_{out} + v_{Thev}}{\frac{1}{g_{m3}} \Big\| r_{O3} + R_{Thev}} = 0,$$

Recognizing that $1/g_{m3} \ll r_{O3}$, and $1/g_{m3} \ll R_{Thev}$ and assuming $g_{m3} = g_{m4} = g_{mp}$ and $r_{O3} = r_{O4} = r_{OP}$, we reduce Eq. (10.206) to

$$\frac{2}{R_{Thev}} (v_{out} + v_{Thev}) + \frac{v_{out}}{r_{OP}} = 0. \quad (10.207)$$

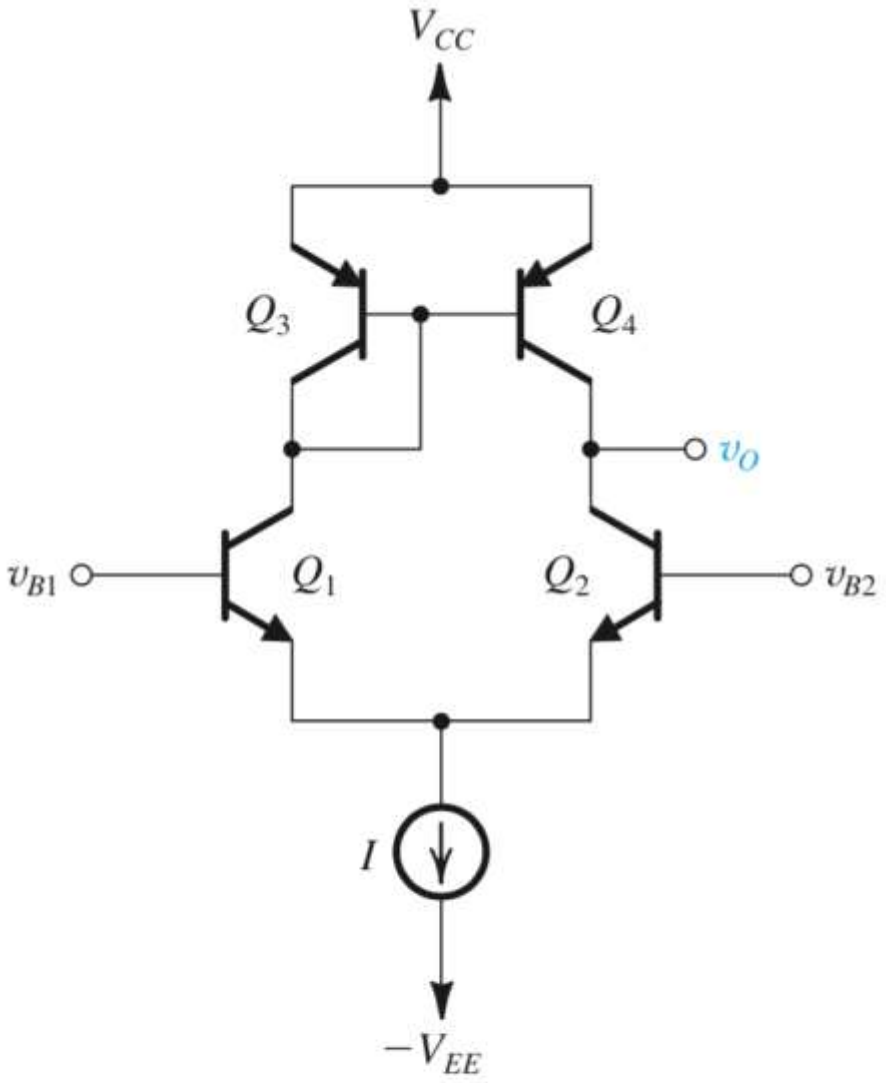
Equations v_{Thev} and (10.207) therefore give

$$v_{out} \left(\frac{1}{r_{ON}} + \frac{1}{r_{OP}} \right) = \frac{g_{mN} r_{ON} (v_{in1} - v_{in2})}{r_{ON}} \quad (10.208)$$

and hence

$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN} (r_{ON} \| r_{OP}). \quad (10.209)$$

结论： $G_m = g_m \quad R_o = r_{o2} \| r_{o4}$



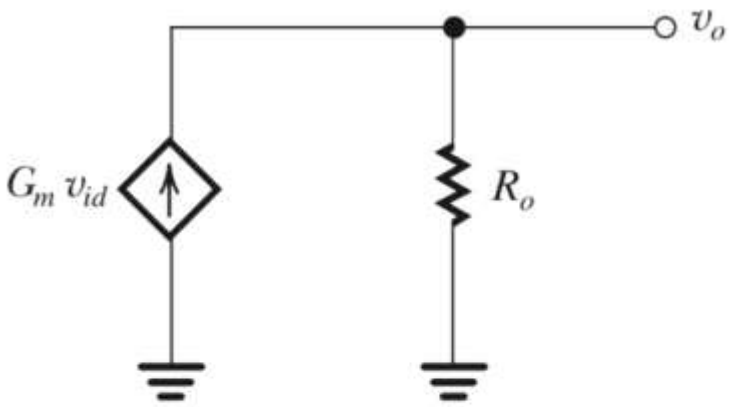
(a)

$$G_m = g_{m1,2}$$

$$R_o = r_{o2} \parallel r_{o4}$$

$$A_d \equiv \frac{v_o}{v_{id}} = G_m R_o = g_m (r_{o2} \parallel r_{o4})$$

$$R_{id} = 2r_\pi$$



(b)

Figure 9.36 **(a)** Current-mirror-loaded bipolar differential pair. **(b)** Small-signal equivalent circuit of the amplifier output when a differential signal $v_{id} \equiv v_{B1} - v_{B2}$ is applied.

9.6 Multistage Amplifiers

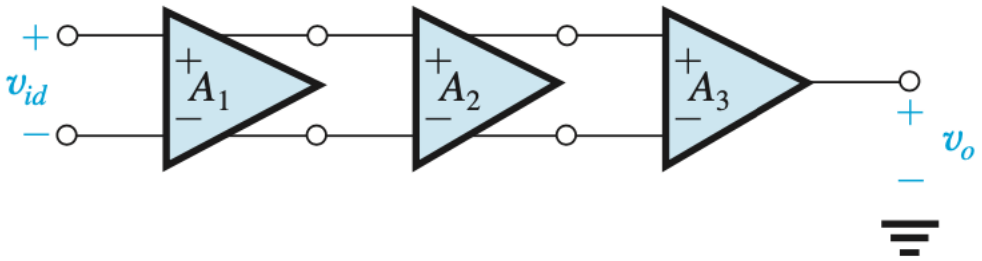
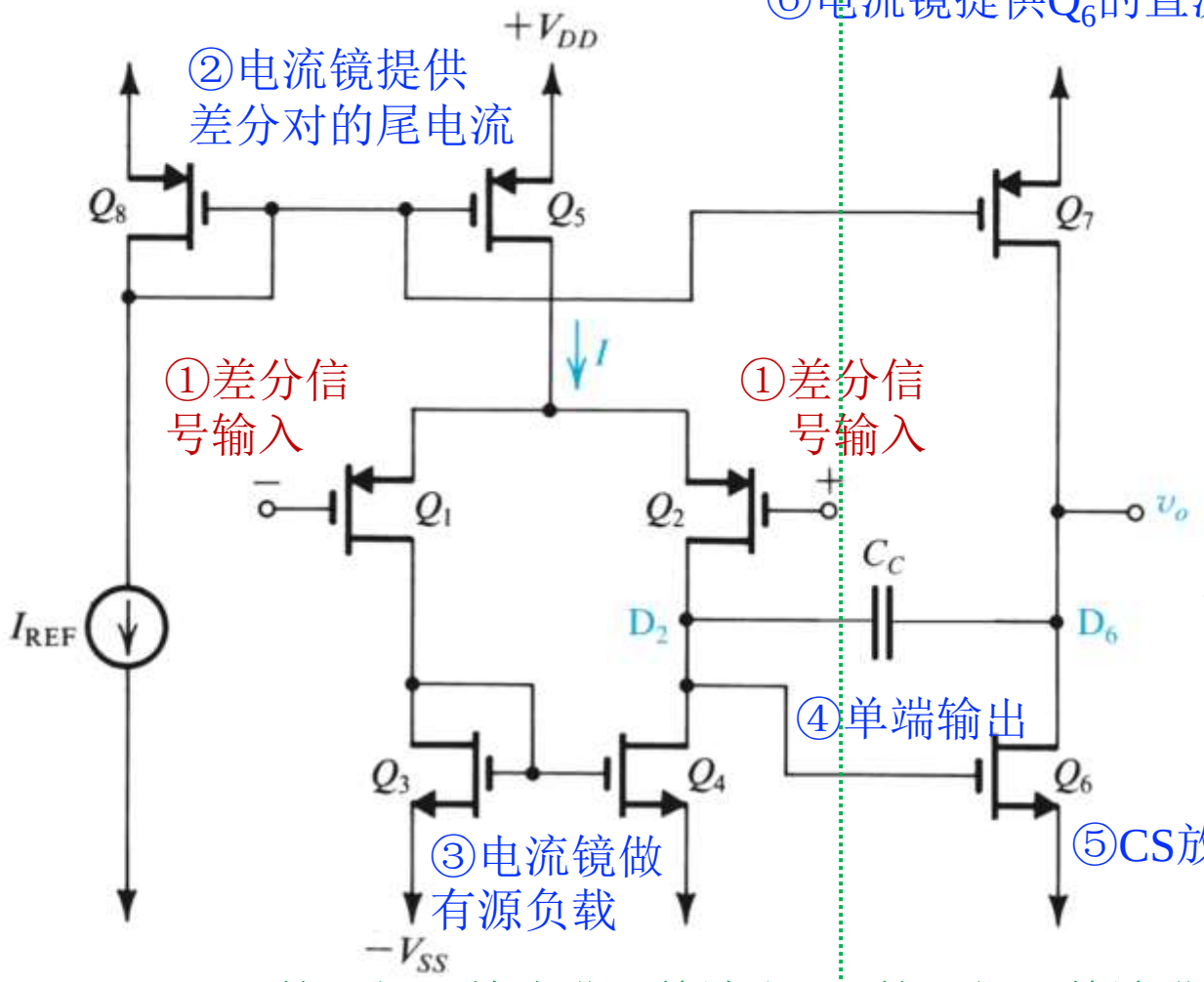


Figure 9.30 A three-stage amplifier consisting of two differential-in, differential-out stages, A_1 and A_2, and a differential-in, single-ended-out stage A_3.

9.6 Multistage Amplifiers

Q: C_C的作用？需学完频率响应后再来理解



⑥电流镜提供Q_6的直流偏置电流

缺点：输出阻抗比较大。

但适用于IC中的运算放大器（IC中不需要驱动小电阻负载）

⑦单端信号输出

$$A_1 = -g_{m1}(r_{o2} \| r_{o4})$$

$$A_2 = -g_{m6}(r_{o6} \| r_{o7})$$

Figure 9.40 Two-stage CMOS op-amp configuration.

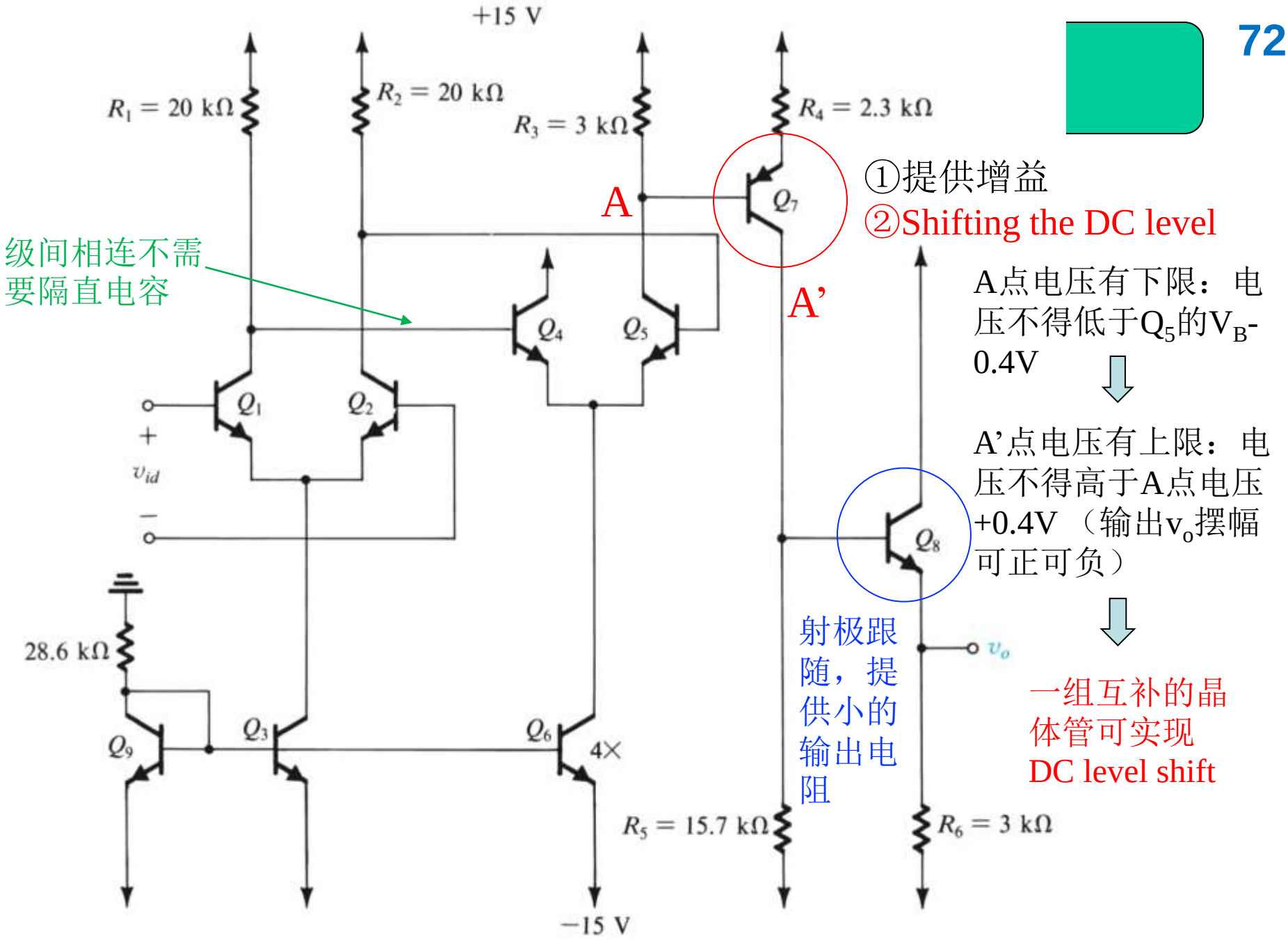
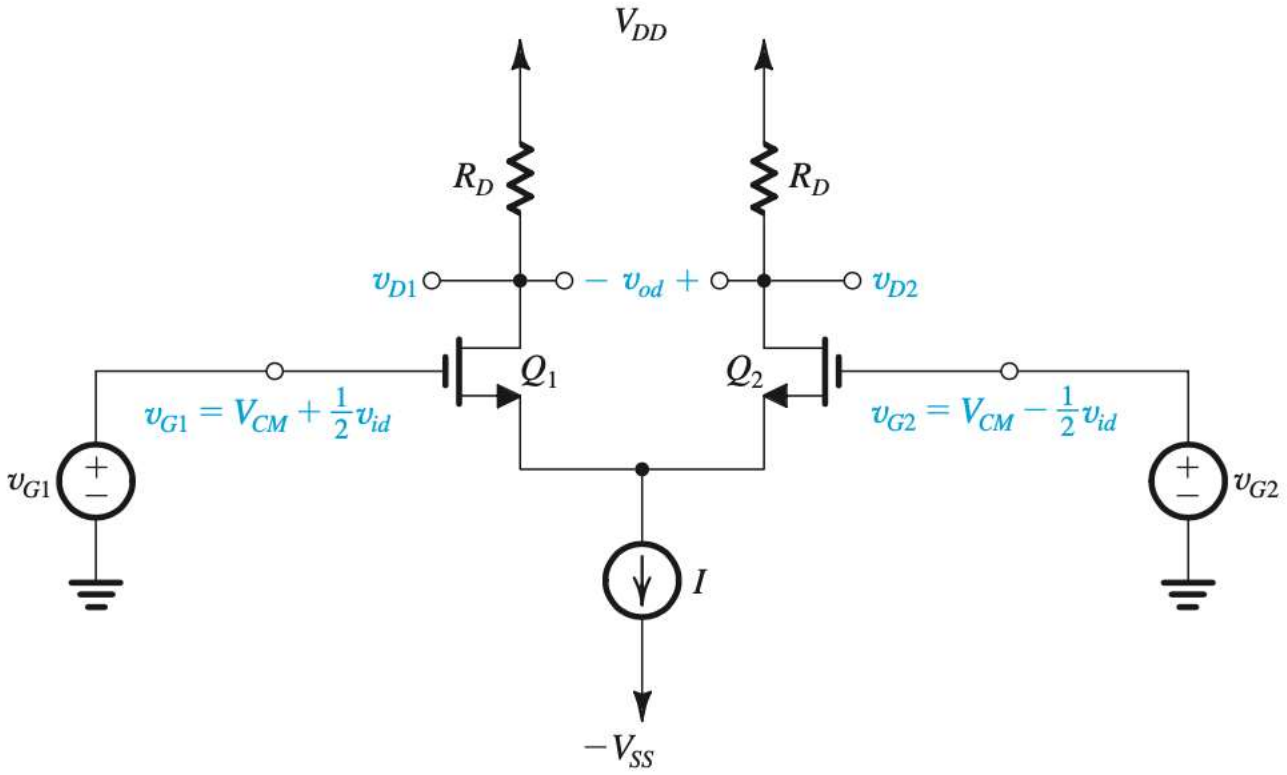


Figure 9.41 A four-stage bipolar op amp.

作业

9.4 A MOS differential amplifier is operated at a total current of 0.8 mA, using transistors with a W/L ratio of 100, $\mu_n C_{ox} = 0.2\ \text{mA/V}^2$, $V_A = 20$ V, and $R_D = 5\ \text{k}\Omega$. Find V_{OV}, g_m, r_o, and A_d.

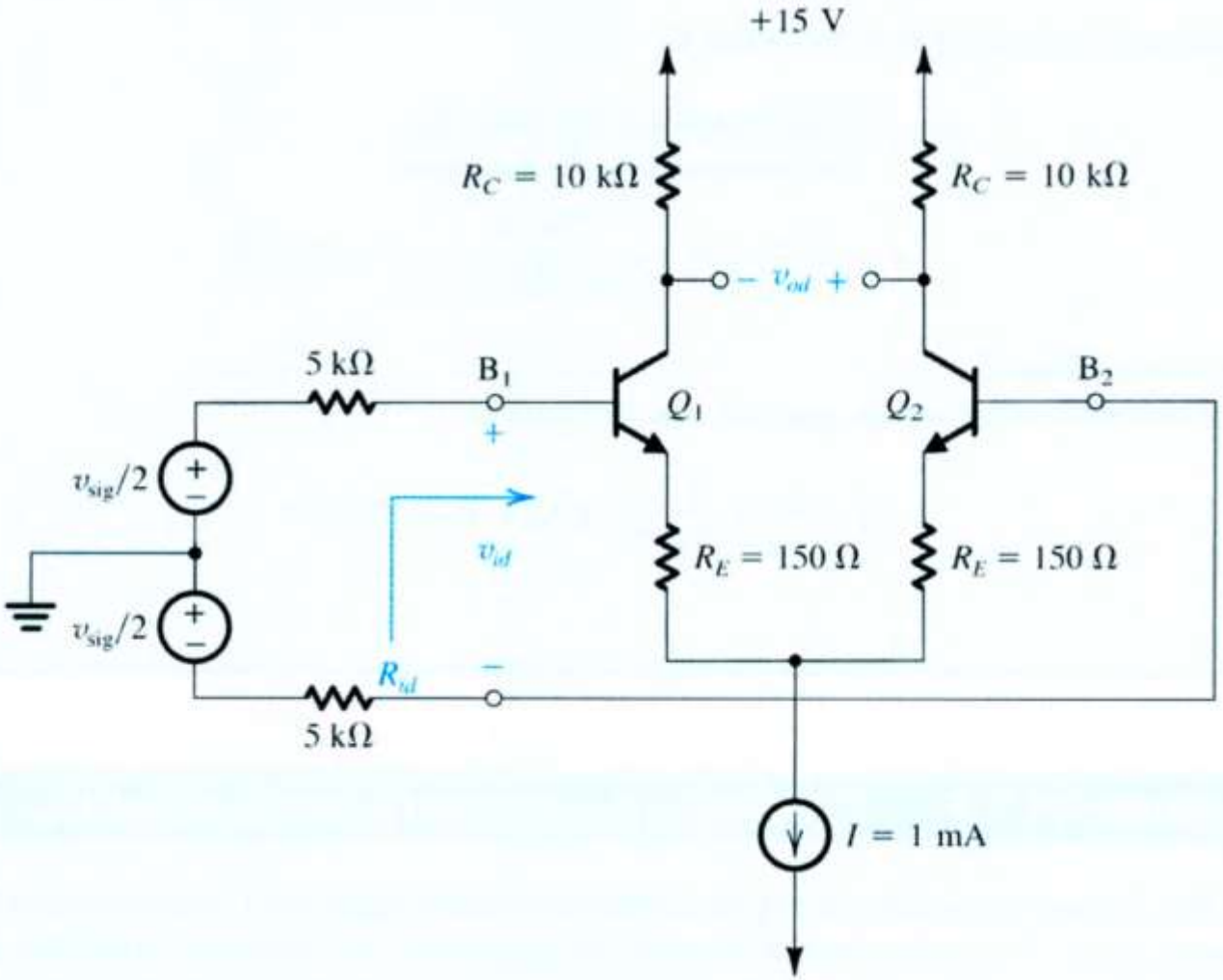
Ans. 0.2 V; 4 mA/V; 50 kΩ; 18.2 V/V



Example 9.3

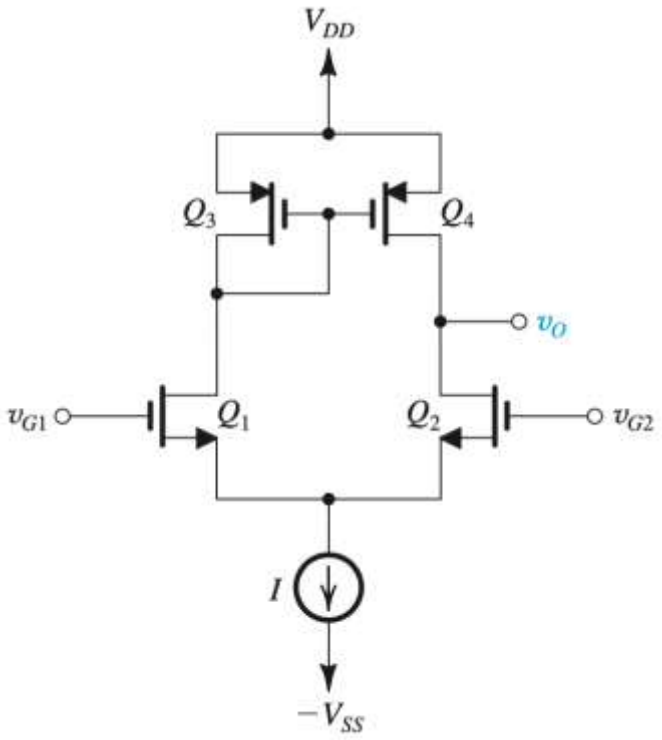
The differential amplifier in Fig. 9.23 uses transistors with $\beta = 100$. Evaluate the following:

(a) The input differential resistance R_{id}.
(b) The overall differential voltage gain v_{od}/v_{sig} (neglect the effect of r_o).



9.17 A current-mirror-loaded MOS differential amplifier of the type shown in Fig. 9.32(a) is specified as follows: $(W/L)_n = 100$, $(W/L)_p = 200$, $\mu_n C_{ox} = 2\mu_p C_{ox} = 0.2\ \text{mA/V}^2$, $V_{An} = |V_{Ap}| = 20$ V, and $I = 0.8$ mA. Calculate G_m, R_o, and A_d.

Ans. 4 mA/V; 25 kΩ; 100 V/V



Example 9.6

Consider the circuit in Fig. 9.37 with the following device geometries (in μm).

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	10/0.4	10/0.4	2.5/0.4	2.5/0.4	20/0.4	5/0.4	20/0.4	20/0.4

Let $I_{REF} = 100\,\mu A$, $V_{tn} = 0.5\,V$, $V_{tp} = -0.5\,V$, $\mu_n C_{ox} = 400\,\mu A/V^2$, $\mu_p C_{ox} = 100\,\mu A/V^2$, $|V_A|$ (for all devices) $= 5\,V$, $V_{DD} = V_{SS} = 1\,V$. For all devices, evaluate I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, and r_o. Also find A_1, A_2, the dc open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of V_A on bias current.