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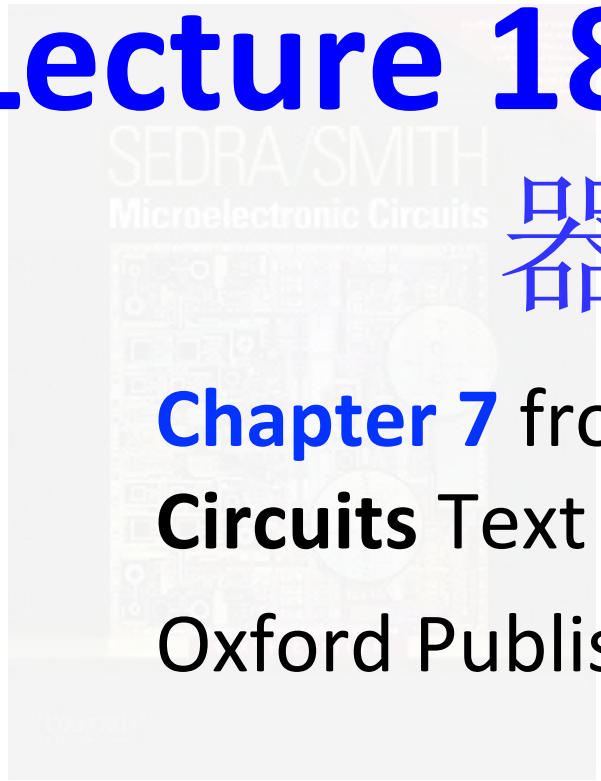
Lecture 18 – 晶体管放大器-part2



Chapter 7 from **Microelectronic Circuits** Text by Sedra and Smith

Oxford Publishing

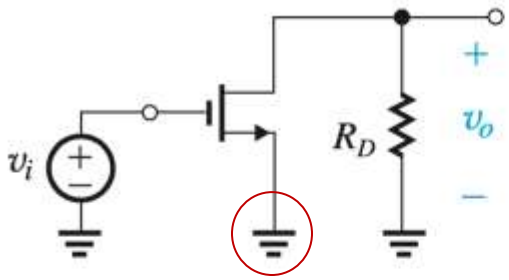
- 8.2.2 π型和T型等效电路（中频）
- 8.3 场效应晶体管放大电路的构成及其分析
- 8.3.1 直流偏置电路及其分析
- 8.3.2 三种接法放大电路的分析计算

- 9.2.2 π型和T型等效电路（中频）
- 9.3 三极管放大电路的构成及其分析
- 9.3.1 直流偏置电路及其分析
- 9.3.2 三种接法放大电路的分析计算

三种基本的晶体管放大器结构

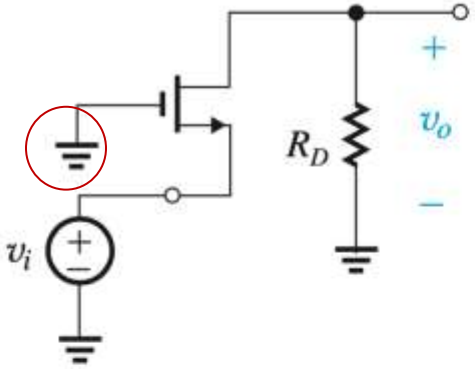
- 先不考虑直流偏置，分析三种基本的晶体管放大器结构（小信号分析）
- 再考虑直流偏置的实现
- 最后构成完整的分立元件的晶体管放大器电路（PCB级）

三个terminals中，选择其中一个接地，另两个terminals分别与其组成两个ports，这一terminal被两个ports共享，所以称为“common *”（共*）



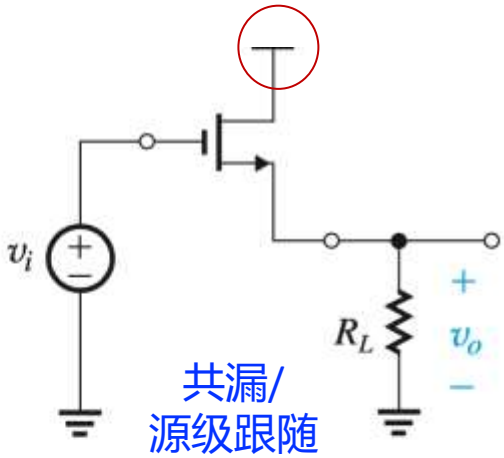
(a) Common Source (CS)

共源



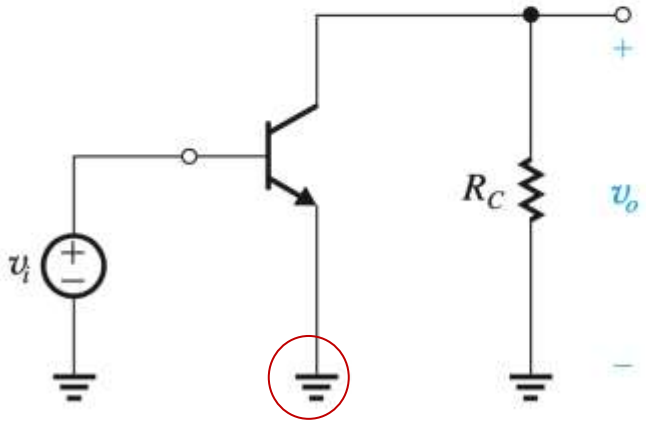
(b) Common Gate (CG)

共栅



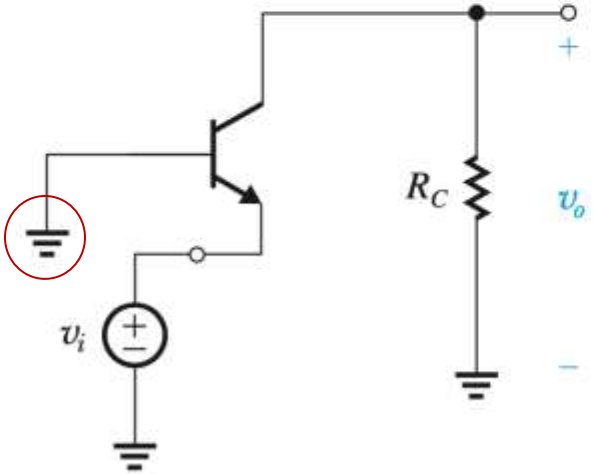
共漏/
源级跟随

(c) Common Drain (CD)
or Source Follower



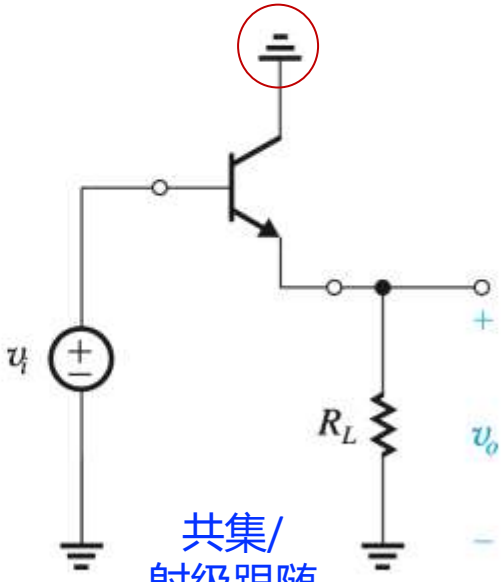
(d) Common-Emitter (CE)

共射



(e) Common-Base (CB)

共基

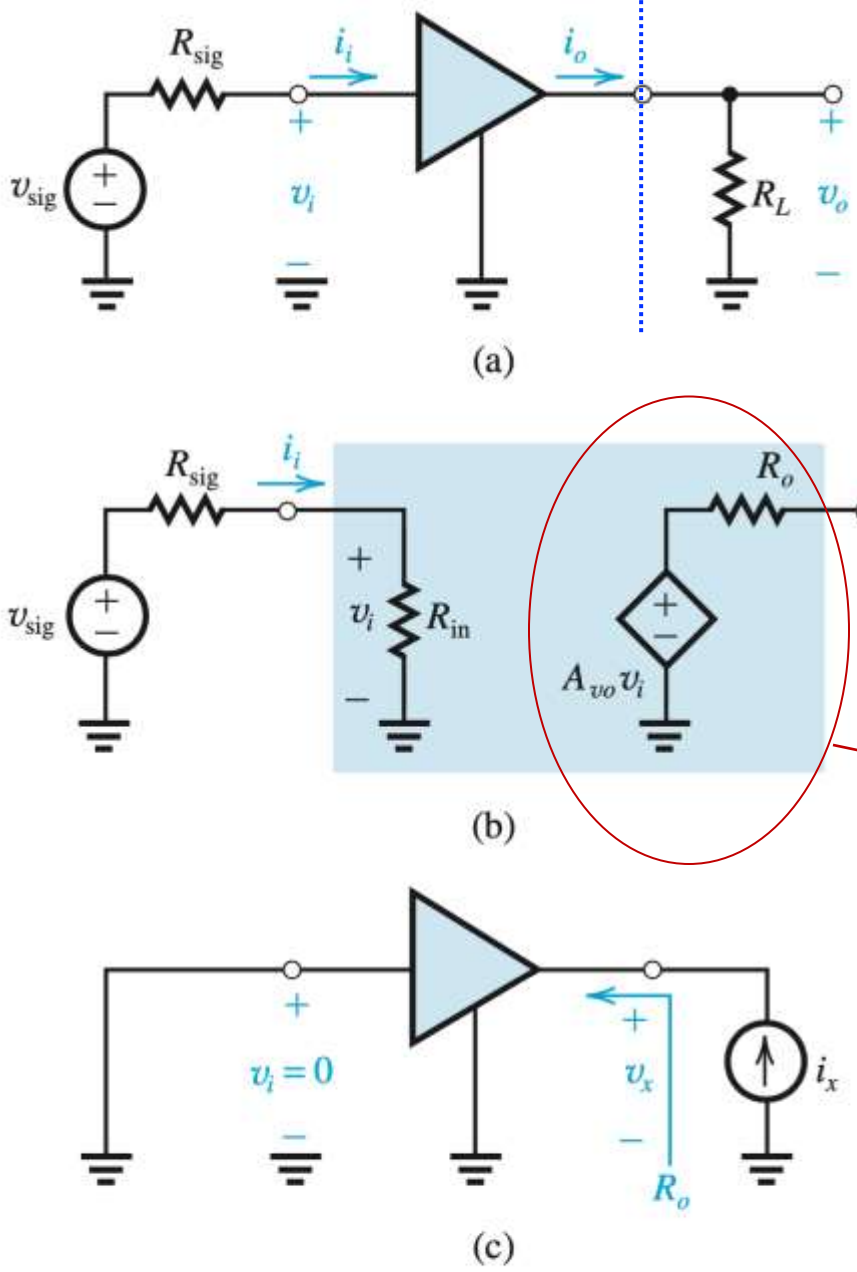


共集/
射级跟随

(f) Common-Collector (CC)
or Emitter Follower

Figure 7.33 The basic configurations of transistor amplifiers. (**a**)–(**c**) For the MOSFET; (**d**)–(**f**) for the BJT.

表征电压电压放大器特征的参数



最主要的三个

- 输入电阻 R_{in} 大比较好

$$R_{in} \equiv \frac{v_i}{i_i}$$

- 开路增益 A_{vo} 大比较好

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

$$v_i = \frac{R_{in}}{R_{in}+R_{sig}} v_{sig}$$

- 输出电阻 R_o 小比较好

$$R_o = \frac{v_x}{i_x}$$

v_i set to zero

放大器从输出（图a蓝色虚线处）往回看的戴维南等效

- 电压增益 A_v

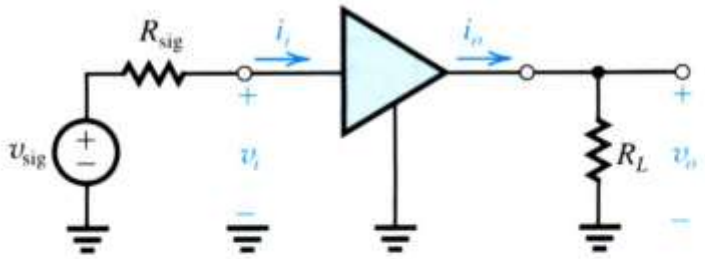
$$A_v \equiv \frac{v_o}{v_i} = A_{vo}\frac{R_L}{R_L+R_o}$$

- 总电压增益

$$G_v \equiv \frac{v_o}{v_{sig}}$$

$$G_v = \frac{R_{in}}{R_{in}+R_{sig}} A_{vo} \frac{R_L}{R_L+R_o}$$

Figure 7.34 Characterization of the amplifier as a functional block: **(a)** An amplifier fed with a voltage signal v_{sig} having a source resistance R_{sig}, and feeding a load resistance R_L; **(b)** equivalent-circuit representation of the circuit in **(a)**; **(c)** determining the amplifier output resistance R_o.



(a)

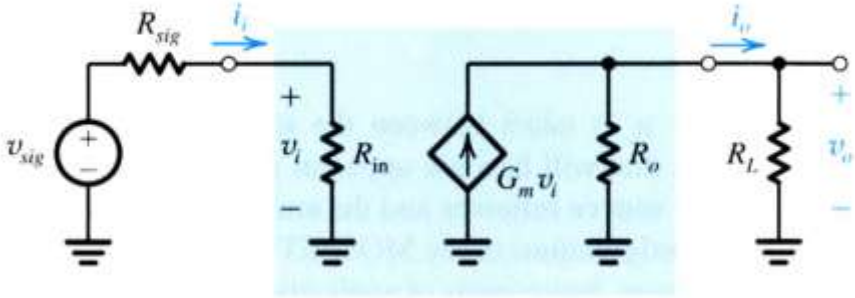
In some cases, we will find it more convenient to represent the amplifier output with the equivalent circuit shown in Fig. 7.35(d). Here, G_m is the **short-circuit transconductance** of the amplifier,

$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{v_o=0}$$

while R_o is the same as in the Thévenin representation. We can use the model in Fig. 7.35(d) to determine the open-circuit voltage gain of the amplifier proper as

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty} = G_m R_o$$

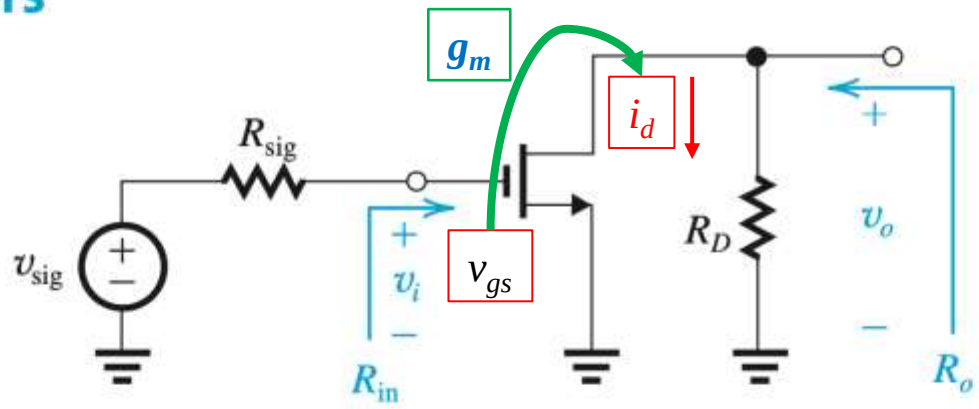
(c)



(d)

g_m 表示器件的跨导
G_m 表示电路的跨导

7.3.3 The Common-Source (CS) and Common-Emitter (CE) Amplifiers

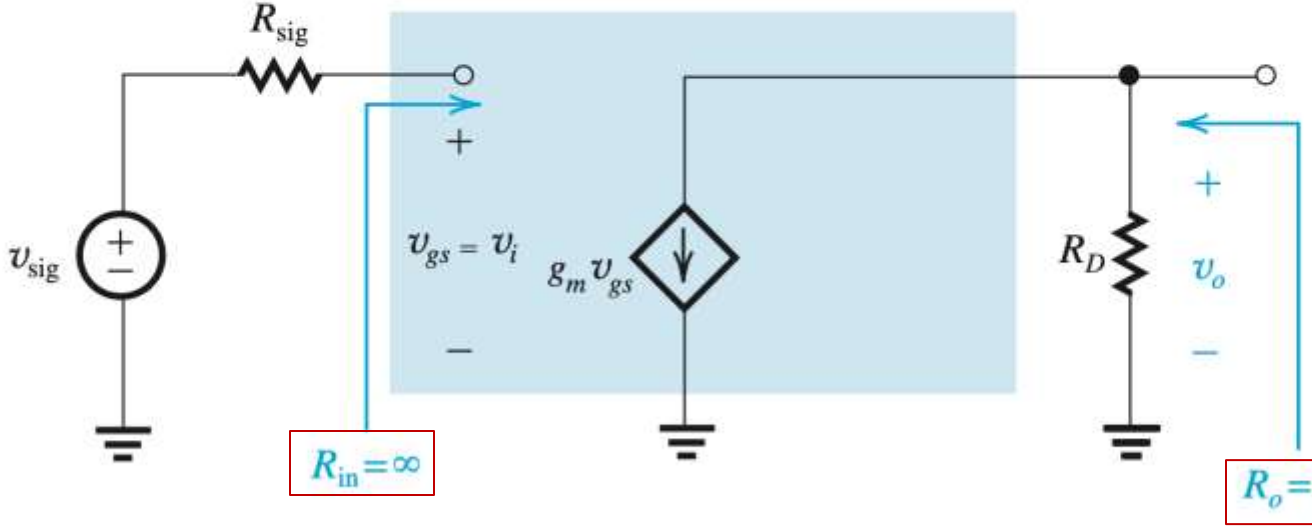


$$R_{in} = \infty$$
$$v_i = v_{sig}$$
$$v_{gs} = v_i$$
$$v_o = -g_m v_{gs} R_D$$
$$R_o = R_D$$

理解并记忆【核心是 v_{gs} 通过 g_m 转化为 i_d】

$A_v = -g_m$ ·(total resistor tied from "D" to ac ground)

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m R_D$$



(b)

如果接有负载 R_L

方法1：戴维南等效

$$A_v = A_{vo} \frac{R_L}{R_L + R_o}$$

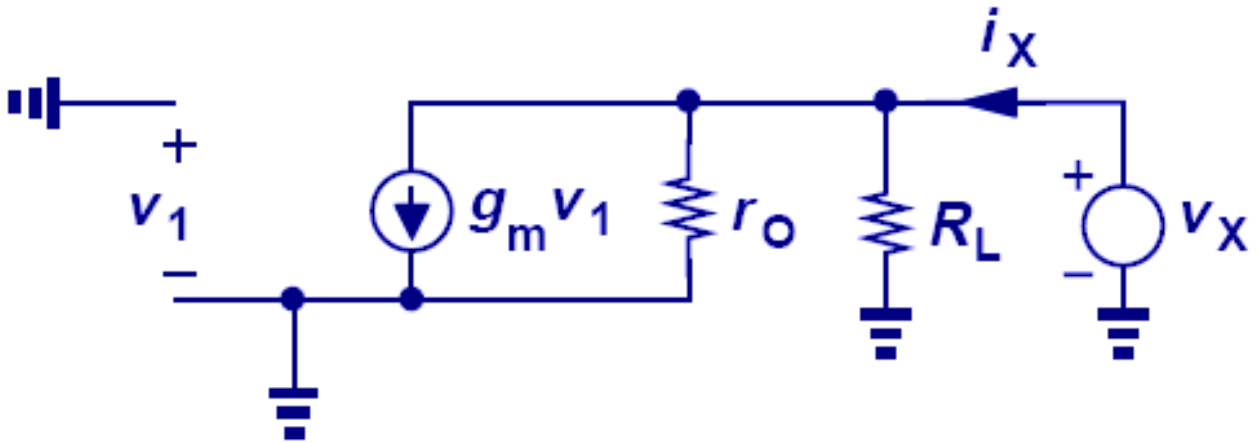
方法2：R_L看做与R_D并联

$$A_v = -g_m (R_D \| R_L)$$

$$G_v \equiv \frac{v_o}{v_{sig}} = -g_m (R_D \| R_L)$$

Figure 7.35 (a) Common-source amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig}. The bias circuit is omitted. (b) The common-source amplifier with the MOSFET replaced with its hybrid-π model.

CS Stage with λ ≠ 0



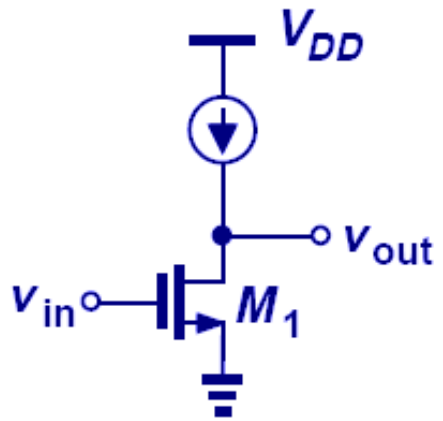
$$A_v = -g_m(R_L \| r_O)$$

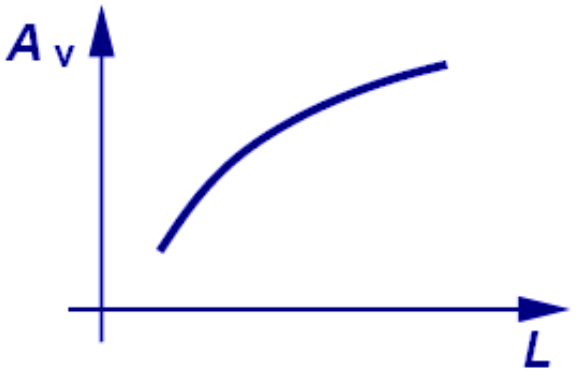
$$R_{in} = \infty$$

$$R_{out} = R_L \| r_O$$

D到地的总电阻

沟道长度对电压增益的变化





$$A_v = -g_m r_O. \tag{7.49}$$

This is the highest voltage gain that a single transistor can provide. Writing $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ and $r_O = (\lambda I_D)^{-1}$, we have

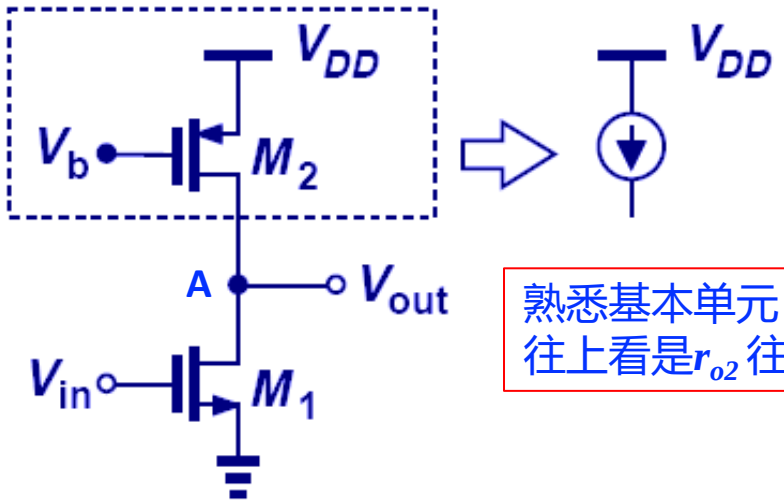
$$|A_v| = \frac{\sqrt{2\mu_n C_{ox}\dfrac{W}{L}}}{\lambda\sqrt{I_D}}. \tag{7.50}$$

This result may imply that $|A_v|$ falls as L increases, but recall from Chapter 6 that $\lambda \propto L^{-1}$:

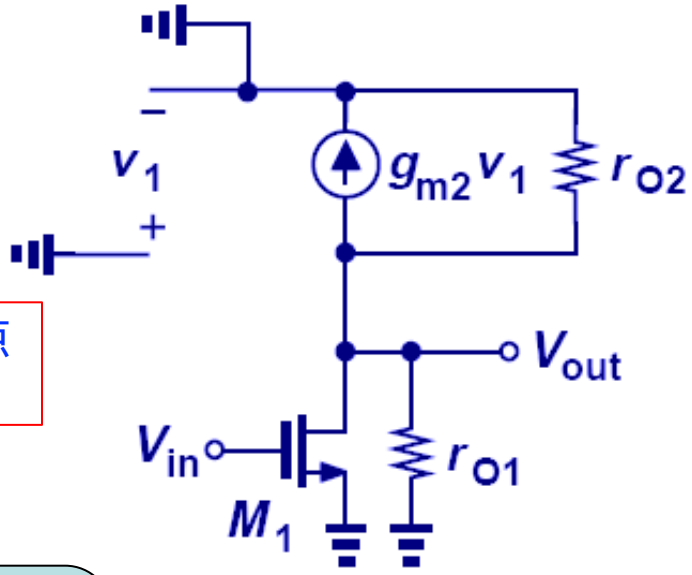
$$|A_v| \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}. \tag{7.51}$$

- 需注意： λ 与 L 成反比
- 现代半导体的趋势是L越来越小 → 单个放大器的 A_v 下降

电流源做负载



熟悉基本单元，然后从A点往上看是r_{o2}往下看是r_{o1}



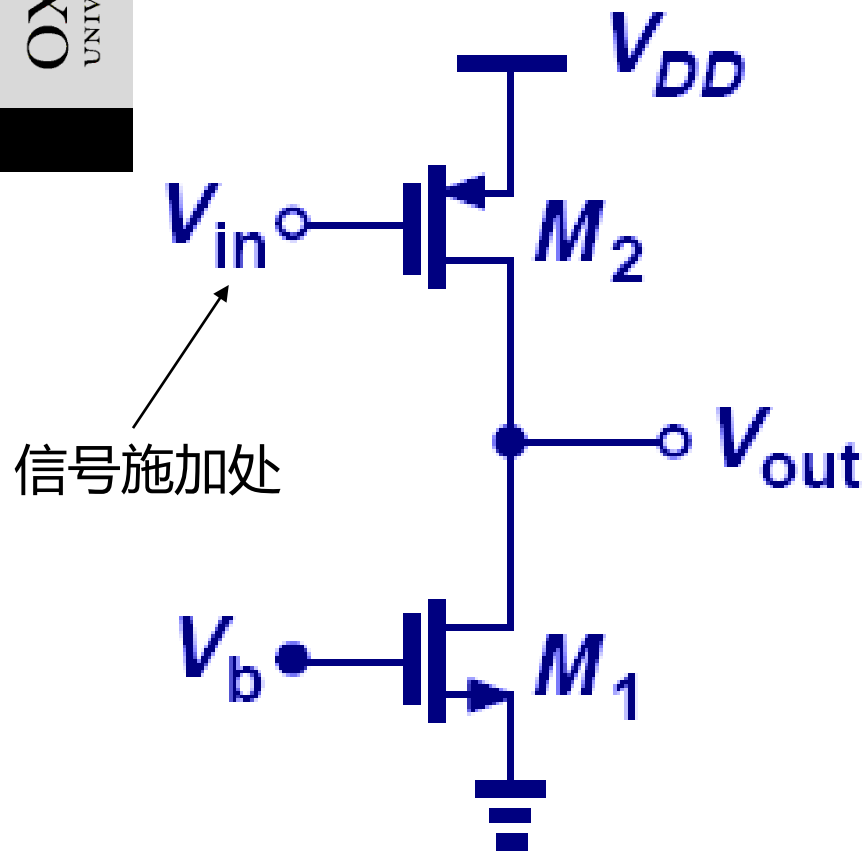
$$A_v = -g_{m1}(r_{O1} \| r_{O2})$$

$$R_{out} = r_{O1} \| r_{O2}$$

- 采用电流源做负载可以有效减轻 headroom 和电压增益的矛盾

在集成电路里，能用MOS替代电阻的地方就尽量不用电阻 → ①电流源提供了大电阻方案 r_o

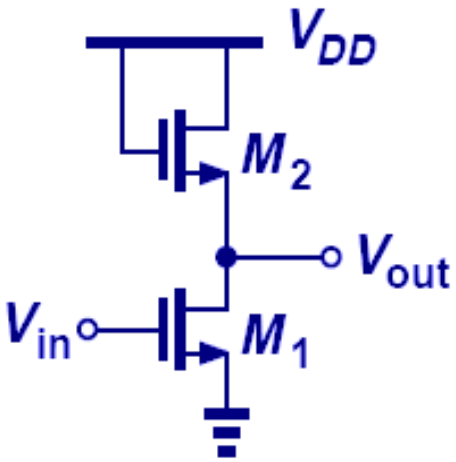
PMOS CS Stage with NMOS as Load

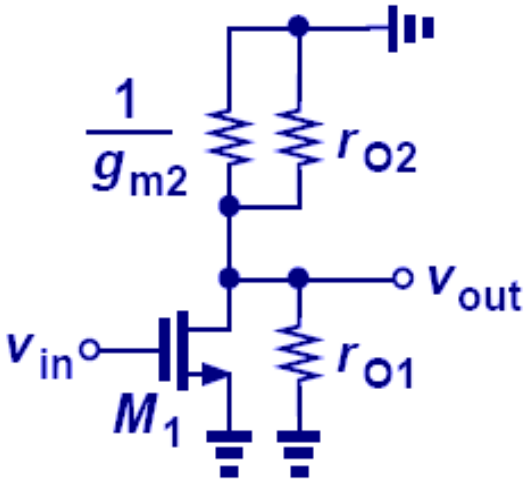


$$A_v = -g_{m2}(r_{O1} \| r_{O2})$$

- 同样, 也可以用 PMOS 作为放大器， NMOS 作为负载

Diode-Connected 作为负载





$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

$$A_v = -g_{m1}\cdot\frac{1}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

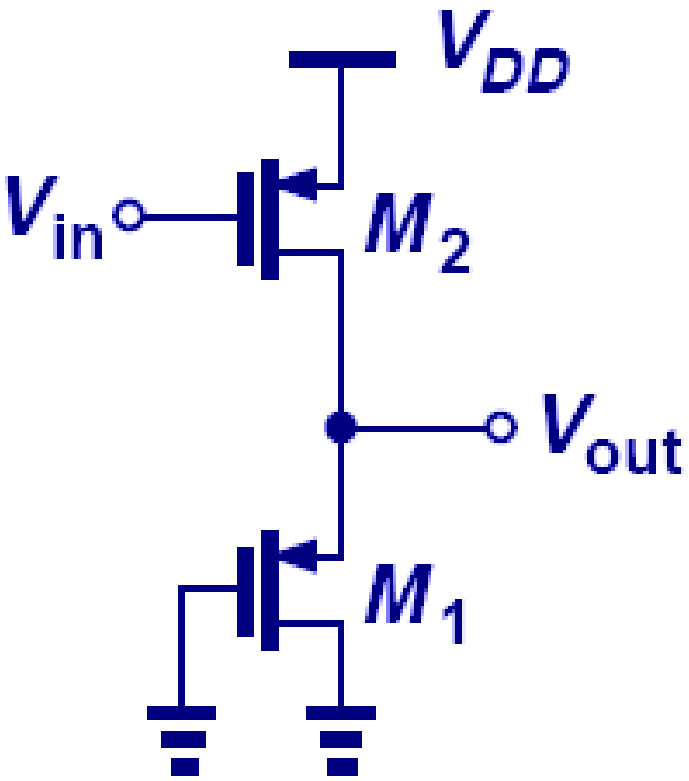
$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \| r_{O2} \| r_{O1}\right)$$

$$A_v = -g_{m1}\cdot\frac{1}{g_{m2}}$$

- 电压增益降低，但带来的好处是：**增益与工艺参数不相关**了！

在集成电路里，能用MOS替代电阻的地方就尽量不用电阻 ⟹ ②diode-connected 结构提供了小电阻方案 $1/g_m$

CS Stage with Diode-Connected PMOS



$$A_v = -g_{m2}\left(\frac{1}{g_{m1}} \| r_{o1} \| r_{o2}\right)$$

- 同样，也可用PMOS作为放大器，NMOS作为负载

$$R_{in} = r_\pi$$

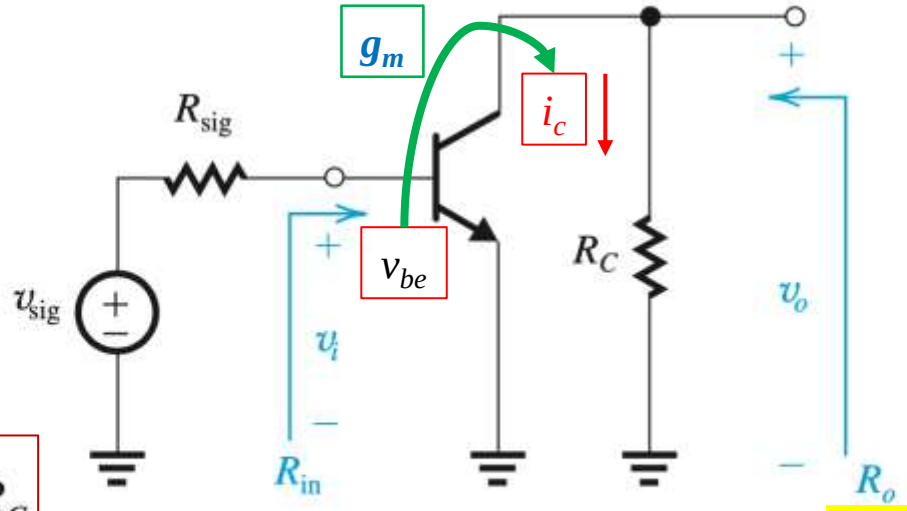
$$v_i = \frac{r_\pi}{r_\pi + R_{sig}} v_{sig}$$

$$v_\pi = v_i$$

$$v_o = -g_m v_\pi R_C$$

$$R_o = R_C$$

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m R_C$$



(a)

如果接有负载 R_L

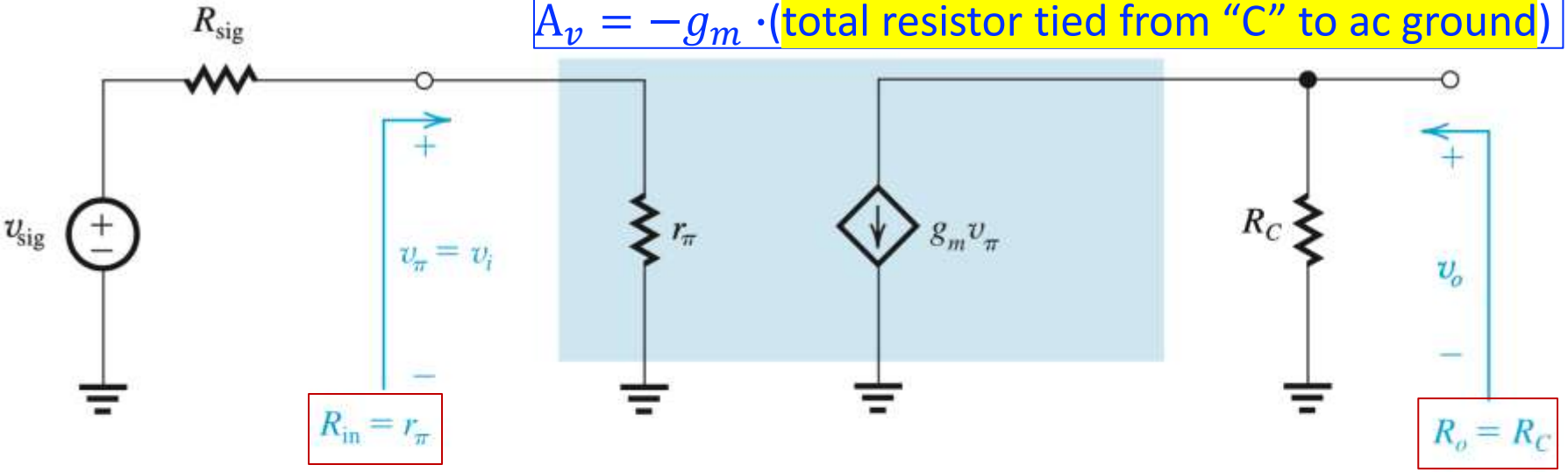
$$A_v = -g_m(R_C \| R_L)$$

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \frac{v_o}{v_i}$$

$$G_v = -\frac{r_\pi}{r_\pi + R_{sig}} g_m(R_C \| R_L)$$

理解并记忆【核心是 v_{be} 通过 g_m 转化为 i_c】

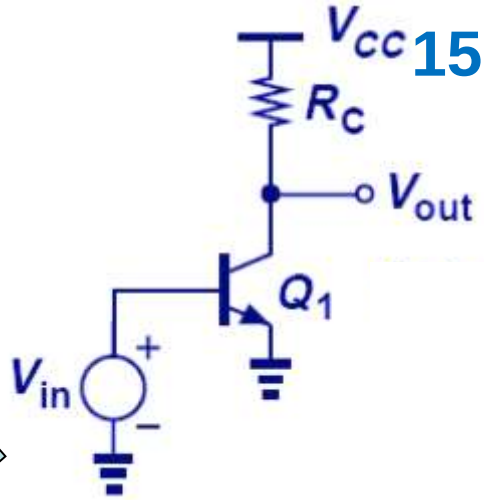
$A_v = -g_m \cdot$(total resistor tied from "C" to ac ground)

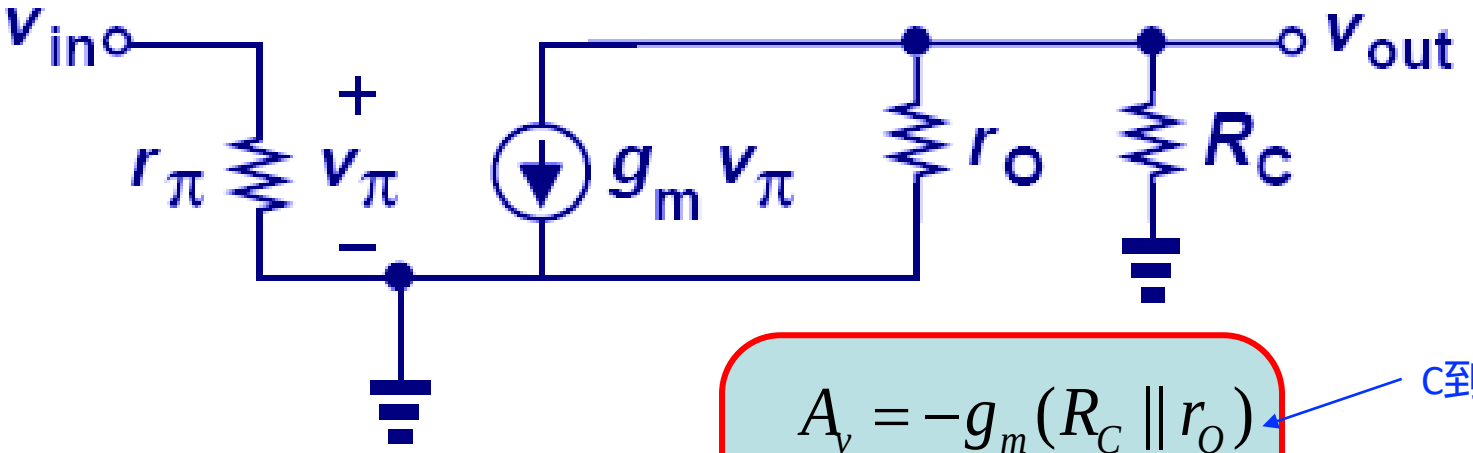


(b)

Figure 7.36 (**a**) Common-emitter amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig}. The bias circuit is omitted. (**b**) The common-emitter amplifier circuit with the BJT replaced by its hybrid-π model.

考虑厄雷效应之后





$$A_v = -g_m(R_C \| r_O)$$

$$R_{out} = R_C \| r_O$$

$$R_{in} = r_\pi$$

C到地的总电阻

- 厄雷效应会导致电压增益的降低；

Example 7.8

A CE amplifier utilizes a BJT with $\beta = 100$ is biased at $I_C = 1$ mA and has a collector resistance $R_C = 5\,\text{k}\Omega$. Find R_{in}, R_o, and A_{vo}. If the amplifier is fed with a signal source having a resistance of 5 kΩ, and a load resistance $R_L = 5\,\text{k}\Omega$ is connected to the output terminal, find the resulting A_v and G_v. If $\hat{v}_\pi$ is to be limited to 5 mV, what are the corresponding $\hat{v}_{sig}$ and $\hat{v}_o$ with the load connected?

①根据直流偏置计算小信号参数

$$g_m = \frac{I_C}{V_T} = \frac{1\,\text{mA}}{0.025\,\text{V}} = 40\,\text{mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40\,\text{mA/V}} = 2.5\,\text{k}\Omega$$

②计算放大器特征参数

$$R_{in} = r_\pi = 2.5\,\text{k}\Omega$$

$$A_{vo} = -g_m R_C = -40\,\text{mA/V} \times 5\,\text{k}\Omega = -200\,\text{V/V}$$

$$R_o = R_C = 5\,\text{k}\Omega$$

③计算其他参数

$$A_v = A_{vo}\frac{R_L}{R_L + R_o} = -200 \times \frac{5}{5+5} = -100\,\text{V/V}$$

或

$$A_v = -g_m(R_C \| R_L) = -40(5 \| 5) = -100\,\text{V/V}$$

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v = \frac{2.5}{2.5+5} \times -100 = -33.3\,\text{V/V}$$

④v_π（v_{be}）需满足小信号近似的前提 $v_\pi << V_T$

$$\hat{v}_{sig} = \left(\frac{R_{in} + R_{sig}}{R_{in}}\right)\hat{v}_\pi = \frac{2.5+5}{2.5} \times 5 = 15\,\text{mV}$$

$$\hat{v}_o = G_v \hat{v}_{sig} = 33.3 \times 0.015 = 0.5\,\text{V}$$

内在增益

$$A_v = -g_m r_O$$

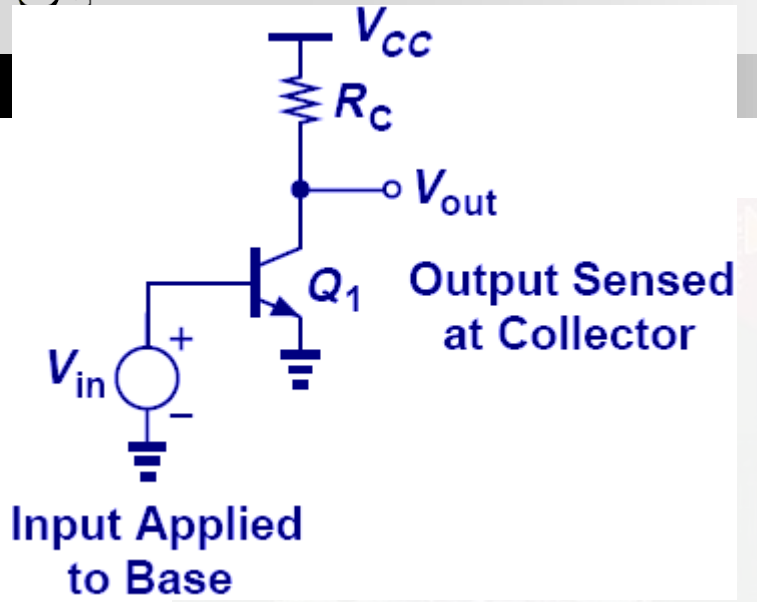
$$|A_v| = \frac{V_A}{V_T}$$

$$g_m = I_C / V_T$$

$$r_O = V_A / I_C$$

- 当 R_C 趋于∞时, 电压增益达到最大值（ $-g_m r_O$ ），此最大值即放大器的内在增益
- 内在增益与偏置电流的大小无关.

Limitation on CE Voltage Gain

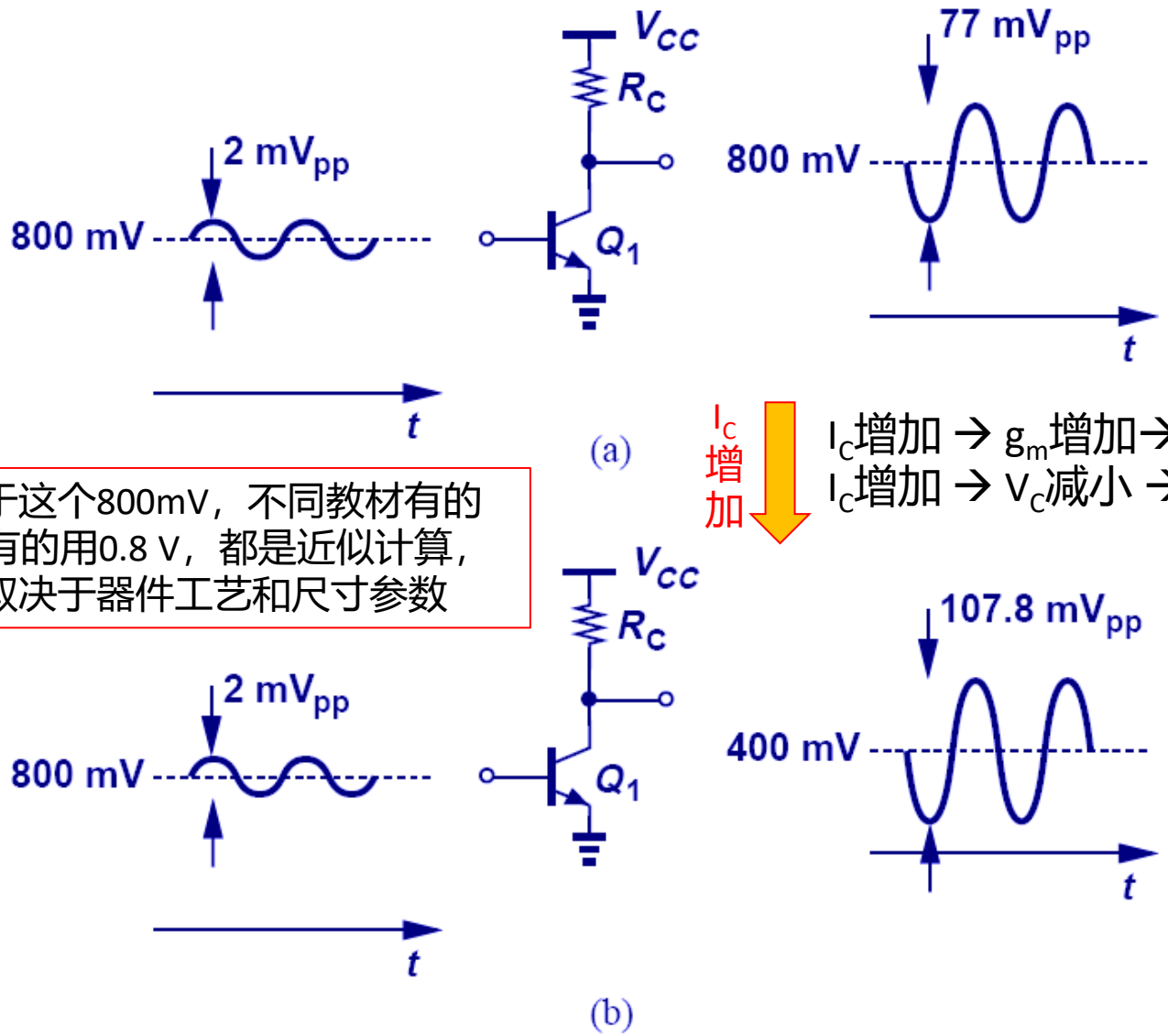


$$A_v = -g_m R_C$$

$$|A_v| = \frac{I_C R_C}{V_T} = \frac{V_{RC}}{V_T} < \frac{V_{CC}}{V_T}$$

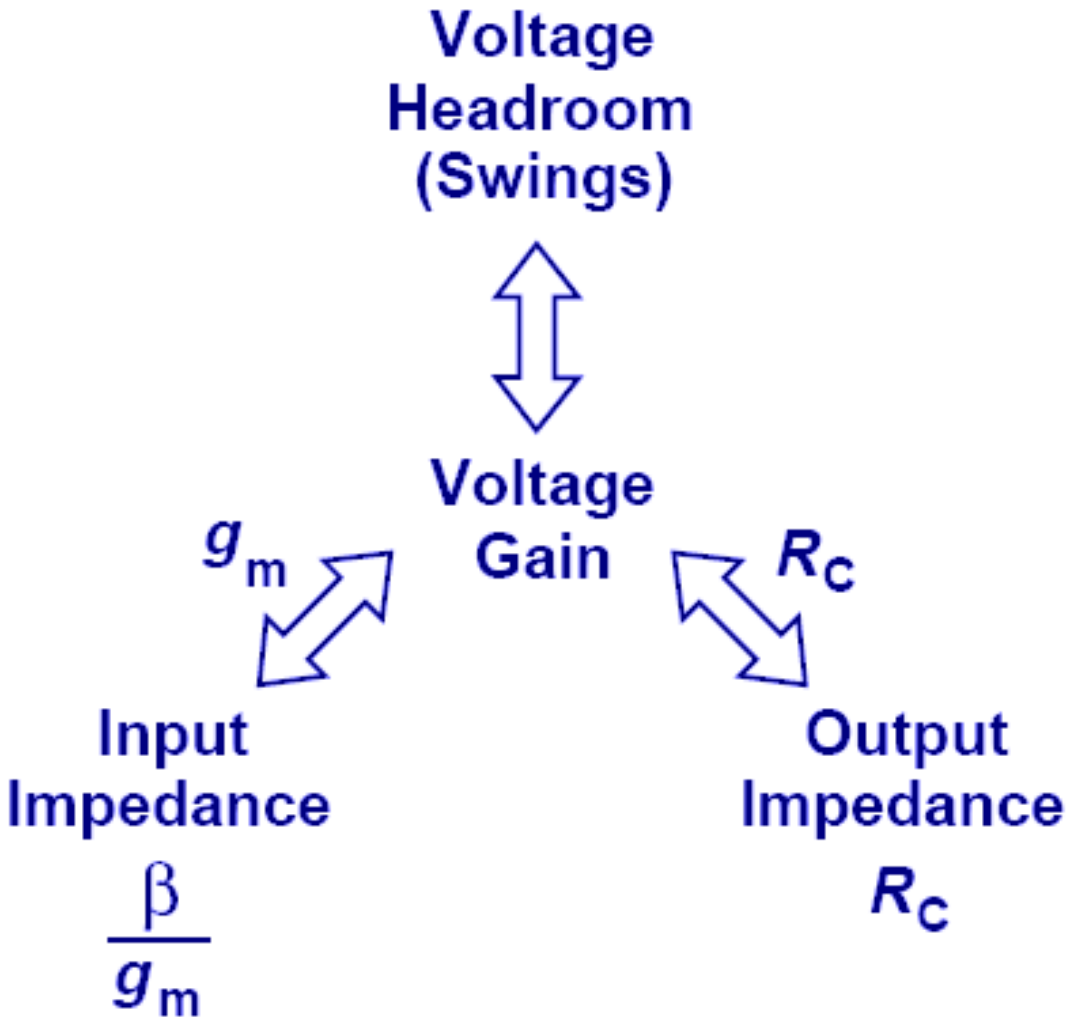
- 因为 $g_m = I_C/V_T$，CE 组态的电压增益可以表达成 V_{RC} / V_T.
- V_{RC} 是V_{CC} 和 V_{CE}之间的电压差， 为了保证三极管工作于放大区， **V_C最低不得低于 V_B-0.4V**

电压增益和 headroom 的 trade-off



不用纠结于这个800mV，不同教材有的用0.7 V，有的用0.8 V，都是近似计算，实际数值取决于器件工艺和尺寸参数

CE组态设计指标的折衷（trade-off）



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CS/CE小结

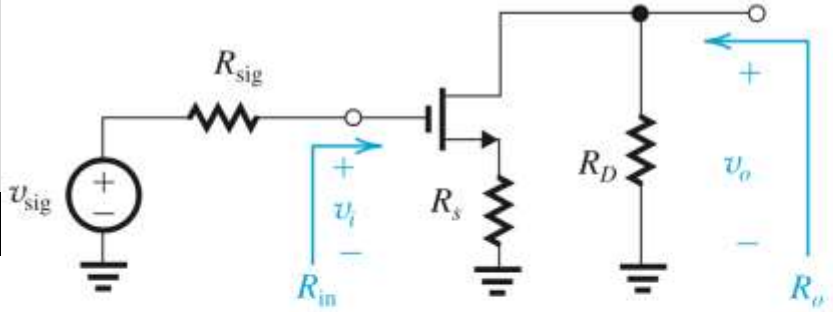
- 具有较高的输入电阻（CS为∞）、较高的输出电阻、高的增益（一般作为多级放大器中的主要增益级）

- 减小R_C或R_D可以降低输出电阻，但增益也会降低，一般CS和CE不会提供较小的输出电阻，我们会在CS和CE之后加一级CD或CC来提供小输出电阻，以有效驱动负载

- 高频响应不佳，往往与CG和CB相组合，来获得较好的高频频率特性

7.3.4 The Common-Source (Common-Emitter) Amplifier with a Source (Emitter) Resistance

源极退化/发射极退化结构



(a)

- S（或 E）通过一个电阻接地
- 因 S 或 E 不直接接地，因此用 T 模型比较方便

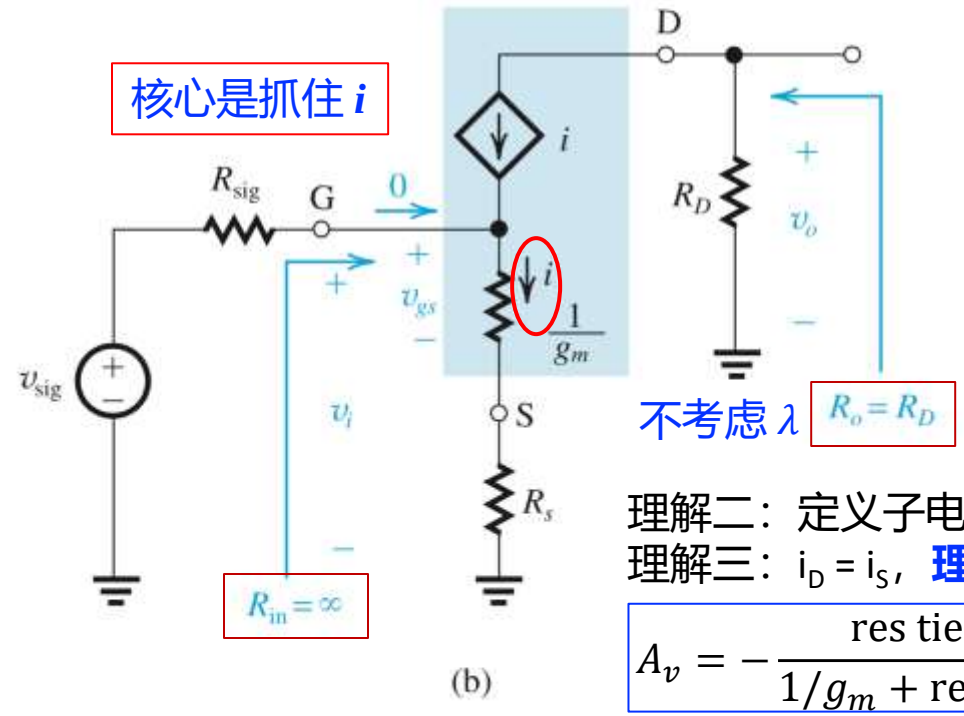
输入分压，R_S可以控制实际到达 gs 的电压

$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_s} = \frac{v_i}{1 + g_m R_s}$$

反馈因子

Rs 本质上是一个负反馈（假设G点电压因某种原因突然有一向上的波动，则 i 增加，S 点电压增加，从而导致 v_{gs} 减小，i 减小 → 对波动有抑制作用）

核心是抓住 *i*



(b)

$$i = \frac{v_i}{1/g_m + R_s} = \left(\frac{g_m}{1 + g_m R_s}\right) v_i$$

$$v_o = -iR_D$$

$$A_{vo} \equiv \frac{v_o}{v_i} = -\frac{g_m R_D}{1 + g_m R_s}$$

不考虑 λ $R_o = R_D$

理解一：增益按反馈因子缩放

理解二：定义子电路（R_s和NMOS）**跨导G_m**

理解三：$i_D = i_S$，**理解并记忆【$v_o v_i$用 i 表示】**

$$A_{vo} = -G_m R_D$$

$$G_m = \frac{g_m}{1 + g_m R_s}$$

$$A_v = -\frac{\text{res tied from "D" to ac GND}}{1/g_m + \text{res tied from "S" to ac GND}}$$

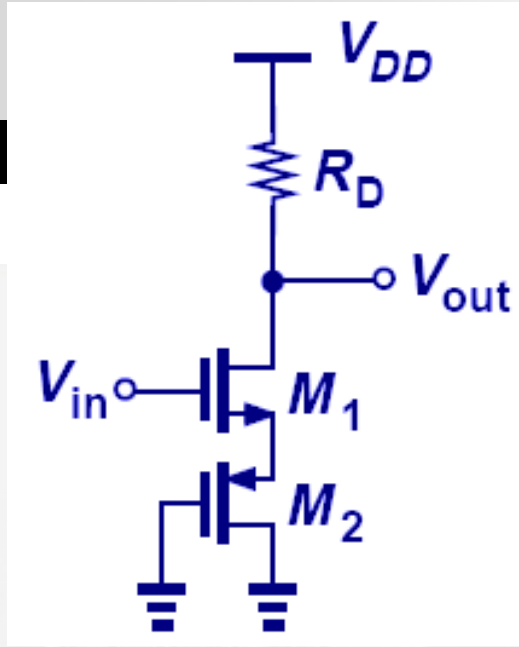
考虑R_L

$$A_v = -\frac{g_m (R_D \| R_L)}{1 + g_m R_s}$$

$$A_v = -\frac{R_D \| R_L}{1/g_m + R_s}$$

Figure 7.37 The CS amplifier with a source resistance R_s: **(a)** circuit without bias details; **(b)** equivalent circuit with the MOSFET represented by its T model.

Example of CS Stage with Degeneration

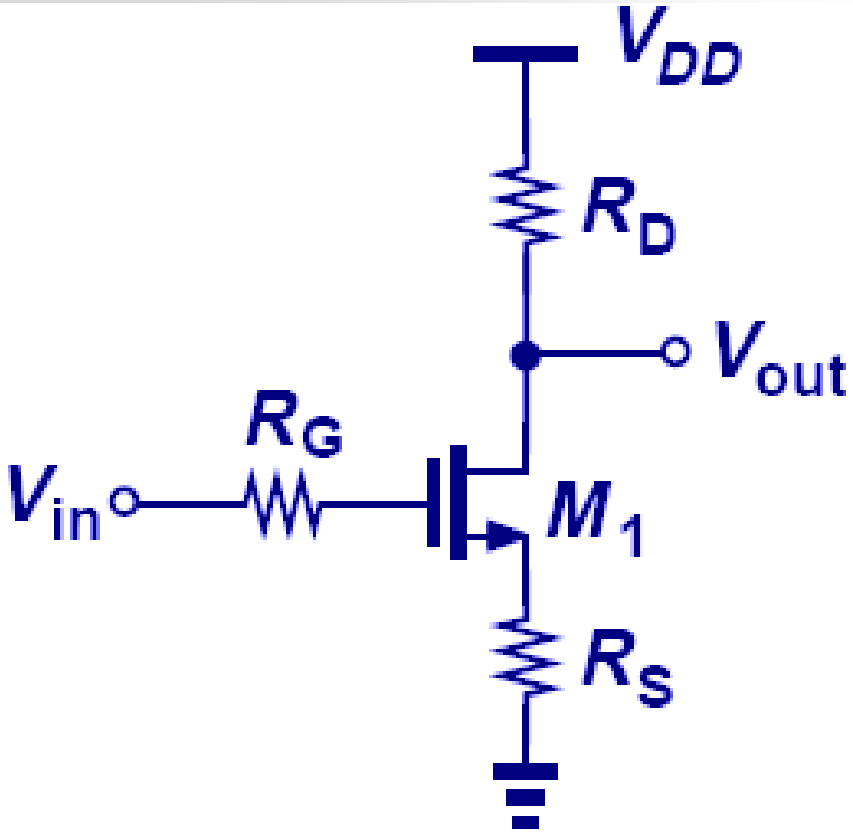


求电压增益

$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- 也可用 diode-connected MOS管替代退化电阻.

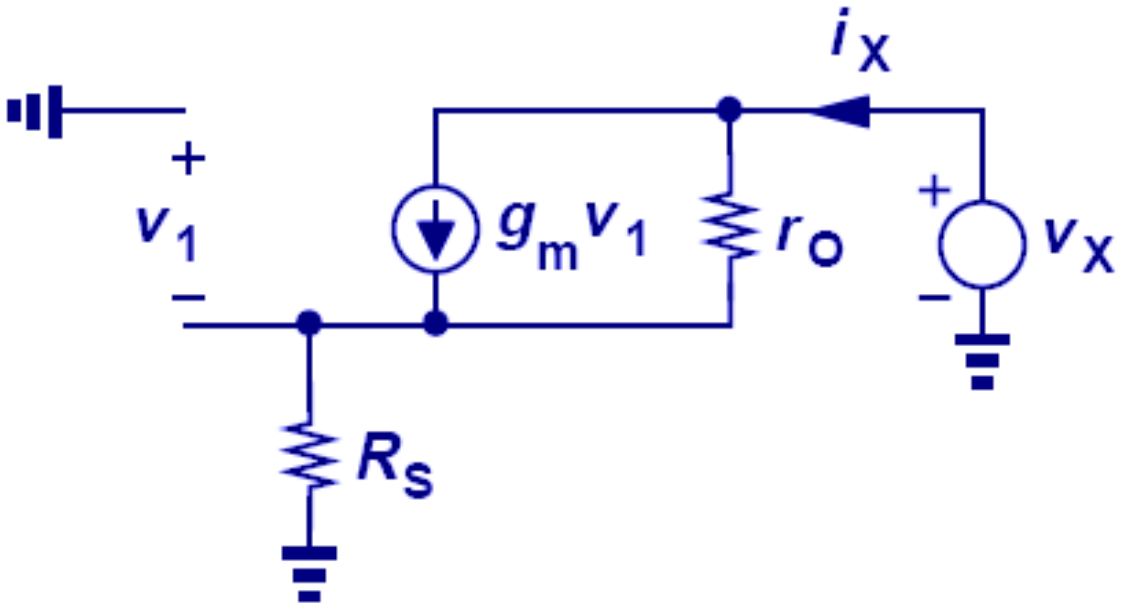
栅极电阻的影响



$$V_{R_G} = 0$$

- 因为栅极没有电流，所以不对电压增益、输入输出阻抗有影响

退化电阻对输出阻抗的影响



$$\frac{v_X}{i_X} = r_O(1 + g_m R_S) + R_S$$

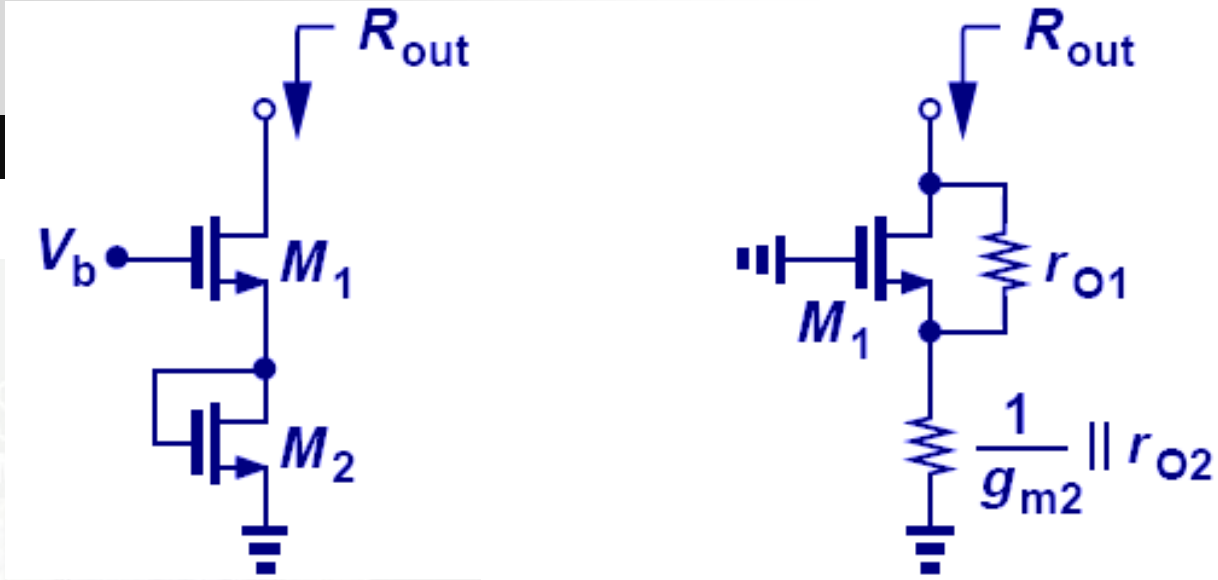
$$= (1 + g_m r_O)R_S + r_O$$

$$= R_S + r_O + g_m R_S r_O$$

可以看成对r_o的放大，也可以看成对R_S的放大，总体来说，阻抗大幅增加 → 是个更好的恒流源

- 在分析源极退化结构电路时，仅当我们计算输出电阻时才考虑沟道长度调制效应；

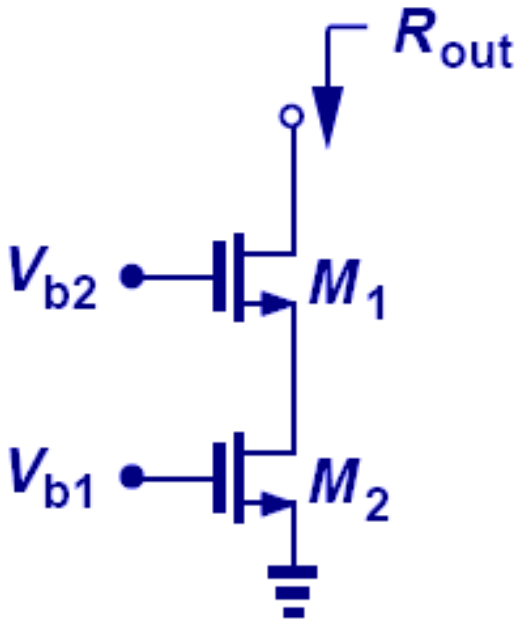
输出阻抗Example (I)

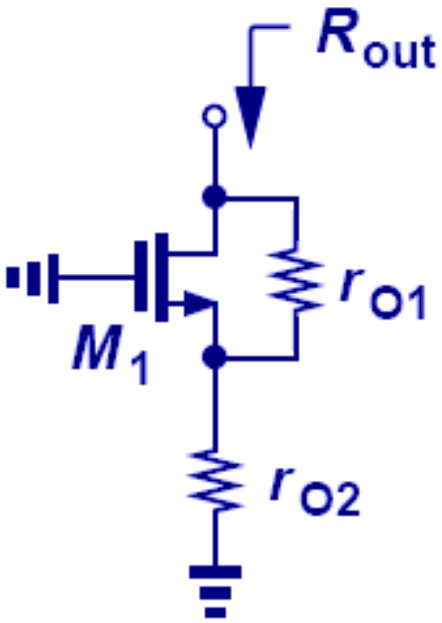


$$R_{out} = r_{O1} + (1 + g_{m1} r_{O1}) \left(\frac{1}{g_{m2}} \| r_{O2} \right)$$

- 当 $1/g_m$ 与 r_{O2} 并联时，一般我们仅需考虑 $1/g_m$ 就可以了。【因为一般情况下$1/g_m$ 比较小】

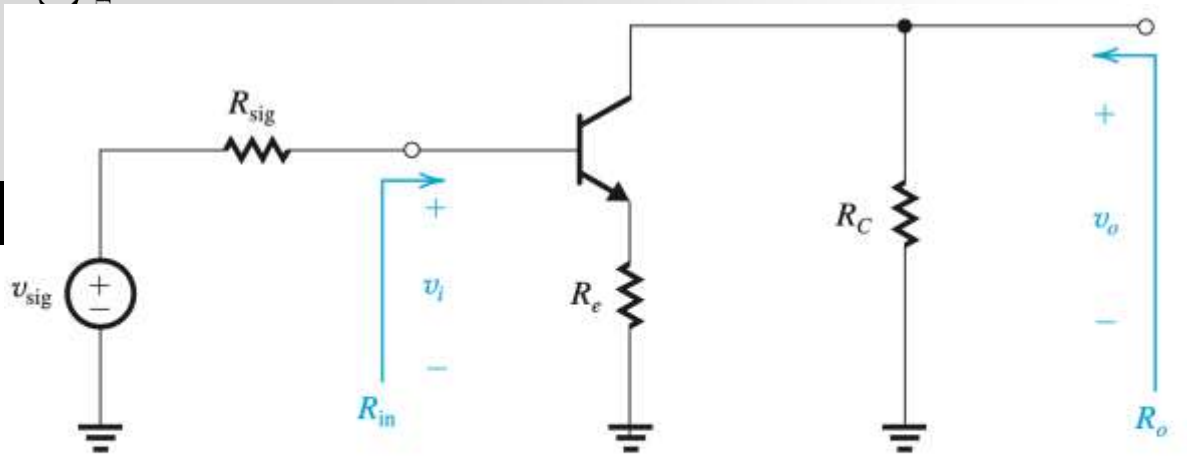
输出阻抗 Example (II)





$$R_{out} \approx (1 + g_{m1} r_{O1}) r_{O2} + r_{O1}$$

This is a very important result. It states that *the input resistance looking into the base is* $(\beta+1)$ *times the total resistance in the emitter*, and is known as the **resistance-reflection rule**. The



$$R_{in} \equiv \frac{v_i}{i_b}$$

$$i_b = \frac{i_e}{\beta+1}$$

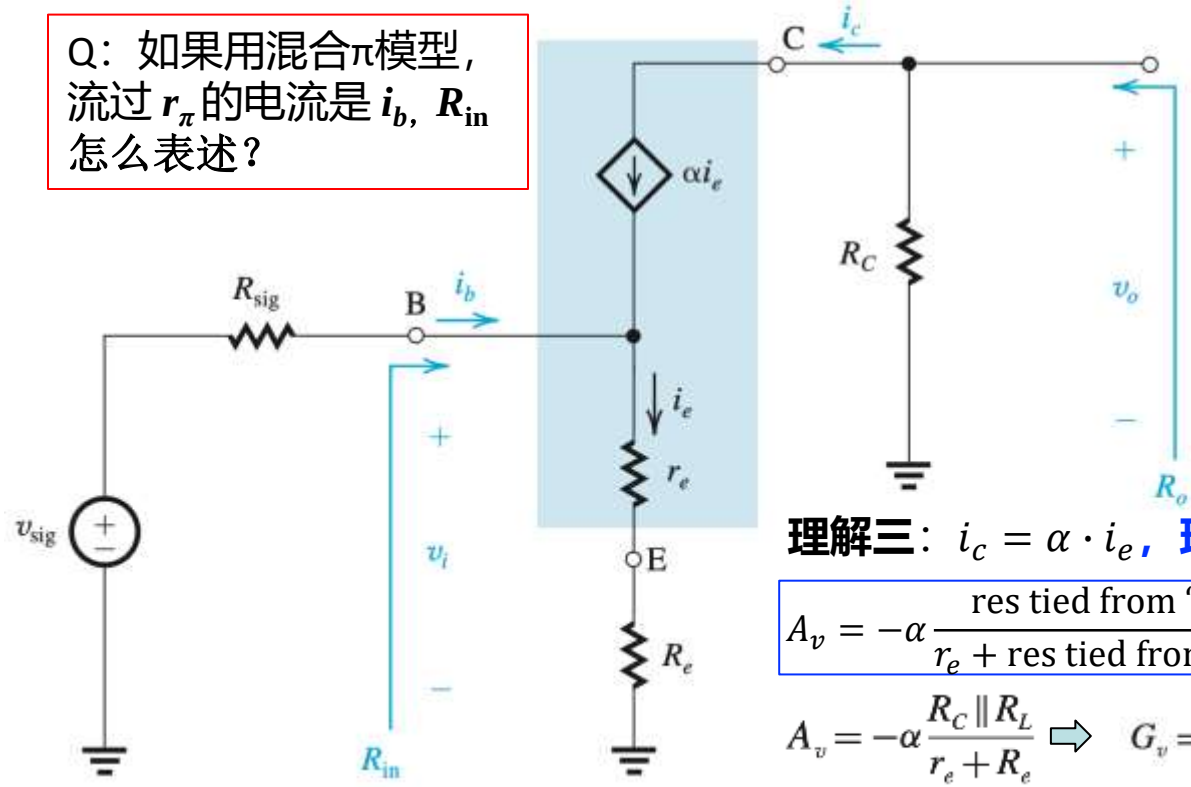
$$i_e = \frac{v_i}{r_e + R_e}$$

$$R_{in} = (\beta+1)(r_e + R_e)$$

输入阻抗大幅提升
CE是 β/g_m

理解：B点到地的电压为$i_e(r_e + R_e)$
从B点看进去，除以 i_b，为输入电阻

Q：如果用混合π模型，流过 r_π 的电流是 i_b，R_{in} 怎么表述？



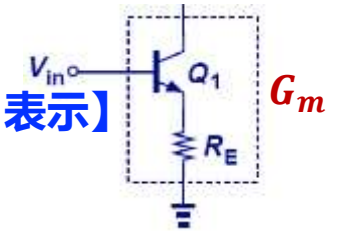
$$A_{vo} = -\frac{\alpha}{r_e}\frac{R_C}{1+R_e/r_e} \Leftarrow \frac{\text{输出到地的电压}}{\text{输入到地的电压}}$$

$$A_{vo} = -\frac{g_m R_C}{1+R_e/r_e} \simeq -\frac{g_m R_C}{1+g_m R_e}$$

理解一 反馈因子

理解二：子电路（R_e和npn）**跨导 G_m**

$$G_m = \frac{g_m}{1+g_m R_e}$$

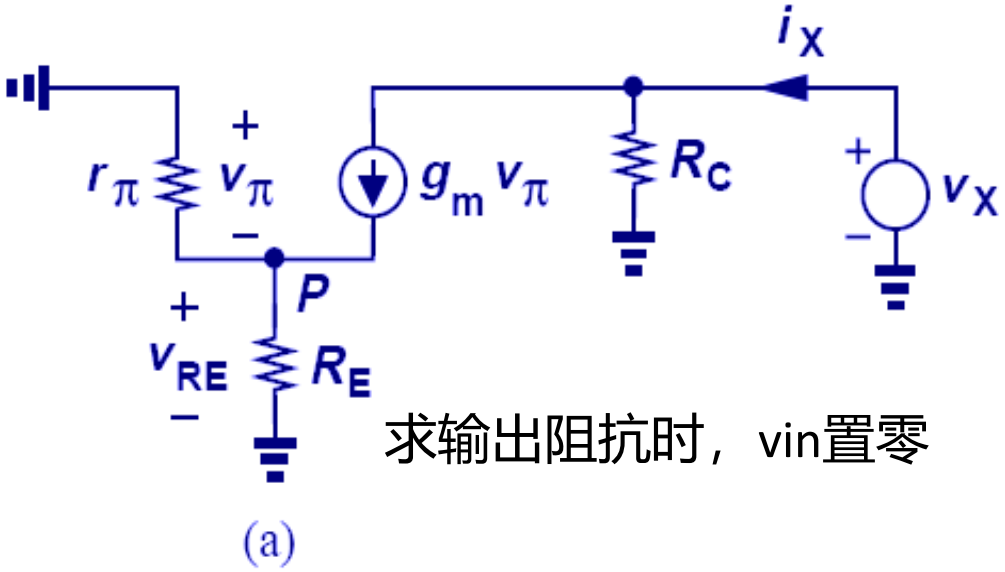


理解三：$i_c = \alpha \cdot i_e$，**理解并记忆【$v_o v_i$ 用 i 表示】**

$$A_v = -\alpha \frac{\text{res tied from "C" to ac GND}}{r_e + \text{res tied from "E" to ac GND}}$$

$$A_v = -\alpha \frac{R_C \parallel R_L}{r_e + R_e} \Rightarrow G_v = \frac{R_{in}}{R_{in}+R_{sig}} \times -\alpha \frac{R_C \parallel R_L}{r_e + R_e}$$

发射极退化结构的输出阻抗



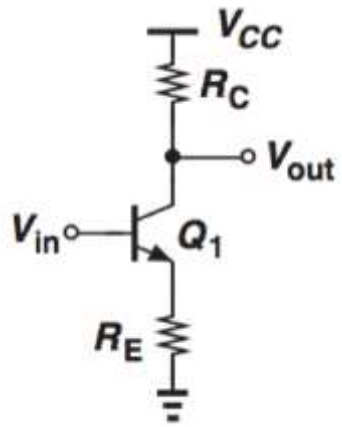
求输出阻抗时，vin置零

(a)

$$V_A = \infty$$

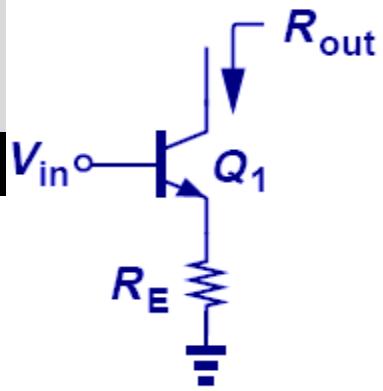
$$v_{in} = 0 = v_\pi + \left(\frac{v_\pi}{r_\pi} + g_m v_\pi \right) R_E \Rightarrow v_\pi = 0$$

$$R_{out} = \frac{v_X}{i_X} = R_C$$

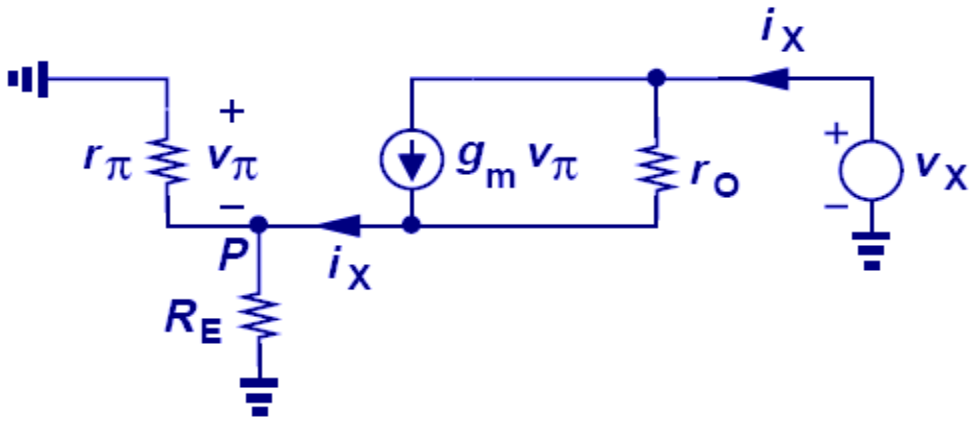


思考：若考虑厄雷效应呢?

厄雷效应对输出阻抗的影响

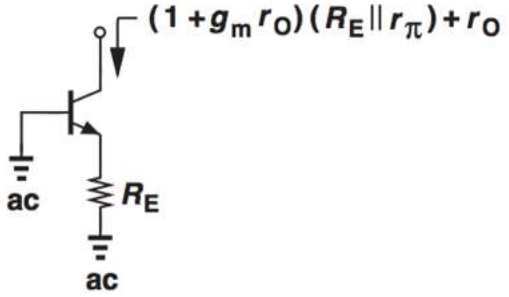


(a)

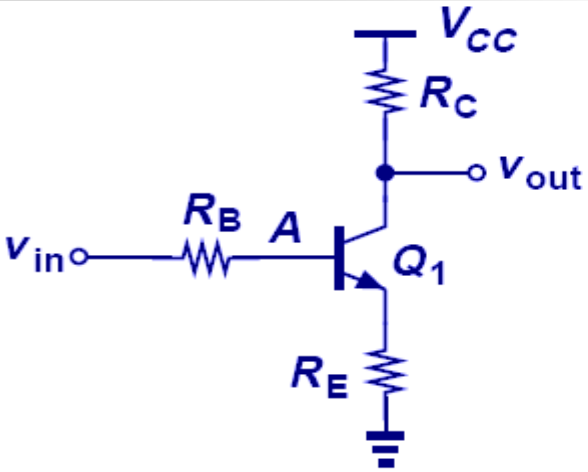


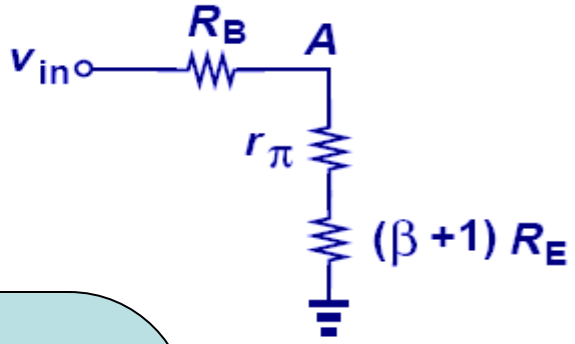
(b)

- 输出阻抗显著增加；
- 更适合用作恒流源；



基极电阻的影响





$$V_A = \infty$$

方法1：找信号通路上的中间点A进行分拆，级联计算

$$\frac{v_{out}}{v_{in}} = \frac{v_A}{v_{in}} \cdot \frac{v_{out}}{v_A} = \frac{r_\pi + (\beta+1)R_E}{R_B + r_\pi + (\beta+1)R_E} \cdot \frac{-R_C}{\alpha/g_m + R_E}$$

方法2：直接写出v_{out}、v_{in}的表达式【抓住$i_B i_C$】

$$\frac{v_{out}}{v_{in}} = \frac{-\beta R_C}{r_\pi + (\beta+1)R_E + R_B} = \frac{-\beta i_B \cdot R_C}{i_B \cdot (R_B + r_\pi) + (\beta+1) i_B \cdot R_E}$$

$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1}}$$

（R_B折算到E端时需缩小**β+1**倍）

Example 7.9

a signal source having a resistance of 5 kΩ, $g_m = \frac{I_C}{V_T} = \frac{1\text{ mA}}{0.025\text{ V}} = 40\text{ mA/V}$

For the CE amplifier specified in Example 7.8, what value of R_e is needed to raise R_{in} to a value four times that of R_{sig}? With R_e included, find A_{vo}, R_o, A_v, and G_v. Also, if $\hat{v}_\pi$ is limited to 5 mV, what are the corresponding values of $\hat{v}_{sig}$ and $\hat{v}_o$?

① $20 = (\beta+1)(r_e + R_e) \Rightarrow r_e + R_e \simeq 200\ \Omega \Rightarrow R_e = 200 - 25 = 175\ \Omega$

②

$$A_{vo} = -\alpha \frac{R_C}{r_e + R_e}$$

$$\simeq -\frac{5000}{25+175} = -25\text{ V/V}$$

$$R_o = R_C = 5\text{ k}\Omega\text{ (unchanged)}$$

$$A_v = A_{vo}\frac{R_L}{R_L + R_o} = -25 \times \frac{5}{5+5} = -12.5\text{ V/V}$$

$$G_v = \frac{R_{in}}{R_{in}+R_{sig}} A_v = -\frac{20}{20+5} \times 12.5 = -10\text{ V/V}$$

③

$$\hat{v}_i = \hat{v}_\pi \left(\frac{r_e + R_e}{r_e}\right)$$

$$= 5\left(1 + \frac{175}{25}\right) = 40\text{ mV}$$

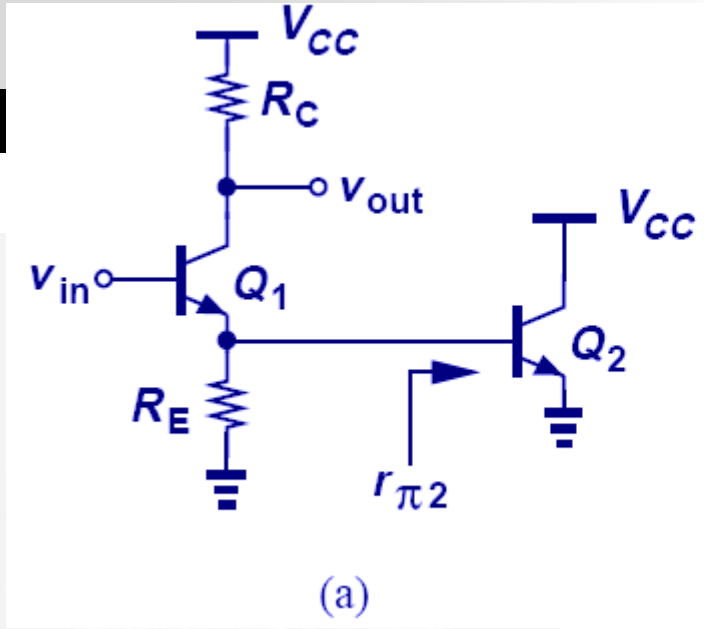
$$\hat{v}_{sig} = \hat{v}_i \frac{R_{in} + R_{sig}}{R_{in}}$$

$$= 40\left(1 + \frac{5}{20}\right) = 50\text{ mV}$$

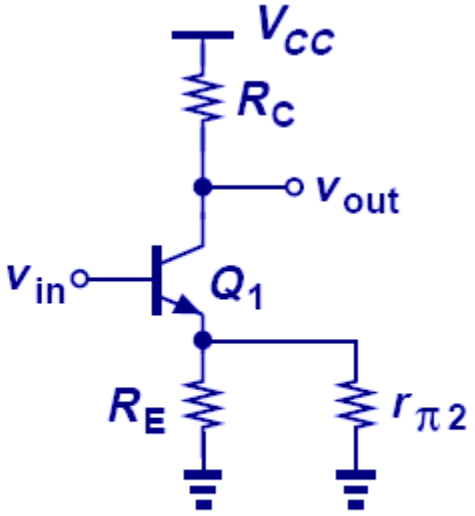
$$\hat{v}_o = \hat{v}_{sig} \times |G_v|$$

$$= 50 \times 10 = 500\text{ mV} = 0.5\text{ V}$$

发射极退化 Example I



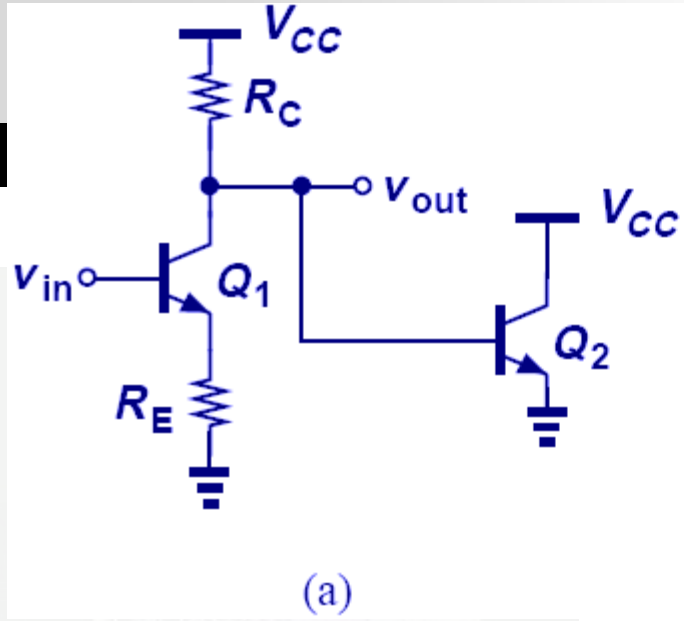
(a)



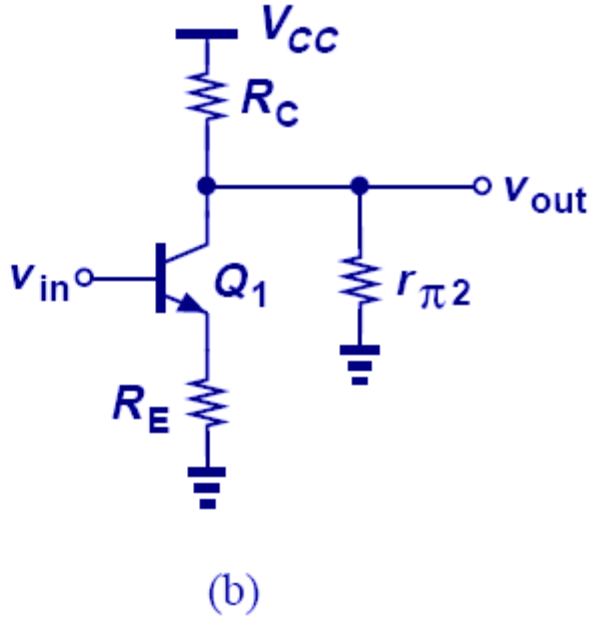
(b)

$$A_v = -\frac{R_C}{\frac{1}{g_{m1}} + R_E \parallel r_{\pi 2}}$$

发射极退化 Example II



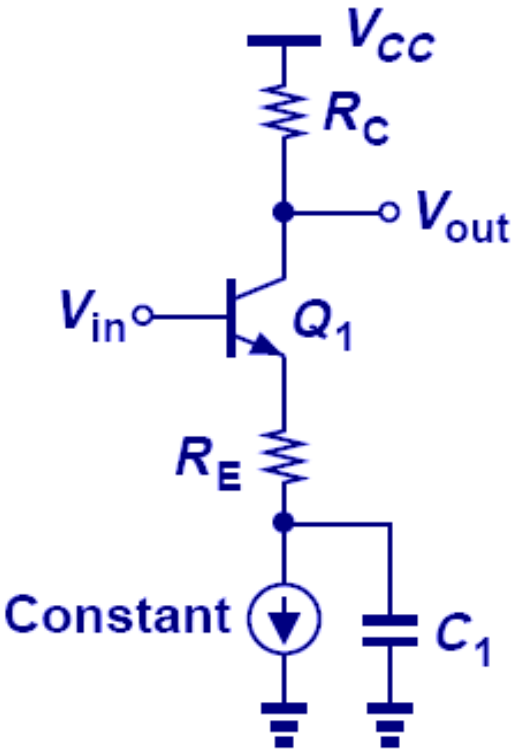
(a)



(b)

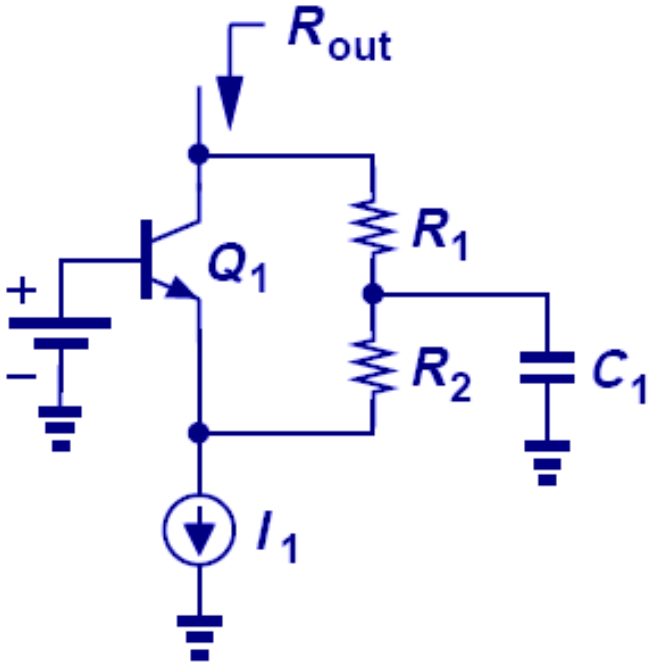
$$A_v = -\frac{R_C \parallel r_{\pi 2}}{\frac{1}{g_{m1}} + R_E}$$

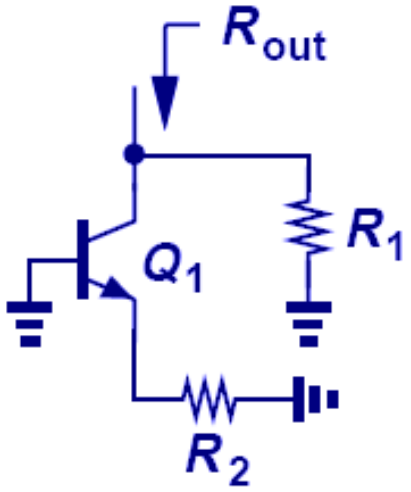
发射极电容

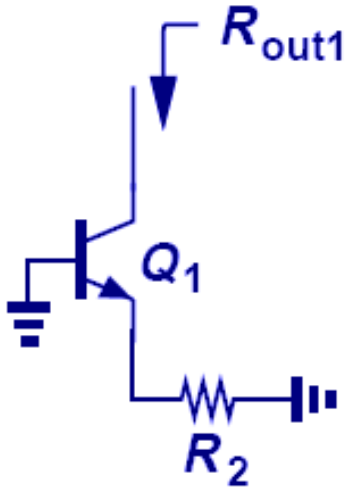


- 直流时：电容开路，不影响直流偏置；
- 交流小信号时：电容短路，提供R_E到GND的通路（电流源开路）

本课程的核心：培养对电路的洞察力



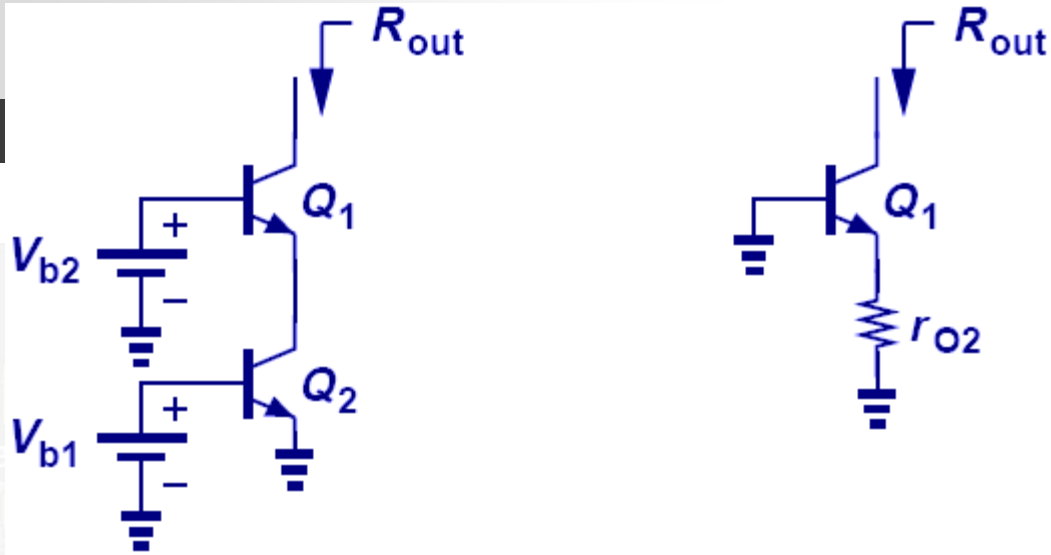




$$R_{out} = R_1 \| R_{out1} \Longrightarrow R_{out1} = r_O + (g_m r_O + 1)(R_2 \| r_\pi) \Longrightarrow R_{out} = [r_O + (g_m r_O + 1)(R_2 \| r_\pi)] \| R_1$$

- 基于对基本电路特性的熟悉和积累，遇到复杂问题时，无需画出小信号等效电路，可直接写出电路特性；
- 这一洞察力的培养，对模拟电路的分析至关重要！

举例2



$$R_{out} = r_{O1} + (g_{m1} r_{O1} + 1)(R_{O2} \| r_{\pi 1})$$

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源极退化/射极退化小结

- 源极射极电阻的存在，使得增益降低，但输入阻抗增加，牺牲增益获得了更好的输入阻抗
- 源极射极电阻的存在，大幅增加了输出阻抗，更加接近理想电流源了
- 当有基极电阻存在时，可除以（β+1）折算到射极，再计算增益

7.3.5 The Common-Gate (CG) and the Common-Base (CB) Amplifiers

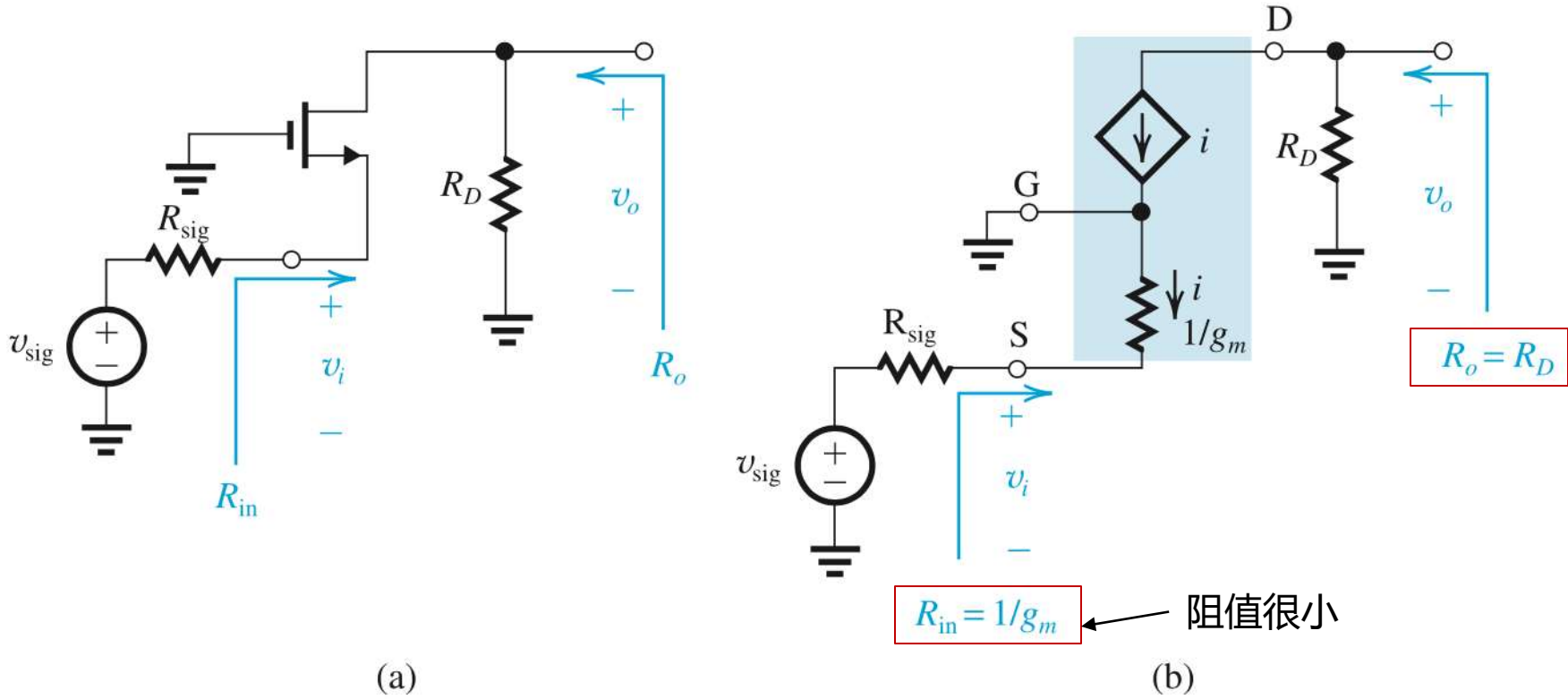


Figure 7.39 **(a)** Common-gate (CG) amplifier with bias arrangement omitted. **(b)** Equivalent circuit of the CG amplifier with the MOSFET replaced with its T model.

CG电压增益是正的

$$v_o = -iR_D$$

$$i = -\frac{v_i}{1/g_m}$$

$$A_{vo} \equiv \frac{v_o}{v_i} = g_m R_D$$

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{1/g_m}{1/g_m + R_{sig}}$$

理解一：信号通路上S点进行分拆，级联计算

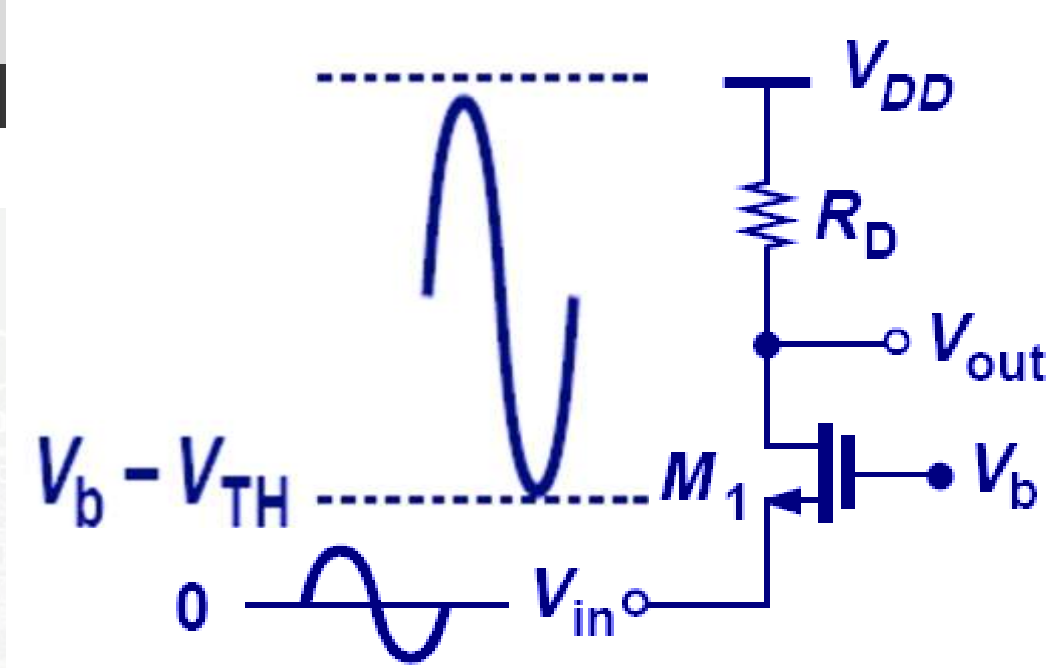
$$G_v = \frac{1/g_m}{R_{sig} + 1/g_m}[g_m(R_D \| R_L)]$$

$$= \frac{(R_D \| R_L)}{R_{sig} + 1/g_m}$$

理解二：$i_d = i_s$，**理解并记忆抓住电流，写出$v_o v_i$的表达式**

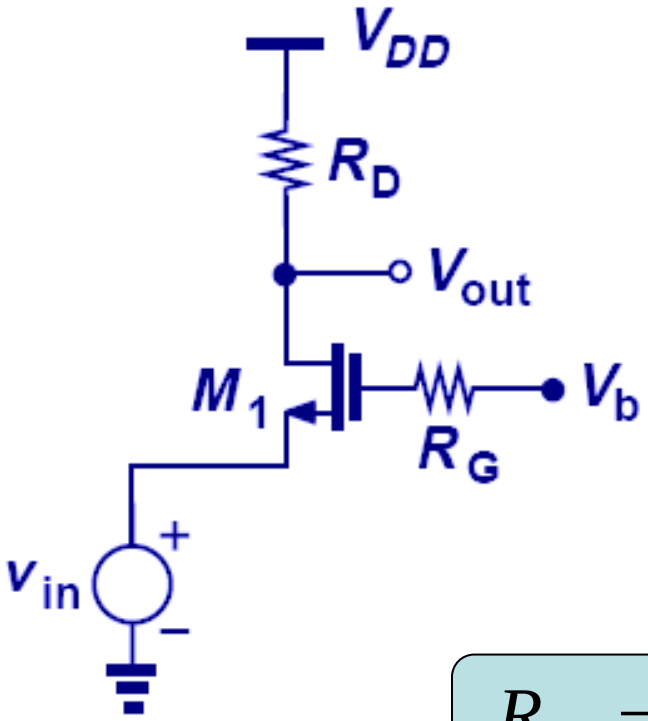
$$G_v = \frac{\text{res tied from "D" to ac GND}}{\text{total res in source circuit}}$$

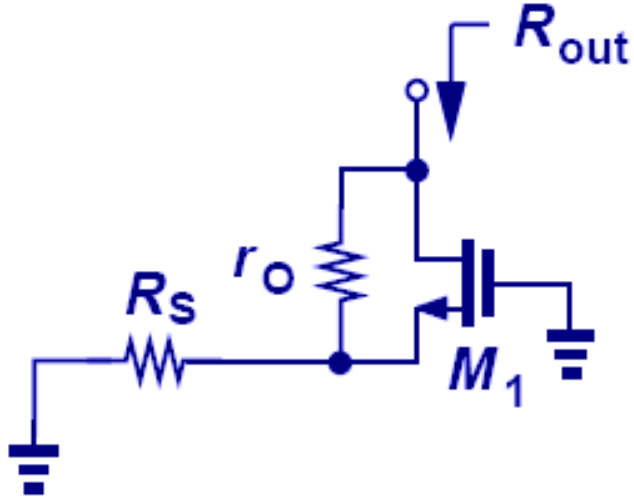
Signal Levels in CG Stage



- 为了保持 M_1 工作于饱和区, V_{out} 的信号波动不能使V_{out}小于 V_b-V_{TH}.

Generalized CG Behavior

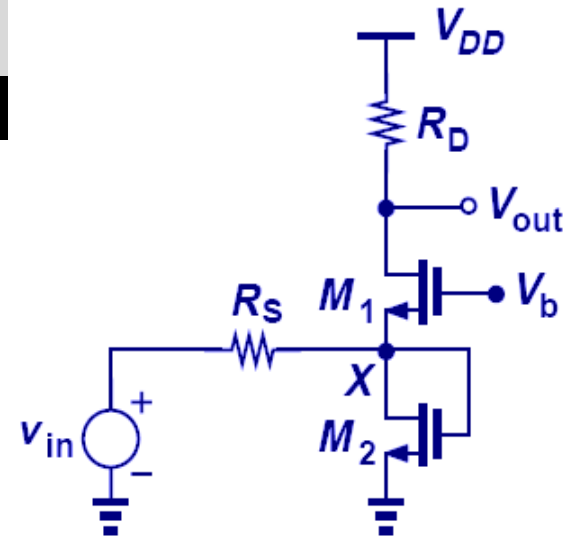


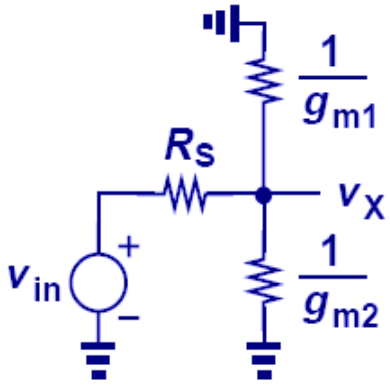


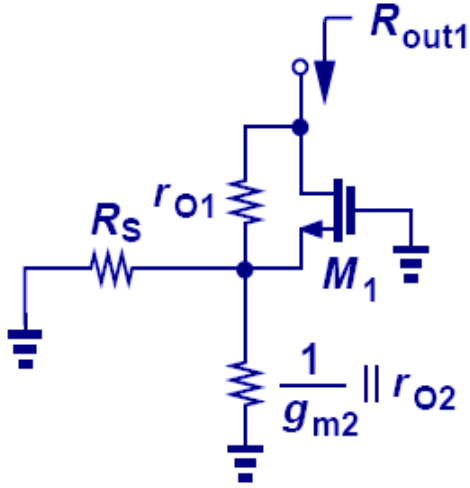
$$R_{out} = (1 + g_m r_O) R_S + r_O$$

- 栅极电阻没影响；
- 若考虑信号源电阻，输出阻抗特性与源极退化的CS结构一样；

Example of CG Stage







$$\frac{v_X}{v_{in}} = \frac{1/g_{m1} \| 1/g_{m2}}{R_S + 1/g_{m1} \| 1/g_{m2}} \qquad \frac{v_{out}}{v_X} = g_{m1} R_D$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} R_D}{1 + (g_{m1} + g_{m2}) R_S} \qquad R_{out} \approx \left[(1 + g_{m1} r_{O1}) \left(\frac{1}{g_{m2}} \| R_S \right) + r_{O1} \right] \| R_D$$

- Diode-connected M_2 作电阻使用，其阻值为$1/g_{m2}$
- 通过X点，级联计算

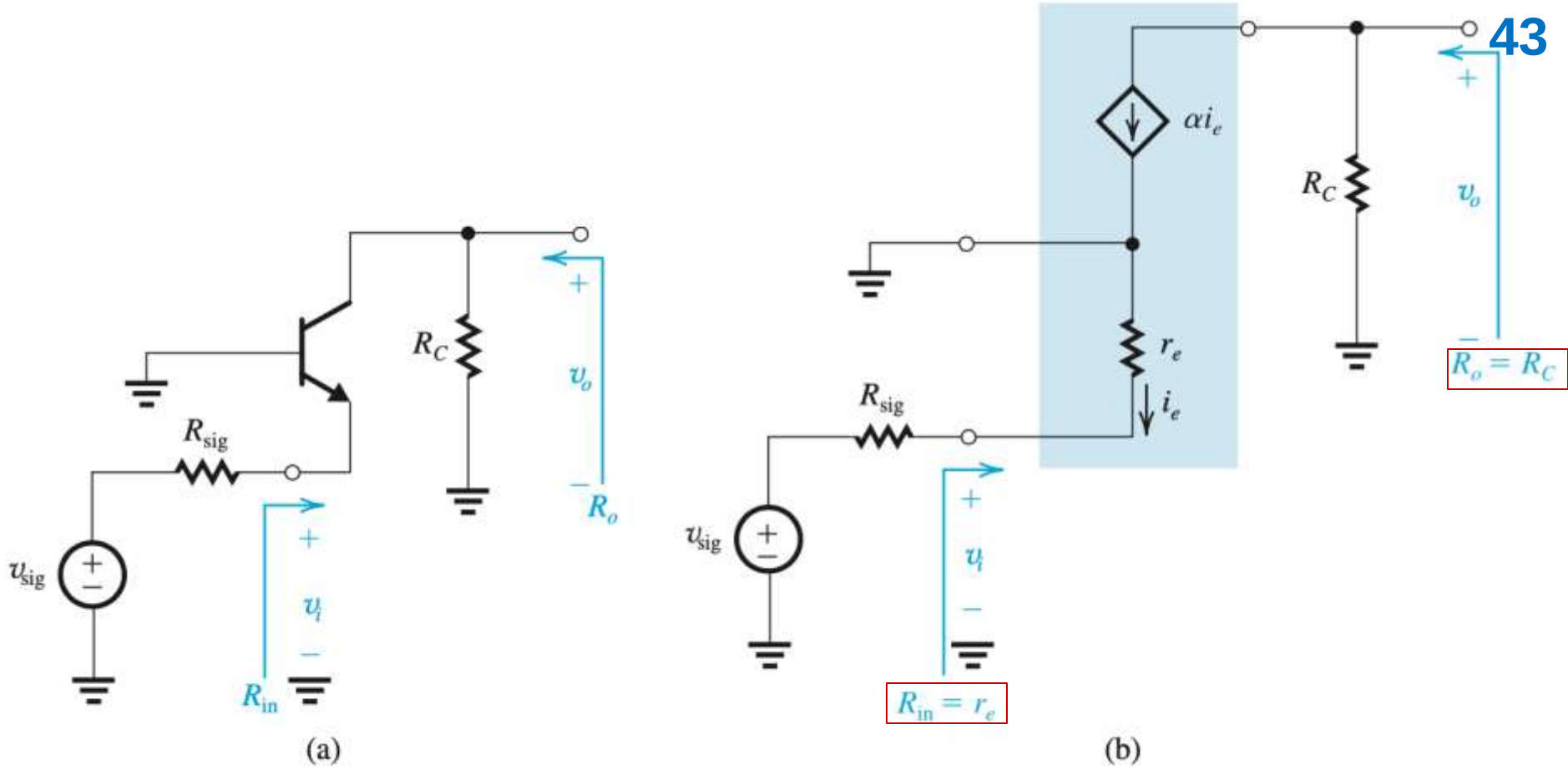


Figure 7.40 (**a**) CB amplifier with bias details omitted; (**b**) amplifier equivalent circuit with the BJT represented by its T model.

$$R_{in} = r_e = \frac{\alpha}{g_m} \simeq 1/g_m$$

$$G_v \equiv \frac{v_o}{v_{sig}} = \alpha \frac{R_C \| R_L}{R_{sig} + r_e}$$

$$A_{vo} = \frac{\alpha}{r_e} R_C = g_m R_C$$

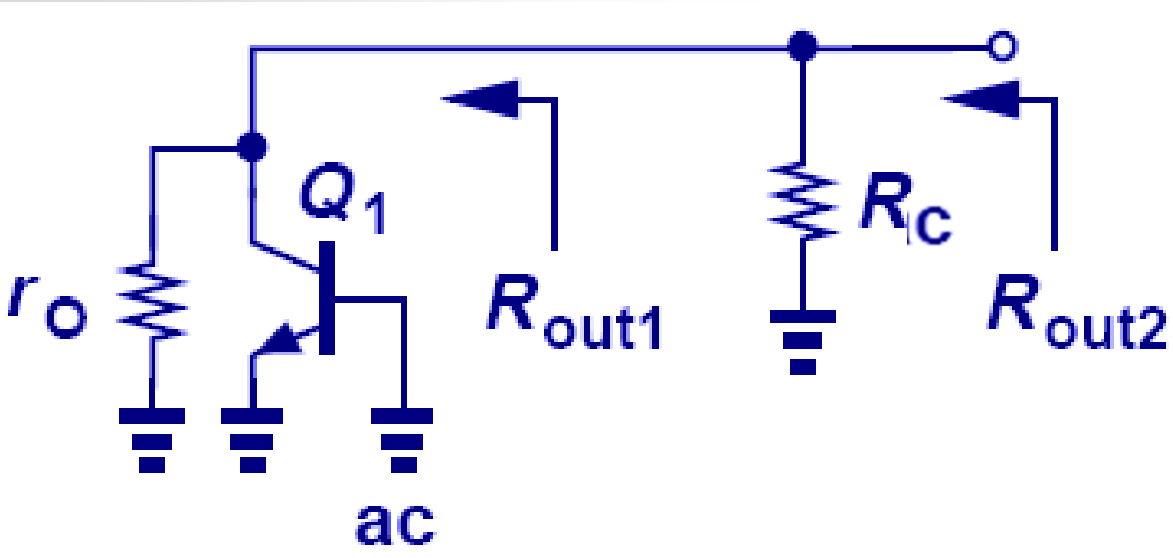
理解：$i_c = \alpha i_e$，**理解并记忆**

抓住电流，写出$v_o v_i$的表达式

$$G_v = \alpha \frac{\text{res tied from "C" to ac GND}}{\text{total res in emitter circuit}}$$

估算时，α可近似为1

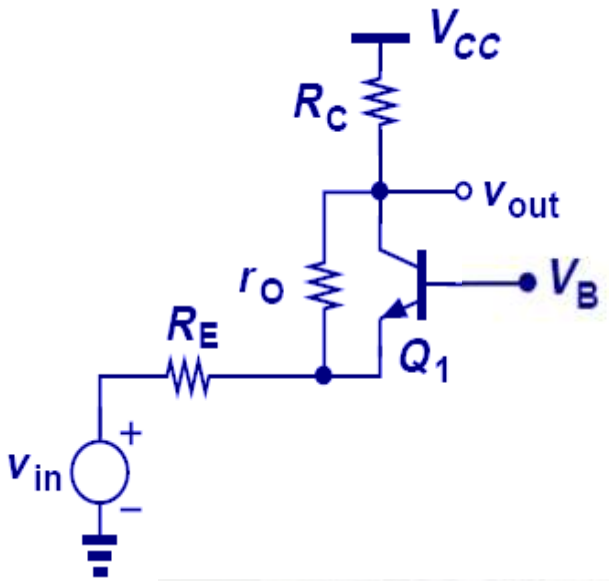
CB的输出阻抗（考虑厄雷效应）

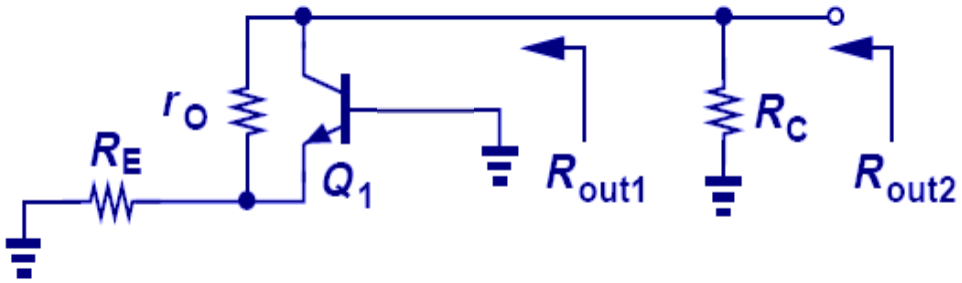


$$R_{out} = r_O \| R_C$$

- CB的输出阻抗与CE一样

CB的输出阻抗（考虑厄雷效应）

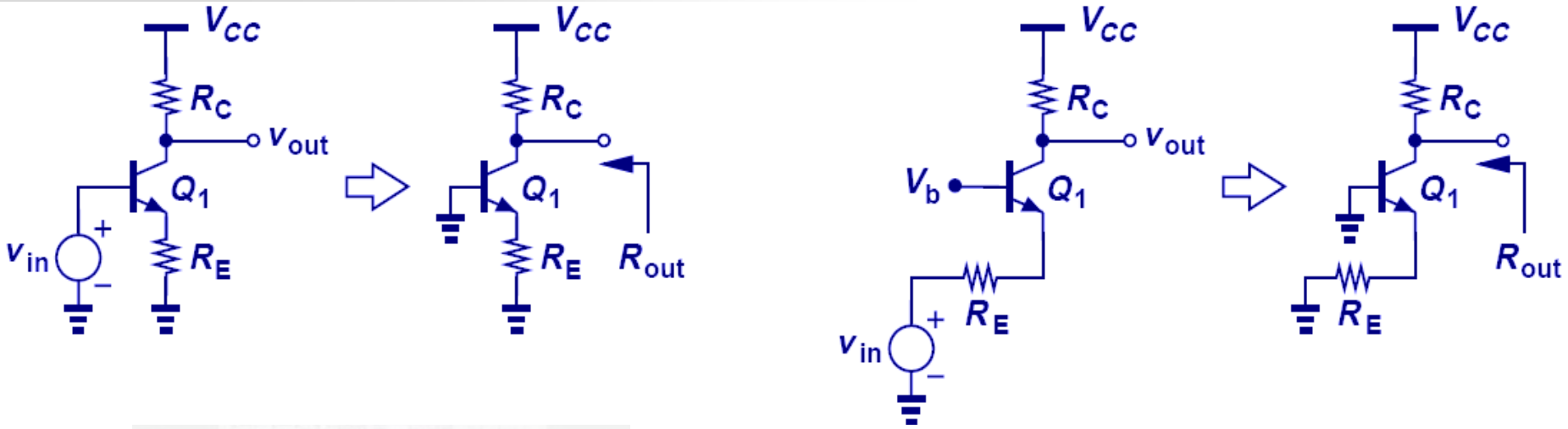




$$R_{out1} = [1 + g_m(R_E \parallel r_\pi)]r_O + (R_E \parallel r_\pi)$$

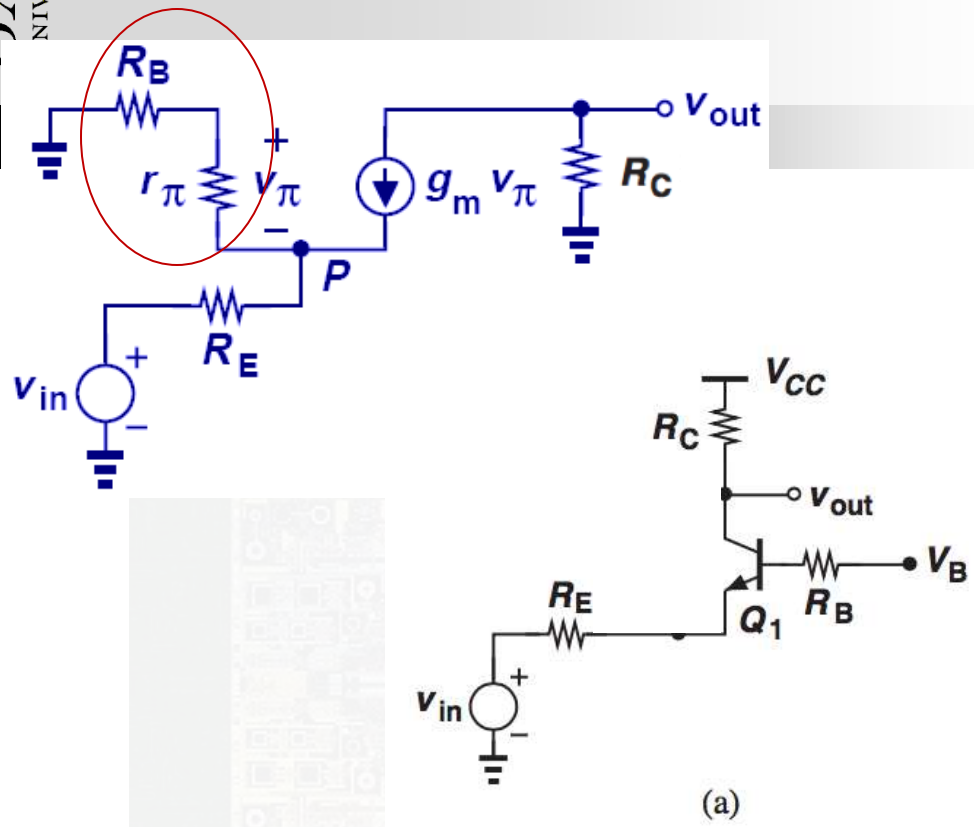
$$R_{out} = R_C \parallel R_{out1}$$

CE 和 CB 输出阻抗比较



- 计算输出阻抗时，因输入信号需短路，所以输入信号是加在发射极还是基极，小信号电路是一样的。

考虑基极电阻

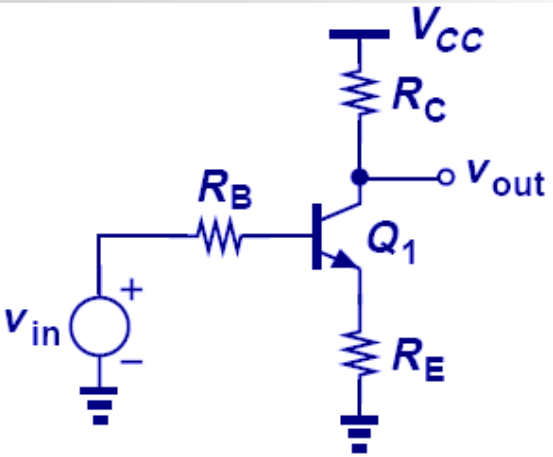


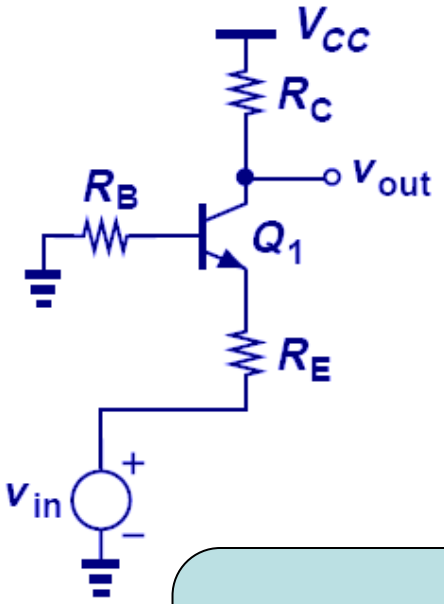
理解：原先的r_π变成$r_\pi + R_B$了，r_π折算到E极为$1/g_m$，$r_\pi + R_B$折算到E极为 $1/g_m + R_B/(\beta+1)$

$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

- 基极电阻使电路的电压增益降低【基极电阻折算到E极，需缩小β+1倍】；

有基极电阻时，CB和CE的比较



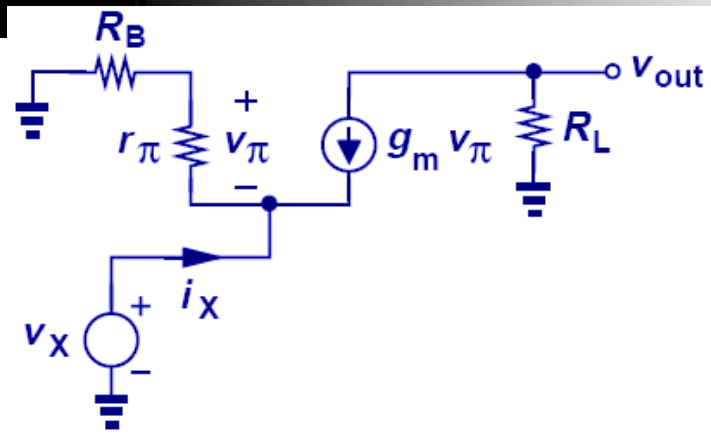


$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1}}$$

$$A_v \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

- 有基极电阻时，CB和CE的电压增益幅度是一样的，但符号不一样；
- 输入信号无论加在E，还是B，都是使V_{BE}变化，只是符号不一样，所以增益的公式也和CE类似；

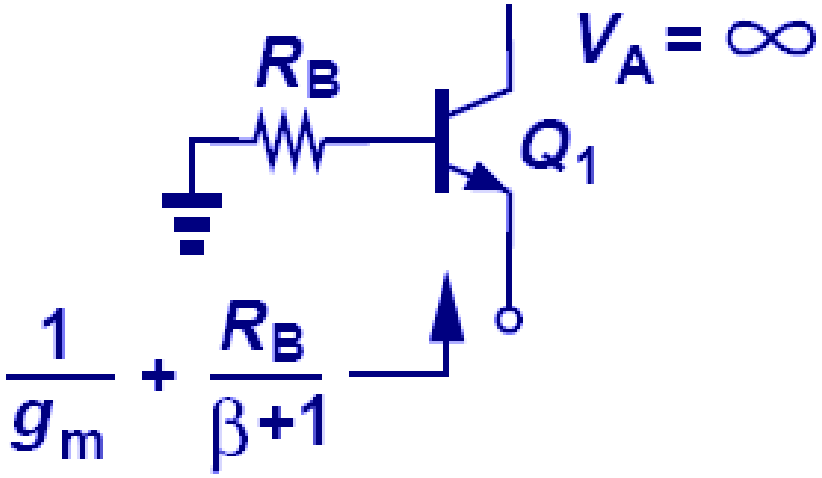
有基极电阻时CB的输入阻抗

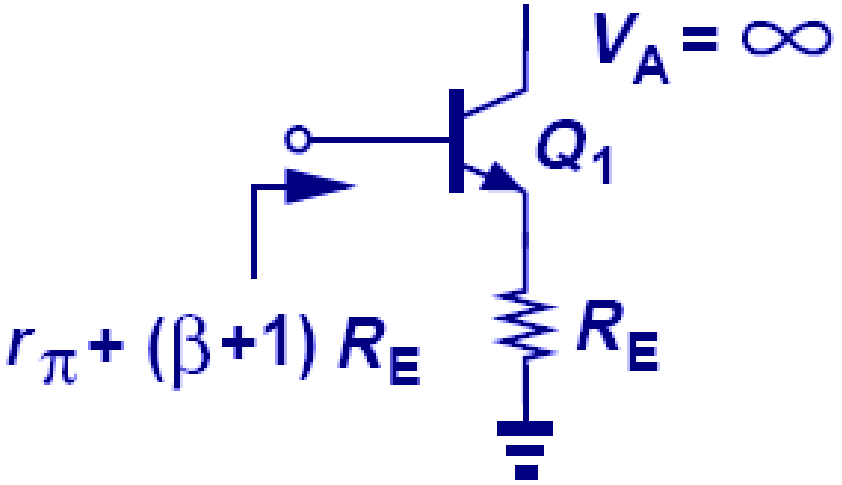


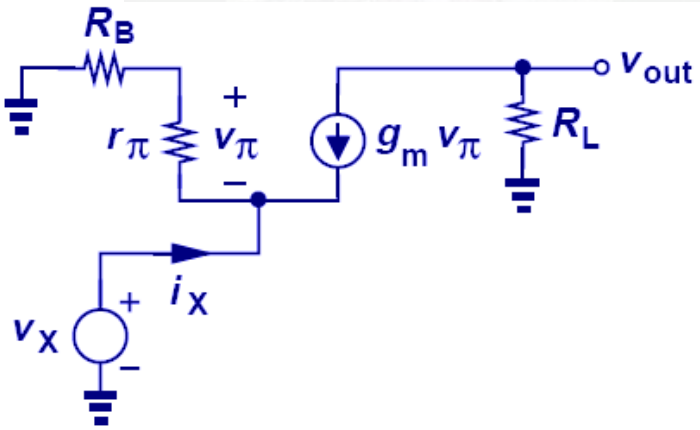
$$\frac{v_X}{i_X} = \frac{r_\pi + R_B}{\beta + 1} \approx \frac{1}{g_m} + \frac{R_B}{\beta + 1}$$

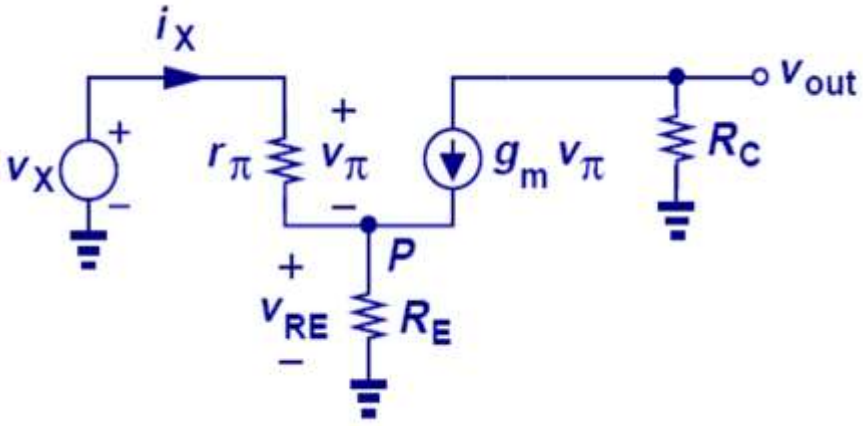
R_B也要折算到E极（$1/g_m$本来就是r_π折算到E极的结果）

从E看和从B看的输入阻抗的区别





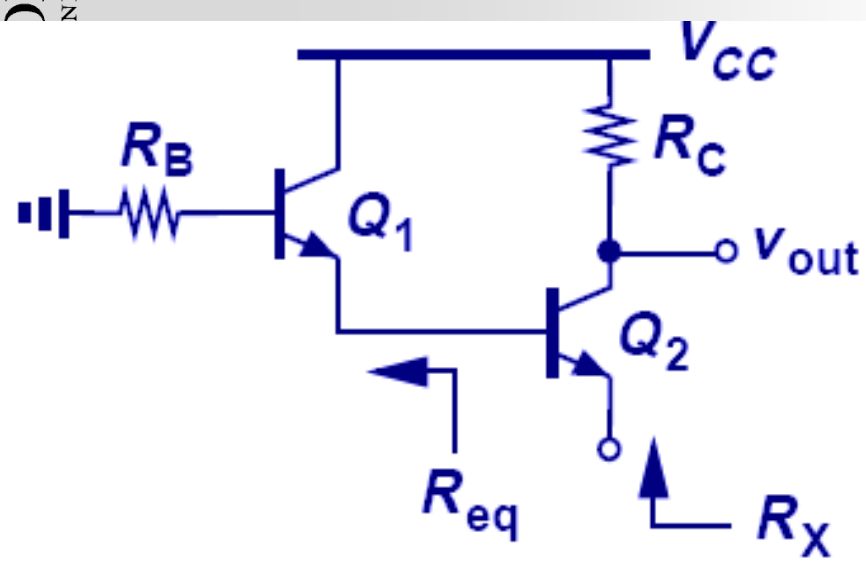


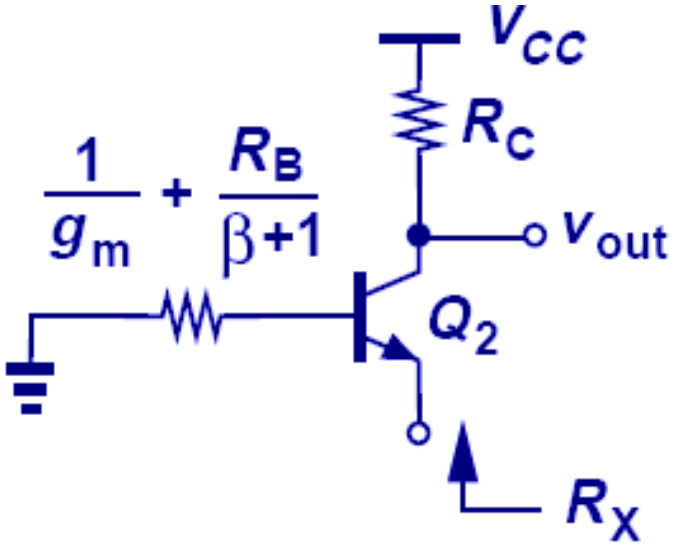


折算到E端，R_B需缩小β+1倍

折算到B端，R_E需放大β+1倍

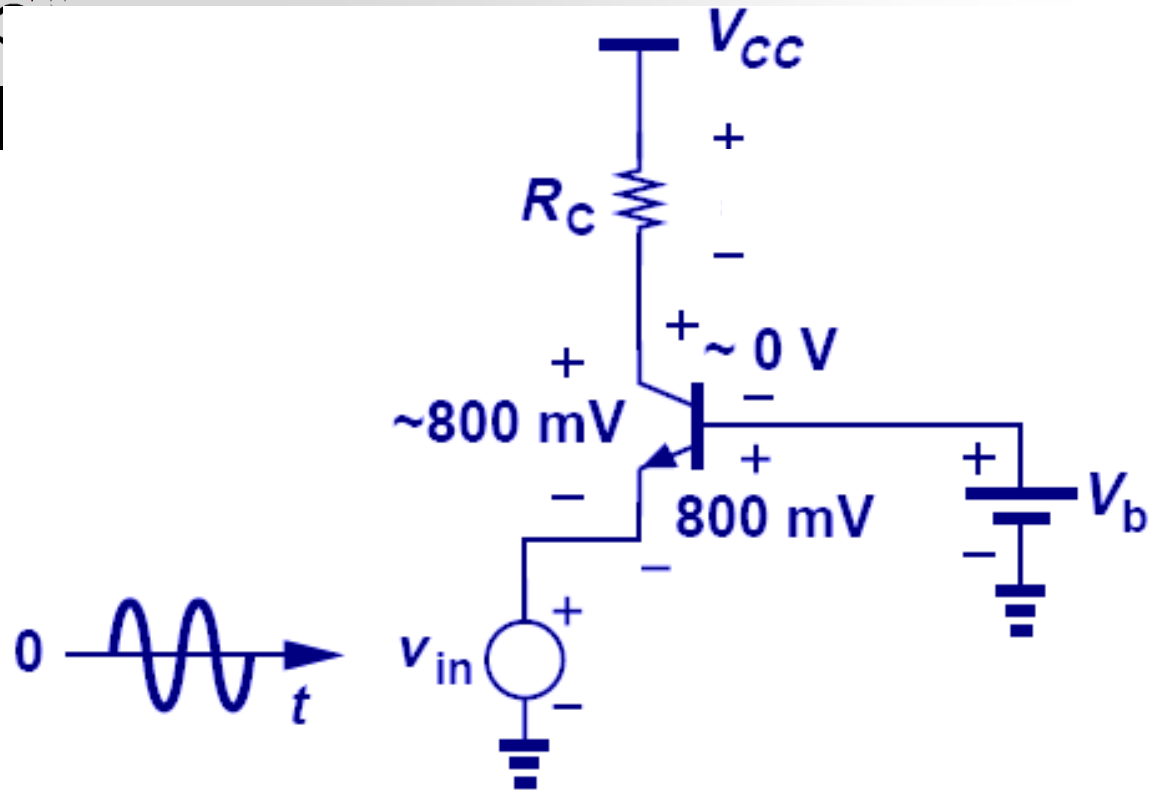
输入阻抗举例

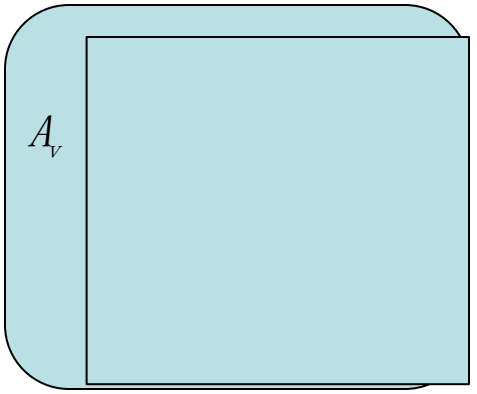

V_{CC}
R_B
R_C
Q_1
v_{out}
Q_2
R_{eq}
R_X


V_{CC}
R_C
$\frac{1}{g_m} + \frac{R_B}{\beta+1}$
v_{out}
Q_2
R_X

$$R_X =$$

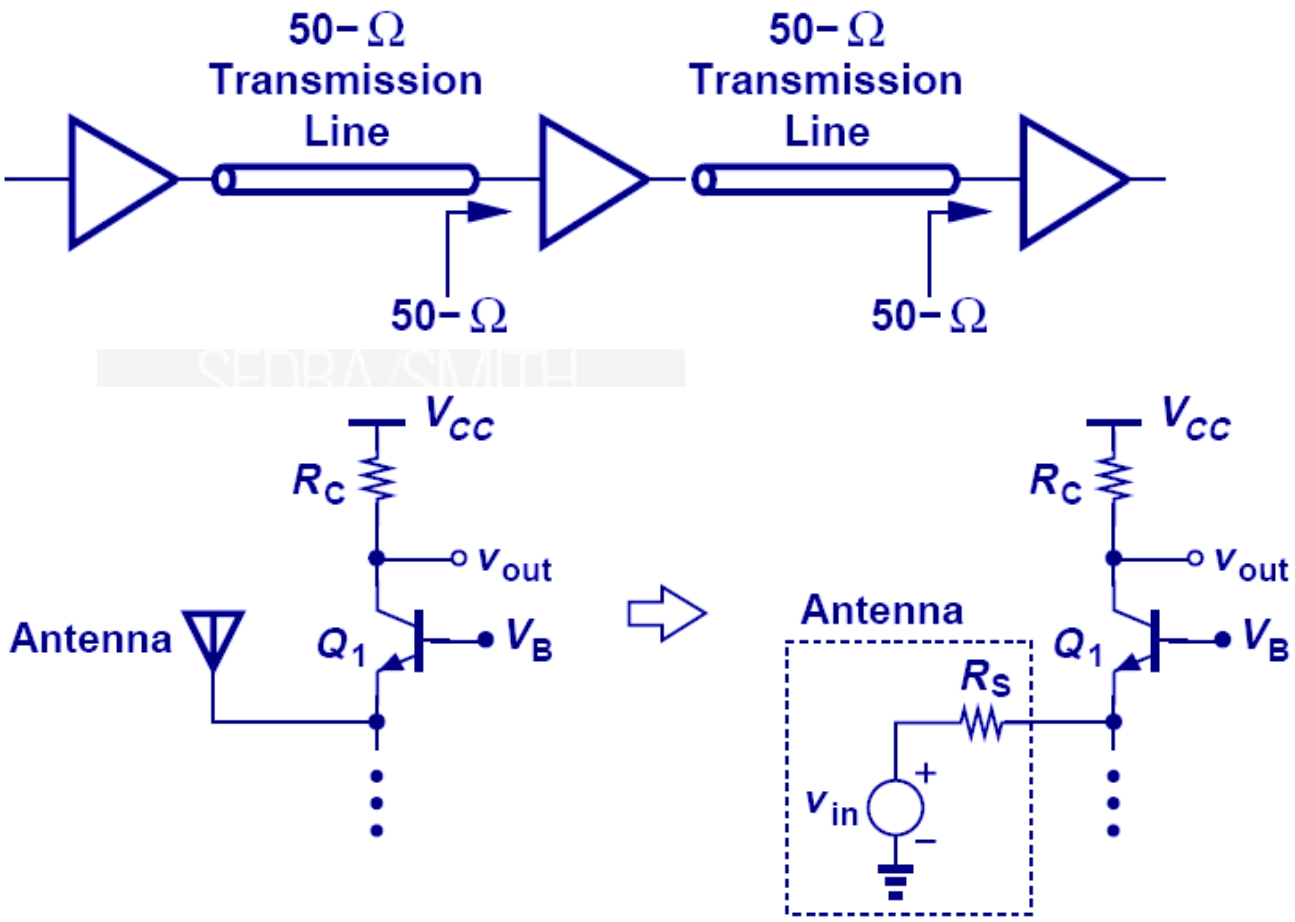
增益和Headroom的折衷





- 为了保证三极管工作在放大区, R_C 上面最大的电压降不能超过V_{CC}-(V_B-0.4V)

CB的实际应用

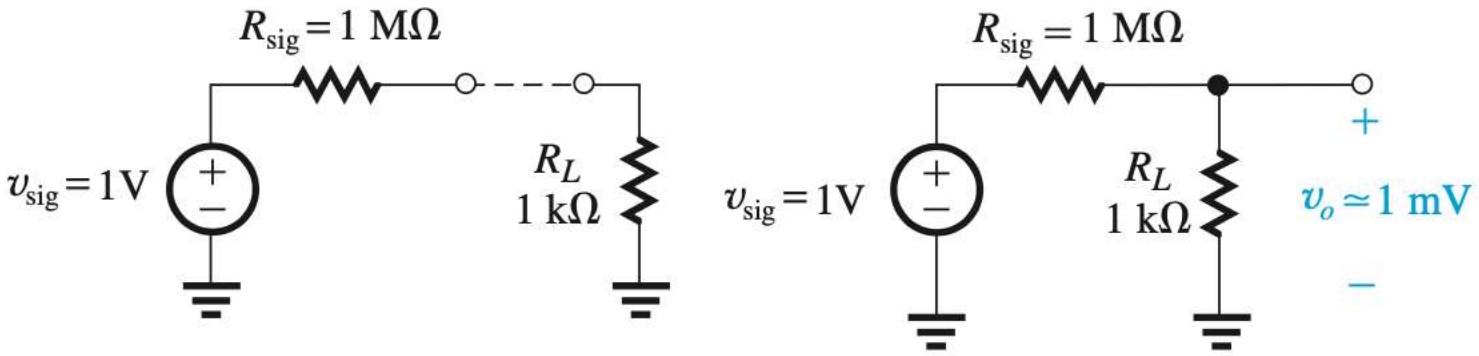


- 在射频电路与系统中，为了避免反射，输入阻抗一般要匹配到50欧姆.
- $1/g_m$ 可以方便地设计出50欧姆的输入阻抗

CG/CB 小结

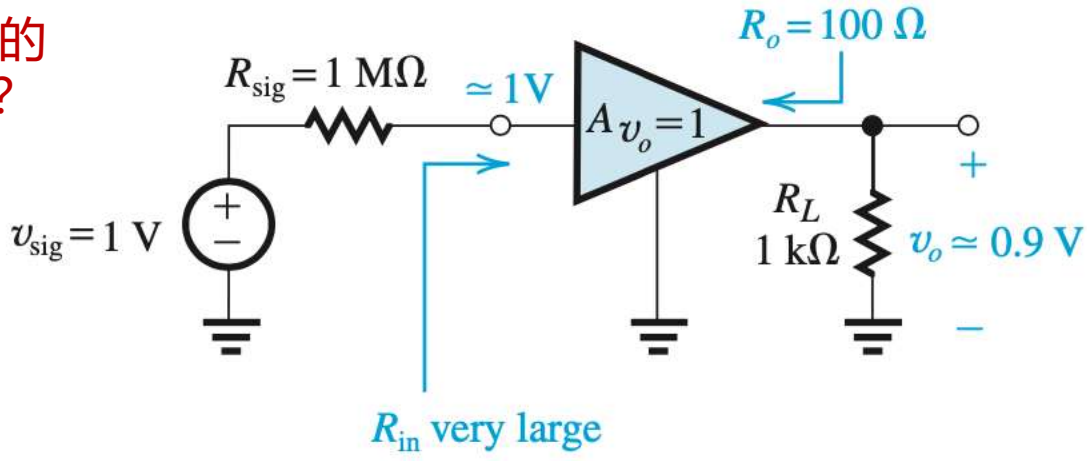
- 增益为正，表达式与CS/CE相同
- 输入阻抗为$1/g_m$（无基极电阻时），输入阻抗小且可调，适合于射频电路阻抗匹配
- 当基极有电阻时，计算增益和输入阻抗时，都需将基极电阻折算到E极，折算方法是除以（β+1）
- CG/CB有较好的高频特性（如前所述，CS/CE高频特性不佳），所以高频电路往往将 CG/CB + CS/CE 组合起来用

Motivation： 需要一个电压Buffer



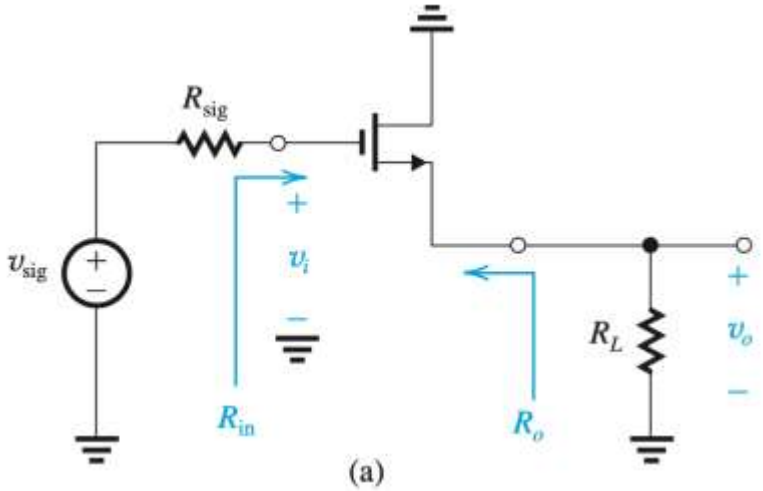
①若信号源内阻较大，直接驱动一个低电阻，电压幅度损失严重

Q：我们已经学过的Buffer的实现方式?



②插入一个电压Buffer（增益约为1，输入阻抗很大，输出阻抗很小），可有效解决这一问题

Figure 7.41 Illustrating the need for a unity-gain voltage buffer amplifier.

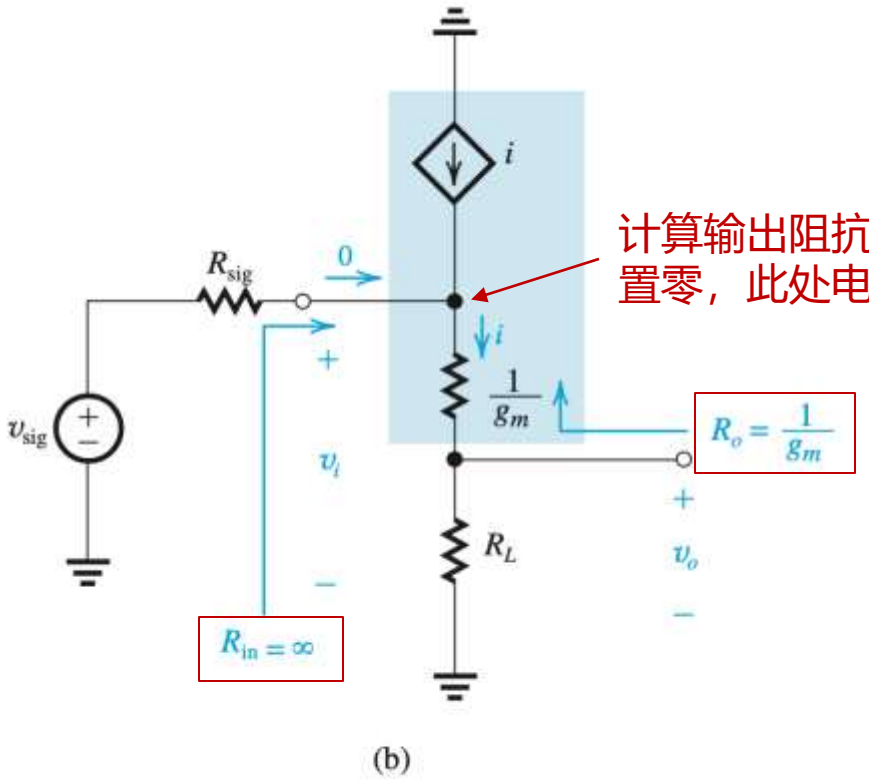


$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m}$$

理解：可看成在E极的电阻分压

$$A_{vo} = 1 \Leftarrow (\text{若} R_L = \infty)$$

$$G_v = A_v = \frac{R_L}{R_L + 1/g_m} \Leftarrow (R_{in} = \infty)$$



计算输出阻抗时，v_{sig}置零，此处电压为0

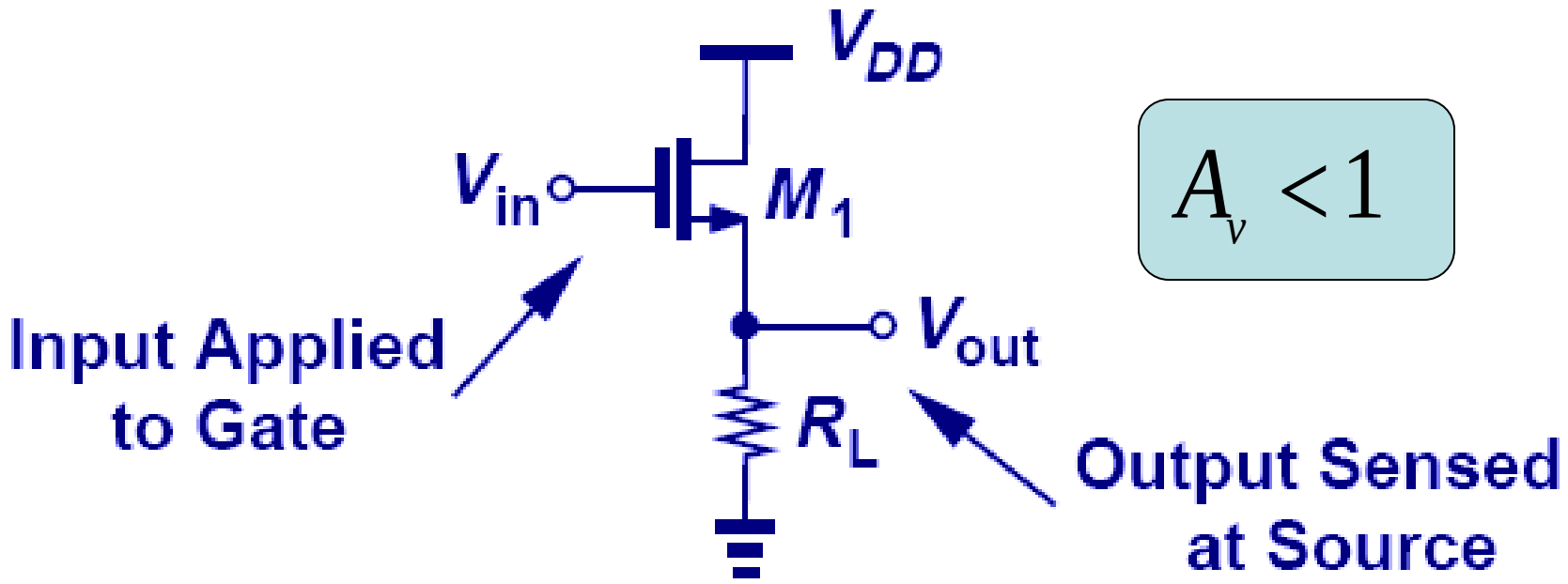
输出阻抗较低，适合驱动低电阻负载

Q：如果考虑沟道调制效应呢？

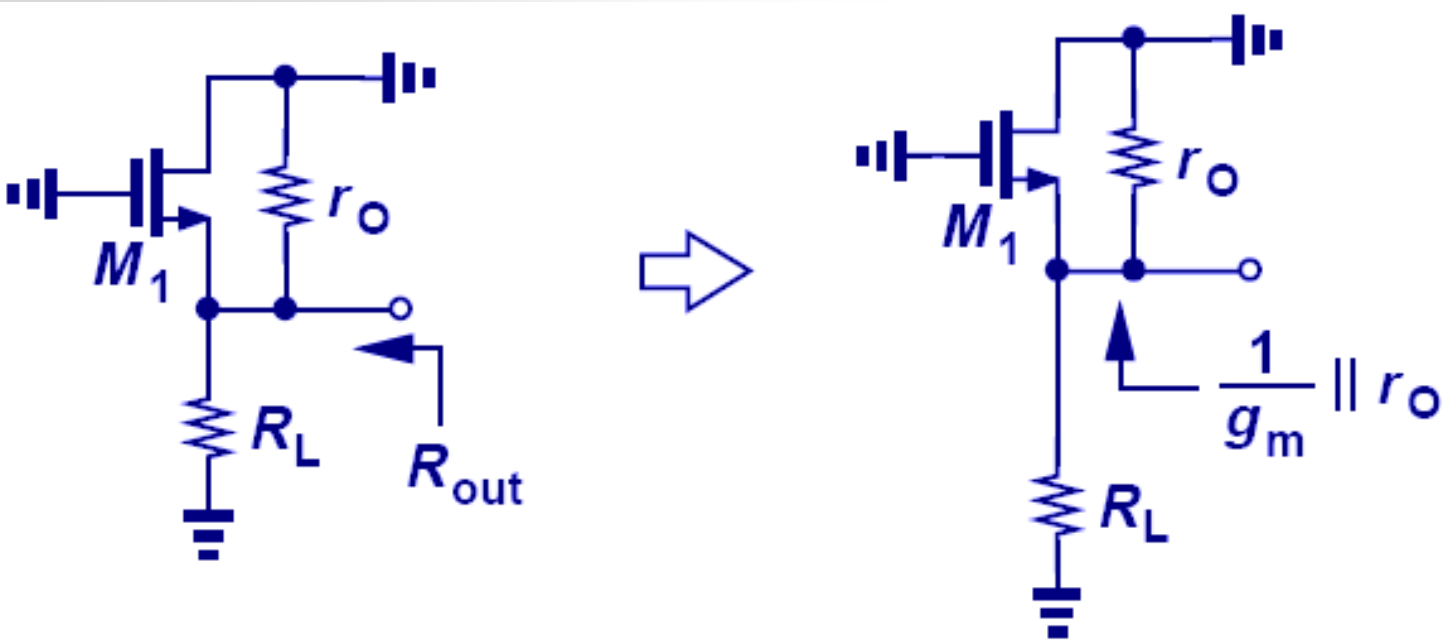
$$R_o = \frac{1}{g_m} || r_o$$

Figure 7.42 **(a)** Common-drain amplifier or source follower with the bias circuit omitted. **(b)** Equivalent circuit of the source follower obtained by replacing the MOSFET with its T model.

Source Follower Stage
（源极跟随组态）



Source Follower 的输出阻抗



输出阻抗计算时，要看清楚从哪里看进去的输出阻抗，是否包含R_L？若无说明，一般不包含R_L

$$R_{out} = \frac{1}{g_m} \| r_O \| R_L \approx \frac{1}{g_m} \| R_L$$

- Source follower 的**输出阻抗相对较低**，输入阻抗很大，因此，可用作缓冲器（buffer）

Source Follower Example

Example 7.16

A source follower is realized as shown in Fig. 7.30(a), where M_2 serves as a current source. Calculate the voltage gain of the circuit.

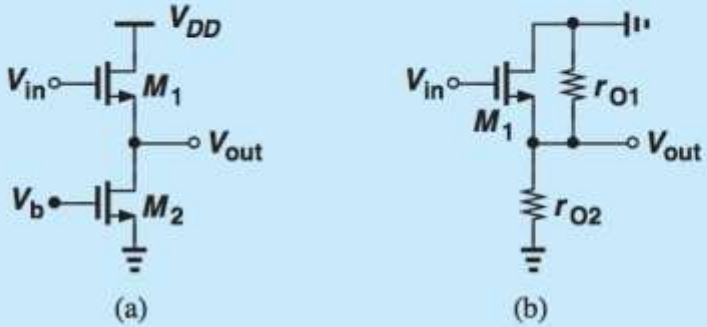
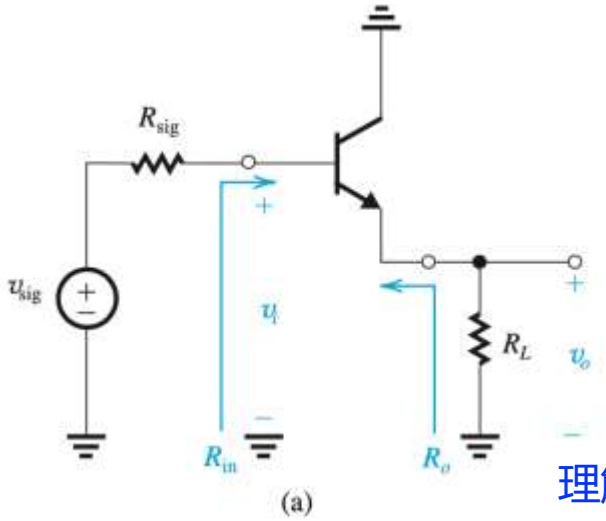


Figure 7.30 (a) Follower with ideal current source, (b) simplified circuit.

Solution Since M_2 simply presents an impedance of r_{O2} from the output node to ac ground [Fig. 7.30(b)], we substitute $R_L = r_{O2}$ in Eq. (7.131):

$$A_v = \frac{r_{O1} || r_{O2}}{\dfrac{1}{g_{m1}} + r_{O1} || r_{O2}}. \tag{7.132}$$

If $r_{O1} || r_{O2} \gg 1/g_{m1}$, then $A_v \approx 1$.



$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + r_e}$$

从v_i到v_o的电压增益，可以用E处的电阻分压来理解

$$A_{vo} = 1 \Leftarrow (\text{若} R_L = \infty)$$

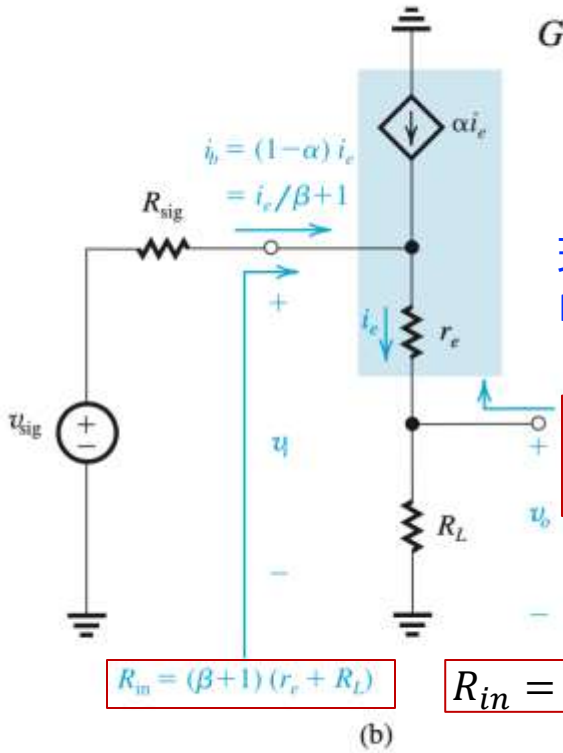
$$R_{in} \neq \infty \Rightarrow \frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}}$$

理解2：将E极电阻折算到B，$R_L + R_E$乘以(β+1)

$$G_v = \frac{(\beta+1)R_L}{(\beta+1)R_L + (\beta+1)r_e + R_{sig}} = \frac{(\beta+1)(r_e + R_L)}{(\beta+1)(r_e + R_L) + R_{sig}}$$

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times A_v$$

理解1：级联



理解3：将基极电阻折算到E，R_{sig}除以(β+1)，**理解并记忆**

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + r_e + R_{sig}/(\beta+1)}$$

$$R_{out} = r_e + \frac{R_{sig}}{\beta+1}$$

输出阻抗从E看进去，需要将B处的电阻折算到E处（除以 β+1）

$$R_{in} = r_\pi + (\beta+1)R_L$$

输入阻抗从B看进去，需要将E处的电阻折算到B处（乘以 β+1）

Figure 7.43 (**a**) Common-collector amplifier or emitter follower with the bias circuit omitted. (**b**) Equivalent circuit obtained by replacing the BJT with its T model.

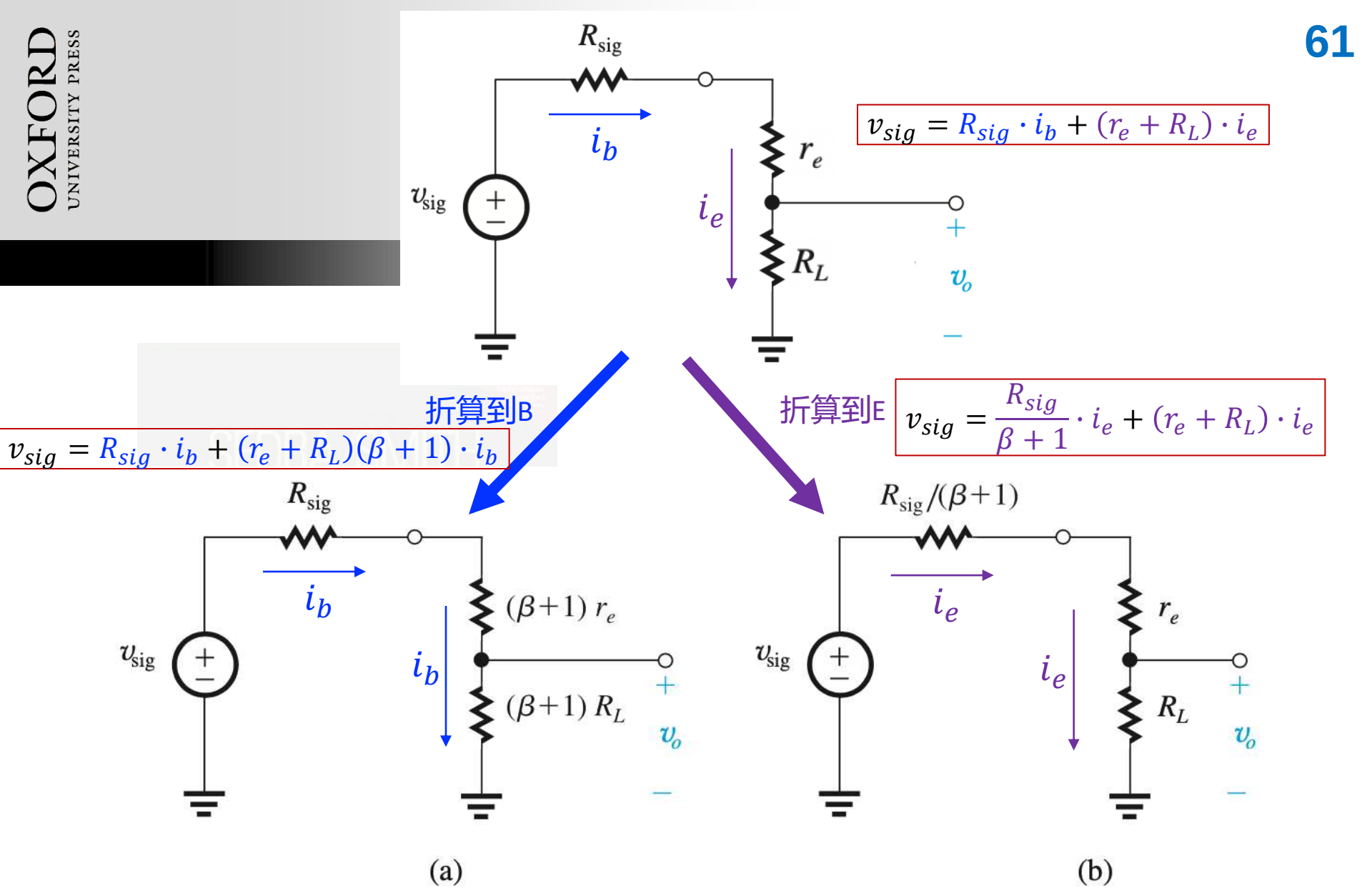


Figure 7.44 Simple equivalent circuits for the emitter follower obtained by (**a**) reflecting r_e and R_L to the base side, and (**b**) reflecting v_{sig} and R_{sig} to the emitter side. Note that the circuit in (**b**) can be obtained from that in (**a**) by simply dividing all resistances by $(\beta + 1)$.

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射极跟随的戴维南等效电路

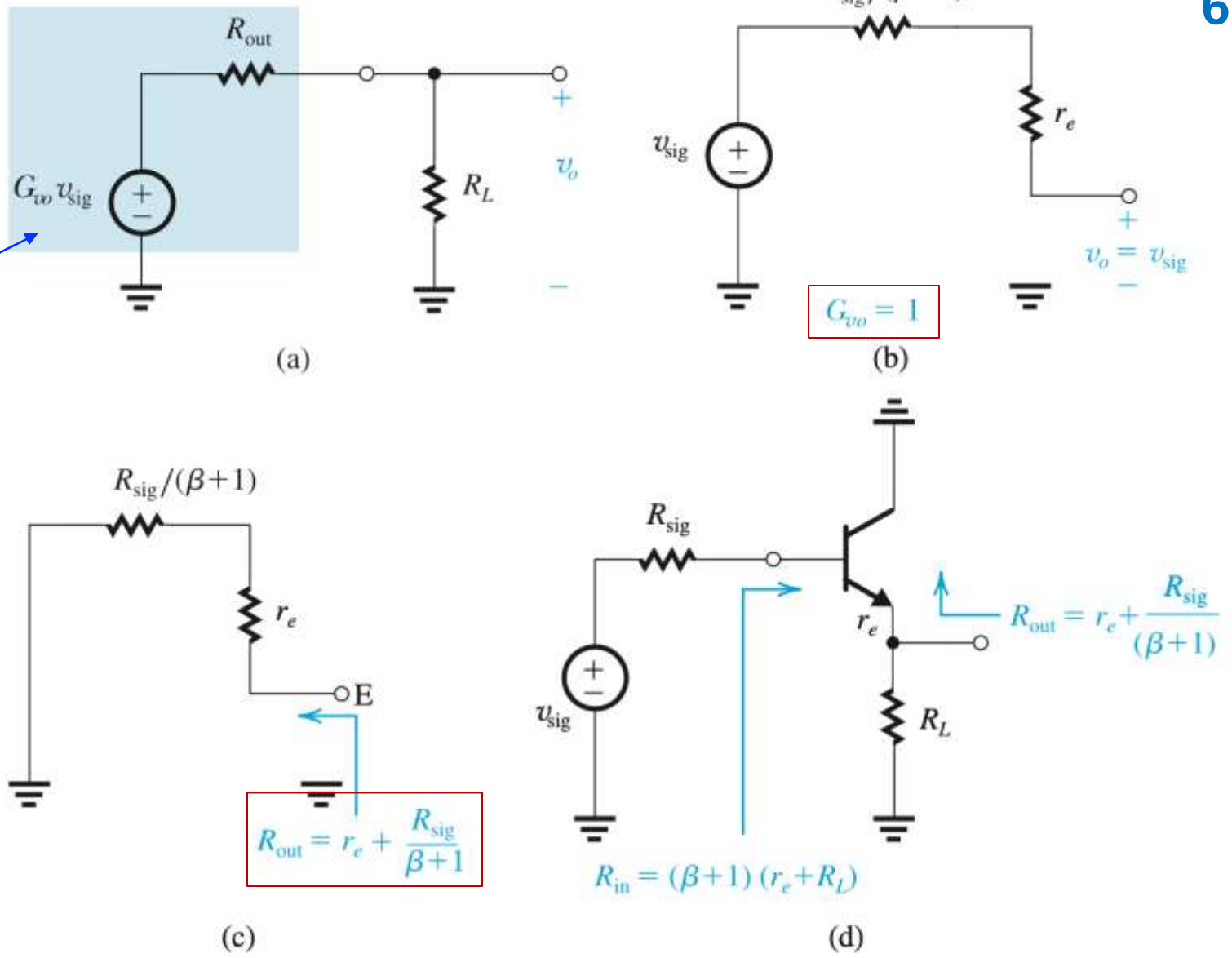
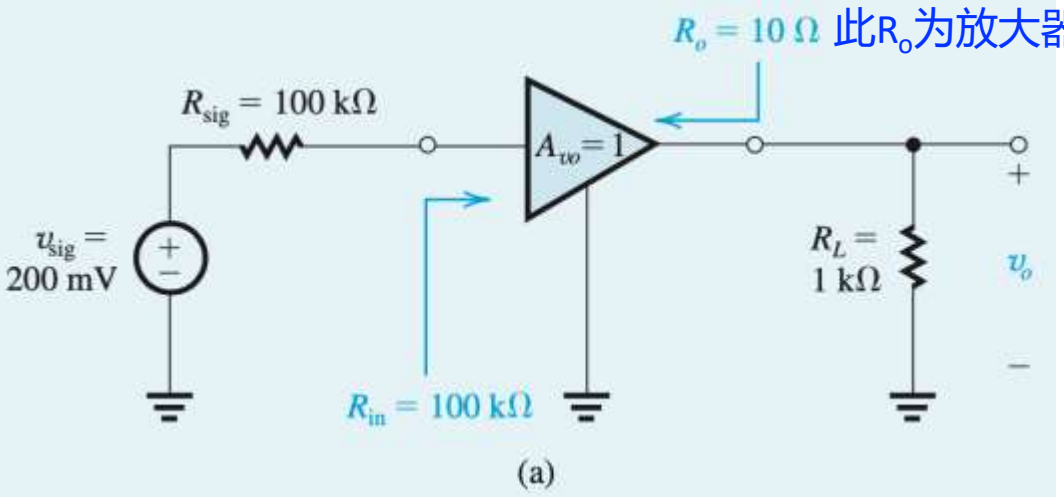


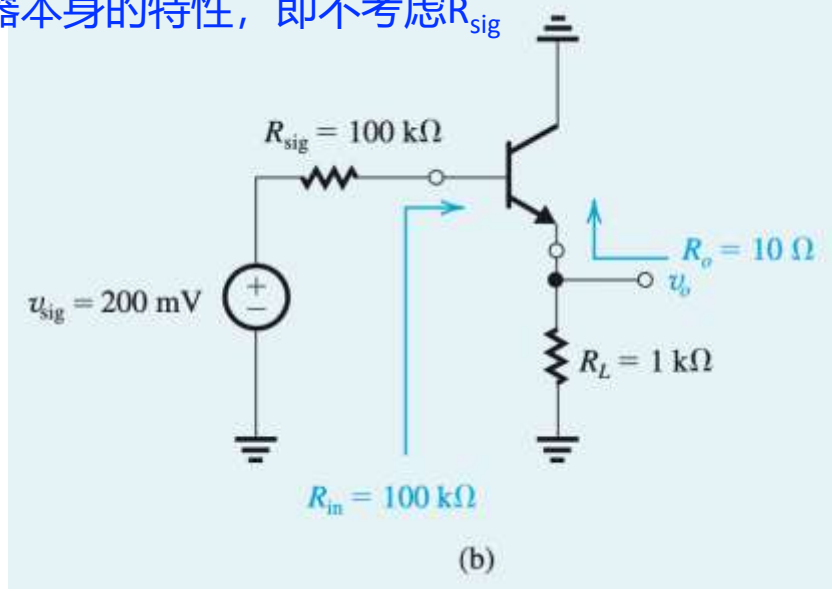
Figure 7.45 (**a**) Thévenin representation of the output of the emitter follower. (**b**) Obtaining G_{vo} from the equivalent circuit in Fig. 7.44(b). (**c**) Obtaining R_{out} from the equivalent circuit in Fig. 7.44(b) with v_{sig} set to zero. (**d**) The emitter follower with R_{in} and R_{out} determined simply by looking into the input and output terminals, respectively.

Example 7.10

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{sig} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 kΩ, and to 0.5 kΩ.



此R_o为放大器本身的特性，即不考虑R_{sig}



①根据 $R_o = r_e = \alpha/g_m$，得到 g_m

$$10\ \Omega = \frac{V_T}{I_E}$$

$$I_E = 2.5\ \text{mA}$$

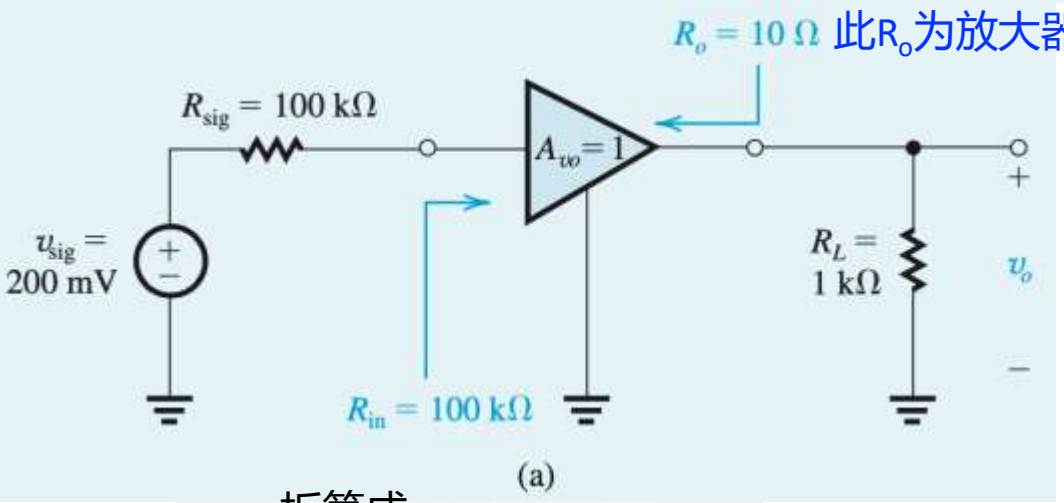
②根据 R_{in}，得到β的最小值

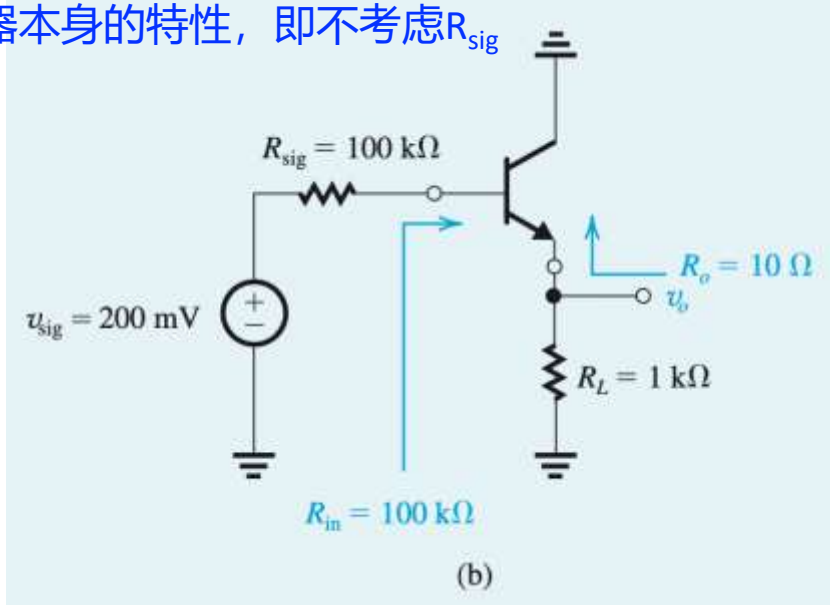
$$R_{in} = (\beta + 1)(r_e + R_L)$$

$$100 = (\beta + 1)(0.01 + 1)$$

Thus, the BJT should have a β with a minimum value of 98.

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{sig} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 kΩ, and to 0.5 kΩ.





③ $v_\pi = 5\ mV$ ⇨ 折算成v_{sig} $\dfrac{5\ mV}{10} \cdot \left(10 + 1k + \dfrac{100k}{101}\right) \approx 1\ V$

④ 分析负载变化时情形，用戴维南等效后比较方便

$$R_{out} = \frac{R_{sig}}{\beta + 1} + r_e = \frac{100}{101} + 0.01 = 1\ \text{k}\Omega$$

$$v_o = v_{sig} \frac{R_L}{R_L + R_{out}}$$

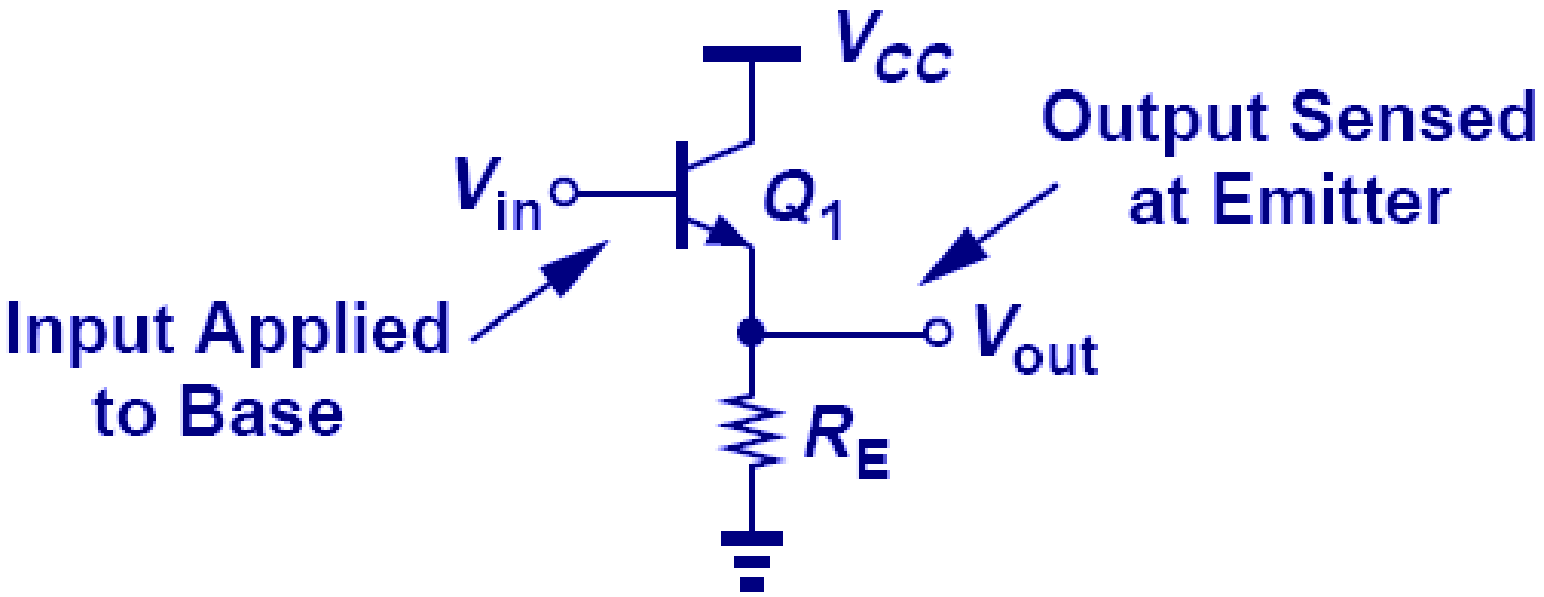
For $R_L = 2$ kΩ,

$$v_o = 200\ \text{mV} \times \frac{2}{2+1} = 133.3\ \text{mV}$$

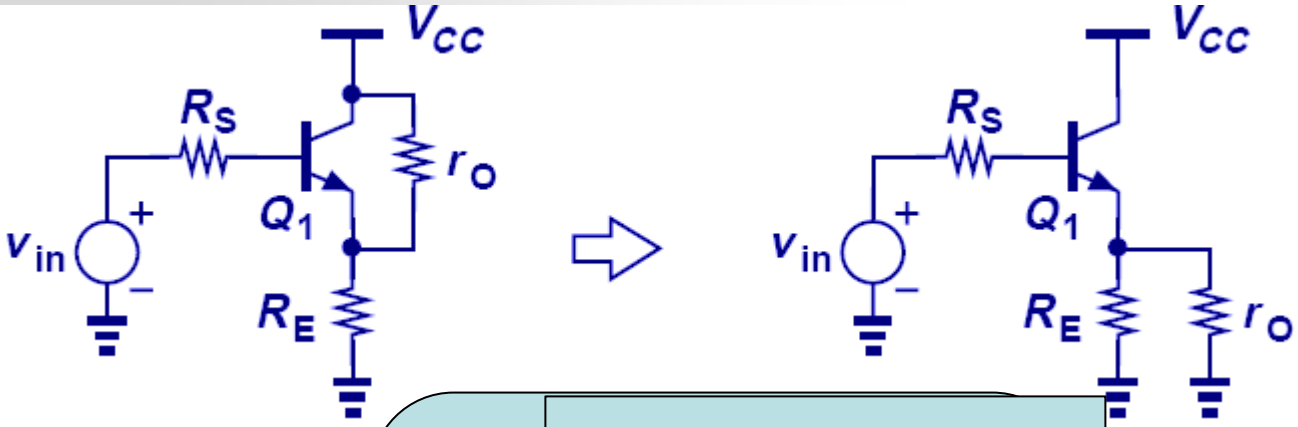
and for $R_L = 0.5$ kΩ,

$$v_o = 200\ \text{mV} \times \frac{0.5}{0.5+1} = 66.7\ \text{mV}$$

射极跟随 (Common Collector Amplifier)



考虑厄雷效应



$A_v =$

$R_{in} =$

$R_{out} =$

- 因为 r_O 与 R_E 并联，所以只需将 R_E 替换成 $R_E||r_o$ 即可；

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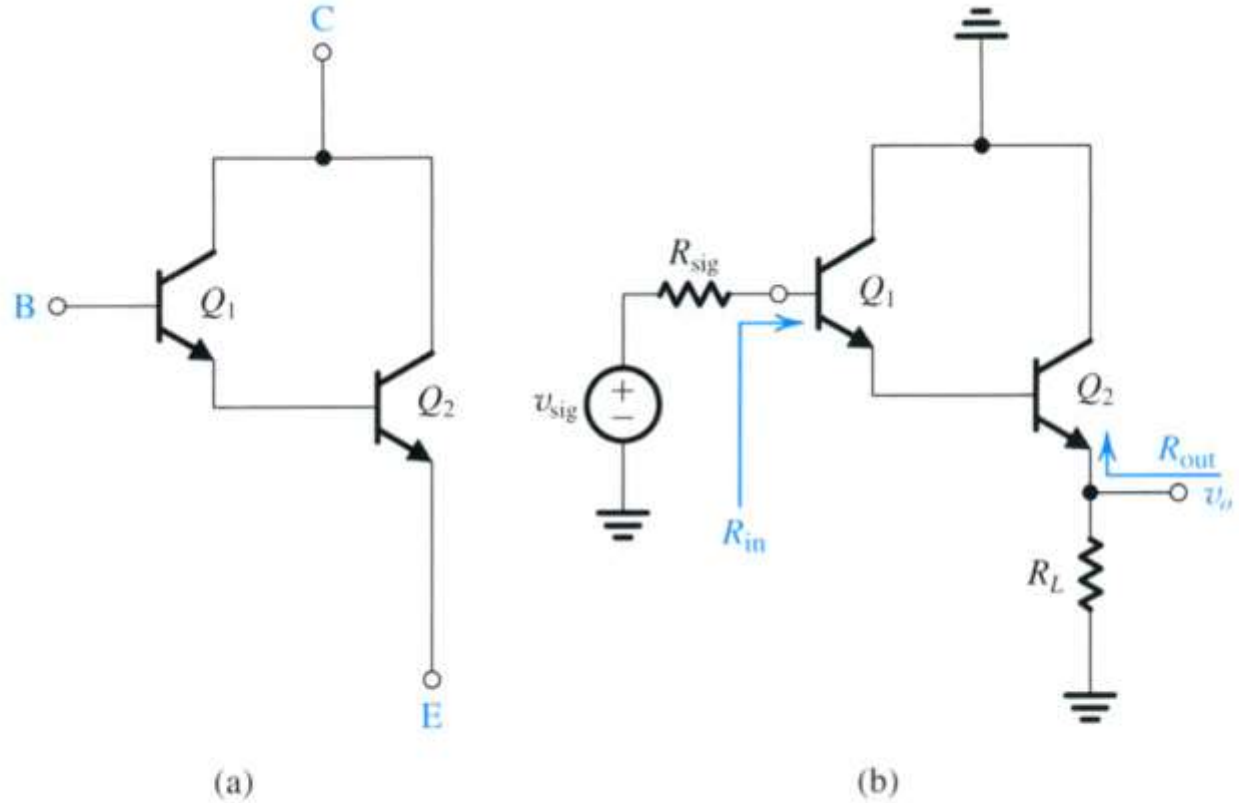

Figure 7.48 (**a**) The Darlington configuration. (**b**) Voltage follower using the Darlington configuration.

Enhancing the Emitter-Follower: The Darlington Configuration From the above we see that the performance of the emitter follower can be improved by increasing the value of β. It follows that we can obtain an enhanced emitter follower by placing two BJTs in cascade, as shown in Fig. 7.48(a). This is known as the **Darlington configuration**, and the pair of cascaded transistors as the **Darlington pair**. The Darlington pair can be thought of as a composite transistor with $\beta = \beta_1\beta_2$. It can be used to implement a high-performance voltage follower, as shown in Fig. 7.48(b).

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源极跟随/射极跟随 小结

- 增益略小于1
- 输出阻抗较小，可作为Buffer，有效驱动负载，常用于多级放大器的最后一级
- 功率放大器（PA）的实现方式

小结

- **BJT vs. MOSFET**

	MOSFET	BJT
输入阻抗	大	
跨导 g_m		大
分立电路设计（PCB）		绝大多数
集成电路设计（IC）	多数	
实现增益的主要结构	CS（可多级）	CE（可多级）
牺牲增益获取其他性能提升的方法	源极退化结构	发射极退化结构

- **什么时候考虑 r_o，什么时候不考虑?**
  - **直流偏置时，不考虑**
  - **分立电路设计时，一般可不考虑**
  - **IC设计时，必须考虑**

考试时会明确说明需不需要考虑 r_o

Table 7.4 Characteristics of MOSFET Amplifiers

Amplifier type	Characteristics[a] R_{in}	A_{vo}	R_o	A_v	G_v
Common source (Fig. 7.35)	∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_s (Fig. 7.37)	∞	$-\dfrac{g_m R_D}{1+g_m R_s}$	R_D	$\dfrac{-g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$	$-\dfrac{g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate (Fig. 7.39)	$\dfrac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\dfrac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Source follower (Fig. 7.42)	∞	1	$\dfrac{1}{g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$

[a] For the interpretation of R_{in}, A_{vo}, and R_o, refer to Fig. 7.34(b).

Table 7.5 Characteristics of BJT Amplifiers[a,b]

	R_{in}	A_{vo}	R_o	A_v	G_v
Common emitter (Fig. 7.36)	$(\beta+1)r_e$	$-g_mR_C$	R_C	$-g_m(R_C \parallel R_L)$ $-\alpha\dfrac{R_C \parallel R_L}{r_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{sig}+(\beta+1)r_e}$
Common emitter with R_e (Fig. 7.38)	$(\beta+1)(r_e+R_e)$	$-\dfrac{g_mR_C}{1+g_mR_e}$	R_C	$\dfrac{-g_m(R_C \parallel R_L)}{1+g_mR_e}$ $-\alpha\dfrac{R_C \parallel R_L}{r_e+R_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{sig}+(\beta+1)(r_e+R_e)}$
Common base (Fig. 7.40)	r_e	g_mR_C	R_C	$g_m(R_C \parallel R_L)$ $\alpha\dfrac{R_C \parallel R_L}{r_e}$	$\alpha\dfrac{R_C \parallel R_L}{R_{sig}+r_e}$
Emitter follower (Fig. 7.43)	$(\beta+1)(r_e+R_L)$	1	r_e	$\dfrac{R_L}{R_L+r_e}$	$\dfrac{R_L}{R_L+r_e+R_{sig}/(\beta+1)}$ $G_{vo}=1$ $R_{out}=r_e+\dfrac{R_{sig}}{\beta+1}$

[a] For the interpretation of R_m, A_{vo}, and R_o refer to Fig. 7.34.
[b] Setting $\beta=\infty$ ($\alpha=1$) and replacing r_e with $1/g_m$, R_C with R_D, and R_e with R_s results in the corresponding formulas for MOSFET amplifiers (Table 7.4).

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作业

7.21 A CS amplifier utilizes a MOSFET biased at $I_D = 0.25$ mA with $V_{OV} = 0.25$ V and $R_D = 20$ kΩ. The amplifier is fed with a signal source having $R_{sig} = 100$ kΩ, and a 20-kΩ load is connected to the output. Find R_{in}, A_{vo}, R_o, A_v, and G_v. If, to maintain reasonable linearity, the peak of the input sine-wave signal is limited to 10% of $2V_{OV}$, what is the peak of the sine-wave voltage at the output?

Ans. ∞; −40 V/V; 20 kΩ; −20 V/V; −20 V/V; 1 V

7.24 Show that with R_e included, and v_π limited to a maximum value $\hat{v}_\pi$, the maximum allowable input signal, $\hat{v}_{sig}$, is given by

$$\hat{v}_{sig} = \hat{v}_\pi \left(1 + \frac{R_e}{r_e} + \frac{R_{sig}}{r_\pi}\right)$$

If the transistor is biased at $I_C = 0.5$ mA and has a β of 100, what value of R_e is needed to permit an input signal $\hat{v}_{sig}$ of 100 mV from a source with a resistance $R_{sig} = 10$ kΩ while limiting $\hat{v}_\pi$ to 10 mV? What is R_{in} for this amplifier? If the total resistance in the collector is 10 kΩ, what G_v value results?

Ans. 350 Ω; 40.4 kΩ; −19.8 V/V

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7.25 A CG amplifier is required to match a signal source with $R_{sig} = 100\ \Omega$. At what current I_D should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 kΩ, what is the overall voltage gain?

Ans. 1 mA; 10 V/V

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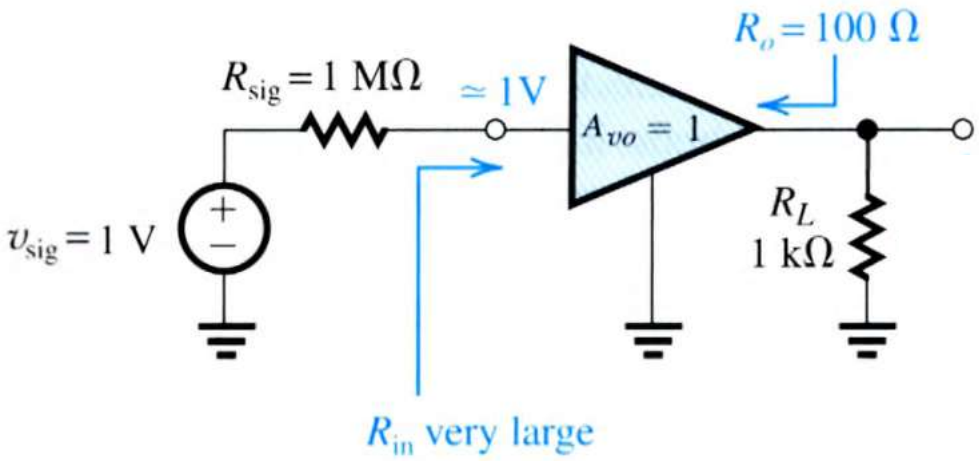
D7.28 It is required to design a source follower that implements the buffer amplifier shown in Fig. 7.42(c). If the MOSFET is operated with an overdrive voltage $V_{OV} = 0.25$ V, at what drain current should it be biased? Find the output signal amplitude and the signal amplitude between gate and source.

Ans. 1.25 mA; 0.91 V; 91 mV



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7.30 An emitter follower uses a transistor with $\beta = 100$ and is biased at $I_C = 5$ mA. It operates between a source with a resistance of 10 kΩ and a load of 1 kΩ. Find R_{in}, G_{vo}, R_{out}, and G_v. What is the peak amplitude of v_{sig} that results in v_π having a peak amplitude of 5 mV? Find the resulting peak amplitude at the output.

Ans. 101.5 kΩ; 1 V/V; 104 Ω; 0.91 V/V; 1.1 V; 1 V