Lecture28-输出级电路和功率放大器

- **13.1 A类、B类和AB类输出级电路分析**
  - 13.1.1 A类、B类和AB类输出级电路主要性能参数的分析计算，包括电源功率、负载功率、晶体管耗散功率、放大器效率和输出信号摆幅等
  - 13.1.2 AB类放大器的偏置
- **13.2 开关功率放大器基本概念（概要介绍D类放大器结构和工作原理）**

为何需要功率放大器（功放, PA, power amplifier）？

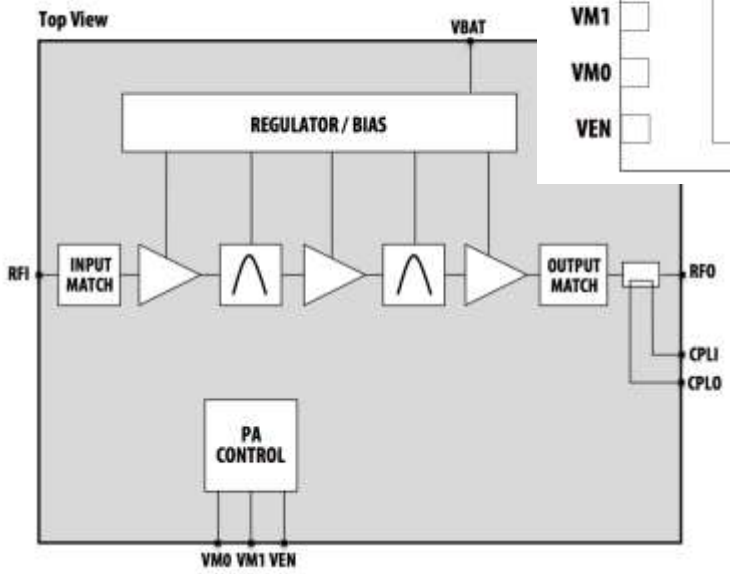
- 实际应用中往往需要用大功率来驱动负载
- 案例1：手机需要输出1W的功率给天线；（1W=30dBm）
- 案例2：高保真的音响系统需要几十~几百瓦的输出功率；
- 一般的电压/电流放大器不能满足上述需求 → 功率放大器有特殊的结构
- 此外，大功率输出时，小信号近似的前提已不成立，故严格地讲，不能简单地直接使用小信号模型分析

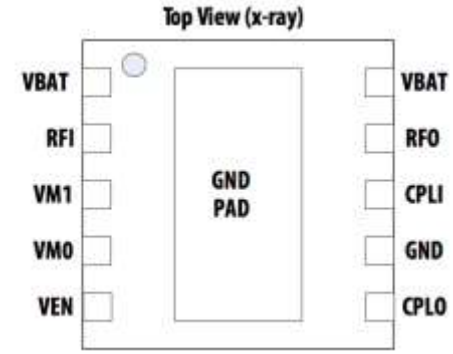
典型的商用功放芯片～Avago 手机功放芯片

AJAV-5602

W-CDMA/HSPA Band II Power Amplifier

Functional Block Diagram





Features

- High-performance 3G power amplifier
  - UMTS Band 2 (1850 – 1910 MHz)
  - W-CDMA, HSPA, and HSPA+ Compliant
- Integrated TX filtering
  - Delivers best noise in the industry
- Integrated directional coupler
- Integrated regulators and PA bias
- Single direct connection to the battery
  - No external switches or isolation inductors
- High linear efficiency
- Low average current
- High capacity CMOS process
- Small 3×3 mm package

Table 1. Absolute Minimum and Maximum Ratings [1]

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage [2]	V_{BATT}		-0.3	-	4.5	V
Control Voltage [3]	V_{CTRL}	$V_{CTRL} < V_{BATT}$	-0.3	-	4.5	V
RF Input Power [4]			-	-	+10	dBm
Maximum Linear Output Power [2]	P_{MAX}	HP mode	+26.5	+27.0	-	dBm
Power Added Efficiency [2,5,6]	PAE	HP mode	-	40	-	%

典型的日常用音响

漫步者S2.1MKII参数

综述介绍 | 报价 | 图片(45) | 参数 | 点评(55) | 论坛 | 评测行情 | 促销 | 在线购买

重要参数 | 标准配件 | 售后服务

声明：仅供参考，以当地实际销售信息为准

音箱类型：电脑音箱，低音炮音箱
音箱系统：2.1声道

有源无源：有源
调节方式：遥控

供电方式：电源：220V/50Hz
功能特点：暂无数据

音箱尺寸：低音炮：348×400×489mm
音箱材质：木质

漫步者S2.1MKII详细参数

+加入对比

基本参数	音箱类型	电脑音箱，低音炮音箱
	音箱系统	2.1声道
	有源无源	有源
	调节方式	遥控
技术参数	供电方式	电源：220V/50Hz
	额定功率	300W
	频率响应	20Hz-20KHz
	扬声器单元	10英寸+3.5英寸
	信噪比	90dB
	失真度	≤0.5% 1W 1KHz
	防磁功能	支持

漫步者 S2.1

参考价：￥749-2500

点评分：★★★★☆ (55条)

加入对比+ 详细信息

音箱品牌排行

1	漫步者	9	DOSS
2	惠威	10	金河田
3	麦博	11	三诺
4	JBL	12	不见不散
5	奋达	13	雅兰仕
6	飞利浦	14	声擎
7	耳神	15	索尼
8	哈曼卡顿	16	联想

漫步者音箱排行 更

1  漫步者S2.1MI

￥2500

典型的移动终端耳机

具有线控和麦克风功能的 Apple 入耳式耳机

RMB 598

技术规格

响应频率 : 5 Hz 到 21 kHz

阻抗 : 23 欧姆

驱动单元 : 定制双向平衡电枢（每个耳塞内配有低音扩音器和高音扩音器）

重量 : 10.2 克（0.4 盎司）

线缆长度 : 从音频插孔到分线处为 1065 毫米；从分线处到耳罩为 330 毫米

常规

带线控和麦克风

功放的特性

- 负载电阻较小（高保真音响系统的典型值为8、16、32 Ω）
- 电流较大.
- 电压摆幅较大.
- 需要供电电源提供大量的功率.
- 消耗大量的功率，产生“热”

PA的分类

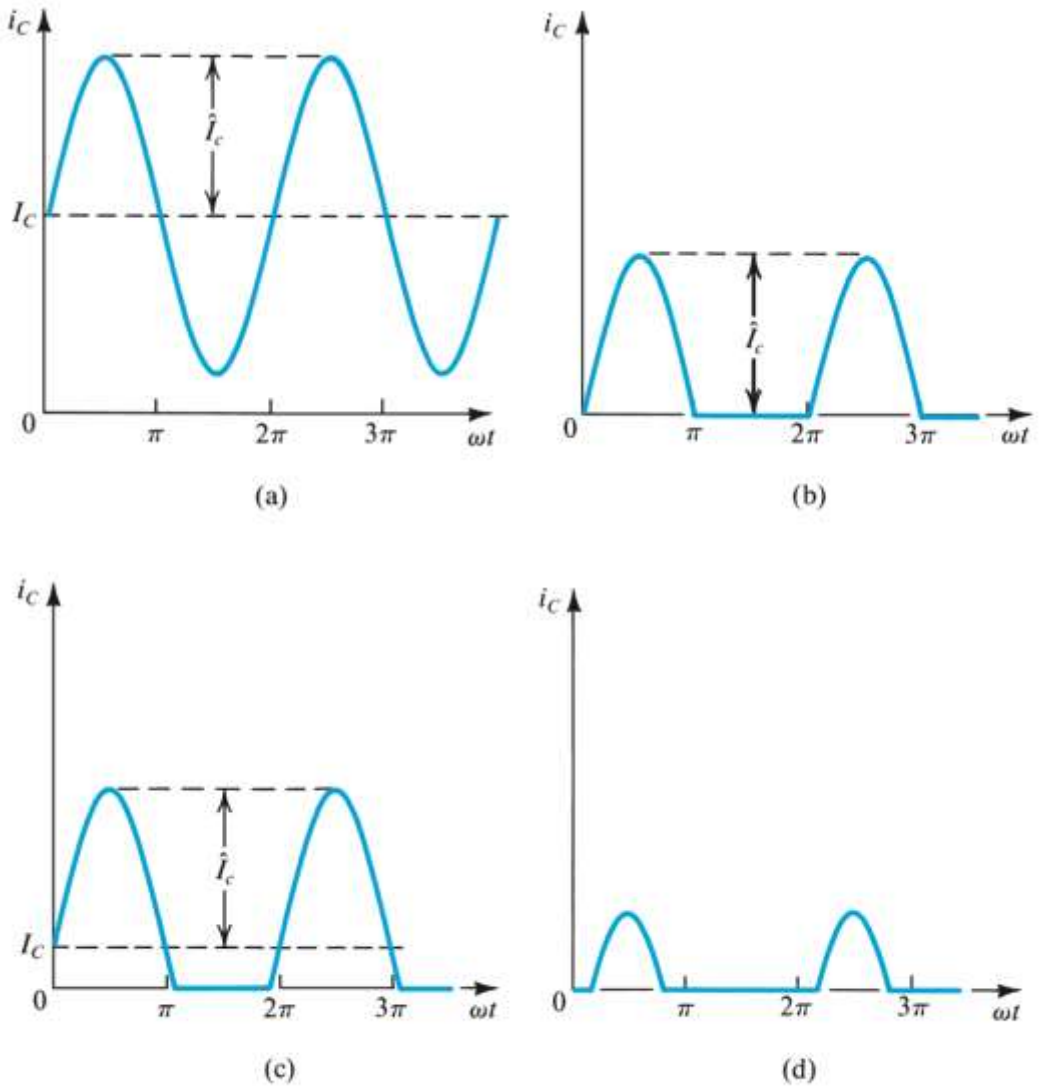
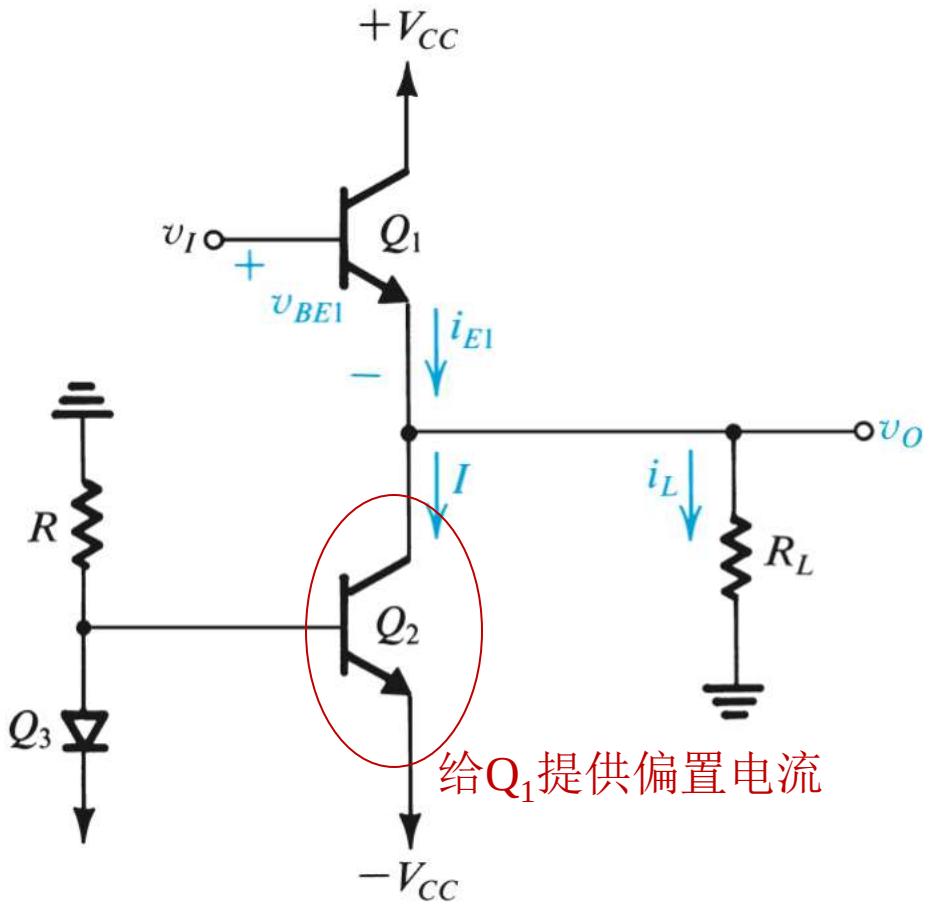


Figure 12.1 Collector-current waveforms for transistors operating in (a) class A, (b) class B, (c) class AB, and (d) class C amplifier stages.

- 根据晶体管的工作时间（导通角）大小来区分
- （a）晶体管的偏置电流 I_C 大于输出信号的幅度 I_c，管子所有时间都导通，导通角=360°，A类功放
- （b）晶体管的偏置电流 $I_C = 0$， 管子一半时间导通，导通角=180°，B类功放
- （c）晶体管的偏置电流 I_C 略大于0，管子导通的时间略多于一般，导通角介于180°和360°之间，AB类功放
- （d）C类，不要求掌握

A类功放

- 典型的A类功放：发射极跟随结构



①为了保证Q_1始终导通，I要大于负载上流过电流的峰值（当i_L是负的峰值时，i_{E1}仍为正）

$$i_{E1}=I+i_L$$

I要足够大，以保证Q_1始终导通

Figure 12.2 An emitter follower (Q_1) biased with a constant current I supplied by transistor Q_2.

A类功放

②分析电路的传输特性　　$v_O = v_I - v_{BE1}$

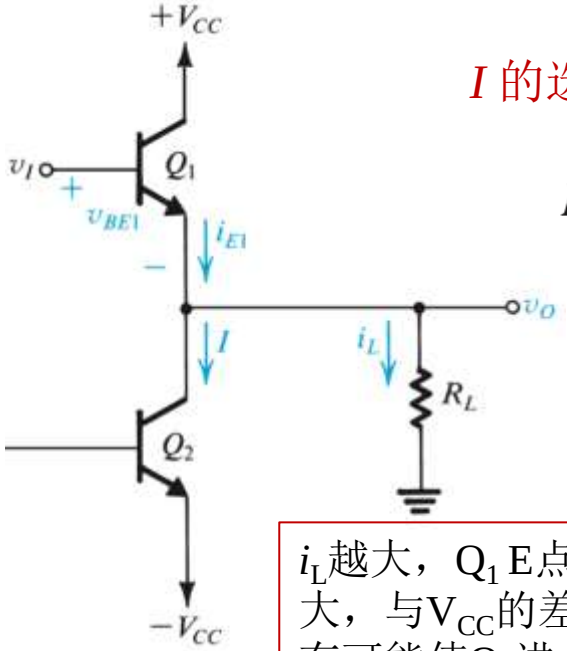
- 输出最大值，i_L达到正峰值时，Q_1到达放大区临界点，V_{CE1sat}为Q_1的饱和压降（放大区和饱和区临界点）

$$v_{Omax} = V_{CC} - V_{CE1sat}$$

- 输出最小值，i_L到达负峰值时，Q_2到达放大区临界点

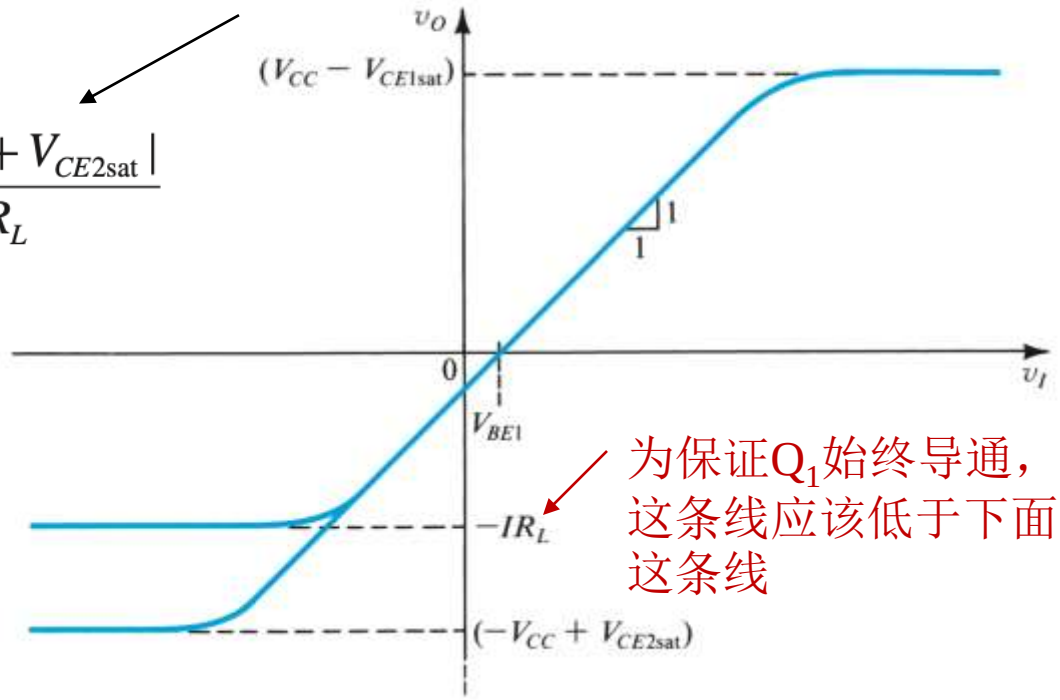
$$v_{Omin} = -V_{CC} + V_{CE2sat}$$

此时，Q_1仍应导通，$|i_L| < I$，$|v_{Omin}| = |- i_{L,peak} R_L| < |-IR_L|$



I 的选择：

$$I \geq \frac{|-V_{CC} + V_{CE2sat}|}{R_L}$$



为保证Q_1始终导通，这条线应该低于下面这条线

i_L越大，Q_1 E点电压越大，与V_{CC}的差越小，有可能使Q_1进入饱和区（V_{CE}=0.3V，V_{CEsat}）

A类功放

③波形分析，忽略Q_1、Q_2的 V_{CEsat}

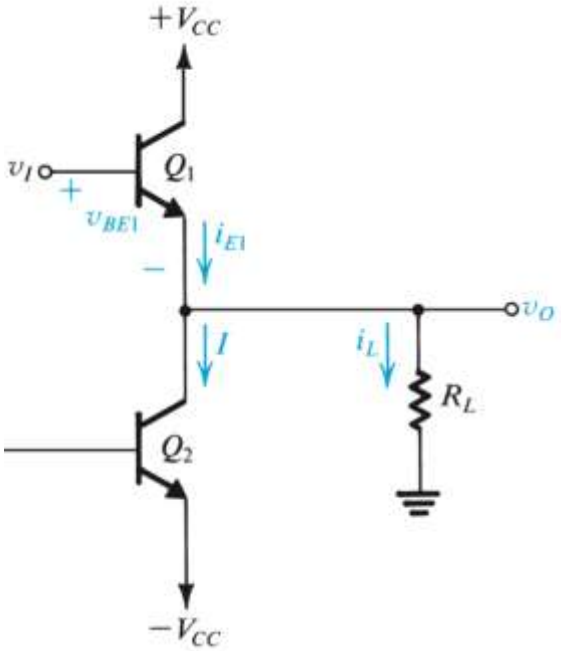
(a) 输出电压可摆幅至 $\pm V_{CC}$；

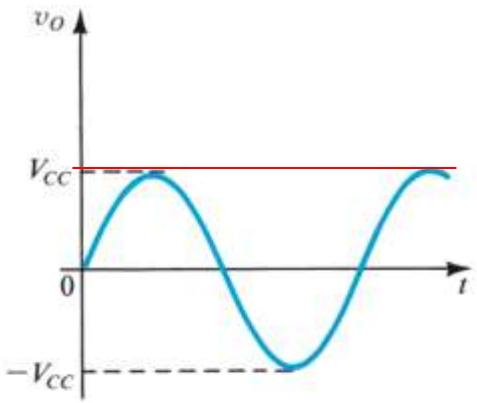
(b) Q_1的$v_{CE1} = V_{CC} - v_O$

(c) 假设偏置电流 I 选择为临界值 $I = V_{CC}/R_L$，则 i_{C1}在 0~2I 之间摆动

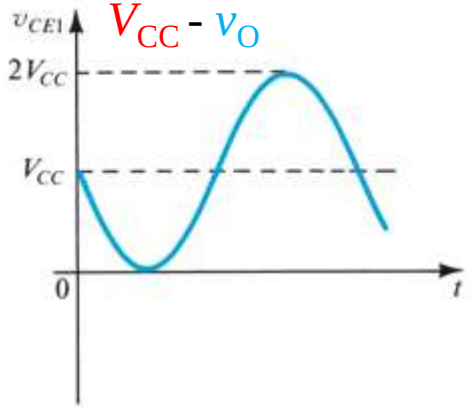
(d) Q_1的瞬时功耗

$$p_{D1} \equiv v_{CE1} i_{C1}$$





(a)



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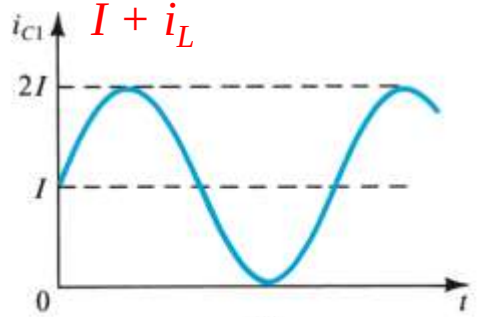

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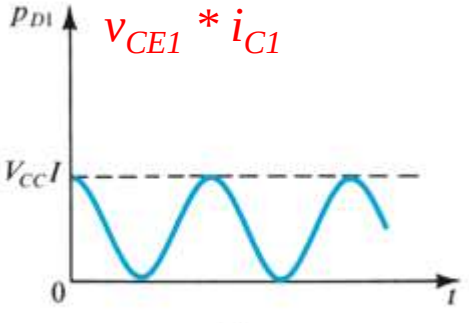
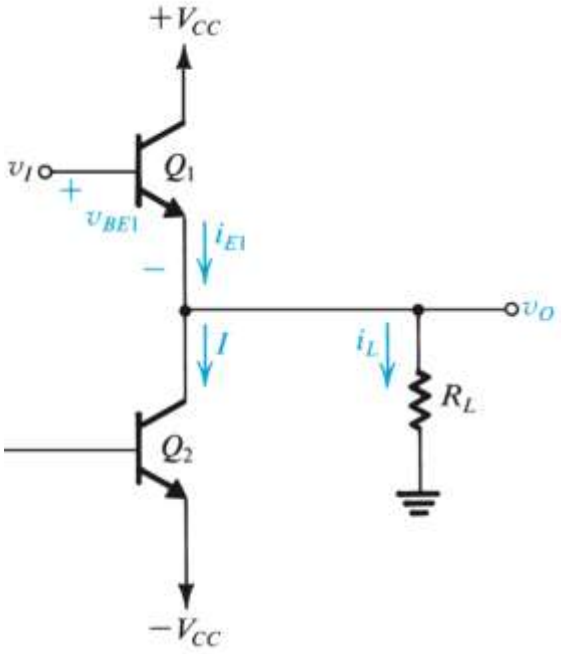


(d)

A类功放

④Q_1功耗的两个特殊情况

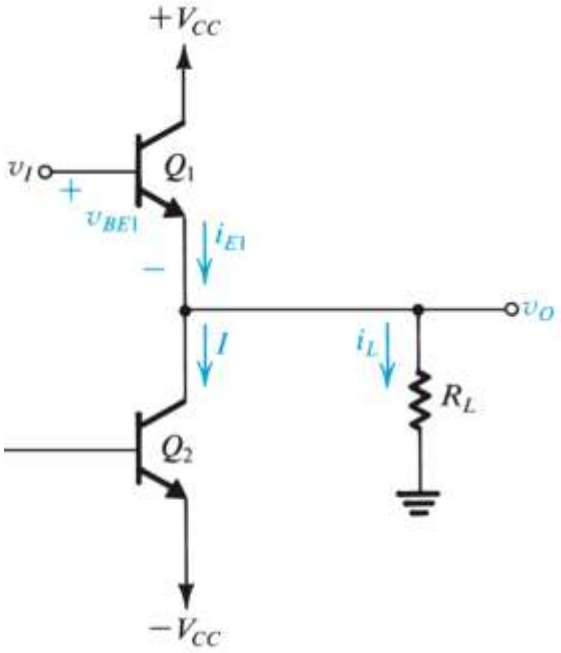
- R_L为开路，$i_{C1}=I$，Q_1的瞬时功耗取决于v_O，v_O为$-V_{CC}$时达到最大$p_{D1}=2V_{CC}I$
- R_L为短路，输入为正时，电流i_L就会无穷大，所以需要短路保护。

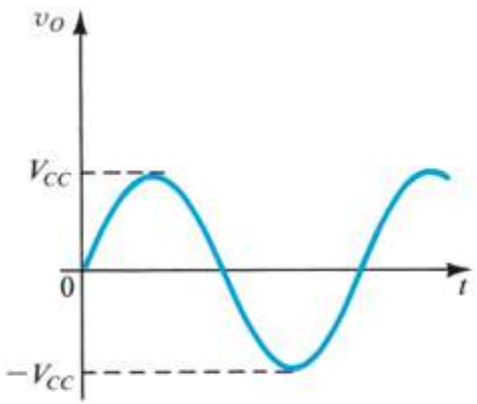


A类功放

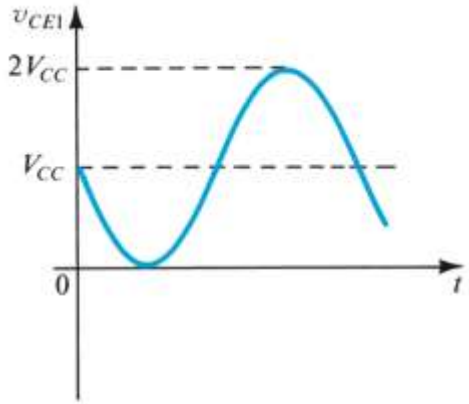
④Q_2的功耗

- 流过的电流始终为 I，v_{C2}从$-V_{CC}$到V_{CC}变化，最大瞬时功耗 $2V_{CC}I$. 平均功耗 $V_{CC}I$.





(a)



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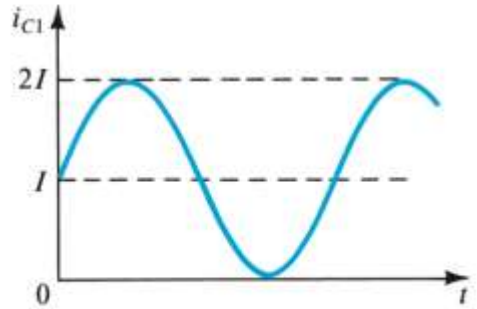
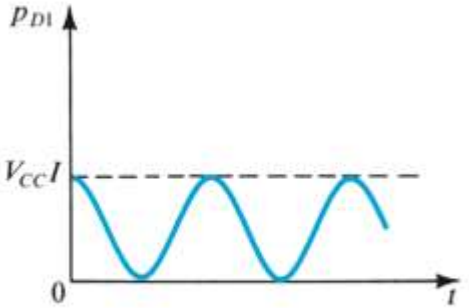


(c)



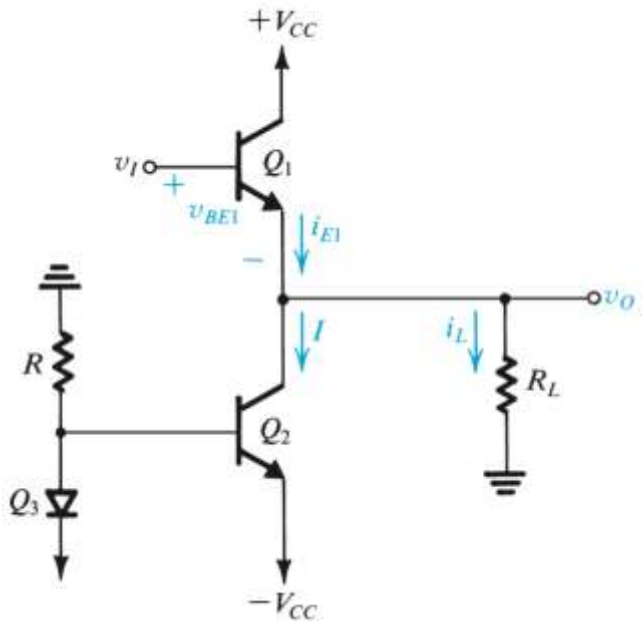
(d)

Example 12.1

Consider the emitter follower in Fig. 12.2 with $V_{CC} = 10\,\text{V}$, $I = 100\,\text{mA}$, and $R_L = 100\,\Omega$.

(a) Find the power dissipated in Q_1 and Q_2 under quiescent conditions $(v_O = 0)$.

(b) For a sinusoidal output voltage of maximum possible amplitude (neglecting V_{CEsat}), find the average power dissipation in Q_1 and Q_2. Also find the load power.

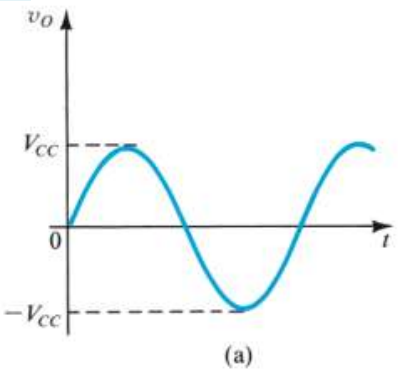


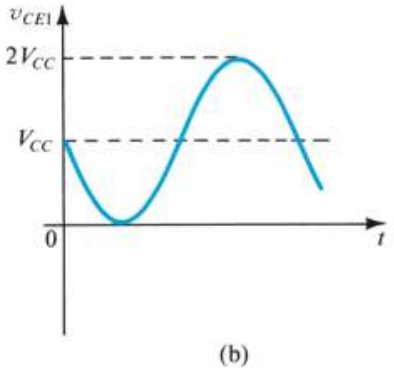
①静态条件时，Q_1、Q_2

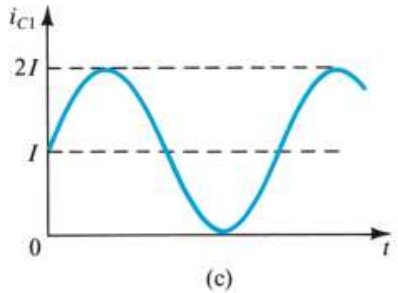
$I = 100\,\text{mA}$

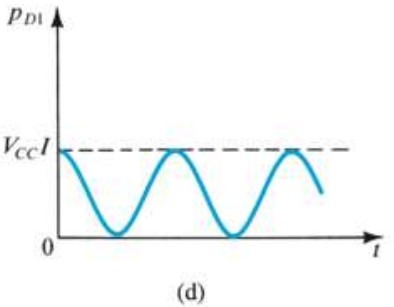
$V_{CE} = V_{CC} = 10\,\text{V}$,

$$P_{D1} = P_{D2} = V_{CC} I = 10 \times 0.1 = 1\,\text{W}$$









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(a) Find the power dissipated in Q_1 and Q_2 under quiescent conditions $(v_O = 0)$.

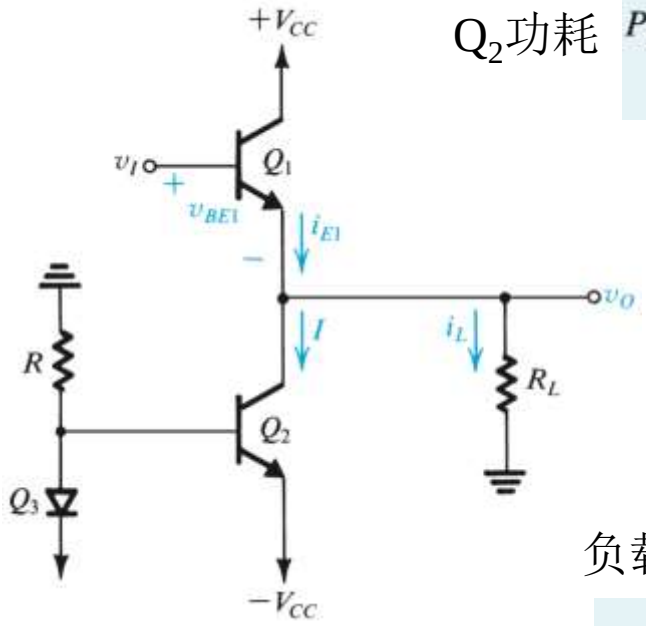
(b) For a sinusoidal output voltage of maximum possible amplitude (neglecting V_{CEsat}), find the average power dissipation in Q_1 and Q_2. Also find the load power.

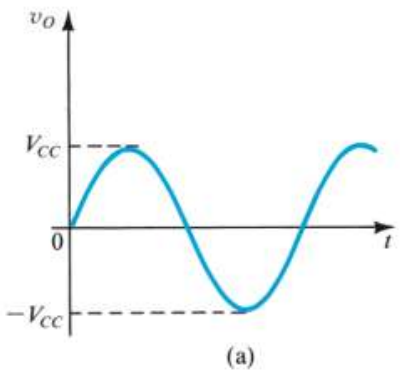
② Q_1功耗，根据图（d）

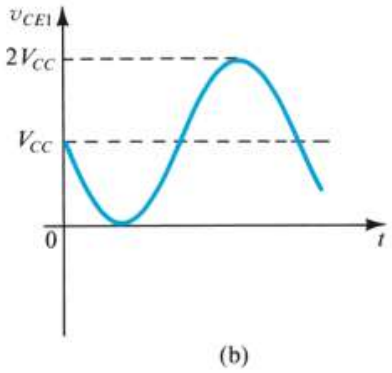
$$P_{D1} = \frac{1}{2}V_{CC}I = \frac{1}{2} \times 10 \times 0.1 = 0.5\,\text{W}$$

Q_2功耗

$$P_{D2} = I \times v_{CE}\big|_{\text{average}}$$
$$= I \times V_{CC} = 0.1 \times 10 = 1\,\text{W}$$

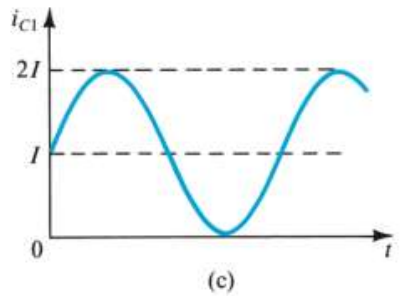


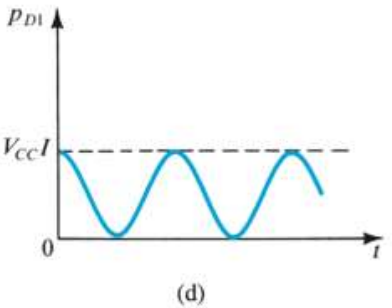




负载功耗

$$P_L = \frac{V_{orms}^2}{R_L}$$
$$= \frac{(10/\sqrt{2})^2}{100} = 0.5\,\text{W}$$





A类功放

④效率。PA效率的定义 $\eta \equiv \dfrac{\text{Load power}(P_L)}{\text{Supply power}(P_S)}$

不考虑V_{CEsat}，输出峰值最大为V_{CC}，且电流I为临界 $I\times R_L=V_{CC}$

输出电压峰值

$$P_L = \frac{(\hat{V}_o/\sqrt{2})^2}{R_L} = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

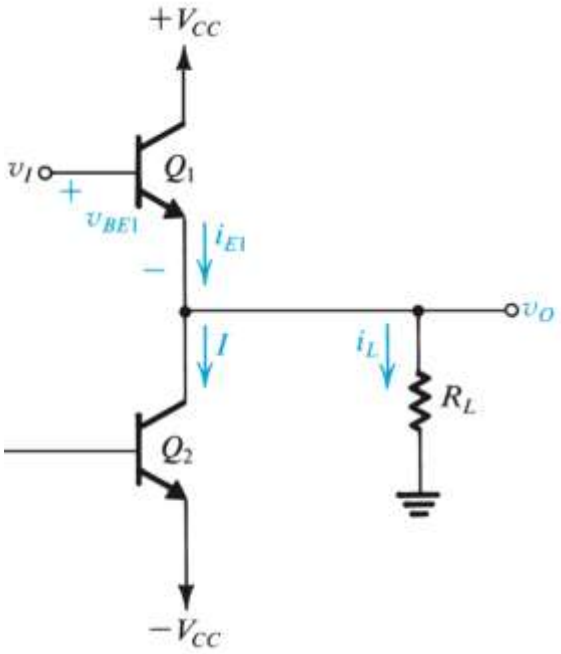
Q_1的平均电流为I，Q_2的电流恒定为I

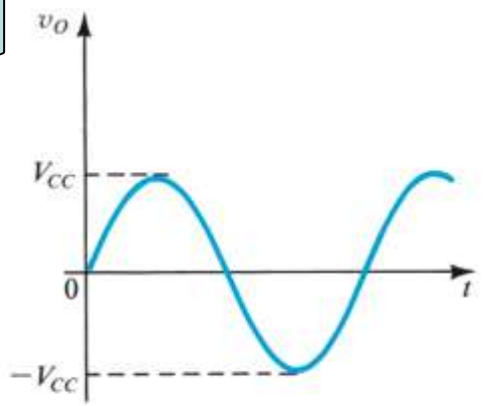
$$P_S = 2V_{CC}I$$

$$\eta = \frac{1}{4}\frac{\hat{V}_o^2}{IR_LV_{CC}} = \frac{1}{4}\left(\frac{\hat{V}_o}{IR_L}\right)\left(\frac{\hat{V}_o}{V_{CC}}\right)$$

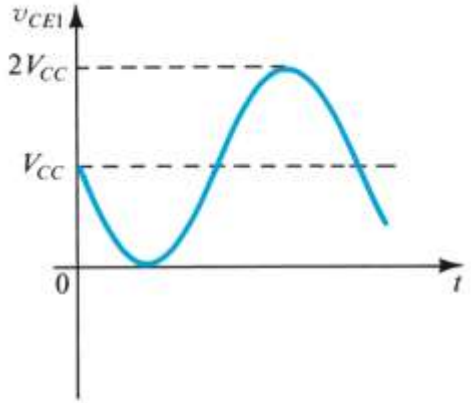
$$\hat{V}_o = V_{CC} = IR_L$$

$$\eta \le 25\%$$

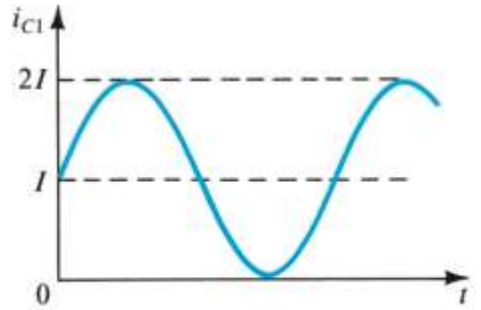




(a)



(b)



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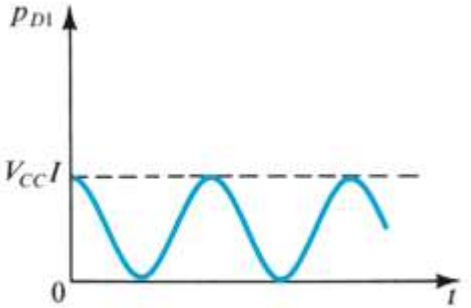


(d)

B类功放

- Q_N、Q_P只有一半的时间导通（导通角180°），且不同时导通
- 若v_I为正时，Q_N开，$v_o = v_I - v_{BE,N}$，Q_P关（$v_B > v_E$，反偏）→ Q_N **Push** 电流到R_L；
- 当v_I为负时，Q_P开，$v_o = v_I + |v_{BE,P}|$，Q_N关（$v_B < v_E$，反偏）→ 从R_L **Pull**电流到Q_P；
- 故称为Push-Pull结构（推挽结构）

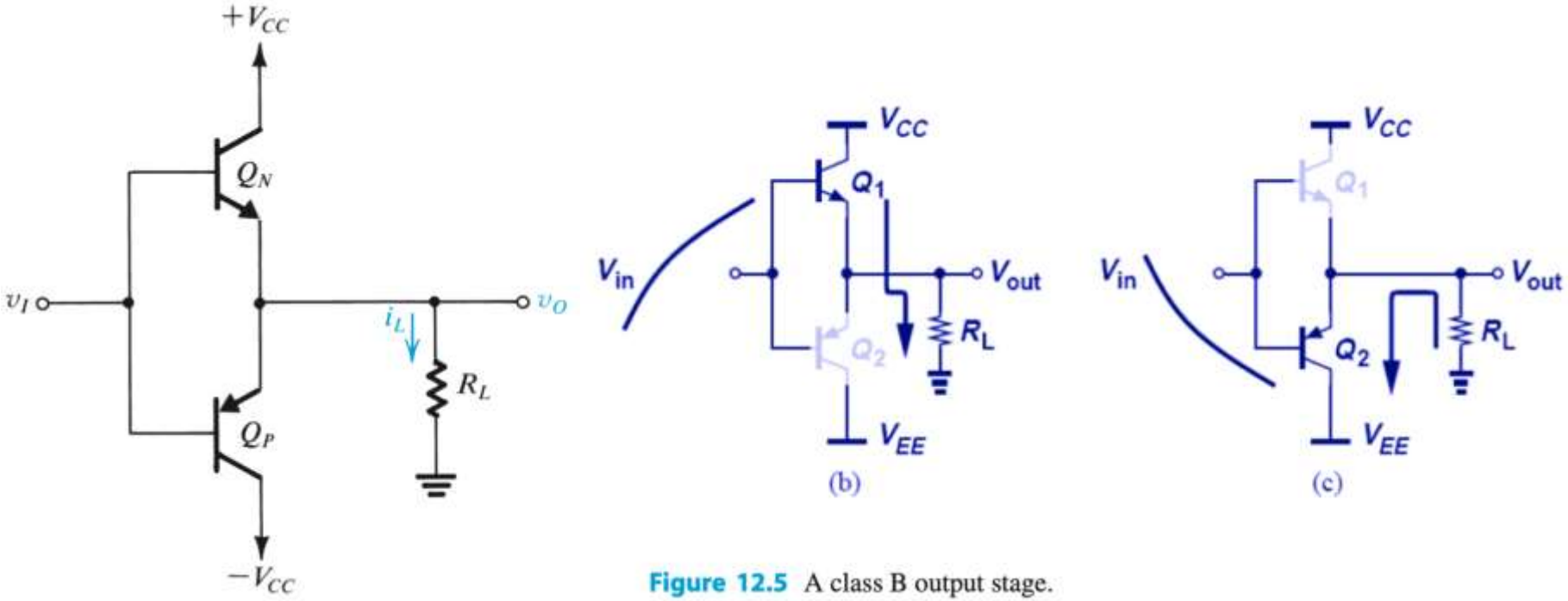
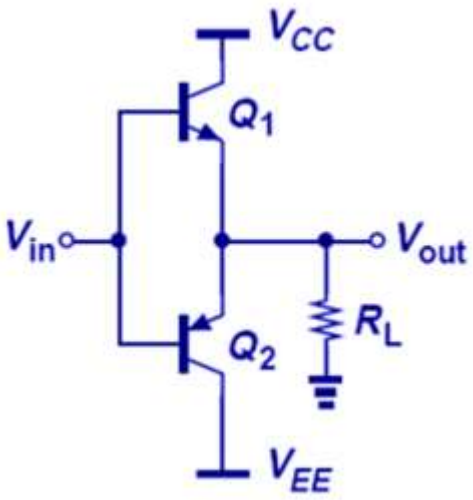
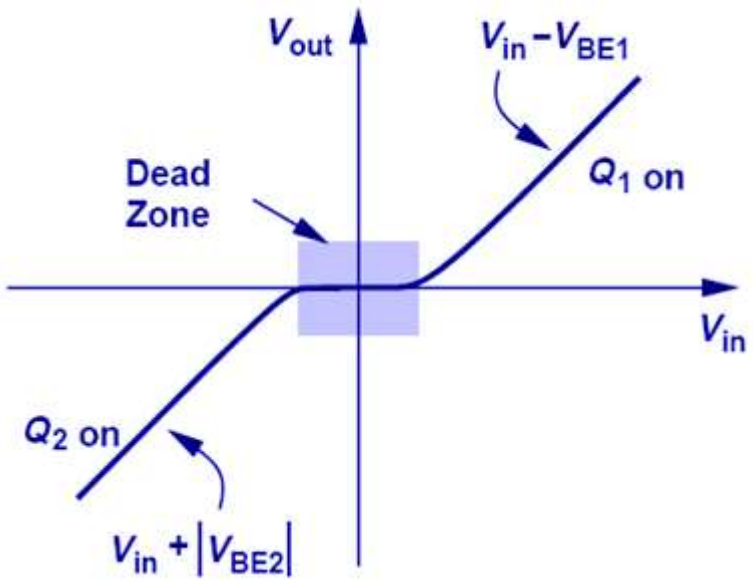


Figure 12.5 A class B output stage.

B类功放

①传输特性





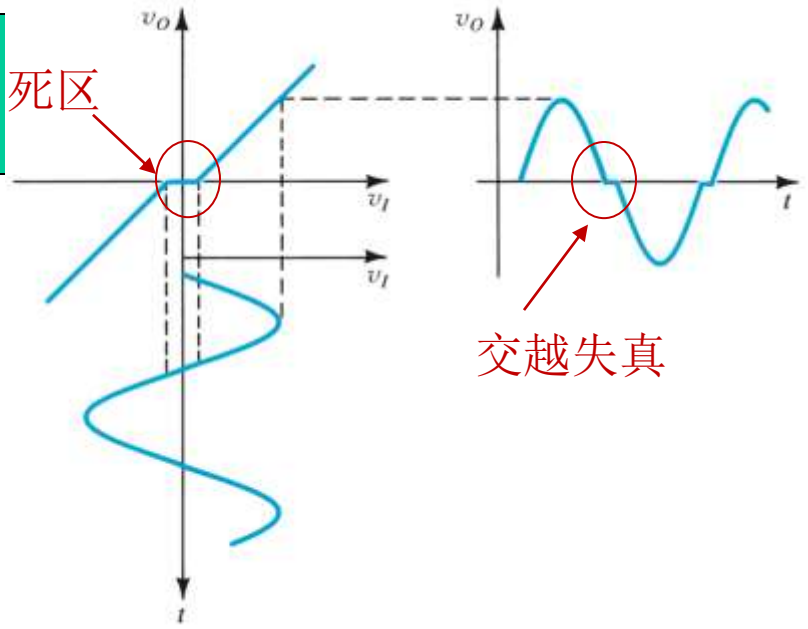
- 当V_{in}接近于零时，存在“死区”（Q_1和Q_2都关闭）→ 非线性；

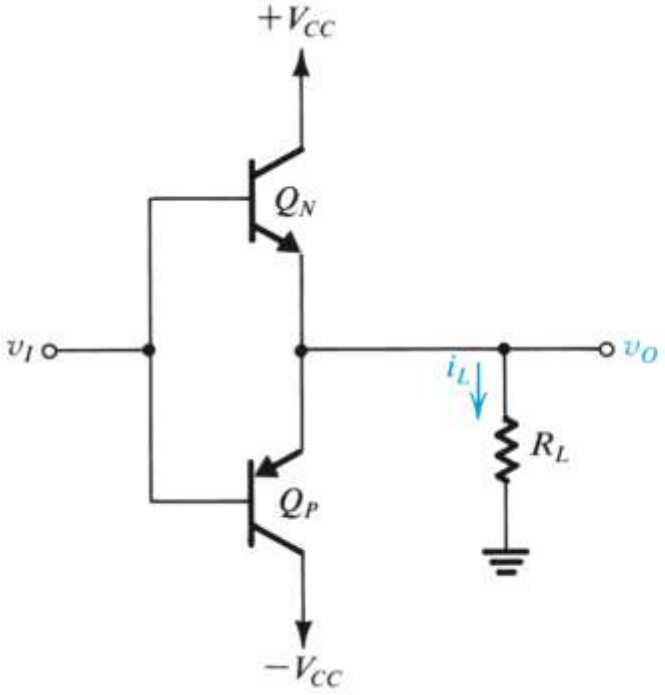
- 观察①：**Q_1和Q_2不可能同时开启**（Q_1开启→$V_{in}>V_{out}$；Q_2开启→$V_{in}<V_{out}$，矛盾）；
- 观察②：**如果$V_{in}=0$，V_{out}必须也为0**（如果$V_{out}>0$，那么流经R_L的电流V_{out}/R_L只能是由Q_1提供，也即Q_1开启→$V_{out}<V_{in}=0$，矛盾；同理V_{out}也不可能小于0）

B类功放

①传输特性

- 输入在0V附近时，两个管子都关闭，该区域称为“死区”，存在“交越失真”（crossover distortion）
- 每个管子的开启时间略小于一半





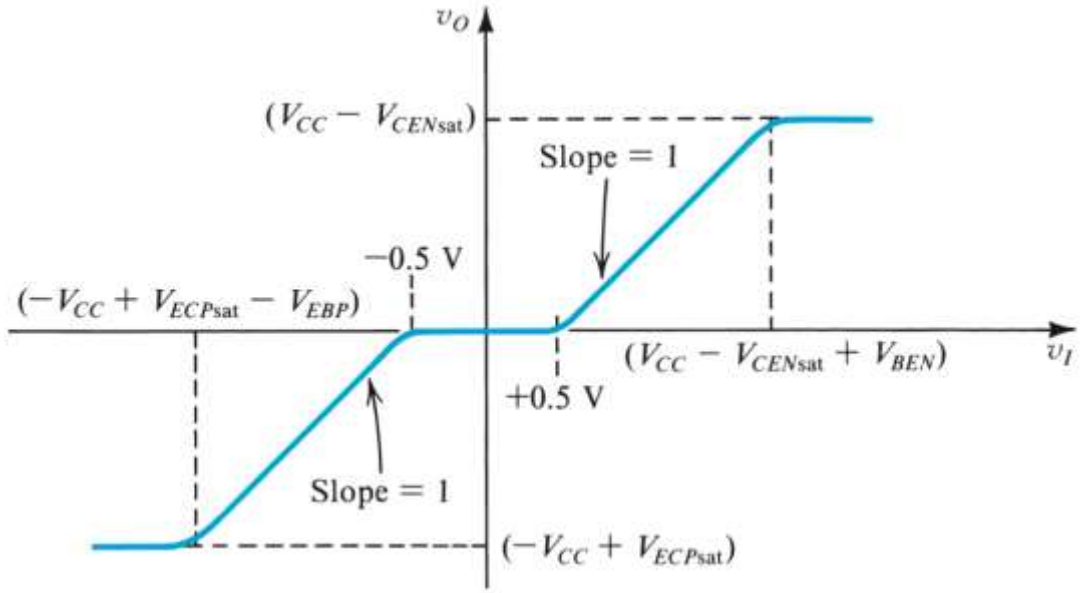


Figure 12.5 A class B output stage.

Crossover Distortion的影响

Did you know?

The ear is quite sensitive to the clipping or crossover distortion produced by followers or push-pull stages. With a sinusoidal input at frequency f_{in}, the output is no longer a pure sinusoid, exhibiting harmonics at $2f_{in}$, $3f_{in}$, etc. One may then say that the ear is sensitive to harmonics. In fact, many audio enthusiasts, especially guitarists, prefer power amplifiers that use vacuum tubes (also called "valves") because these devices have softer clipping characteristics than do transistors.

人耳对“crossover distortion”比较敏感，所以音响发烧友会选择“真空管”功放，真空管功放具有较为平缓的过渡特性

Dorchase DA-803 a Stereo Vacuum Tube Integrated Amplifier,Hybrid Connection,USB/DAC Input, Headphone Output, Pre Output,35Wx2,

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B类功放

②效率，不考虑交越失真，不考虑饱和压降

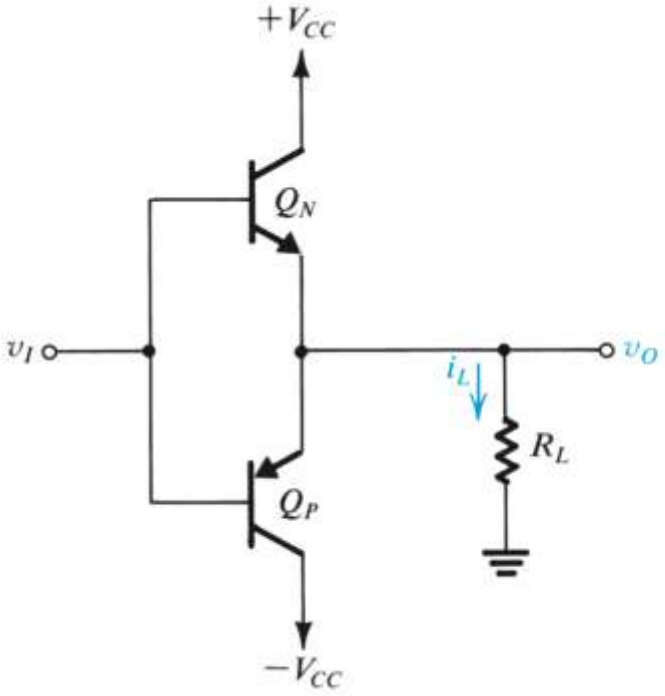
$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

- 考虑正半周，Q_N导通，Q_P关闭，流过Q_N的电流为峰值 $\hat{V}_o/R_L$ 的半个正弦波

  所以，Q_N从$+V_{CC}$抽取的平均电流为 $\dfrac{1}{2\pi}\displaystyle\int_0^{\pi}\frac{\hat{V}_o}{R_L}\sin\theta\,\mathrm{d}\theta = \frac{\hat{V}_o}{\pi R_L}$

$$\int_0^{\pi}\sin(\theta)\,\mathrm{d}\theta = 2$$

- 从单个电源抽取的平均功率 $P_{S+} = P_{S-} = \dfrac{1}{\pi}\dfrac{\hat{V}_o}{R_L}V_{CC}$ **总功率：** $P_S = \dfrac{2}{\pi}\dfrac{\hat{V}_o}{R_L}V_{CC}$



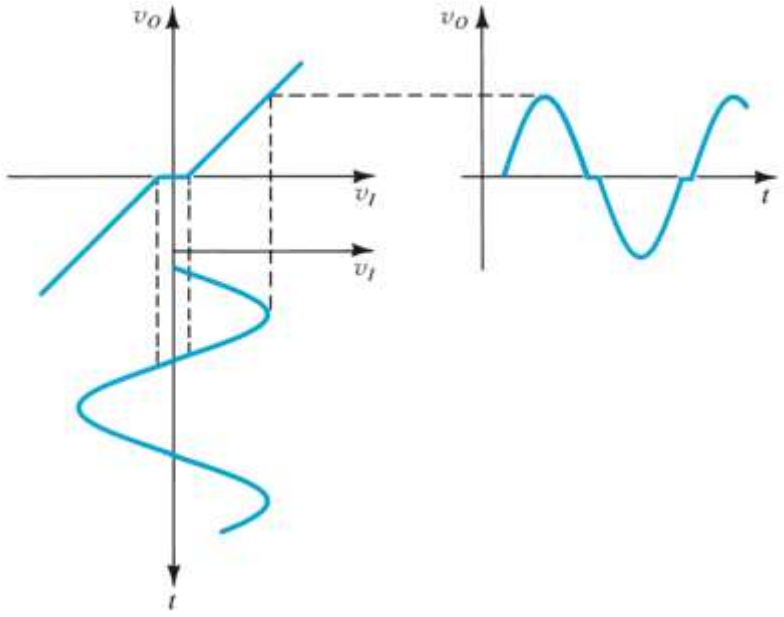


Figure 12.5 A class B output stage.

B类功放

②**效率**，不考虑交越失真，不考虑饱和压降

$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

$$P_S = \frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC}$$

$$\eta = \left(\frac{1}{2}\frac{\hat{V}_o^2}{R_L}\right) \Big/ \left(\frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC}\right) = \frac{\pi}{4}\frac{\hat{V}_o}{V_{CC}}$$

最大效率，输出电压达到最大极限值时

$$\eta_{\max} = \frac{\pi}{4} = 78.5\%$$

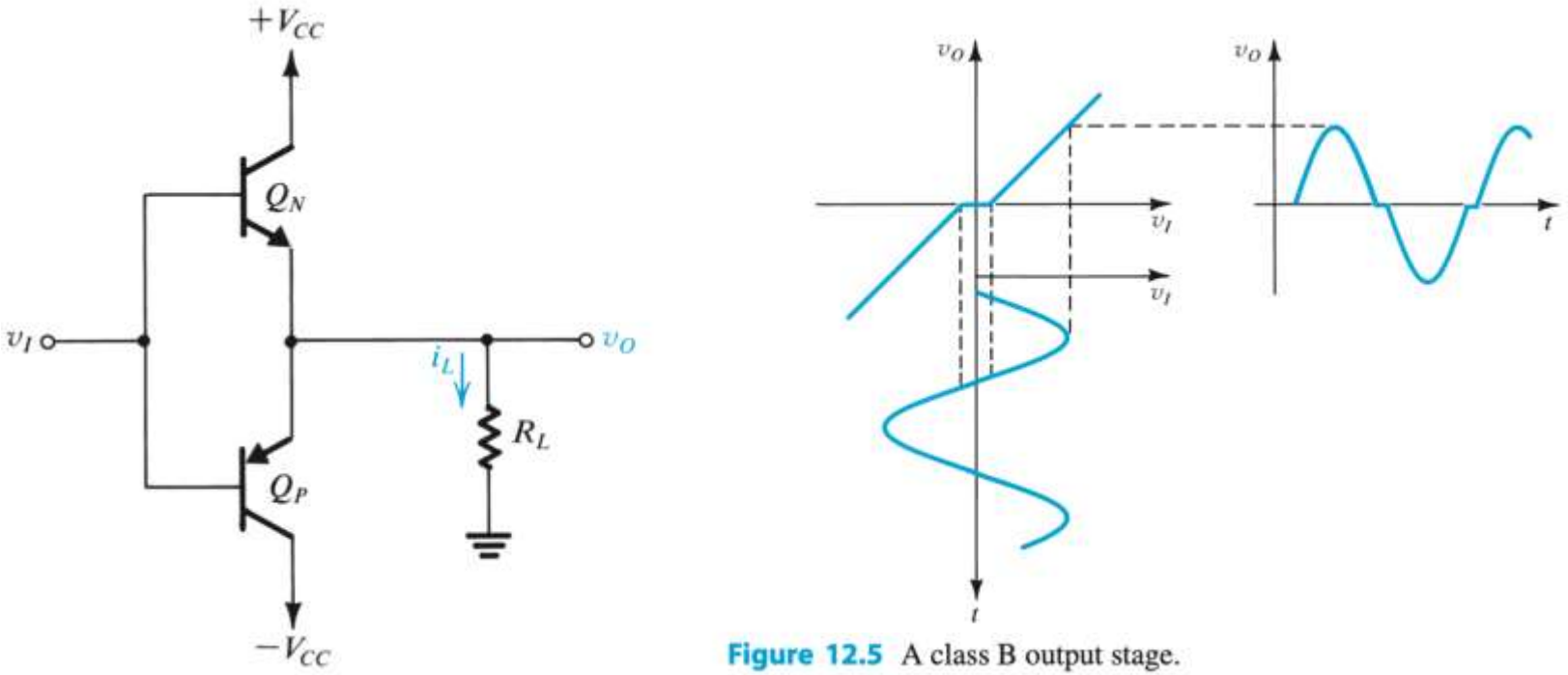


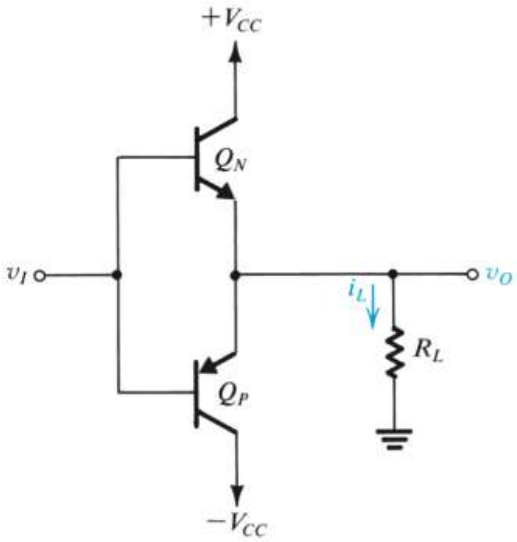
Figure 12.5 A class B output stage.

B类功放

③功耗

$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L} \qquad P_S = \frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC} \qquad \eta = \frac{\pi}{4}\frac{\hat{V}_o}{V_{CC}}$$

- 两个晶体管的总功耗 = 电源功率 — 负载功耗：$P_D = P_S - P_L = \frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC} - \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$
- 单个晶体管的最高功耗：$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L}$



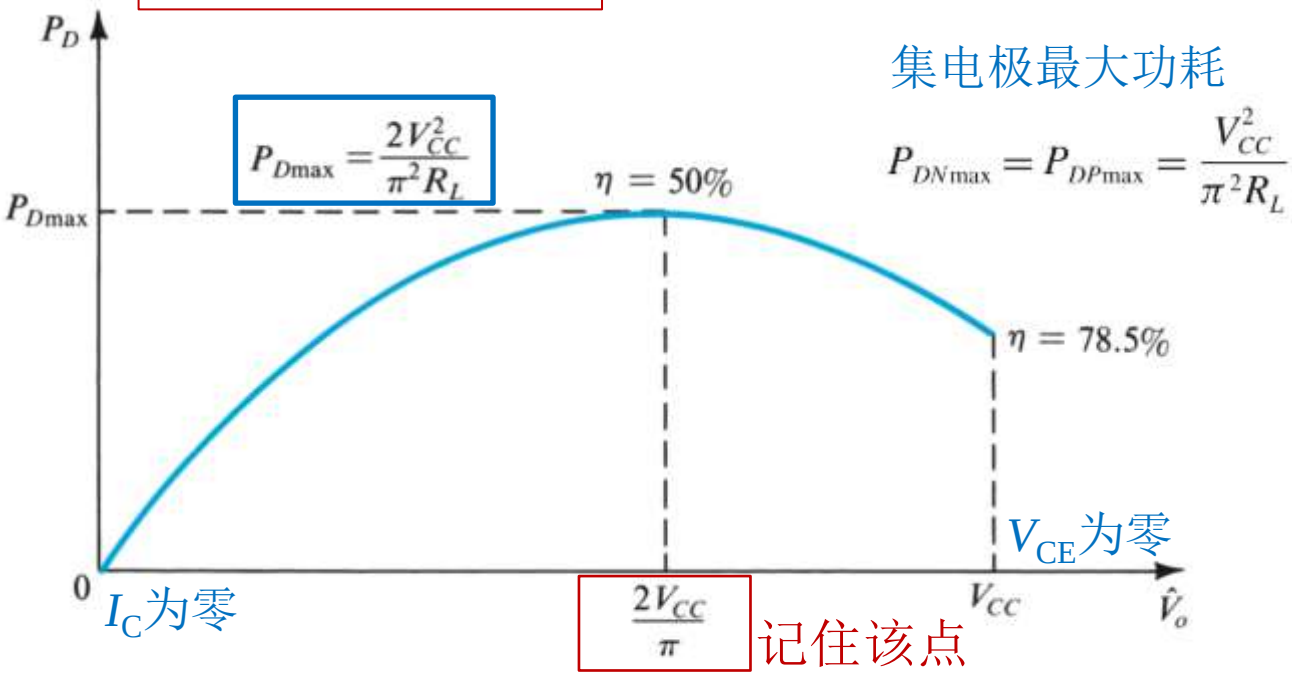


Figure 12.8 Power dissipation of the class B output stage versus amplitude of the output sinusoid.

Figure 12.5 A class B output stage.

B类功放

③最大管压降

输出电压正半周达到峰值($V_{CC} - V_{CES}$)时，
Q_P（关闭着）的V_{CE}经历了最大管压降：$2V_{CC} - V_{CES}$

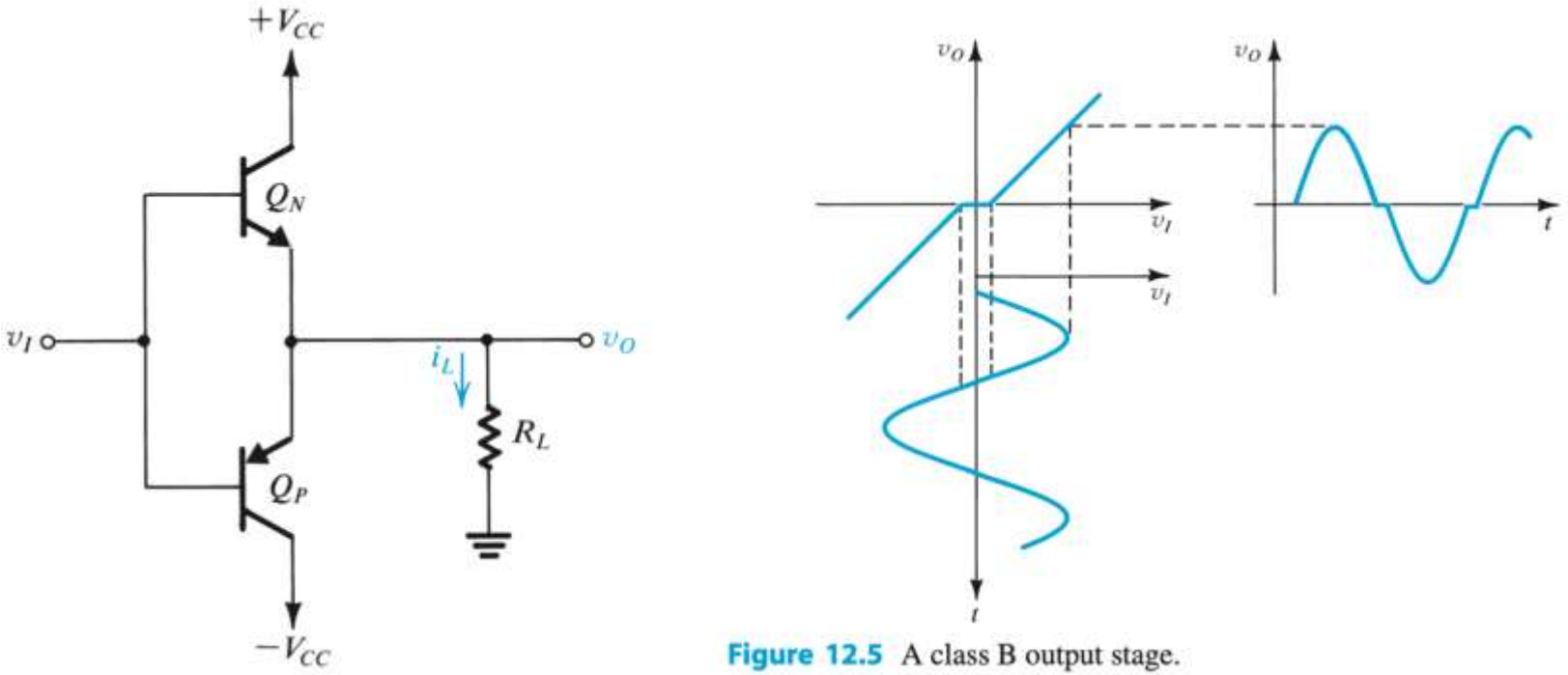
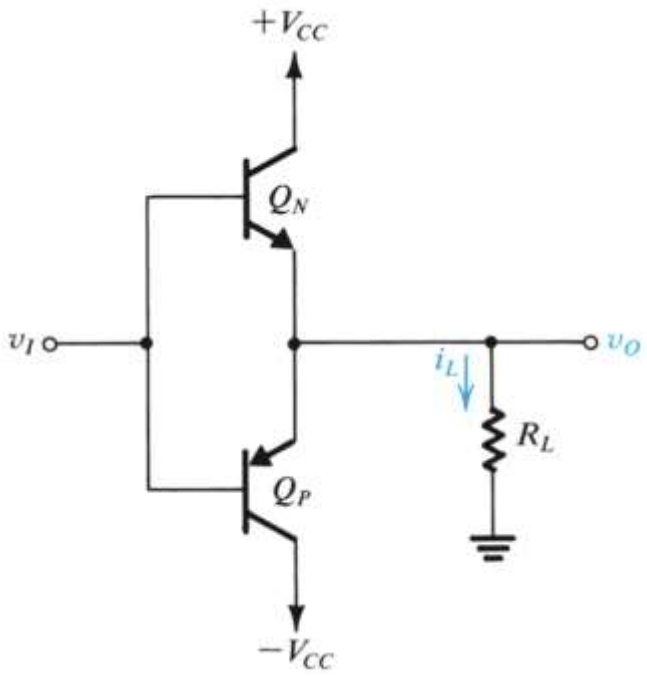


Figure 12.5 A class B output stage.

It is required to design a class B output stage to deliver an average power of 20 W to an 8-Ω load. The power supply is to be selected such that V_{CC} is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion, and allows for including short-circuit protection circuitry. (The latter will be discussed in Section 12.6.) Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power-conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.

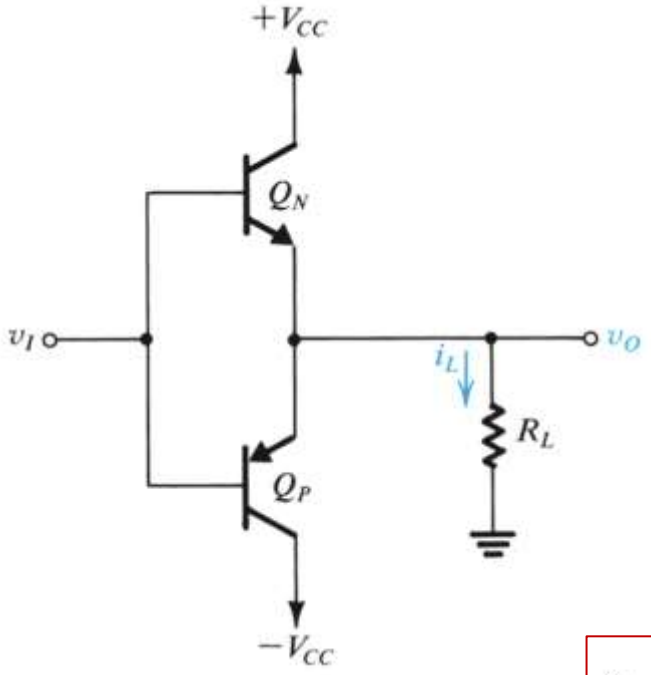


①根据负载功耗和负载电阻，可计算输出电压峰值

$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L} \Rightarrow \hat{V}_o = \sqrt{2P_L R_L} = \sqrt{2 \times 20 \times 8} = 17.9 \text{ V}$$

⇒ Therefore we select $V_{CC} = 23$ V.

It is required to design a class B output stage to deliver an average power of 20 W to an 8-Ω load. The power supply is to be selected such that V_{CC} is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion, and allows for including short-circuit protection circuitry. (The latter will be discussed in Section 12.6.) Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power-conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.



②从电源抽取的峰值电流 $\hat{I}_o = \dfrac{\hat{V}_o}{R_L} = \dfrac{17.9}{8} = 2.24\ \text{A}$

③从电源抽取的平均功耗（半个正弦波电流求平均值）

$$P_{S+} = P_{S-} = \frac{1}{\pi} \times 2.24 \times 23 = 16.4\ \text{W}$$

$$P_{S+} = P_{S-} = \frac{1}{\pi}\frac{\hat{V}_o}{R_L}V_{CC}$$

④效率 $\eta = \dfrac{P_L}{P_S} = \dfrac{20}{32.8} \times 100 = 61\%$

⑤单个晶体管上的最大功耗

$$\hat{V}_o|_{P_{D\max}} = \frac{2}{\pi}V_{CC}$$

$$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L}$$

$$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L} = \frac{(23)^2}{\pi^2 \times 8} = 6.7\ \text{W}$$

B类功放

⑤双电源供电 vs. 单电源供电

称为**OTL**电路
（Output Transformerless）

**传统PA是基于变压器的*

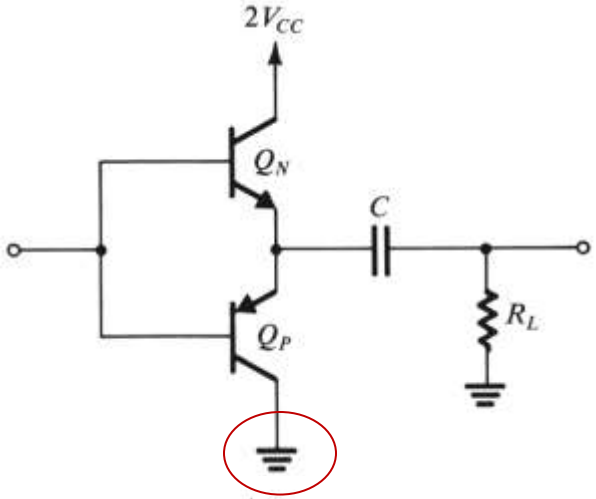


Figure 12.10 Class B output stage operated with a single power supply.

称为**OCL**电路
（Output Capacitorless）

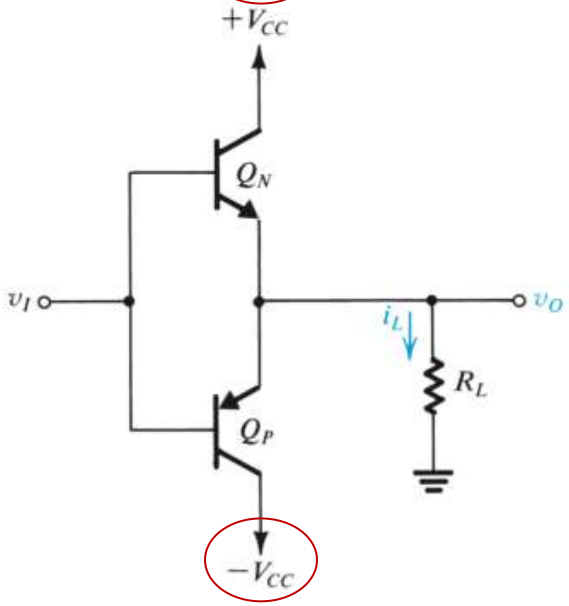


Figure 12.5 A class B output stage.

AB类功放

- **为了解决“交越失真”问题，发展出AB类功放**
- 当输入 = 输出 = 0V 时，$V_{BB}/2$ 提供晶体管的 V_{BE}，两个晶体管都导通工作（导通角略大于180°）

$$i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T}$$

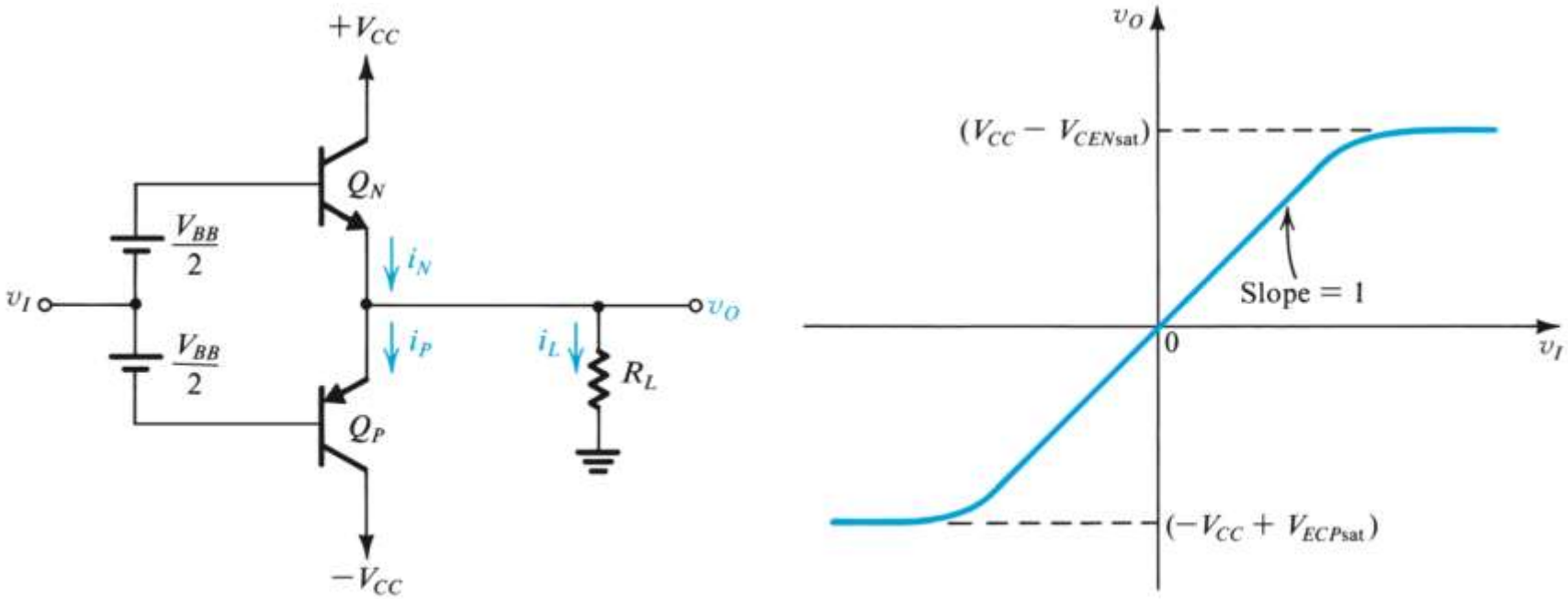


Figure 12.11 Class AB output stage. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P, giving rise to a bias current I_Q given by Eq. (12.23). Thus, for small v_I, both transistors conduct and crossover distortion is almost completely eliminated.

AB类功放

①**传输特性。**当输入电压从0开始增加时，$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN}$

$i_N = i_P + i_L$

- 输出电压增加 → i_L增加 → i_N增加 → v_{BEN}增加，而Q_N和Q_P的v_{BE}之和恒定为V_{BB} → v_{BEP}减小→i_P减小

约束关系2

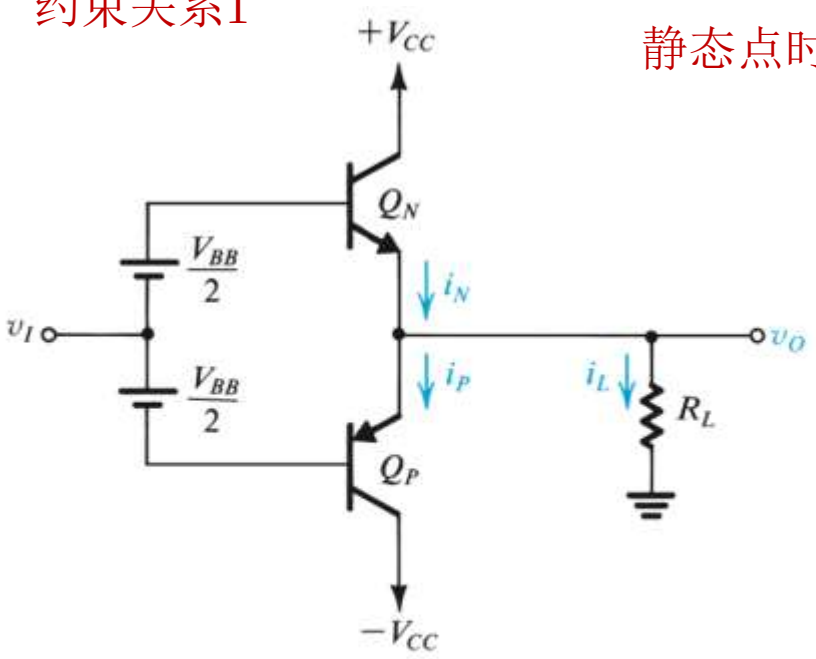
$v_{BEN} + v_{EBP} = V_{BB}$ ⇒ $V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$ ⇒ $i_N i_P = I_Q^2$ → $i_N^2 - i_L i_N - I_Q^2 = 0$

约束关系1

静态点时 $I_Q = I_S e^{V_{BB}/2V_T}$

i_L由i_N驱动， i_P逐渐减小

过渡平缓，解决“死区”



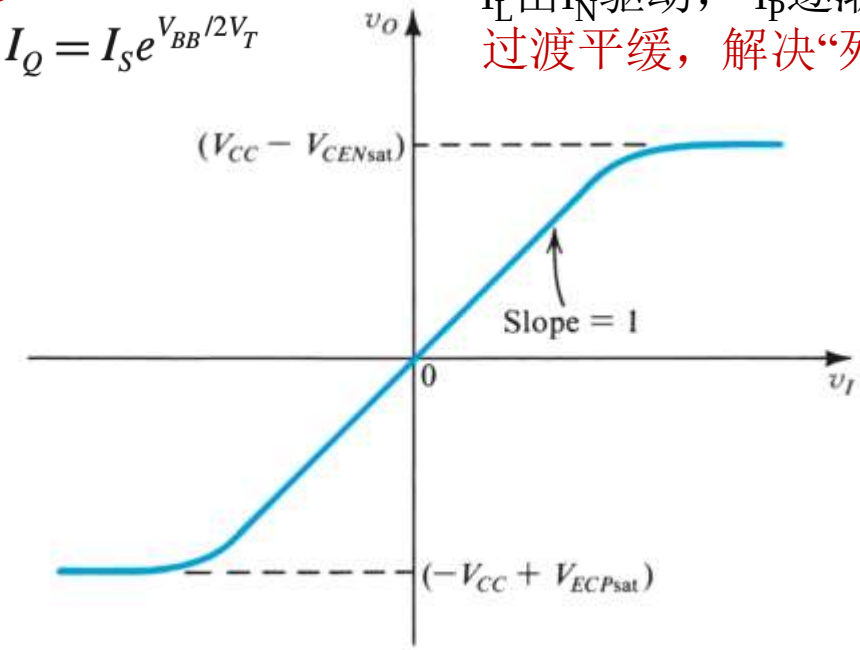
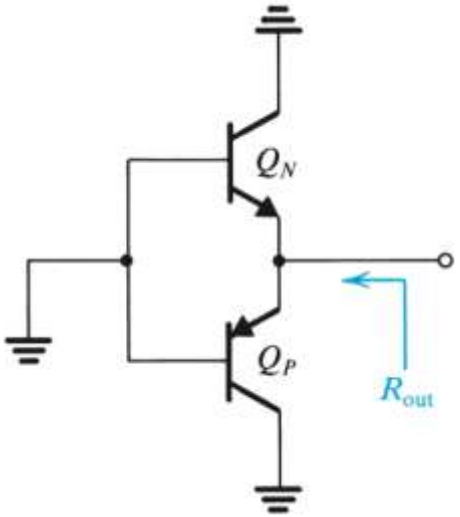


Figure 12.11 Class AB output stage. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P, giving rise to a bias current I_Q given by Eq. (12.23). Thus, for small v_I, both transistors conduct and crossover distortion is almost completely eliminated.

AB类功放

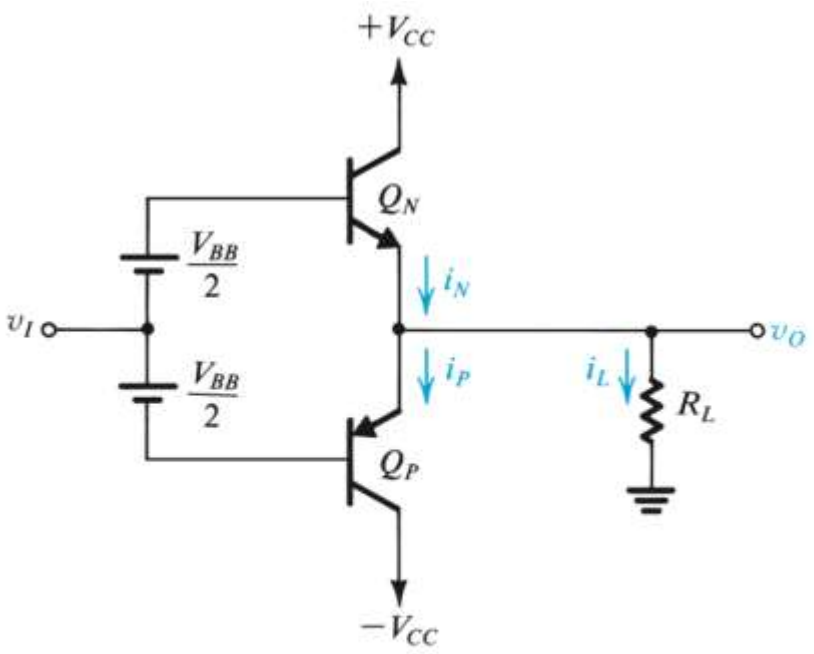
②静态点附近的输出阻抗。

$$R_{\text{out}} = r_{eN} \parallel r_{eP}$$



i_P i_N一增一减 → 静态点附近R_{out}变化平缓→基本上没有交越失真

$$R_{\text{out}} = \frac{V_T}{i_N} \parallel \frac{V_T}{i_P} = \frac{V_T}{i_P + i_N}$$



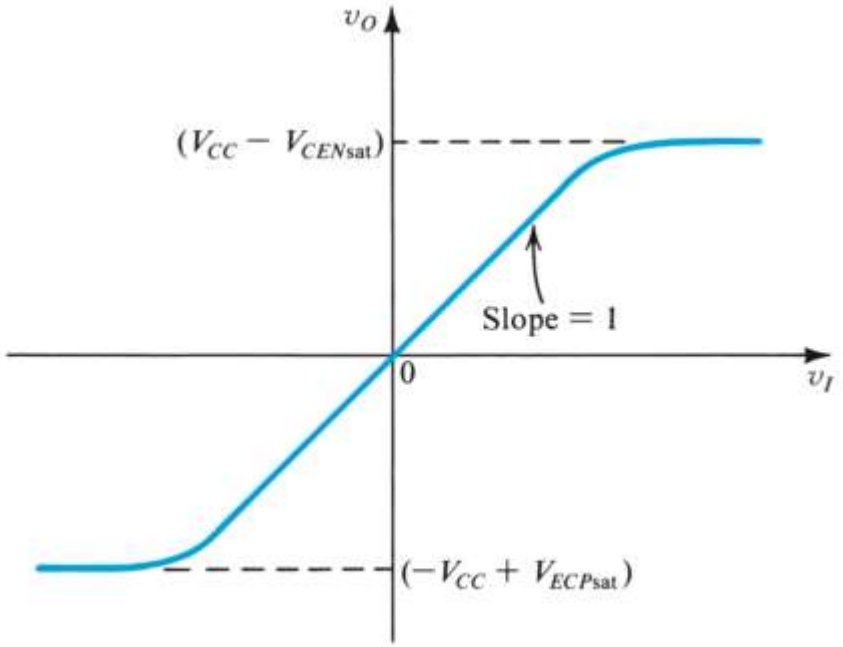


Figure 12.11 Class AB output stage. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P, giving rise to a bias current I_Q given by Eq. (12.23). Thus, for small v_I, both transistors conduct and crossover distortion is almost completely eliminated.

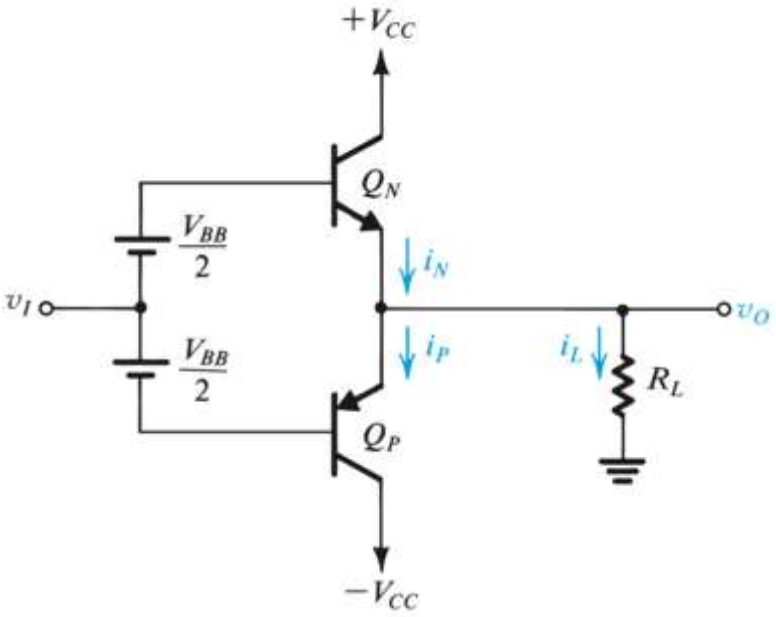
Example 12.3

In this example we explore the details of the transfer characteristic, v_O versus v_I, of the class AB circuit in Fig. 12.11. For this purpose let $V_{CC} = 15$ V, $I_Q = 2$ mA, and $R_L = 100\ \Omega$. Assume that Q_N and Q_P are matched and have $I_S = 10^{-13}$ A. First, determine the required value of the bias voltage V_{BB}. Then, find the transfer characteristic for v_O in the range -10 V to $+10$ V.

①

$$V_{BB} = 2V_T \ln(I_Q/I_S)$$

$$= 2 \times 0.025 \ln\left(2 \times 10^{-3}/10^{-13}\right) = 1.186 \text{ V}$$



②

1. Assume a value for v_O.
2. Determine the load current i_L,

$$i_L = v_O/R_L$$

$$i_N^2 - i_L i_N - I_Q^2 = 0$$

3. Use Eq. (12.27) to determine the current conducted by Q_N, i_N.
4. Determine v_{BEN} from

$$v_{BEN} = V_T \ln(i_N/I_S)$$

5. Determine v_I from

$$v_I = v_O + v_{BEN} - V_{BB}/2$$

In this example we explore the details of the transfer characteristic, v_O versus v_I, of the class AB circuit in Fig. 12.11. For this purpose let $V_{CC} = 15$ V, $I_Q = 2$ mA, and $R_L = 100\ \Omega$. Assume that Q_N and Q_P are matched and have $I_S = 10^{-13}$ A. First, determine the required value of the bias voltage V_{BB}. Then, find the transfer characteristic for v_O in the range −10 V to +10 V.

静态点附近过渡平缓，基本解决了“交越失真”问题

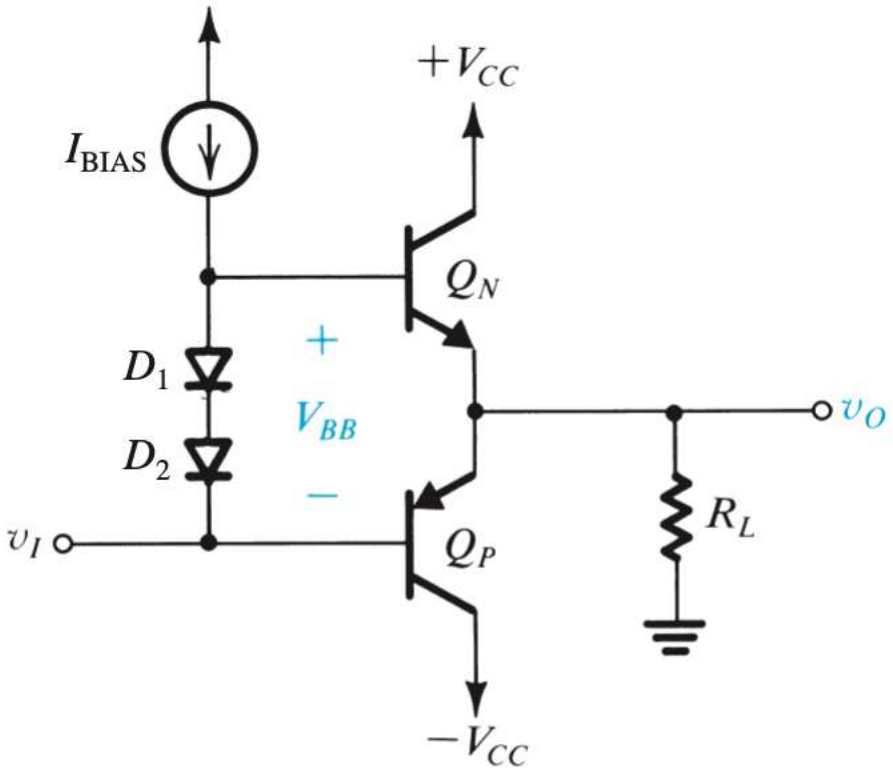
v_O (V)	i_L (mA)	i_N (mA)	i_P (mA)	v_{BEN} (V)	v_{EBP} (V)	v_I (V)	v_O/v_I	R_{out} (Ω)	v_o/v_i
+10.0	100	100.04	0.04	0.691	0.495	10.1	0.99	0.25	1.00
+5.0	50	50.08	0.08	0.673	0.513	5.08	0.98	0.50	1.00
+1.0	10	10.39	0.39	0.634	0.552	1.041	0.96	2.32	0.98
+0.5	5	5.70	0.70	0.619	0.567	0.526	0.95	4.03	0.96
+0.2	2	3.24	1.24	0.605	0.581	0.212	0.94	5.58	0.95
+0.1	1	2.56	1.56	0.599	0.587	0.106	0.94	6.07	0.94
0	0	2	2	0.593	0.593	0	—	6.25	0.94
–0.1	–1	1.56	2.56	0.587	0.599	–0.106	0.94	6.07	0.94
–0.2	–2	1.24	3.24	0.581	0.605	–0.212	0.94	5.58	0.95
–0.5	–5	0.70	5.70	0.567	0.619	–0.526	0.95	4.03	0.96
–1.0	–10	0.39	10.39	0.552	0.634	–1.041	0.96	2.32	0.98
–5.0	–50	0.08	50.08	0.513	0.673	–5.08	0.98	0.50	1.00
–10.0	–100	0.04	100.04	0.495	0.691	–10.1	0.99	0.25	1.00

AB类功放

③偏置方案1

12.5.1 Biasing Using Diodes

用二极管来实现V_{BB}



为了更好地控制二极管V_D和三极管V_{BE}的匹配，二极管可以用diode-connected 结构实现（同样是BJT的话，I_S容易做到一致）

Figure 12.14 A class AB output stage utilizing diodes for biasing. If the junction area of the output devices, Q_N and Q_P, is n times that of the biasing devices D_1 and D_2, a quiescent current $I_Q = nI_{BIAS}$ flows in the output devices.

Example 12.4

Consider the class AB output stage under the conditions that $V_{CC} = 15\ \text{V}, R_L = 100\ \Omega$, and the output is sinusoidal with a maximum amplitude of 10 V. Let Q_N and Q_P be matched with $I_S = 10^{-13}$ A and $\beta = 50$. Assume that the biasing diodes have one-third the junction area of the output devices. Find the value of I_{BIAS} that guarantees a minimum of 1 mA through the diodes at all times. Determine the quiescent current and the quiescent power dissipation in the output transistors (i.e., at $v_O = 0$). Also find V_{BB} for $v_O = 0$, +10 V, and −10 V.

静态时，Q_NQ_P基极电流约为0，二极管电流为I_{BIAS}

工作时，Q_N基极电流设为I_B，二极管电流为$I_{BIAS} - I_B$，该值需大于1mA

Solution

①流过管子的最大电流→最大i_B

The maximum current through Q_N is approximately equal to $i_{Lmax} = 10\ \text{V}/0.1\ \text{k}\Omega = 100\ \text{mA}$. Thus the maximum base current in Q_N is approximately 2 mA. To maintain a minimum of 1 mA through the diodes, we select $I_{BIAS} = 3\ \text{mA}$. The area ratio of 3 yields a quiescent current of 9 mA through Q_N and Q_P. The quiescent power dissipation is

②求出二极管偏置电流的最小值

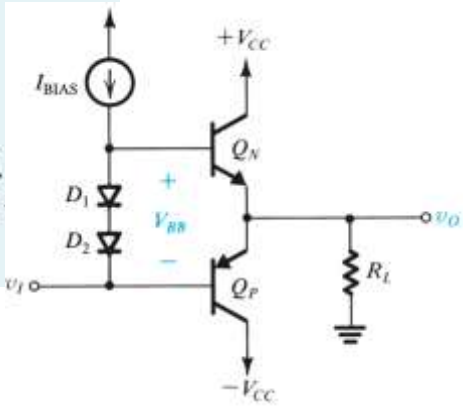
③静态时流过Q_NQ_P的电流很小，i_B很小，3mA全部流到二极管

$$P_{DQ} = 2 \times 15 \times 9 = 270\ \text{mW}$$

For $v_O = 0$, the base current of Q_N is $9/51 \simeq 0.18$ mA, leaving a current of $3 - 0.18 = 2.82$ mA to flow through the diodes. Since the diodes have $I_S = \frac{1}{3} \times 10^{-13}$ A, the voltage V_{BB} will be

$$V_{BB} = 2V_T \ln\left(\frac{2.82\ \text{mA}}{I_S}\right) = 1.26\ \text{V}$$

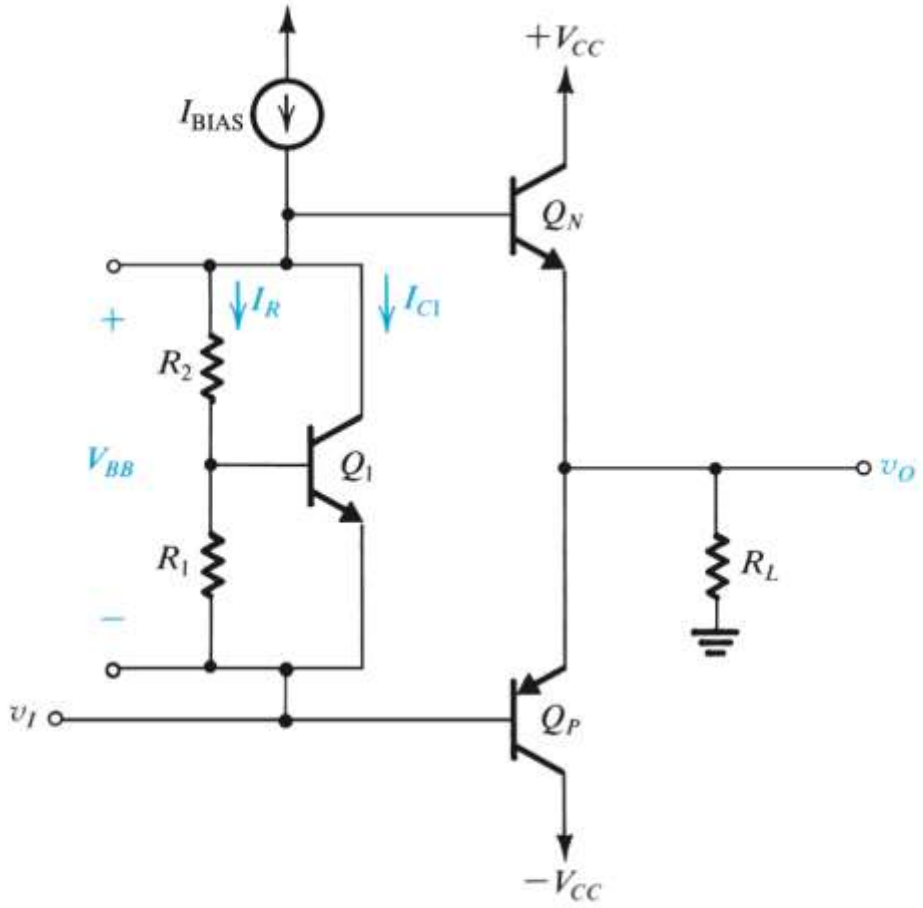
At $v_O = +10$ V, the current through the diodes will decrease to 1 mA, resulting in $V_{BB} \simeq 1.21$ V. At the other extreme of $v_O = -10$ V, Q_N will be conducting a very small current; thus its base current is negligibly small and all of I_{BIAS} (3 mA) flows through the diodes, resulting in $V_{BB} \simeq 1.26$ V.



AB类功放

③偏置方案2

12.5.2 Biasing Using the V_{BE} Multiplier



忽略Q_1的基极电流

$$I_R = \frac{V_{BE1}}{R_1}$$

$$\Rightarrow V_{BB} = I_R(R_1 + R_2)$$

$$= V_{BE1}\left(1 + \frac{R_2}{R_1}\right)$$

忽略Q_N的基极电流

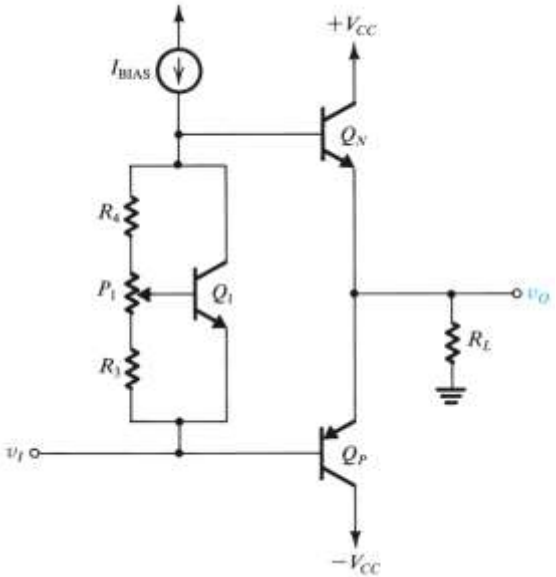
$$I_{C1} = I_{\text{BIAS}} - I_R$$

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}}$$

Figure 12.15 A class AB output stage utilizing a V_{BE} multiplier for biasing.

Example 12.5

It is required to redesign the output stage of Example 12.4 utilizing a V_{BE} multiplier for biasing. Use a small-geometry transistor for Q_1 with $I_S = 10^{-14}$ A and design for a quiescent current $I_Q = 2$ mA.



①Q_N峰值电流100 mA → Q_N 基极电流最大2 mA，要保证multiplier始终能有至少1mA的电流 → 选择 $I_{BIAS} = 3$ mA

②在静态条件下（输出0V，管子接近关闭区域）， Q_N 电流很小，其基极电流可忽略，3mA全部流入multiplier

③$I_R + I_{C1}$ 最大3mA，最小1mA，选择I_R为0.5mA

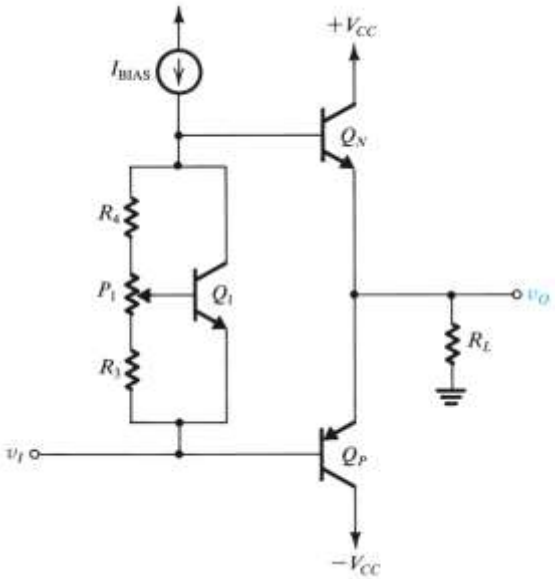
④Q_N静态电流2 mA ⇨ $V_{BB} = 2V_T \ln \dfrac{2 \times 10^{-3}}{10^{-13}} = 1.19$ V

Example 12.4

Consider the class AB output stage under the conditions that $V_{CC} = 15$ V, $R_L = 100\ \Omega$, and the output is sinusoidal with a maximum amplitude of 10 V. Let Q_N and Q_P be matched with $I_S = 10^{-13}$ A and $\beta = 50$. Assume that the biasing diodes have one-third the junction area of the output devices. Find the value of I_{BIAS} that guarantees a minimum of 1 mA through the diodes at all times. Determine the quiescent current and the quiescent power dissipation in the output transistors (i.e., at $v_O = 0$). Also find V_{BB} for $v_O = 0$, +10 V, and −10 V.

Example 12.5

It is required to redesign the output stage of Example 12.4 utilizing a V_{BE} multiplier for biasing. Use a small-geometry transistor for Q_1 with $I_S = 10^{-14}$ A and design for a quiescent current $I_Q = 2$ mA.



③选择I_R为0.5mA

④Q_N静态电流2 mA ⇨ $V_{BB} = 2V_T \ln \dfrac{2 \times 10^{-3}}{10^{-13}} = 1.19\ \text{V}$

We can now determine $R_1 + R_2$ as follows:

$$R_1 + R_2 = \frac{V_{BB}}{I_R} = \frac{1.19}{0.5} = 2.38\ \text{k}\Omega$$

At a collector current of 2.5 mA, Q_1 has

$$V_{BE1} = V_T \ln \frac{2.5 \times 10^{-3}}{10^{-14}} = 0.66\ \text{V}$$

Example 12.4

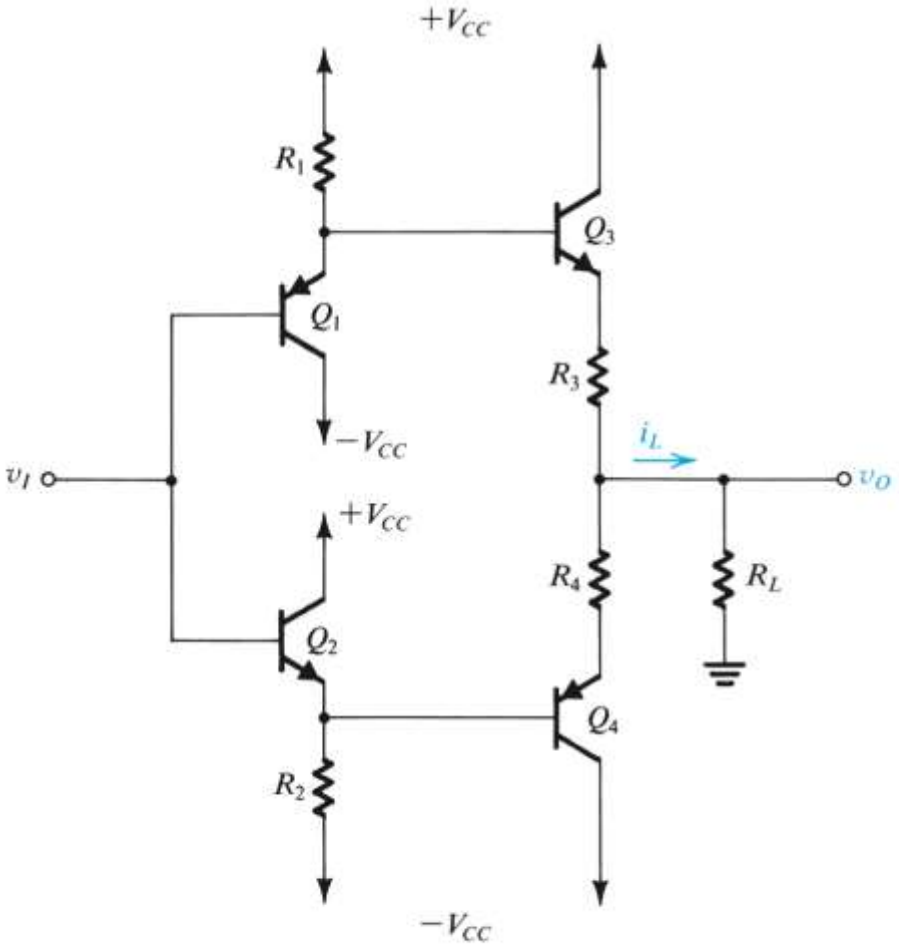
⇨ $R_1 = \dfrac{0.66}{0.5} = 1.32\ \text{k}\Omega$ $\quad R_2 = 2.38 - 1.32 = 1.06\ \text{k}\Omega$

Consider the class AB output stage under the conditions that $V_{CC} = 15$ V, $R_L = 100\ \Omega$, and the output is sinusoidal with a maximum amplitude of 10 V. Let Q_N and Q_P be matched with $I_S = 10^{-13}$ A and $\beta = 50$. Assume that the biasing diodes have one-third the junction area of the output devices. Find the value of I_{BIAS} that guarantees a minimum of 1 mA through the diodes at all times. Determine the quiescent current and the quiescent power dissipation in the output transistors (i.e., at $v_O = 0$). Also find V_{BB} for $v_O = 0$, +10 V, and −10 V.

AB类功放

④改进结构

12.6.1 Use of Input Emitter Followers



前面加一级发射极跟随结构

① 提供V_{BB}

② 增加输入阻抗

Figure 12.17 A class AB output stage with an input buffer. In addition to providing a high input resistance, the buffer transistors Q_1 and Q_2 bias the output transistors Q_3 and Q_4.

AB类功放

④改进结构

12.6.2 Use of Compound Devices

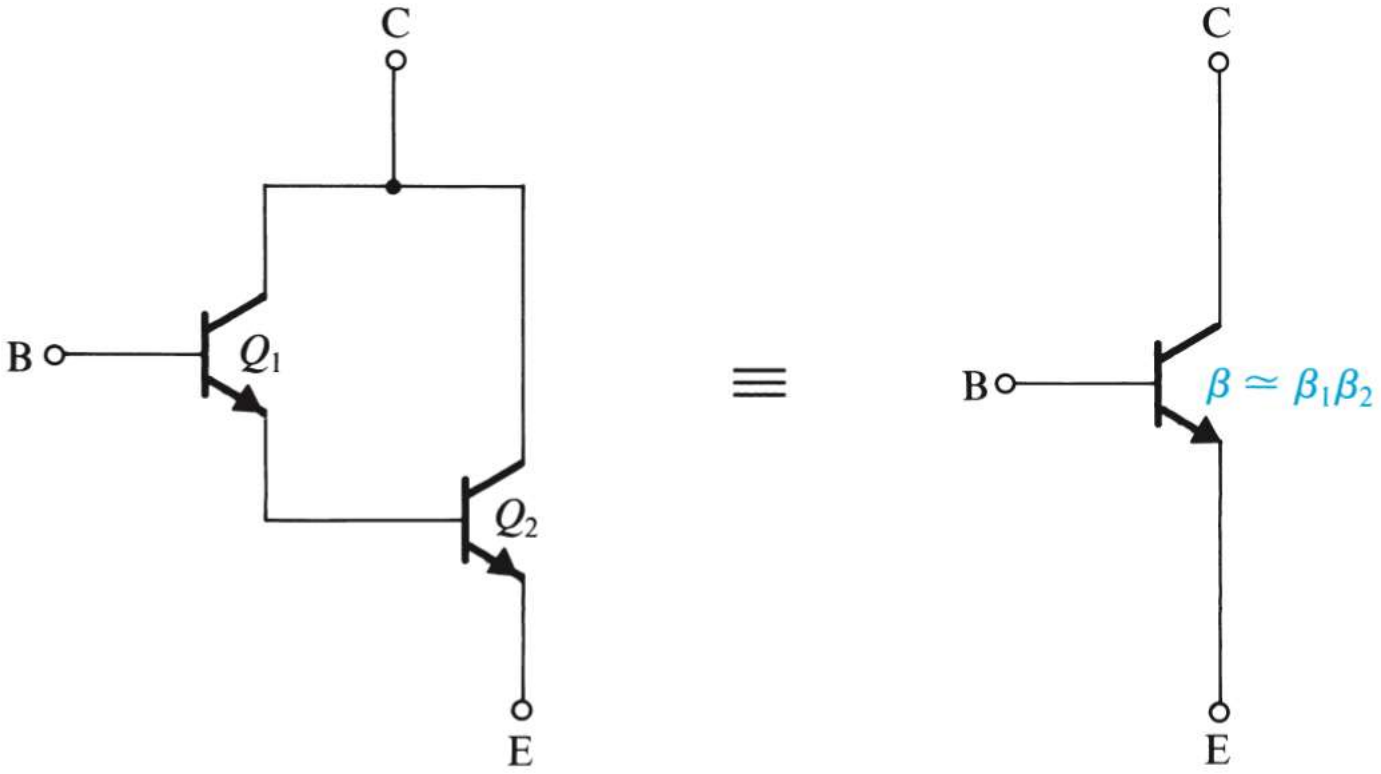


Figure 12.18 The Darlington configuration.

AB类功放

④改进结构

12.6.2 Use of Compound Devices

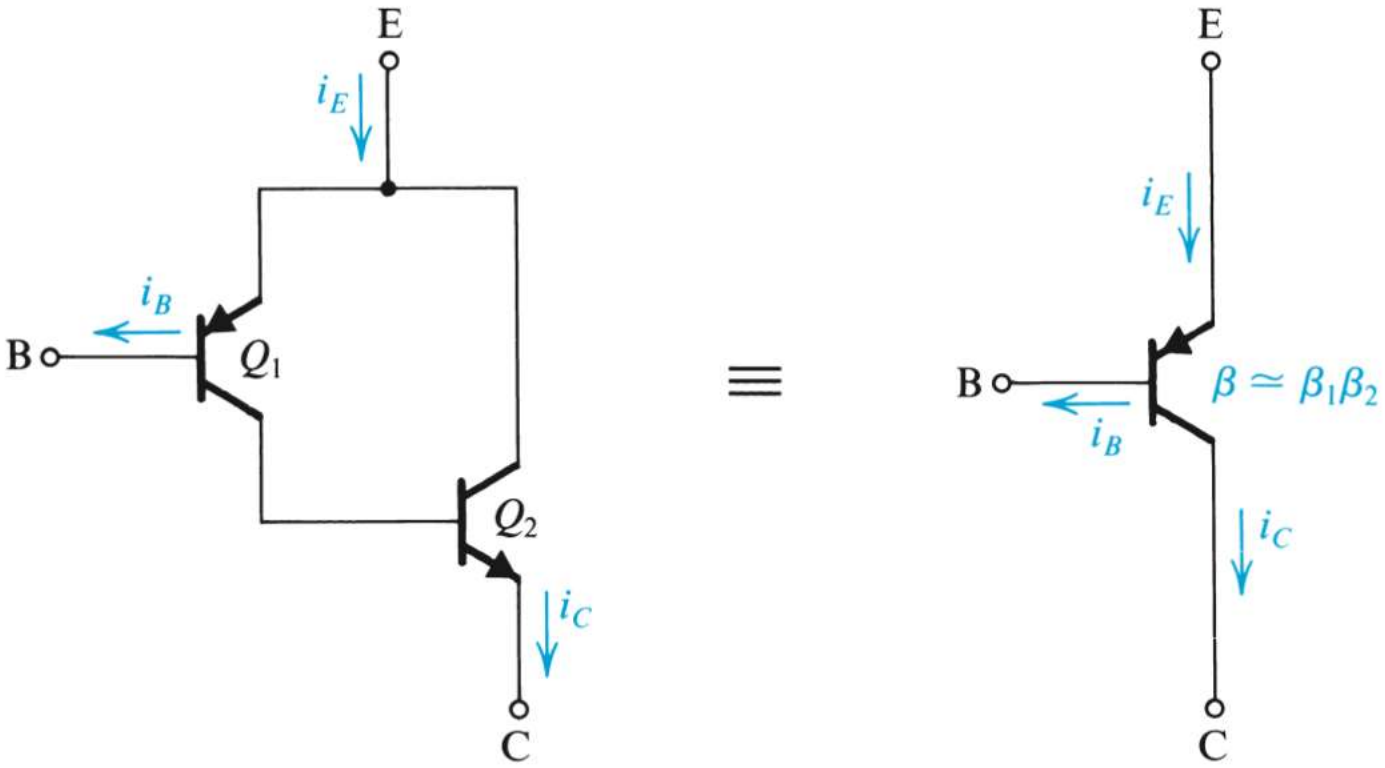


Figure 12.19 The compound-*pnp* configuration.

AB类功放

④改进结构

12.6.2 Use of Compound Devices

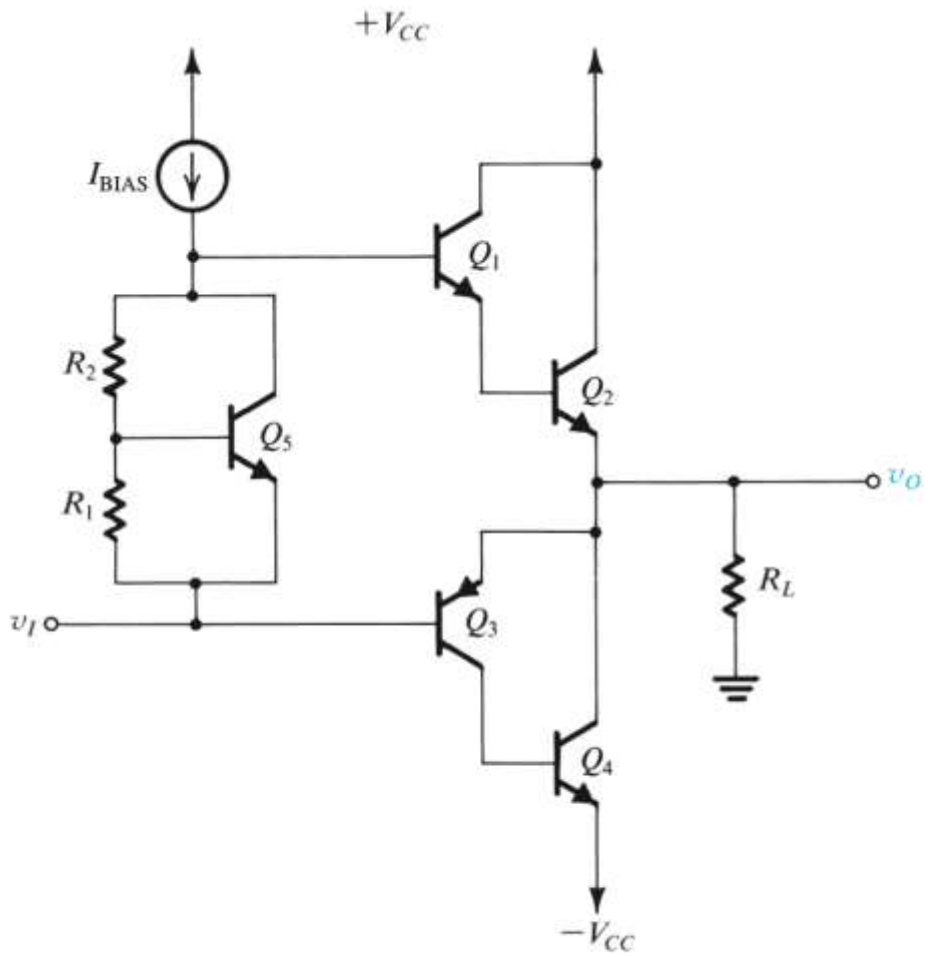
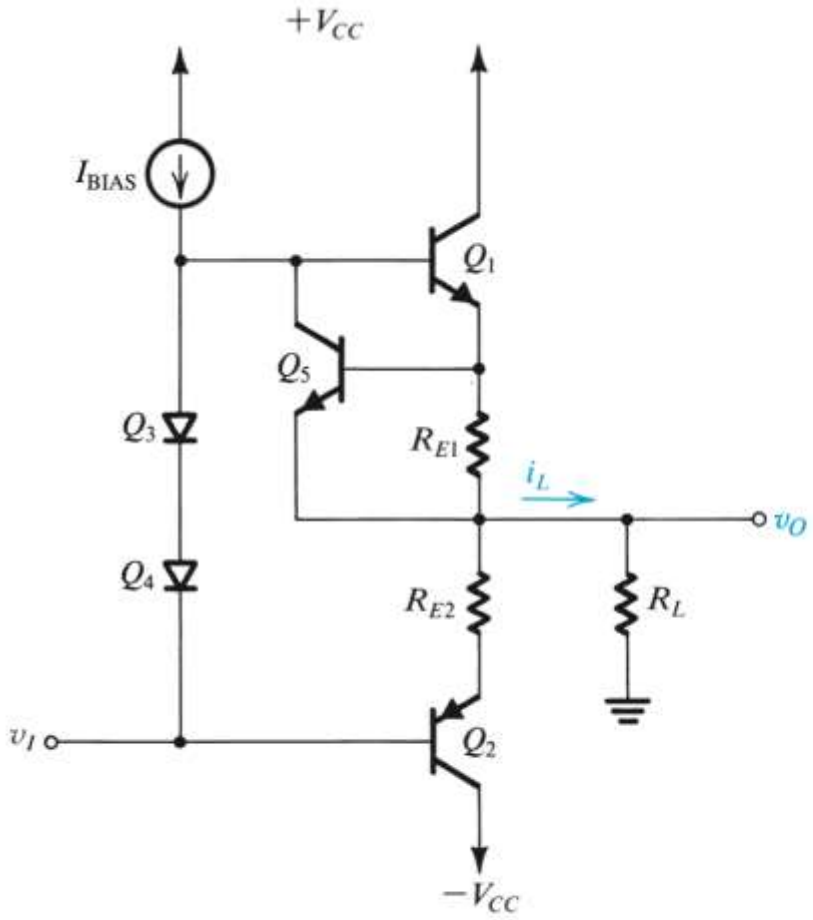


Figure 12.20 A class AB output stage utilizing a Darlington *npn* and a compound *pnp*. Biasing is obtained using a V_{BE} multiplier.

AB类功放

⑤短路保护



流过Q_1的电流过大时，R_{E1}上的电压降使得Q_5开启，减小流过Q_1的电流

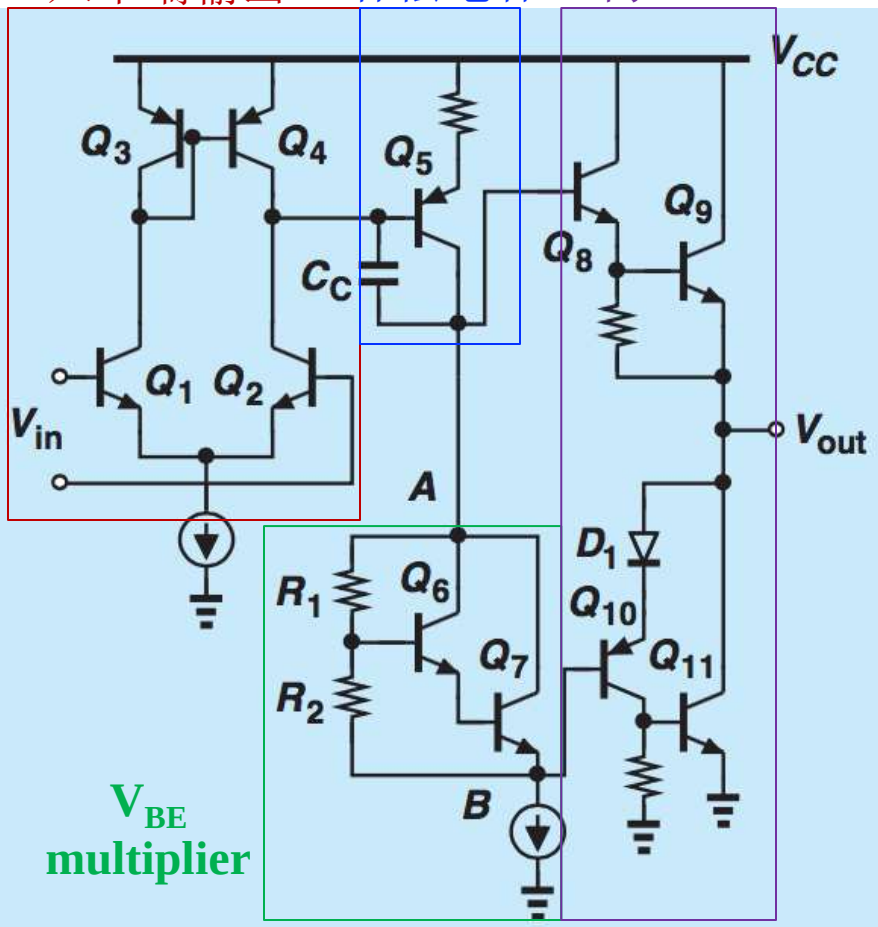
Figure 12.21 A class AB output stage with short-circuit protection. The protection circuit shown operates in the event of an output short circuit while v_o is positive.

实例

Did you know?

Many audio power amplifiers are implemented as "hybrids." A hybrid consists of a small board (called the "substrate") with the components mounted on it in chip form (rather than in packaged form). Shown below is the simplified circuit diagram of the STK4200, a 100-W audio PA manufactured by Sanyo. We recognize most of the circuit configurations here. Transistors Q_1-Q_4 form a differential pair with active load, serving as a simple op amp. Transistor Q_5 realizes the second gain stage, and C_c performs Miller compensation. Devices Q_6 and Q_7 along with R_1 and R_2 comprise a "V_{BE} multiplier," creating a dc voltage difference of about four V_{BE}'s between A and B. Finally, Q_8-Q_{11} and D_1 operate as a push-pull stage. The circuit is placed in a negative feedback loop in a manner similar to a noninverting amplifier.

第一级差分输入单端输出　第二级含补偿电容　推挽结构PA



Simplified circuit of high-power audio amplifier STK4200.

AB类功放——MOSFET

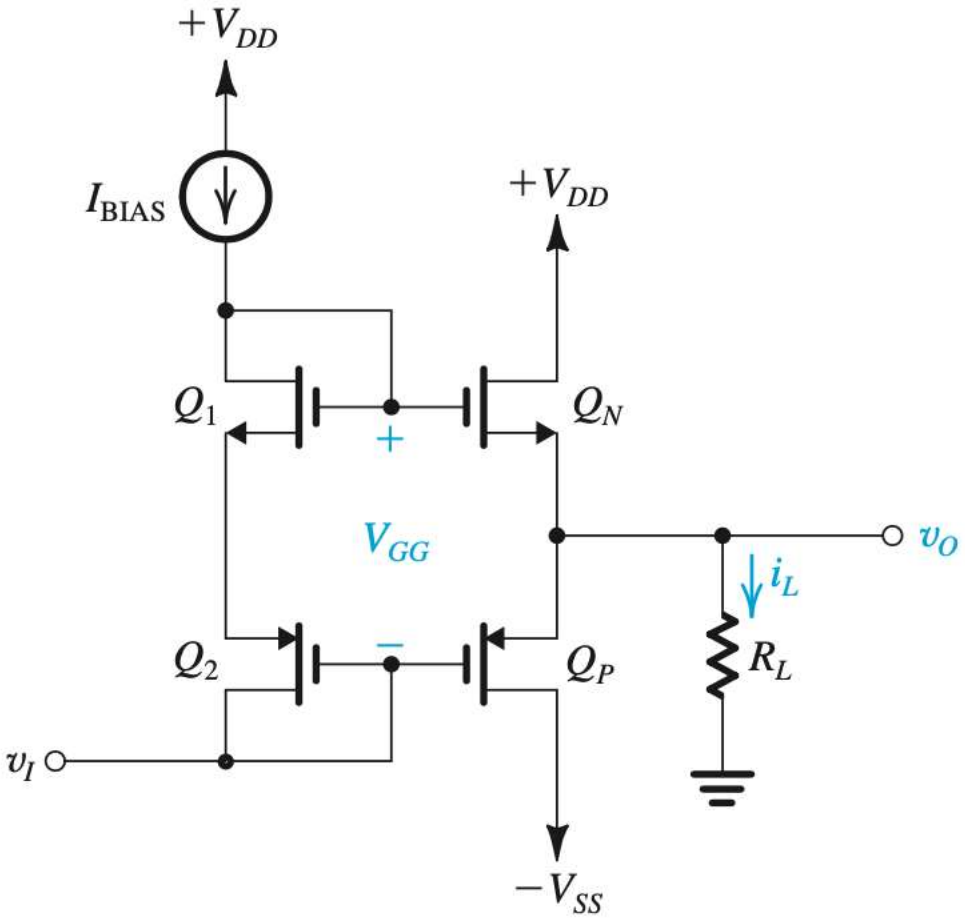


Figure 12.23 Classical CMOS class AB output stage. This circuit is the CMOS counterpart of the BJT circuit in Fig. 11.14 with the biasing diodes implemented with diode-connected MOSFETs Q_1 and Q_2

简化版本，大致理解即可

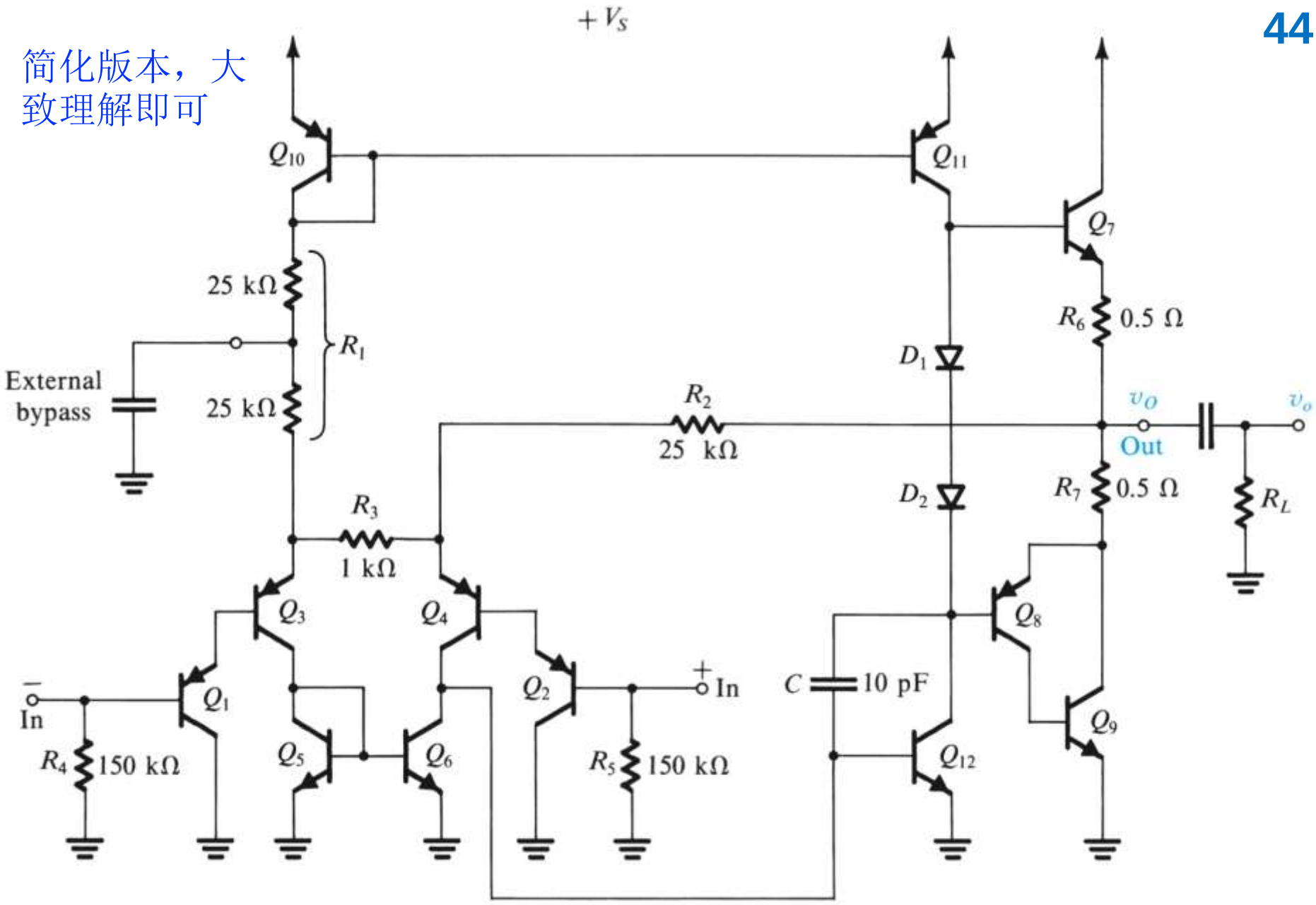
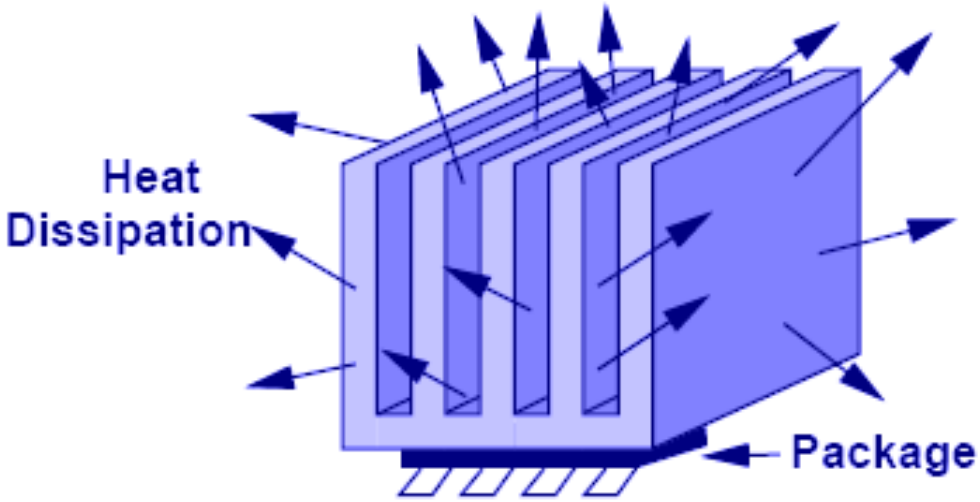


Figure 12.29 The simplified internal circuit of the LM380 IC power amplifier. (Courtesy National Semiconductor Corporation.)

热沉



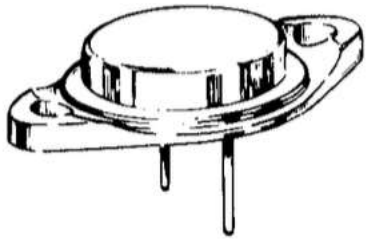


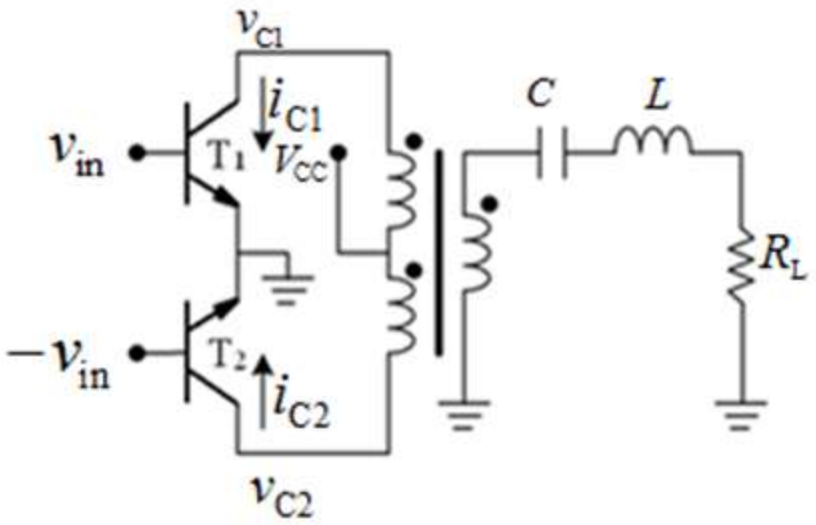
Figure 11.25 The popular TO3 package for power transistors. The case is metal with a diameter of about 2.2 cm; the outside dimension of the "seating plane" is about 4 cm. The seating plane has two holes for screws to bolt it to a heat sink. The collector is electrically connected to the case. Therefore an electrically insulating but thermally conducting spacer is used between the transistor case and the "heat sink."

- 常用的散热手段，除了PA，在LED等其他地方也能经常见到

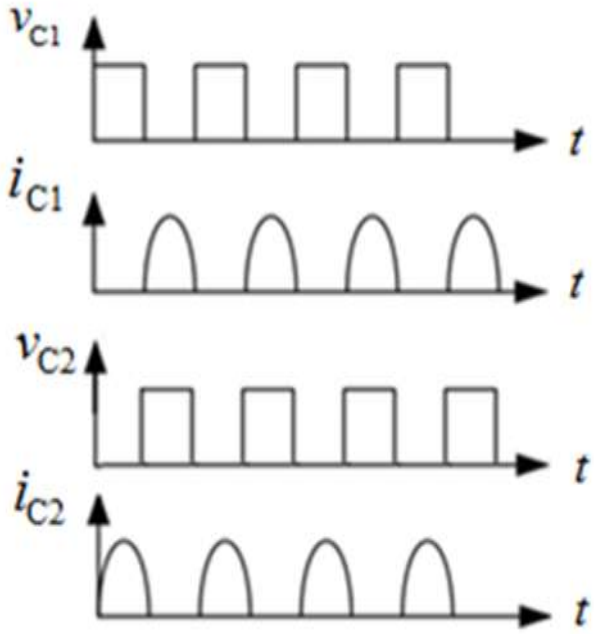
开关功率放大器

- 为了使功率放大器具有更高的效率，就必须大大减小晶体管功耗，直至为0，于是出现了开关功率放大器。对于一个理想开关，其两端电压和流过的电流并不同时出现，因此，其直流功耗为0。而开关功率放大器正是通过减少加在晶体管两端电压和流过的电流波形的交叠时间来提高效率的。
- 根据电路组成、驱动信号、工作方式等不同，开关功率放大器分为D类、E类和F类等。

D类功率放大器



主要由两只开关管和由谐振在基波频率的串联LC电路形成的滤波电路组成。该滤波电路对基波呈现的阻抗可以忽略，但对谐波具有很高的阻抗，从而可以阻止各谐波输出。



开关管T_1和T_2集电极的电流i_{C1}和i_{C2}呈推挽状态作用于变压器初级，但电流脉冲出现期间，对应的开关管的集电极电压全部为0。因此理想情况下，D类功放可达到100%的效率。

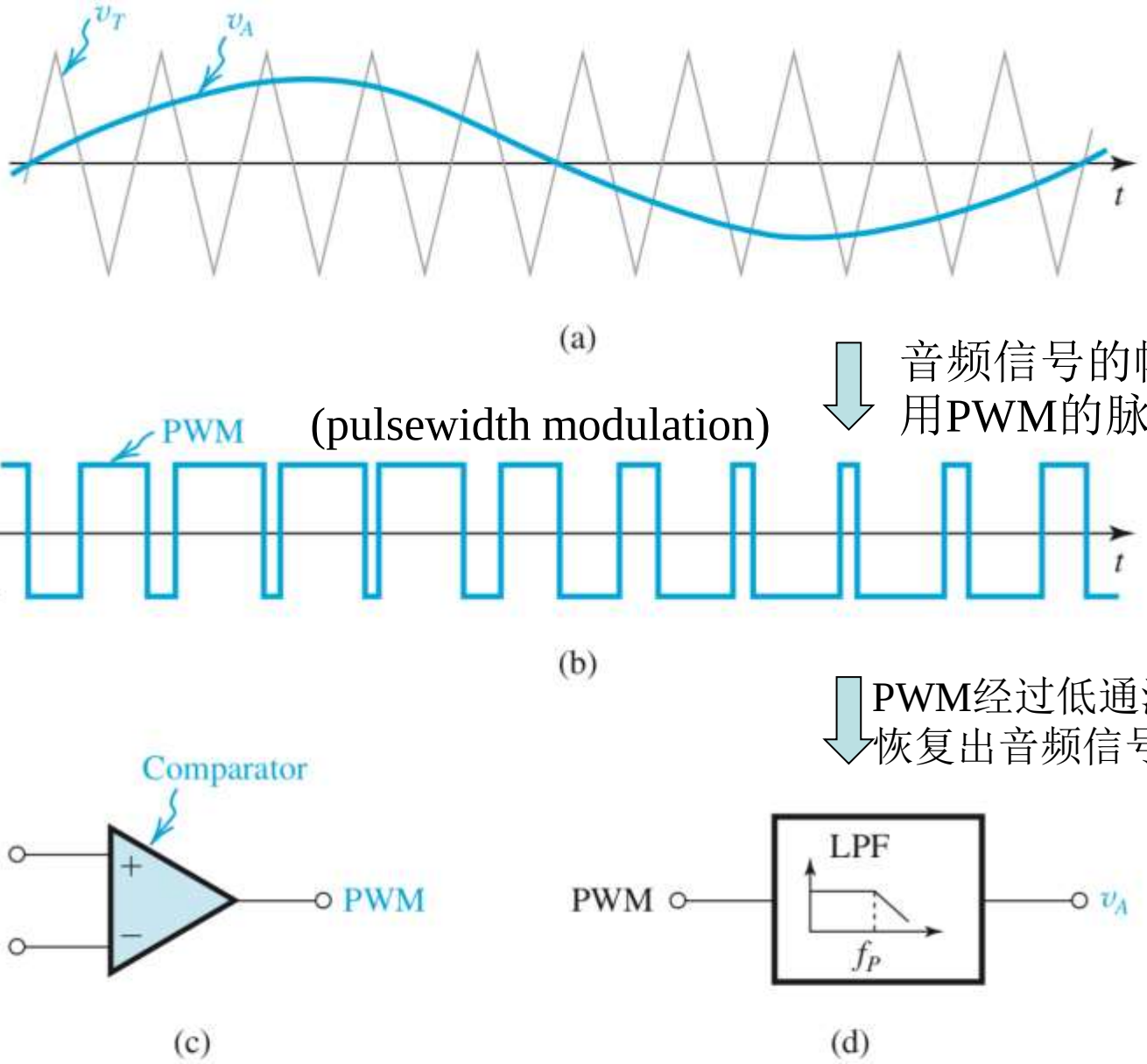
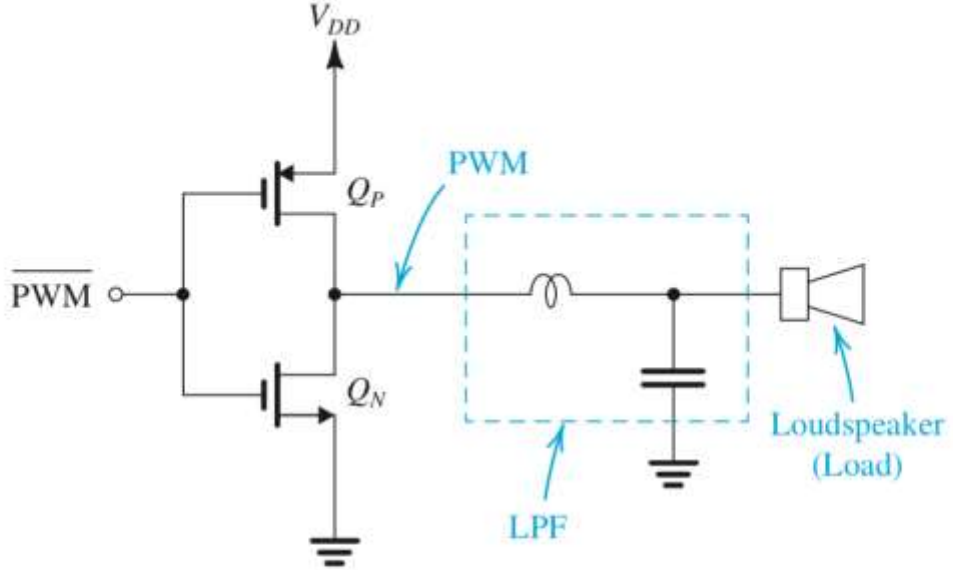
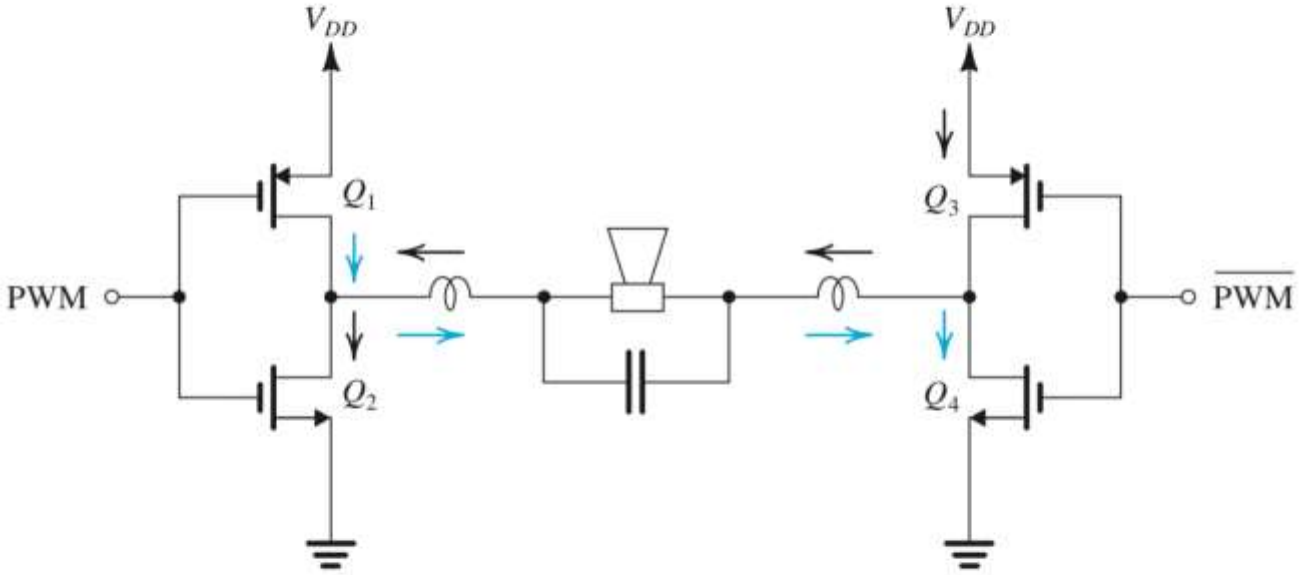


Figure 12.33 (**a**) By comparing the magnitude of the audio signal v_A to that of a triangular wave v_T, the PWM signal in (**b**) can be generated by using the comparator in (**c**). (**d**) The original signal v_A can be recovered from the PWM signal by means of a low-pass filter with a passband frequency f_P slightly larger than the highest audio-frequency component of v_A.



(a)



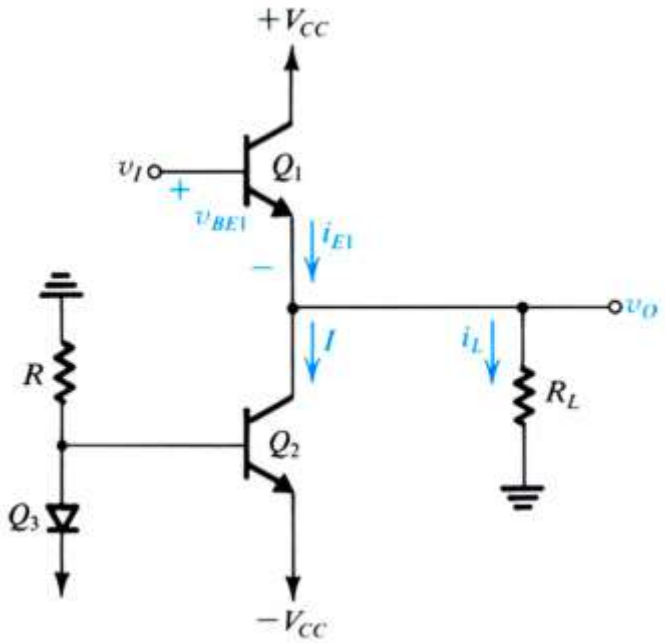
(b)

Figure 12.34 Two schemes for driving the load of a class D amplifier. The differential scheme in (**b**) results in doubling the voltage excursion across the load.

作业

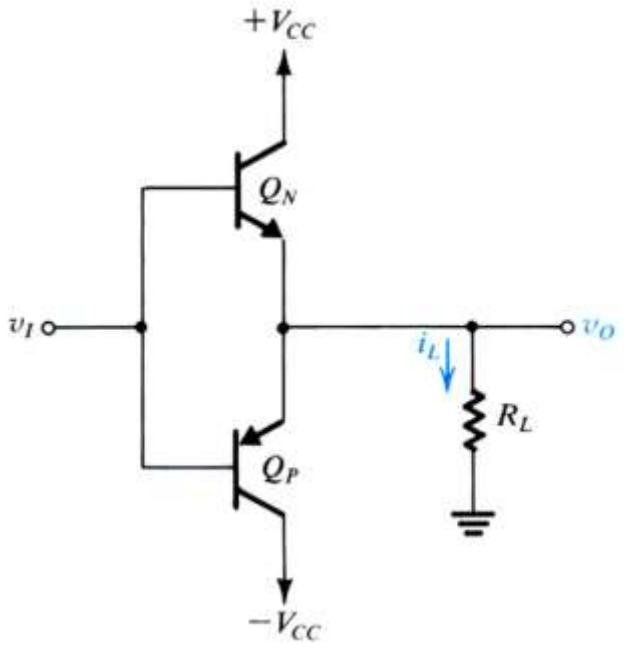
12.3 For the emitter follower of Fig. 12.3, let $V_{CC} = 10\,\text{V}$, $I = 100\,\text{mA}$, and $R_L = 100\,\Omega$. If the output voltage is an 8-V-peak sinusoid, find: (a) the power delivered to the load; (b) the average power drawn from the supplies; (c) the power-conversion efficiency. Ignore the loss in Q_3 and R.

Ans. 0.32 W; 2 W; 16%



12.4 For the class B output stage of Fig. 12.6, let $V_{CC}=6$ V and $R_L=4\,\Omega$. If the output is a sinusoid with 4.5-V peak amplitude, find (a) the output power; (b) the average power drawn from each supply; (c) the power efficiency obtained at this output voltage; (d) the peak currents supplied by v_I, assuming that $\beta_N=\beta_P=50$; and (e) the maximum power that each transistor must be capable of dissipating safely.

Ans. (a) 2.53 W; (b) 2.15 W; (c) 59%; (d) 22.1 mA; (e) 0.91 W



12.8 Consider a V_{BE} multiplier with $R_1 = R_2 = 1.2\,\text{k}\Omega$, utilizing a transistor that has $V_{BE} = 0.6\,\text{V}$ at $I_C = 1\,\text{mA}$, and a very high β. (a) Find the value of the current I that should be supplied to the multiplier to obtain a terminal voltage of 1.2 V. (b) Find the value of I that will result in the terminal voltage changing (from the 1.2-V value) by +50 mV, ~~+100 mV, +200 mV, −50 mV, −100 mV, −200 mV.~~

Ans. (a) 1.5 mA; (b) 3.24 mA, ~~7.93 mA, 55.18 mA, 0.85 mA, 0.59 mA, 0.43 mA~~