Lecture 14 – MOSFET
场效应晶体管-part1

Chapter 5 from **Microelectronic Circuits** Text by Sedra and Smith

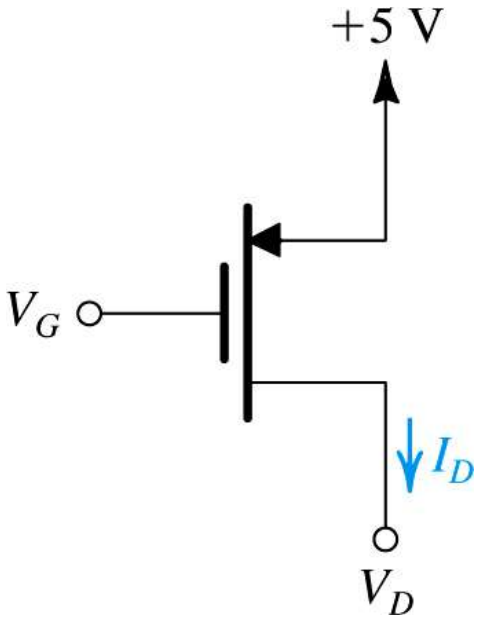
Oxford Publishing

课程纲要

- 9.1 场效应晶体管的结构和工作原理
- 9.1.1 重点介绍N沟道增强型MOSFET的结构和工作原理
- 9.1.2 认识不同类型场效应管的符号和结构差异
- 9.2 场效应晶体管的特性及其等效模型
- 9.2.1 输入特性、输出特性和转移特性
- 9.2.2 π型和T型等效电路（中频）
- 9.3 场效应晶体管放大电路的构成及其分析
- 9.3.1 直流偏置电路及其分析
- 9.3.2 三种接法放大电路的分析计算

Introduction

- **Q:** 一个 three-terminal device可能的工作方式?
  - **A:** 受控源，如电压控制电流源，右图为一个典型的PMOS器件，“5V”和“V_G”之间的电压控制流过“5V”和“V_D”的电流
  - 电压控制电流源可用来设计电压电压放大器



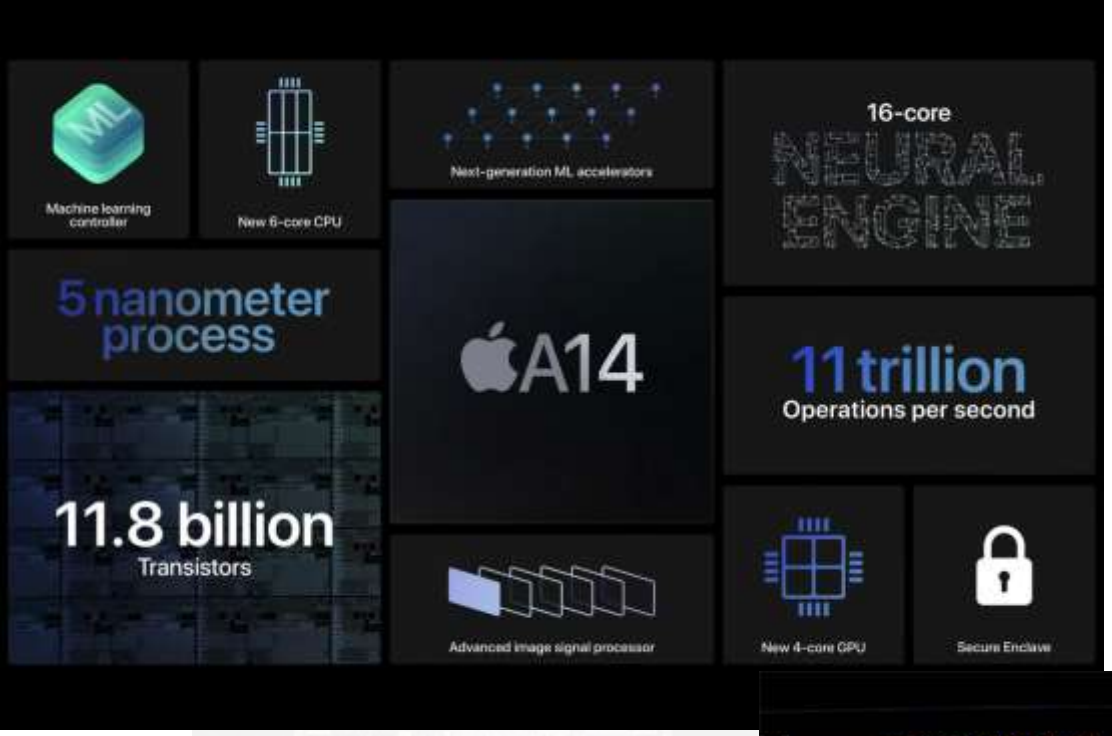
Introduction

note: MOSFET is more widely used in implementation of modern electronic devices 工业界，**MOSFET是绝对主流**

- **Q:** 两种主要的 three-terminal 半导体器件?
  - metal-oxide-semiconductor field-effect transistor (MOSFET)
  - bipolar junction transistor (BJT)
- **Q:** 其中MOSFET是最为广泛使用的?
  - 尺寸小
  - 容易制造
  - 功耗低
- **Q:** Transistor（晶体管）的主要应用
  - 信号放大器
  - 逻辑电路
  - Memory
- **Q:** Transistor（晶体管）的核心工作原理
  - **电压控制的电流源**

Processor name	Kirin 990 5G	Apple A13 Bionic	Snapdragon 855 Plus
CPU	Tri-cluster octa-core (2 x Cortex-A76 cores @2.86GHz 2x Cortex-A76 cores @2.36GHz 4x Cortex-A55 cores @1.95GHz)	Dual-cluster hexa-core (2x Lightning cores @2.66 GHz 4x Thunder efficiency cores)	Tri-cluster octa-core (1x Kryo 485 @2.96 GHz 3x Kryo 485 @2.42 GHz 4x Kryo 485 @1.78 GHz)
GPU	Mali-G76MP16, 700MHz	Apple-designed quad-core	Adreno 640, 700MHz
Process	TSMS 7NM+ EUV	TSMS 7nm+	TSMS 7nm
NPU	2 + 1 Da Vinci (three cores)	octa-core Neural Engine	Qualcomm Hexagon 690
RAM	LPDDR4X	LPDDR4X	LPDDR4X
Modem	Integrated Balong 5G D/L Speed 2.3 Gbps U/L Speed 1.25 Gbps	LTE	Snapdragon X50 external 5G D/L speed 2 Gbps U/L speed 316 Mbps
Geekbench score	**Single-Core: 3,842** **Multi-Core: 11,644**	**Single-Core: 5,415** **Multi-Core: 11,294**	**Single-Core: 3,623** **Multi-Core: 11,365**

Year 2019

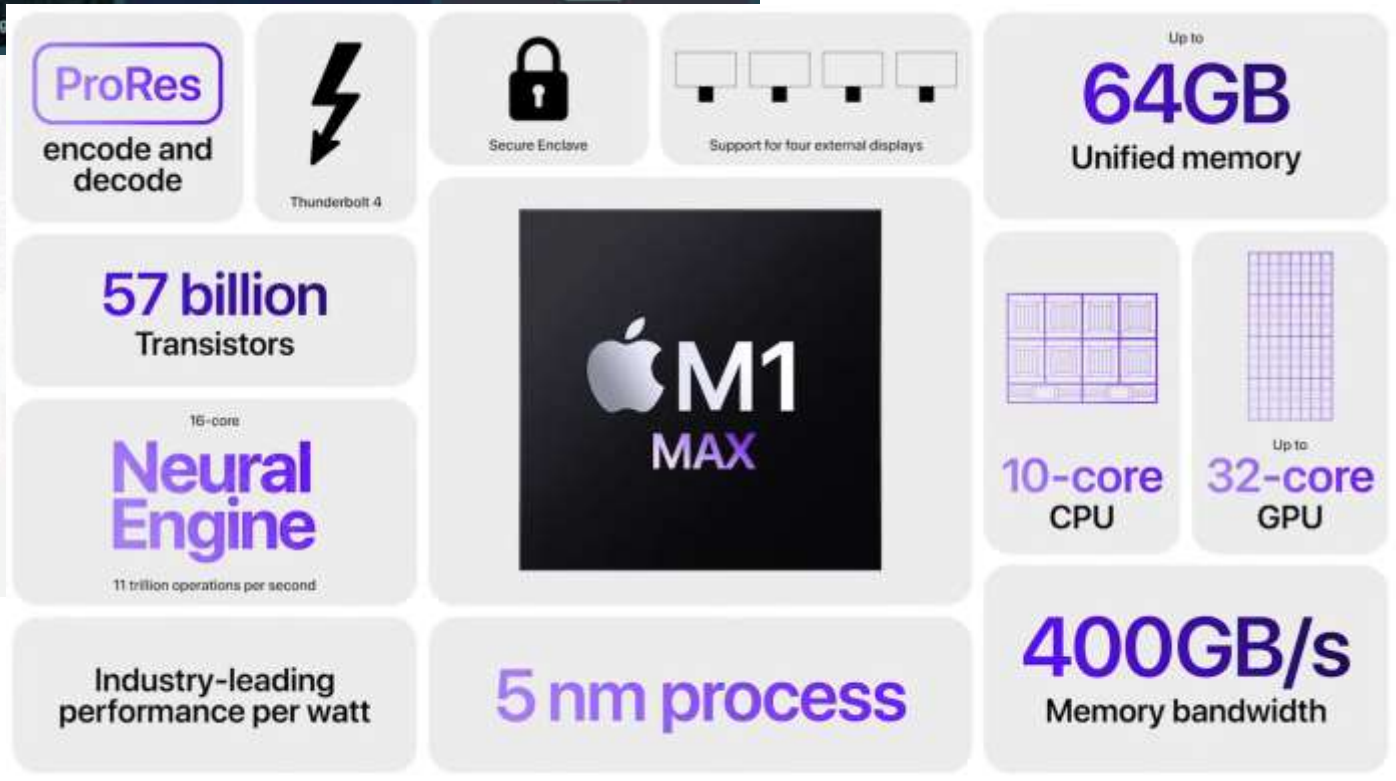

Machine learning controller
New 6-core CPU
Next-generation ML accelerators
16-core
NEURAL ENGINE
5 nanometer process
A14
11 trillion
Operations per second
11.8 billion
Transistors
Advanced image signal processor
New 4-core GPU
Secure Enclave

Year 2020

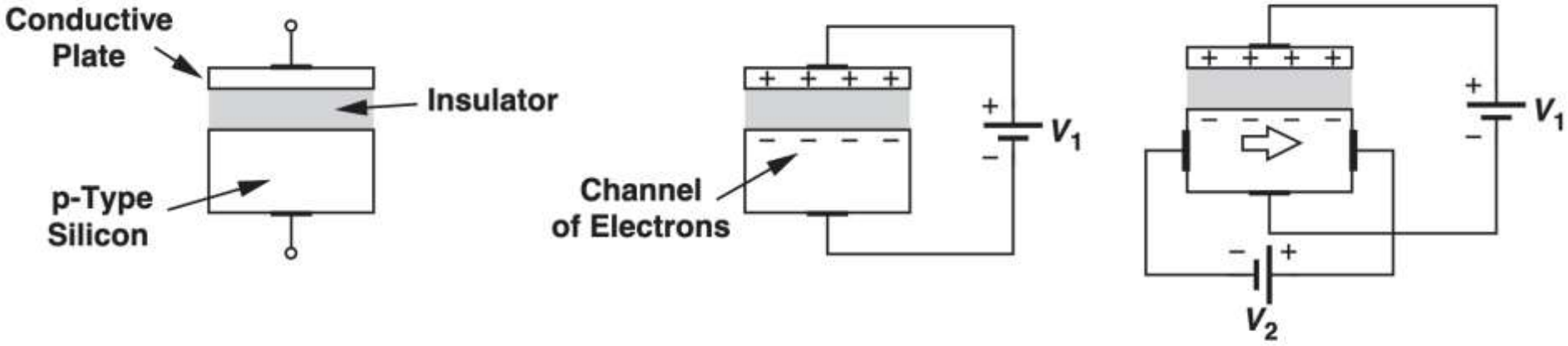

5 nanometer 5G SoC
15.3 Billion
Transistors
The Most Powerful
5G
Kirin 9000
Chip, Ever
World's 1st 24-Core Mali-G78 GPU
Quad
ISP
2 Big-Core
1 Tiny-Cor
NPU
New 8-Core CPU
Frequency up to
3.13GHz
Super Uplink
5G
Downlink CA


15 billion
transistors
50% faster
CPU
vs. competition
2x
system cache
30% faster
GPU
vs. competition
Faster
NEURAL ENGINE
A15
15.8 trillion
operations per second
New video encoder
New video decoder
New ISP
New display eng

Year 2021


ProRes
encode and decode
Thunderbolt 4
Secure Enclave
Support for four external displays
Up to
64GB
Unified memory
57 billion
Transistors
M1
MAX
16-core
Neural Engine
11 trillion operations per second
10-core
CPU
Up to
32-core
GPU
Industry-leading performance per watt
5 nm process
400GB/s
Memory bandwidth

Metal-Oxide-Semiconductor (MOS)



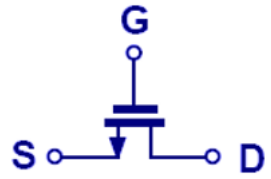
- MOS 结构可看作一平板电容，上电极（Conductive Plate）带正电，二氧化硅为中间介质，下电极（p-Type Silicon）带负电
- Q=CV，channel中的负电荷量（电子浓度、沟道电导率）受电压V_1控制，C越大，控制能力越强，所以要求SiO_2厚度小
- 施加V_2后，沟道中电子定向移动形成电流，电流大小受电压V_1控制 → 电压控制电流源

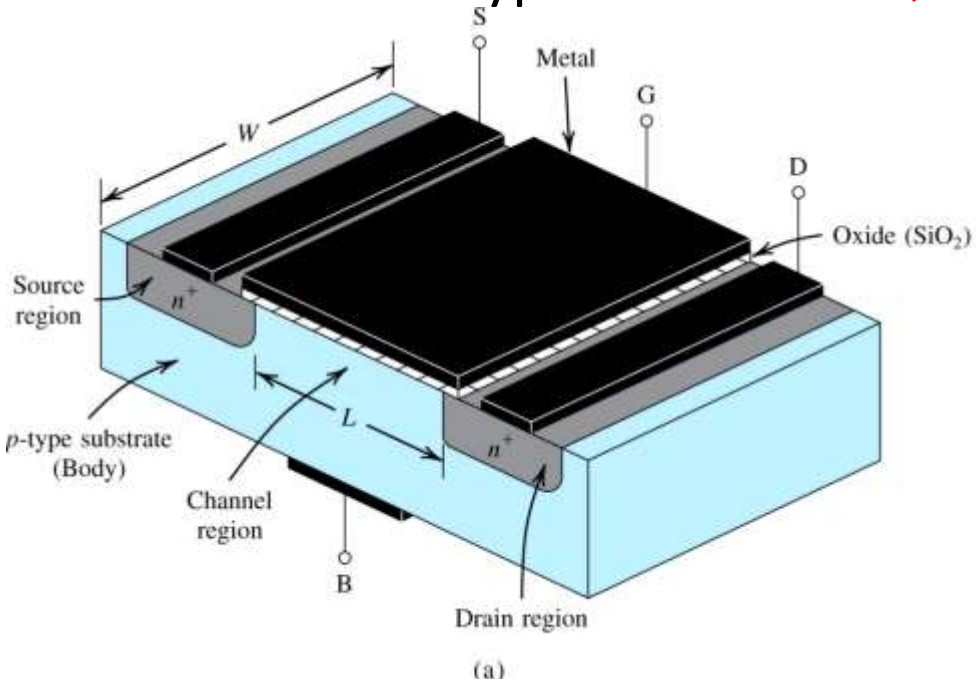
5.1. Device Structure and Operation器件结构与工作原理

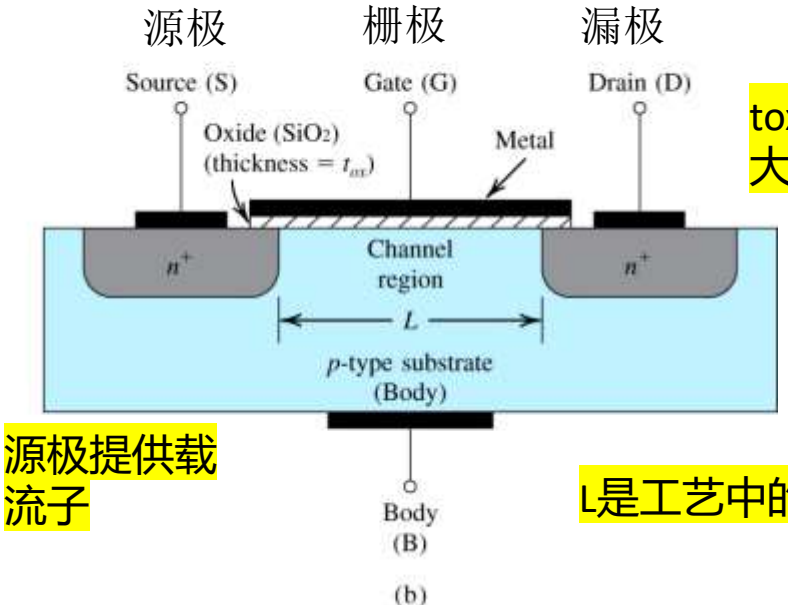
- L的最小值是表征工艺的关键参数
- 对称结构，“源”和“漏”可以调换.
- 为了防止PN结正偏，B往往是系统中的最低电位，所以一般情况下可以将其忽略→三端器件（S，D，G）

符为。最是

- Figure 5.1. shows general structure of the *n*-channel enhancement-type MOSFET N沟道增强型MOSFET







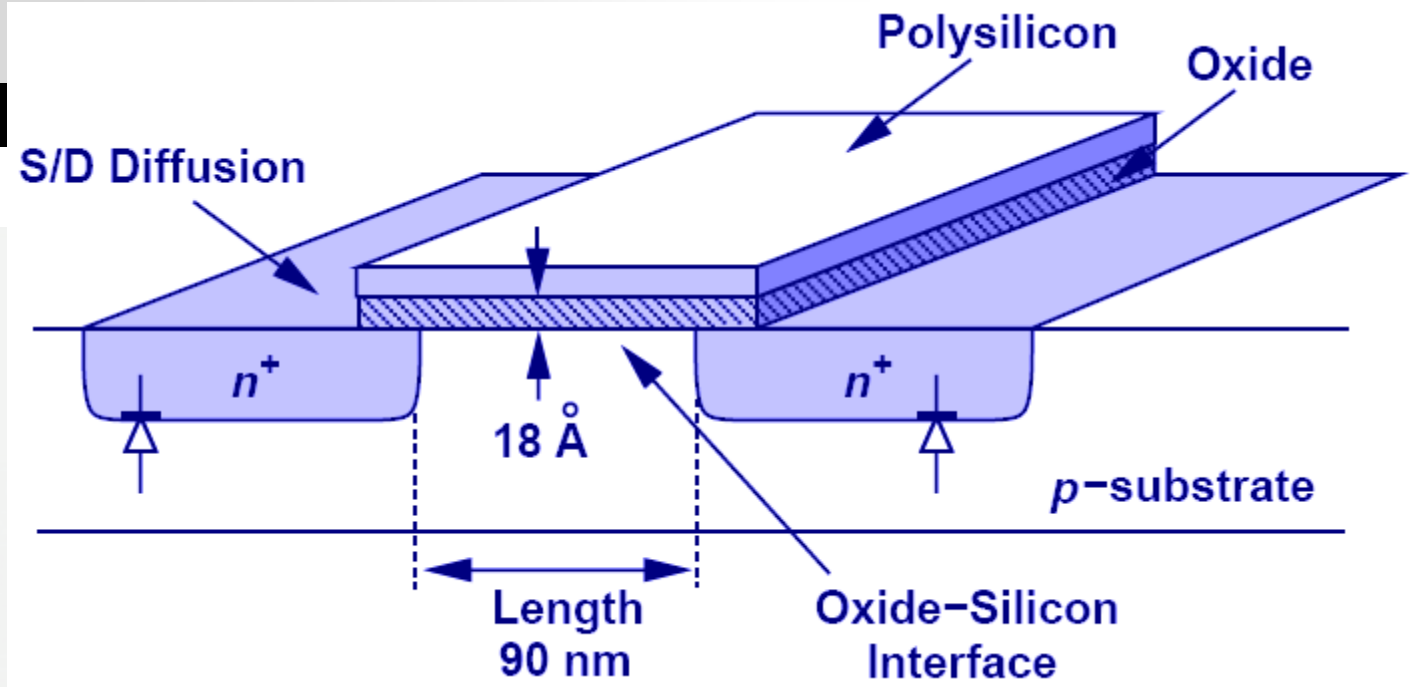
tox影响大小

源极提供载流子

L是工艺中的关键

Figure 5.1: Physical structure of the **enhancement-type NMOS transistor**: **(a)** perspective view, **(b)** cross-section. Note that typically **L** = 0.03*um* to 1*um*, **W** = 0.1*um* to 100*um*, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10*nm*.

近几年的 N沟道增强型 MOSFET 结构



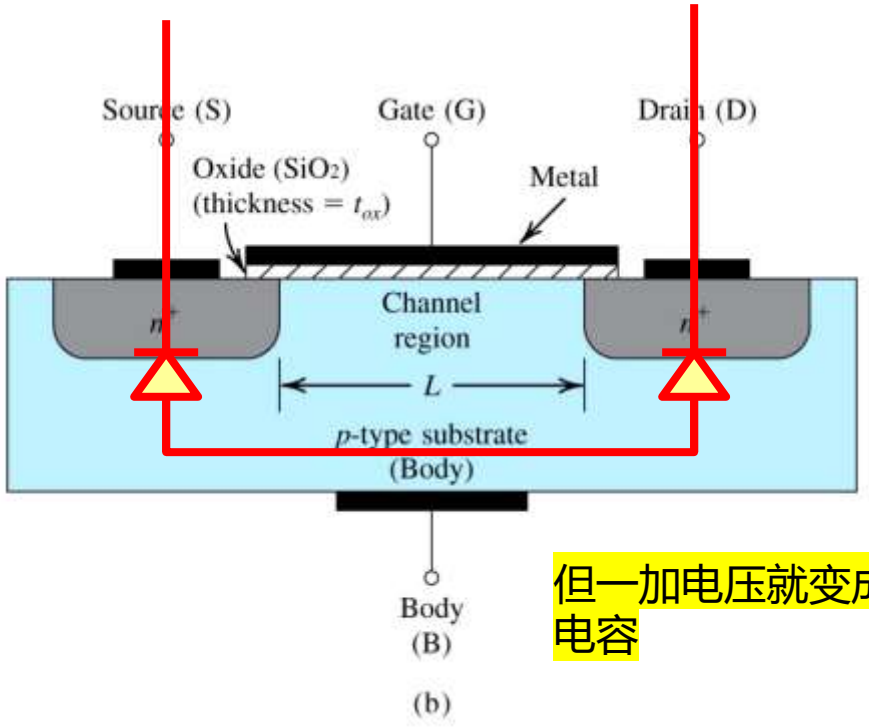
- 栅极采用多晶硅（polysilicon），绝缘层采用SiO_2（也称为栅氧）.
- p-衬底一般处于最低电位，所以衬底和S、D分别构成两个反向偏置的pn结
- D的电位高于S的电位，电子从S流向D（电流从D流向S）

5.1.2. **Operation with Zero Gate Voltage**

$V_G = 0$ 时，S和D之间不导通

当Gate电压为0时，默认两个pn结仍在，永远不会导通，不会有电流流过。

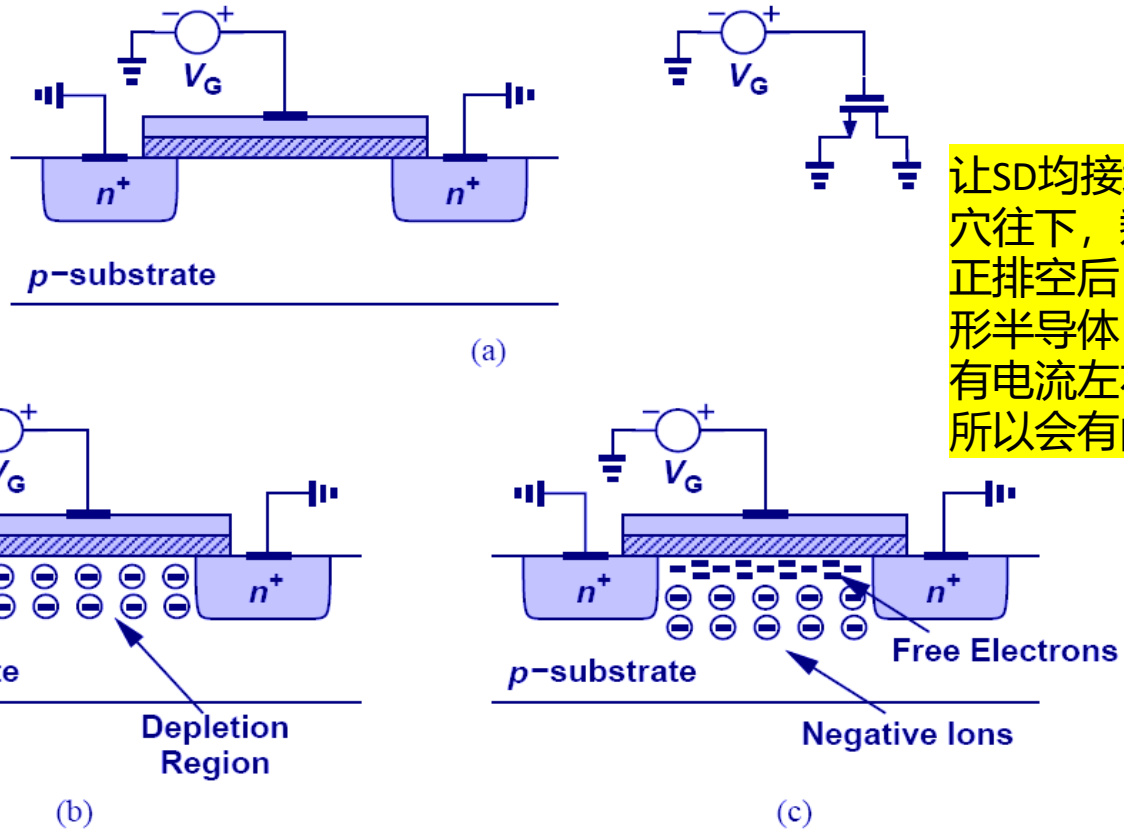
- With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
- "They" prevent current conduction from drain to source when a voltage v_{DS} is applied.
  - yielding very high resistance (10^{12}*ohms*)



但一加电压就变成电容

Figure 5.1: Physical structure…

Channel (沟道) 的形成



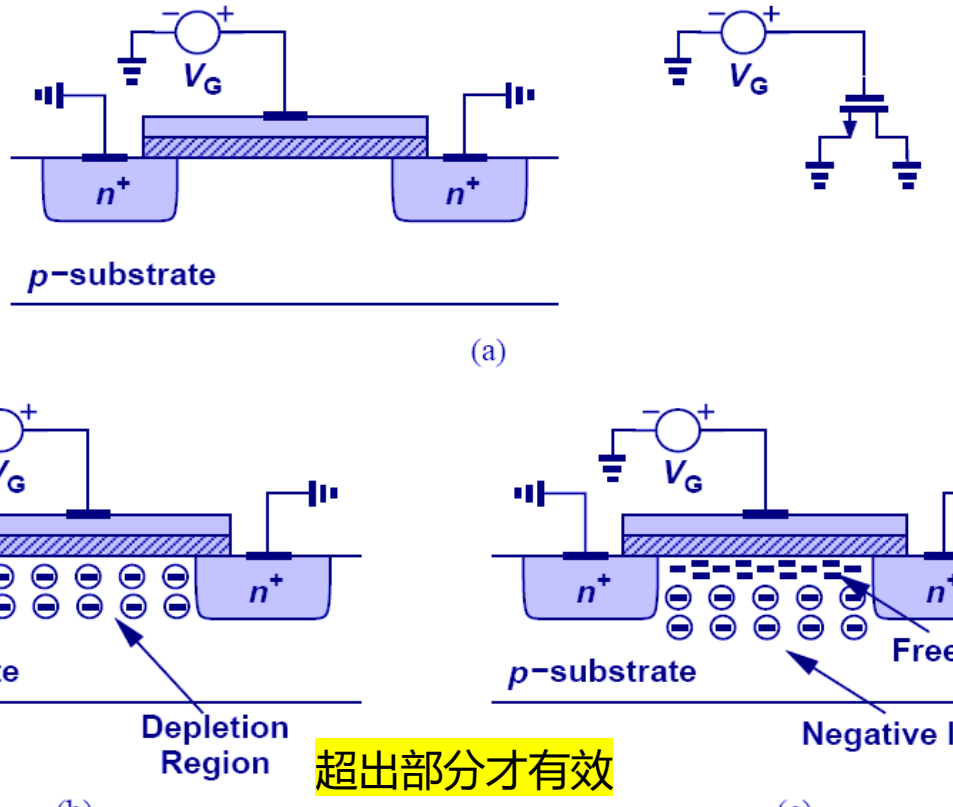
让SD均接地，变化G，看分布
穴往下，剩下固定不变的负
正排空后，会有电子被吸上
形半导体，载流子是大量电
有电流左右移动。
所以会有阈值电压，超出阈

写为Vgs是因为
一般相同

- 当V_{GS}从零开始增加时，首先，衬底的空穴被栅极的正电荷排斥，留下带负电的固定负离子，形成耗尽区；
- 然后，当V_{GS}继续增加时，电子被吸引到栅极和衬底的交界面，形成“反型层（沟道）”（使靠近栅极附近的极薄的一个衬底区域反型，p→n，形成n沟道，连通n型的源极和n型的漏极）；存在一个阈值，当V_{GS}大于该阈值时，沟道形成；该阈值称为阈值电压V_{TH}（V_t），超出阈值电压部分的VGS称为有效电压（或overdrive voltage）

$$v_{GS} - V_t \equiv v_{OV}$$

Channel (沟道) 的形成



Cox为单位面积电容乘以面积即可得。C。而W和L是设计参数调整。

超出部分才有效

$$v_{GS} - V_t \equiv v_{OV}$$

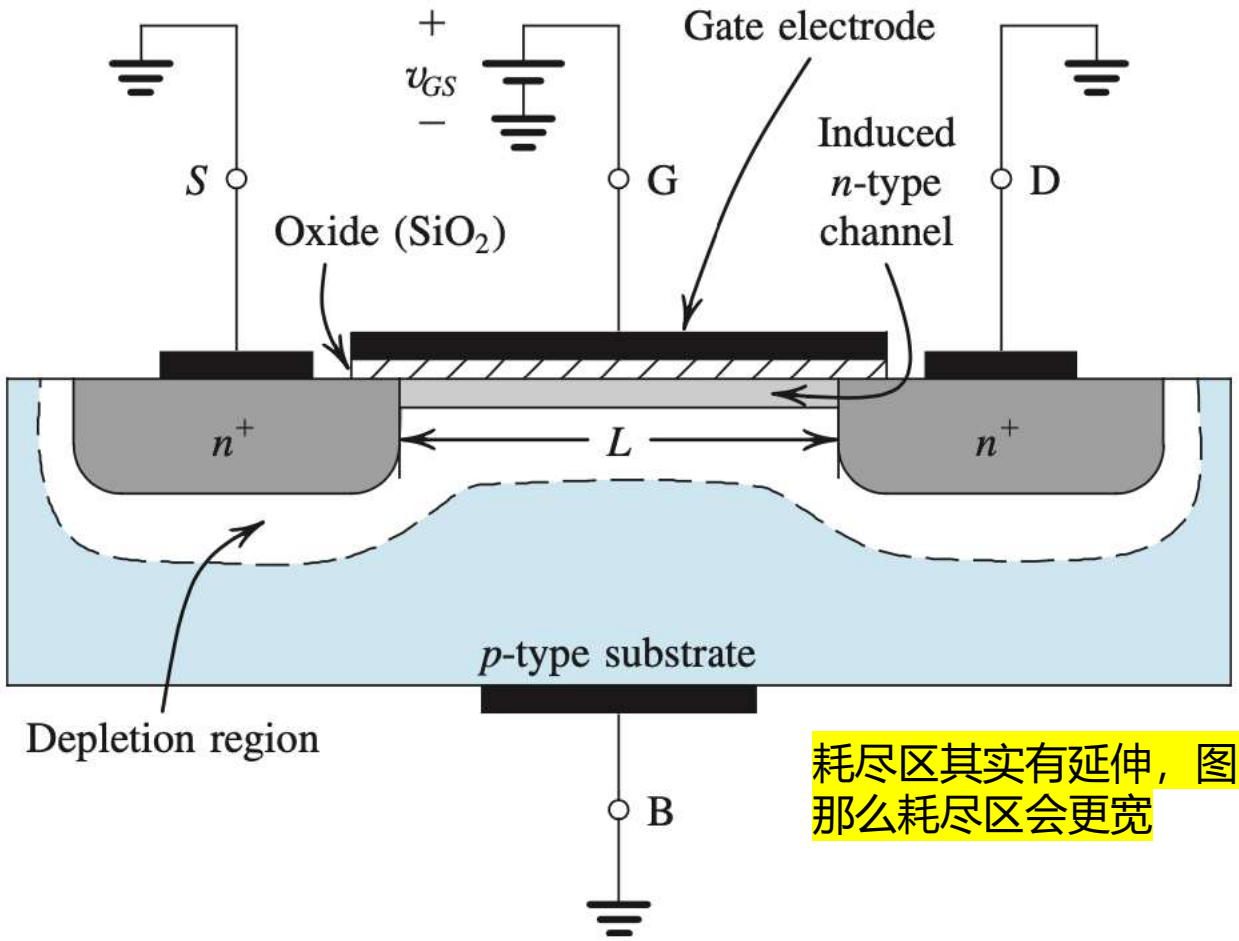
- 沟道中的电荷量

$$Q = Cv_{OV}$$
$$C = C_{ox}WL$$
$$\Longrightarrow \quad |Q| = C_{ox}(WL)v_{OV}$$

where C_{ox}, called the **oxide capacitance**, is the capacitance of the parallel-plate capacitor per unit gate area (in units of F/m^2), W is the width of the channel, and L is the length of the channel. The oxide capacitance C_{ox} is given by

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

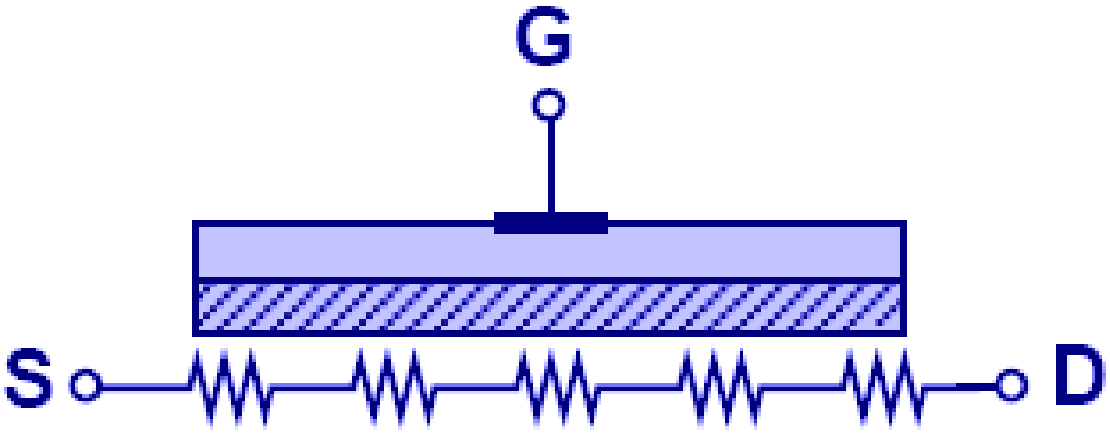
$$\epsilon_{ox} = 3.9\epsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$



耗尽区其实有延伸，图中白色均是。若D不
那么耗尽区会更宽

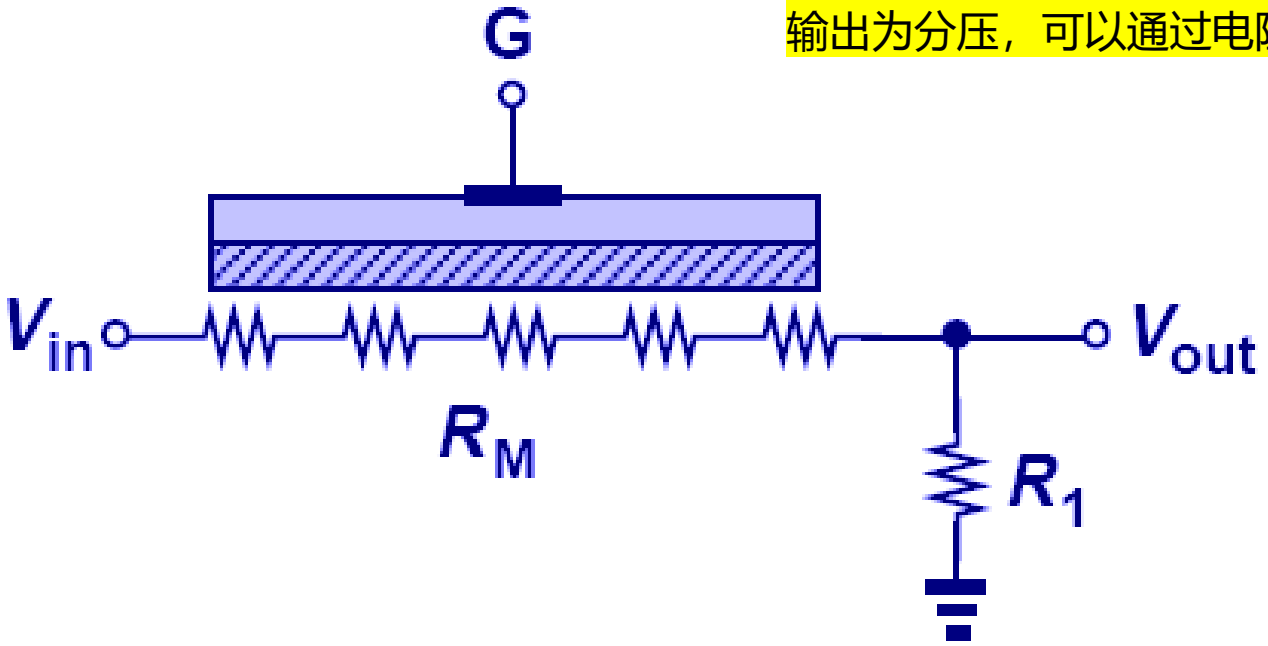
Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

压控电阻（Voltage-Dependent Resistor）



- 反型沟道可以看作一个电阻；
- V_{GS}越大 → 沟道内电荷（电子）越多 → 沟道电阻越小
- 沟道内的电荷密度取决于栅极电压，所以该电阻是一压控电阻；

压控衰减器 （Voltage-Controlled Attenuator）



输出为分压，可以通过电阻调节

- 当栅极电压降低时，沟道电阻增加，导致V_{out}减小；
- 应用：当手机靠近基站时，接收到的信号强度显著增加，这时使用压控衰减器可以适当减小信号强度，以避免接收机饱和；

5.1.3. Creating a Channel for Current Flow

压控电阻的定量分析

V_{tn} is used for *n*-type MOSFET, V_{tp} is used for *p*-channel

为了和 V_T（26 mV）区分，有时也将阈值电压写成 V_{TH}

- **threshold voltage** (V_t) – is the minimum value of v_{GS} required to form a conducting channel between drain and source 阈值电压
  - typically between 0.3 and 0.6V_{dc}
- **field-effect** – when positive v_{GS} is applied, an electric field develops between the gate electrode and induced *n*-channel – the conductivity of this channel is affected by the strength of field
  - SiO_2 layer acts as dielectric

电压V_{GS}产生电场，该电场影响沟道的电导率，故称为“场效应”

- **effective / overdrive voltage** – is the difference between v_{GS} applied and V_t. 有效电压

$$(eq5.1)\quad v_{OV} \equiv v_{GS} - V_t$$

只有超过V_t部分的V_{GS}才是有效的

- **oxide capacitance** (C_{ox}) – is the capacitance of the parallel plate capacitor per unit gate area (F/m^2)

ε_{ox} is permittivity of SiO_2 =3.45**E**–11(F/m)
t_{ox} is thickness of SiO_2 layer

$$(eq5.3)\ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \text{ in } F/m^2$$

5.1.3. Creating a Channel for Current Flow

目的：求沟道电阻；
方法：加电压，求电流

- **Q:** What is main requirement for *n*-channel to form?
  - **A:** The voltage across the "oxide" layer must exceed V_t.
  - 形成沟道的条件：栅极G与沟道的电压差 > V_t
- For example, when v_{DS} = 0…
  - the voltage at every point along channel is zero
  - the voltage across the oxide layer is uniform and equal to v_{GS}
  - 若v_{DS} = 0，则沟道内每一点的电压都相等=V_S=0

真实的沟道不是均匀的，因为有VD

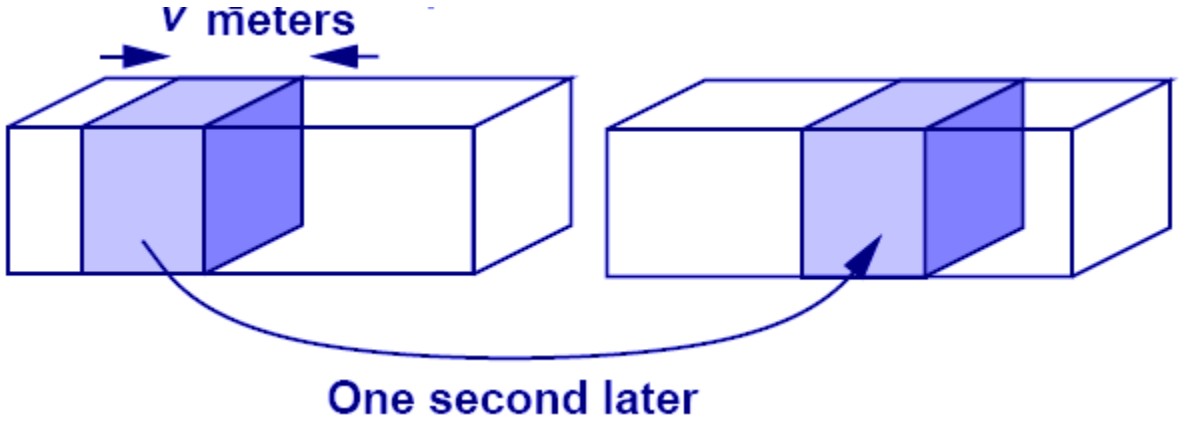
- **Q:** How can one express the magnitude of electron charge contained in the channel?
  - **A:** See below… 沟道内电荷量计算
  - 当V_{OV}=0时，沟道刚刚要形成，此时Q=0；

W and *L* represent width and length of channel respectively

(eq5.2) $|Q| = C_{ox}(WL)v_{OV}$ in *C*

- **Q:** What is effect of v_{OV} on *n*-channel?
  - **A:** As v_{OV} grows, so does the electron density in the *n*-channel. Conductivity increases. v_{OV} 增加→沟道中的电荷增加→导电性增加

电荷密度和电流（回顾）



$$I = Q \cdot v$$

电流=每秒流过的电荷=电子每秒运动的距离*单位长度的电荷

- 电子从源到漏运动形成的电流，与沟道内电荷密度、电子运动的速度相关；

5.1.4. **Applying a Small v_{DS}**

- **Q:** For small values of v_{DS}, how does one calculate i_{DS} (aka. i_D)? **A:** Equation (5.7)…
- **Q:** What is the origin of this equation?
  - **A:** Current is defined in terms of **charge per unit length of *n*-channel** as well as **electron drift velocity.**

$$|Q| = C_{ox}(WL)v_{OV}$$

$$v_{n\text{-drift}} = -\mu_n E$$

μ_n represents mobility of electrons at surface of the n-channel in m^2/Vs

$$\text{(eq5.7)}\ i_D = \underbrace{(C_{ox}Wv_{OV})}_{\text{charge per unit length of } n\text{-channel in } C/m}\underbrace{\left(\frac{\mu_n v_{DS}}{L}\right)}_{\text{electron drift velocity in } m^2/Vs} \text{ in } A$$

单位长度电荷 移动速度

电流=每秒流过的电荷=电子每秒运动的距离*单位长度的电荷

5.1.4. Applying a Small v_{DS}

当$V_{GS}>V_t$（$V_{OV}>0$），且V_{DS}较小时，MOSFET等效为一个电阻，其值受有效电压V_{OV}的控制

- **Q:** What is observed from equation (5.7)?
  - **A:** For small values of v_{DS}, the *n*-channel acts like a variable resistance whose value is controlled by v_{OV}.
  - 当V_{DS}较小时，沟道可看成一个压控电阻

(eq5.7) $$i_D = \left[(\mu_n C_{ox}) \frac{W}{L} v_{OV} \right] v_{DS} \quad \text{in } A$$

电阻的电导计算：

$$g_{DS} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) v_{OV}$$

电导和电阻

(eq5.8a) $$r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{\underbrace{(\mu_n C_{ox})}_{\text{process transconductance parameter}} \left(\frac{W}{L} \right) v_{OV}} \quad \text{in } \Omega$$

aspect ratio

W/L是一个设计参数。只要比值一样，大多数性能都是一样的

5.1.4. **Applying a Small v_{DS}**

Note that this is one **VERY IMPORTANT** equation in Chapter 5.

m equation (5.7)?

v_{DS}, the *n*-channel acts like a

hose value is controlled by v_{OV}.

(eq5.7) $$i_D = \left[\left(\mu_n C_{ox} \right) \frac{W}{L} v_{OV} \right] v_{DS} \text{ in } A$$

适用的前提是Vds差很小，化Vd基本为0

(eq5.8a) $$r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{\underbrace{\left(\mu_n C_{ox} \right)}_{\substack{\text{process} \\ \text{transconductance} \\ \text{parameter}}} \underbrace{\left(\frac{W}{L} \right)}_{\substack{\text{aspect} \\ \text{ratio}}} v_{OV}} \text{ in } \Omega$$

5.1.4. **Applying a Small v_{DS}**

K_n' 和 k_n 是两个常用参数，不要混淆

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right) v_{OV}$$

- **Q:** What three factors is r_{DS} dependent on?
  - **A: process transconductance parameter for NMOS** ($k_n' = \mu_n C_{ox}$) – which is determined by the manufacturing process 工艺决定
  - **A: aspect ratio** (W/L) – which is dependent on size requirements / allocations 设计师决定，L_{min}代表工艺
  - **A: overdrive voltage** (v_{OV}) – which is applied by the user
  - **MOSFET transconductance parameter** $k_n = k_n' * W/L$

阶段性结论1：当V_{DS}极小时，MOSFET等效为一个压控电阻，i_D和V_{DS}呈线性关系

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)}$$

k_n is known as **NMOS-FET transconductance parameter** and is defined as $\mu_n C_{ox} W/L$

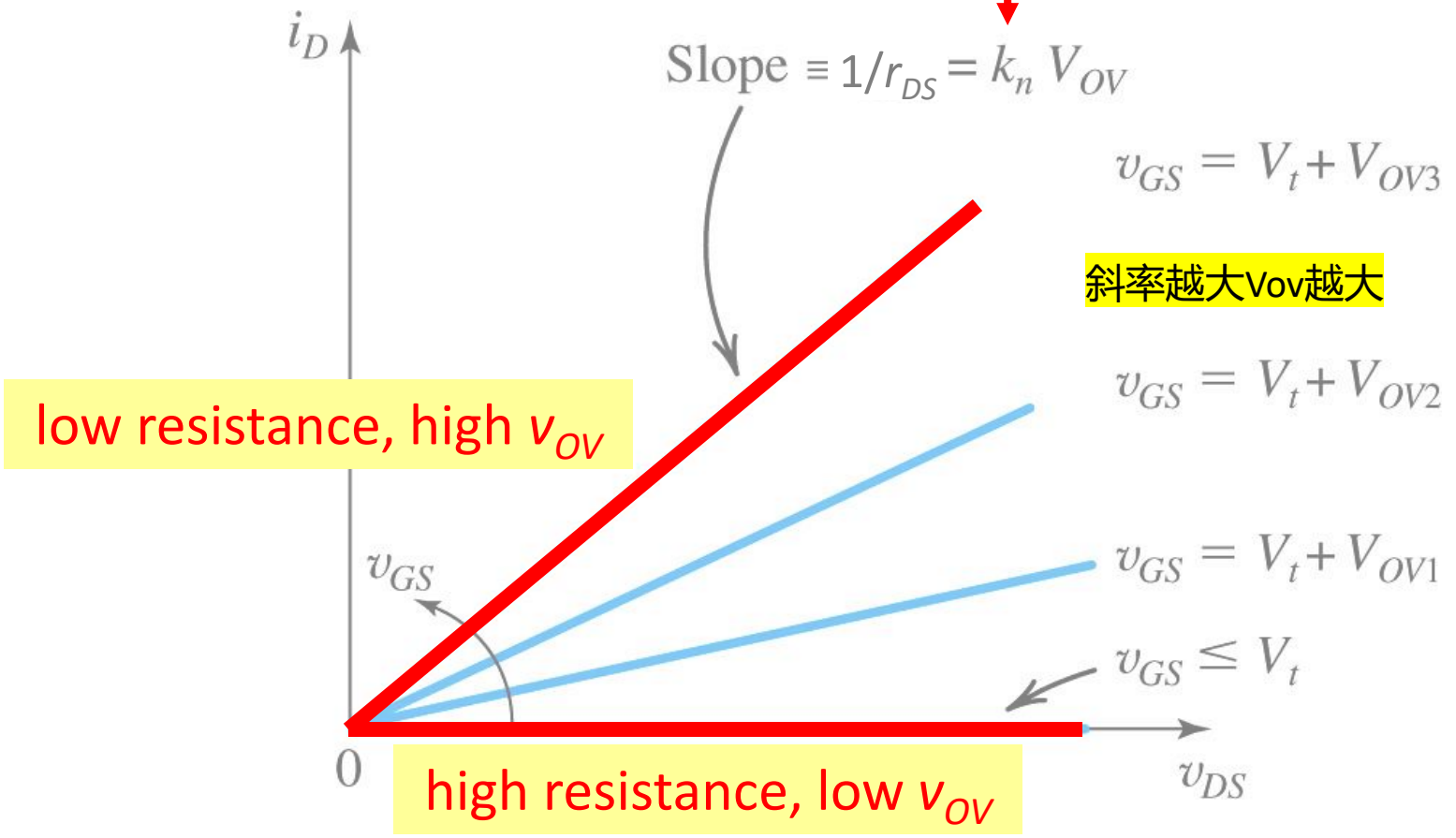
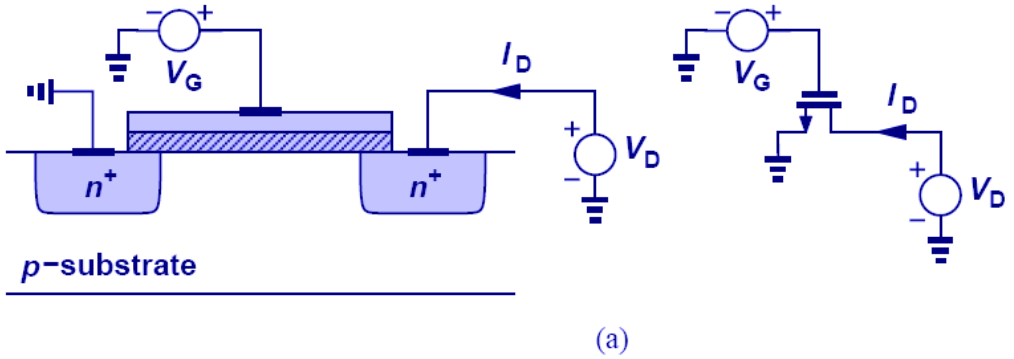
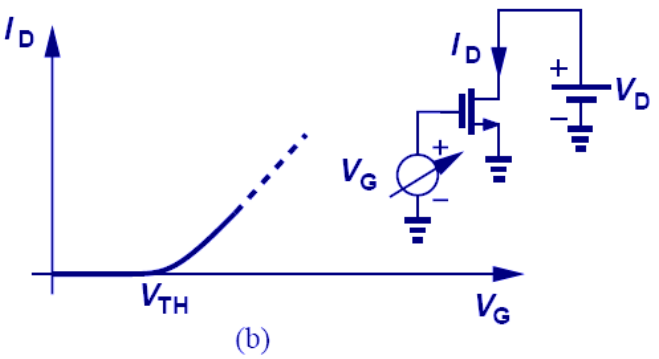
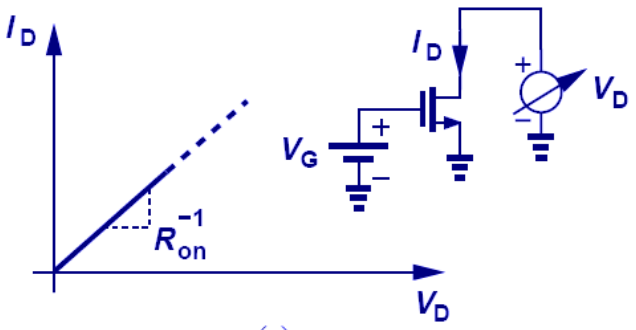


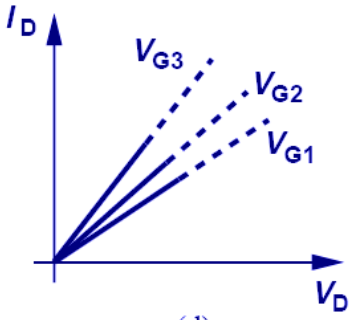
Figure 5.4: The i_D-v_{DS} characteristics of the MOSFET in Figure 5.3. when the voltage applied between drain and source V_{DS} is kept small.

MOSFET 特性







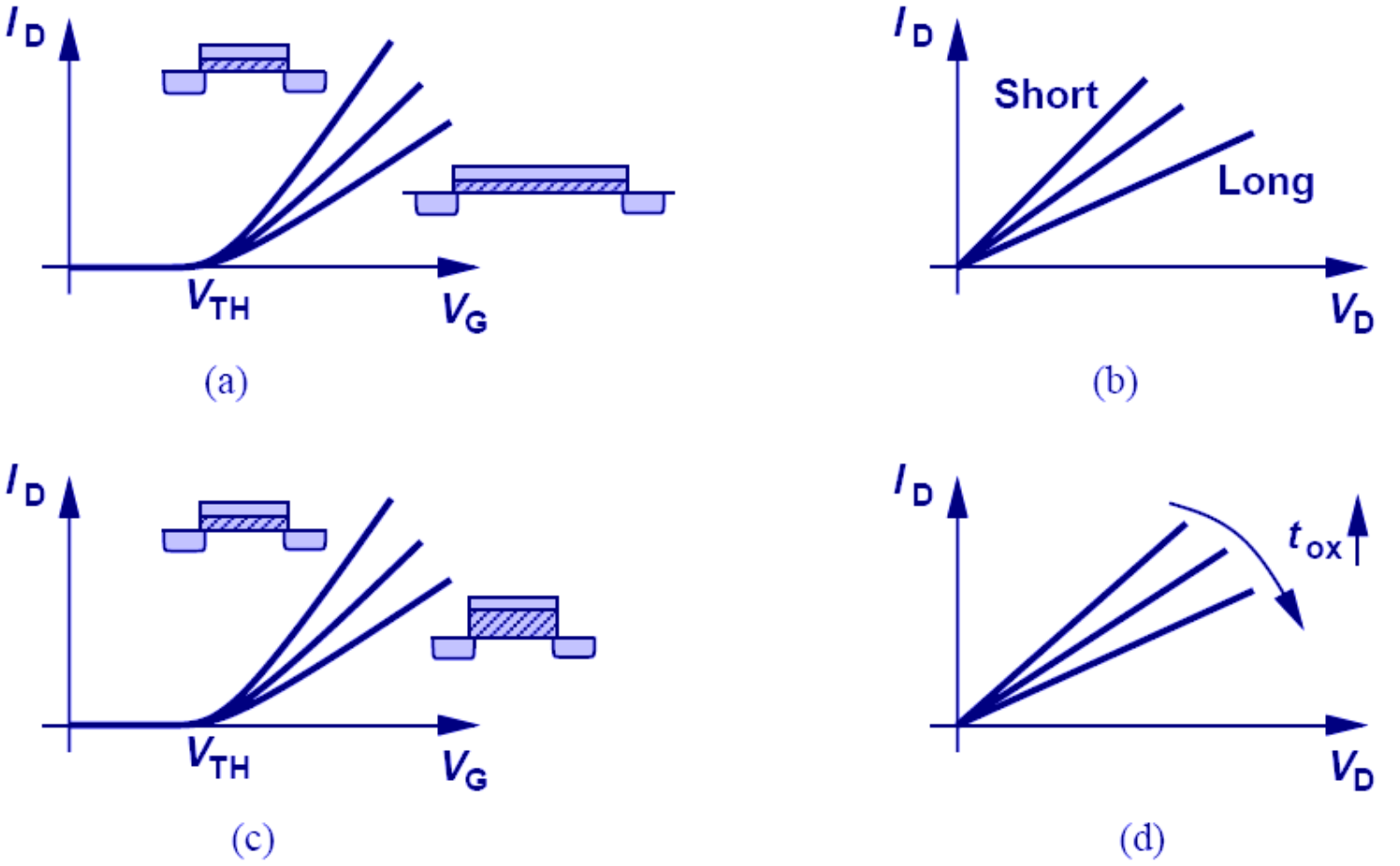


- MOSFET三端器件，有两个施加电压V_{GS}、V_{DS}，一个响应电流I_{DS}，因此，表征MOSFET“电压电流约束关系”的方法有
  - (b) 固定 V_D 测量 I_D vs. V_G（转移特性）；
  - (c) 固定 V_G 测量 I_D vs. V_D（输出特性）；
- (d) 显示了栅极电压对沟道电阻的影响；
- MOSFET 的输入特性：无栅极电流，输入阻抗∞

沟道长度 L 和 栅氧厚度 t_{ox} 的影响

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)}$$

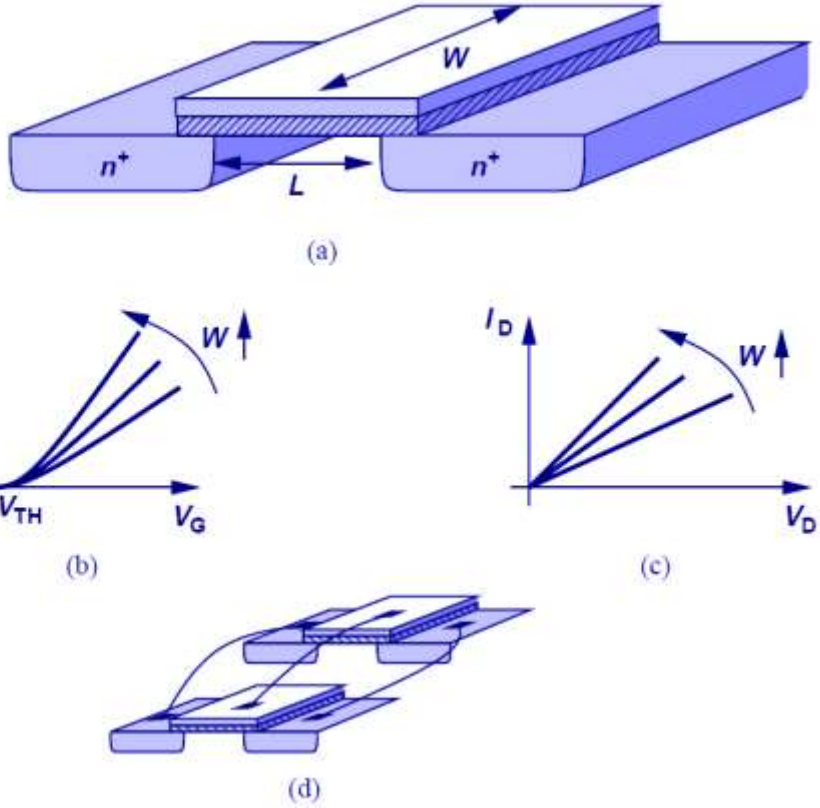
固定V_{GS}、V_{DS}，分析L和t_{ox}对沟道电导的影响



- 短的沟道长度和薄的栅氧厚度可以降低沟道电阻（为何？），从而导致漏极电流的增加

沟道宽度 W 的影响

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)}$$

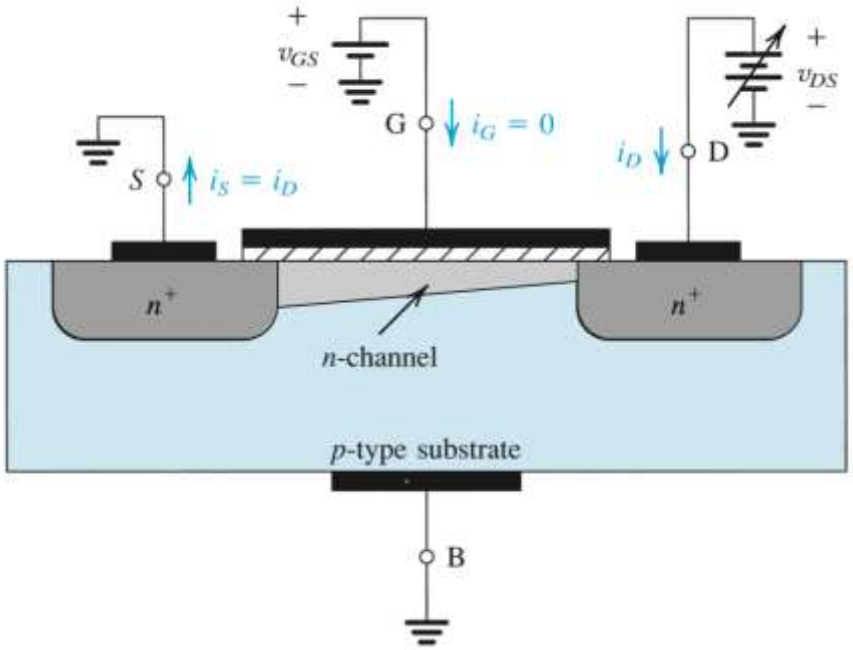


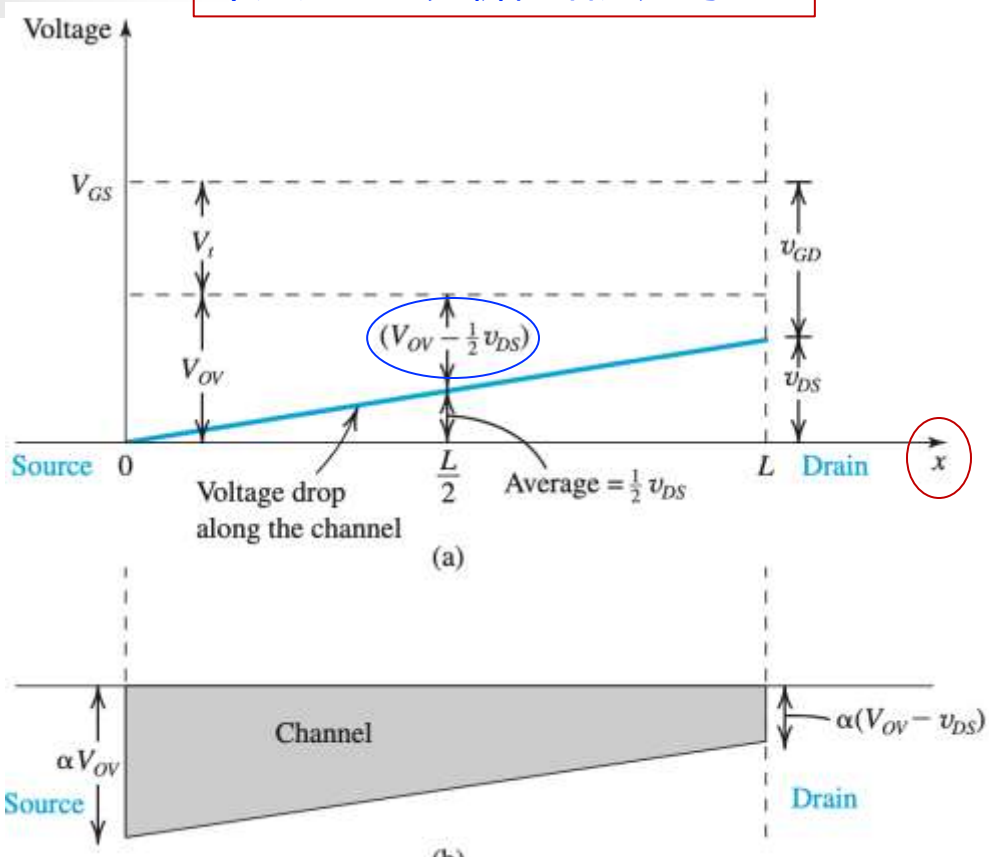
- 沟道宽度增加 → 沟道电阻降低 → 漏极电流增加；但是，沟道宽度增加的同时，栅氧电容值也随之增加，这会限制电路的速度；
- 沟道宽度的增加可看作两个器件的并联；

5.1.5. Operation as v_{DS} is Increased

接下来考虑情况2：V_{DS}逐渐增大时…

不太严谨的分析，结论是对的





沟道深度与V_{GX}相关，0 < x < L

均匀沟道（v_{DS}=0）内的电荷量 $|Q| = C_{ox}(WL)v_{OV}$ $i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)v_{OV}\right]v_{DS}$

锥形沟道（图中没有画出W）内的电荷量：有效电压用平均值替代

$$i_D = k_n'\left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

5.1.5. Operation as v_{DS} is Increased

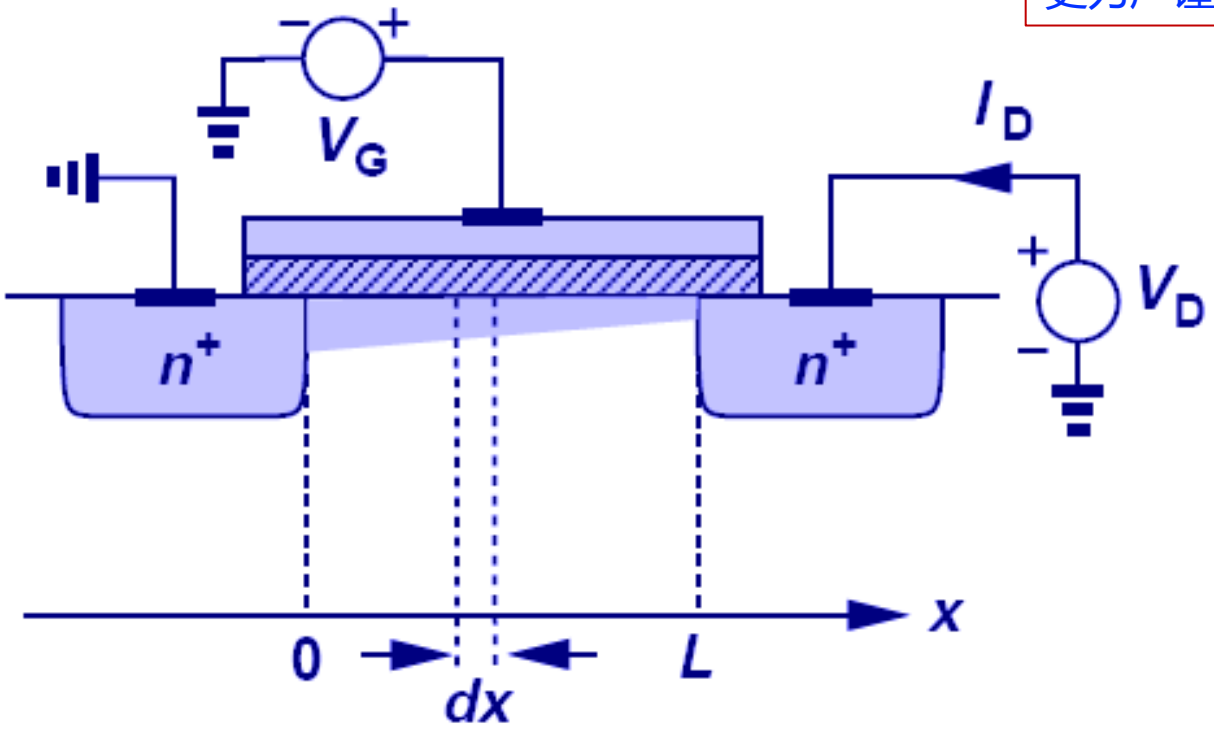
接下来考虑情况2：V_{DS}逐渐增大时…

- **Q:** What happens to i_D when v_{DS} increases beyond "small values"?
  - **A:** The relationship between them ceases to be linear.
- **Q:** How can this non-linearity be explained?
  - **step #1:** Assume that v_{GS} is held constant at value greater than V_t.
  - **step #2:** Also assume that v_{DS} is applied and appears as voltage drop across *n*-channel.
  - **step #3:** Note that voltage decreases from v_{GS} at the source end of channel to v_{GD} at drain end, where…
    - $v_{GD} = v_{GS} - v_{DS}$
    - $v_{GD} = V_t + v_{OV} - v_{DS}$

当V_{DS}逐渐增大时，沟道内的电位从S到D逐渐增加，因此，G与沟道的电位差从S端的V_{GS}逐渐减小到D端的V_{GD}

沟道内某一点的电荷密度

更为严谨的分析



- 令 x 为沟道内源和漏之间的一点， V(x) 为该点的电势; 那么该点的电荷密度（单位长度内的电荷）为：

$$Q(x) = WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right] \qquad \text{(C/μm)}$$

栅极与x点的电势差

漏极电流

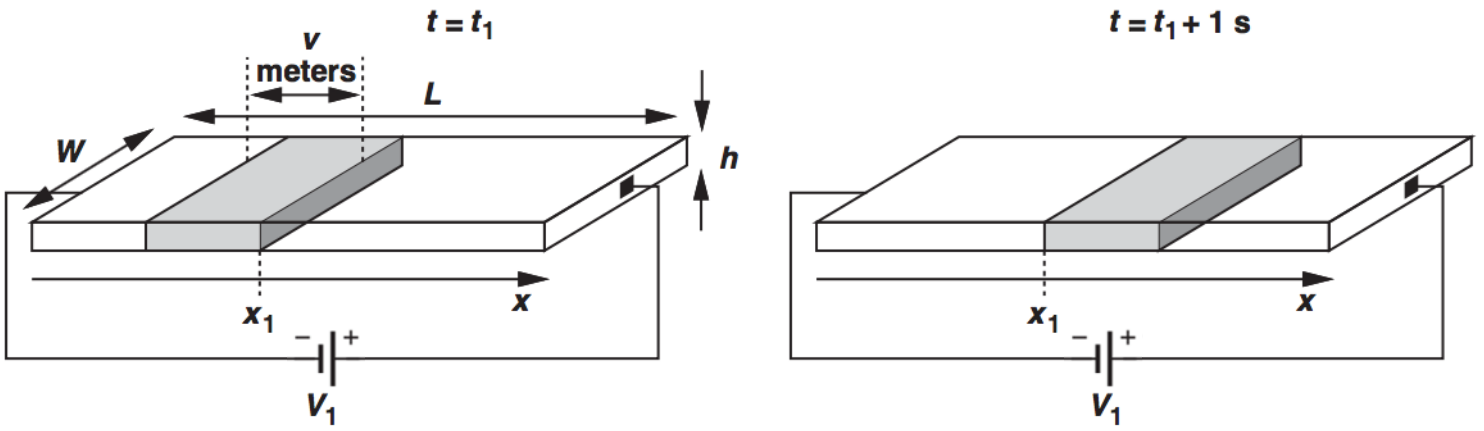


Figure 6.15 Relationship between charge velocity and current.

As explained in Chapter 2,

$$v = -\mu_n E, \tag{6.5}$$

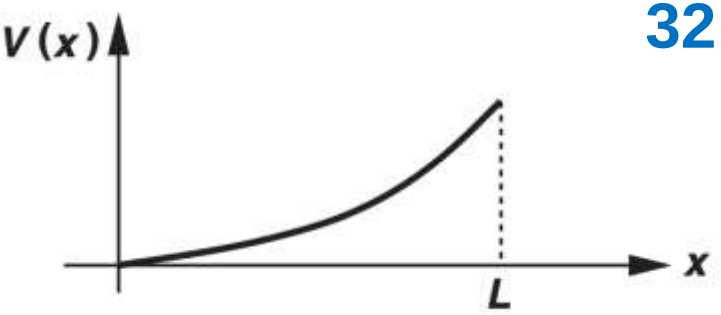
$$= +\mu_n \frac{dV}{dx}, \tag{6.6}$$

where dV/dx denotes the derivative of the voltage at a given point. Combining Eqs. (6.3), (6.4), and (6.6), we obtain

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}. \tag{6.7}$$

单位长度内的电荷　电子运动速度

漏极电流



$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}. \tag{6.7}$$

沟道内电势的导数不是常数

Interestingly, since I_D must remain constant along the channel (why?), $V(x)$ and dV/dx must vary such that the product of $V_{GS} - V(x) - V_{TH}$ and dV/dx is independent of x.

While it is possible to solve the above differential equation to obtain $V(x)$ in terms of I_D (and the reader is encouraged to do that), our immediate need is to find an expression for I_D in terms of the terminal voltages. To this end, we write

$$\int_{x=0}^{x=L} I_D\, dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n C_{ox} W[V_{GS} - V(x) - V_{TH}]\, dV. \tag{6.8}$$

That is,

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right]. \tag{6.9}$$

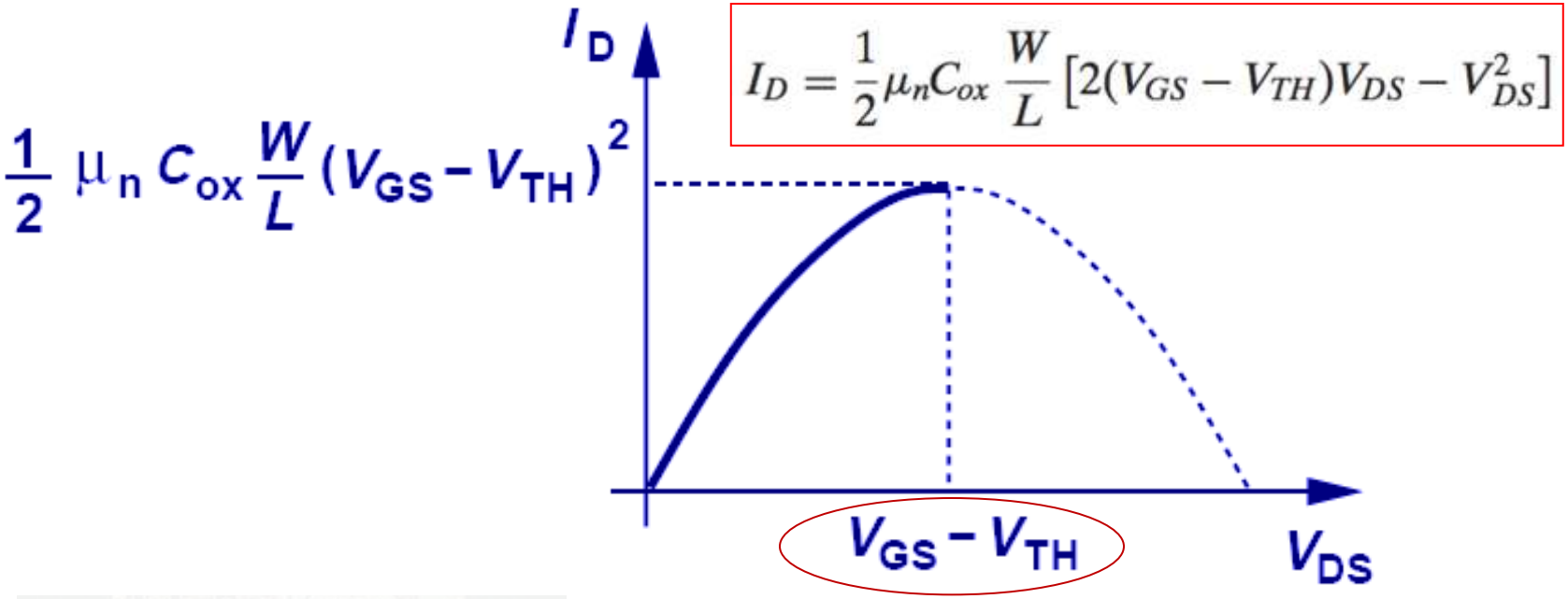
注意：该结论其实包含了我们的阶段性结论1。当V_{DS}很小时，两次项可以忽略

I_D-V_{DS} 抛物线关系

阶段性结论1：当V_{DS}极小时，MOSFET等效为一个压控电阻，i_D和V_{DS}呈线性关系

阶段性结论2：当V_{DS}较小时，MOSFET的i_D和V_{DS}呈抛物线关系

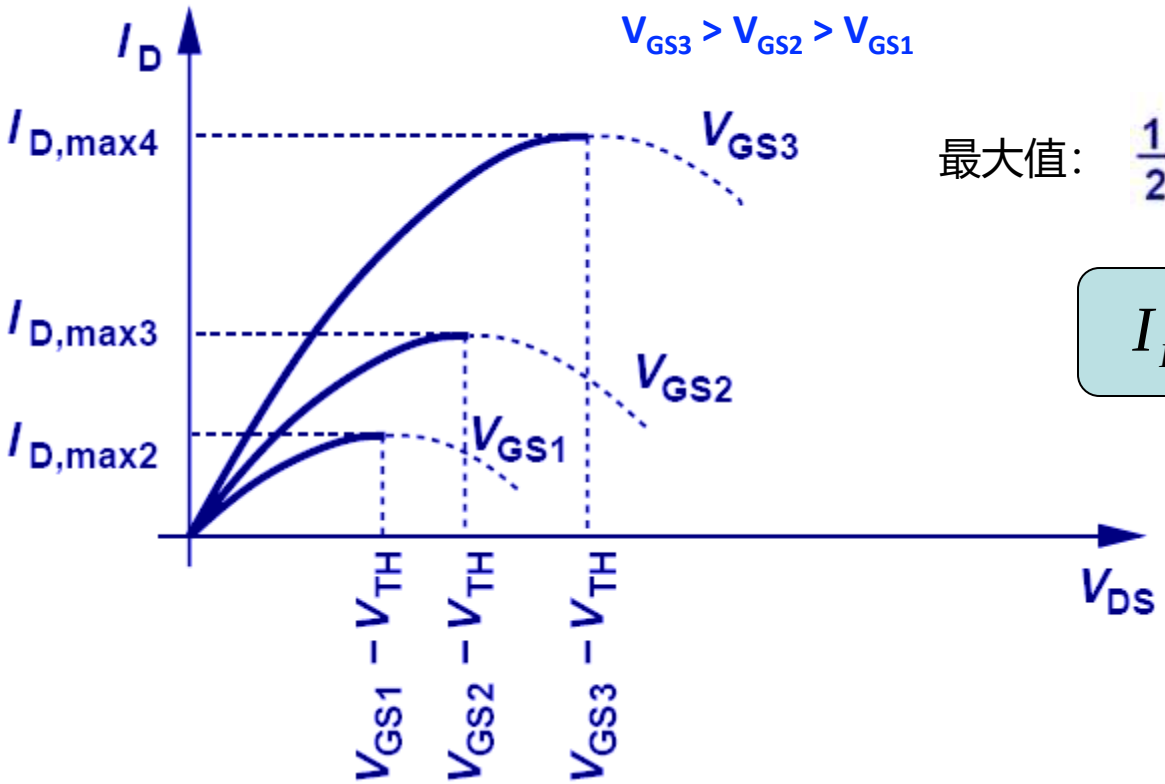
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]$$



- 若固定 V_G，观察 I_D vs.V_{DS}, 则 I_D 和 V_{DS} 呈抛物线关系.
- 当 $V_{DS} = V_{GS} - V_{TH} = V_{OV}$ 时， I_D 达到最大值

Vgs增加，抛物线发生变化

不同 V_{GS} 值对I_D-V_{DS}的影响



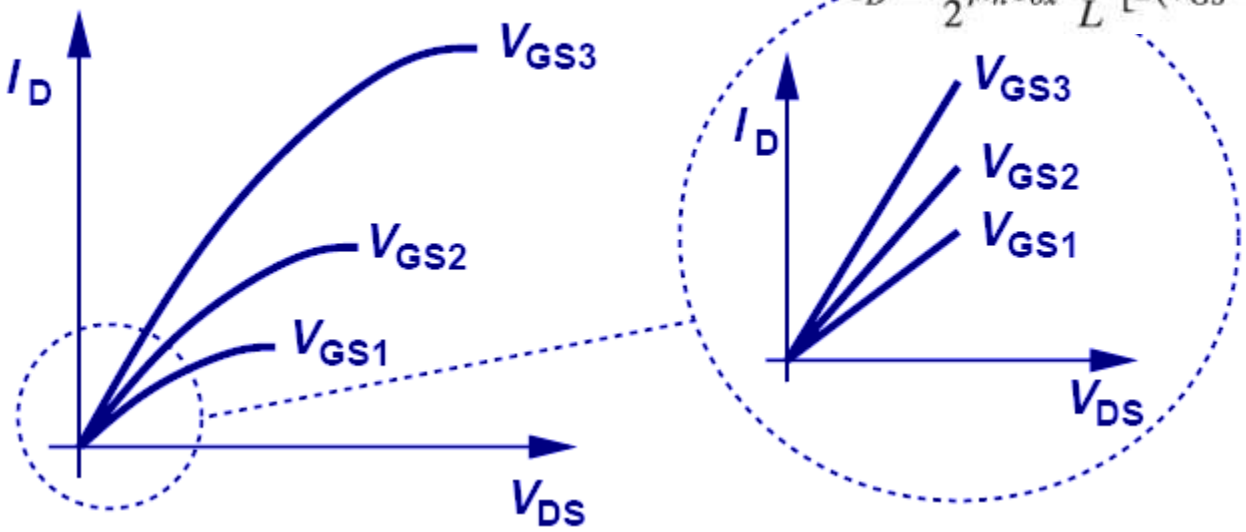
$V_{GS3} > V_{GS2} > V_{GS1}$

最大值：$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$

$$I_{D,\max} \propto (V_{GS} - V_{TH})^2$$

线性电阻

阶段性结论1（线性电阻）是阶段性结论2（抛物线）的特殊情况



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]$$

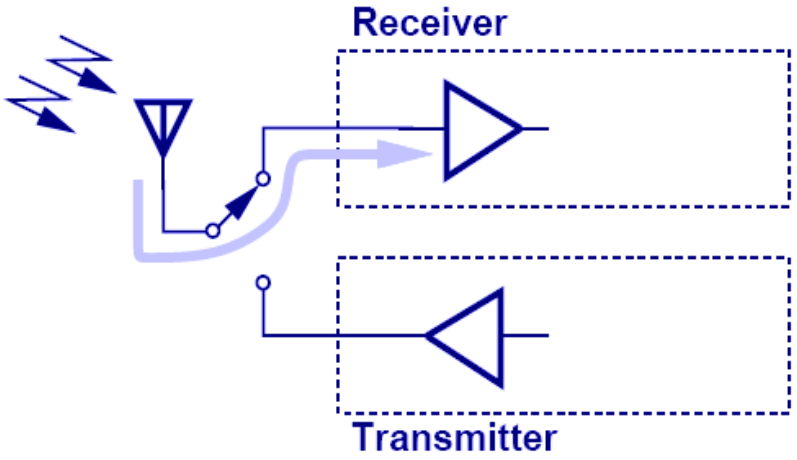
The nonlinear relationship between I_D and V_{DS} reveals that the transistor *cannot* generally be modeled as a simple linear resistor. However, if $V_{DS} \ll 2(V_{GS}-V_{TH})$, Eq. (6.9) reduces to:

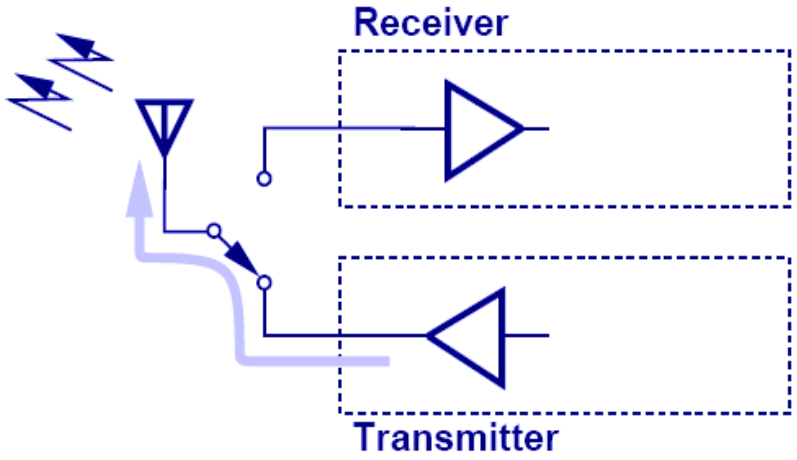
$$I_D \approx \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})V_{DS}, \qquad (6.11)$$

- 当 V_{DS} 比较小时, 可看作一电阻, 其阻值受栅极电压控制
- 应用：无线收发机的开关（switch）

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$$

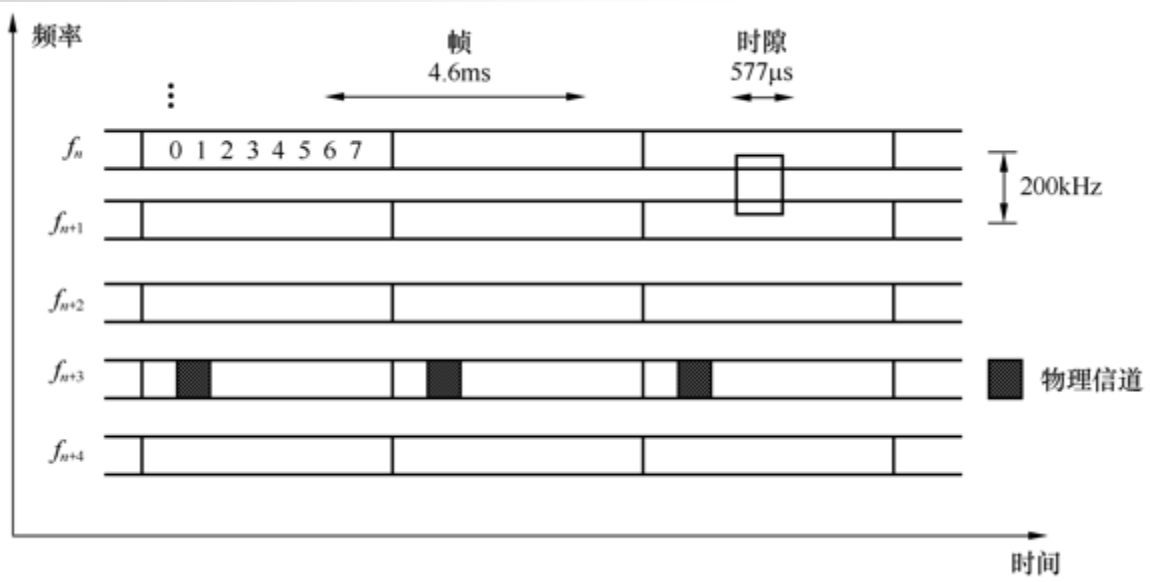
应用





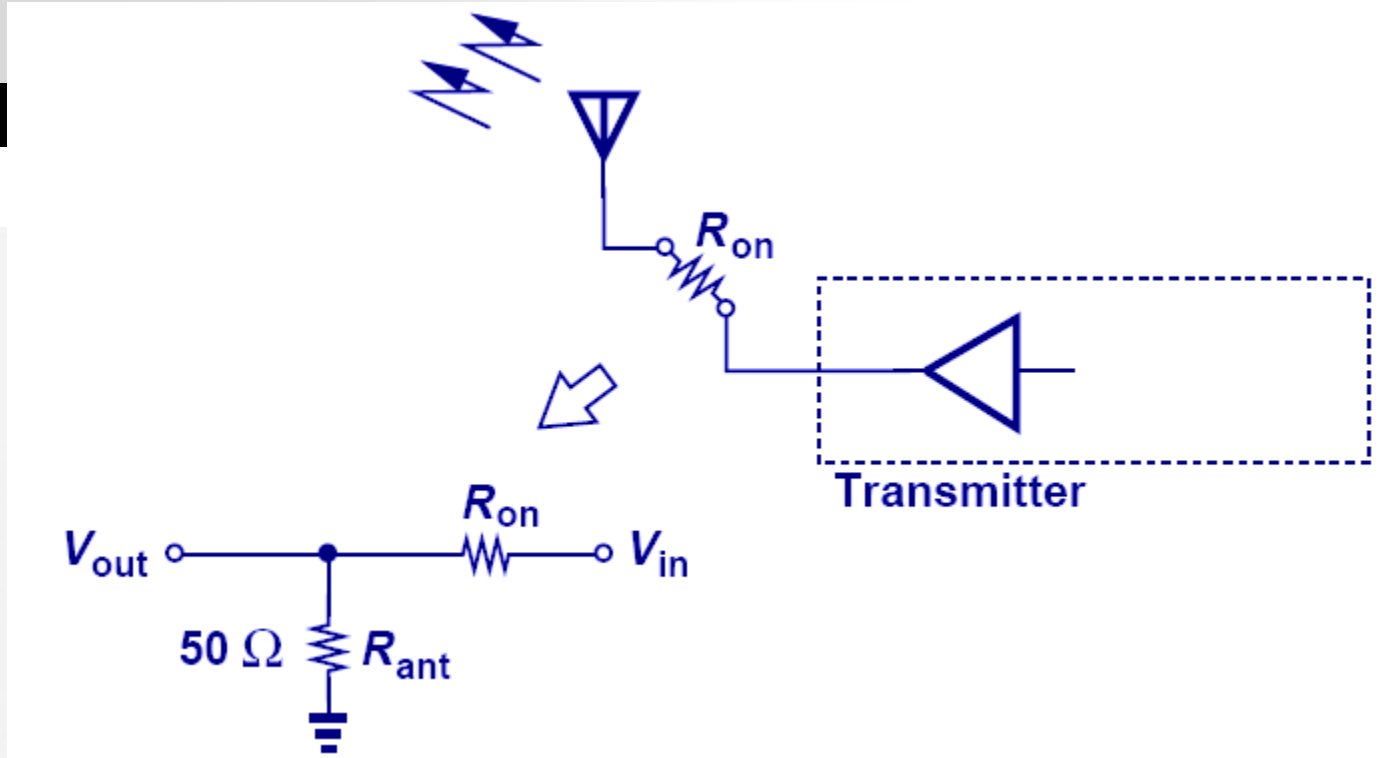
- 时分多址（TDMA）

GSM 的 TDMA/FDMA 接入方式



- GSM蜂窝系统采用时分多址、频分多址和频分双工（TDMA/FDMA/FDD）制式。
- 在25MHz的频段中共分125个频道，频道间隔200kHz。每载波含8个（以后可扩展为16个）时隙，时隙宽为0.577ms。
- 8个时隙构成一个TDMA帧，帧长为4.615ms，如图7-7所示。

开启电阻的影响



- 为了使信号衰减最小, 开关的开启电阻 （R_{on}）应尽可能小. 这意味着大的 W/L 或大的 V_{GS}.

Example 6.5

In the cordless phone of Example 6.4, the switch connecting the transmitter to the antenna must negligibly attenuate the signal, e.g., by no more than 10%. If $V_{DD} = 1.8\,\text{V}$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, and $V_{TH} = 0.4\,\text{V}$, determine the minimum required aspect ratio of the switch. Assume the antenna can be modeled as a 50-Ω resistor.

Solution As depicted in Fig. 6.20, we wish to ensure

$$\frac{V_{out}}{V_{in}} \geq 0.9 \tag{6.13}$$

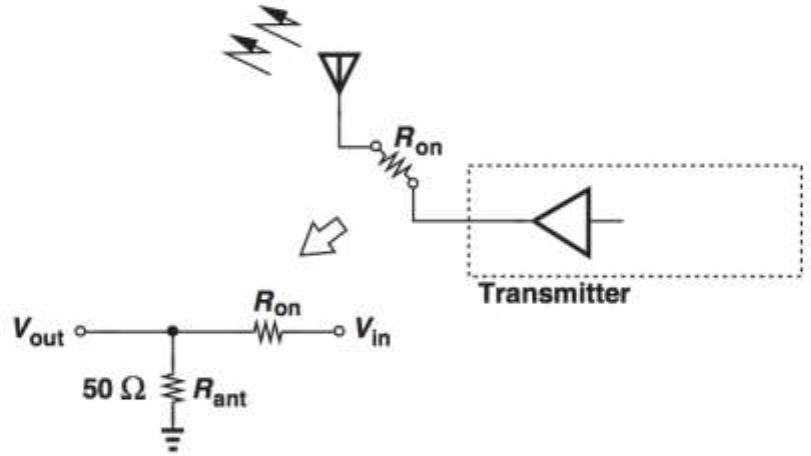


Figure 6.20 Signal degradation due to on-resistance of antenna switch.

and hence

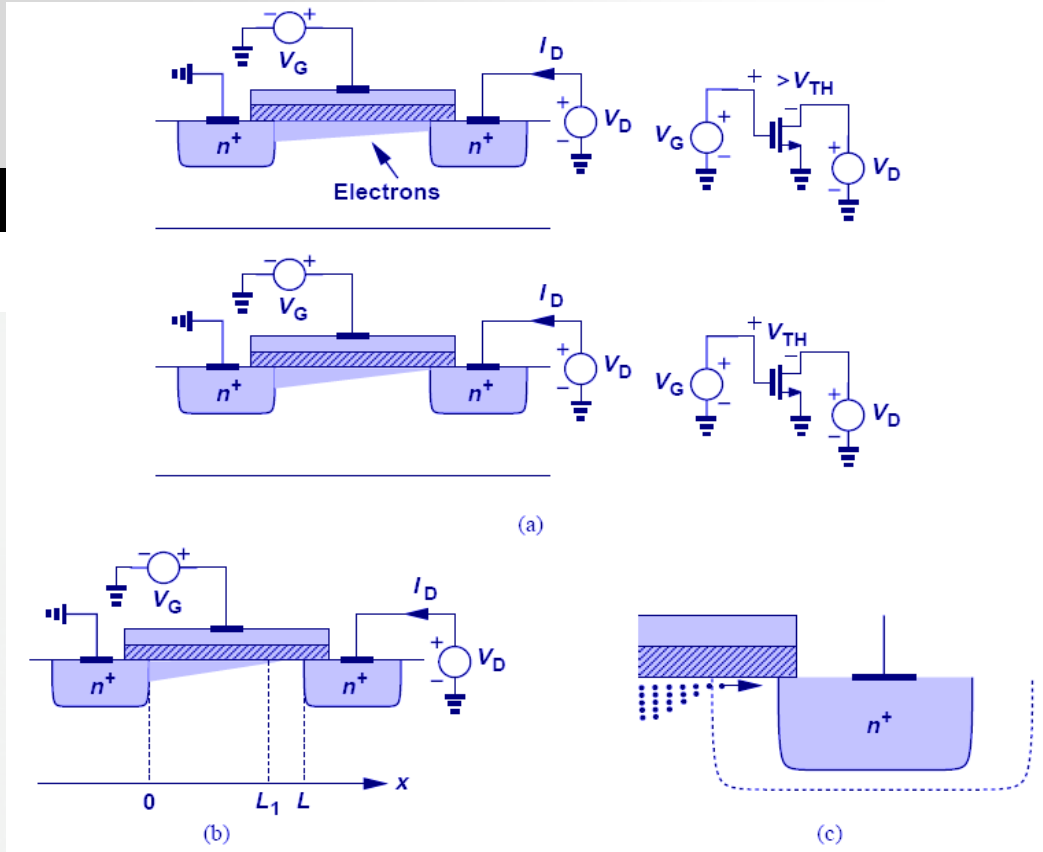
$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)}$$

$$R_{on} \leq 5.6\,\Omega. \tag{6.14}$$

Setting V_{GS} to the maximum value, V_{DD}, we obtain from Eq. (6.12),

$$\frac{W}{L} \geq 1276. \tag{6.15}$$

沟道夹断（Channel Pinch-Off）



思考1：夹断点左移后，电子在L_1和L点之间是如何运动的？

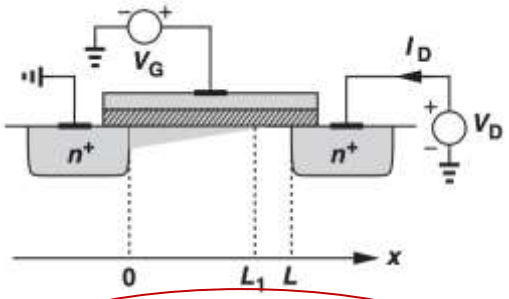
A: (c)到达耗尽区边缘的电子被迅速扫到漏极

思考2：夹断后的电流I_D等于多少？

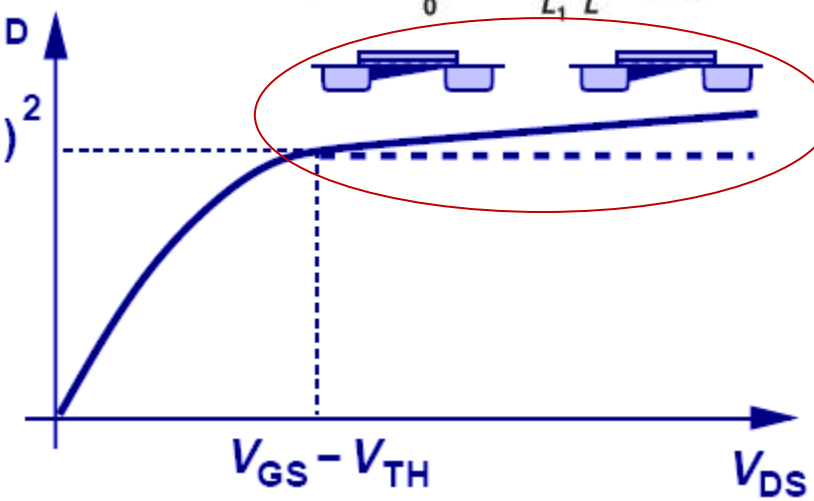
A: 耗尽区的电场强度不影响电流。电流I_D与“沟道长度为L_1，D处刚好夹断（$V_{DS}=V_{OV}$）”的情形一致

- 当漏极电压从零开始逐渐增加时，V_G-V_D逐渐减小，当V_G-V_D小到一定程度，不足以使漏极附近的衬底反型时，漏极处的沟道就消失了，我们称之为“沟道在此处夹断”；
- 令反型所需的栅极与衬底之间的电压差为V_{th}（阈值电压），那么，当$V_G - V_D = V_{th}$时，漏极处的沟道开始夹断；当V_D继续增加，$V_G - V_D < V_{th}$，源和漏之间必定有一点（L_1），其电势比V_G刚好低V_{th}，L_1即新的夹断点，也即沟道变短

沟道长度调制



$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$$



电压控制电流源

沟道夹断后，L需用有效的沟道长度L_1替代，L_1与V_{DS}相关

L_1是L的修正：

$$1+\lambda(v_{DS}-v_{OV})$$

简化为：

$$(1+\lambda v_{DS})$$

$$I_D=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

用来调整影响

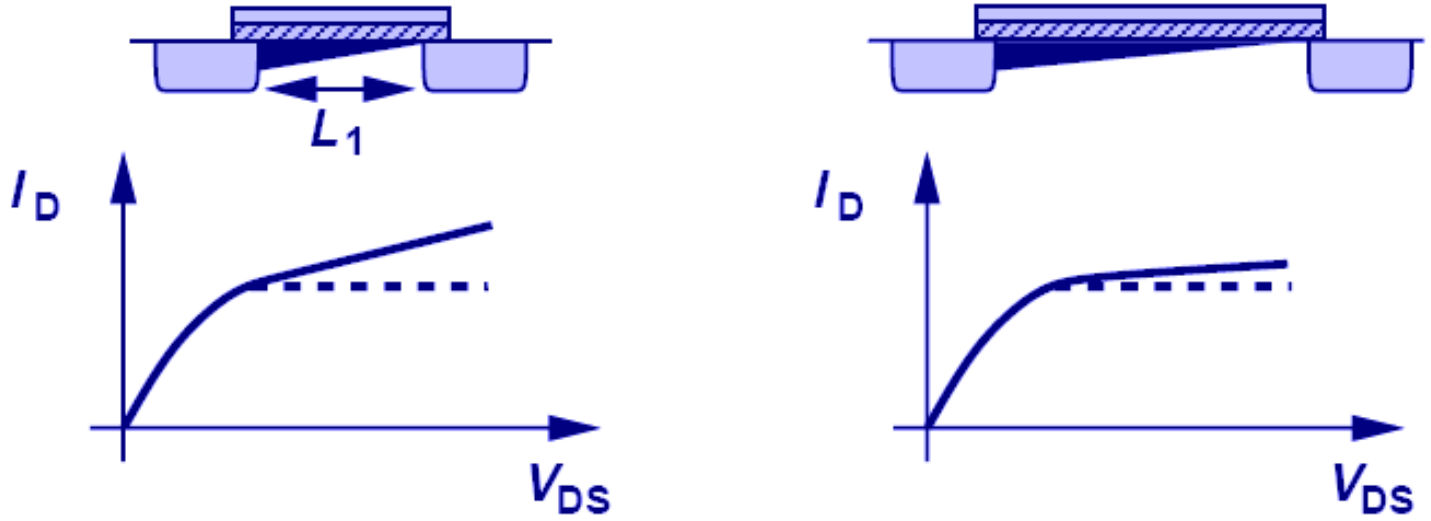
L_1

沟道长度调制系数

图中红色区域

- V_{DS}增加 → 沟道长度减小 → 电流增加
- 沟道越短，沟道调制效应越明显，越先进的工艺影响越大
- 初步分析时（特别是对于L较大的长沟道器件），可忽略沟道调制效应 → 当$V_{DS}>V_{OV}$时，电流I_D保持恒定

λ 和 L 的影响



- 沟道L越短，沟道调制效应越明显

沟道调制效应

延长线交于一点

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS}-V_{tn})^2(1+\lambda v_{DS})$$

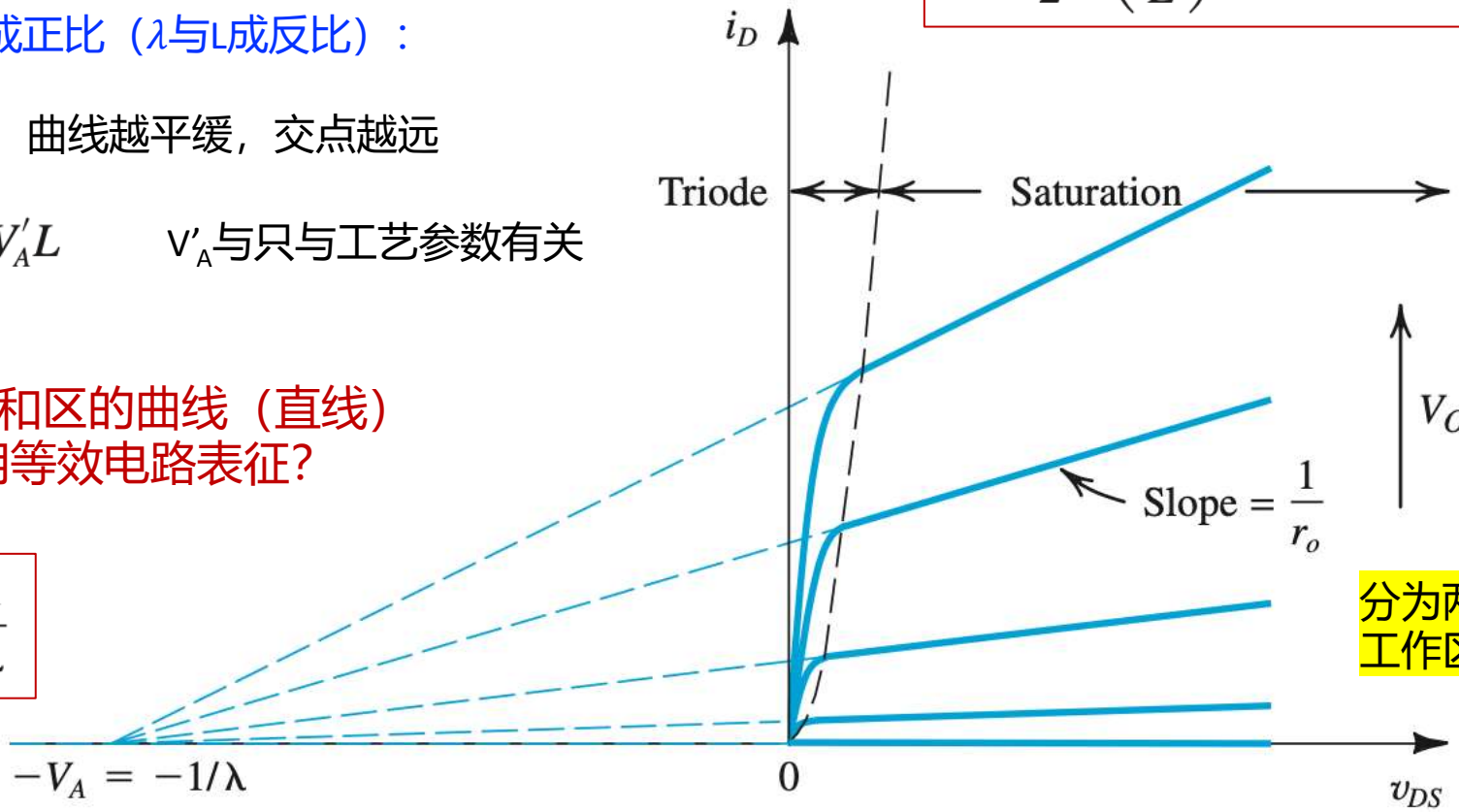
V_A与L成正比（λ与L成反比）：

L越大，曲线越平缓，交点越远

$V_A = V_A'L$　　V'_A与只与工艺参数有关

Q：饱和区的曲线（直线）如何用等效电路表征？

$$V_A = \frac{1}{\lambda}$$



分为两个工作区

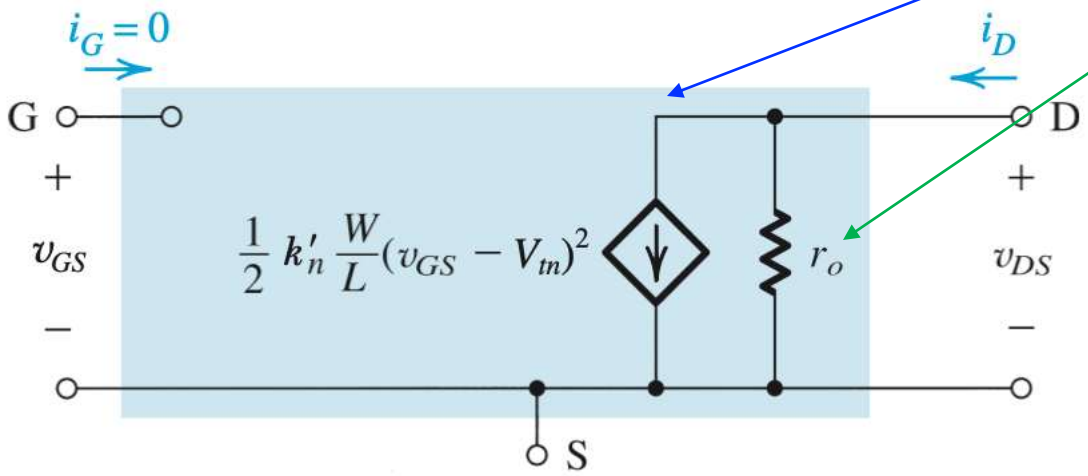
Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

意思范围普遍适用

L很长即不考虑1+.....

饱和区大信号等效电路模型

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS}-V_{tn})^2(1+\lambda v_{DS})$$



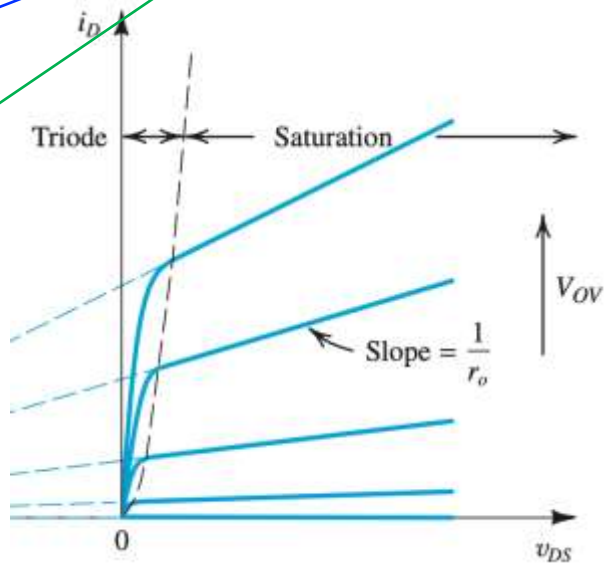
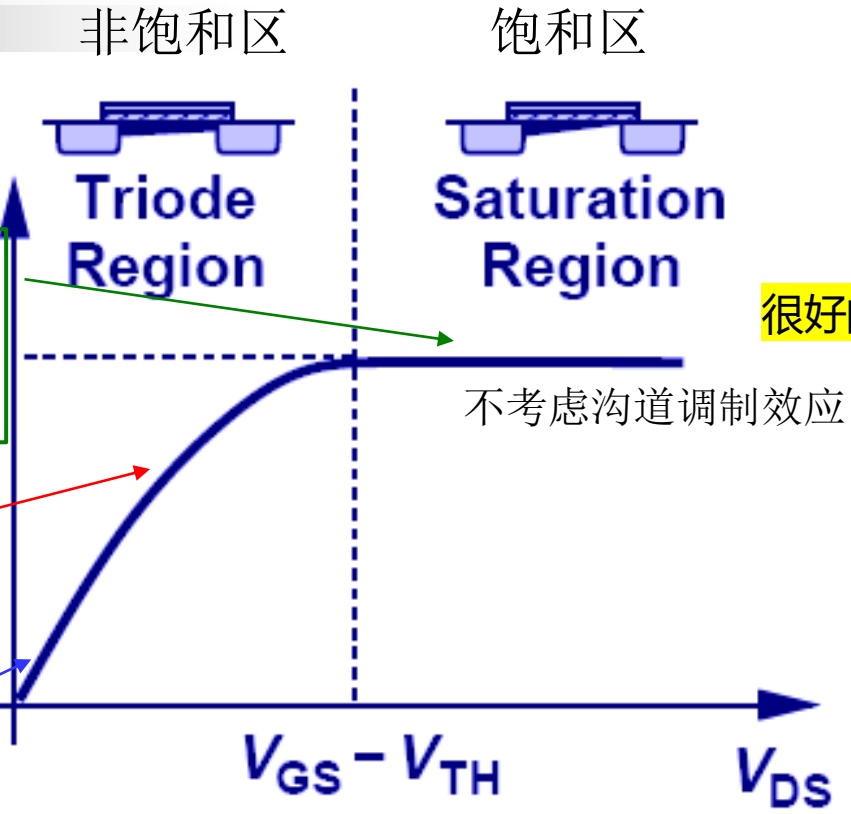


Figure 5.18 Large-signal, equivalent-circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (5.27).

$$r_o = \frac{V_A}{I_D'}$$

$$I_D' = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_{tn})^2$$

不同的工作区域



$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$$

很好的恒流源

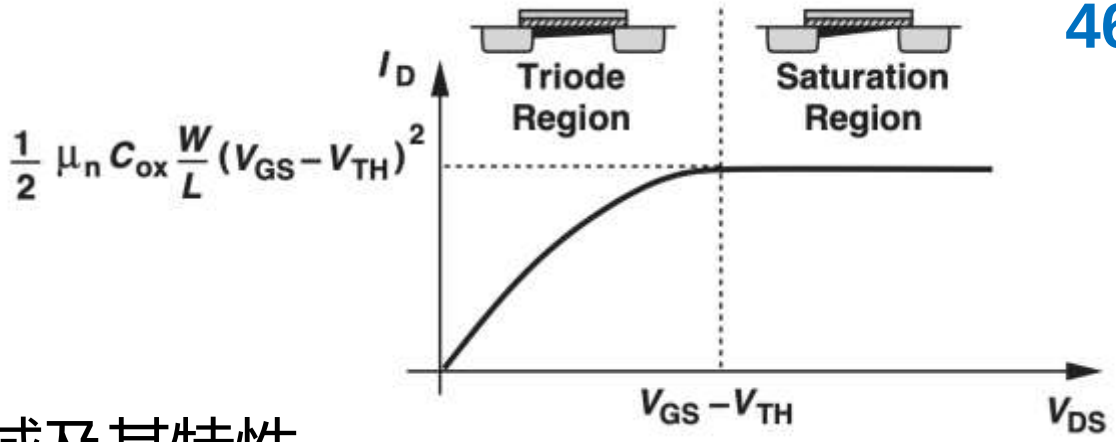
不考虑沟道调制效应

$$I_D=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]$$

(eq5.7) $i_D=\left[(\mu_n C_{ox})\frac{W}{L}v_{OV}\right]v_{DS}$ in A

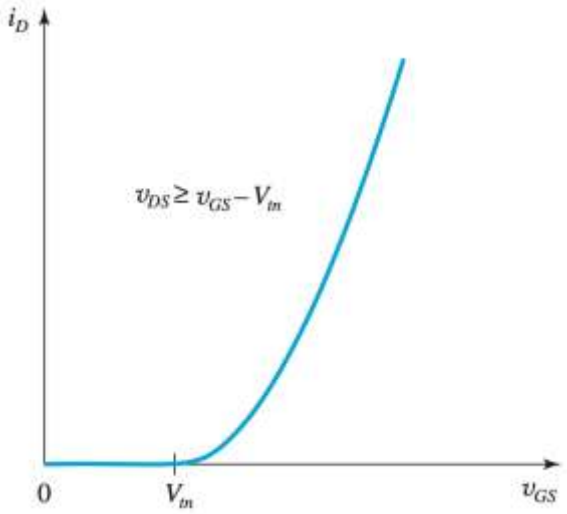
(eq5.8a) $r_{DS}=\frac{v_{DS}}{i_D}=\frac{1}{\underbrace{(\mu_n C_{ox})}_{\text{process transconductance parameter}}\left(\frac{W}{L}\right)_{\text{aspect ratio}}v_{OV}}$ in Ω

小结



$V_{OV} = V_{GS} - V_{TH}$

- 增强型NMOS的工作区域及其特性
  - 饱和区 $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$
  - 饱和区，考虑沟道调制效应 $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$
  - 非饱和区 $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]$
  - 非饱和区，V_{DS}很小时 $R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$



- 熟练掌握转移特性和输出特性的曲线及关键坐标点

作业

5.1 A 0.18-μm fabrication process is specified to have $t_{ox} = 4$ nm, $\mu_n = 450\ \text{cm}^2/\text{V}\cdot\text{s}$, and $V_t = 0.5$ V. Find the value of the process transconductance parameter k_n'. For a MOSFET with minimum length fabricated in this process, find the required value of W so that the device exhibits a channel resistance r_{DS} of 1 kΩ at $v_{GS} = 1$ V.

Ans. 388 μA/V^2; 0.93 μm

5.2 For a 65-nm process technology for which $t_{ox} = 1.4$ nm, $\mu_n = 216\ \text{cm}^2/\text{V}\cdot\text{s}$, and $V_t = 0.35$ V, find C_{ox}, k_n', and the values of v_{OV} and v_{GS} required to operate a transistor having $W/L = 10$ in saturation with $i_D = 50$ μA. What is the minimum value of v_{DS} needed?

Ans. 24.6 fF/μm^2; 531 μA/V^2; 0.14 V; 0.49 V; 0.14 V

5.6 An NMOS transistor is fabricated in a 0.18-μm process having $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$ and $V_A' = 5$ V/μm of channel length. If $L = 0.8$ μm and $W = 16$ μm, find V_A and λ. Find the value of i_D that results when the device is operated with an overdrive voltage $v_{OV} = 0.2$ V and $v_{DS} = 0.8$ V. Also, find the value of r_o at this operating point. If v_{DS} is increased by 1 V, what is the corresponding change in i_D?

Ans. 4 V; 0.25 V^{-1}; 192 μA; 25 kΩ; 40 μA