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Lecture 15 – MOSFET
场效应晶体管-part2

Chapter 5 from **Microelectronic Circuits** Text by Sedra and Smith

Oxford Publishing

不同的工作区域

沟道存在

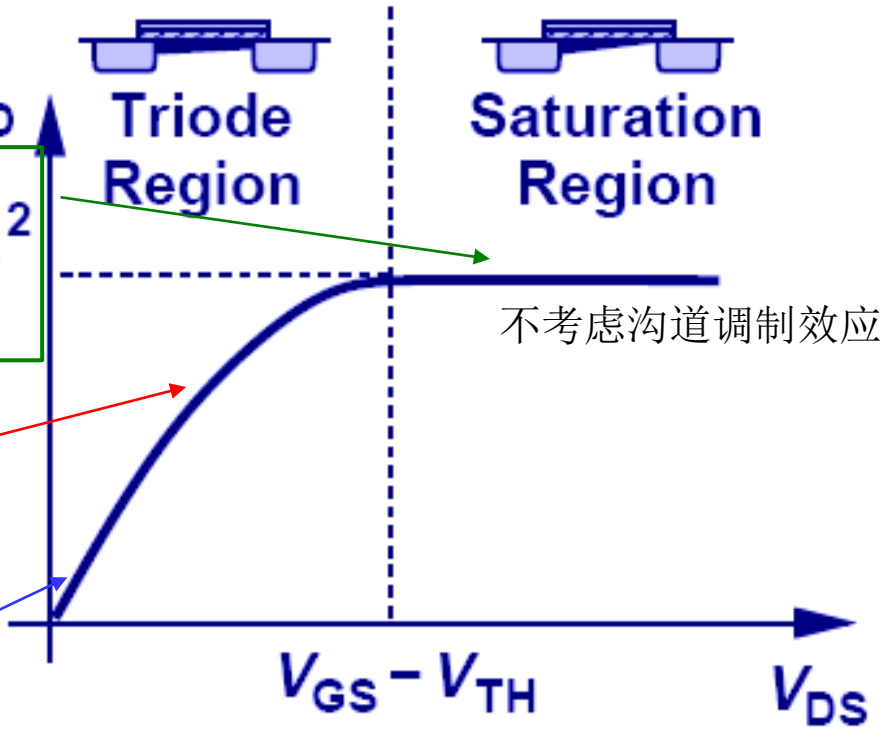
沟道减小，漏极沟道夹断

非饱和区　　饱和区

抛物线可以不记牢，但这个一定

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$$

$$I_D=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]$$

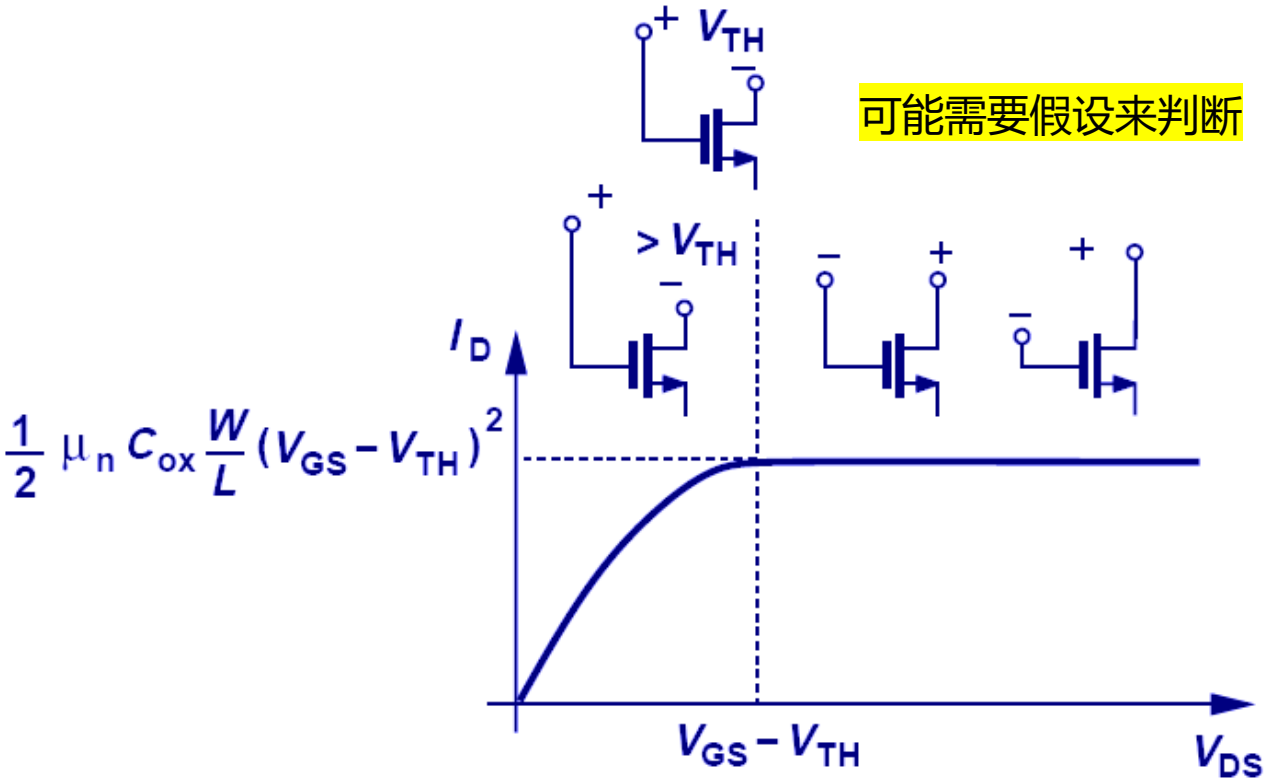


(eq5.7) $i_D=\left[(\mu_n C_{ox})\frac{W}{L}v_{OV}\right]v_{DS}$ in A

(eq5.8a) $r_{DS}=\frac{v_{DS}}{i_D}=\frac{1}{(\mu_n C_{ox})\left(\frac{W}{L}\right)v_{OV}}$ in Ω

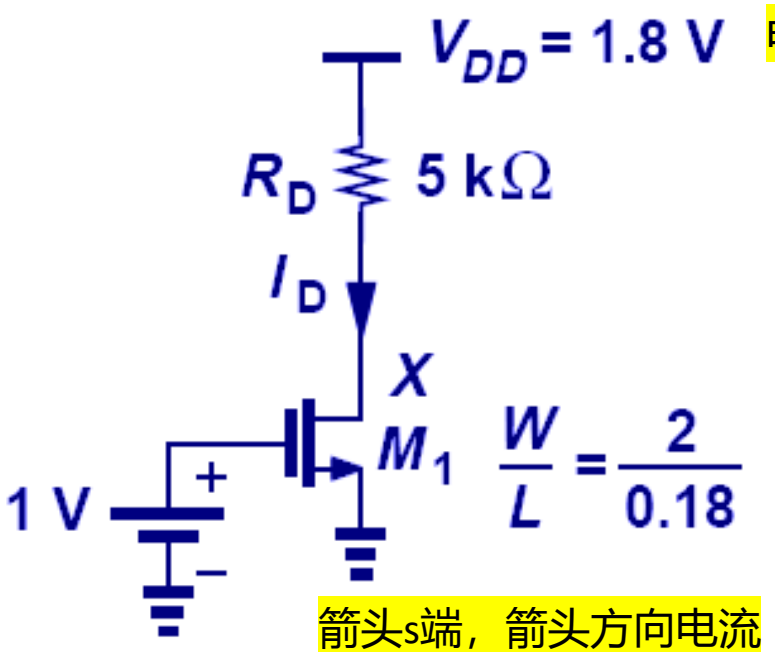
process transconductance parameter　aspect ratio

如何判断工作区域（很重要！）



- 方法一，从物理上理解：当V_G-V_D > V_{TH}时，漏极附近仍有沟道，MOSFET 工作在非饱和区；当V_D继续增加，导致V_G-V_D等于或小于 V_{TH}时，漏极附近无沟道（沟道夹断），MOSFET进入饱和区。
- 方法二，从符号上理解（电路分析中最有效），要使MOSFET工作在饱和区，V_D的下限为V_G-V_{TH}（参考电路图）；
- 方法三，记住这张图的横坐标，当$V_{DS} > V_{OV}$时，进入饱和区；

饱和区 还是 非饱和区?



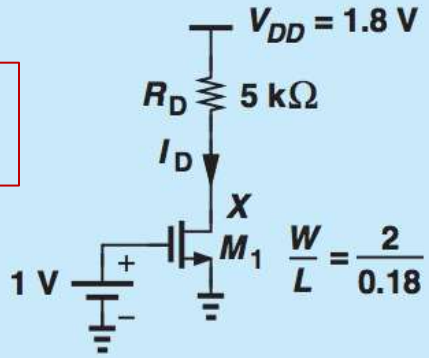
首先看Vgs，正常情况下1V够，所以开启。
2看是否饱和，看Vg和Vd关系，若Vg-Vd《Vth，则饱和。所以Vd有最小饱和工作电压。上限为Vdd，不能大于电源

- 当工作区域不确定时，我们采用本课程通用的方法：“先假设，再验证”！

Example 6.6

Calculate the bias current of M_1 in Fig. 6.23. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$ and $V_{TH} = 0.4$ V. If the gate voltage increases by 10 mV, what is the change in the drain voltage?

注意，题目中若没有明确说明V_A或λ，则不用考虑沟道调制效应



Solution It is unclear a priori in which region M_1 operates. Let us assume M_1 is saturated and proceed. Since $V_{GS} = 1$ V,

假设在饱和区

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6.18}$$

$$= 200\,\mu\text{A}. \tag{6.19}$$

We must check our assumption by calculating the drain potential:

$$V_X = V_{DD} - R_D I_D \tag{6.20}$$

$$= 0.8\text{ V}. \tag{6.21}$$

V_D最低不得低于V_G-V_{TH}

The drain voltage is lower than the gate voltage, but by less than V_{TH}. The illustration in Fig. 6.22 therefore indicates that M_1 indeed operates in saturation.

If the gate voltage increases to 1.01 V, then

$$I_D = 206.7\,\mu\text{A}, \tag{6.22}$$

lowering V_X to

$$V_X = 0.766\text{ V}. \tag{6.23}$$

Fortunately, M_1 is still saturated. The 34-mV change in V_X reveals that the circuit can *amplify* the input.

也有放大功能

Example 5.1

Consider a process technology for which $L_{min} = 0.18\ \mu m$, $t_{ox} = 4\ nm$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_t = 0.5\ V$.

(a) Find C_{ox} and k_n'.

(b) For a MOSFET with $W/L = 1.8\ \mu m/0.18\ \mu m$, calculate the values of v_{OV}, v_{GS}, and v_{DSmin} needed to operate the transistor in the saturation region with a current $i_D = 100\ \mu A$. 饱和区Vds=Vov

(c) For the device in (b), find the values of v_{OV} and v_{GS} required to cause the device to operate as a 1000-Ω resistor for very small v_{DS}.

(a)

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{4 \times 10^{-9}} = 8.63 \times 10^{-3}\ F/m^2$$

$$= 8.63\ fF/\mu m^2$$

$$k_n' = \mu_n C_{ox} = 450\ (cm^2/V \cdot s) \times 8.63\ (fF/\mu m^2)$$

$$= 450 \times 10^8\ (\mu m^2/V \cdot s) \times 8.63 \times 10^{-15}\ (F/\mu m^2)$$

$$= 388 \times 10^{-6}\ (F/V \cdot s)$$

$$= 388\ \mu A/V^2$$

Consider a process technology for which $L_{min} = 0.18\ \mu m$, $t_{ox} = 4\ nm$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_t = 0.5\ V$.

(a) Find C_{ox} and k_n'.

(b) For a MOSFET with $W/L = 1.8\ \mu m/0.18\ \mu m$, calculate the values of v_{OV}, v_{GS}, and v_{DSmin} needed to operate the transistor in the saturation region with a current $i_D = 100\ \mu A$.

(c) For the device in (b), find the values of v_{OV} and v_{GS} required to cause the device to operate as a 1000-Ω resistor for very small v_{DS}.

(b) For operation in the saturation region,

$$i_D = \frac{1}{2} k_n' \frac{W}{L} v_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 388 \times \frac{1.8}{0.18} v_{OV}^2$$

which gives

$$v_{OV} = 0.23\ V$$

Thus,

$$v_{GS} = V_t + v_{OV} = 0.73\ V$$

and

$$v_{DSmin} = v_{OV} = 0.23\ V$$

Consider a process technology for which $L_{min} = 0.18\ \mu m$, $t_{ox} = 4\ nm$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_t = 0.5\ V$.

(a) Find C_{ox} and k_n'.

(b) For a MOSFET with $W/L = 1.8\ \mu m/0.18\ \mu m$, calculate the values of v_{OV}, v_{GS}, and v_{DSmin} needed to operate the transistor in the saturation region with a current $i_D = 100\ \mu A$.

(c) For the device in (b), find the values of v_{OV} and v_{GS} required to cause the device to operate as a 1000-Ω resistor for very small v_{DS}.

(c) For the MOSFET in the triode region with v_{DS} very small,

$$r_{DS} = \frac{1}{k_n' \frac{W}{L} v_{OV}}$$

Thus

$$1000 = \frac{1}{388 \times 10^{-6} \times 10 \times v_{OV}}$$

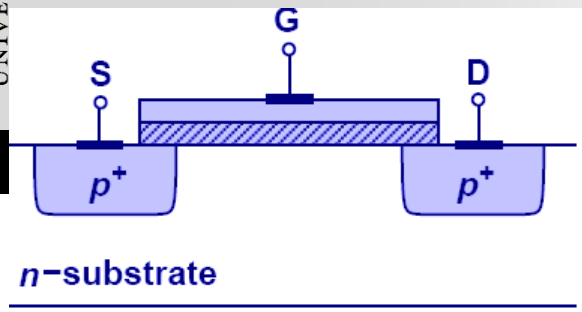
which gives

$$v_{OV} = 0.26\ V$$

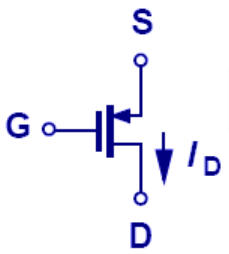
Thus,

$$v_{GS} = 0.76\ V$$

PMOS 晶体管

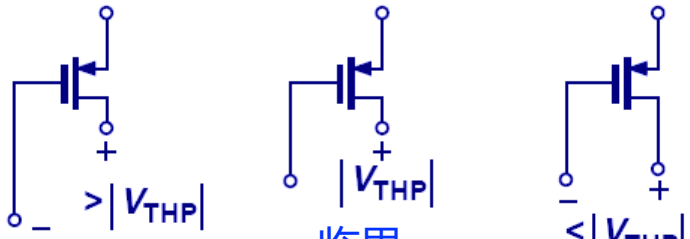


(a)



(b)

VS接最高电位，VG最低电位。



非饱和区　临界　(c)　饱和区

如何判断工作区：

从符号上理解（电路分析中最有效），要使PMOS工作在饱和区，V_D的上限为$V_G + |V_{TH}|$

- MOSFET 器件也可以制造在n衬底上，以空穴作载流子，这类MOSFET被称为 PMOS 晶体管，相应的，之前我们讨论的制造在p衬底上，以电子作为载流子的MOSFET被称为NMOS.
- PMOS的特性与NMOS类似，只是极性相反。S电势最高

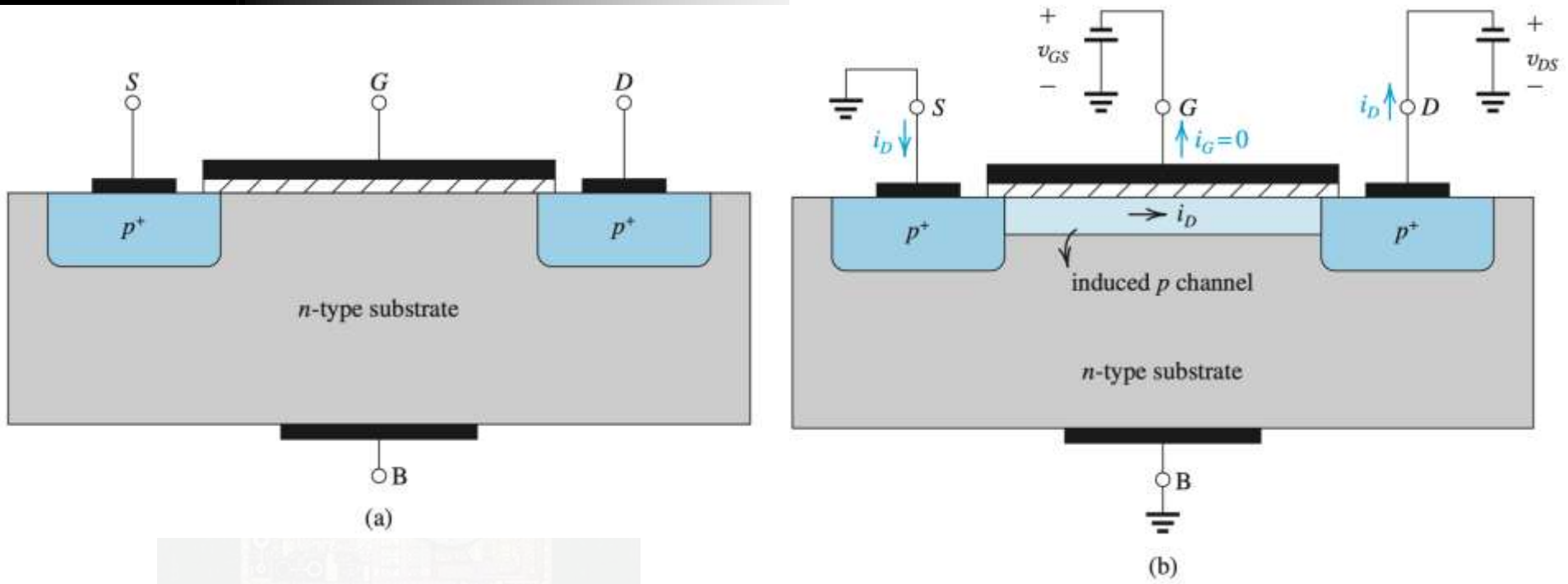
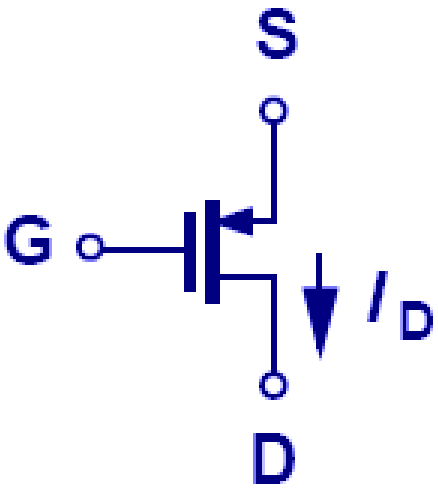


Figure 5.9 **(a)** Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor shown in Fig. 5.1(b) except that all semiconductor regions are reversed in polarity. **(b)** A negative voltage v_{GS} of magnitude greater than $|V_{tp}|$ induces a p channel, and a negative v_{DS} causes a current i_D to flow from source to drain.

PMOS 方程



$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$$

$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right]$$

$$I_{D,sat} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(|V_{GS}| - |V_{TH}|)^2(1 + \lambda|V_{DS}|)$$

$$I_{D,tri} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[2(|V_{GS}| - |V_{TH}|)|V_{DS}| - V_{DS}^2\right]$$

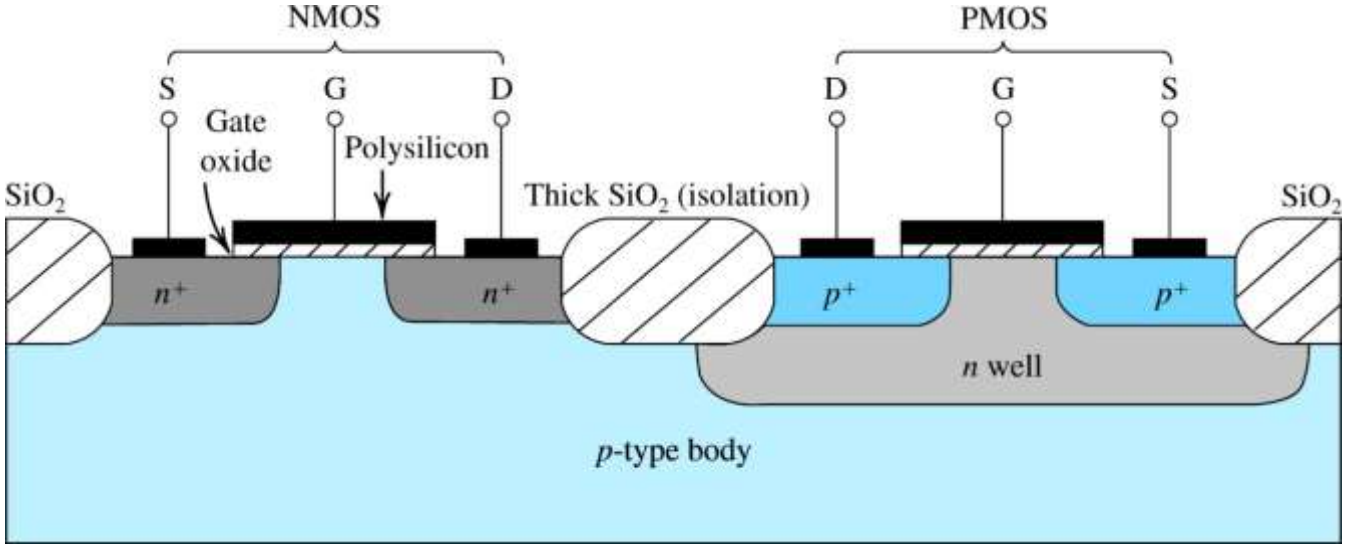
用绝对值表示，公式与NMOS可以统一

5.1.7. The *p*-Channel MOSFET

- PMOS technology originally dominated the MOS field (over NMOS). However, as manufacturing difficulties associated with NMOS were solved, "they" took over
- **Q:** Why is NMOS advantageous over PMOS?
  - **A:** Because electron mobility μ_n is 2 – 4 times greater than hole mobility μ_p.
- **complementary MOS** (CMOS) **technology** – is technology which allows fabrication of both N and PMOS transistors on a single chip.

5.1.8. Complementary MOS or CMOS

- CMOS employs MOS transistors of both polarities.



- 在p衬底上先制备一个n阱（n-well），然后在n阱里制备PMOS，在p衬底上制备NMOS，该技术称之为CMOS（Complementary MOS）.
- Intel第一代CPU，4004，是使用纯NMOS技术，之后都采用了CMOS技术

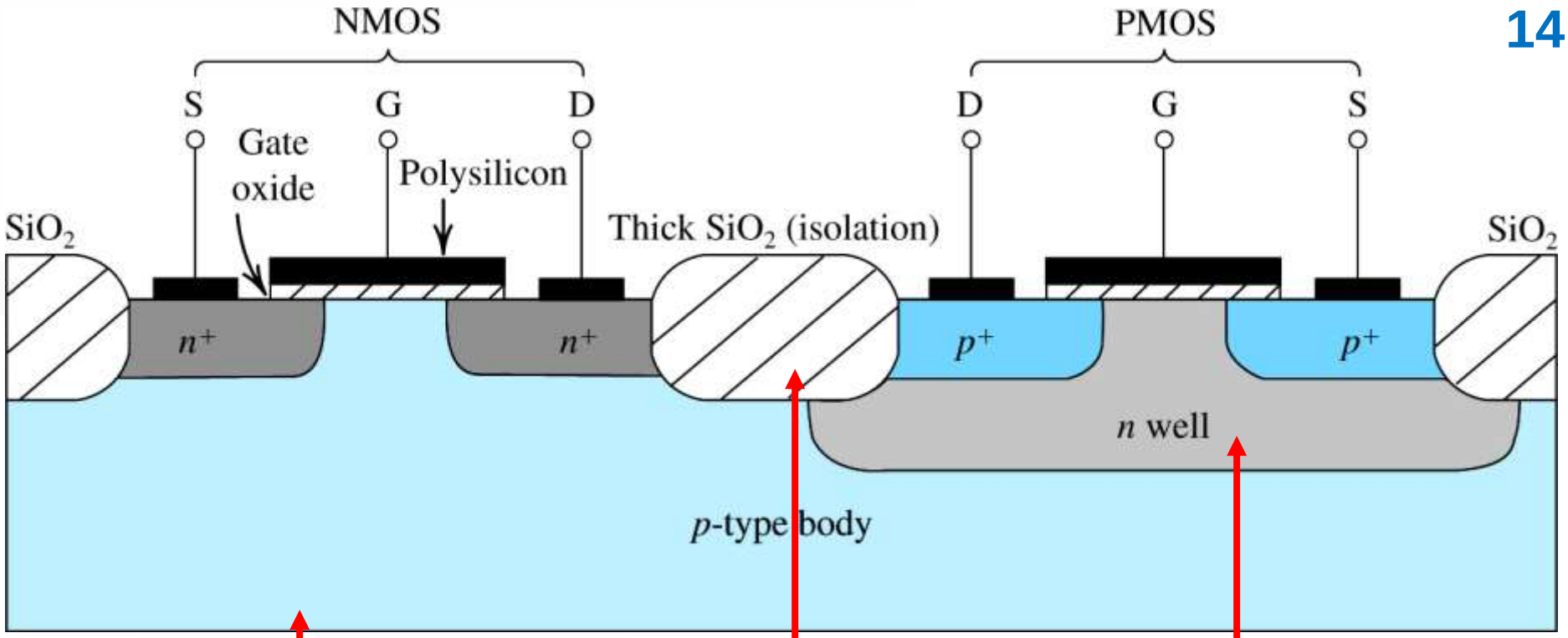


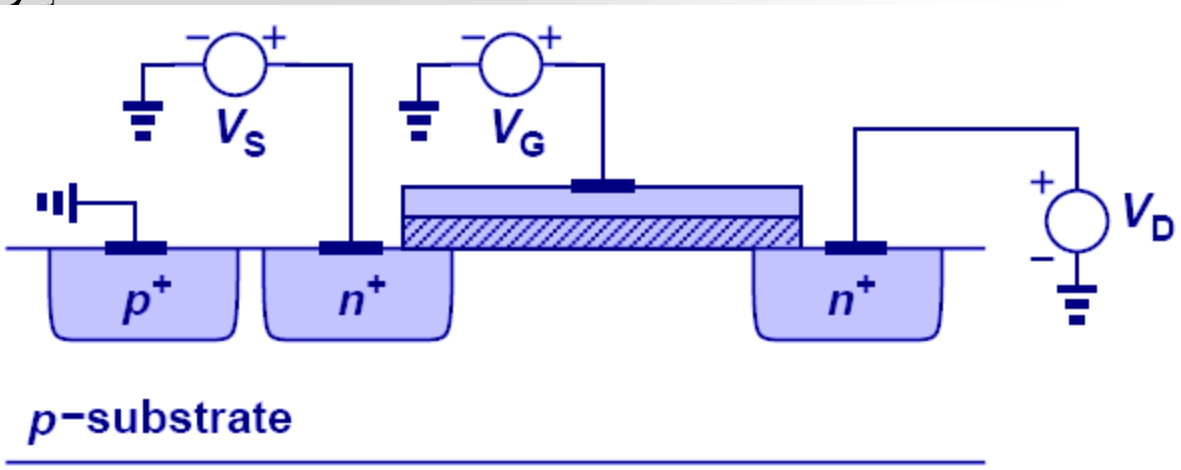
Figure 5.10: Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

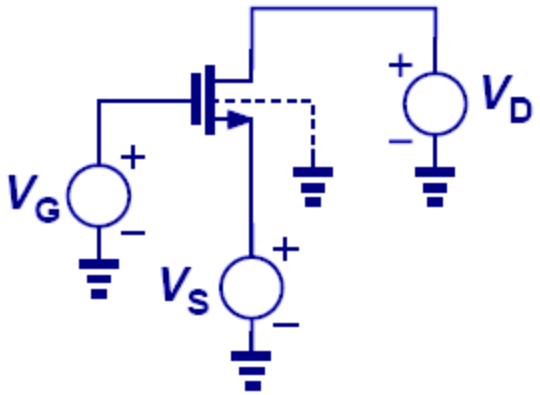
p-type semiconductor provides the MOS body (and allows generation of n-channel)

SiO_2 is used to isolate NMOS from PMOS

n-well is added to allow generation of *p*-channel

衬底效应





若Vs不接地，则需要画出

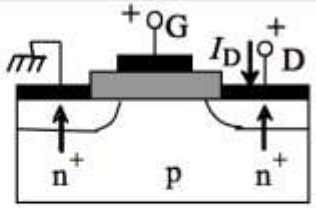
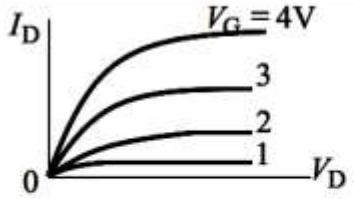
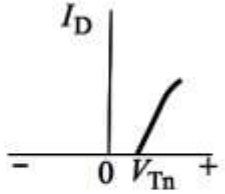
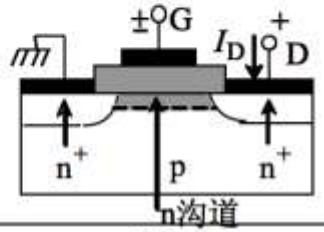
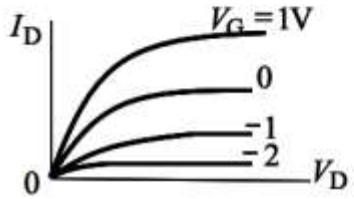
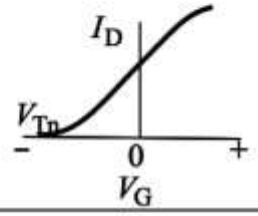
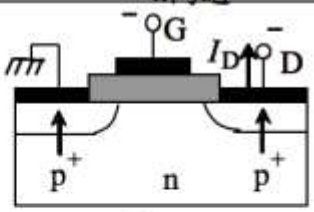
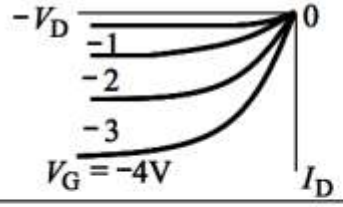
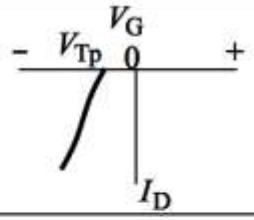
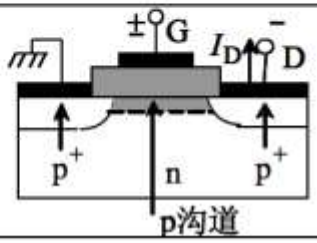
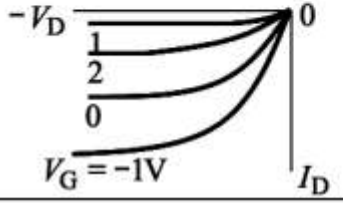
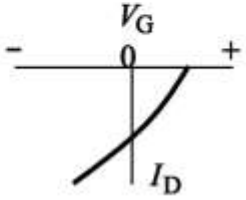
了解就可以　　用修正后的Vth表征，不用管

$$V_{TH} = V_{TH0} + \rho\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

- NMOS，当源极电压大于零时，因衬底始终接地，V_{SB}会对MOSFET的阈值电压产生影响，称之为衬底效应（Body Effect）

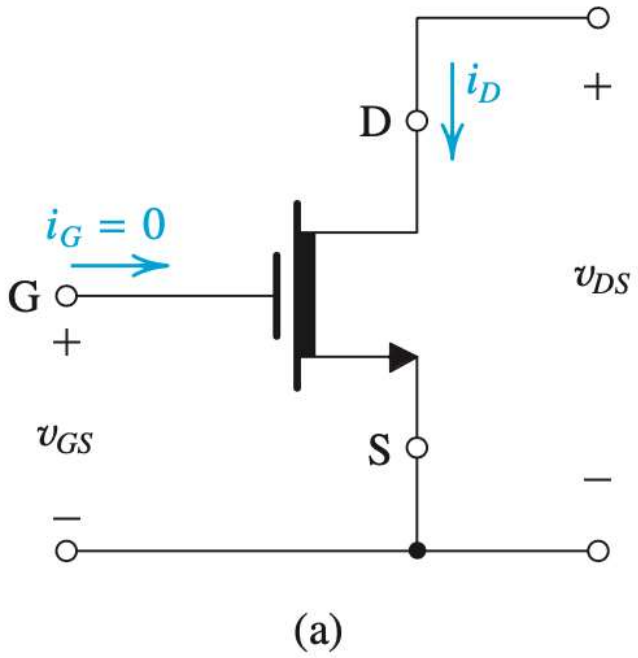
MOSFET的种类

重点理解

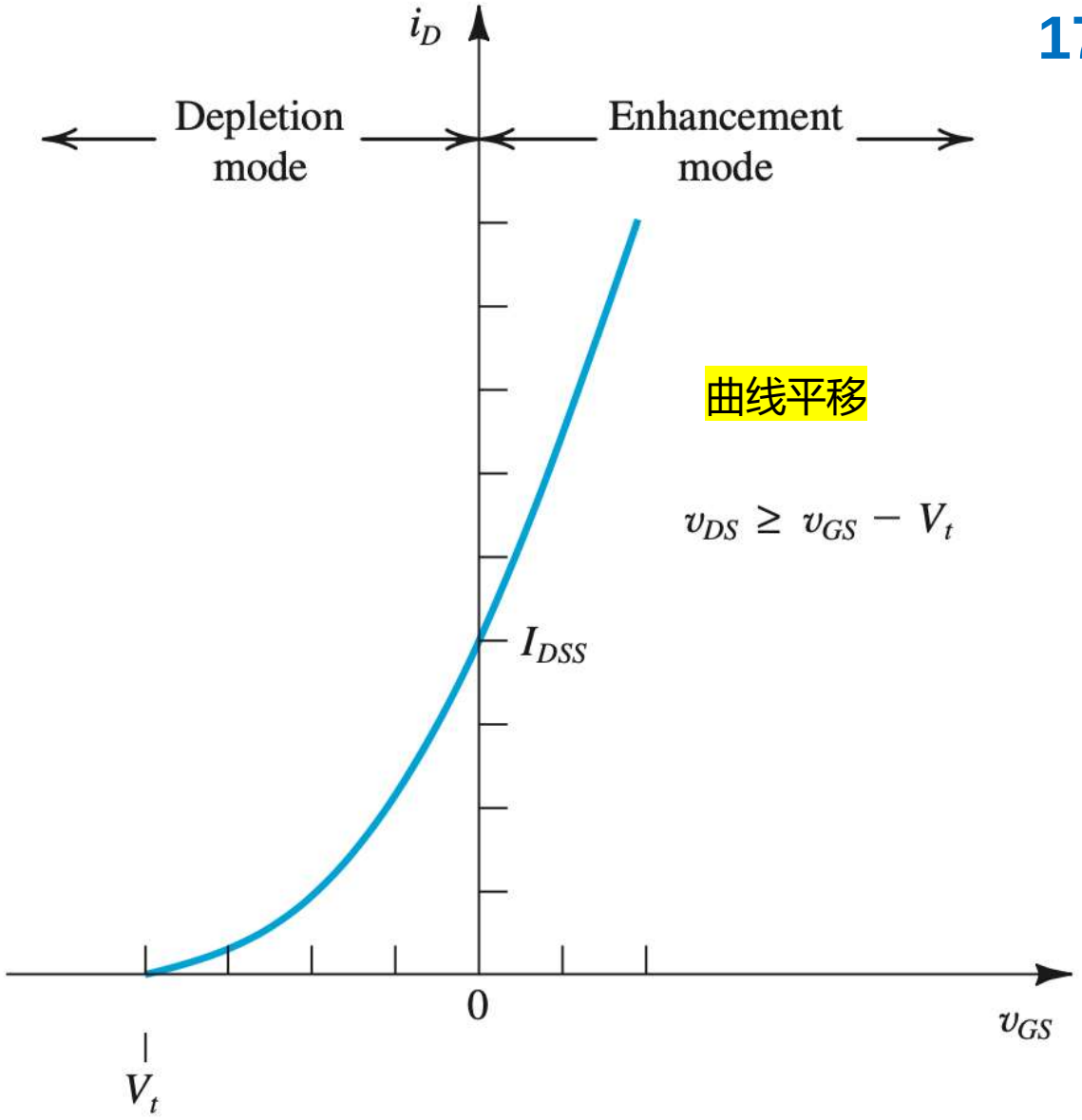
类型	剖面图	输出特性	转移特性
n沟增强型 (常闭)			
n沟耗尽型 (常开)			
p沟增强型 (常闭)			
p沟耗尽型 (常开)			

耗尽型：V_{GS}=0 时已具有沟道

粗线，一开始有沟道，耗尽型



(a)



(b)

Figure 5.27 The circuit symbol **(a)** and the i_D–v_{GS} characteristic in saturation **(b)** for an *n*-channel depletion-type MOSFET.

Quick Recap!

- The equation used to define i_D depends on relationship btw v_{DS} and v_{OV}.
  - $v_{DS} << v_{OV}$
  - $v_{DS} < v_{OV}$
  - $v_{DS} >= v_{OV}$
  - $v_{DS} >> v_{OV}$

μ_n represents mobility of electrons at surface of the n-channel in m^2/Vs

(eq5.7) $i_D = \underbrace{(C_{ox} W v_{OV})}_{\text{charge per unit length of } n\text{-channel in } C/m} \underbrace{\left(\frac{\mu_n v_{DS}}{L}\right)}_{\text{electron drift velocity in } m^2/Vs}$ in A

(eq5.14) $i_D = (\mu_n C_{ox}) \frac{W}{L} (v_{OV} - \frac{1}{2} v_{DS}) v_{DS}$ in A

(eq5.17) $\boxed{i_D = \frac{1}{2} (\mu_n C_{ox}) \frac{W}{L} v_{OV}^2}$ in A （饱和区）最重要！

(eq5.23) $i_D = \frac{1}{2} (\mu_n C_{ox}) \frac{W}{L} v_{OV}^2 (1 + \lambda v_{DS})$ in A

考虑效应

5.2. Current-Voltage Characteristics
伏安特性，电流电压约束关系

- Figure 5.11. shows an *n*-channel enhancement MOSFET. N沟道增强型MOSFET的电路符号
- There are four terminals:
  - drain (D), gate (G), body (B), and source (S).
- Although, it is assumed that body and source are connected.

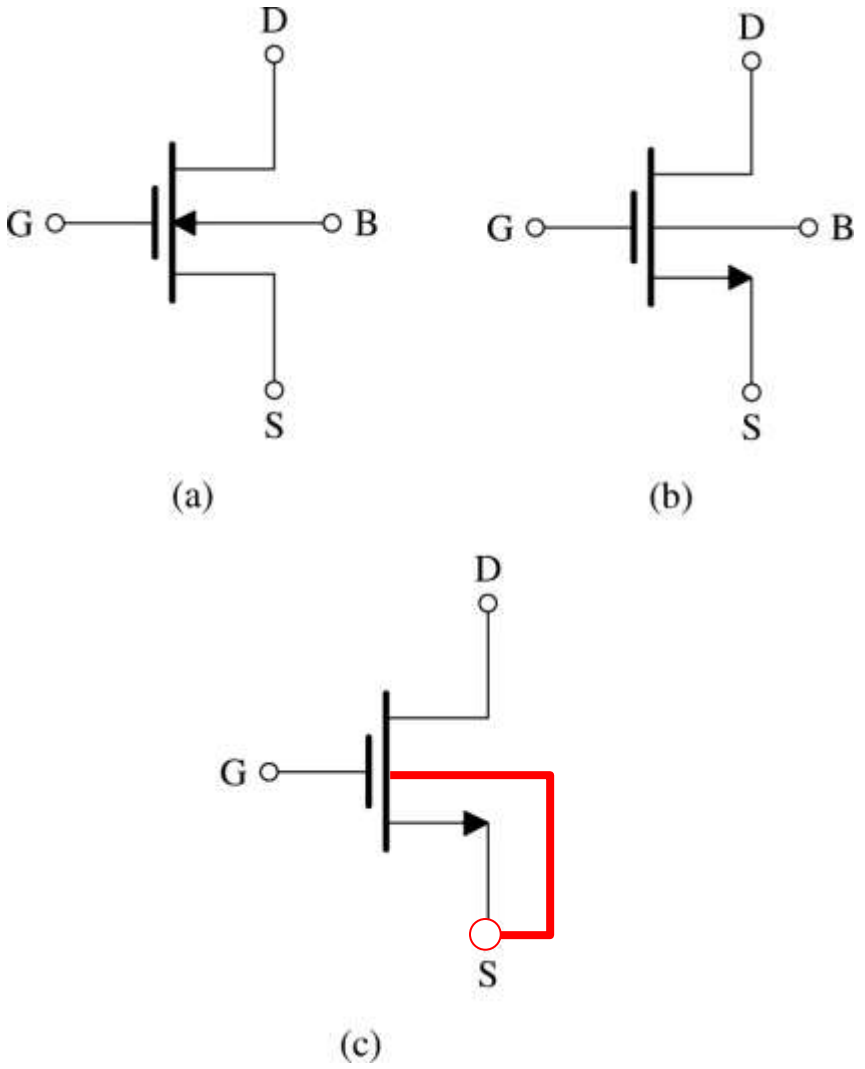
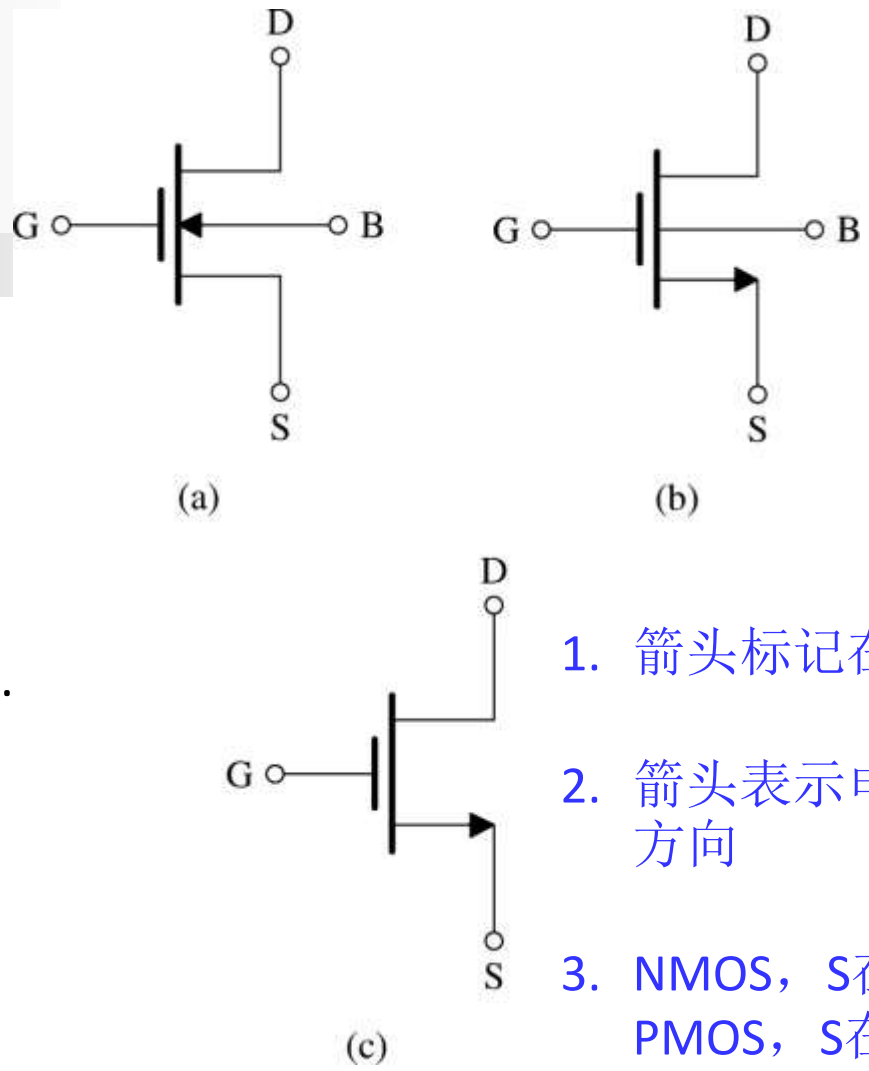


Figure 5.11 (a): Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

v_D is always $> v_S$

5.2. Current-Voltage Characteristics

- Although MOSFET is symmetrical device, one often designates terminals as source and drain.
- **Q:** How does one make this designation?
  - **A:** By polarity of voltage applied.
- Arrowheads designate "normal" direction of current flow
  - Note that, in part (b), we designate current as D→S.
  - No need to place arrow with B.



1. 箭头标记在S端
2. 箭头表示电流方向
3. NMOS，S在下
   PMOS，S在上

Figure 5.11 (a): Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

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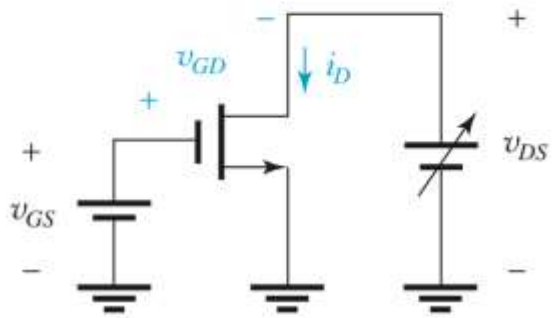
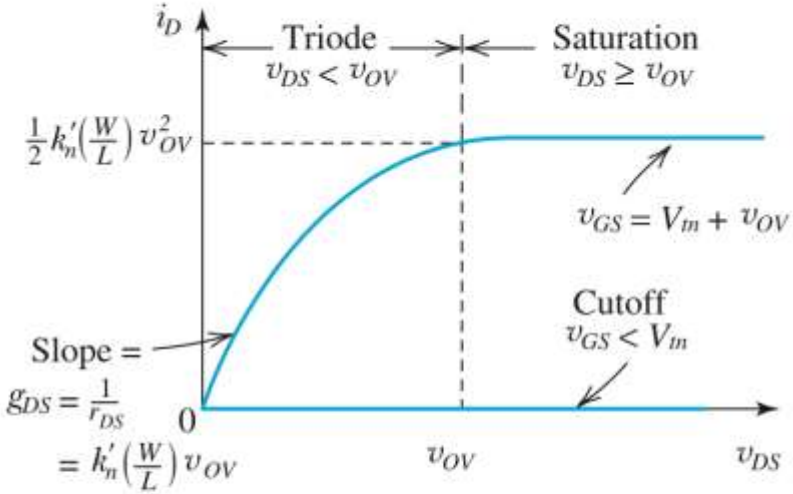
Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

三个不同的工作区域

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

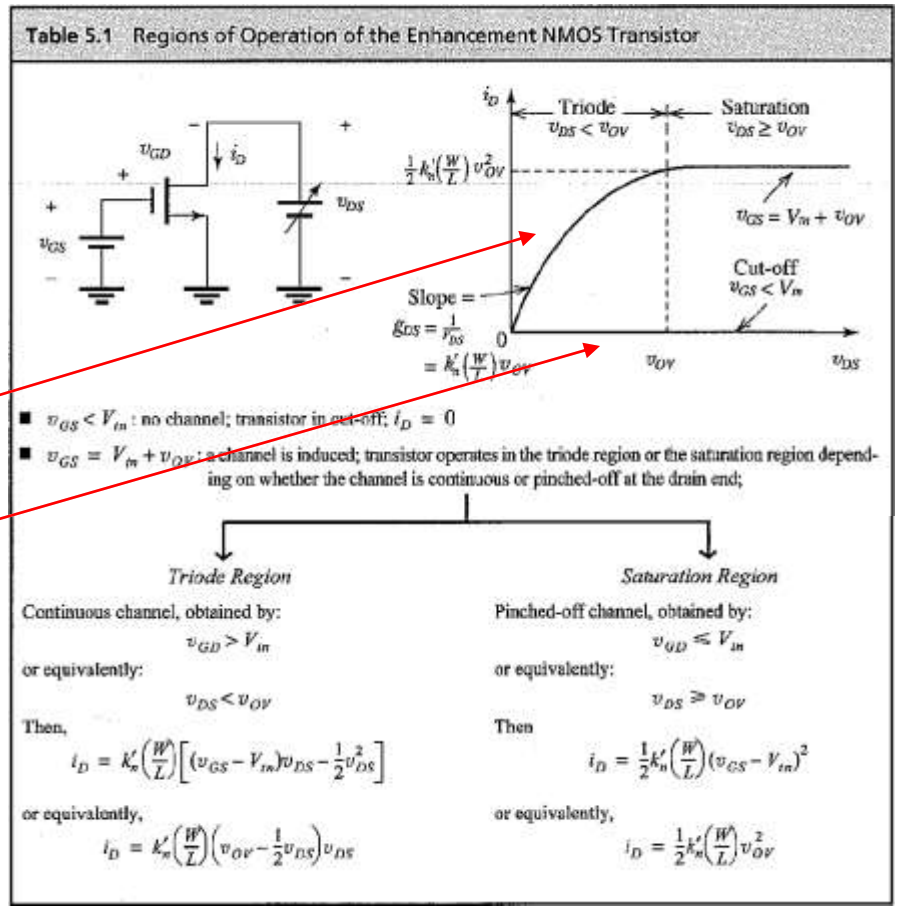
or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Vgs控制
作区域

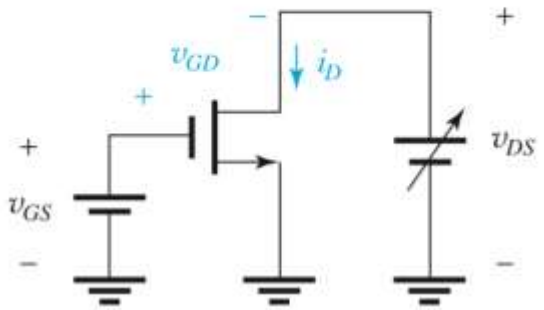
5.2.2. The i_D-v_{DS} Characteristics

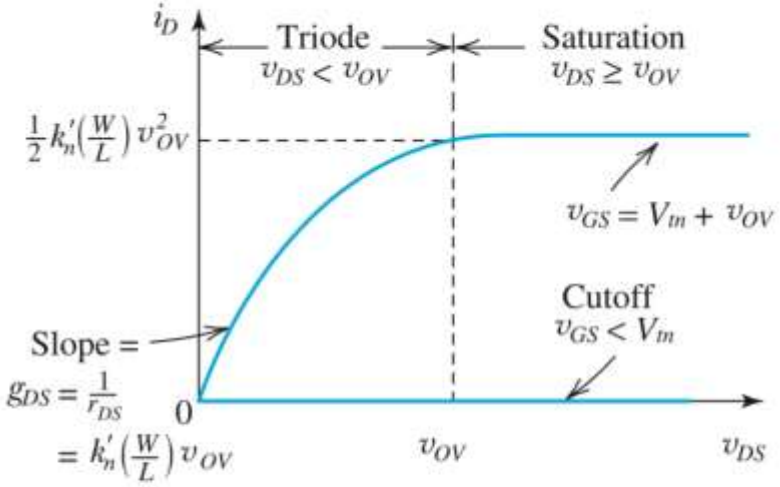
- At top of table, it shows circuit consisting of NMOS transistor and two dc supplies (v_{DS}, v_{GS})
- This circuit is used to demonstrate i_D-v_{DS} characteristic
  - 1st set v_{GS} to desired constant
  - 2nd vary v_{DS}
- Two curves are shown…
  - $v_{GS} < V_{tn}$
  - $v_{GS} = V_{tn} + v_{OV}$



1. 首先根据 V_{GS} 判断器件是否 turn on
2. 其次，再根据 V_D 与 V_G 的关系，判断器件是否在饱和区
3. 若作为放大器使用，一般都需要工作在饱和区，可以先假设，再验证

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

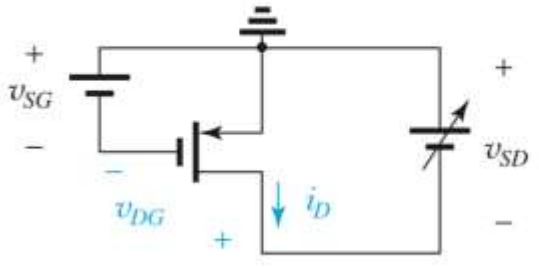
Then

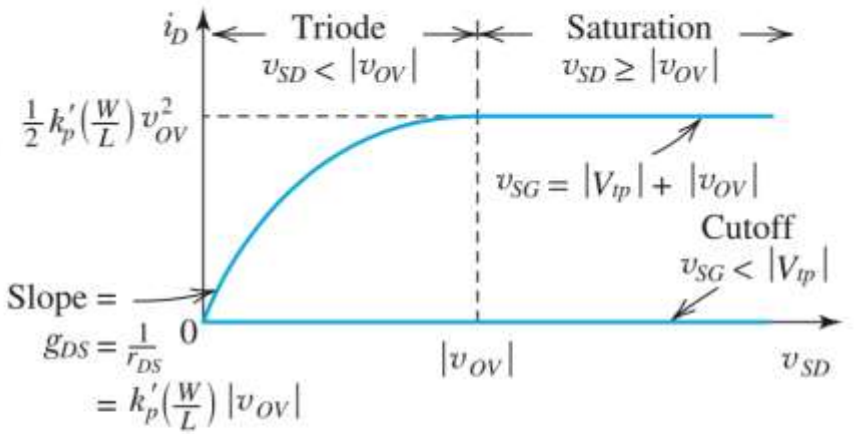
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor





- $v_{SG} < |V_{tp}|$: no channel; transistor in cutoff; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

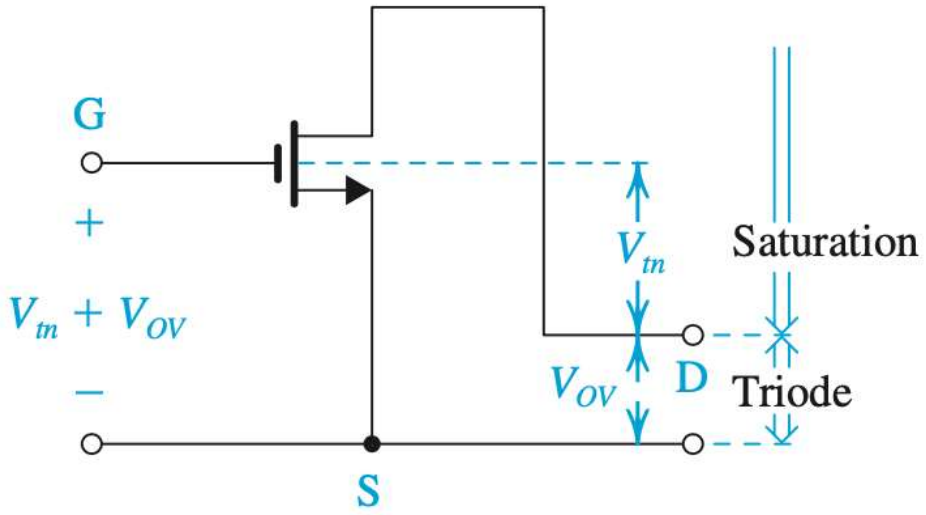
$$v_{SD} \geq |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

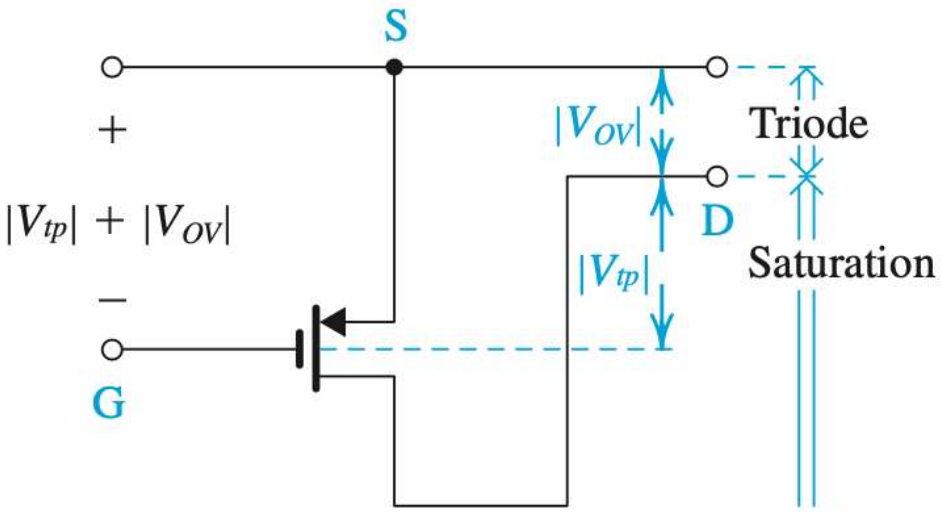
or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$



NMOS: V_D最低不得低于V_G-V_{TH}

Figure 5.12 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.



PMOS: V_D最高不得高于V_G+$|V_{TH}|$

Figure 5.20 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

equation (5.14)

as v_{GS} increases, so do the **(1)** saturation current and **(2)** beginning of the saturation region

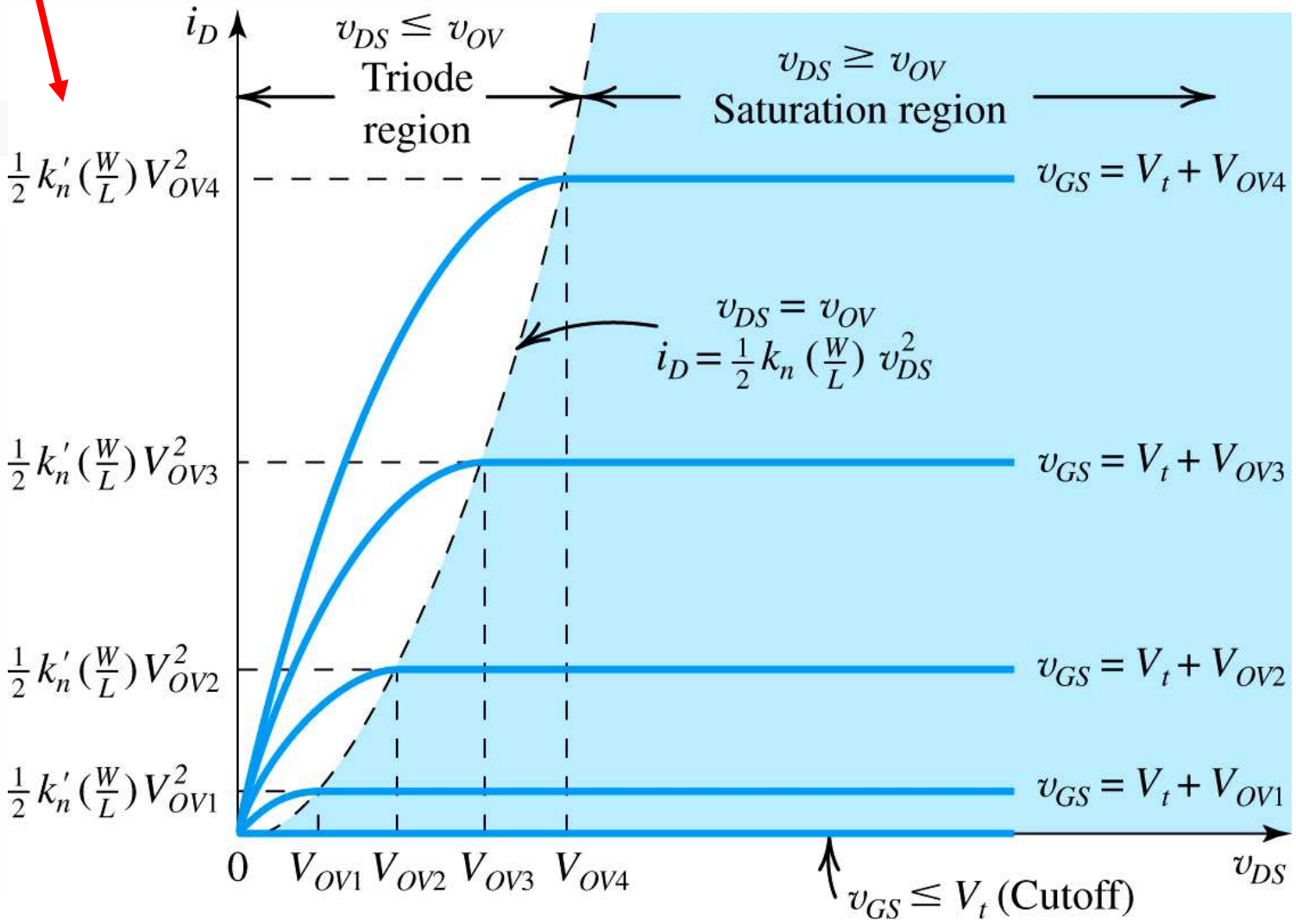


Figure 5.13: The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor

5.2.2. The i_D-v_{DS} Characteristic 输出特性

放大是使用Qpoint点或者下图

- **Q:** When MOSFET's are employed to design amplifier, in what range will they be operated?
  - **A:** saturation
- In saturation, the drain current (i_D) is…
  - dependent on v_{GS}
  - independent of v_{DS}
  - 理想的压控电流源！
- In effect, it becomes a voltage-controlled current source.
  - This is key for amplification.

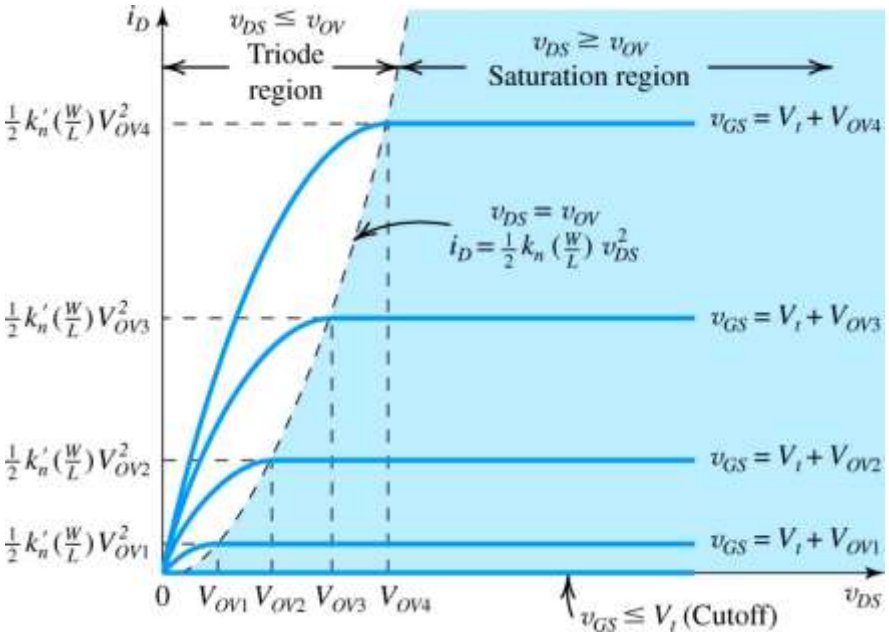


Figure 5.13: The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor

5.2.2. The i_D-v_{GS} Characteristic 转移特性

- **Q:** What is one problem with (5.21)?
  - **A:** It is nonlinear w/ respect to v_{OV} … however, this is not of concern now.

- In effect, it becomes a voltage-controlled current source.
  - **This is key for** amplification.
  - Refer to (5.21).

(eq5.21) $$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\overbrace{(v_{GS}-V_{tn})^2}^{v_{OV}^2}$$

this relationship provides basis for application of MOSFET as amplifier

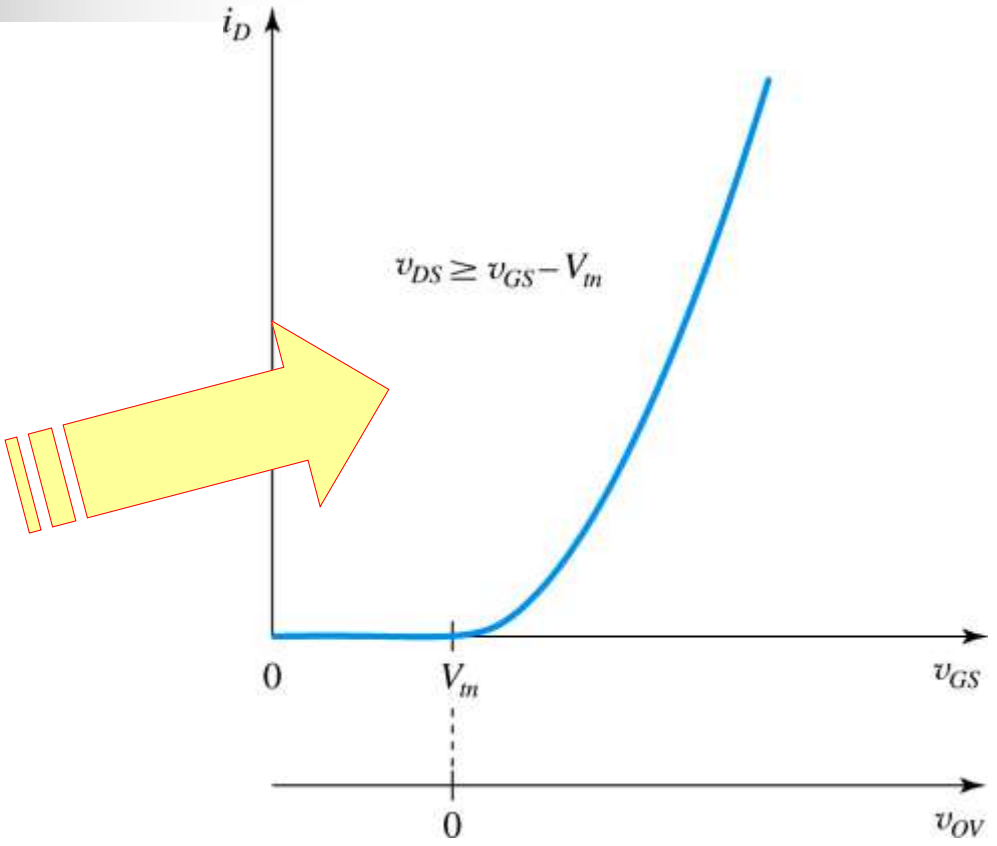
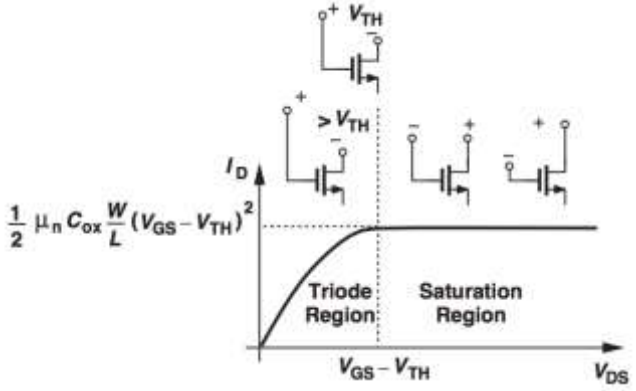
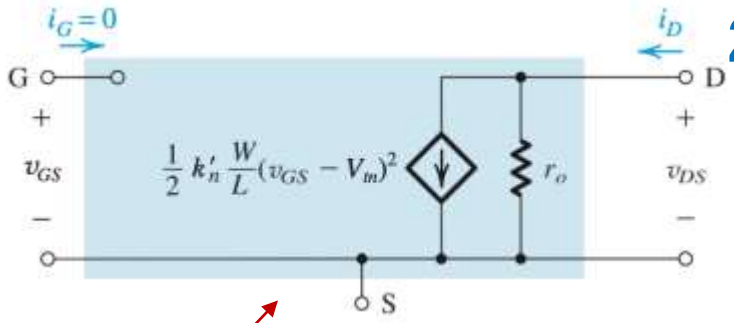


Figure 5.14: The i_D-v_{GS} characteristic of an NMOS transistor operating in the saturation region. The i_D-v_{OV} characteristic can be obtained by simply re-labeling the horizontal axis, that is, shifting the origin to the point $v_{GS} = V_{tn}$.

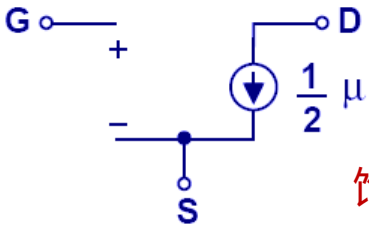
large-signal models
大信号模型





$V_{GS} > V_{TH}$

$V_{DS} > V_{GS} - V_{TH}$



$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

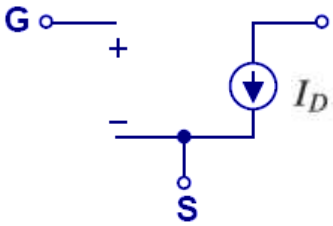
饱和区，考虑沟道调制效应

(a)

$V_{GS} > V_{TH}$

$V_{DS} < V_{GS} - V_{TH}$

非饱和区



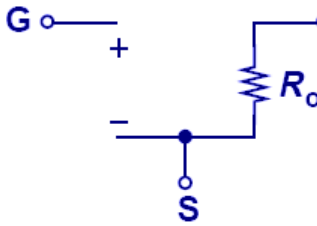
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS} - V_{DS}^2]$$

(b)

$V_{GS} > V_{TH}$

$V_{DS} << 2(V_{GS} - V_{TH})$

非饱和区（V_{DS}很小时）



$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$$

(c)

- 基于V_{DS}的不同，MOSFET 有不同的大信号模型.
- **大信号模型**~器件大范围的电压电流约束关系，往往是非线性的；**小信号模型**~叠加于大信号模型某一直流工作点之上的微小变化信号的模型，**将非线性曲线在微小范围内线性化**

Example 5.2

Consider an NMOS transistor fabricated in a 0.18-μm process with $L = 0.18\ \mu m$ and $W = 2\ \mu m$. The process technology is specified to have $C_{ox} = 8.6\ fF/\mu m^2$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_{tn} = 0.5\ V$.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100\ \mu A$.

(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50\ \mu A$.

(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3\ V$. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by −0.01 V.

$$k_n' = \mu_n C_{ox}$$
$$= 450 \times 10^{-4} \times 8.6 \times 10^{-15} \times 10^{12}\ A/V^2$$
$$= 387\ \mu A/V^2$$

$$k_n = k_n'\left(\frac{W}{L}\right)$$
$$= 387\left(\frac{2}{0.18}\right) = 4.3\ mA/V^2$$

(a) With the transistor operating in saturation,

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

which results in

$$V_{OV} = 0.22\ V$$

Thus,

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.22 = 0.72\ V$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{OV} = 0.22\ V$$

Example 5.2

Consider an NMOS transistor fabricated in a 0.18-μm process with $L = 0.18\ \mu m$ and $W = 2\ \mu m$. The process technology is specified to have $C_{ox} = 8.6\ fF/\mu m^2$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_{tn} = 0.5\ V$.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100\ \mu A$.

(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50\ \mu A$.

(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3\ V$. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by −0.01 V.

(b) With V_{GS} kept constant at 0.72 V and I_D reduced from the value obtained at the edge of saturation, the MOSFET will now be operating in the triode region, thus

50小于100，进入非饱和区

$$I_D = k_n\left[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$50 = 4.3 \times 10^3\left[0.22V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

which can be rearranged to the form

$$V_{DS}^2 - 0.44V_{DS} + 0.023 = 0$$

This quadratic equation has two solutions

$$V_{DS} = 0.06\ V \quad \text{and} \quad V_{DS} = 0.39\ V$$

The second answer is greater than V_{OV} and thus is physically meaningless, since we know that the transistor is operating in the triode region. Thus we have

$$V_{DS} = 0.06\ V$$

Example 5.2

Consider an NMOS transistor fabricated in a 0.18-μm process with $L = 0.18\ \mu m$ and $W = 2\ \mu m$. The process technology is specified to have $C_{ox} = 8.6\ fF/\mu m^2$, $\mu_n = 450\ cm^2/V \cdot s$, and $V_{tn} = 0.5\ V$.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100\ \mu A$.

(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50\ \mu A$.

(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3\ V$. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by −0.01 V.

(c) For $v_{GS} = 0.7\ V$, $V_{OV} = 0.2\ V$, and since $V_{DS} = 0.3\ V$, the transistor is operating in saturation and

$v_{OV} = v_{GS} - v_{tn}$

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

$$= \frac{1}{2} \times 4300 \times 0.04$$

$$= 86\ \mu A$$

Now for $v_{GS} = 0.710\ V$, $v_{OV} = 0.21\ V$ and

$$i_D = \frac{1}{2} \times 4300 \times 0.21^2 = 94.8\ \mu A$$

and for $v_{GS} = 0.690\ V$, $v_{OV} = 0.19\ V$, and

$$i_D = \frac{1}{2} \times 4300 \times 0.19^2 = 77.6\ \mu A$$

Thus, with $\Delta v_{GS} = +0.01\ V$, $\Delta i_D = 8.8\ \mu A$; and for $\Delta v_{GS} = -0.01\ V$, $\Delta i_D = -8.4\ \mu A$.

MOSFET 电路直流分析

选合理的Qpoint进行直流分析，可以理解为就是求Id

- 基于 MOSFET 的“电流电压”约束关系
- 基于基本电路原理与分析方法
- 为简单起见，若无明确说明，一般我们不考虑沟道调制效应
- 根据有效电压V_{OV}来分析电路，会比较方便

$$V_{OV} = V_{GS} - V_{tn} \text{ for NMOS and } |V_{OV}| = V_{SG} - |V_{tp}| \text{ for PMOS}$$

Example 5.3

Design the circuit of Fig. 5.21: that is, determine the values of R_D and R_S so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $L = 1\ \mu$m, and $W = 32\ \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

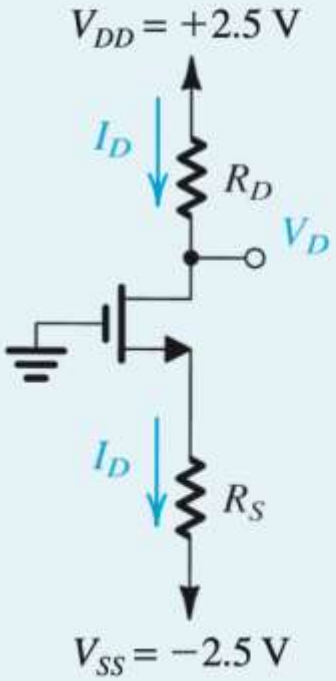


Figure 5.21 Circuit for Example 5.3.

①根据V_{DD}，V_D，I_D，求R_D

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5\ \text{k}\Omega$$

Example 5.3

Design the circuit of Fig. 5.21: that is, determine the values of R_D and R_S so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $L = 1\ \mu$m, and $W = 32\ \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

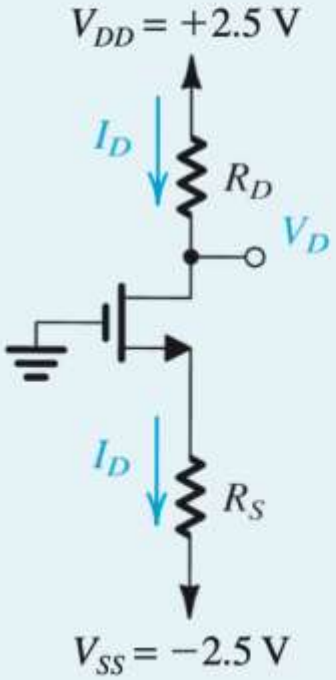


Figure 5.21 Circuit for Example 5.3.

②求R_S，需要知道V_S，V_S可以根据V_{GS}得到，V_{GS}可以由$V_{OV} + V_{TH}$得到，V_{OV}由I_D决定。

③判断MOSFET的工作状态。$V_D > V_G$ → 饱和区

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2 \Longrightarrow V_{OV} = 0.5\text{ V} \Longrightarrow V_{GS} = V_t + V_{OV} \Longrightarrow$$

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25\text{ k}\Omega$$

Example 5.4

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the i–v relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = k_n'(W/L)$ and V_{tn}. Neglect channel-length modulation (i.e., $\lambda = 0$). Note that this two-terminal device is known as a **diode-connected transistor**.

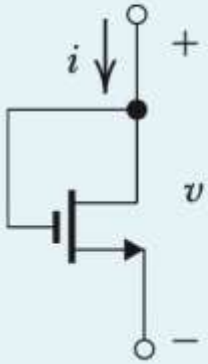


Figure 5.22

平方电阻可以在小范围内变成线性，芯片内部都这样使用，否则布线代价太大

① $V_D = V_G$ → 工作于饱和区

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

② $i = i_D$ and $v = v_{GS}$

$$i = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v - V_{tn})^2 \quad \Longrightarrow \quad i = \frac{1}{2}k_n(v - V_{tn})^2$$

Example 5.5

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/ V^2.

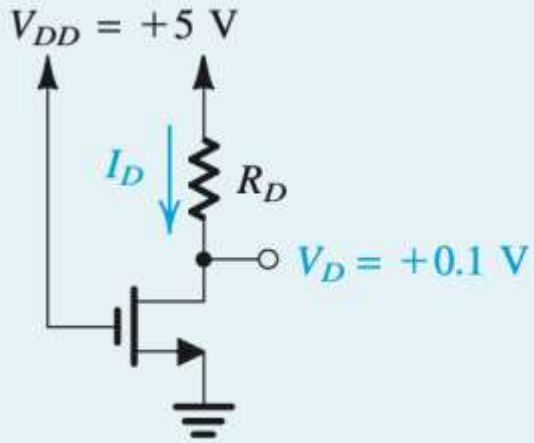


Figure 5.23 Circuit for Example 5.5.

①V_D低于V_G-V_{TH} → 工作于非饱和区

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right] = 0.395 \text{ mA}$$

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1}{0.395} = 253\ \Omega$$

②根据V_D求R_D

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega$$

Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

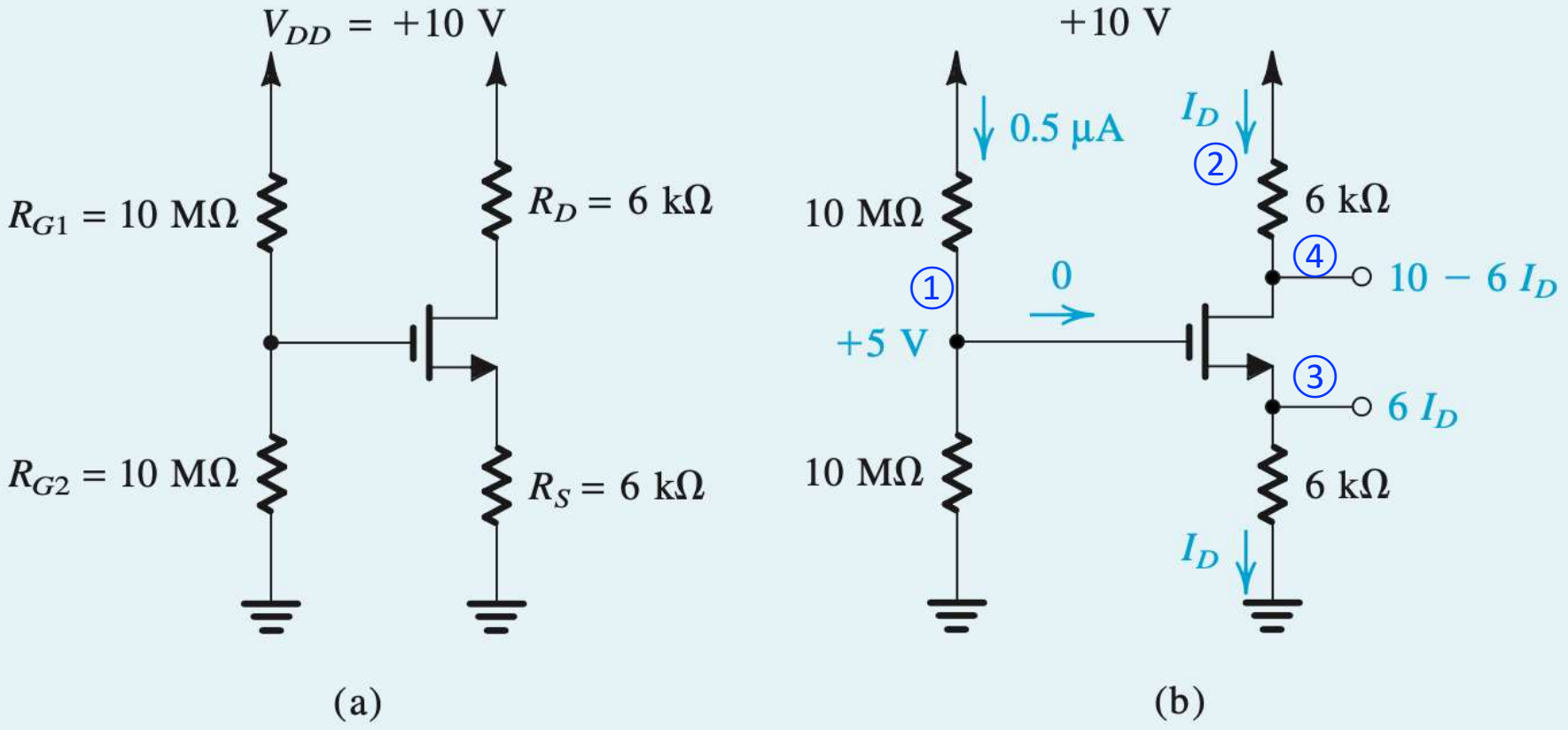


Figure 5.24 **(a)** Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

③ $V_{GS} = 5 - 6I_D$ 假设工作在饱和区 $I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_{tn})^2$ ⇨ $18I_D^2 - 25I_D + 8 = 0$

Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

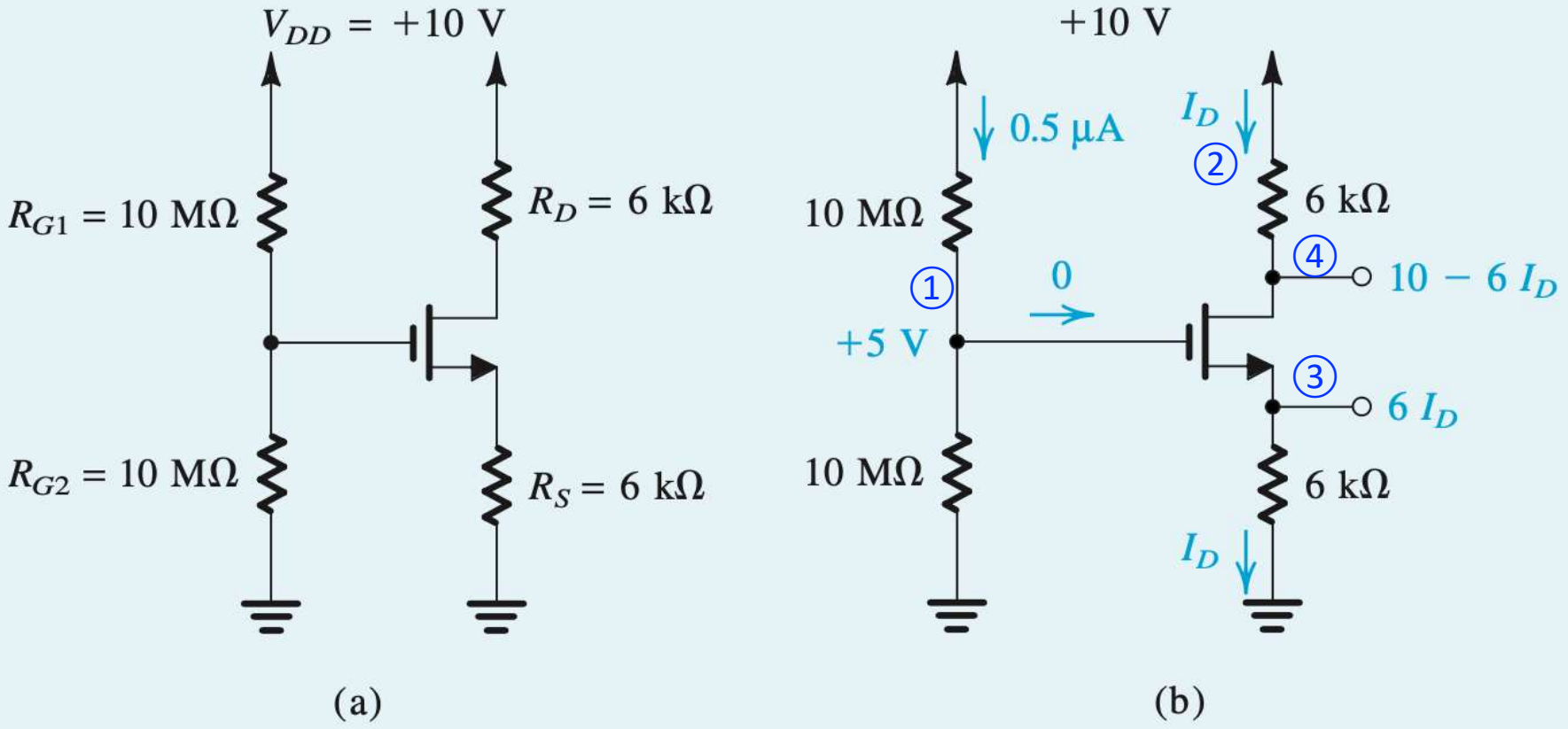


Figure 5.24 **(a)** Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

③ $18I_D^2 - 25I_D + 8 = 0$ 两个解 I_D: 0.89 mA and 0.5 mA $6 \times 0.89 = 5.34$ V > 5 V

Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

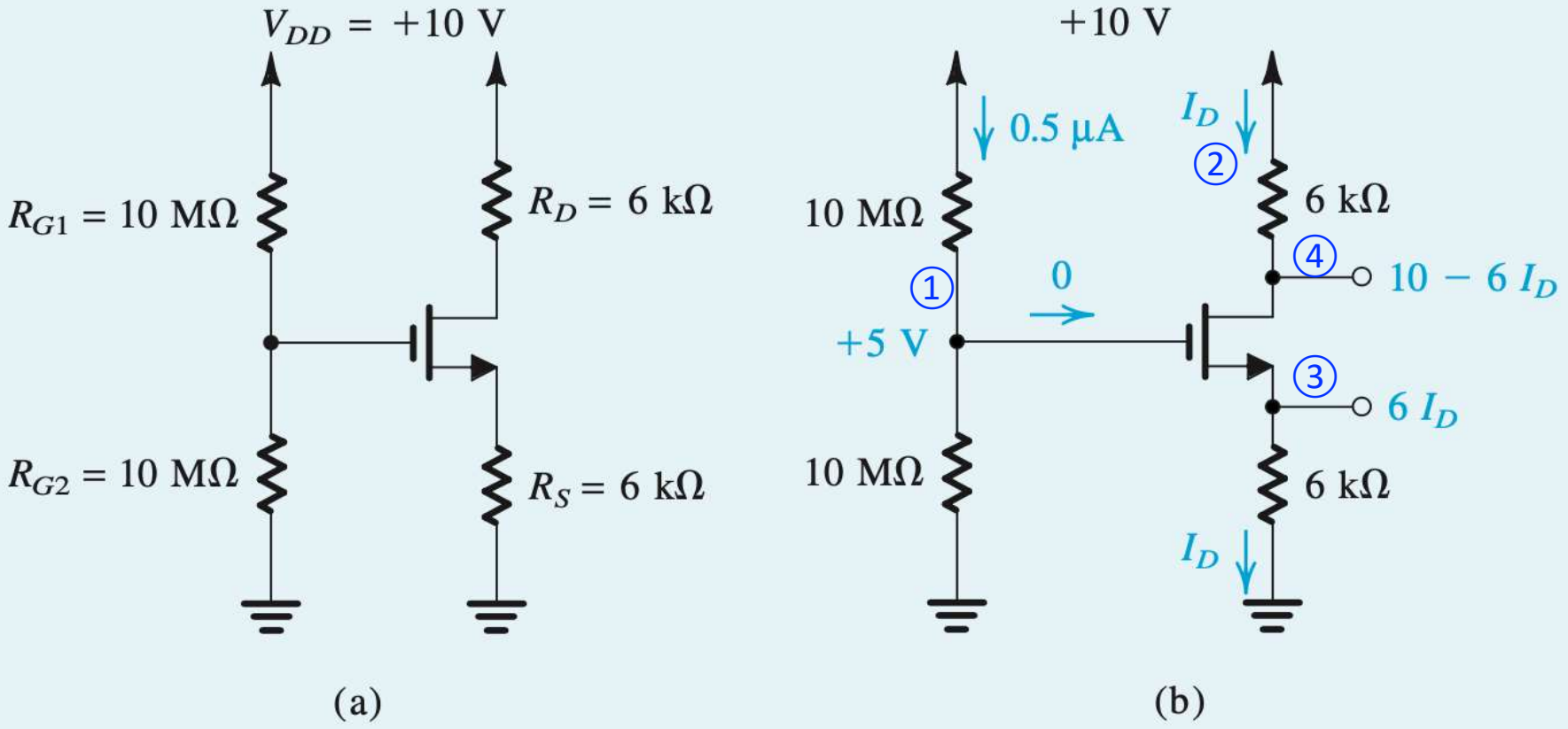


Figure 5.24 **(a)** Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

④ $I_D = 0.5$ mA $\quad V_S = 0.5 \times 6 = +3$ V $\quad V_D = 10 - 6 \times 0.5 = +7$ V > 5 V

Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the PMOS transistor have $V_{tp} = -1$ V and $k_p'(W/L) = 1$ mA/V^2. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?

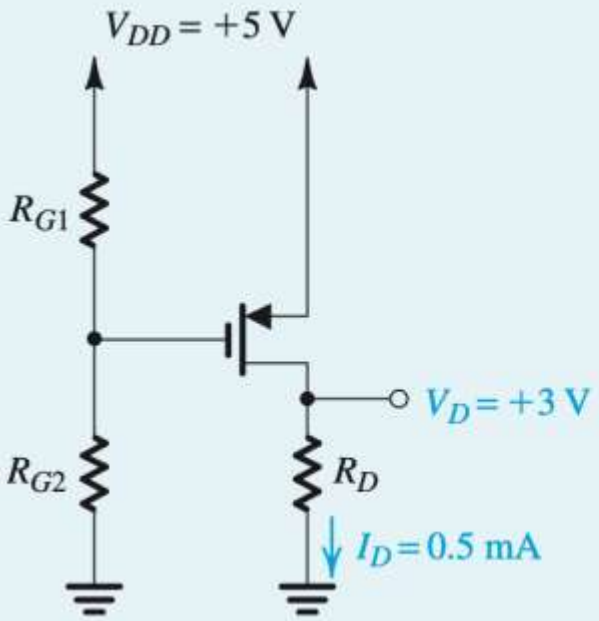


Figure 5.25 Circuit for Example 5.7.

①工作于饱和区

$$I_D = \frac{1}{2}k_p'\frac{W}{L}|V_{OV}|^2 \Longrightarrow |V_{OV}| = 1\text{ V} \Longrightarrow V_{SG} = |V_{tp}| + |V_{OV}| = 1 + 1 = 2\text{ V}$$

$$V_G = 3\ V \Longrightarrow \text{A possible selection is } R_{G1} = 2\text{ M}\Omega \text{ and } R_{G2} = 3\text{ M}\Omega.$$

Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the PMOS transistor have $V_{tp} = -1$ V and $k_p'(W/L) = 1$ mA/V^2. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?

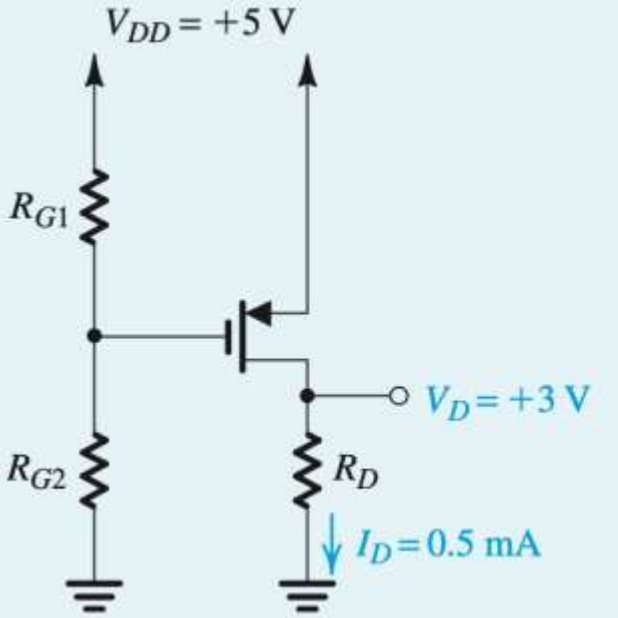


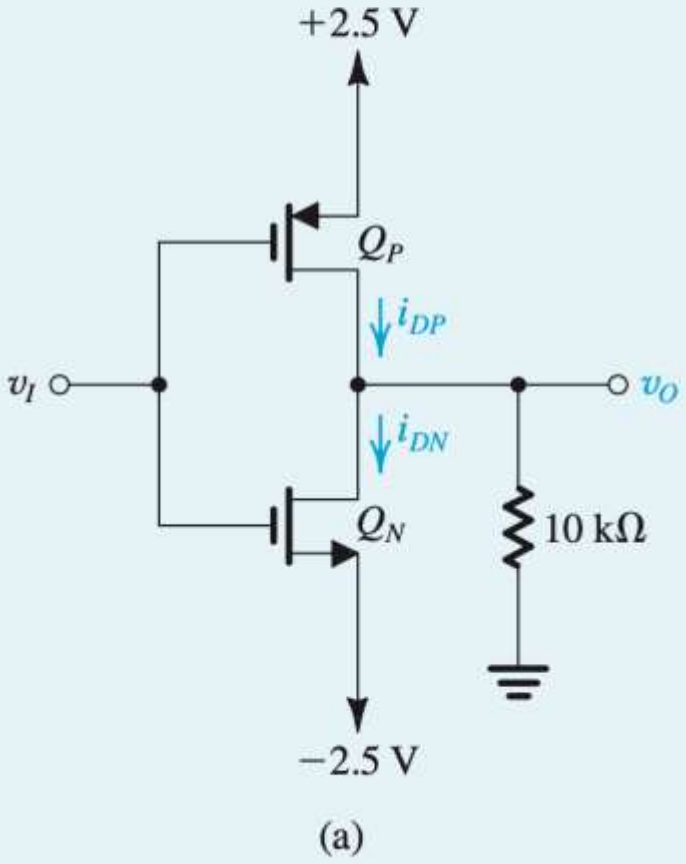
Figure 5.25 Circuit for Example 5.7.

②确保V_D的上限不超过 $V_G + |V_{TH}|$

$$V_{D\max} = 3 + 1 = 4 \text{ V} \quad \Rightarrow \quad R_D = \frac{4}{0.5} = 8 \text{ k}\Omega$$

Example 5.8

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0\ \text{V}$, $+2.5\ \text{V}$, and $-2.5\ \text{V}$.



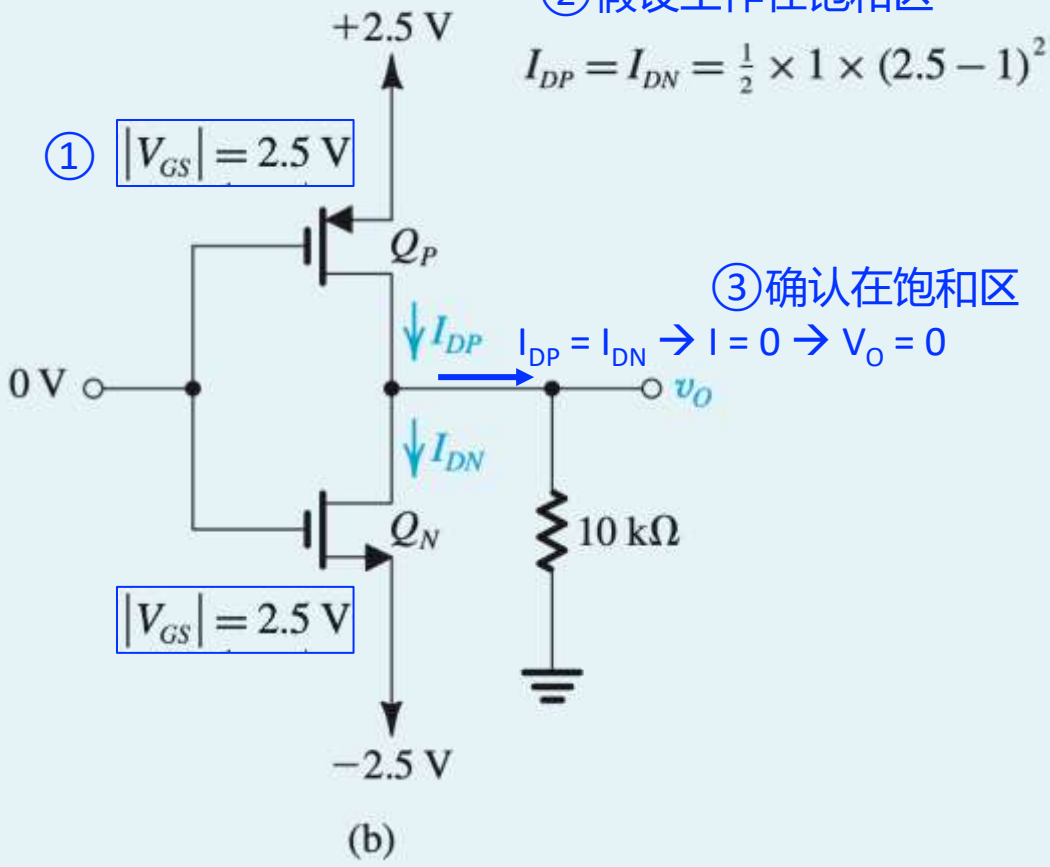
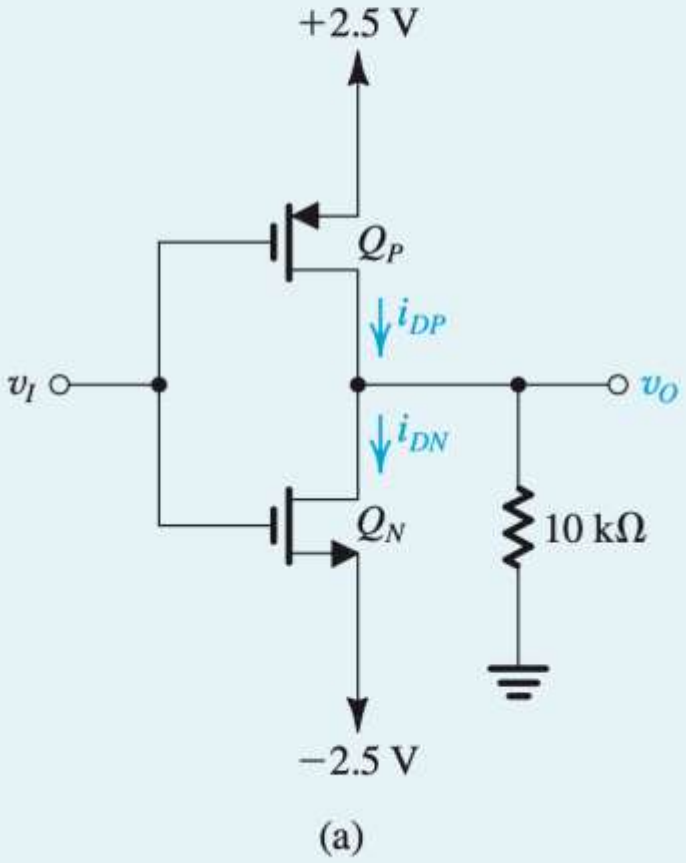


Figure 5.26 Circuits for Example 5.8.

Example 5.8

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0\ \text{V}$, $+2.5\ \text{V}$, and $-2.5\ \text{V}$.



① Q_P cut off

② $V_D < 0$ → 比 $V_G - V_{TH}$ 要低 → 工作在非饱和区

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right]$$

$$I_{DN}(\text{mA}) = \frac{0 - v_O}{10(\text{k}\Omega)}$$

$$I_{DN} = 0.244\ \text{mA}$$

$$v_O = -2.44\ \text{V}$$

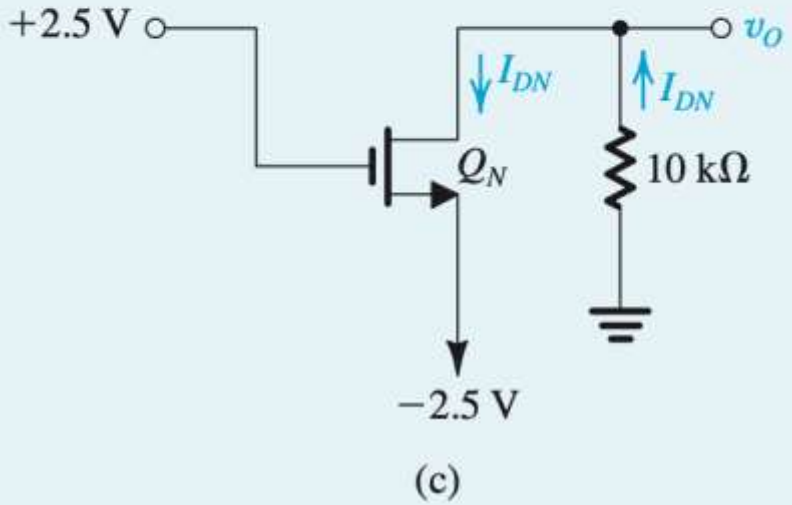
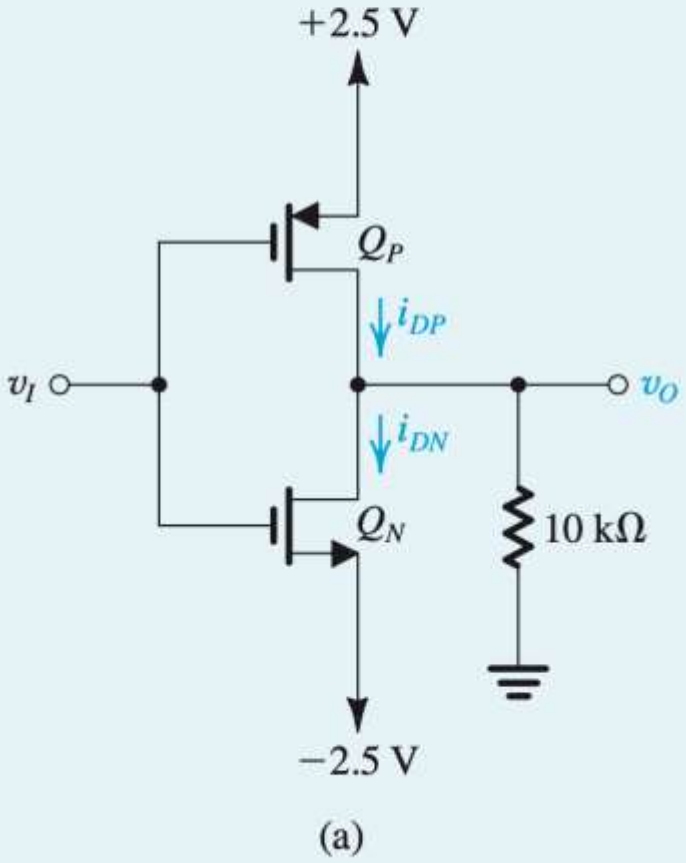


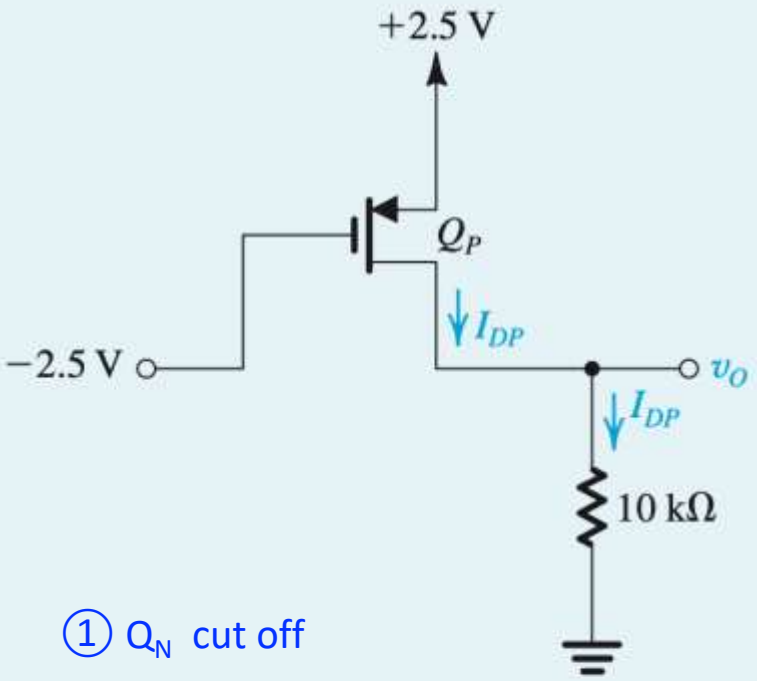
Figure 5.26 Circuits for Example 5.8.

Example 5.8

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0\ \text{V}$, $+2.5\ \text{V}$, and $-2.5\ \text{V}$.



(a)



① Q_N cut off

② $V_D > 0$ → 比 $V_G + |V_{TH}|$ 要高 → 工作在非饱和区

(d)

$$I_{DP} = 0.244\ \text{mA} \text{ and } v_O = +2.44\ \text{V}$$

Figure 5.26 Circuits for Example 5.8.

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D5.8 Redesign the circuit of Fig. 5.21 for the following case: $V_{DD} = -V_{SS} = 1\ \text{V}$, $V_t = 0.4\ \text{V}$, $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$, $W/L = 5\ \mu\text{m}/0.4\ \mu\text{m}$, $I_D = 100\ \mu\text{A}$, and $V_D = +0.2\ \text{V}$.

Ans. $R_D = 8\ \text{k}\Omega$; $R_S = 4\ \text{k}\Omega$

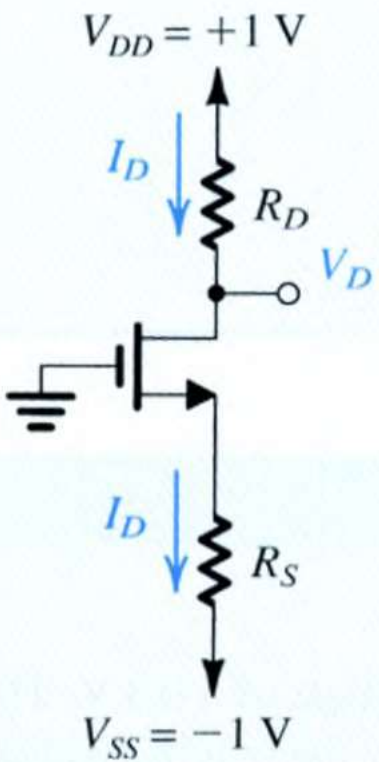


Figure 5.21 Circuit for Example 5.3.

D5.9 For the circuit in Fig. E5.9, find the value of R that results in $V_D = 0.7$ V. The MOSFET has $V_{tn} = 0.5$ V, $\mu_n C_{ox} = 0.4$ mA/V^2, $W/L = \dfrac{0.72\ \mu\text{m}}{0.18\ \mu\text{m}}$, and $\lambda = 0$.

Ans. 34.4 kΩ

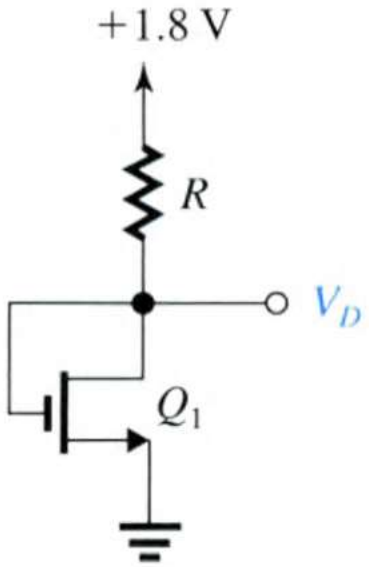
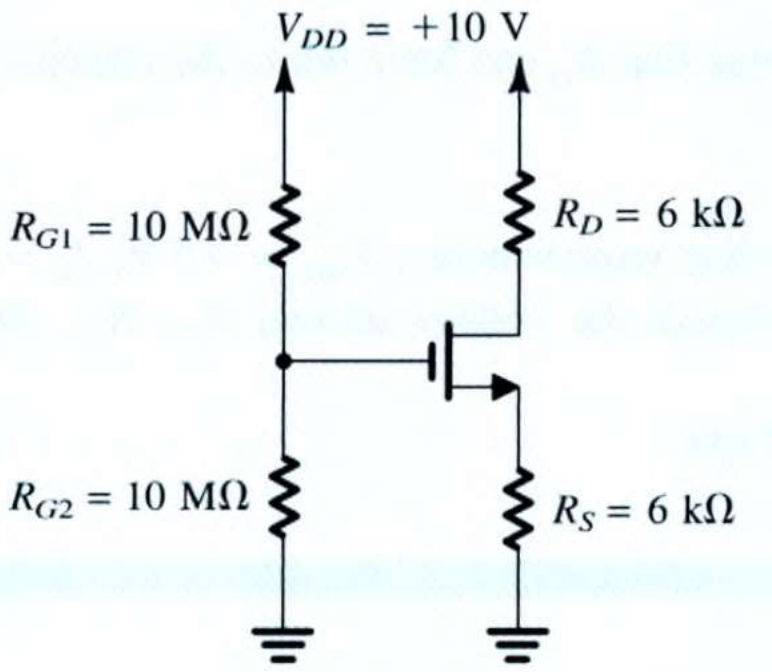


Figure E5.9

5.12 For the circuit of Fig. 5.24, what is the largest value that R_D can have while the transistor remains in the saturation mode?

Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2

Ans. 12 kΩ



D5.14 For the circuit in Fig. E5.14, find the value of R that casues the PMOS transistor to operate with an overdrive voltage $|V_{OV}| = 0.6$ V. The threshold voltage is $V_{tp} = -0.4$ V, the process transconductance parameter $k_p' = 0.1$ mA/V^2, and $W/L = 10\,\mu\text{m}/0.18\,\mu\text{m}$.

Ans. 800 Ω

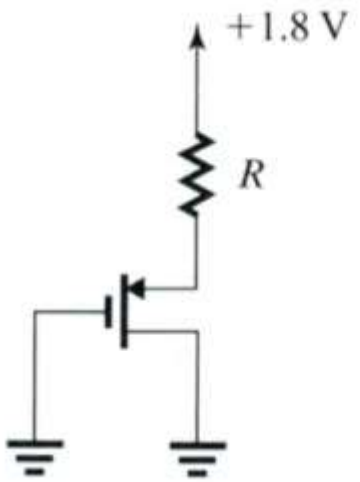


Figure E5.14