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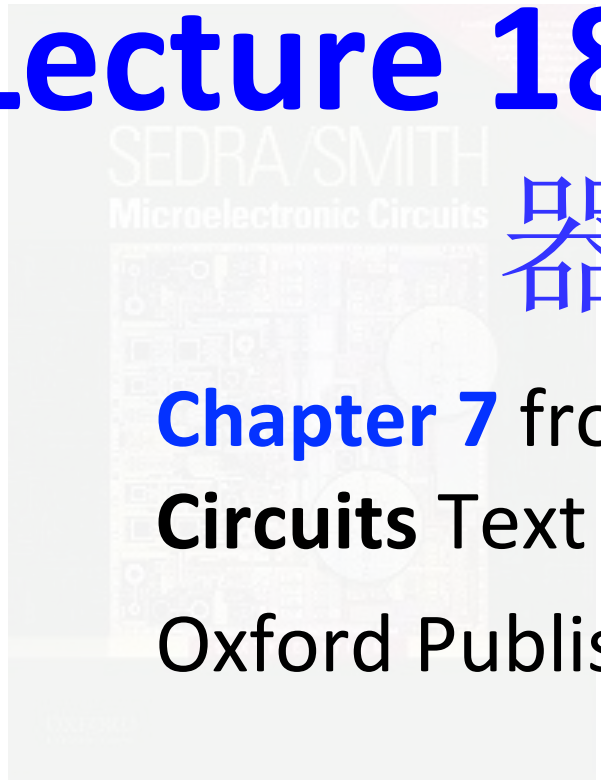
Lecture 18 – 晶体管放大器-part1



Chapter 7 from **Microelectronic Circuits** Text by Sedra and Smith

Oxford Publishing

- 8.2.2 π型和T型等效电路（中频）
- 8.3 场效应晶体管放大电路的构成及其分析
- 8.3.1 直流偏置电路及其分析
- 8.3.2 三种接法放大电路的分析计算

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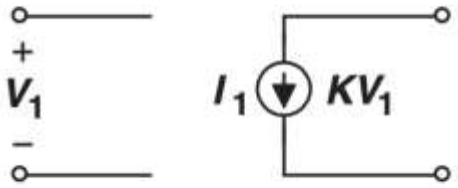
- 9.3 三极管放大电路的构成及其分析
- 9.3.1 直流偏置电路及其分析
- 9.3.2 三种接法放大电路的分析计算

7.1 晶体管放大器设计基础

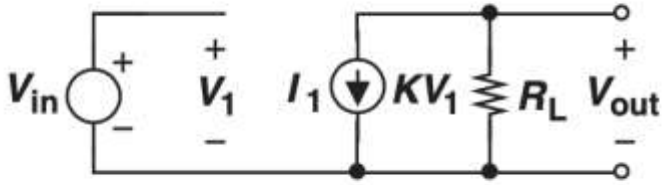
- 基于“压控电流源”，可构建放大器电路



①理想压控电流源 $I_1 = KV_1$

输入阻抗∞

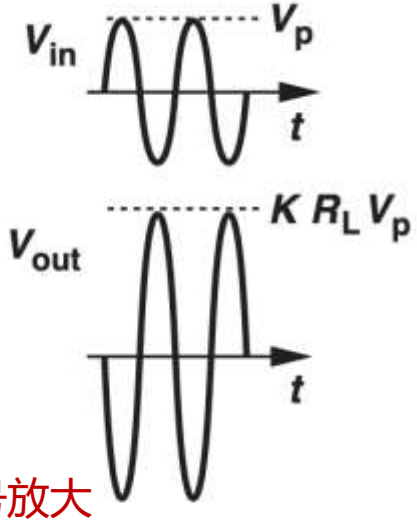
(a)



②接上R_L作为负载，则R_L两端的电压为：

$V_{out} = -KR_L V_{in}$ 若 $KR_L > 1$，则实现信号放大

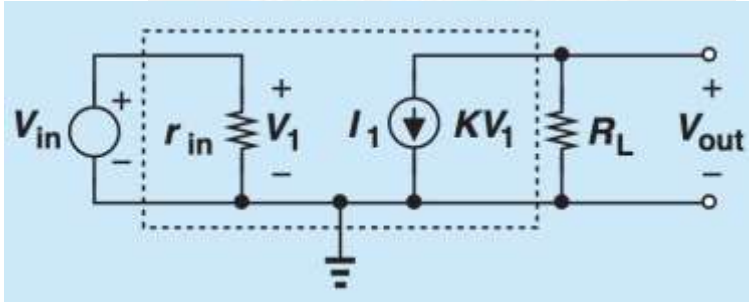
(b)



电压增益： $A_V = \dfrac{V_{out}}{V_{in}} = -KR_L$

Figure 4.1 (a) Voltage-dependent current source, (b) simple amplifier.

线性压控电流源 K→线性电压放大器



若压控电流源具有输入电阻 r_{in}

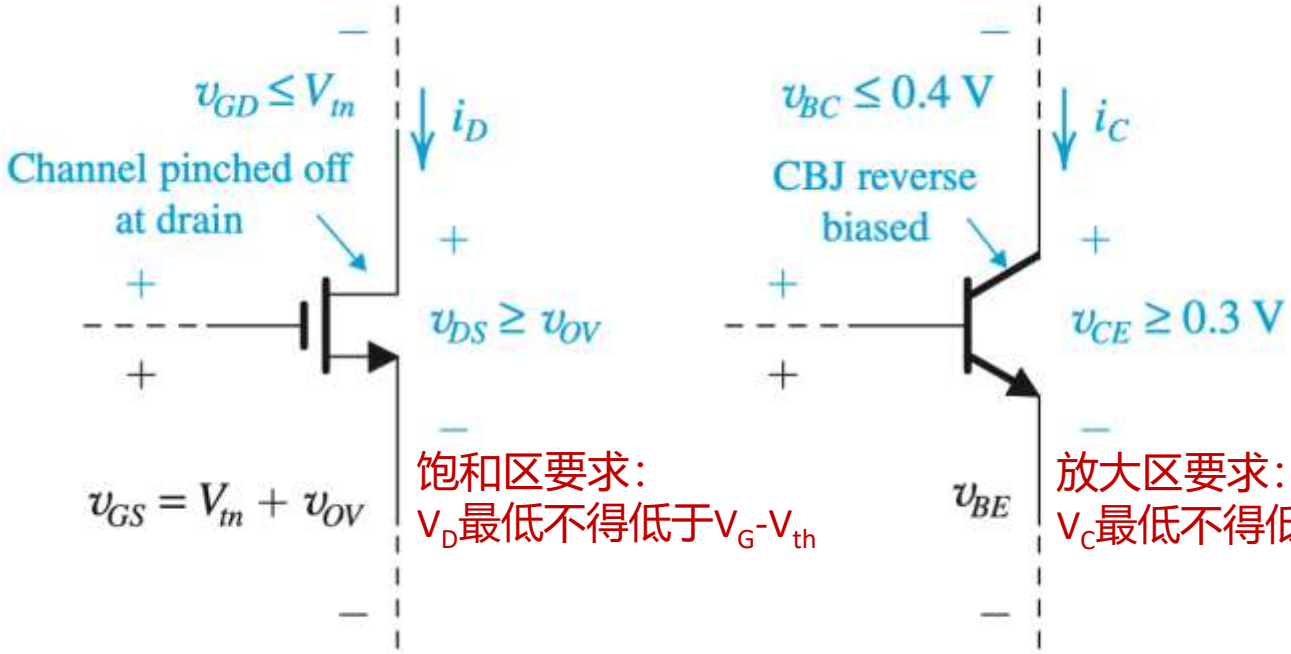
$V_1 = V_{in}$ 增益没有影响

Q：如果信号源V_{in}具有内阻 r_s 呢

A：V_1是V_{in}的分压，V_{out}/V_{in} 降低

晶体管放大器设计基础

- MOSFET 和 BJT 都可以实现“压控电流源”，因此，都可以用来构建放大器



饱和区要求：
V_D最低不得低于V_G-V_{th}

放大区要求：
V_C最低不得低于V_B-0.4V

$i_D = \frac{1}{2} k_n (v_{GS} - V_{tn})^2$

$i_C = I_S e^{v_{BE}/V_T}$

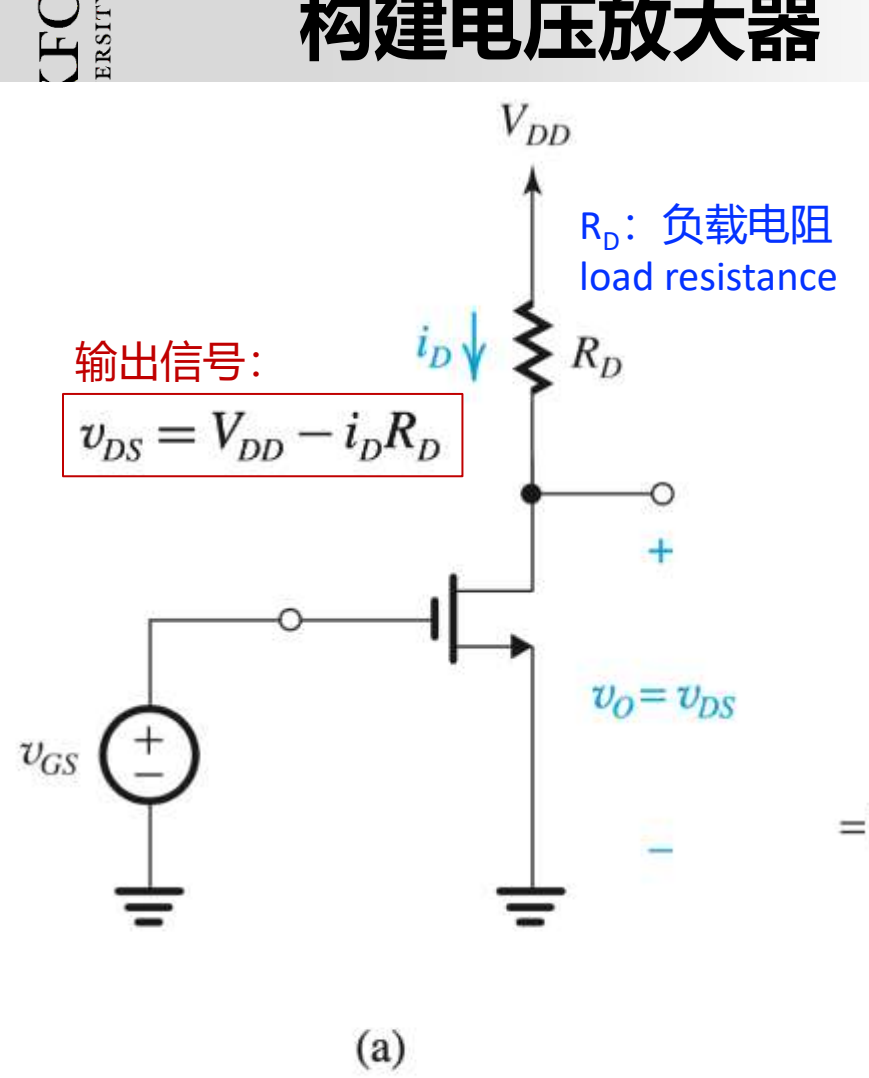
平方关系 → 需要线性化 $i = Kv$ ← 指数关系

本质上都是跨导放大器，输入电压信号，输出电流信号

Q：如何实现电压放大器?

A：通过电阻把电流转化为电压

构建电压放大器



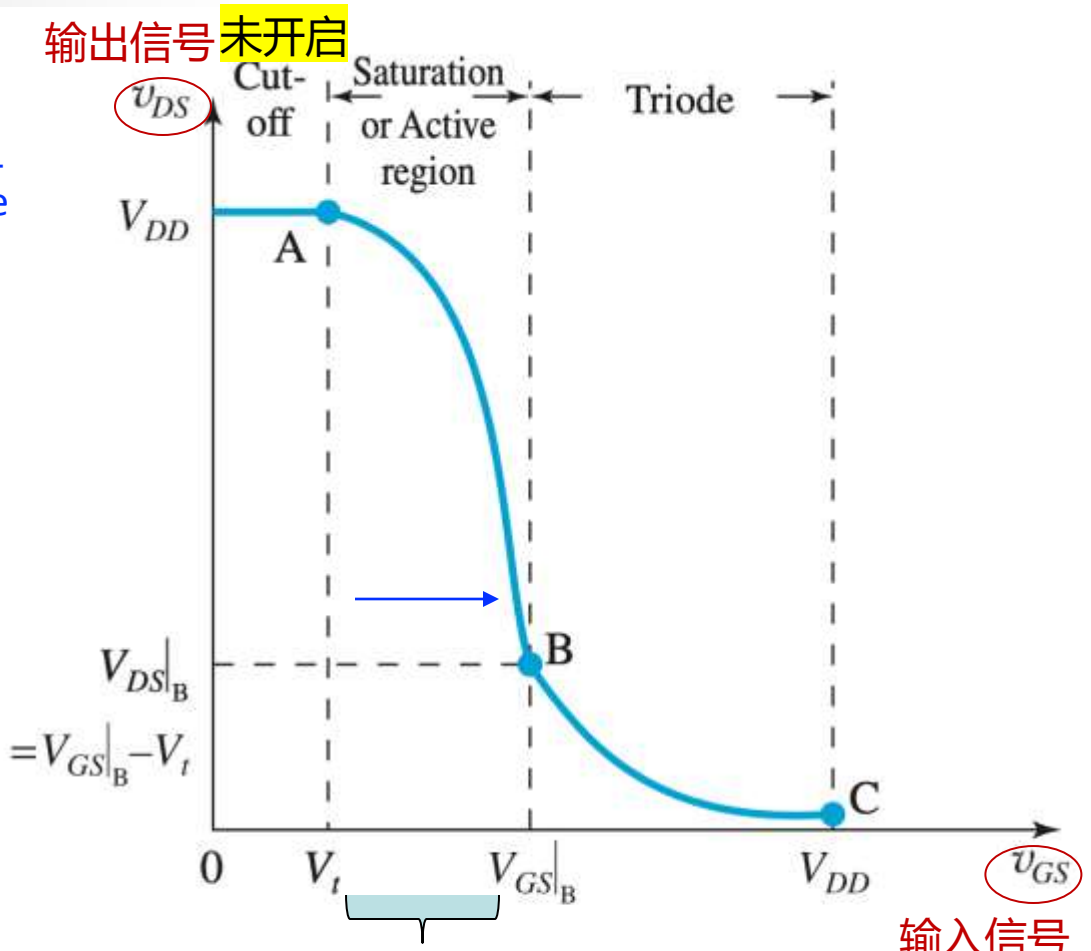
R_D：负载电阻
load resistance

输出信号：

$$v_{DS} = V_{DD} - i_D R_D$$

The Voltage-Transfer Characteristic (VTC)

输出信号未开启



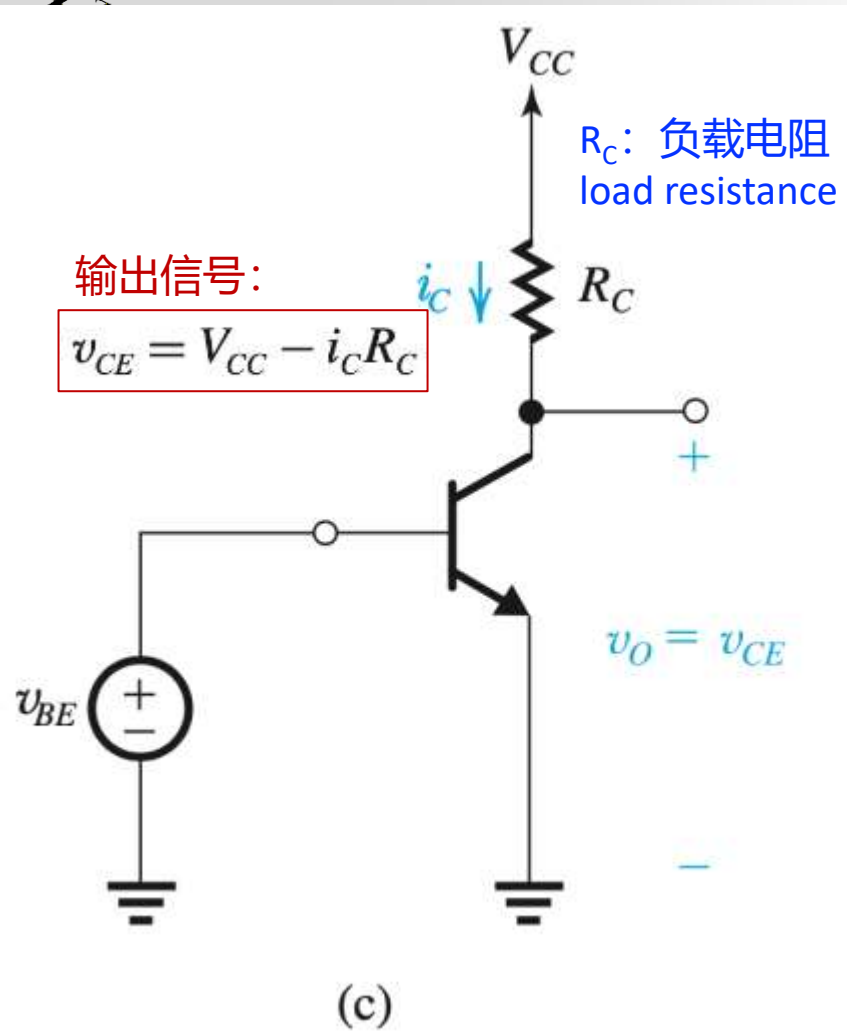
V_{GS}增加→i_D增加 →V_{DS}减小，逐渐趋向于离开饱和区

Figure 7.2 (**a**) An NMOS amplifier and (**b**) its VTC; and (**c**) an *npn* amplifier and (**d**) its VTC.

AB区域为放大器工作区域，输入信号的微小变化将放大，放大倍数为AB曲线上某一点的斜率，该点称为**直流工作点/偏置点/静态点**（Q, quiescent）。若要实现线性放大，需在Q点附近做线性化近似。

构建电压放大器

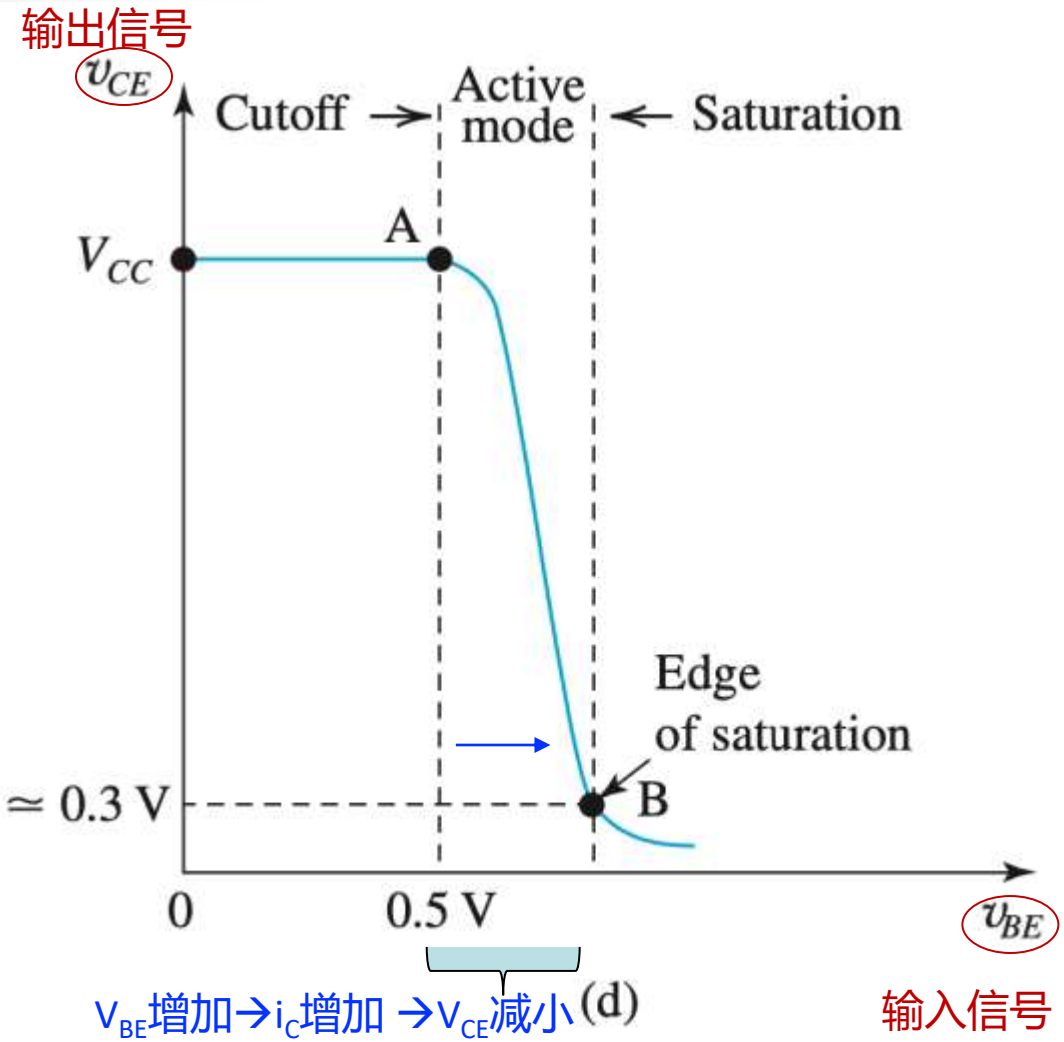
The Voltage-Transfer Characteristic (VTC)



R_C：负载电阻
load resistance

输出信号：

$$v_{CE} = V_{CC} - i_C R_C$$



V_{BE}增加→i_C增加 →V_{CE}减小，逐渐趋向于离开放大区

输入信号

AB区域为放大器工作区域，输入信号的微小变化将放大，放大倍数为AB曲线上某一点的斜率，该点称为**直流工作点/偏置点/静态点**（Q, quiescent）。若要实现线性放大，需在Q点附近做线性化近似。

偏置（Bias）

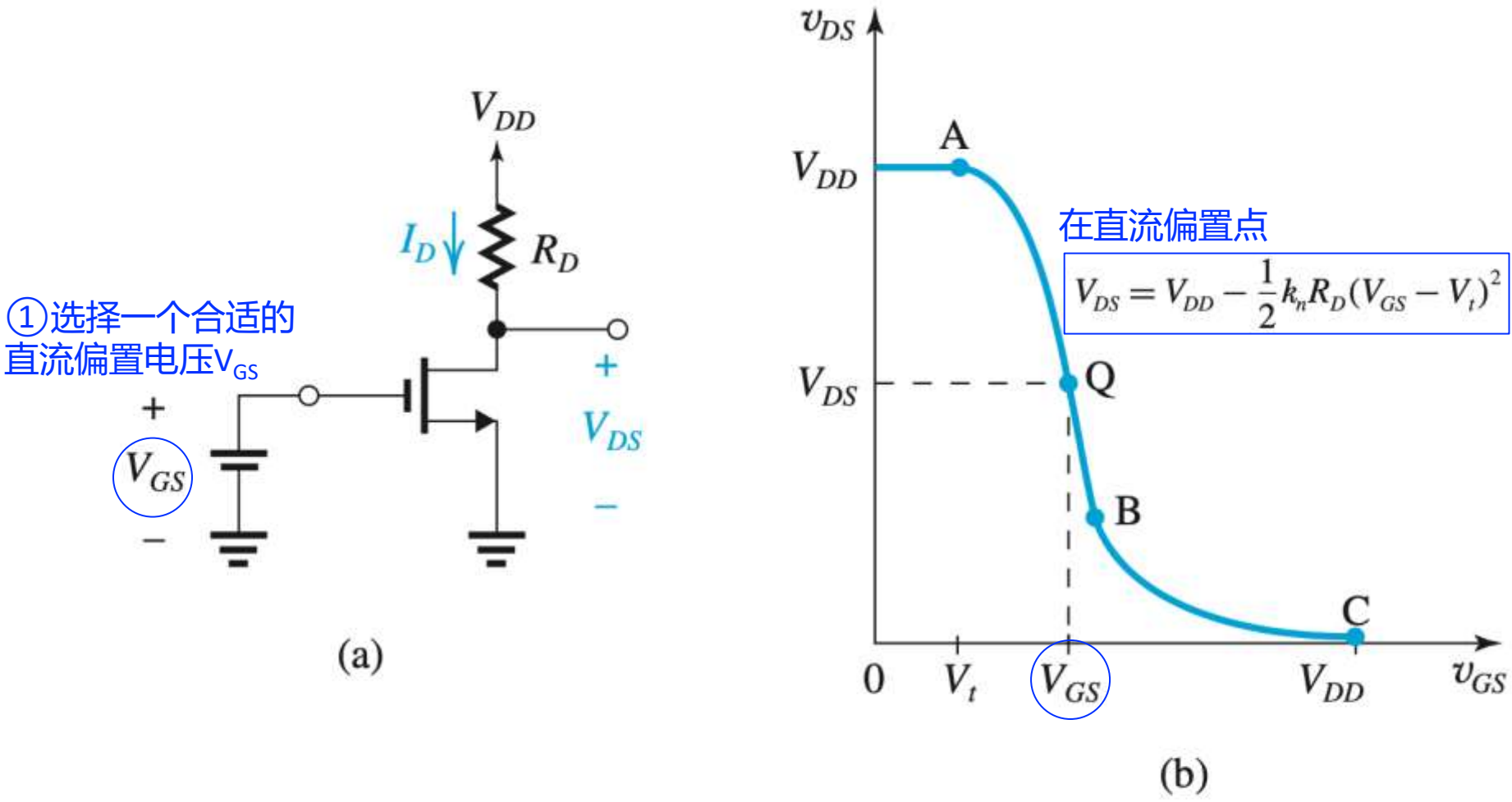
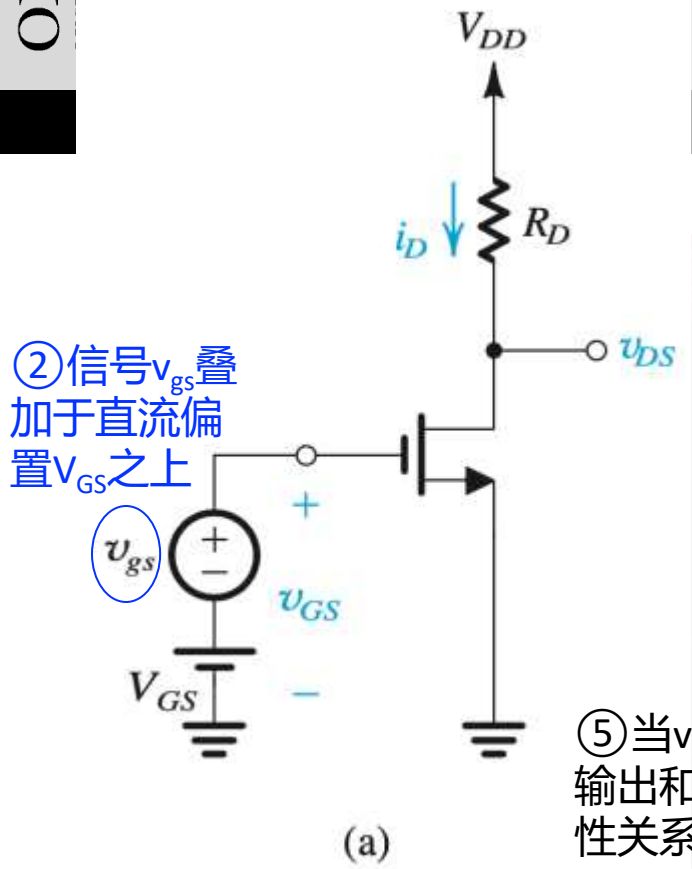
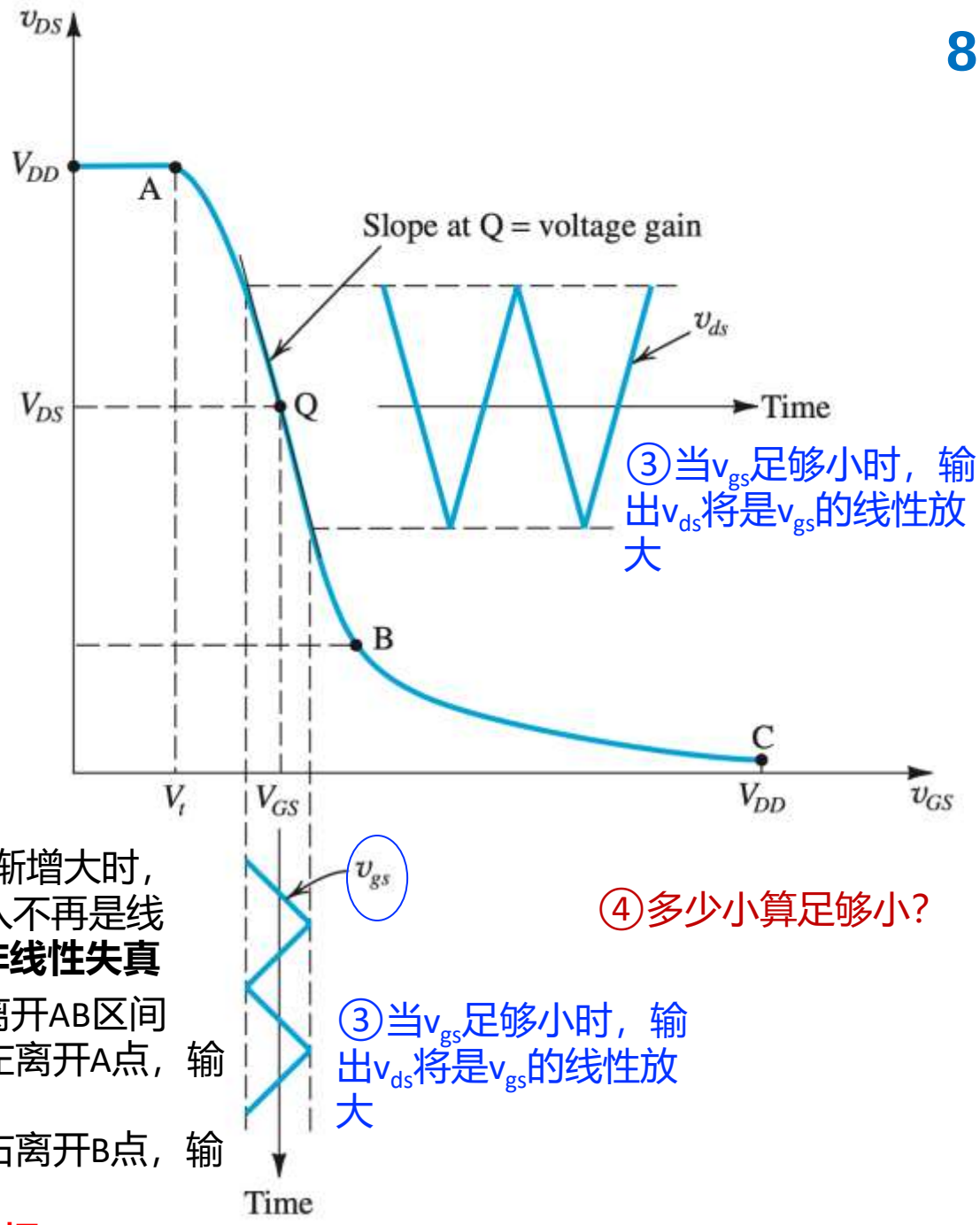


Figure 7.3 Biasing the MOSFET amplifier at a point Q located on the segment AB of the VTC.

偏置（Bias）



②信号v_{gs}叠加于直流偏置V_{GS}之上



③当v_{gs}足够小时，输出v_{ds}将是v_{gs}的线性放大

④多少小算足够小？

⑤当v_{gs}逐渐增大时，输出和输入不再是线性关系—**非线性失真**

⑥当v_{gs}足够大时，瞬时工作点有可能会离开AB区间

- v_{gs}为负的较大值时，瞬时工作点会往左离开A点，输出限制在最大值V_{DD}
- v_{gs}为正的较大值时，瞬时工作点会往右离开B点，输出限制在较小值；
- Q点的选择决定了**输出所允许的最大摆幅（swing）**

多少小算足够小?

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_{TH})^2 \qquad v_{GS} = V_{GS} + v_{gs}$$

瞬时总量　直流量　小信号量

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH}+v_{gs})^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{OV}^2 + v_{gs}^2 + 2V_{OV}v_{gs}]$$

小信号近似前提：$v_{gs} \ll 2V_{OV}$

$$i_D = I_D + \mu_n C_{ox}\frac{W}{L}V_{OV}v_{gs}$$

定义为跨导g_m

瞬时总量　直流量　小信号量i_d，v_{gs}的线性放大

$$i_C = I_S e^{v_{BE}/V_T} \qquad v_{BE} = V_{BE} + v_{be}$$

瞬时总量　直流量　小信号量

$$i_C = I_S e^{(V_{BE}+v_{be})/V_T} = I_S e^{V_{BE}/V_T}\cdot e^{v_{be}/V_T}$$

$$= I_S e^{V_{BE}/V_T}\left[1 + v_{be}/V_T + \frac{(v_{be}/V_T)^2}{2!} + \cdots\right]$$

小信号近似前提：$v_{be} \ll V_T$

$$i_C = I_C + \frac{I_C}{V_T}v_{be}$$

定义为跨导g_m

瞬时总量　直流量　小信号量i_c，v_{be}的线性放大

跨导 g_m

g_m表示小信号$v_{gs}(v_{be})$到小信号$i_d(i_c)$的放大能力，所以是**小信号参数**

$$i_D = I_D + \mu_n C_{ox}\frac{W}{L}V_{OV}v_{gs}$$

瞬时总量　直流量　定义为跨导g_m　小信号量i_d，v_{gs}的线性放大

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$g_m = \mu_n C_{ox}\frac{W}{L}V_{OV}$$ **Gate Bias**

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$ **Drain Current Bias**

$$g_m = \frac{I_D}{V_{OV}/2}$$ **Drain Current and Gate Bias**

$$i_C = I_C + \frac{I_C}{V_T}v_{be}$$

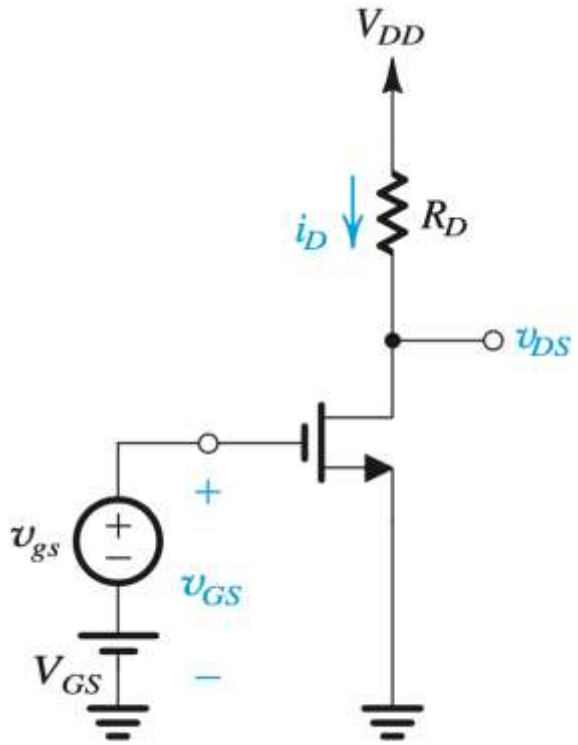
瞬时总量　直流量　定义为跨导g_m　小信号量i_c，v_{be}的线性放大

$$I_C = I_S e^{V_{BE}/V_T}$$

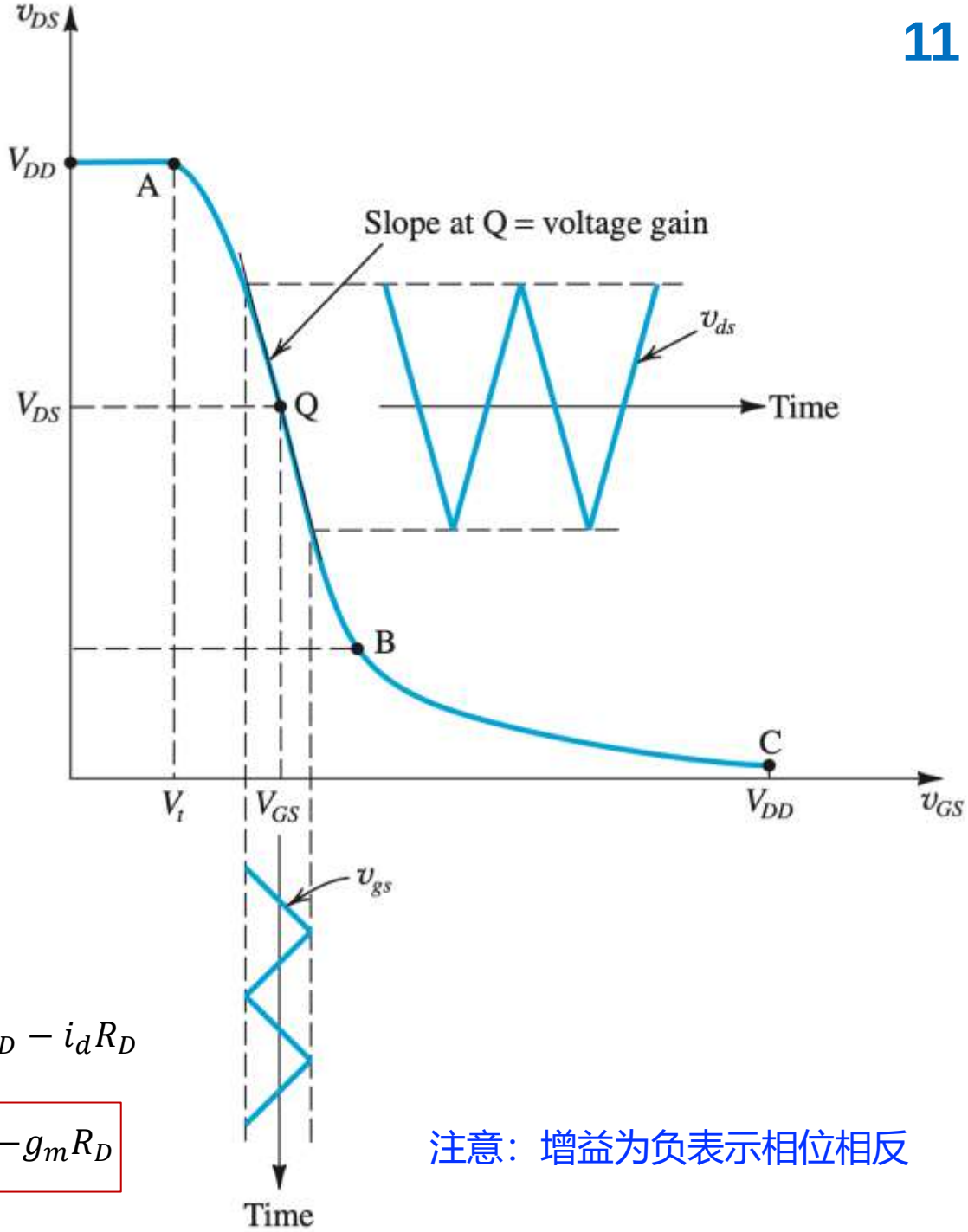
$$g_m = \frac{I_C}{V_T}$$

1. 小信号参数是根据**直流量**（V_{OV}、I_D、I_C）计算的
2. **MOSFET 的$V_{OV}/2$ 相当于BJT的V_T**
3. 一般而言V_T比$V_{OV}/2$要小，所以一般情况下BJT的跨导（增益）比MOSFET要大

小信号电压增益A_V



(a)



$$v_{DS} = V_{DD} - i_D R_D$$

$$= V_{DD} - (I_D + i_d)R_D \quad = V_{DD} - I_D R_D - i_d R_D$$

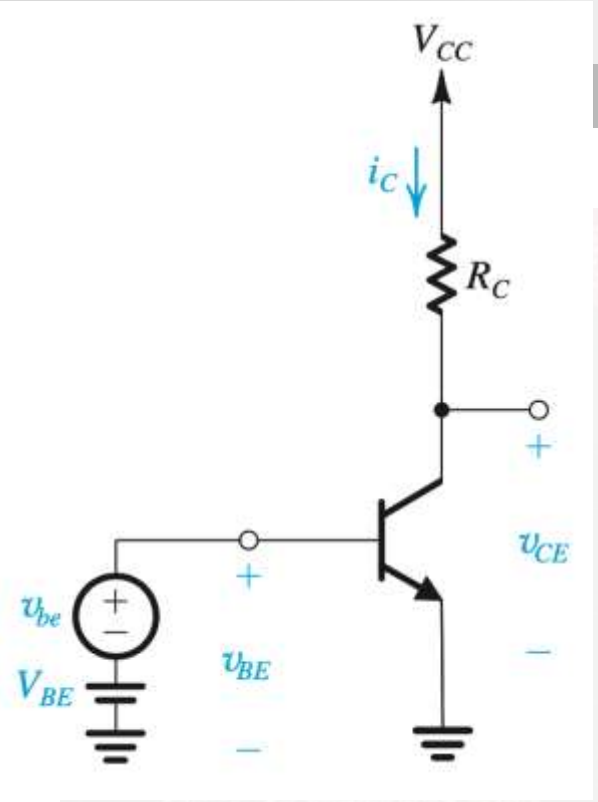
$$= V_{DS} - g_m v_{gs} R_D$$

$$v_{ds}$$

$$A_v = \frac{v_{ds}}{v_{gs}} = -g_m R_D$$

注意：增益为负表示相位相反

小信号电压增益A_V



$$v_{CE} = V_{CC} - i_C R_C$$
$$= V_{CC} - (I_C + i_c)R_C \quad = V_{CC} - I_C R_C - i_c R_C$$
$$= V_{CE} - g_m v_{be} R_C$$

$$\frac{}{v_{ce}}$$

$$A_v = \frac{v_{ce}}{v_{be}} = -g_m R_C$$

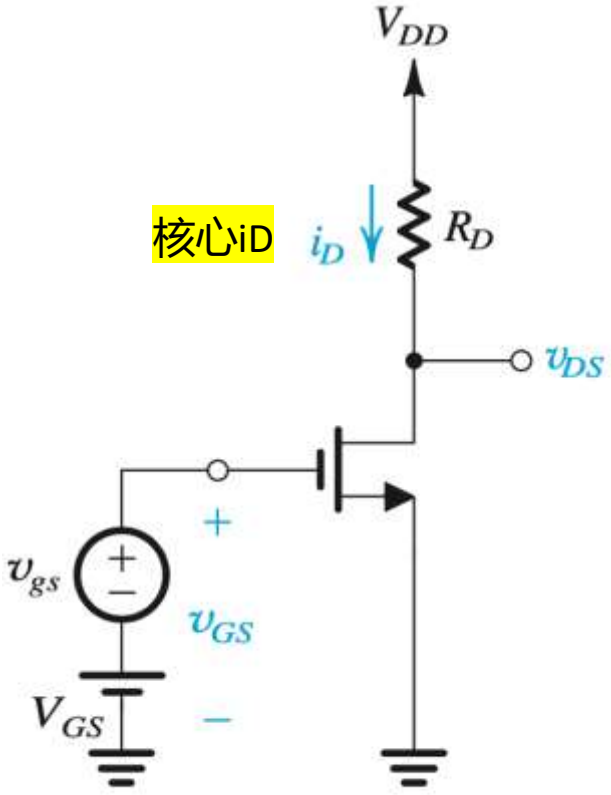
注意：增益为负表示相位相反

Example 7.1

Consider the amplifier circuit shown in Fig. 7.4(a). The transistor is specified to have $V_t = 0.4$ V, $k_n' = 0.4$ mA/V^2, $W/L = 10$, and $\lambda = 0$. Also, let $V_{DD} = 1.8$ V, $R_D = 17.5$ kΩ, and $V_{GS} = 0.6$ V.

(a) For $v_{gs} = 0$ (and hence $v_{ds} = 0$), find V_{OV}, I_D, V_{DS}, and A_v.

(b) What is the maximum symmetrical signal swing allowed at the drain? Hence, find the maximum allowable amplitude of a sinusoidal v_{gs}.



核心iD

$$V_{OV} = 0.6 - 0.4 = 0.2 \text{ V}$$

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2$$
$$= \frac{1}{2} \times 0.4 \times 10 \times 0.2^2 = 0.08 \text{ mA}$$

$$V_{DS} = V_{DD} - R_D I_D$$
$$= 1.8 - 17.5 \times 0.08 = 0.4 \text{ V}$$

$0.4 > 0.6 - V_t$，工作在饱和区

$$A_v = -k_n V_{OV} R_D$$
$$= -0.4 \times 10 \times 0.2 \times 17.5$$
$$= -14 \text{ V/V}$$

Example 7.1

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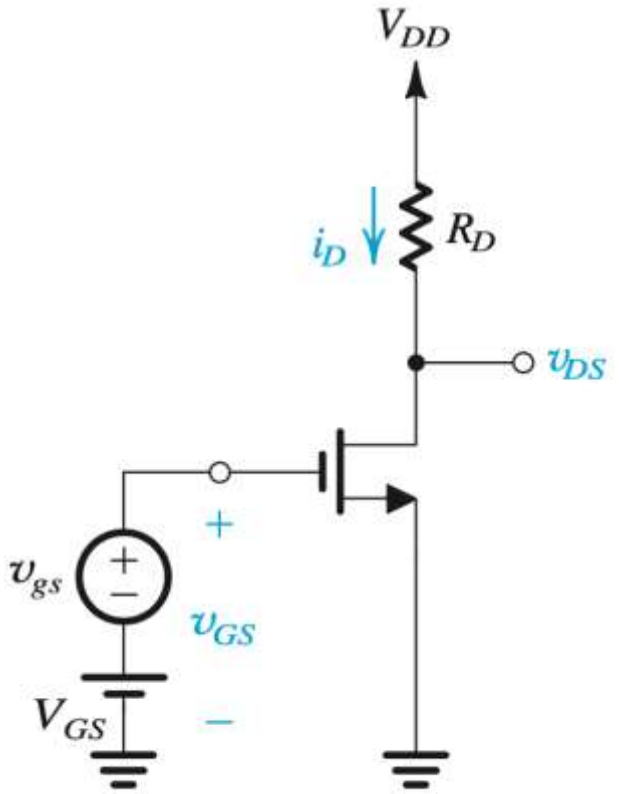

V_{DS} = 0.4V，工作在饱和区的下限是0.2V，所以叠加在V_{DS}上的v_{ds}向下最多能摆动0.2V；上限是V_{DD}，所以向上最多能摆动1.8 - 0.4= 1.4V。所以允许的最大的对称摆幅是 **±0.2V**

对应的 $$\hat{v}_{gs} = \frac{\hat{v}_{ds}}{|A_v|} = \frac{0.2\text{ V}}{14} = 14.2\text{ mV}$$

$v_{gs} \ll 2V_{OV}$ 满足小信号近似条件

Consider the amplifier circuit shown in Fig. 7.4(a). The transistor is specified to have $V_t = 0.4$ V, $k_n' = 0.4$ mA/V^2, $W/L = 10$, and $\lambda = 0$. Also, let $V_{DD} = 1.8$ V, $R_D = 17.5$ kΩ, and $V_{GS} = 0.6$ V.

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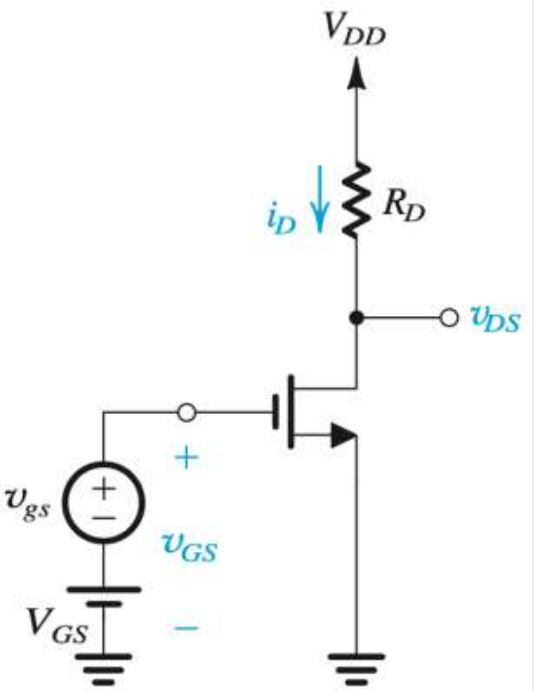
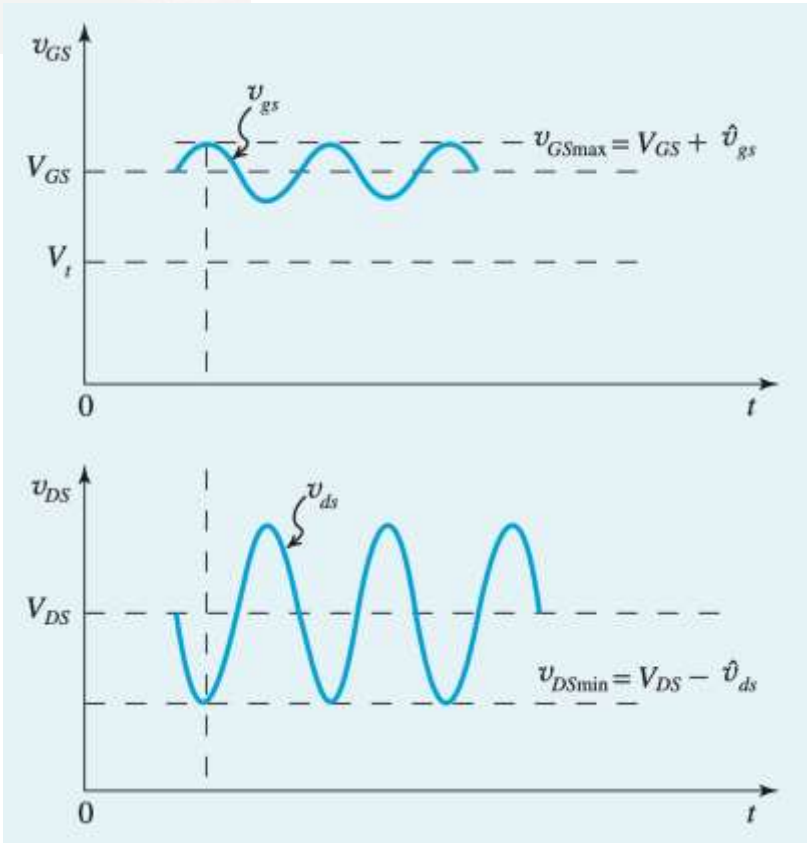




更严谨的分析：v_D最小时，v_G最大，v_D最低不得低于$v_G - V_{TH}$

$$v_{DSmin} \geq v_{GSmax} - V_t$$

$$0.4 - |A_v|\hat{v}_{gs} \geq 0.6 + \hat{v}_{gs} - 0.4$$

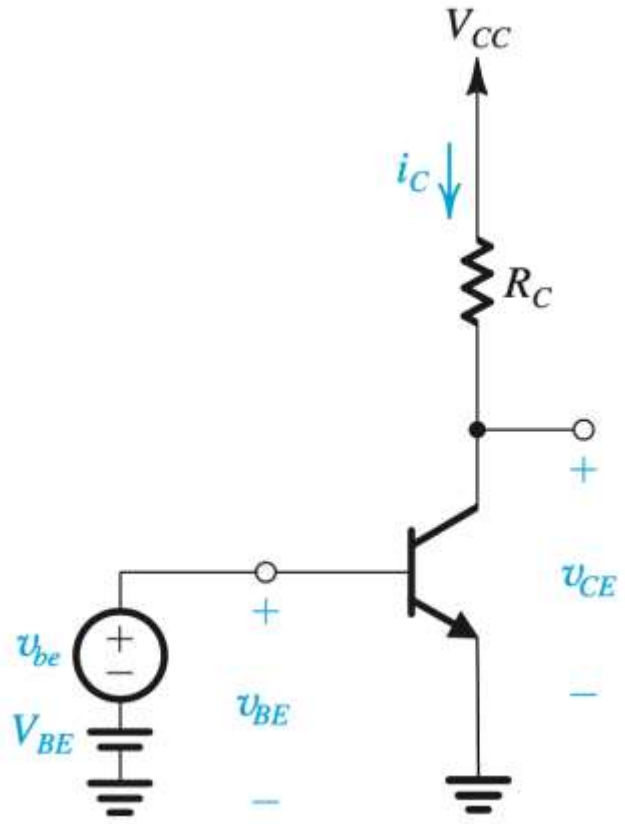
$$\hat{v}_{gs} \leq \frac{0.2}{|A_v| + 1} = 13.3 \text{ mV}$$

临界对应的v_{ds}为 186 mV 与 0.2V 差别不大

Example 7.2

Consider an amplifier circuit using a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8\ \text{k}\Omega$, and a power supply $V_{CC} = 10$ V.

(a) Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of I_C?



(a)

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$= \frac{10 - 3.2}{6.8} = 1\ \text{mA}$$

The value of V_{BE} can be determined from

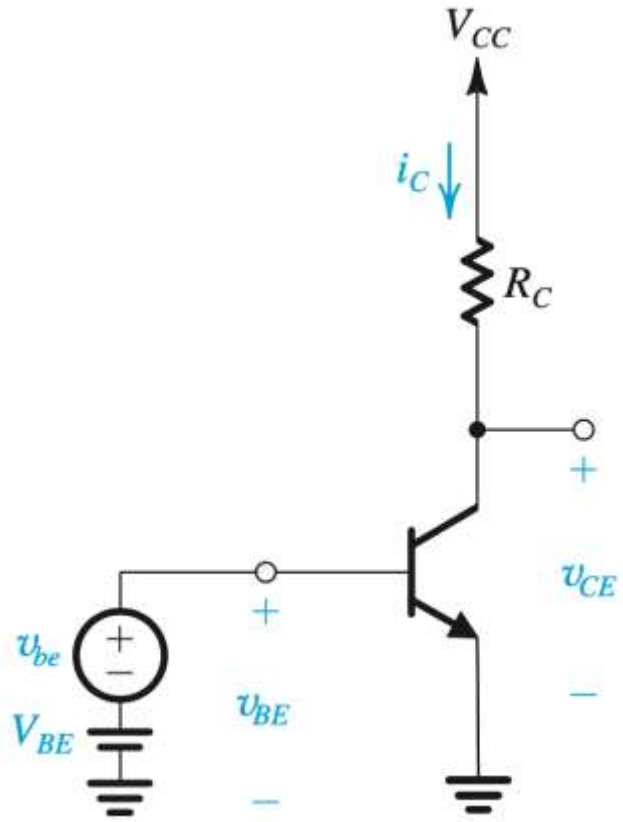
$$1 \times 10^{-3} = 10^{-15}\, e^{V_{BE}/V_T}$$

which results in

$$V_{BE} = 690.8\ \text{mV}$$

Consider an amplifier circuit using a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8\ \text{k}\Omega$, and a power supply $V_{CC} = 10$ V.

(b) Find the voltage gain A_v at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE}, find the amplitude of the output sine-wave signal (assume linear operation).



(b)

$$A_v = -\frac{V_{CC} - V_{CE}}{V_T}$$

$$= \frac{10 - 3.2}{0.025} = -272\ \text{V/V}$$

$$\hat{v}_{ce} = 272 \times 0.005 = 1.36\ \text{V}$$

$$g_m = \frac{I_C}{V_T} = \frac{1\ \text{mA}}{25\ \text{mV}}$$

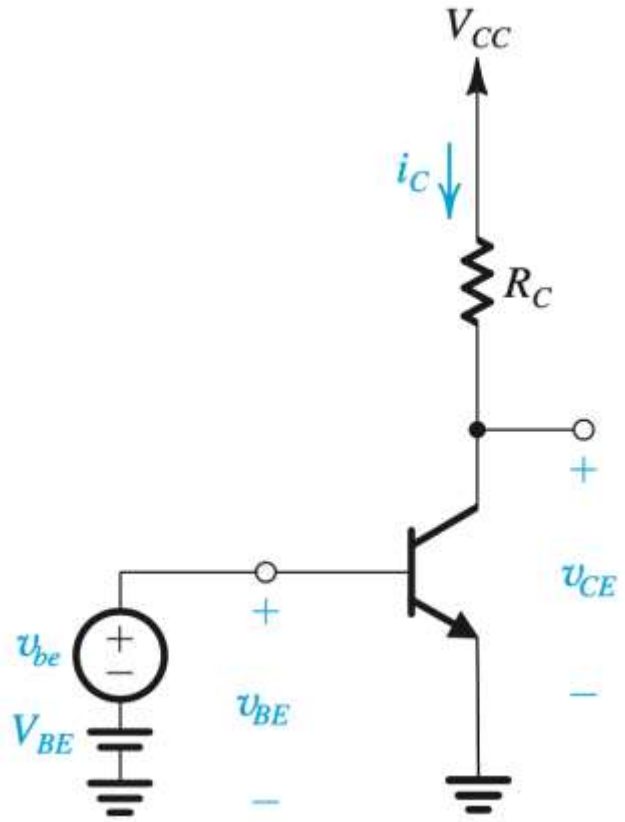
先根据直流量计算出小信号参数g_m

$$A_v = -g_m R_C = -\frac{1}{25} \cdot 6.8k = -272\ V/V$$

5mV符合 $v_{be} \ll V_T$ 的小信号前提

Consider an amplifier circuit using a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8\ \text{k}\Omega$, and a power supply $V_{CC} = 10$ V.

(c) Find the positive increment in v_{BE} (above V_{BE}) that drives the transistor to the edge of saturation, where $v_{CE} = 0.3$ V.



(c) For $v_{CE} = 0.3$ V,

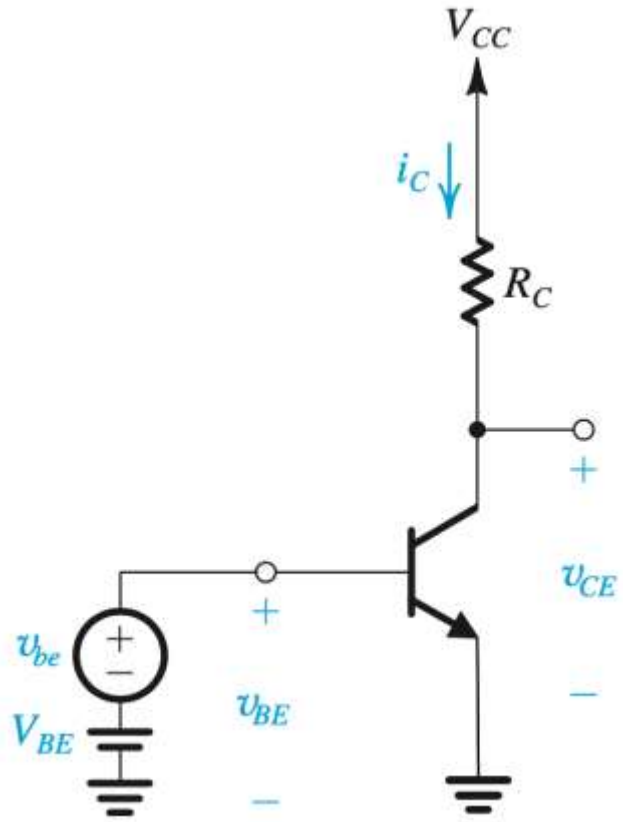
$$i_C = \frac{10 - 0.3}{6.8} = 1.617\ \text{mA}$$

To increase i_C from 1 mA to 1.617 mA, v_{BE} must be increased by

$$\Delta v_{BE} = V_T \ln\left(\frac{1.617}{1}\right) = 12\ \text{mV}$$

Consider an amplifier circuit using a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8\ \text{k}\Omega$, and a power supply $V_{CC} = 10$ V.

(d) Find the negative increment in v_{BE} that drives the transistor to within 1% of cutoff (i.e., to $v_{CE} = 0.99V_{CC}$).



(d) For $v_{CE} = 0.99V_{CC} = 9.9$ V,

$$i_C = \frac{10 - 9.9}{6.8} = 0.0147\ \text{mA}$$

To decrease i_C from 1 mA to 0.0147 mA, v_{BE} must change by

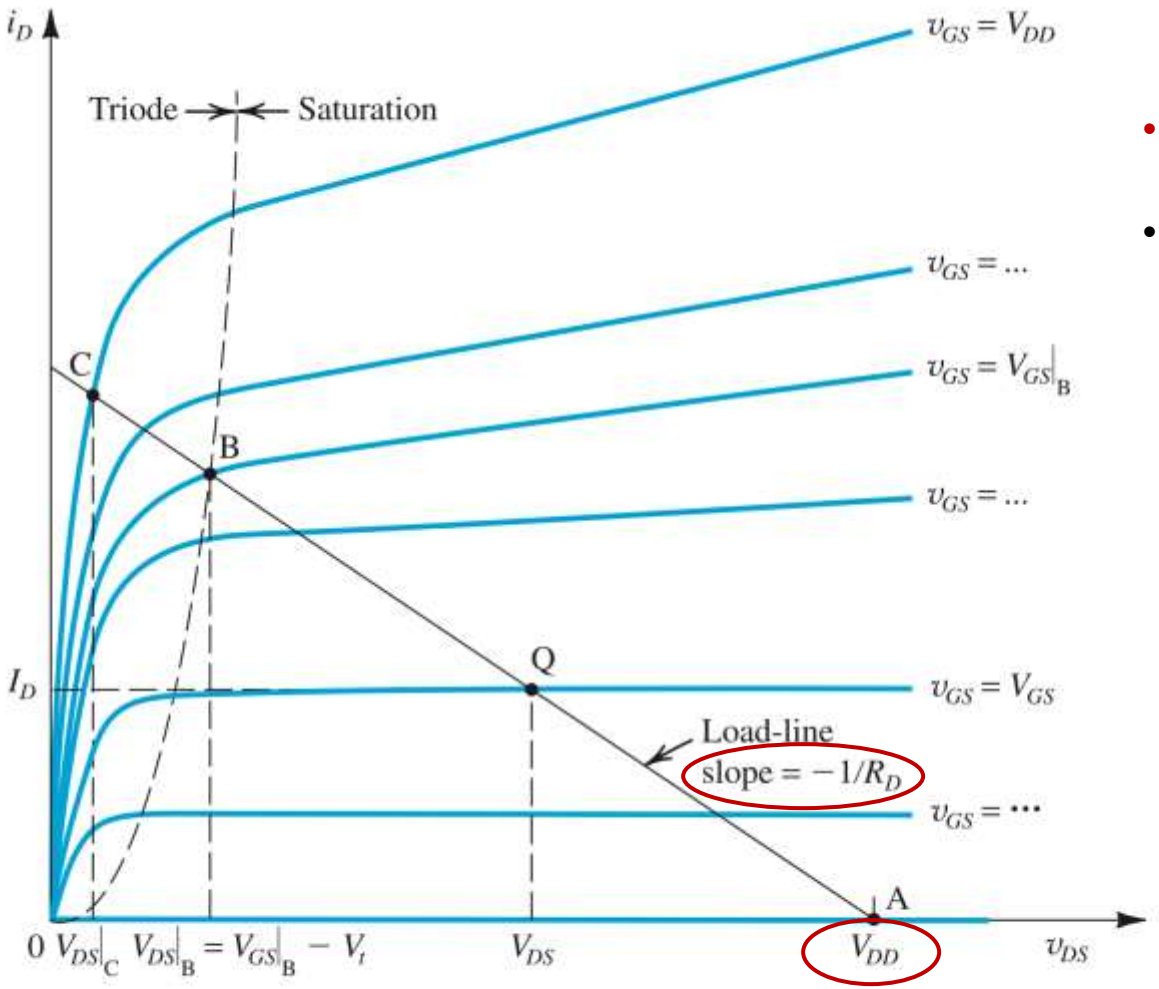
$$\Delta v_{BE} = V_T \ln\left(\frac{0.0147}{1}\right)$$
$$= -105.5\ \text{mV}$$

图示法

- **蓝色曲线**为MOSFET的“电压电流约束关系”
- **黑色曲线**（直线）为外围电路的约束，称为“**load line**”

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS}$$

- **两曲线相交点**即为工作点**Q**
- Load line与横坐标截距为V_{DD}，斜率为$-1/R_D$，所以Q点由V_{GS}和R_D所决定



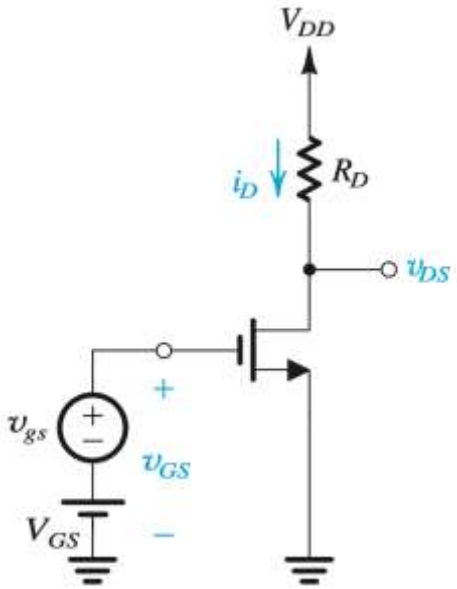
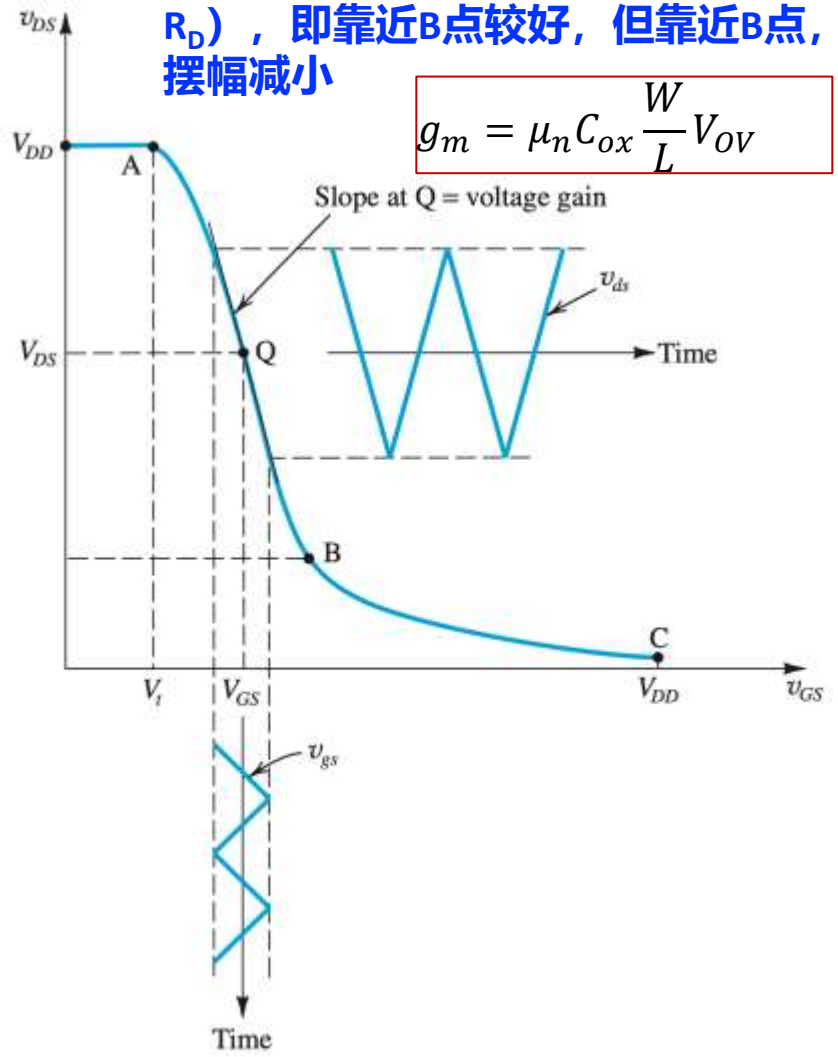


Figure 7.7 Graphical construction to determine the voltage-transfer characteristic of the amplifier in Fig. 7.4(a).

工作点对小信号增益和输出摆幅的影响

①考虑小信号增益，V_{GS}大比较好（固定R_D），即靠近B点较好，但靠近B点，输出摆幅减小

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV}$$



②考虑输出信号摆幅（固定V_{GS}）

- Q_1点（R_D小）离V_{DD}太近，输出信号向上摆幅的空间（headroom）不够
- Q_2点（R_D大）离非饱和区太近，输出信号向下摆幅的空间（legroom）不够

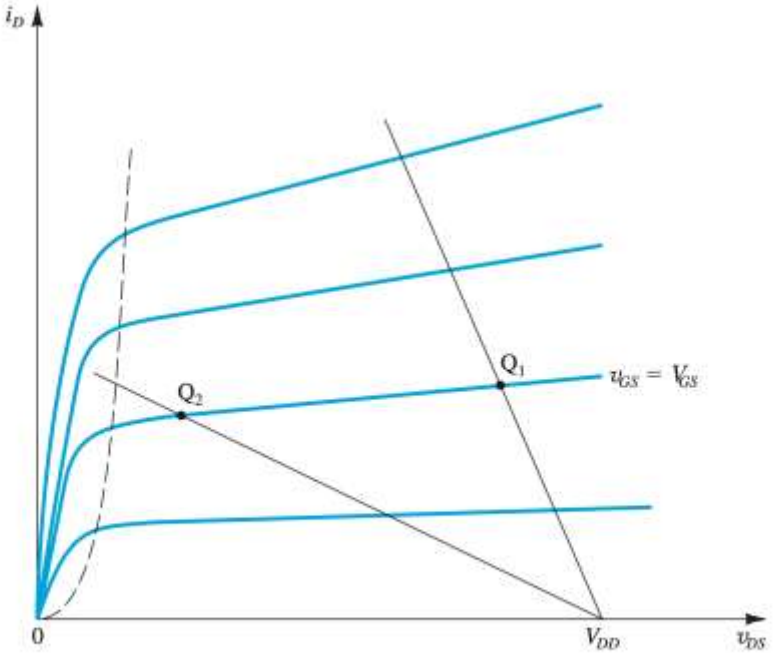


Figure 7.9 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

7.2 小信号工作与模型

- MOSFET 和 BJT 本质上都是压控电流源
  - 输入信号v_{GS}（v_{BE}）的瞬时总量可以拆分成直流量+小信号量

$$v_{GS} = V_{GS} + v_{gs} \qquad v_{BE} = V_{BE} + v_{be}$$

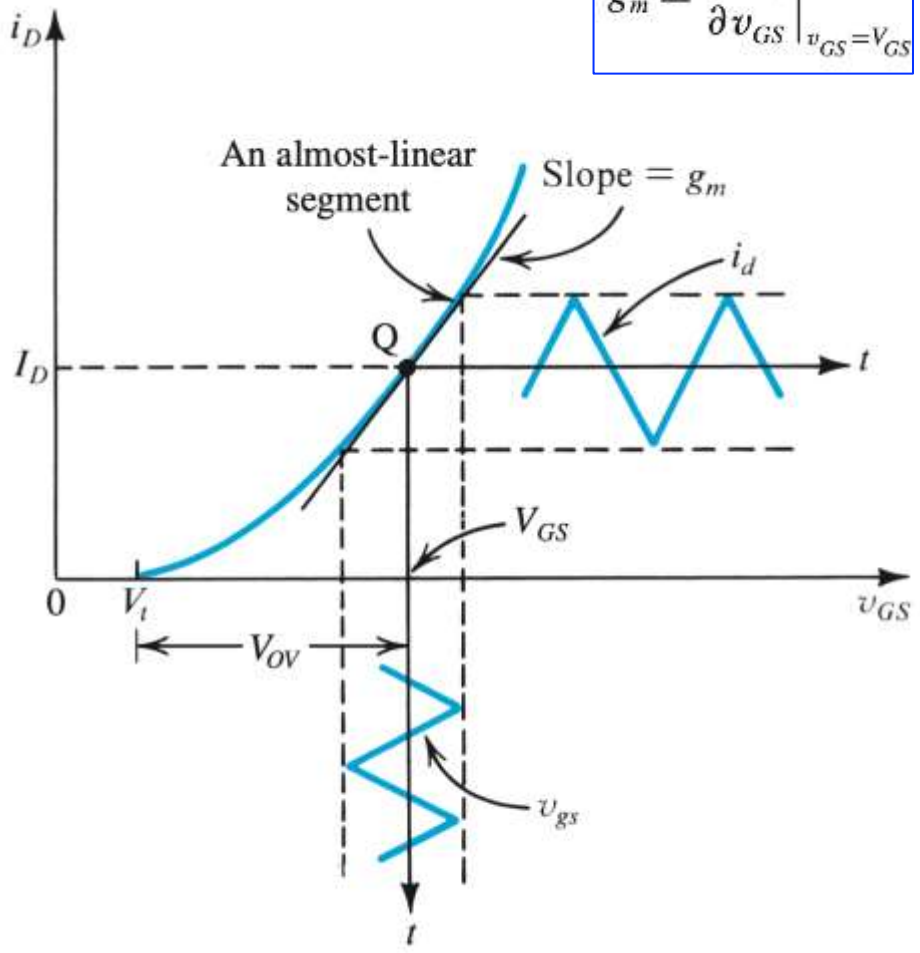
  - 当小信号量足够小时，输出信号i_D（i_C）的瞬时总量也可以视为直流量+小信号量

$$i_D \simeq I_D + i_d \qquad i_C \approx I_C + i_c$$

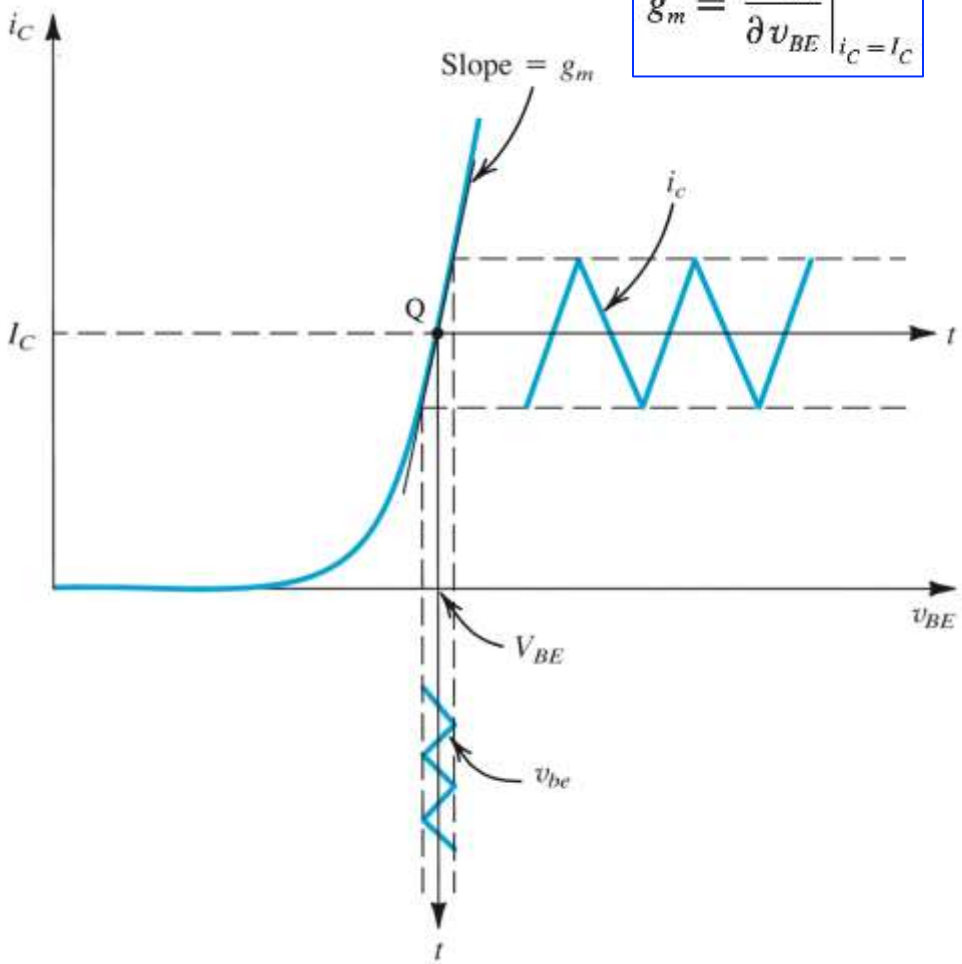
  - 输入电压小信号到输出电流小信号的增益定义为跨导g_m，其值由直流工作点决定
- 利用叠加性，电路的分析可以分三步进行
  - 只考虑直流量（电路的直流分析，不考虑“沟道调制/厄雷”效应） ☑
  - 只考虑小信号量（电路的小信号分析），需要分析晶体管的小信号模型
  - 最后把直流量和小信号量相加，得到瞬时总量

小信号工作与模型

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}}$$



$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C=I_C}$$



小信号分析时的电源、电阻

- 思考1：小信号分析时恒压源、恒流源怎么处理？
  - 恒压源 → 电压不变 →电压的小信号为0 → 短路；
  - 恒流源 → 电流不变 →电流的小信号为0→ 开路；
- 思考2：小信号分析时电阻怎么处理？
  - 电阻 → 电阻的“电流变化”和“电压变化”约束关系依旧是阻值R → 不变
- 提醒：小信号模型处理的是“微扰”，即“微小变化”的问题

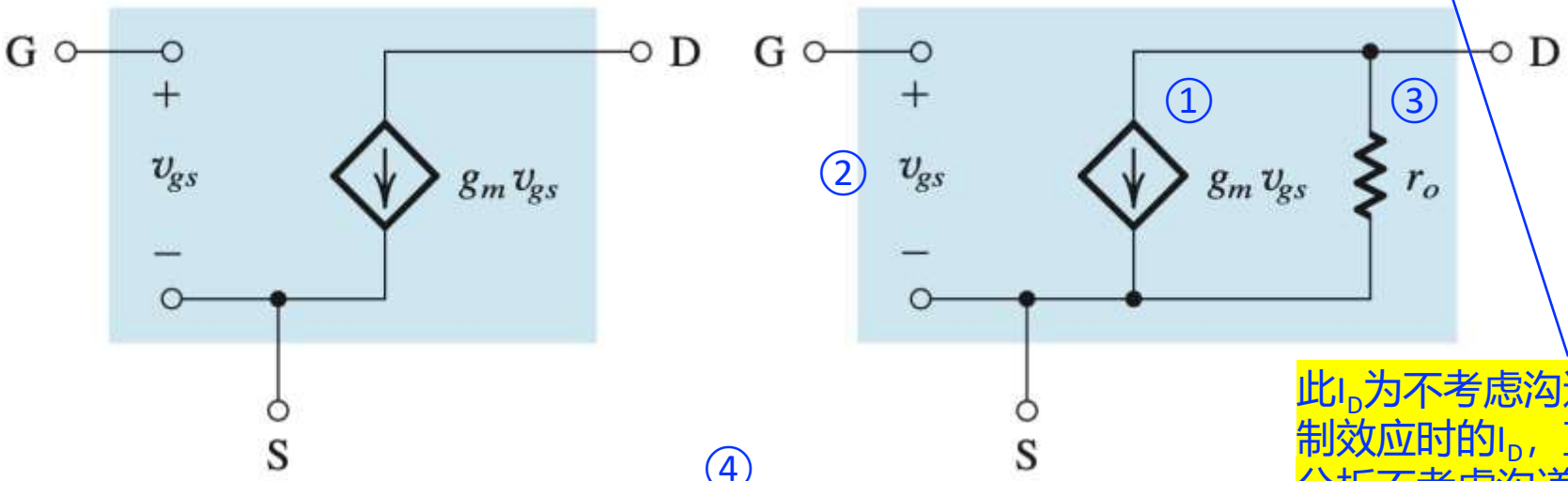
AC Ground（交流地）

- 电压源在小信号分析中等效成“短路”，因此小信号电路中的“地”有两种：一种是常规的真正的“地”，另一种是电压源短路引起的新增“地”，后者我们称之为“交流地”。（小信号分析也称为交流分析）

小信号模型

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} \qquad g_m = \frac{I_D}{V_{OV}/2}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \qquad r_o = \frac{|V_A|}{I_D} \qquad V_A = 1/\lambda$$



④

$$A_v = \frac{v_{ds}}{v_{gs}} = -g_m(R_D \| r_o)$$

此I_D为不考虑沟道调制效应时的I_D，直流分析不考虑沟道调制效应，但交流分析需要考虑

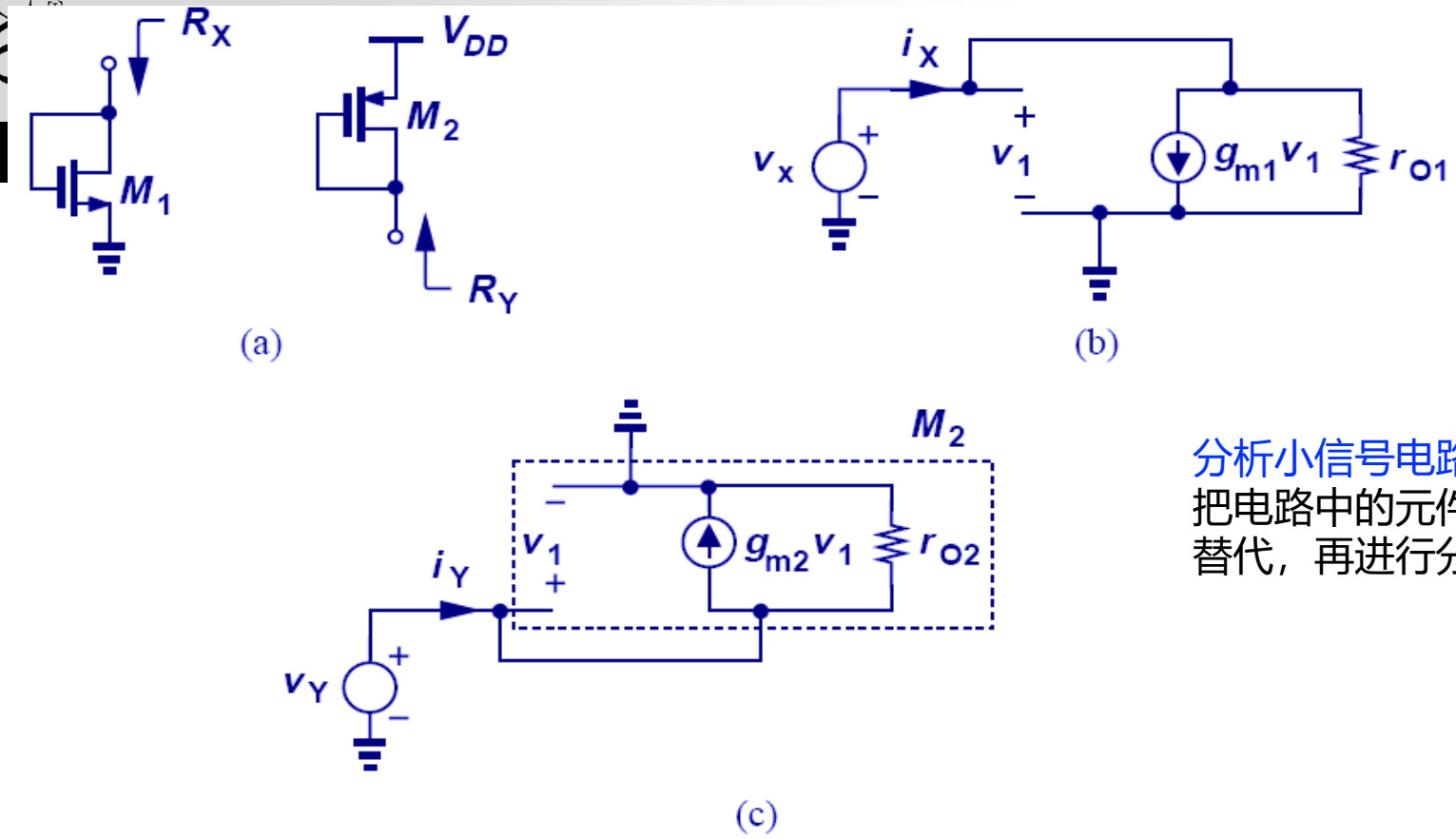
Figure 7.13 Small-signal models for the MOSFET: **(a)** neglecting the dependence of i_D on v_{DS} in the active region (the channel-length modulation effect) and **(b)** including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A|/I_D$. These models apply equally well for both NMOS and PMOS transistors.

⑤

①从输入小信号电压到输出小信号电流的跨导增益为 g_m，MOSFET有三个设计参数（W/L、I_D、V_{OV}），任选两个可以决定g_m，但BJT的g_m只决定于I_C ②输入电阻∞ ③输出电阻，考虑沟道调制效应时，为r_o（大信号模型时有r_o电阻，小信号分析电阻保持不变）r_o一般在 10kΩ~ 1MΩ的范围内 ④ r_o引起电压增益降低 ⑤PMOS和NMOS的小信号模型完全一致

小信号模型（小信号等效电路）的**参数**为两个：g_m和r_o，其值均**由直流参数决定**（I_D、V_{OV}）

PMOS 的小信号模型

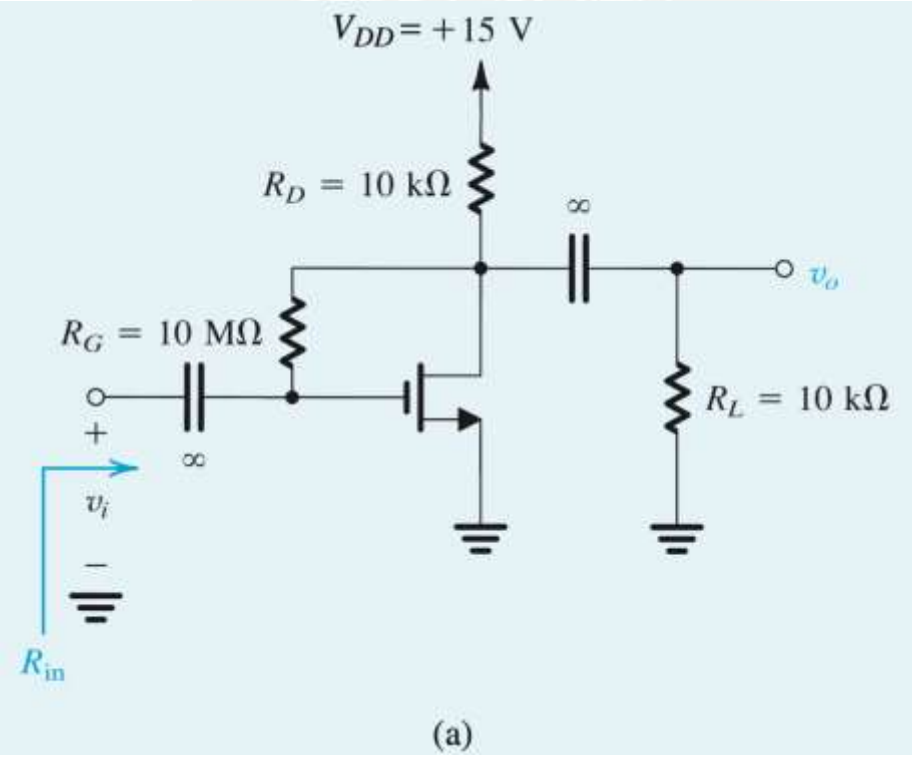


分析小信号电路的初级阶段：
把电路中的元件用小信号模型替代，再进行分析

- PMOS 的小信号模型与 NMOS 完全一致！（小信号模型表征的是“微小变化”，这里的电流方向指“变化电流”的方向，而非总电流方向！）
- $R_X = R_Y = (1/g_m)||r_o$

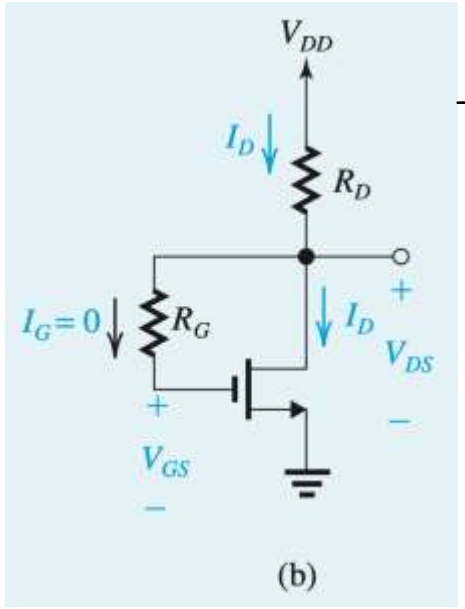
Example 7.3

Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V^2, and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.



(a)

①直流分析，电容开路



(b)

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

⇨ $I_D = 1.06$ mA

$V_{GS} = V_{DS} = 4.4$ V

$V_{OV} = 4.4 - 1.5 = 2.9$ V

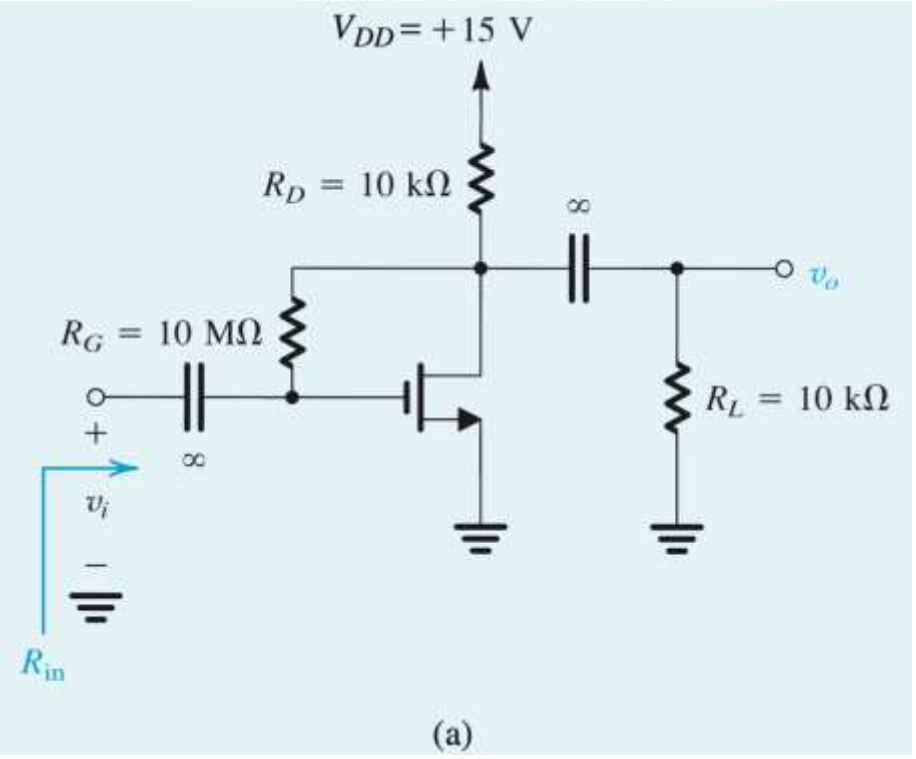
计算小信号参数

$$g_m = k_n V_{OV} = 0.25 \times 2.9 = 0.725 \text{ mA/V}$$

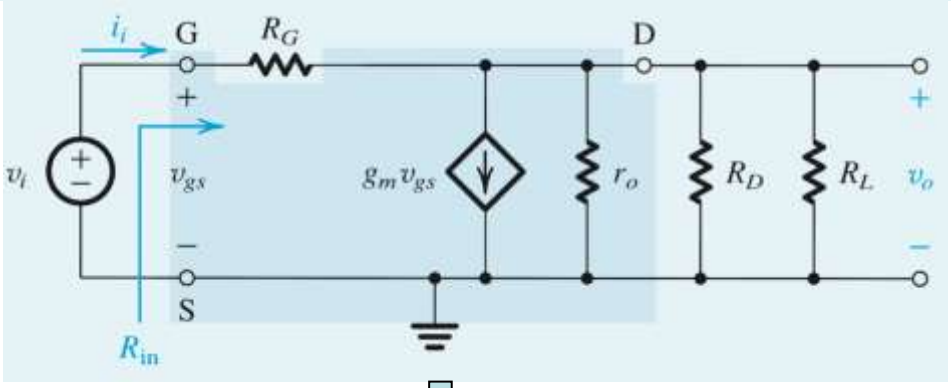
$$r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ kΩ}$$

Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V^2, and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

②小信号分析，电容短路，恒压源虚拟地



(a)



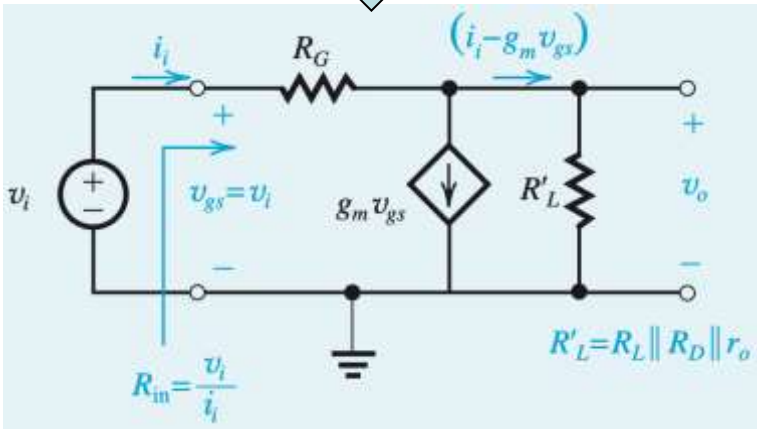
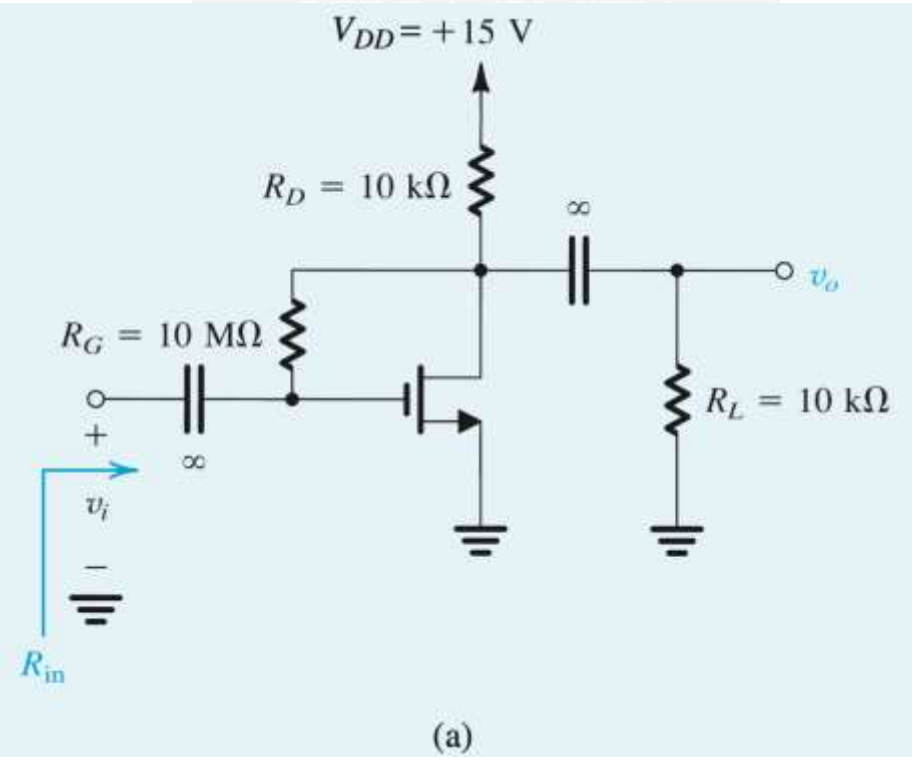
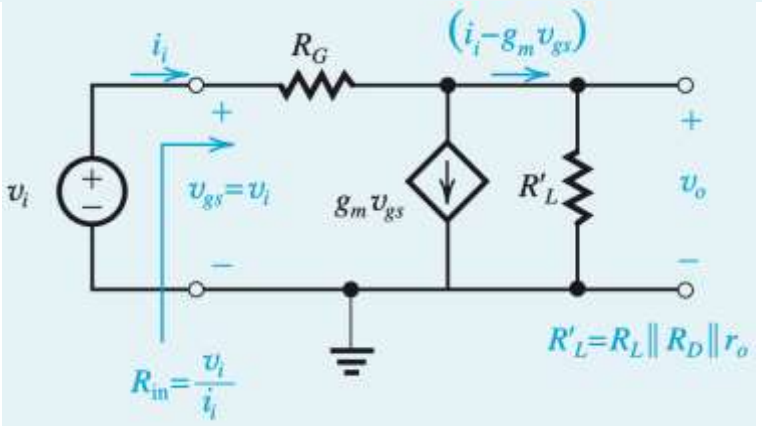


Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V^2, and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

②小信号分析，电容短路，恒压源虚拟地



(a)



$$R_L' = R_L||R_D||r_o$$
$$= 10||10||47 = 4.52\,\text{k}\Omega$$

$$v_o = (i_i - g_m v_{gs})R_L'$$

$$i_i = \frac{v_{gs} - v_o}{R_G}$$

$$A_v \equiv v_o/v_i = v_o/v_{gs}$$

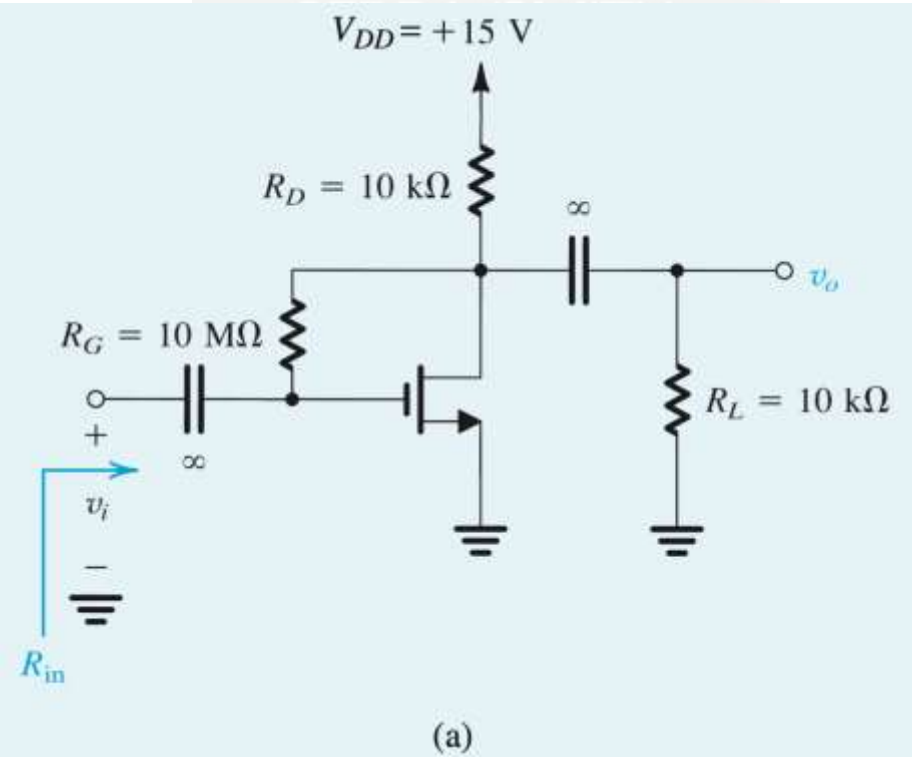
$$A_v = -g_m R_L' \frac{1 - (1/g_m R_G)}{1 + (R_L'/R_G)}$$

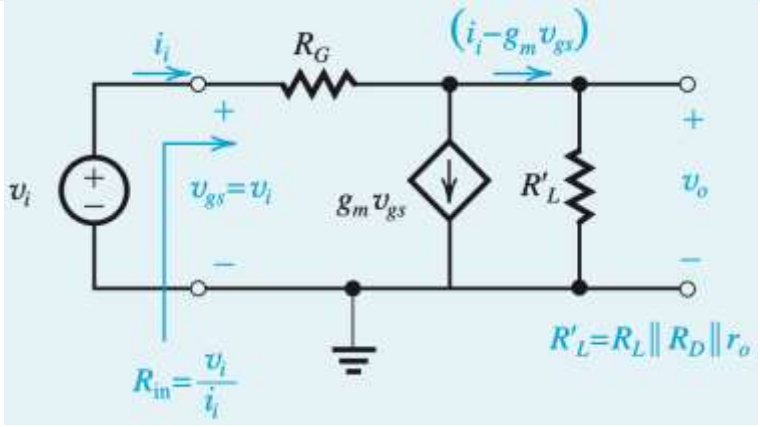
因为R_G很大

$$A_v \simeq -g_m R_L' = -3.3\ \text{V/V}$$

Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V^2, and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

②小信号分析，电容短路，恒压源虚拟地





$$R_{in} \equiv v_i/i_i = v_{gs}/i_i$$

$$i_i = \frac{v_{gs} - v_o}{R_G}$$

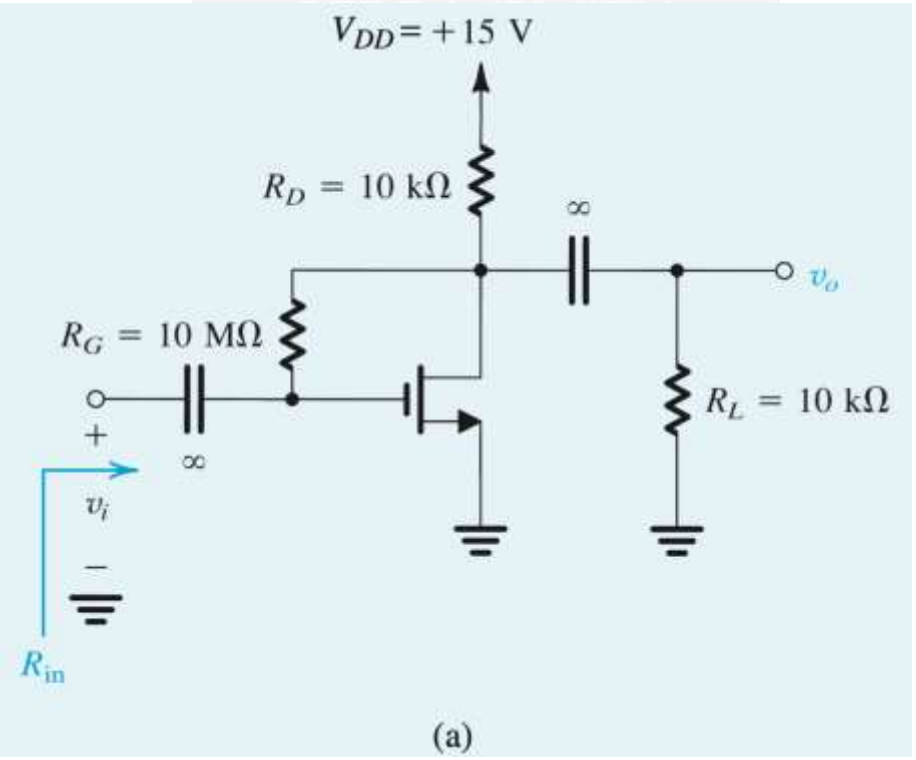
$$v_o = A_v v_{gs} = -g_m R'_L v_{gs}$$

$$R_{in} = \frac{R_G}{1 + g_m R'_L}$$

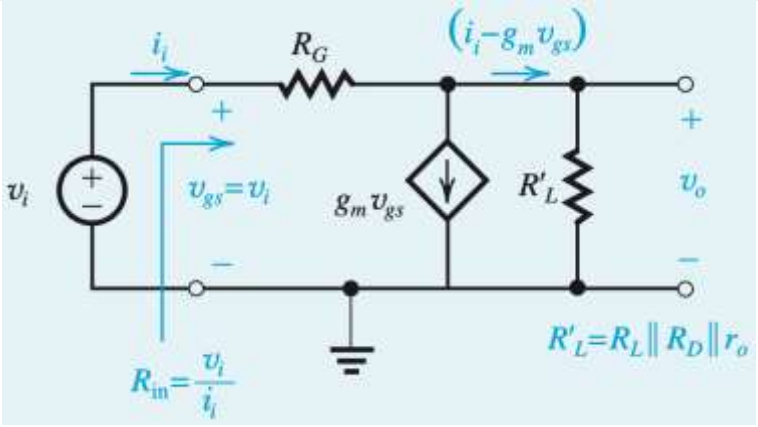
$$= \frac{10\ \text{M}\Omega}{1 + 3.3} = 2.33\ \text{M}\Omega$$

Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V^2, and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

②小信号分析，电容短路，恒压源虚拟地



(a)



最大可允许的输入信号：v_G增加→i_D增加→v_D减小，趋近于饱和区的边界

$$v_{DS\min} = v_{GS\max} - V_t$$

$$V_{DS} - |A_v|\hat{v}_i = V_{GS} + \hat{v}_i - V_t$$

$$V_{DS} = V_{GS}$$

$$\hat{v}_i = \frac{V_t}{|A_v| + 1} = 0.35 \text{ V}$$

<< $2V_{OV}$，在饱和区 ☑

$$2V_{OV} = 5.8 \text{ V}$$

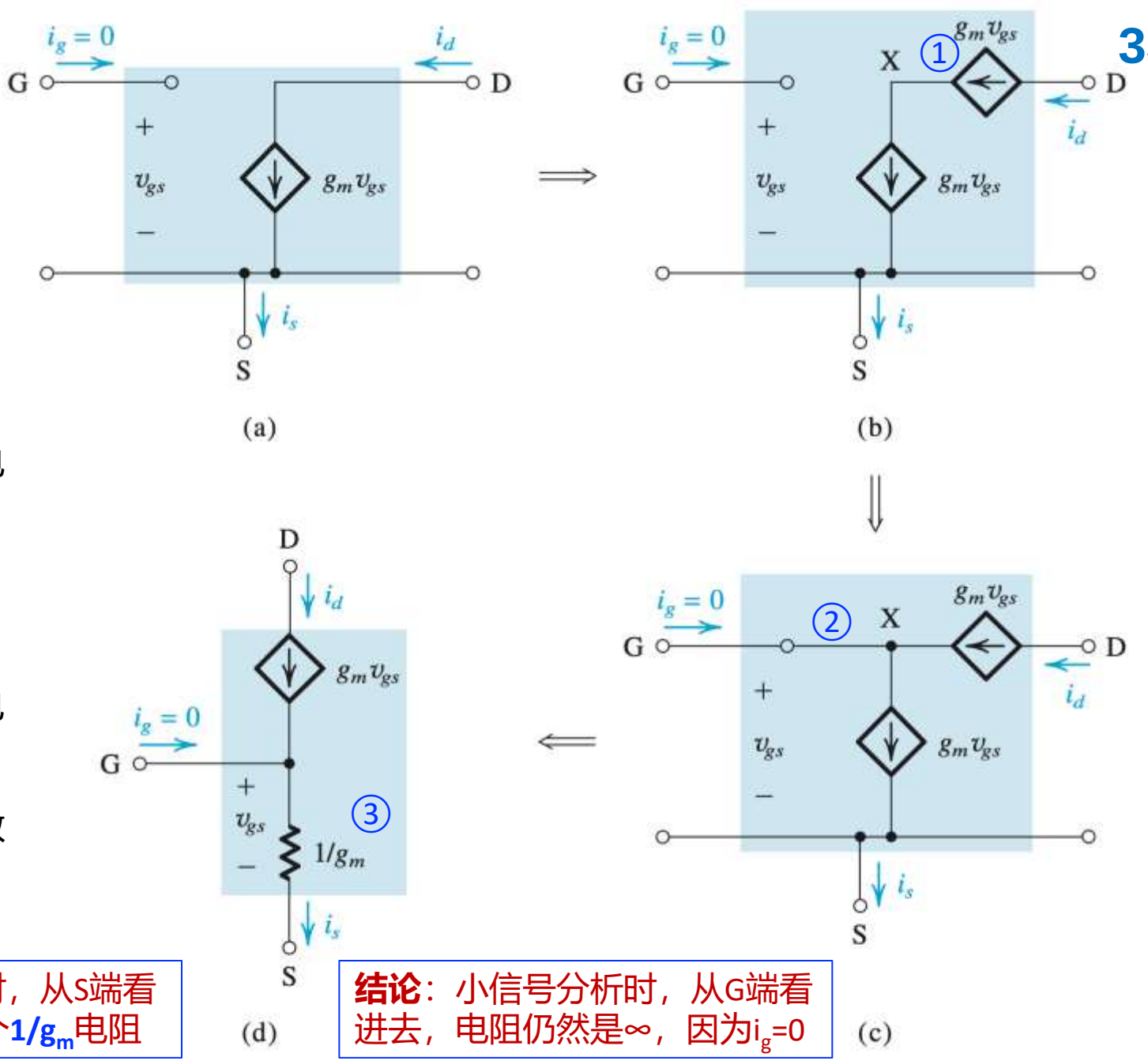
T 型等效电路模型

①串联一个相同的电流源，没什么影响

②保持i_g=0，把X与G相连

③X与S之间的受控电流源用$1/g_m$电阻替代

④若考虑沟道调制效应，在D和S间加上r_o就行



结论：小信号分析时，从S端看进去，G和S间是一个$1/g_m$电阻

结论：小信号分析时，从G端看进去，电阻仍然是∞，因为i_g=0

Figure 7.16 Development of the T equivalent-circuit model for the MOSFET. For simplicity, r_o has been omitted; however, it may be added between D and S in the T model of **(d)**.

T model

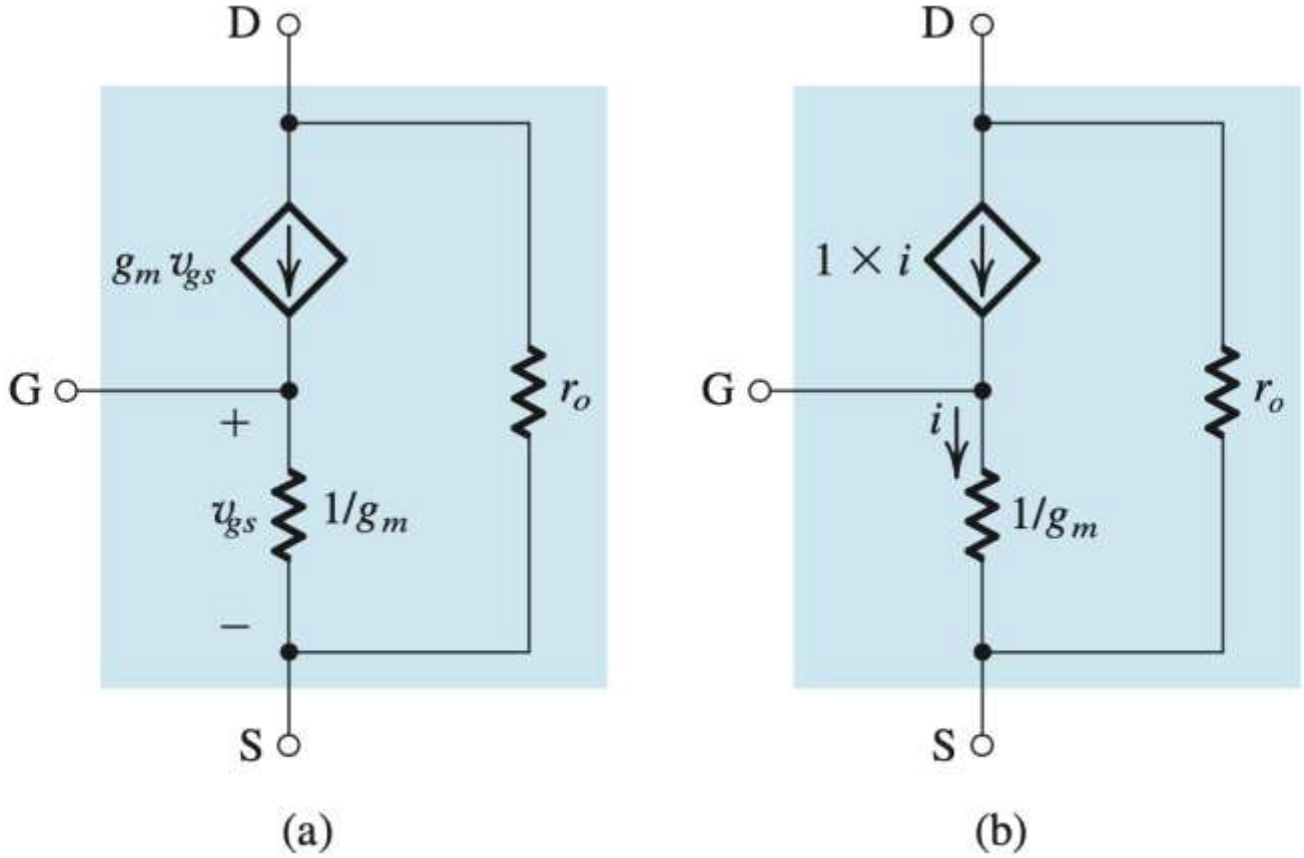


Figure 7.17 (a) The T model of the MOSFET augmented with the drain-to-source resistance r_o. (b) An alternative representation of the T model.

MOSFET的小信号模型有两种形式，两者是等价的

- S接地时，用混合π比较方便；
- S不接地时，用T模型比较方便

hybrid-π model

混合π模型

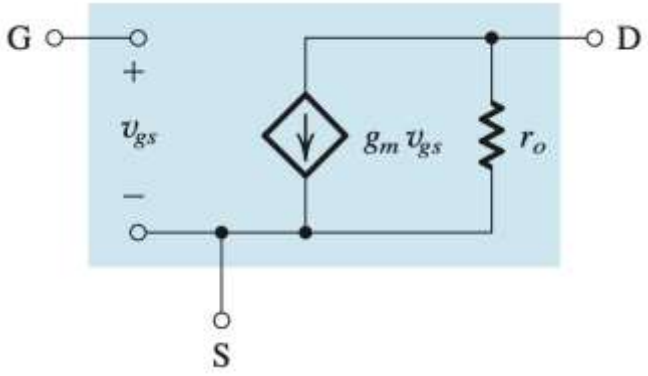
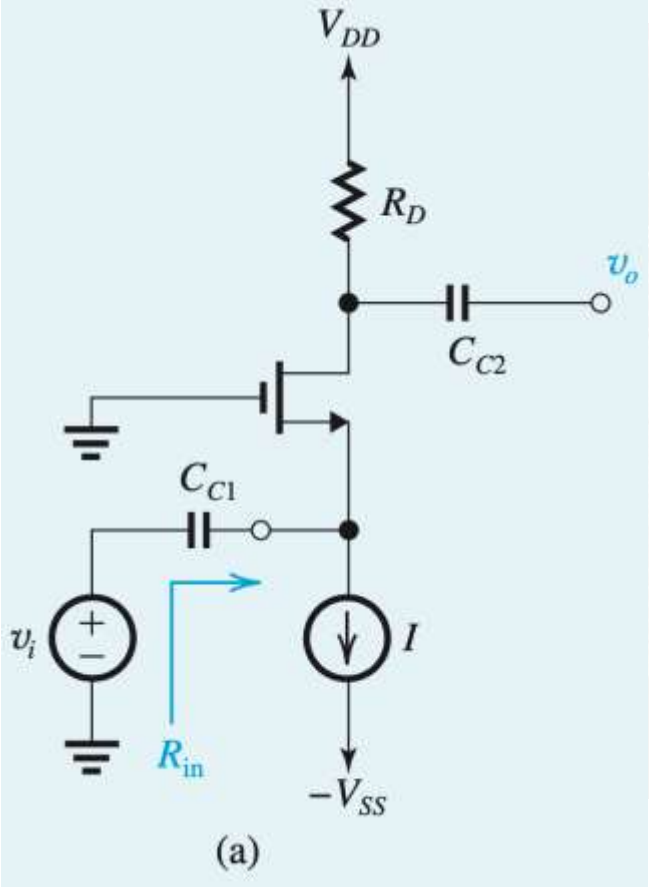
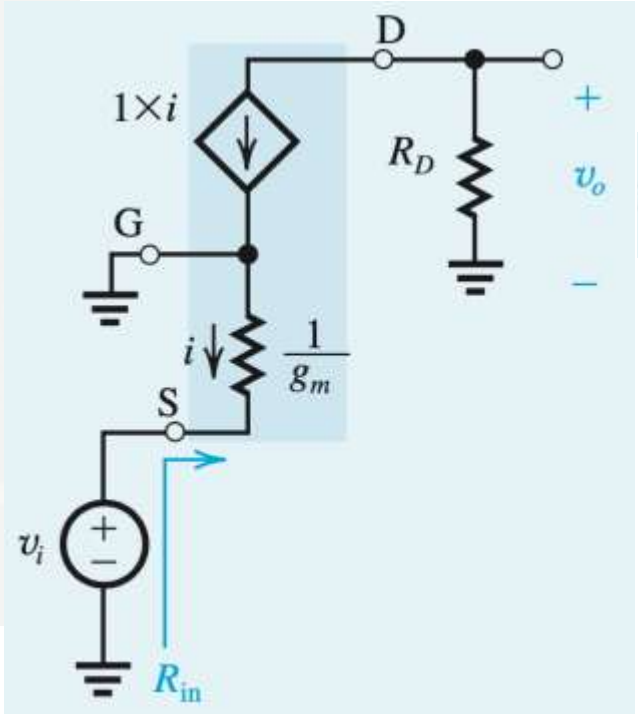


Figure 7.18(a) shows a MOSFET amplifier biased by a constant-current source I. Assume that the values of I and R_D are such that the MOSFET operates in the saturation region. The input signal v_i is coupled to the source terminal by utilizing a large capacitor C_{C1}. Similarly, the output signal at the drain is taken through a large coupling capacitor C_{C2}. Find the input resistance R_{in} and the voltage gain v_o/v_i. Neglect channel-length modulation.



①直流分析，电容开路， $I_D=I$，V_{GS}，V_{OV}可根据I_D算出

②小信号分析，电容短路，恒流源开路，恒压源虚拟地



$$R_{in}=\frac{v_i}{-i}=1/g_m$$

$$v_o=-iR_D=\left(\frac{v_i}{1/g_m}\right)R_D=g_mR_Dv_i$$

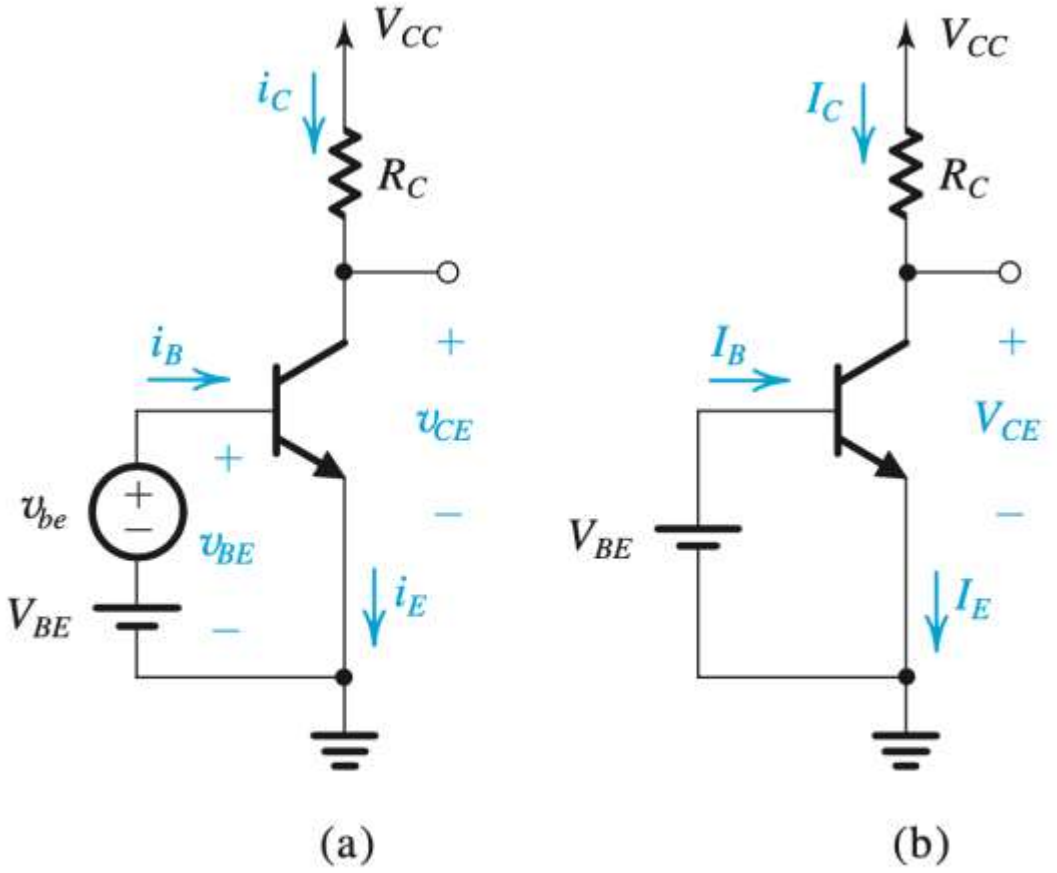
$$A_v\equiv\frac{v_o}{v_i}=g_mR_D$$

这一结构称为**共栅结构**（common-gate），因为gate接地，common to both input and output ports

- 低输入电阻
- 增益为正（相位相同）

BJT

The DC Bias Point



$$I_C = I_S e^{V_{BE}/V_T}$$

$$I_E = I_C/\alpha$$

$$I_B = I_C/\beta$$

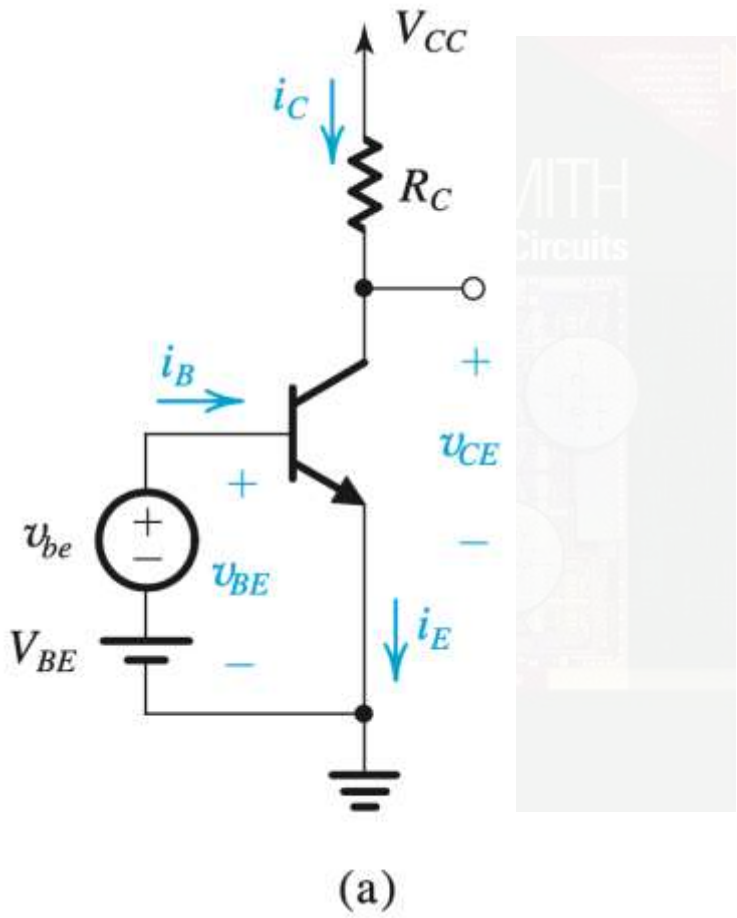
$$V_{CE} = V_{CC} - I_C R_C$$

跨导

$$g_m = \frac{I_C}{V_T}$$

Figure 7.20 (**a**) Conceptual circuit to illustrate the operation of the transistor as an amplifier. (**b**) The circuit of (**a**) with the signal source v_{be} eliminated for dc (bias) analysis.

小信号
基极电流&基极电阻



(a)

$$i_c = g_m v_{be}$$

基极电流瞬时总量

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T} v_{be}$$

$$i_B = I_B + i_b$$

$$i_b = \frac{g_m}{\beta} v_{be}$$

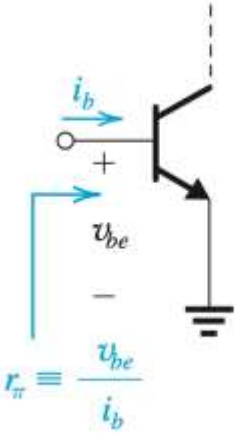
⟹ BE之间，从B看进去，是一个电阻，阻值为 $\frac{\beta}{g_m}$

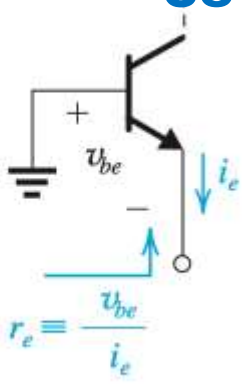
$$r_\pi \equiv \frac{v_{be}}{i_b} = \frac{\beta}{g_m}$$

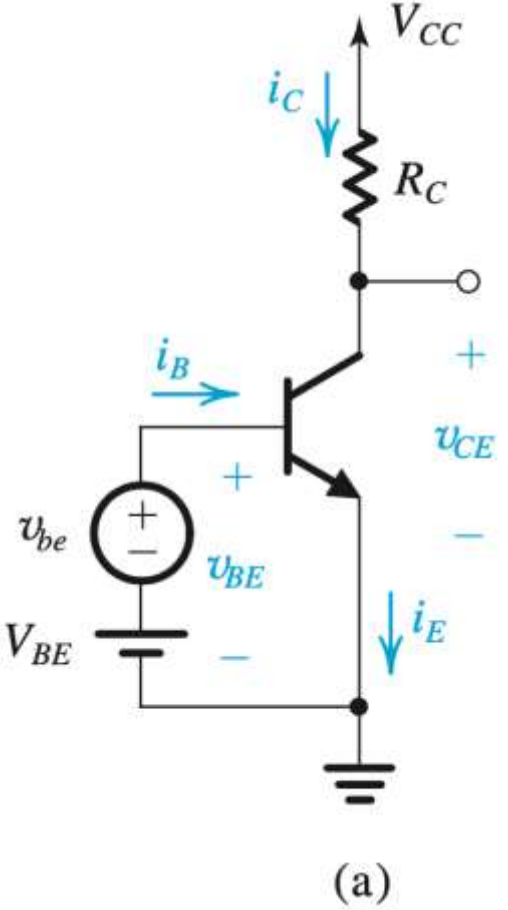
Q: MOSFET有 r_π 吗?

小信号
发射极电流&发射极电阻

$$i_c = g_m v_{be}$$







(a)

发射极电流瞬时总量

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

$$i_E = I_E + i_e$$

$$i_e = \frac{i_c}{\alpha} = \frac{g_m v_{be}}{\alpha}$$

$r_\pi = (\beta+1) r_e$

⟹ BE之间，从E看进去，也是一个电阻，阻值为 $\frac{\alpha}{g_m}$

$$r_e \equiv \frac{v_{be}}{i_e} = \frac{\alpha}{g_m} \simeq \frac{1}{g_m}$$

r_π 和 r_e 之间的关系：都是BE之间，但从不同端看进去

$$v_{be} = i_b r_\pi = i_e r_e \qquad r_\pi = (i_e/i_b) r_e = (\beta+1) r_e$$

因为基极电流小，是发射极电流的1/(β+1)，所以从基极看进去的电阻大，是发射极看进去电阻的(β+1)倍

小信号模型
混合π

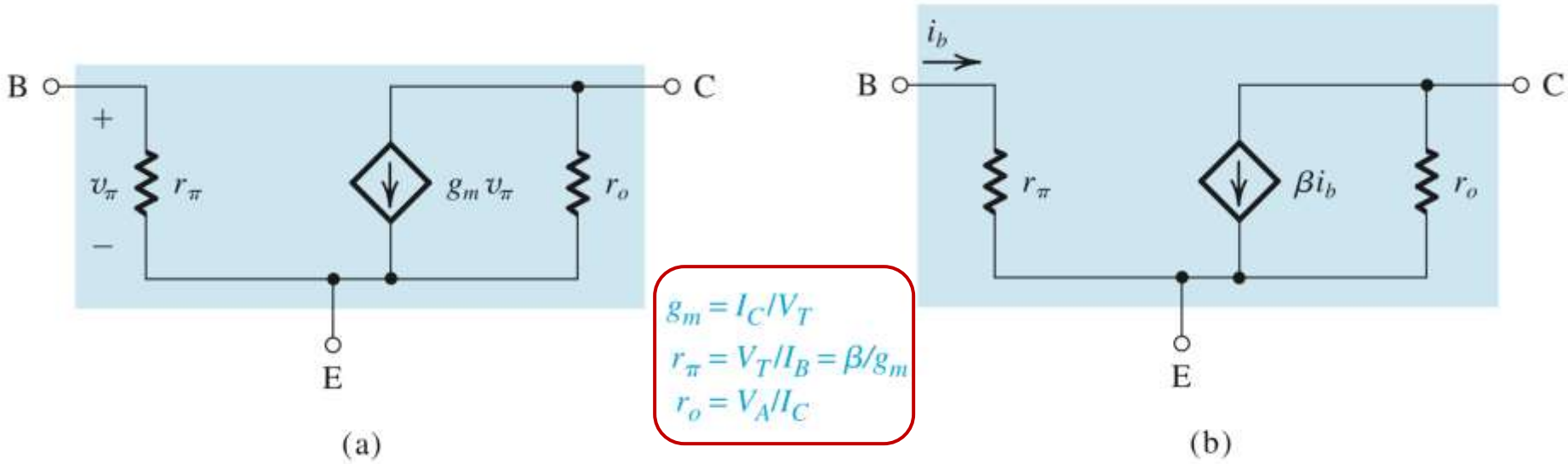
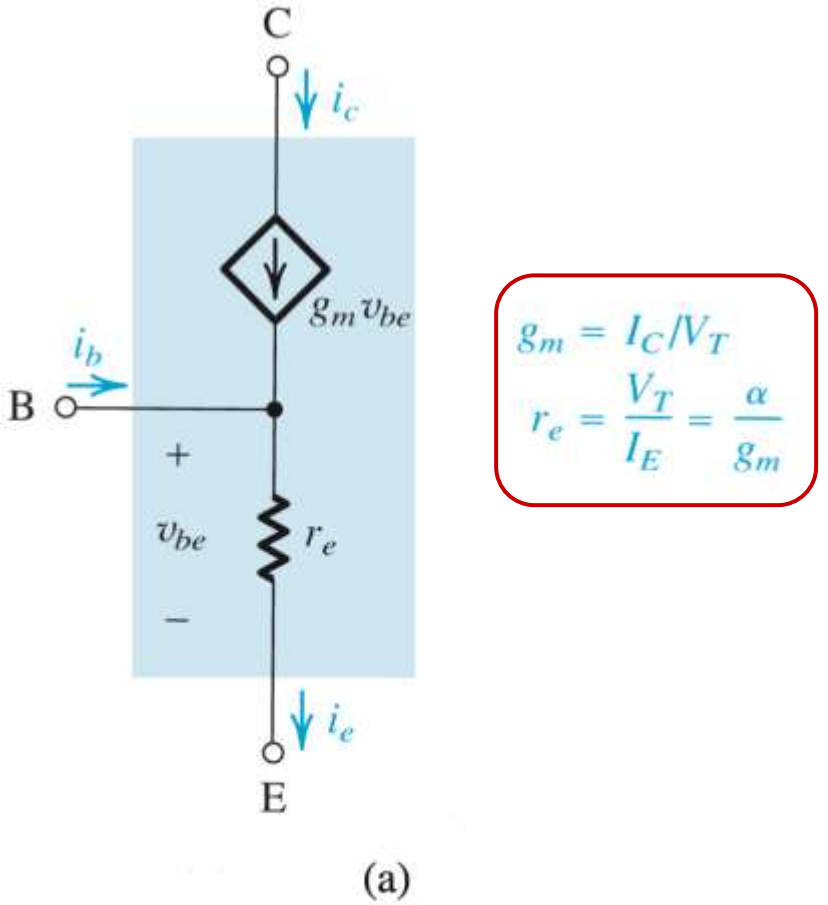


Figure 7.25 The hybrid-π small-signal model, in its two versions, with the resistance r_o included.

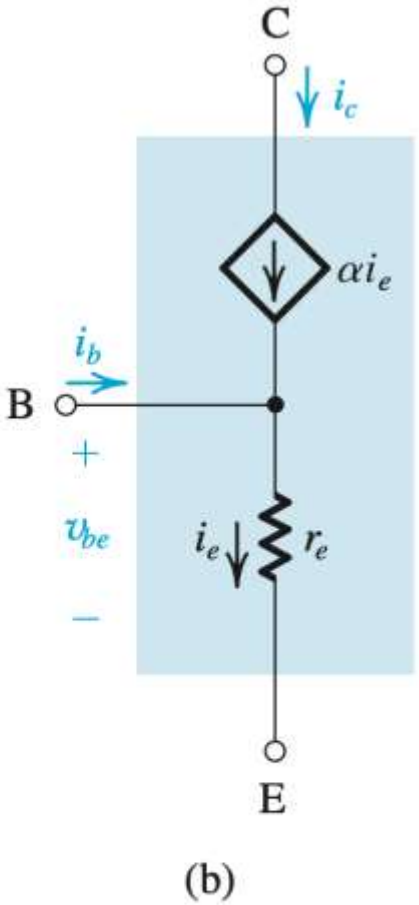
小信号模型参数（g_m、r_π、 r_o）也是由直流参数 I_C 决定的

同样，考虑 r_o 也会使得增益降低 $\dfrac{v_o}{v_{be}} = -g_m(R_C \| r_o)$

小信号模型
T 模型



$$g_m = I_C/V_T$$
$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$



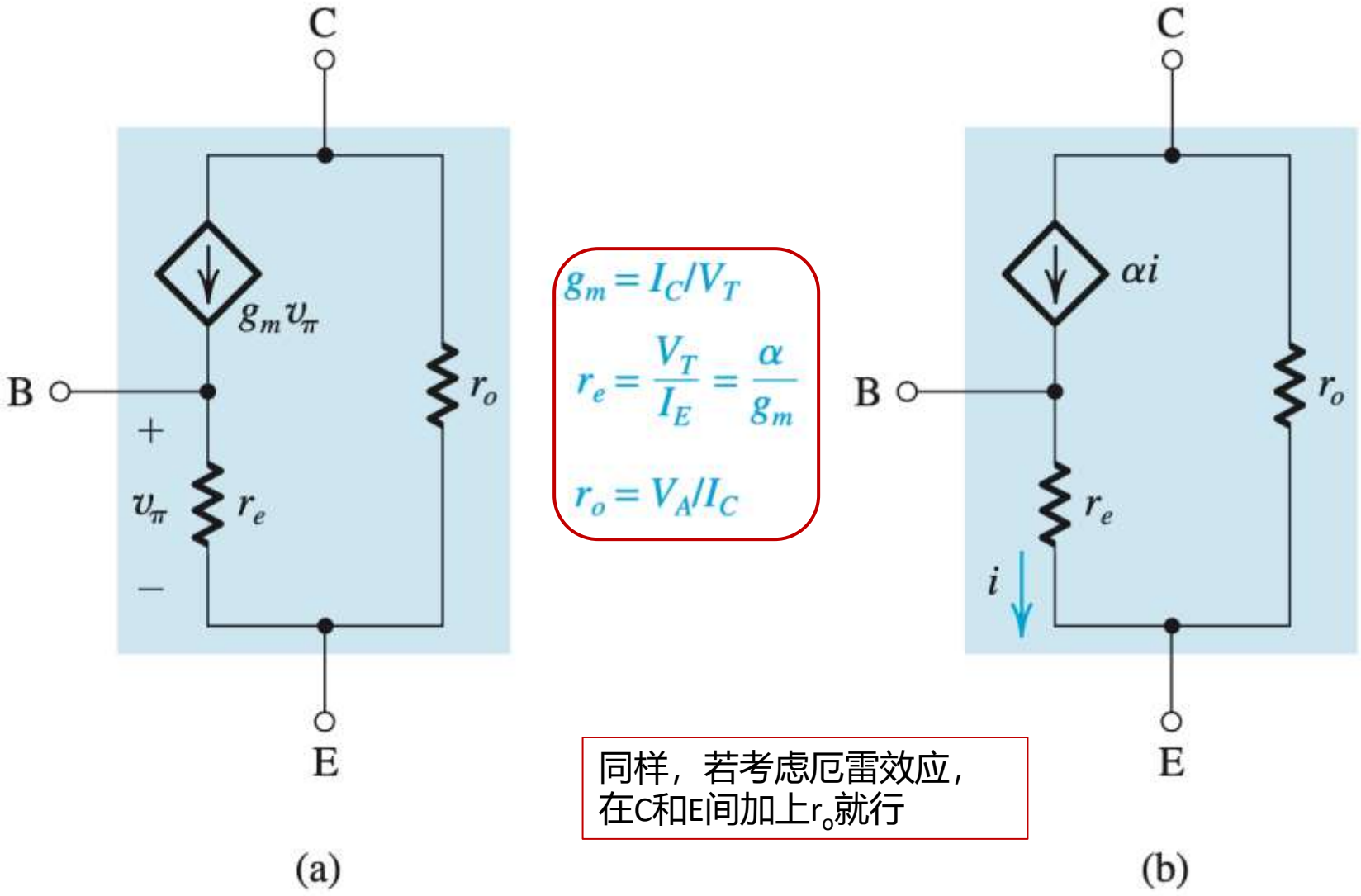
跟MOSFET一致

T 模型用 r_e（$\approx 1/g_m$），
混合π模型用 r_π

同样，两者是等价的
- **E 接地**时，用**混合 π** 比较方便；
- **E 不接地**时，用 **T 模型** 比较方便

同样，若考虑厄雷效应，在C和E间加上r_o就行

Figure 7.26 Two slightly different versions of what is known as the *T model* of the BJT. The circuit in (**a**) is a voltage-controlled current source representation and that in (**b**) is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid-π model.

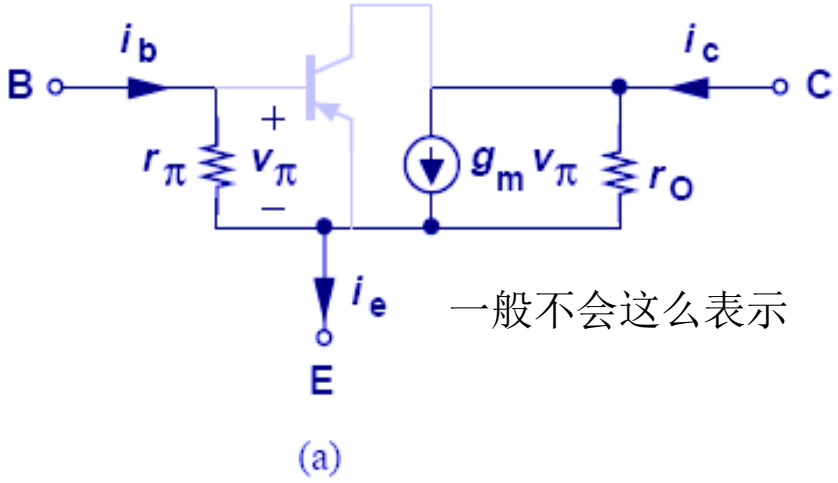


同样，若考虑厄雷效应，
在C和E间加上r_o就行

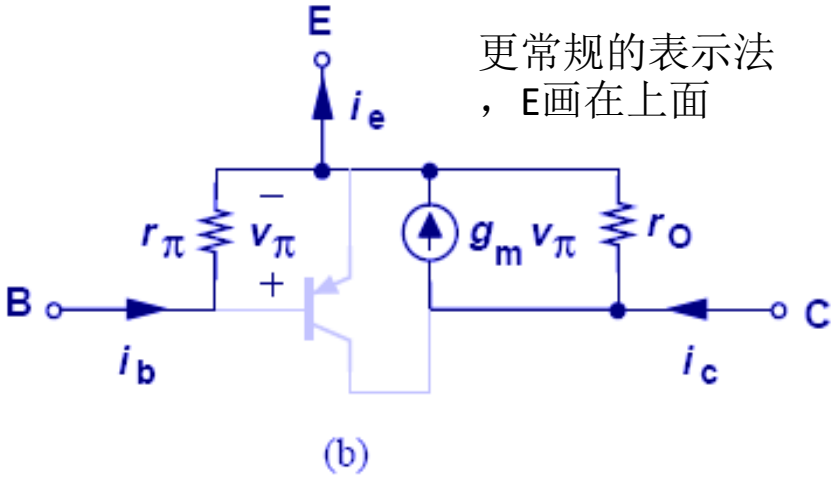
Figure 7.27 The T models of the BJT.

Oxford University Publishing
Microelectronic Circuits by Adel S. Sedra and Kenneth C. Smith (0195323033)

PNP 三极管的小信号模型



(a)

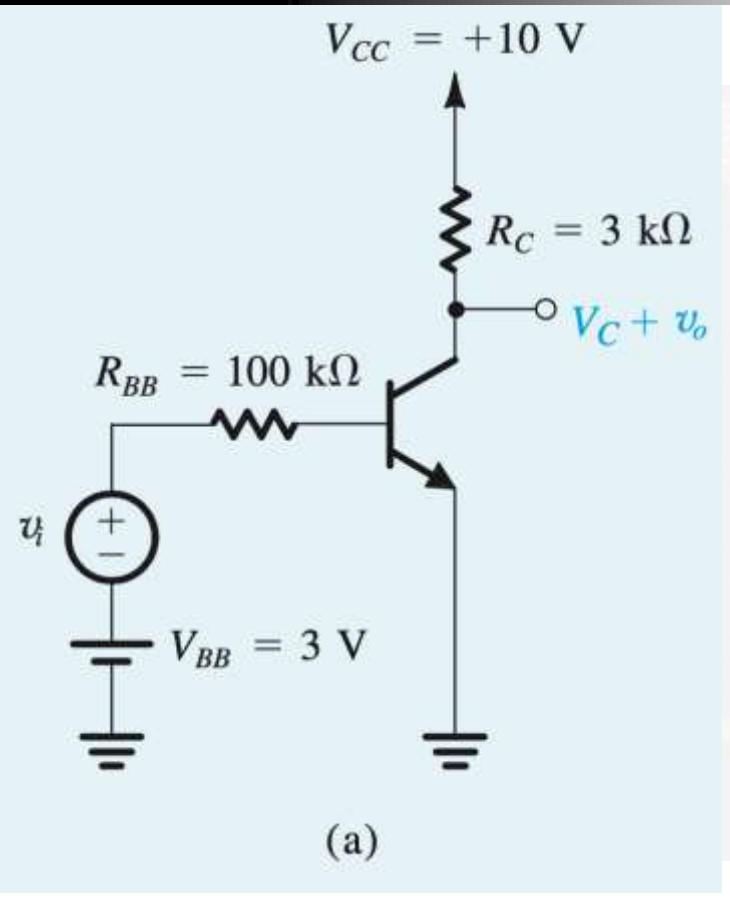


(b)

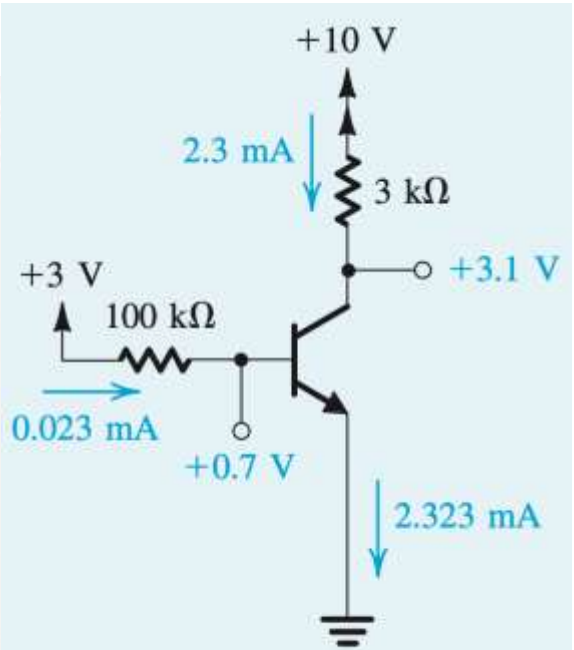
- PNP 三极管的小信号模型与 NPN 三极管的小信号模型完全一致！
- 因为小信号模型表征的是“微小变化”，这里的电流方向指“变化电流”的方向，而非总电流方向！

We wish to analyze the transistor amplifier shown in Fig. 7.28(a) to determine its voltage gain v_o/v_i. Assume $\beta = 100$ and neglect the Early effect.

①直流分析



(a)



(b)

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}} \simeq \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = +10 - 2.3 \times 3 = +3.1 \text{ V}$$

放大区 ☑

②小信号参数计算

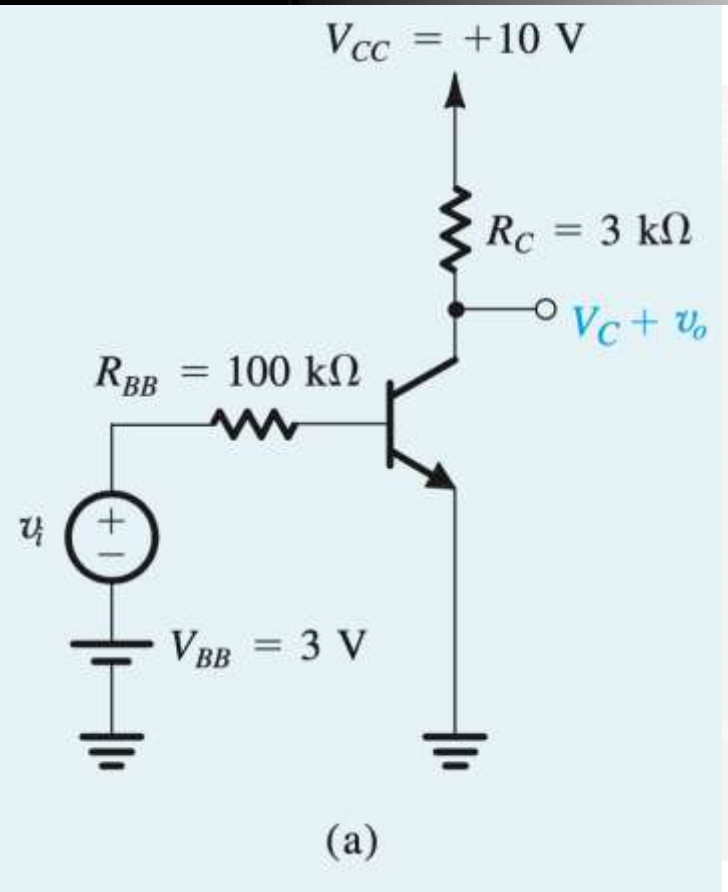
$$g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

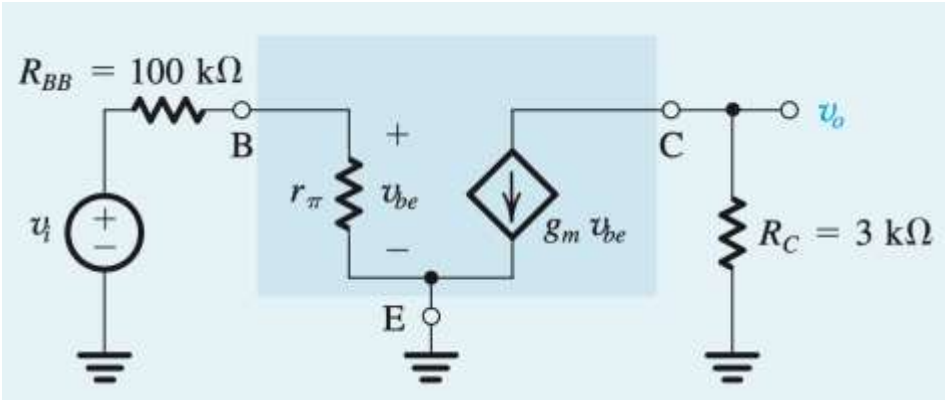
$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

$$r_e = \frac{1}{g_m} = 10.87 \ \Omega$$

We wish to analyze the transistor amplifier shown in Fig. 7.28(a) to determine its voltage gain v_o/v_i. Assume $\beta = 100$ and neglect the Early effect.

③小信号分析，恒压源虚拟地，用混合π模型





$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}}$$

$$= v_i \frac{1.09}{101.09} = 0.011 v_i$$

$$v_o = -g_m v_{be} R_C$$

$$= -92 \times 0.011 v_i \times 3 = -3.04 v_i$$

$$A_v = \frac{v_o}{v_i} = -3.04 \text{ V/V}$$

Example 7.6

To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in the previous example. For this purpose assume that v_i has a triangular waveform. First determine the maximum amplitude that v_i is allowed to have. Then, with the amplitude of v_i set to this value, give the waveforms of the total quantities $i_B(t)$, $v_{BE}(t)$, $i_C(t)$, and $v_C(t)$.

小信号的前提： $v_{be} \ll V_T$ 我们放宽到上限 10 mV，即v_{be}允许最大的峰峰值为20 mV

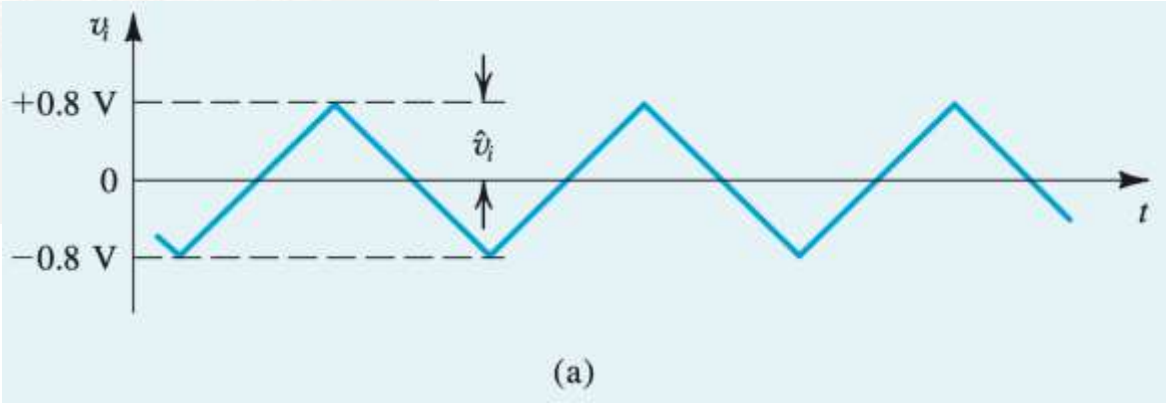
$$\hat{v}_i = \frac{\hat{v}_{be}}{0.011} = \frac{10}{0.011} = 0.91 \text{ V}$$

验证晶体管是否还工作在放大区

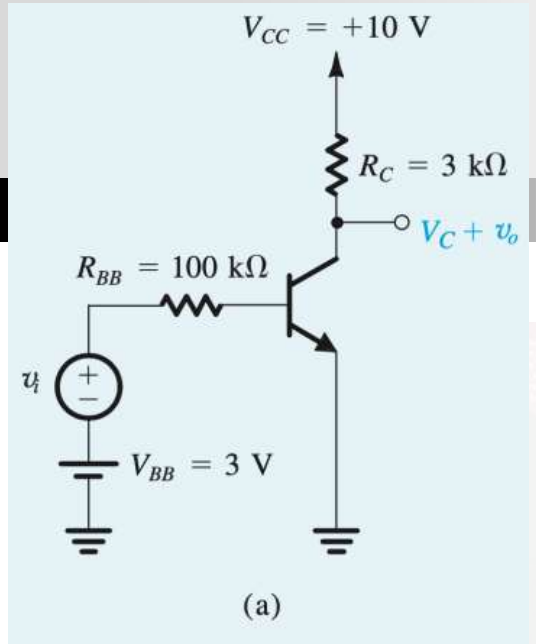
$$V_C = 3.1 \text{ V} \qquad \hat{v}_o = \hat{v}_i \times \text{gain} = 0.91 \times 3.04 = 2.77 \text{ V}$$

3.1 – 2.77 > 0.7 – 0.4 ☑

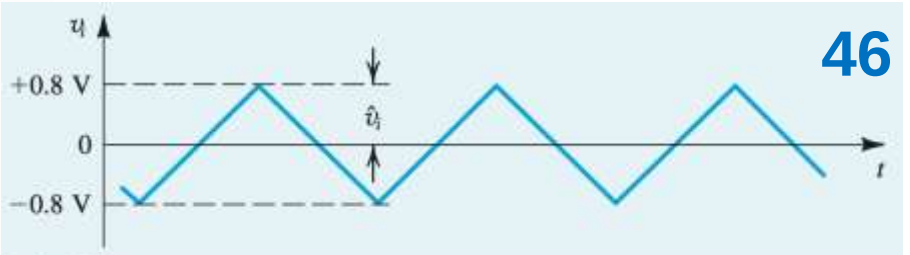
为安全起见，以下我们采用略小一点的 v_i 来进行分析，令 $v_i = 0.8$ V



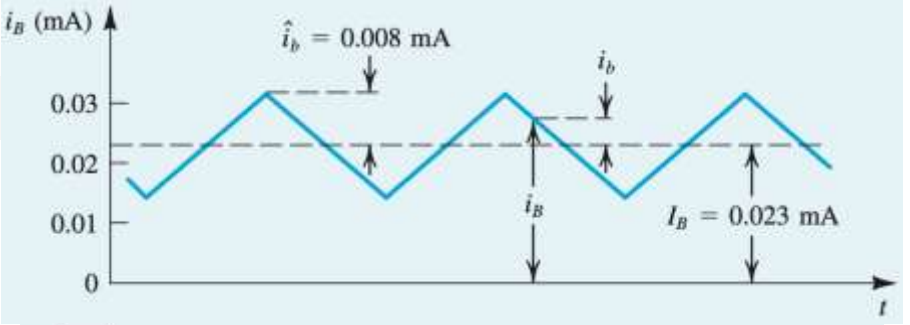
(a)


$V_{CC} = +10$ V
$R_C = 3$ kΩ
$v_C + v_o$
$R_{BB} = 100$ kΩ
v_i
$V_{BB} = 3$ V
(a)

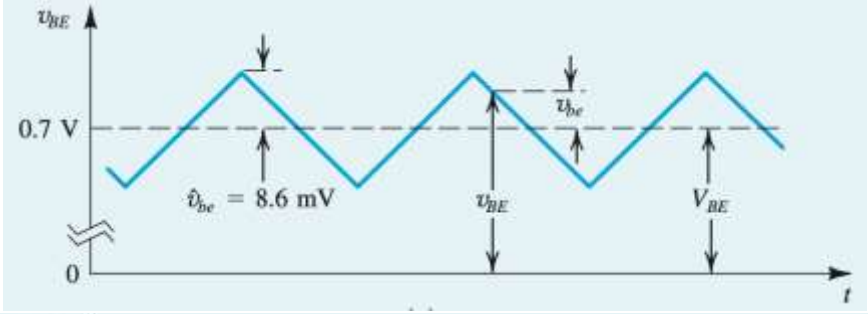
①


v_i
+0.8 V
0
−0.8 V
$\hat{v}_i$
t

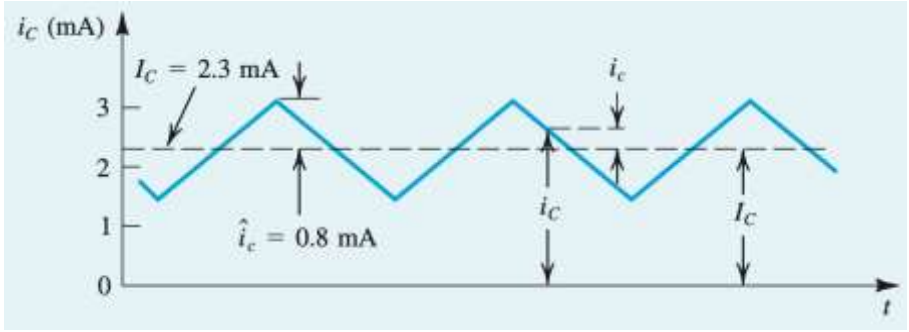
②


i_B (mA)
$\hat{i}_b = 0.008$ mA
i_b
0.03
0.02
0.01
0
i_B
$I_B = 0.023$ mA
t

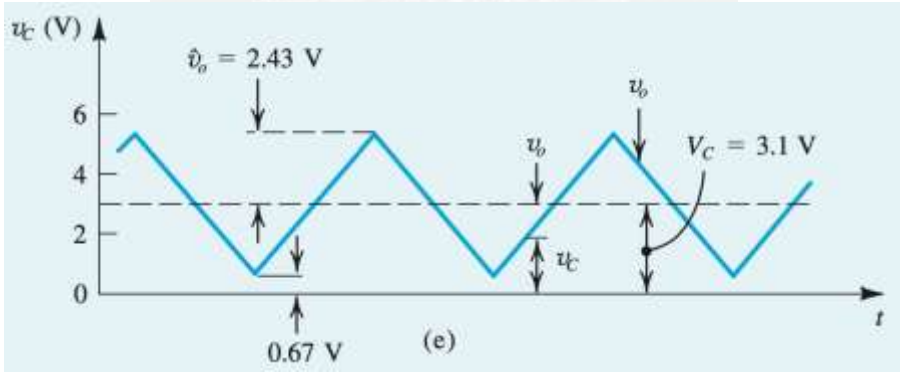
③


v_{BE}
0.7 V
0
$\hat{v}_{be} = 8.6$ mV
v_{BE}
v_{be}
V_{BE}
t

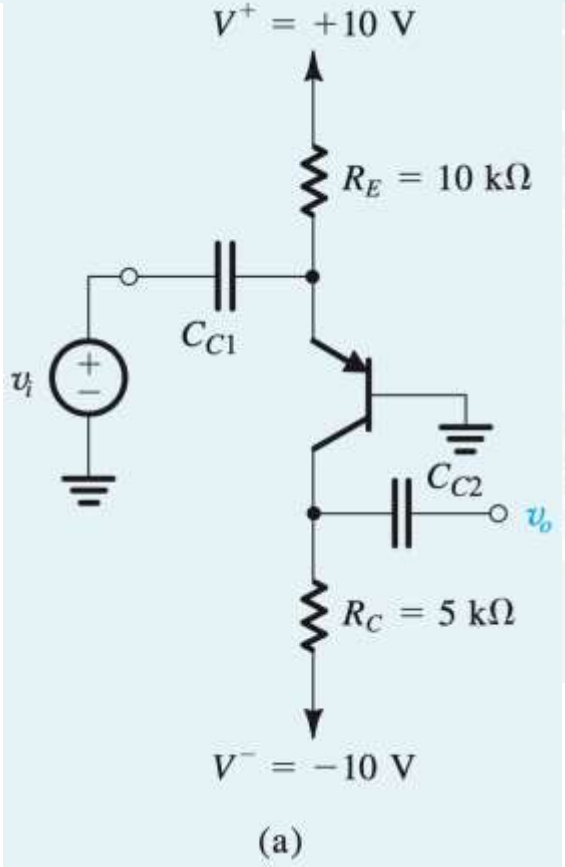
④


i_C (mA)
$I_C = 2.3$ mA
i_c
3
2
1
0
$\hat{i}_c = 0.8$ mA
i_C
I_C
t

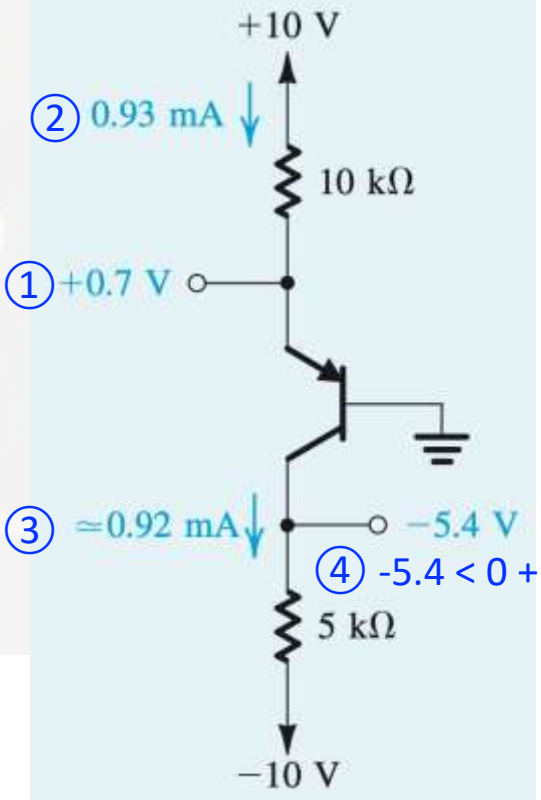
⑤


v_C (V)
$\hat{v}_o = 2.43$ V
v_b
v_o
$V_C = 3.1$ V
6
4
2
0
v_c
0.67 V
(e)
t

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system. You may neglect the Earlv effect.



直流分析



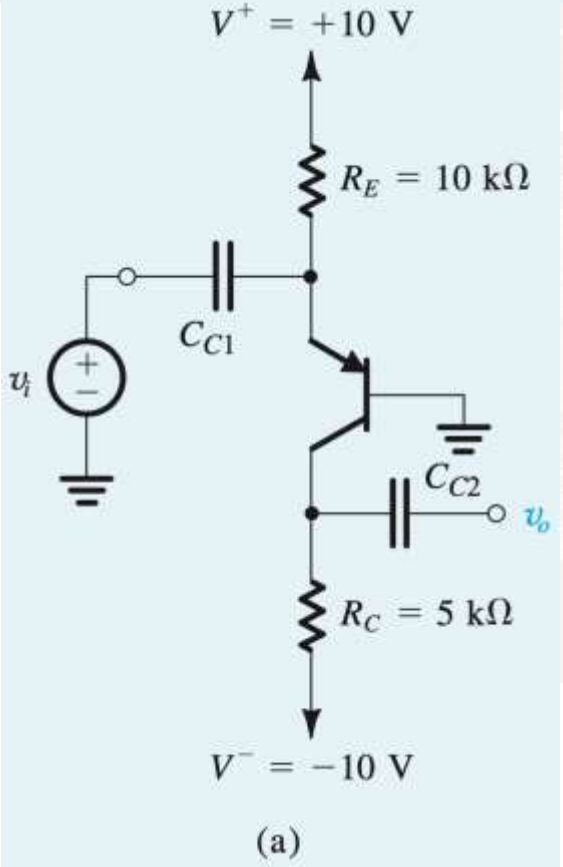
小信号参数计算

$$g_m = \frac{I_C}{V_T} = \frac{0.92}{0.025} = 36.8 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{36.8} = 2.72 \text{ k}\Omega$$

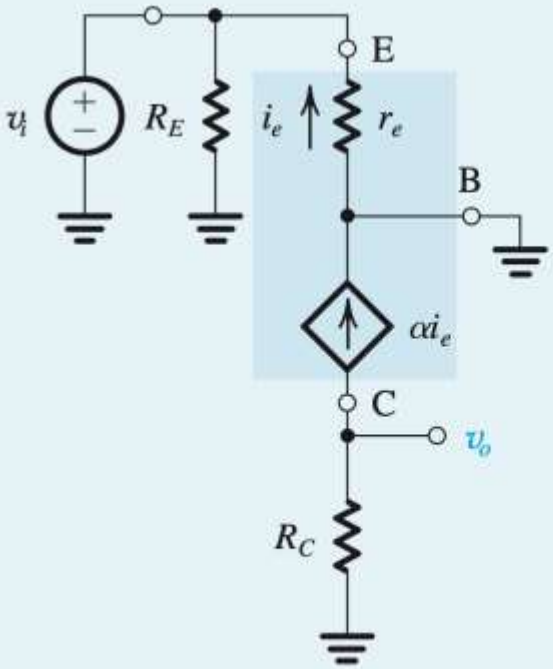
$$r_e = \frac{1}{g_m} = 27.2\ \Omega$$

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system. You may neglect the Earlv effect.



(a)

小信号分析



(d)

$$i_e = -\frac{v_i}{r_e}$$

$$v_o = -\alpha i_e R_C = \frac{\alpha R_C}{r_e} v_i$$

增益为正→同相

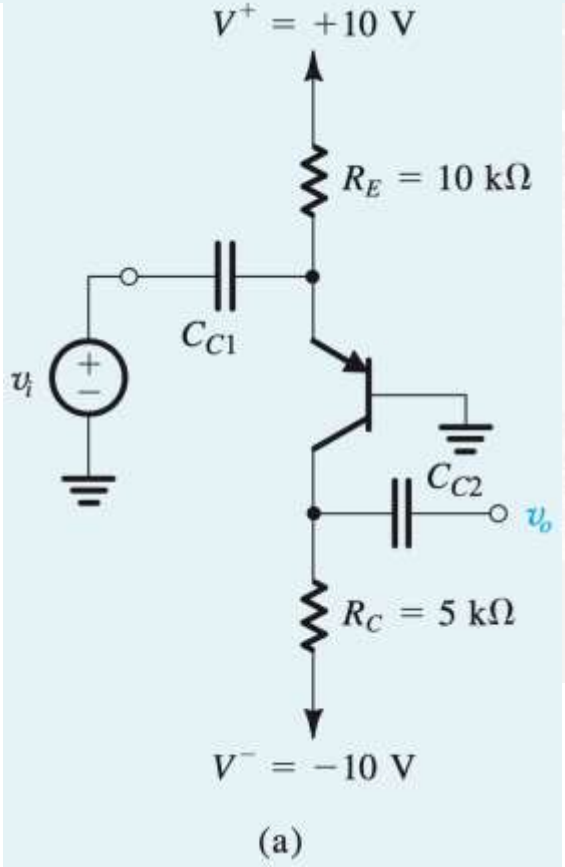
$$A_v = \frac{v_o}{v_i} = \frac{\alpha R_C}{r_e}$$

$$= \frac{0.99 \times 5}{0.0272} = 182 \text{ V/V}$$

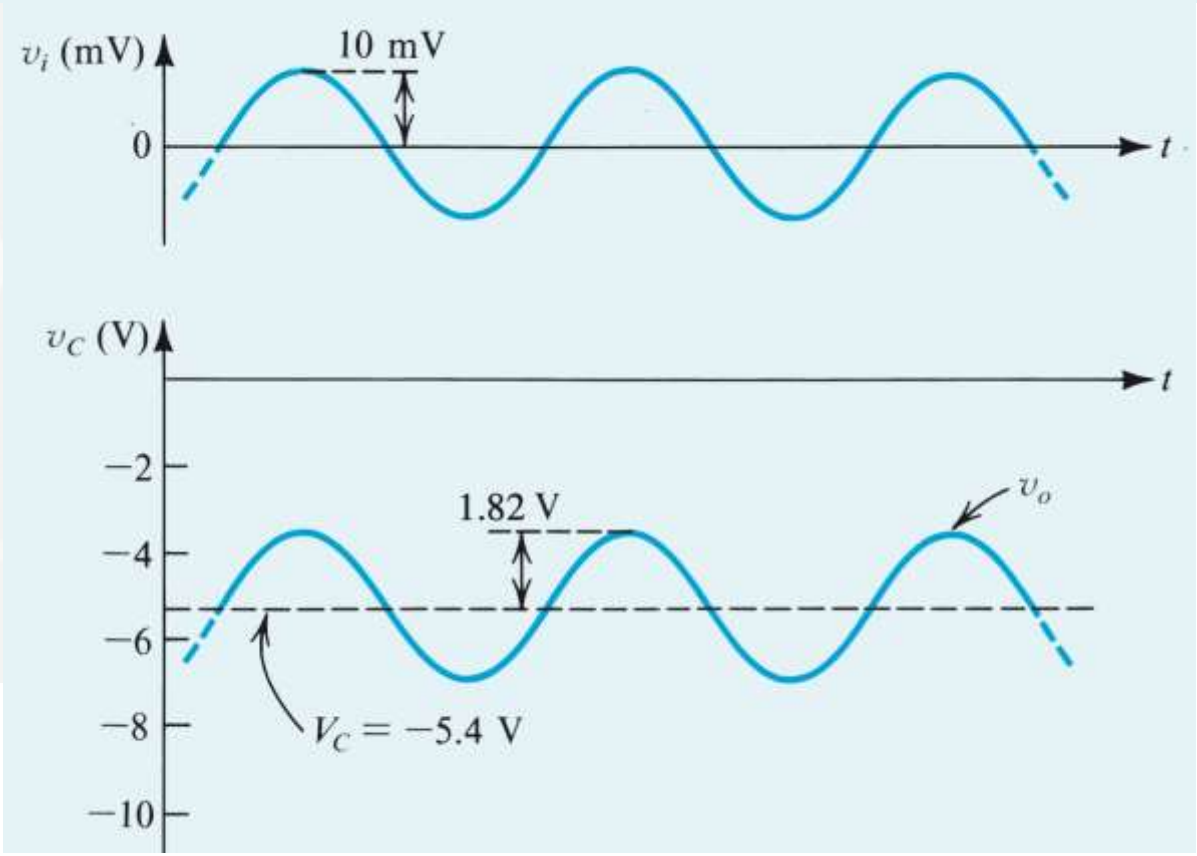
$v_{be} = -v_i$，所以v_i不能超过10 mV

$$\hat{V}_o = 182 \times 0.01 = 1.82 \text{ V}$$

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system. You may neglect the Earlv effect.



(a)

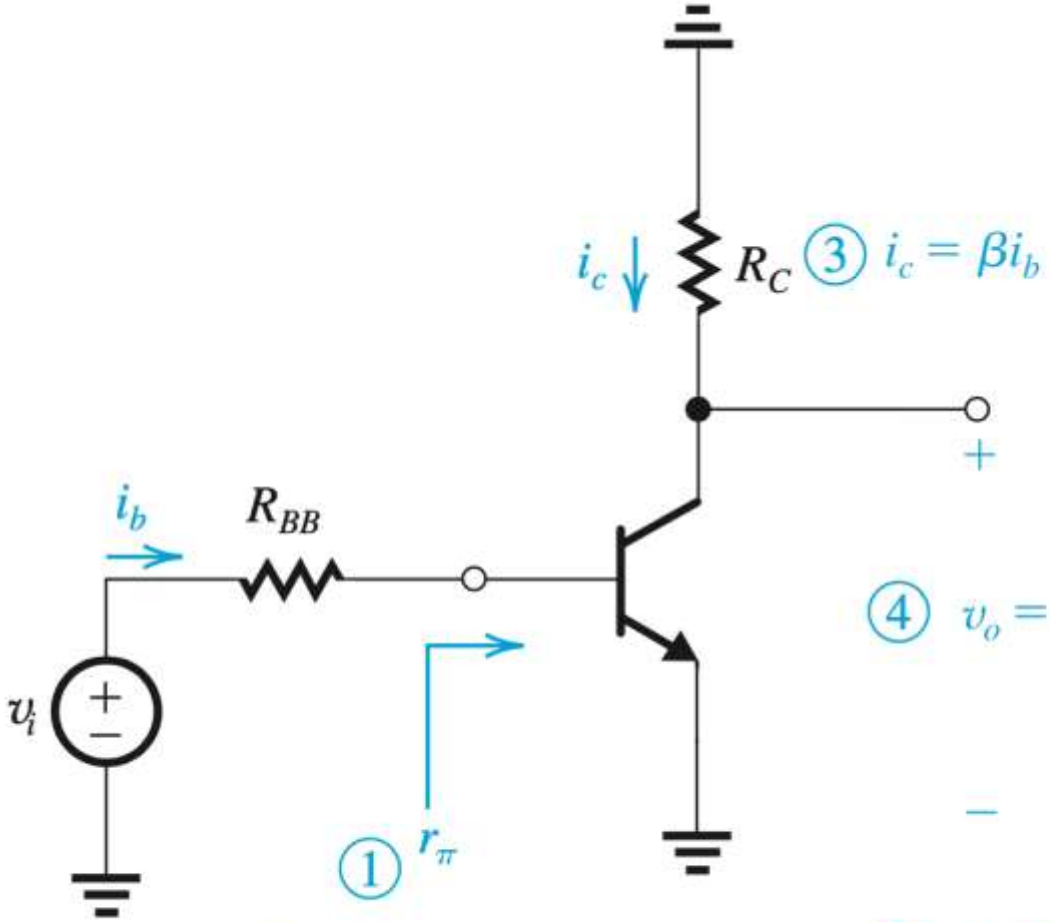


要逐渐养成在电路图上直接进行分析的习惯

①有利于培养对电路的直觉

②能清晰地把握信号在电路中的传输过程

以熟练掌握等效电路模型为前提

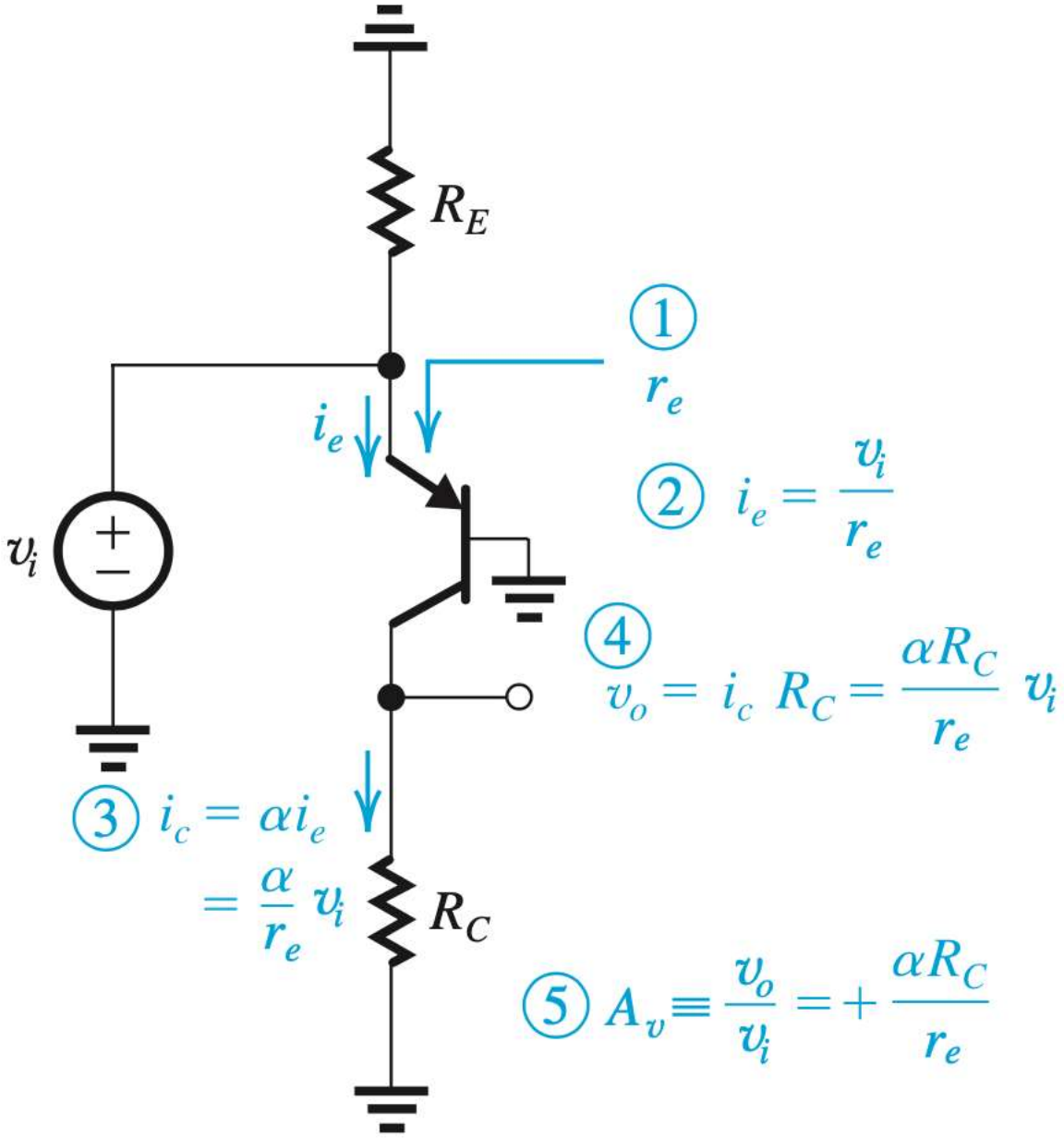


② $i_b = \dfrac{v_i}{R_{BB} + r_\pi}$

④ $v_o = -R_C i_c = -\beta R_C i_b$

$= -\dfrac{\beta R_C}{R_{BB} + r_\pi} v_i$

⑤ $A_v \equiv \dfrac{v_o}{v_i} = -\dfrac{\beta R_C}{R_{BB} + r_\pi}$


R_E
R_C
v_i
i_e
r_e
① r_e
② $i_e = \frac{v_i}{r_e}$
③ $i_c = \alpha i_e = \frac{\alpha}{r_e} v_i$
④ $v_o = i_c R_C = \frac{\alpha R_C}{r_e} v_i$
⑤ $A_v \equiv \frac{v_o}{v_i} = + \frac{\alpha R_C}{r_e}$

小结

Table 7.1 Systematic Procedure for the Analysis of Transistor Amplifier Circuits

1. Eliminate the signal source and determine the dc operating point of the transistor.
2. Calculate the values of the parameters of the small-signal model.
3. Eliminate the dc sources by replacing each dc voltage source by a short circuit and each dc current source by an open circuit.
4. Replace the transistor with one of its small-signal, equivalent-circuit models. Although any of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer in the next section.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance).

Table 7.2 Small-Signal Models of the MOSFET

Small-Signal Parameters

NMOS transistors

- **Transconductance:**

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

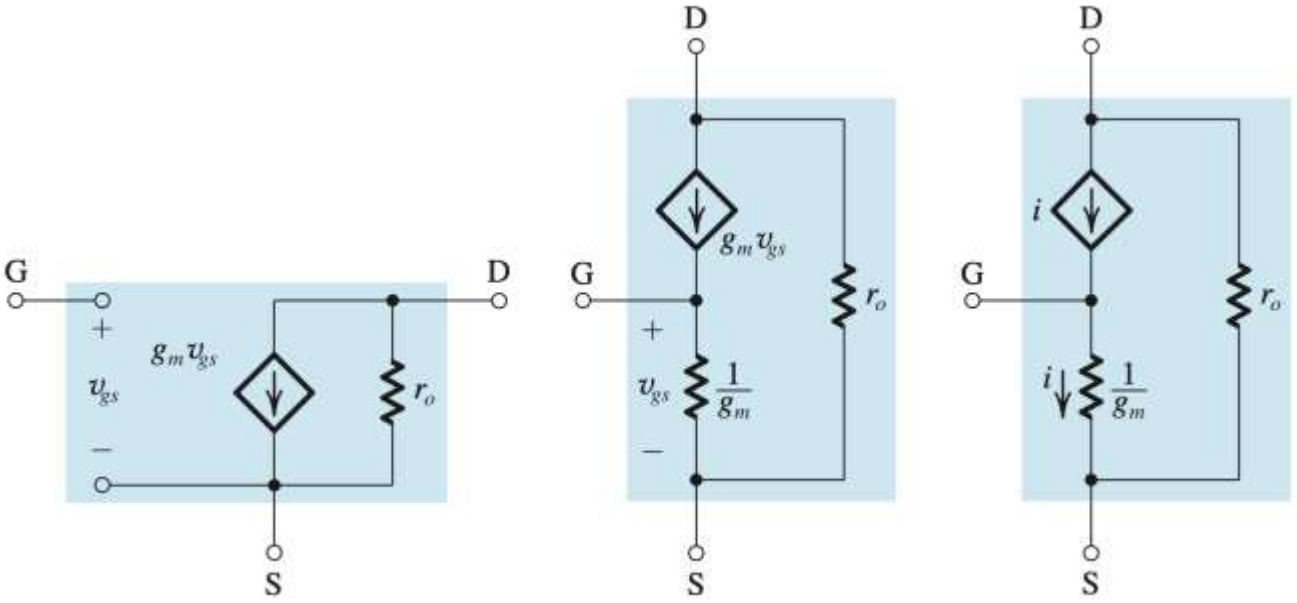
- Output resistance:

$$r_o = V_A / I_D = 1/\lambda I_D$$

PMOS transistors

Same formulas as for NMOS *except* using $|V_{OV}|$, $|V_A|$, $|\lambda|$ and replacing μ_n with μ_p.

Small-Signal, Equivalent-Circuit Models



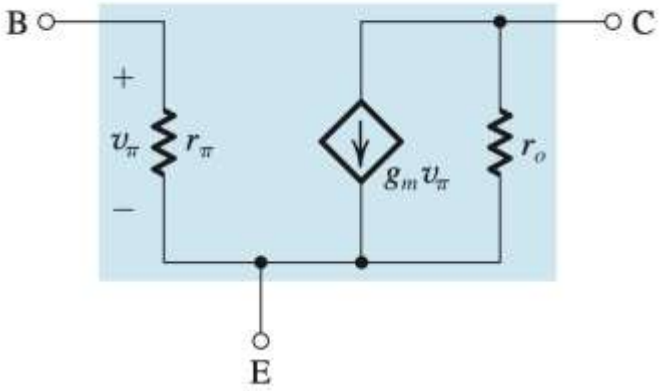
Hybrid-π model

T models

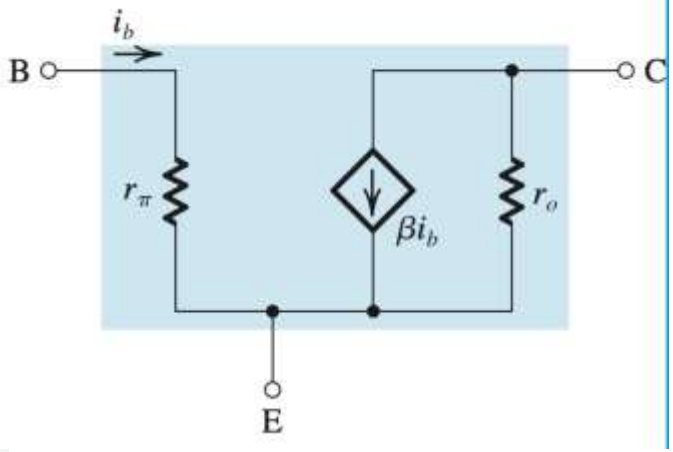
Table 7.3 Small-Signal Models of the BJT

Hybrid-π Model

- $(g_m v_\pi)$ Version

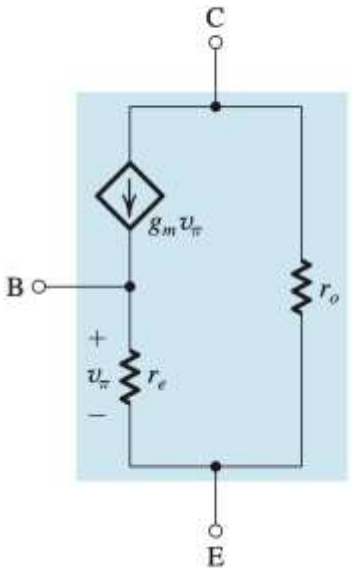


- (βi_b) Version

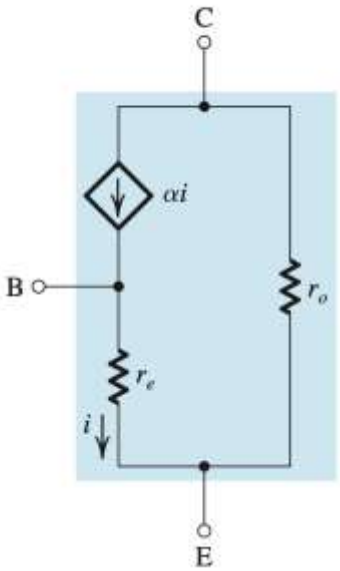


T Model

- $(g_m v_\pi)$ Version



- (αi) Version



Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha \frac{V_T}{I_C} \qquad r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C} \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta + 1) r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

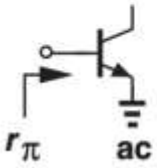
Relationships between α and β

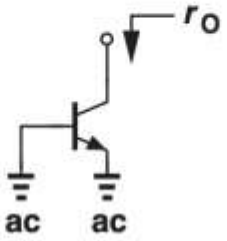
$$\beta = \frac{\alpha}{1 - \alpha} \qquad \alpha = \frac{\beta}{\beta + 1} \qquad \beta + 1 = \frac{1}{1 - \alpha}$$

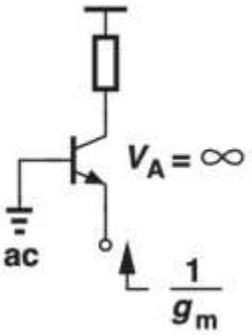
Input and Output Impedances

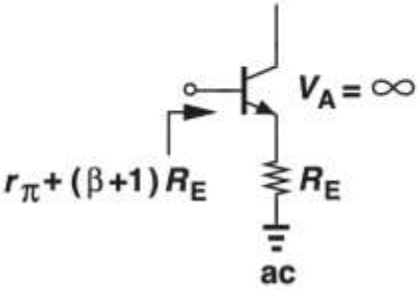
作业

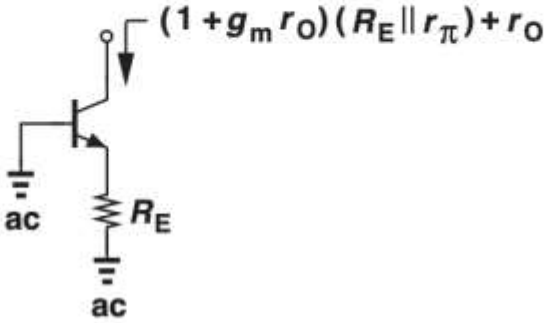
验证常见结构的小信号输入输出电阻表达式（用小信号模型替代MOSFET/BJT，再求输入输出电阻，求输出电阻时注意信号源短路。熟记该图有利于快速直观地分析MOSFET/BJT电路）

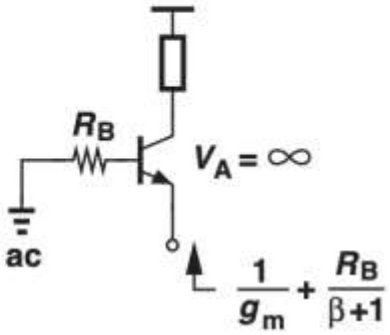


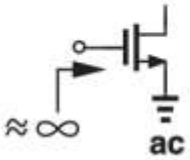


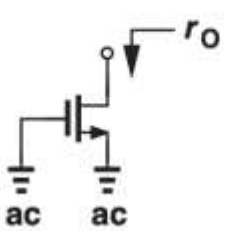


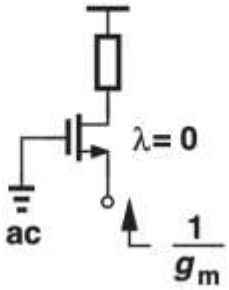


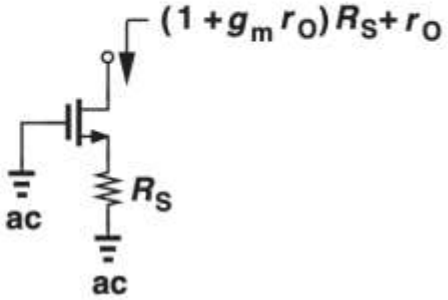












7.4 For the amplifier in Fig. 7.10, let $V_{DD} = 5$ V, $R_D = 10\,\text{k}\Omega$, $V_t = 1$ V, $k_n' = 20\,\mu\text{A/V}^2$, $W/L = 20$, $V_{GS} = 2$ V, and $\lambda = 0$.

(a) Find the dc current I_D and the dc voltage V_{DS}.

(b) Find g_m.

(c) Find the voltage gain.

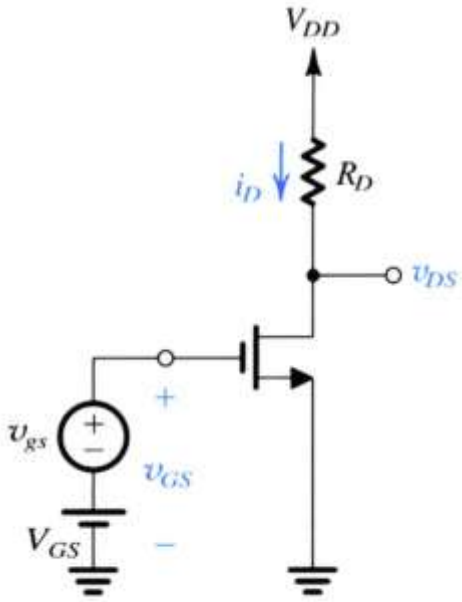
(d) If $v_{gs} = 0.2 \sin \omega t$ volts, find v_{ds} assuming that the small-signal approximation holds. What are the minimum and maximum values of v_{DS}?

(e) Use Eq. (7.28) to determine the various components of i_D. Using the identity $\sin^2 \omega t = \frac{1}{2} - \frac{1}{2}\cos 2\omega t$, show that there is a slight shift in I_D (by how much?) and that there is a second-harmonic component (i.e., a component with frequency 2ω). Express the amplitude of the second-harmonic component as a percentage of the amplitude of the fundamental. (This value is known as the second-harmonic distortion.)

Ans. (a) 0.2 mA, 3 V; (b) 0.4 mA/V; (c) −4 V/V; (d) $v_{ds} = -0.8 \sin \omega t$ volts, 2.2 V, 3.8 V; (e) $i_D = (204 + 80 \sin \omega t - 4 \cos 2\omega t)\,\mu\text{A}$, 5%

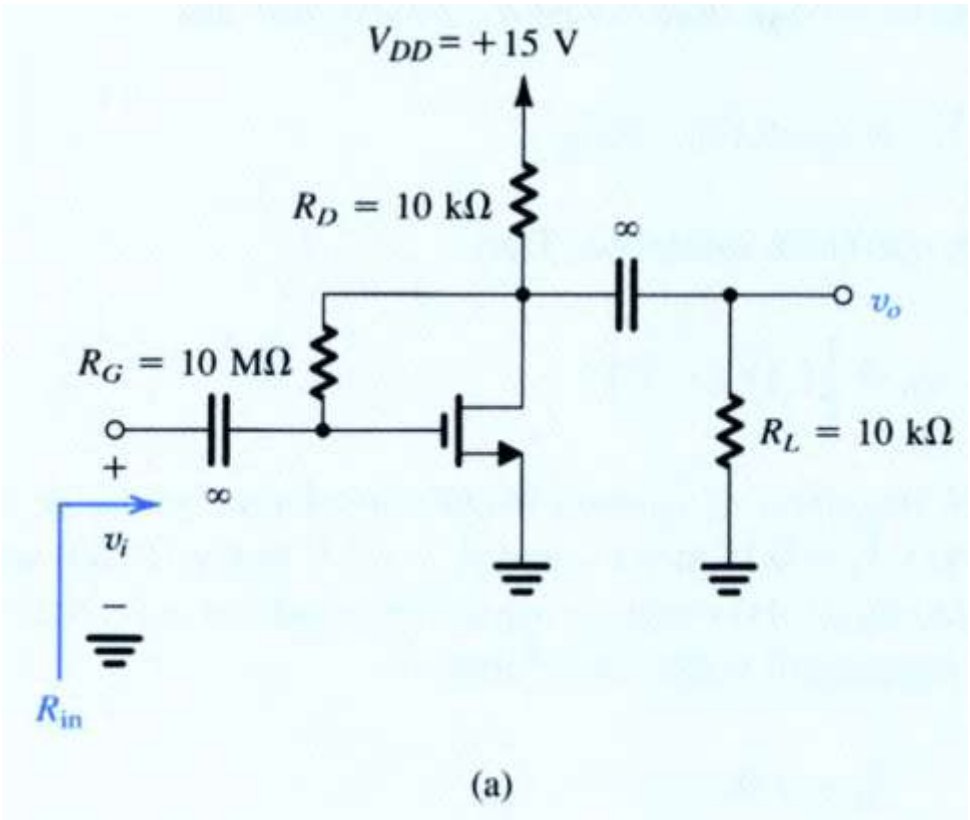
$$i_D = \frac{1}{2}k_n(V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2}k_n(V_{GS} - V_t)^2 + k_n(V_{GS} - V_t)v_{gs} + \frac{1}{2}k_n v_{gs}^2 \qquad (7.28)$$



D7.10 Consider the amplifier circuit of Fig. 7.16(a) without the load resistance R_L and with channel-length modulation neglected. Let $V_{DD} = 5$ V, $V_t = 0.7$ V, and $k_n = 1$ mA/V^2. Find V_{OV}, I_D, R_D, and R_G to obtain a voltage gain of -25 V/V and an input resistance of 0.5 MΩ. What is the maximum allowable input signal, $\hat{v}_i$?

Ans. 0.319 V; 50.9 μA; 78.5 kΩ; 13 MΩ; 27 mV



(a)

7.20 The transistor in Fig. E7.20 is biased with a constant current source $I = 1$ mA and has $\beta = 100$ and $V_A = 100$ V.

(a) Neglecting the Early effect, find the dc voltages at the base, emitter, and collector.

(b) Find g_m, r_π, and r_o.

(c) If terminal Z is connected to ground, X to a signal source v_{sig} with a source resistance $R_{sig} = 2$ kΩ, and Y to an 8-kΩ load resistance, use the hybrid-π model shown in Fig. 7.26 to draw the small-signal equivalent circuit of the amplifier. (Note that the current source I should be replaced with an open circuit.) Calculate the overall voltage gain v_y/v_{sig}. If r_o is neglected, what is the error in estimating the gain magnitude? (*Note:* An infinite capacitance is used to indicate that the capacitance is large enough to act as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.)

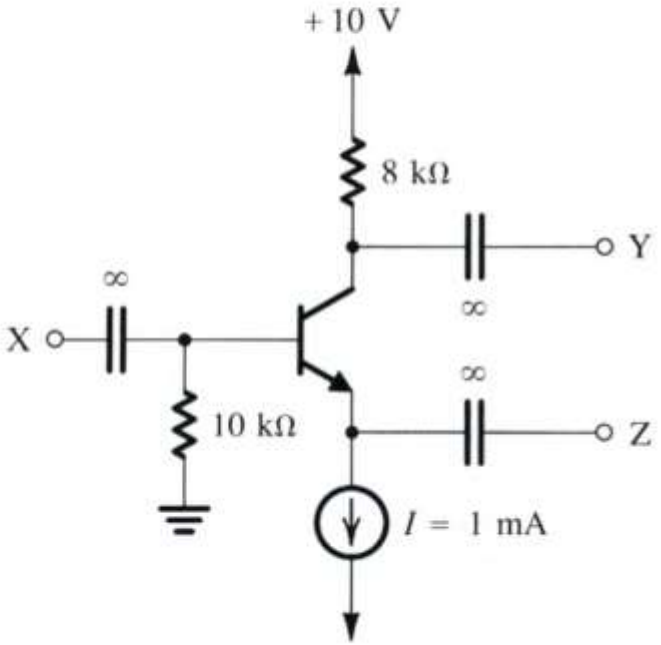


Figure E7.20

Ans. (a) –0.1 V, –0.8 V, +2.1 V; (b) 40 mA/V, 2.5 kΩ, 100 kΩ; (c) –77 V/V, +3.9%