Frequency Synthesizers (1/2)

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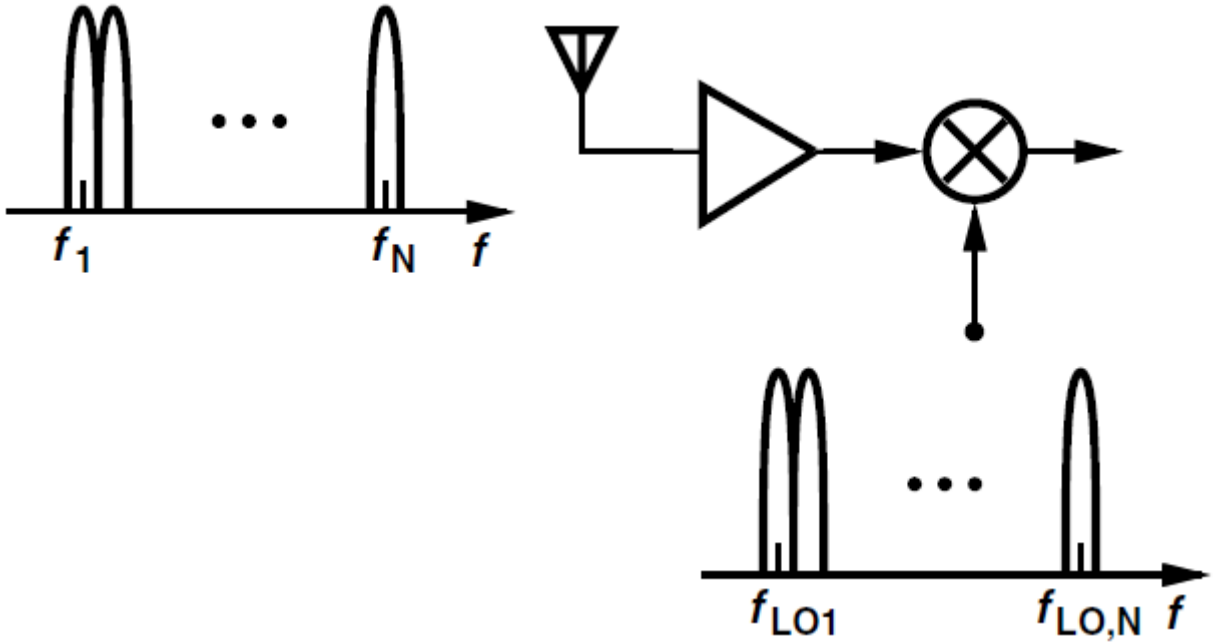
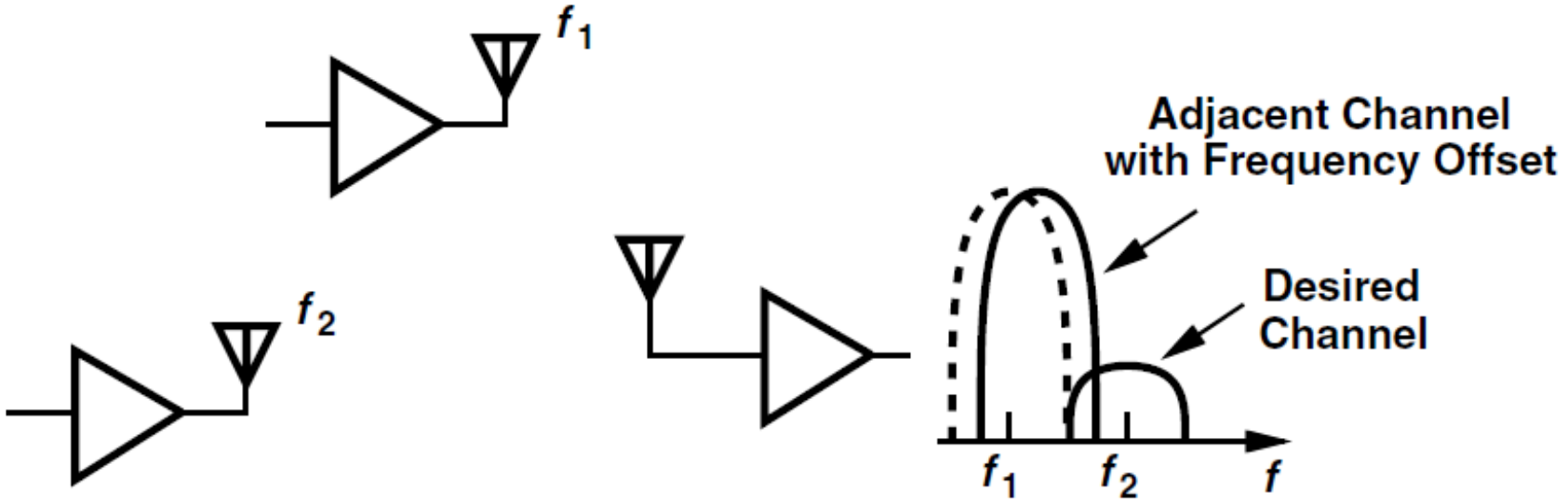
Channel Selection



- For example, Bluetooth has 80 1-MHz channels in the range of 2.400 GHz to 2.480 GHz.
- For each channel, the corresponding frequency is allocated to the user, requiring that the LO frequency be set by a frequency synthesizer.

[B. Razavi, RF Microelectronics]

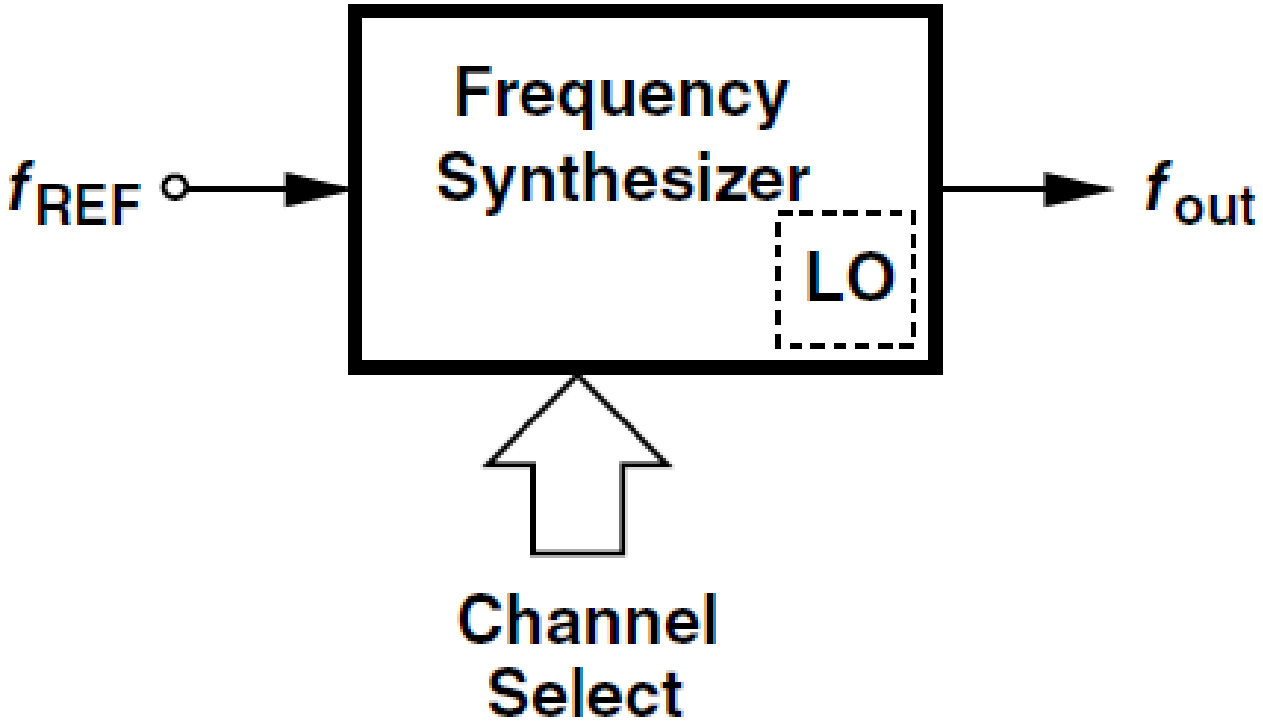
LO Frequency Error



- Narrow, tightly-spaced channels in wireless standards tolerate little error in transmit and receive carrier frequencies
- A slight shift leads to significant spillage of a high-power interferer into a desired channel.

[B. Razavi, RF Microelectronics]

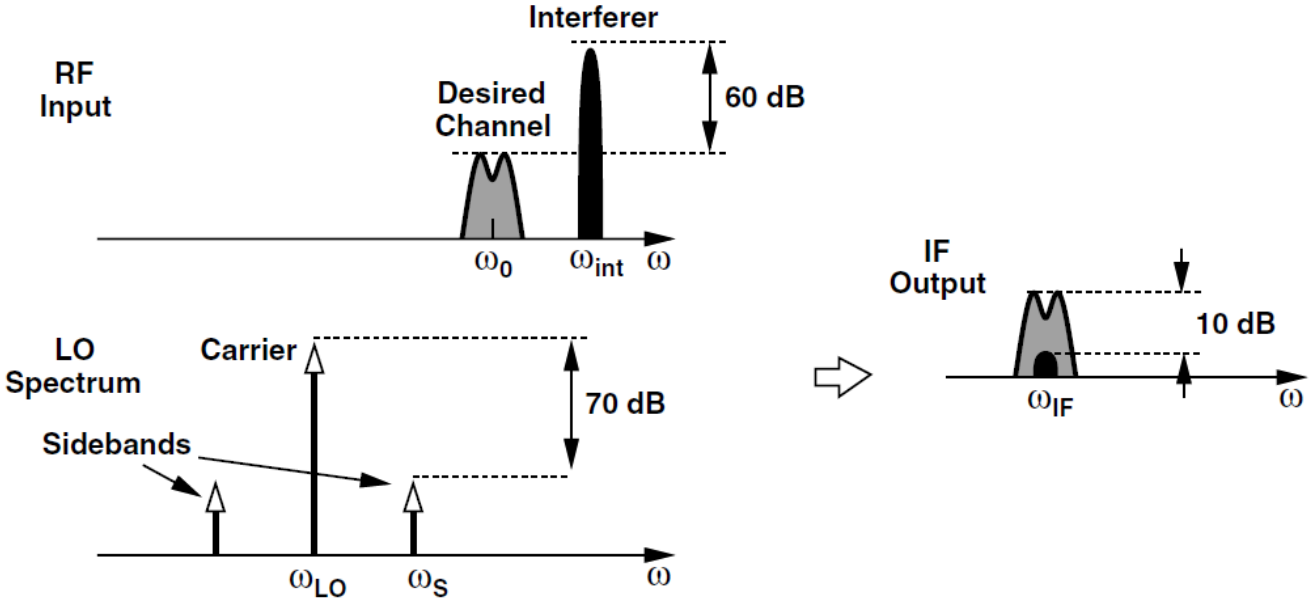
Conceptual Picture



- The output frequency is generated as a multiple of a precise reference, f_{REF}, and this multiple is changed by the channel selection command so as to cover the carrier frequencies required by the standard

[B. Razavi, RF Microelectronics]

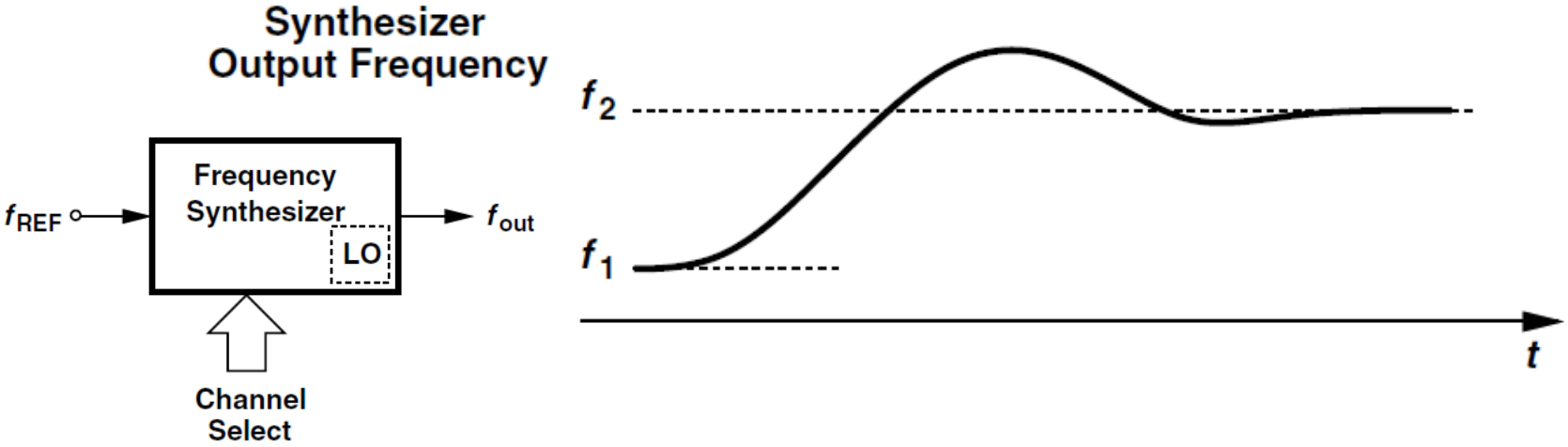
Reciprocal Mixing



- If the control voltage of a VCO is periodically disturbed, then the output spectrum contains sidebands symmetrically disposed around the carrier (spurs)
- Upon downconversion mixing, the desired channel is convolved with the carrier and the interferer with the sideband

[B. Razavi, RF Microelectronics]

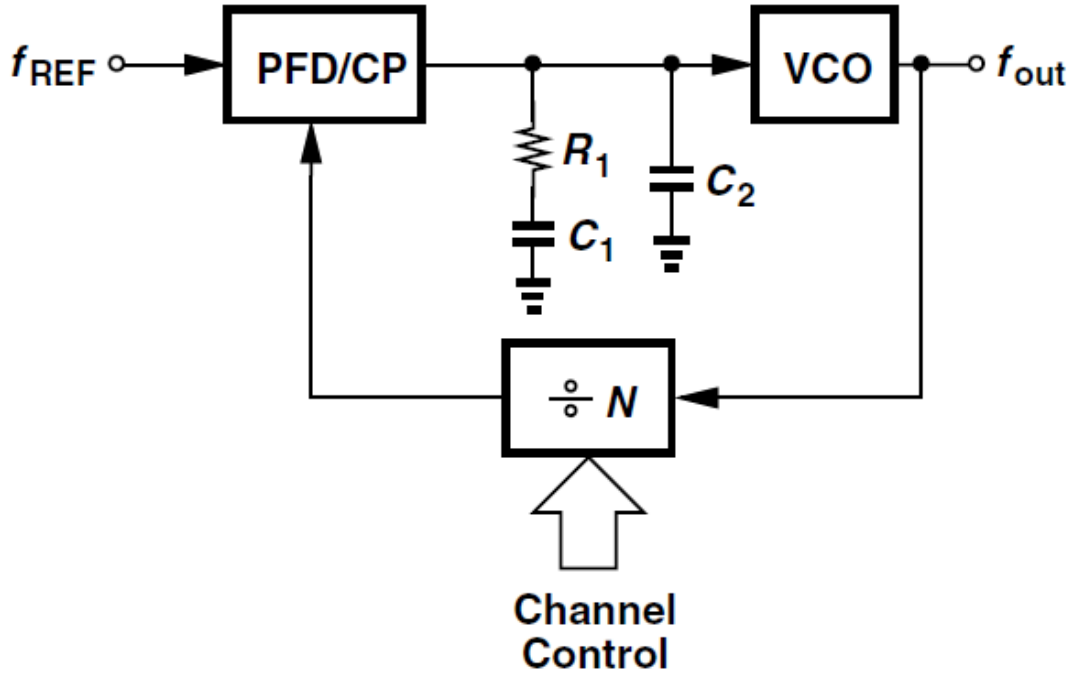
Frequency Settling



- When the digital channel selection command changes value, the synthesizer takes a finite time to settle to a new output frequency, which is called the "lock time"
- This settling time directly determines the channel switching time of a transmitter or receiver

[B. Razavi, RF Microelectronics]

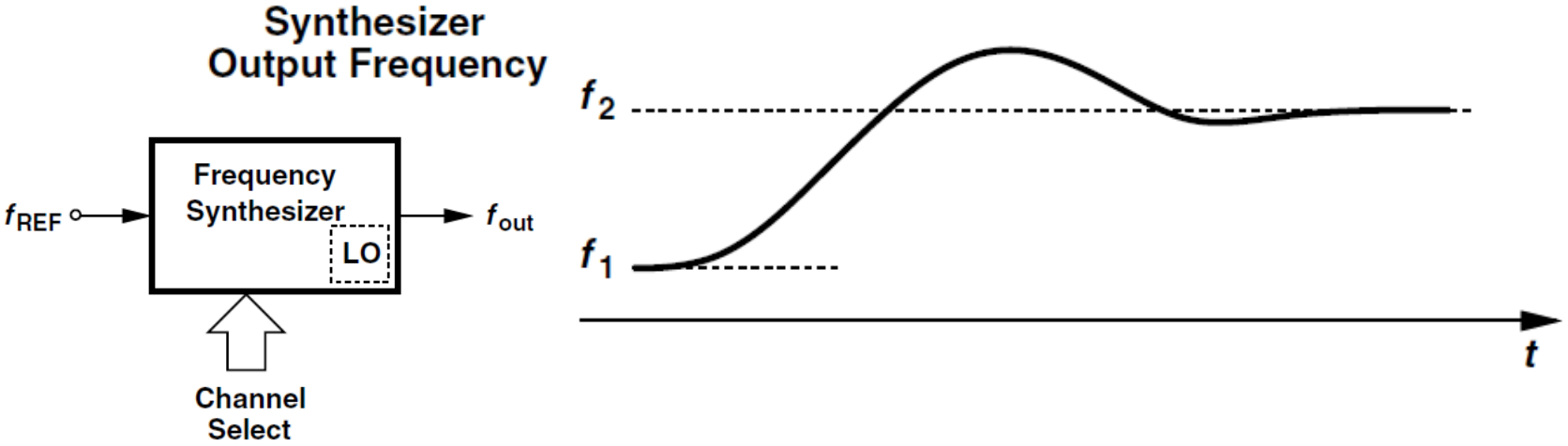
Integer-N Frequency Synthesizer



- Integer-N synthesizers produce an output frequency that is an integer multiple of the reference frequency
- If N increases by 1, then f_{out} increases by f_{REF}; i.e., the minimum channel spacing is equal to the reference frequency

[B. Razavi, RF Microelectronics]

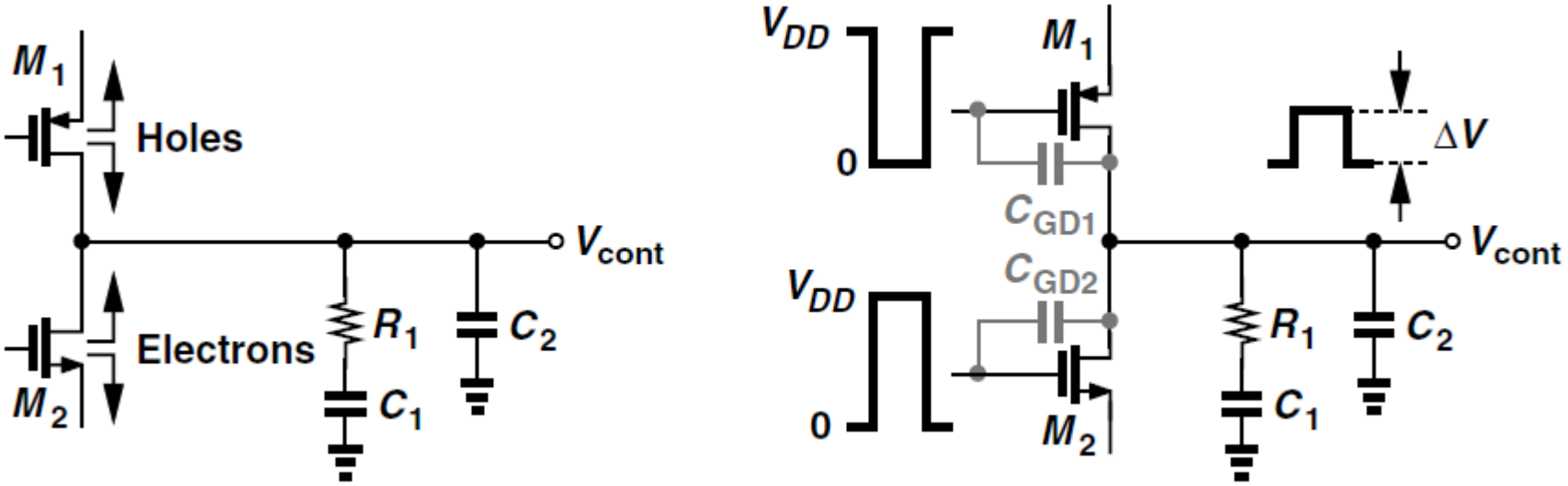
Integer-N Frequency Synthesizer



- The principal drawback of the integer-N architecture is that the channel spacing is equal to the reference frequency
- A rule of thumb for the settling of PLLs is 100 times the reference period
- The lock time (≈100 input cycles) and the loop bandwidth are tightly related to the channel spacing

[B. Razavi, RF Microelectronics]

Charge Injection/Clock Feedthrough

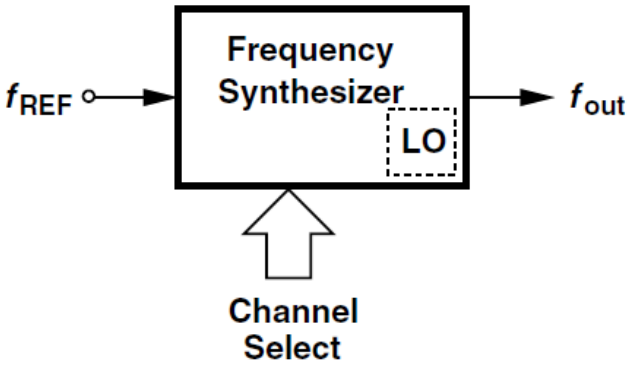


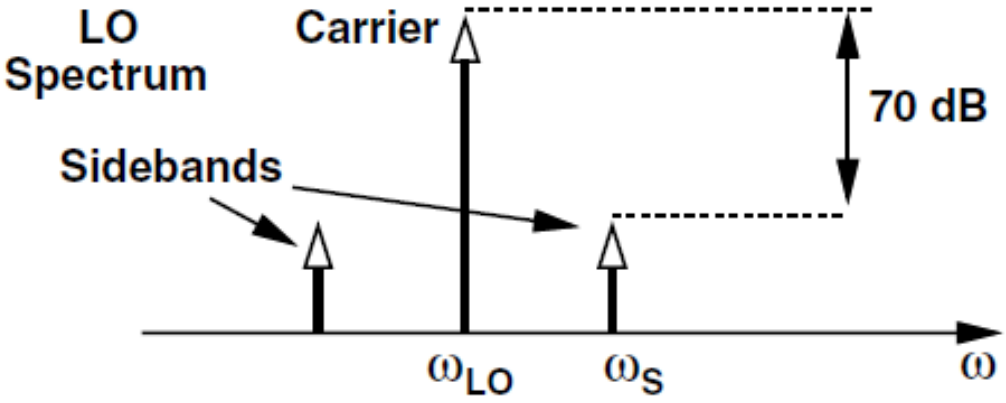
- As the switches turn on, they absorb this charge and as they turn off, they dispel this charge, in both cases through their source and drain terminals

- The clock feedthrough relates to the gate-drain overlap capacitance of the switches

[B. Razavi, RF Microelectronics]

Spurs



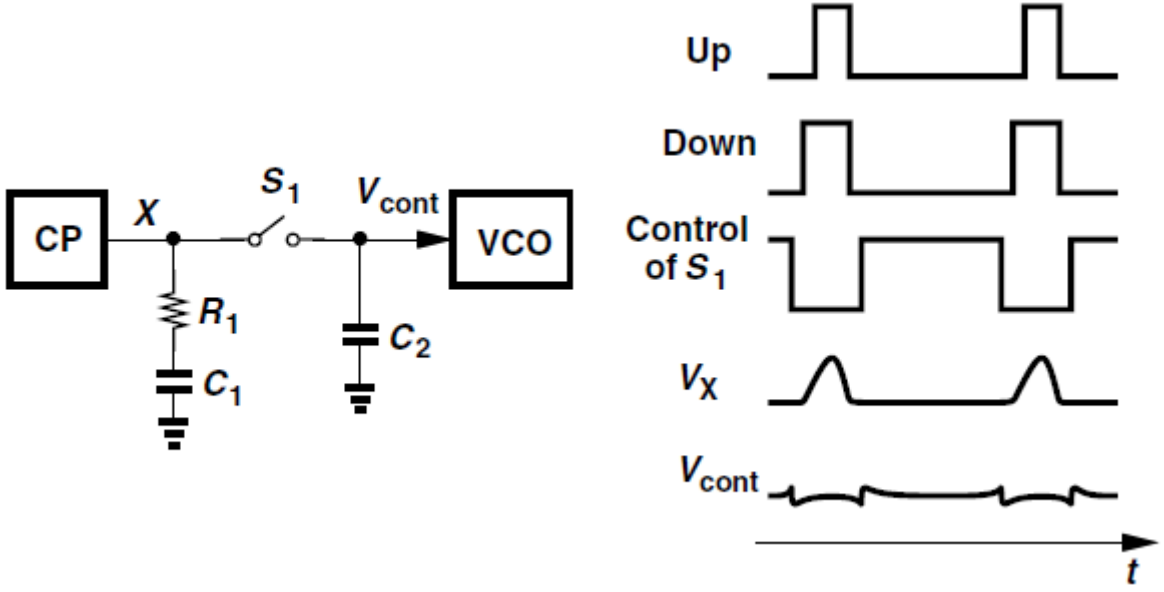


- The issues such as charge sharing, channel length modulation, and Up and Down current mismatch lead to spurs
- There is trade-off between the loop bandwidth and the level of reference spurs

[B. Razavi, RF Microelectronics]

Spur Reduction

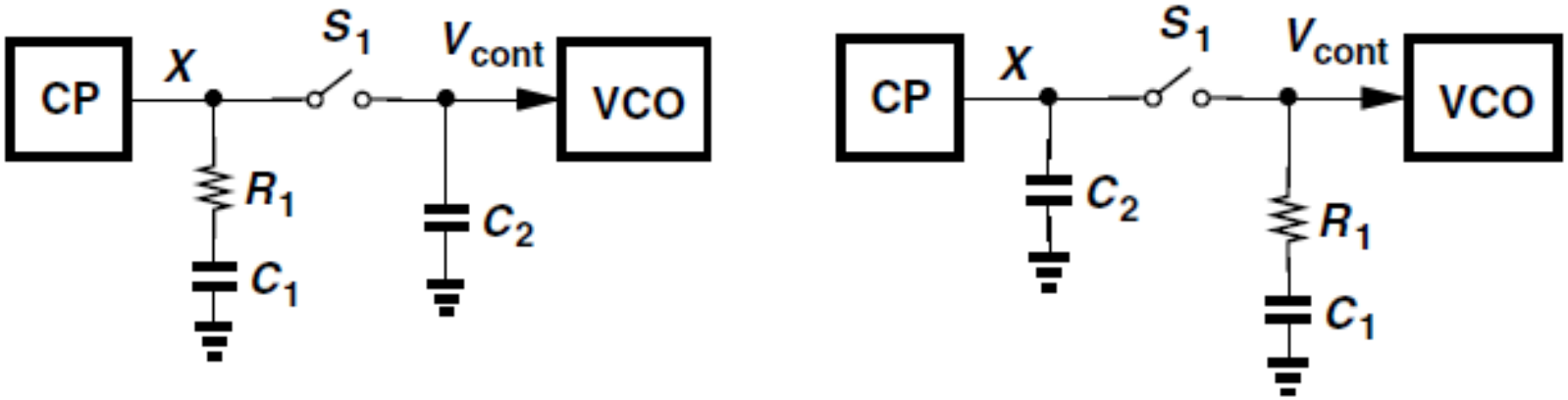
- A key point in devising spur reduction techniques is that the disturbance of the control voltage occurs primarily at the phase comparison instant
- We therefore surmise that the output sidebands (spurs) can be lowered if V_{cont} is isolated from the disturbance for that duration



[B. Razavi, RF Microelectronics]

Spur Reduction

- Unfortunately, the isolation of V_{cont} from the disturbance also eliminates the role of R_1, leading to an unstable PLL
- By switching R_1-C_1 with C_2, the role of R_1 is maintained



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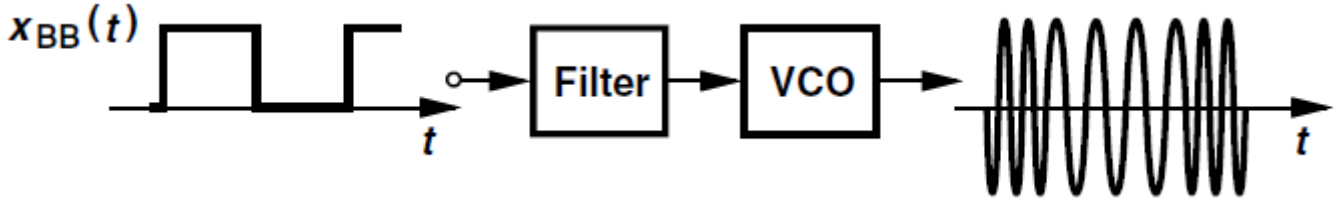
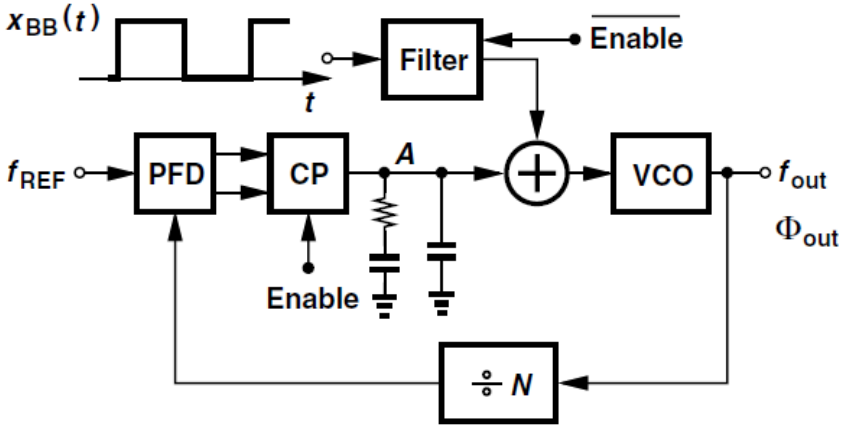
PLL Based Modulation

- FSK and PSK modulation can be realized by means of a VCO that senses the binary data
- In open-loop modulation, the VCO center frequency drifts with time and temperature with no bound



- One remedy is to phase-lock the VCO periodically to a reference so as to reset its center frequency



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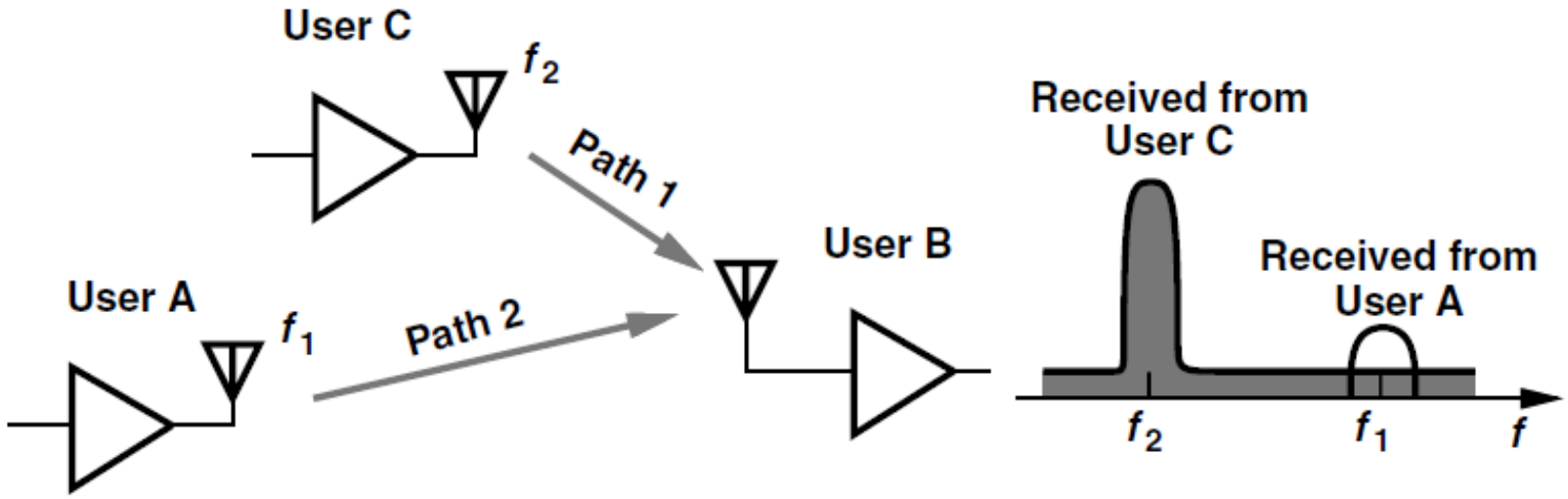
Noise Issue

- User B receives a weak signal around f_1 from user A while user C, located in the close proximity of user B, transmits a high power around f_2 and significant broadband noise
- The noise transmitted by user C corrupts the desired signal around f_1



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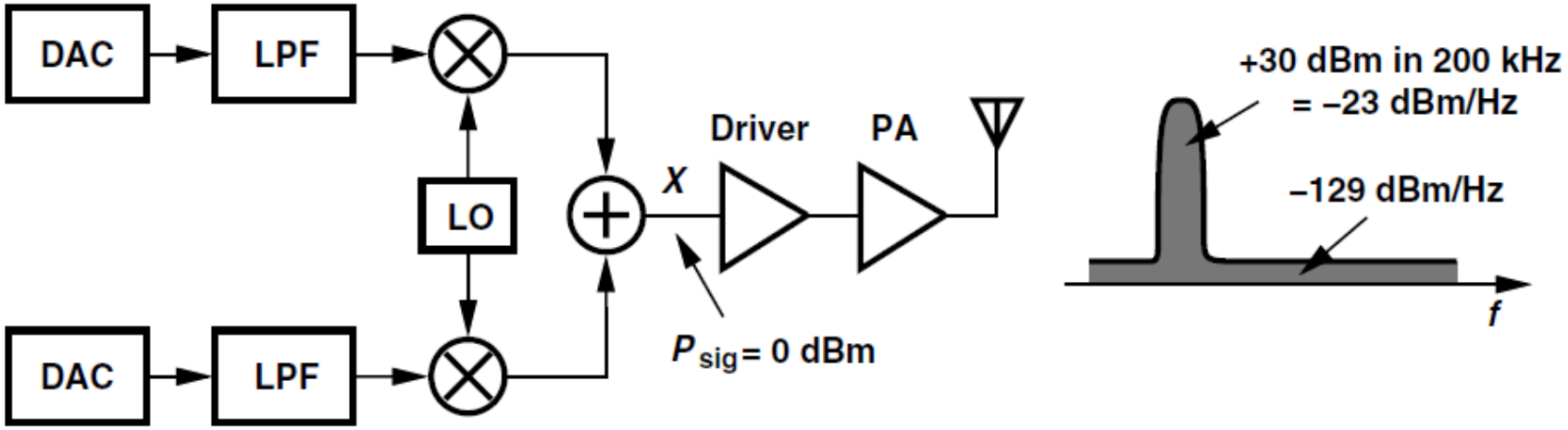
Direct-Conversion TX

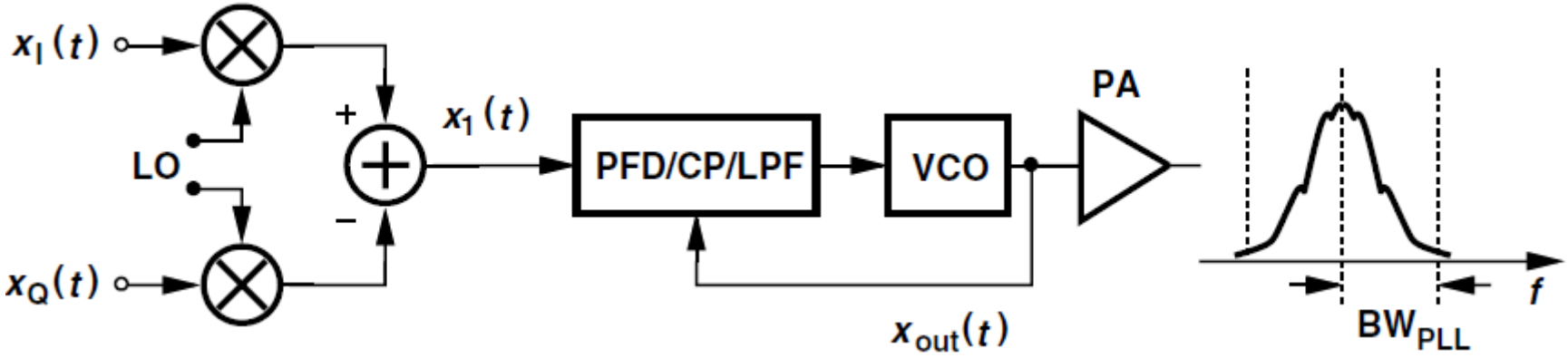
- Each stage in the signal path contributes noise, producing high output noise in the RX band even if the baseband LPF suppresses the out-of-channel DAC output noise
- The far-out phase noise of the LO also manifests itself as broadband noise at the PA output



- The maximum noise that a GSM transmitter is allowed to emit in the GSM receive band, namely, -129 dBm/Hz

[B. Razavi, RF Microelectronics]

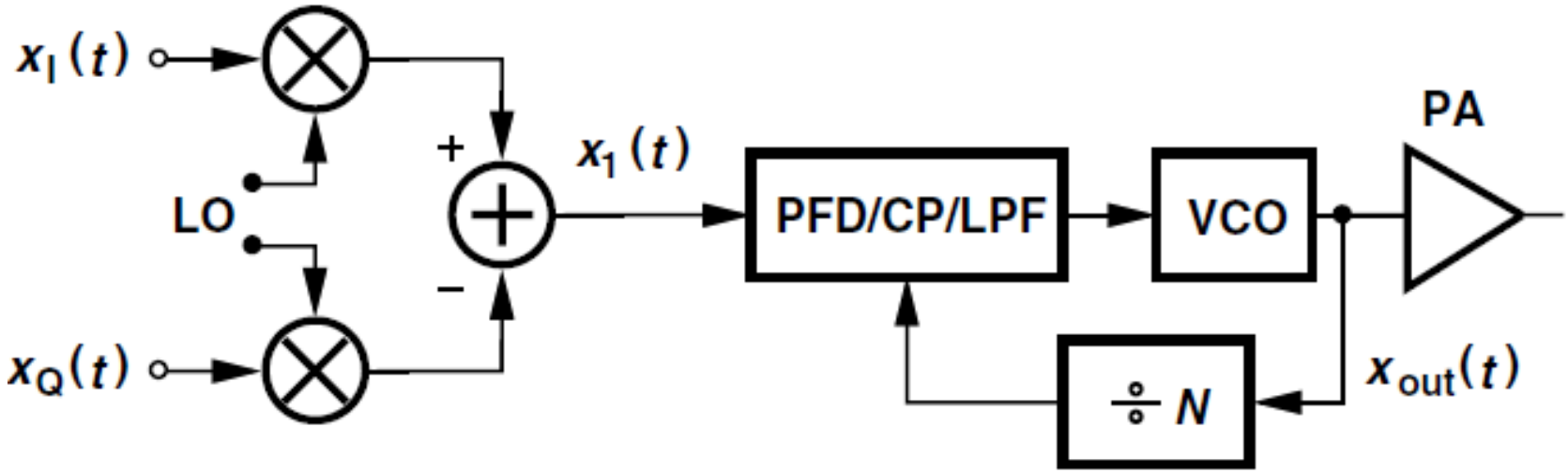
PLL Modulation



- If the PLL bandwidth is only large enough to accommodate the signal, then the broadband noise traveling to the antenna arises primarily from the far-out phase noise of the VCO. So this architecture need only minimize the broadband noise of one building block (VCO)

[B. Razavi, RF Microelectronics]

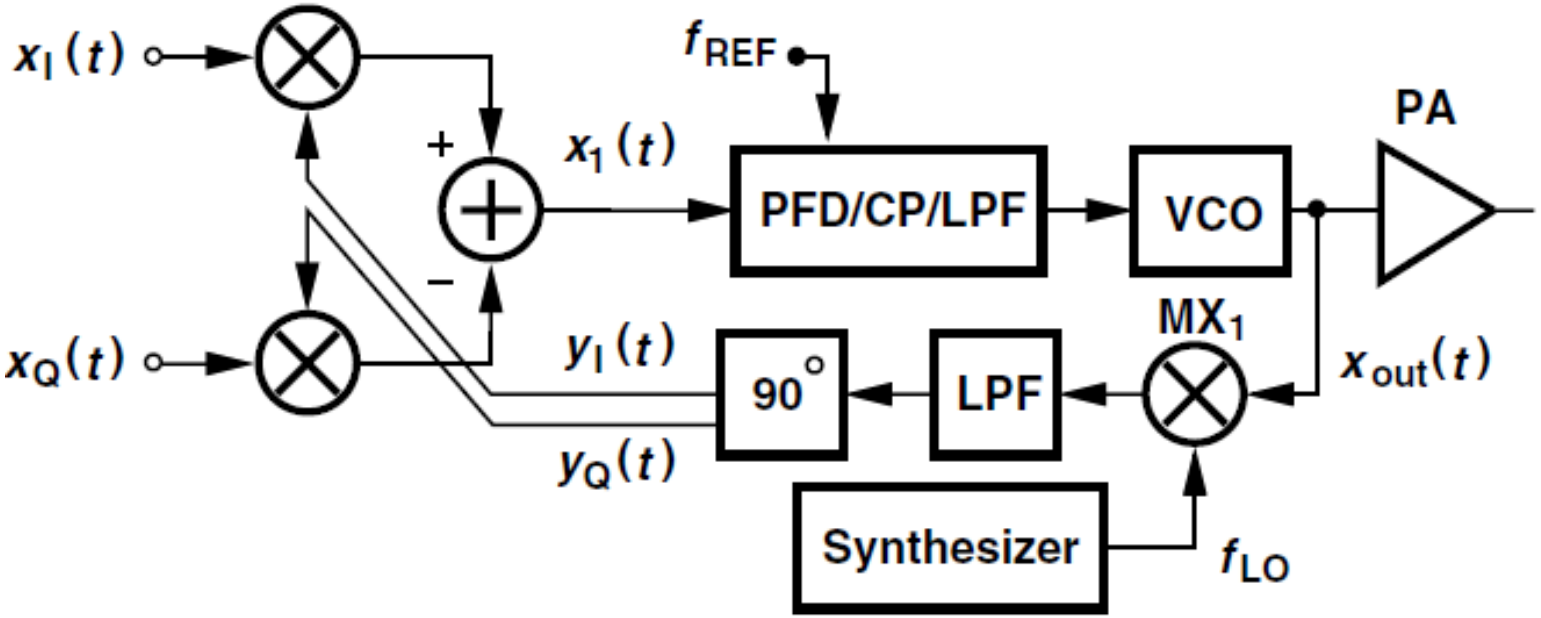
Nx PLL Modulation



- Adding a feedback divider to the PLL proportionally reduces the carrier frequency
- But the PLL multiplies the phase by a factor of N, altering the signal bandwidth and modulation

[B. Razavi, RF Microelectronics]

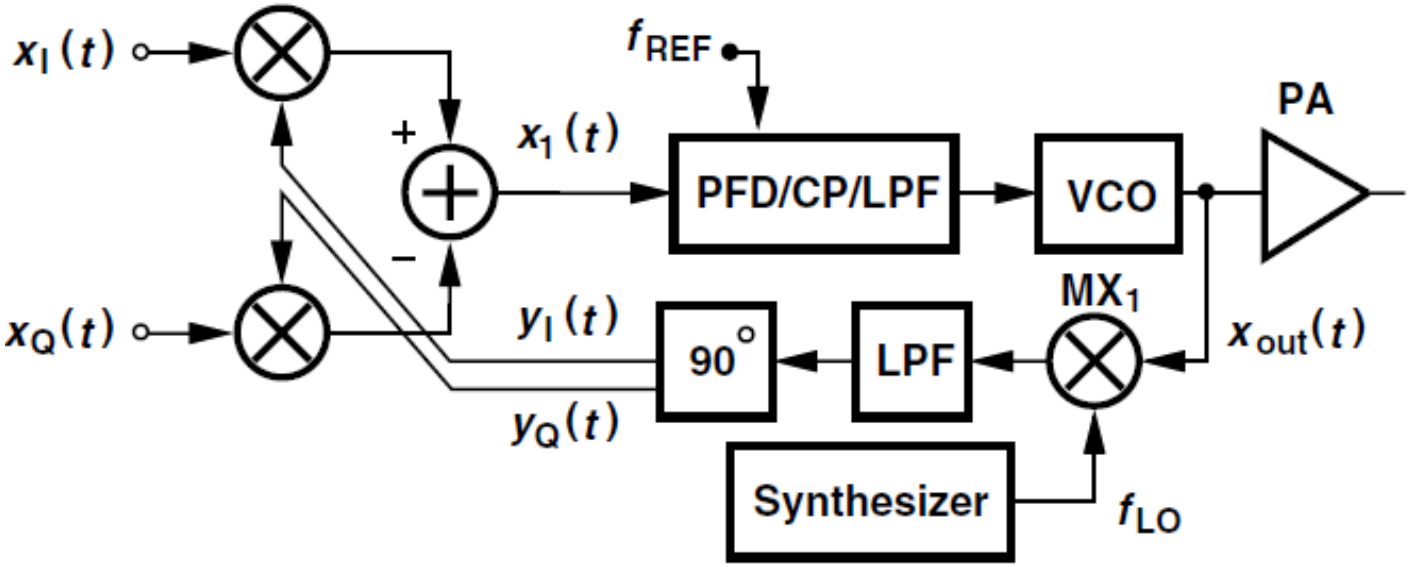
Offset PLL Modulation



- An "offset mixer," MX_1, downconverts the output to a center frequency of f_{REF}, and the result is separated into quadrature phases, mixed with the baseband signals, and applied to the PFD

[B. Razavi, RF Microelectronics]

Offset PLL Modulation

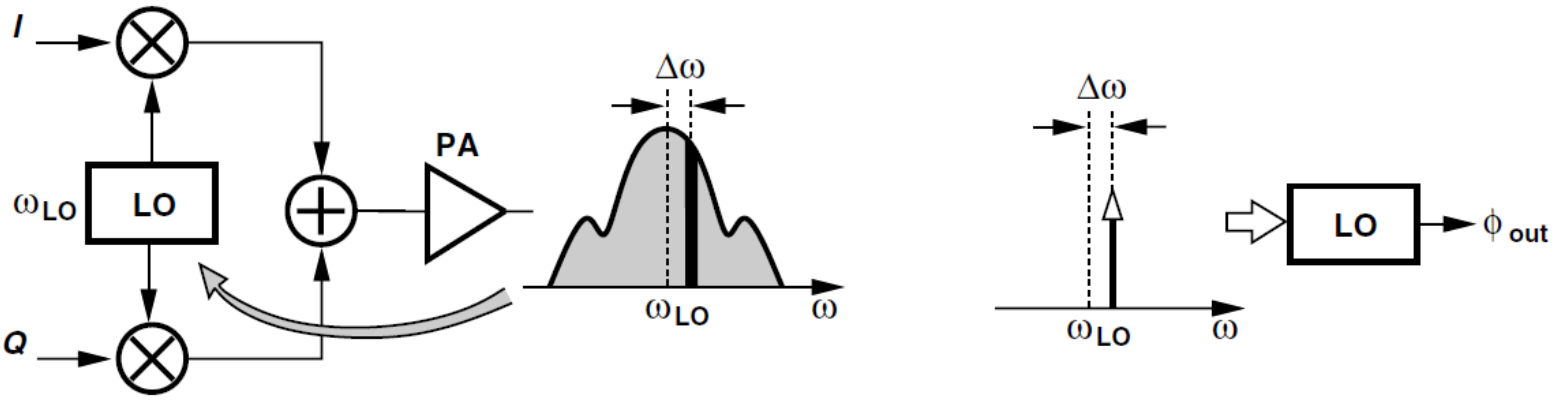


- The local oscillator waveform driving the offset mixer must be generated by another PLL
- The presence of two VCOs on the same chip raises mutual injection pulling between them. To ensure a sufficient difference between their frequencies, the offset frequency, f_{REF}, must be chosen high enough

[B. Razavi, RF Microelectronics]

Oscillator Pulling

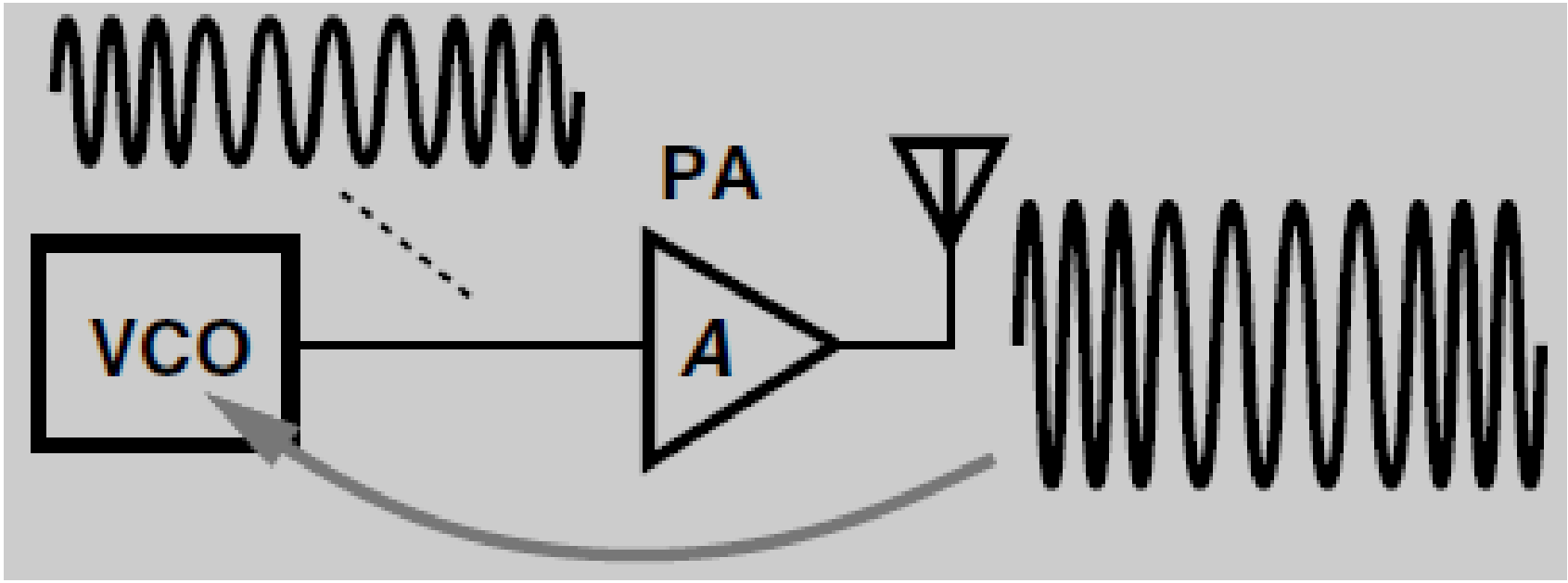
- The PA output exhibits very large swings, which couple to the oscillator through the silicon substrate, package parasitics, and traces on the PCB.



- In order to avoid injection pulling, the PA output frequency and the oscillator frequency must be made sufficiently different

[B. Razavi, RF Microelectronics]

VCO Pulling

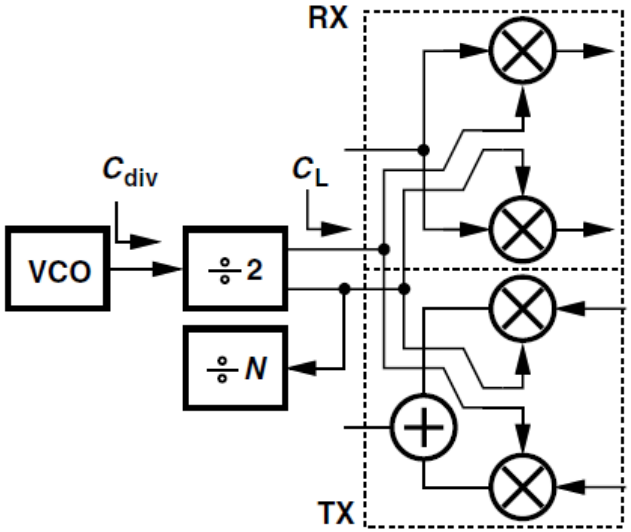


- The instantaneous output voltage of the PA is simply an amplified replica of that of the VCO
- The overall effect on the VCO is typically negligible

[B. Razavi, RF Microelectronics]

Divider

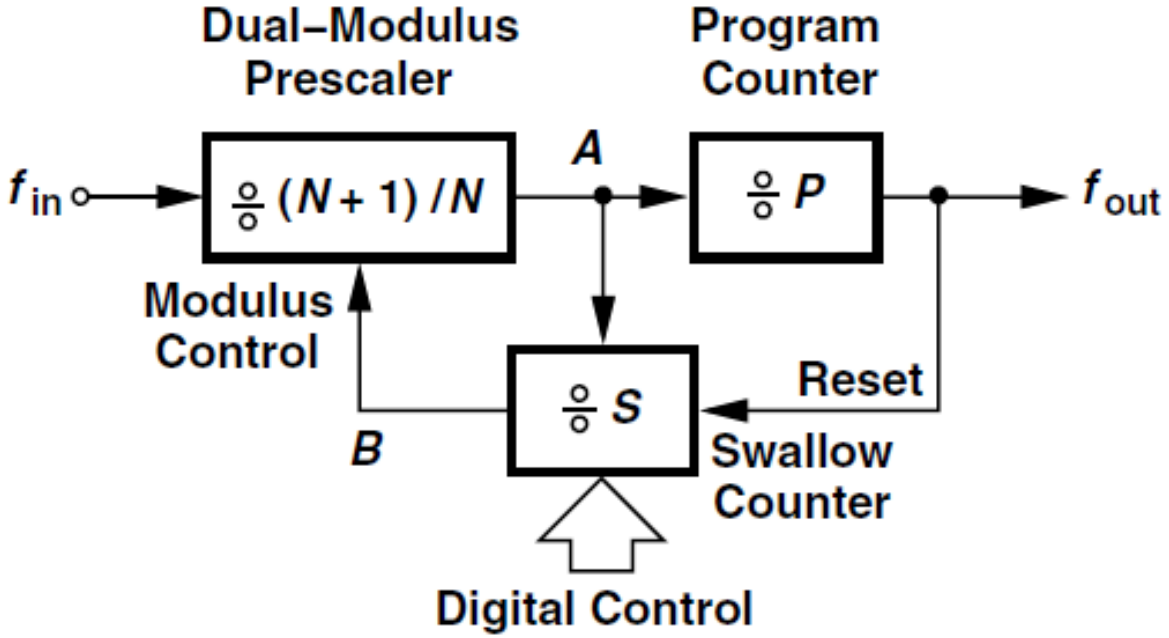
- The divider modulus, N, must change in unity steps
- The first stage of the divider must operate as fast as the VCO
- The divider input capacitance load the VCO
- The divider must consume low power



- A buffer can be inserted at the input and/or output of the divider but at the cost of greater power dissipation

[B. Razavi, RF Microelectronics]

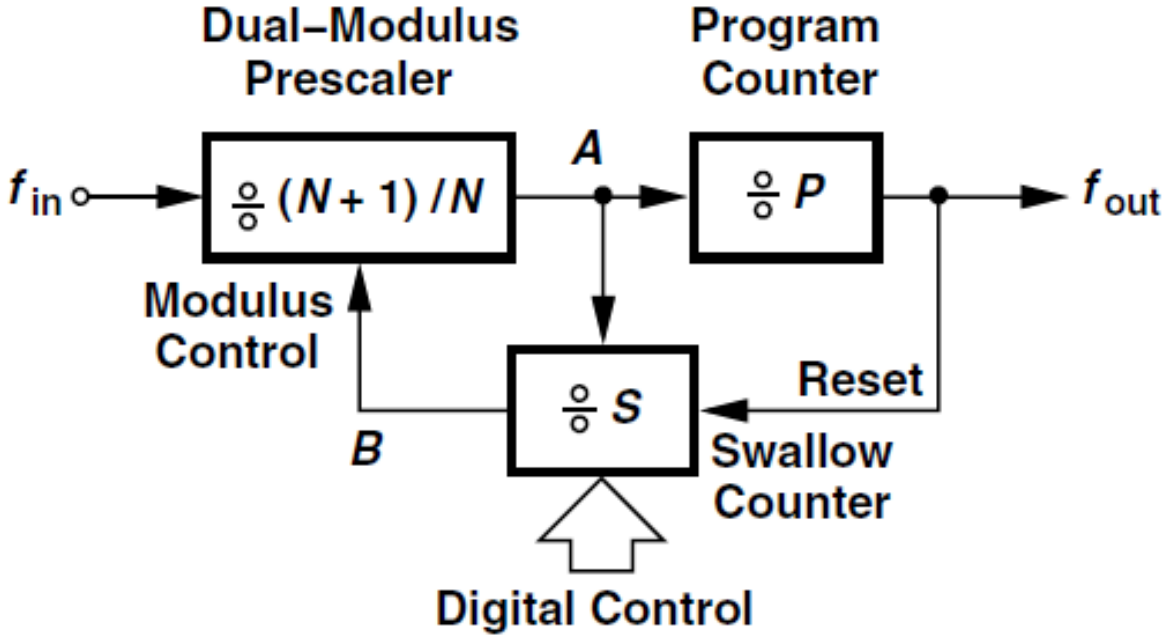
Pulse Swallow Divider



- Dual-modulus prescaler: provides a divide ratio of N+1 or N
- Swallow counter: divides its input frequency by a factor of S, which controls the modulus of the prescaler
- Program counter: has a constant modulus, P. When it counts P pulses at its input, it resets the swallow counter

[B. Razavi, RF Microelectronics]

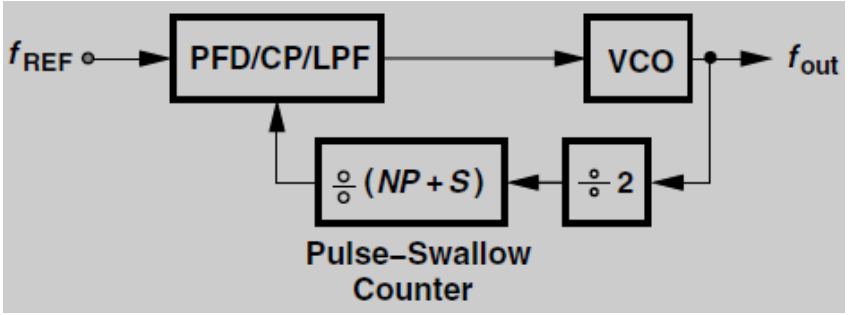
Pulse Swallow Divider

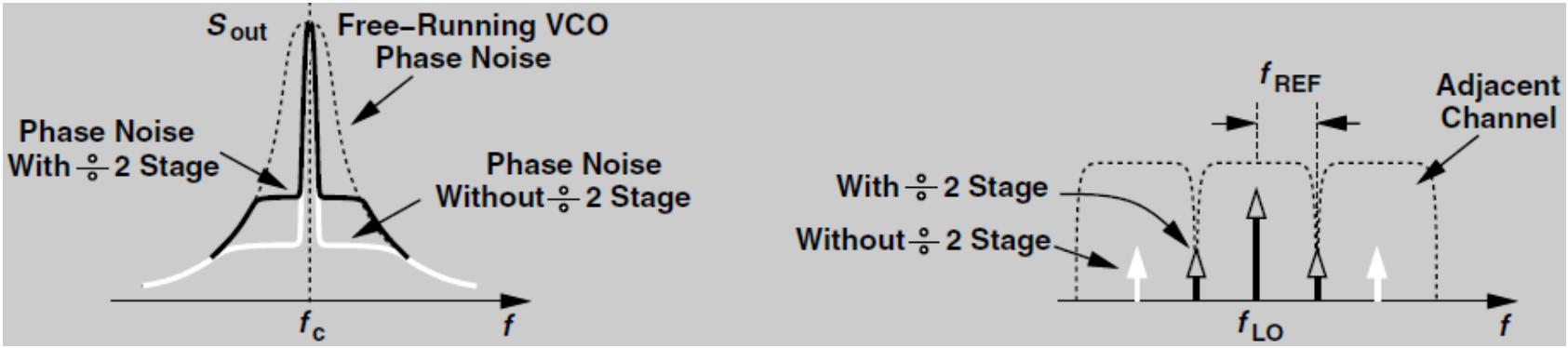


- Adding the total number of the pulses at the prescaler input in the two modes, we have (N+1)S+N(P-S)=NP+S
- Sensing the high-frequency input, the prescaler proves the most challenging (Power Scaling Techniques)

[B. Razavi, RF Microelectronics]

Pulse Swallow Divider with ÷2

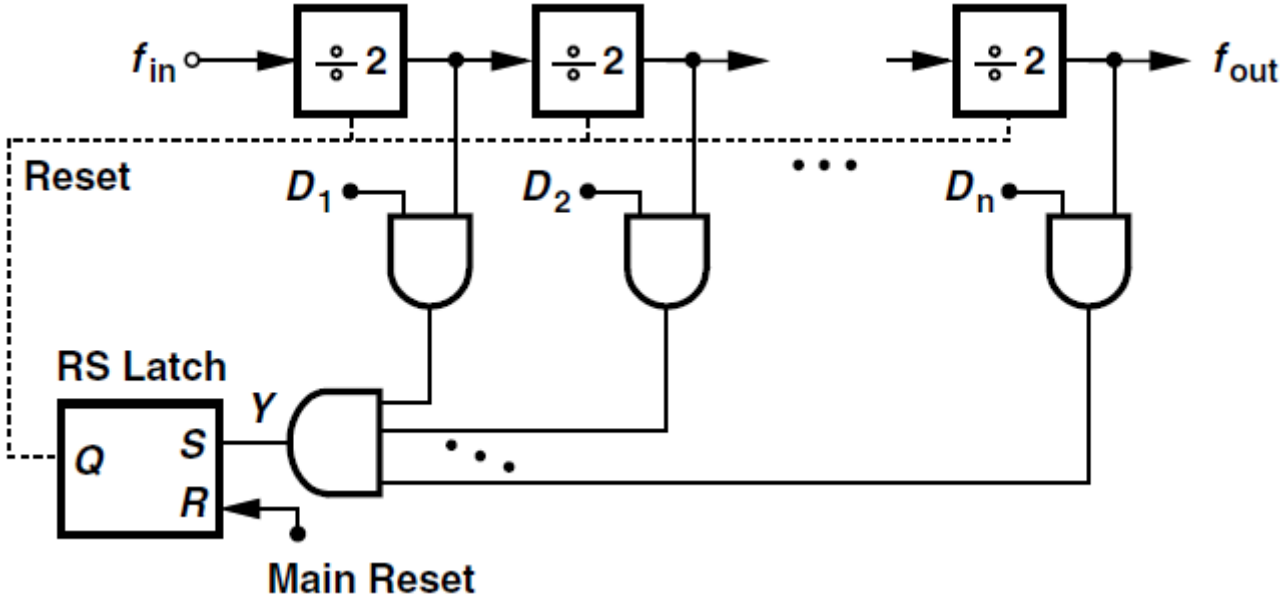




- f_{REF}=fch/2. The lock speed and the loop bandwidth are therefore scaled down by a factor of two, making the VCO phase noise more pronounced
- The reference sideband lies at the edge of the adjacent channel rather than in the middle of the channel

[B. Razavi, RF Microelectronics]

Swallow Counter

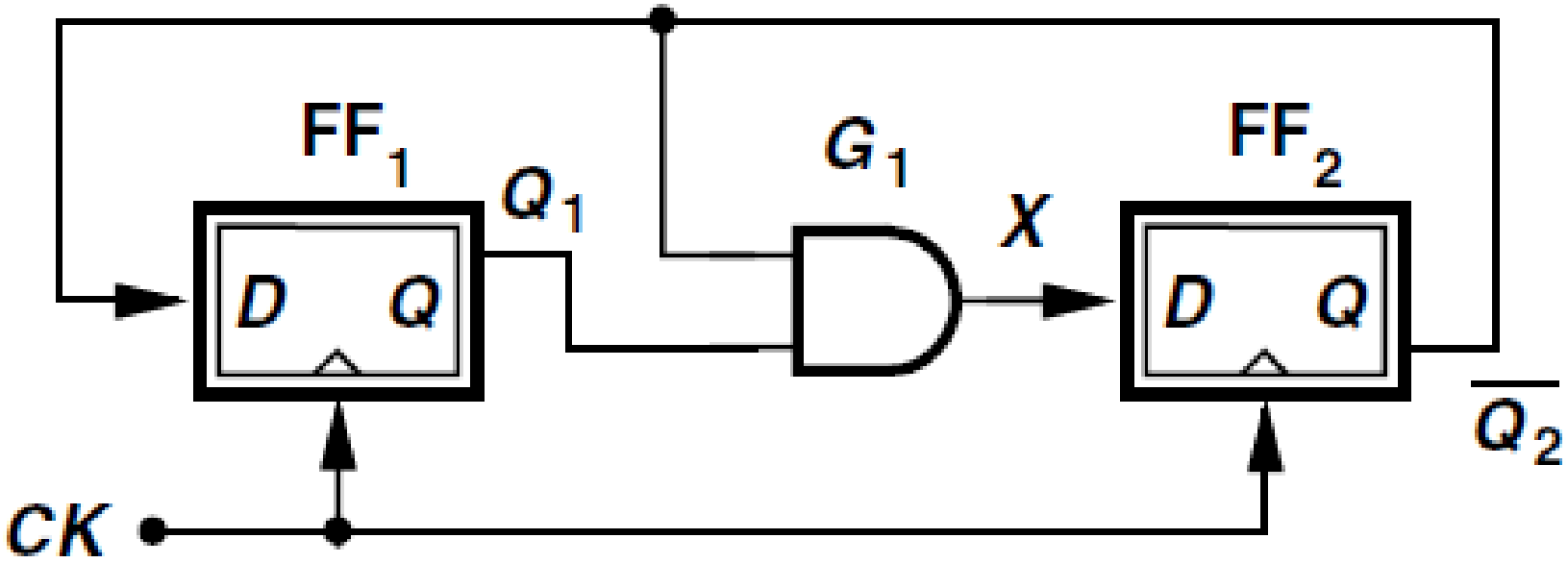


- Cascaded ÷2 stages count the input and the NAND gates compare the count with the digital input, $D_nD_{n-1}\cdots D_1$
- Once the count reaches the digital input, Y goes high, setting the RS latch. The latch output then disables the ÷2 stages

[B. Razavi, RF Microelectronics]

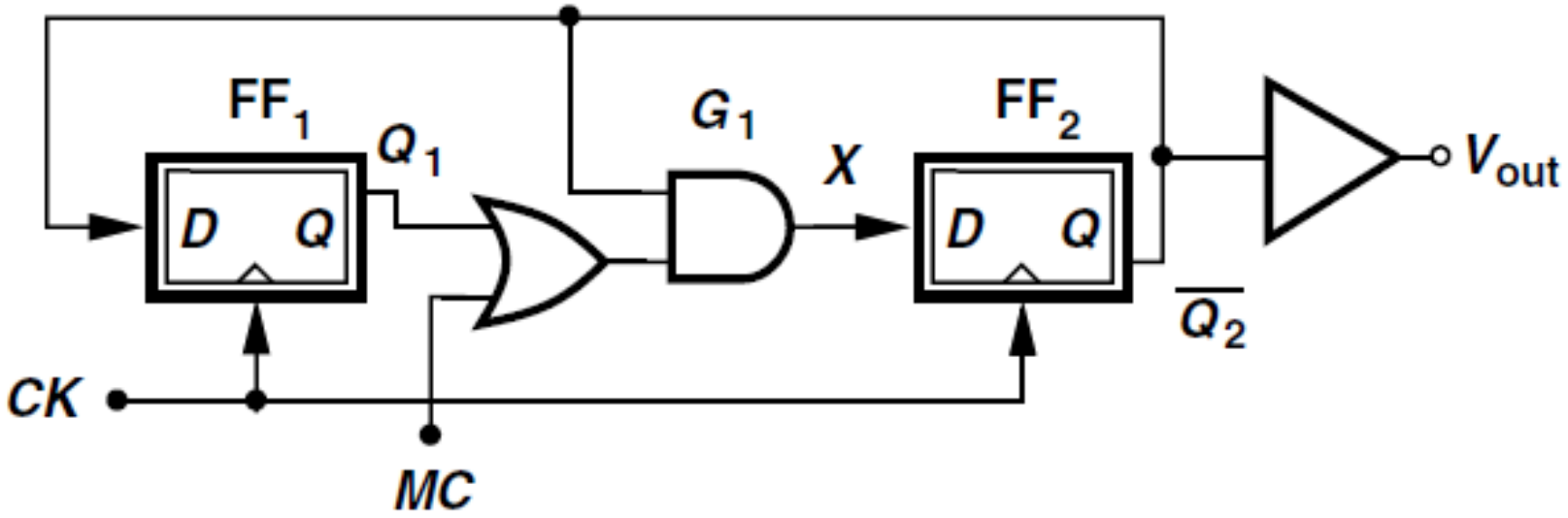
Divide-by-3 Circuit

- Note that a ÷2 circuit can be realized as a D-flipflop placed in a negative feedback loop
- A ÷3 circuit, on the other hand, requires two flipflops



[B. Razavi, RF Microelectronics]

Divide-by-2/3 Circuit

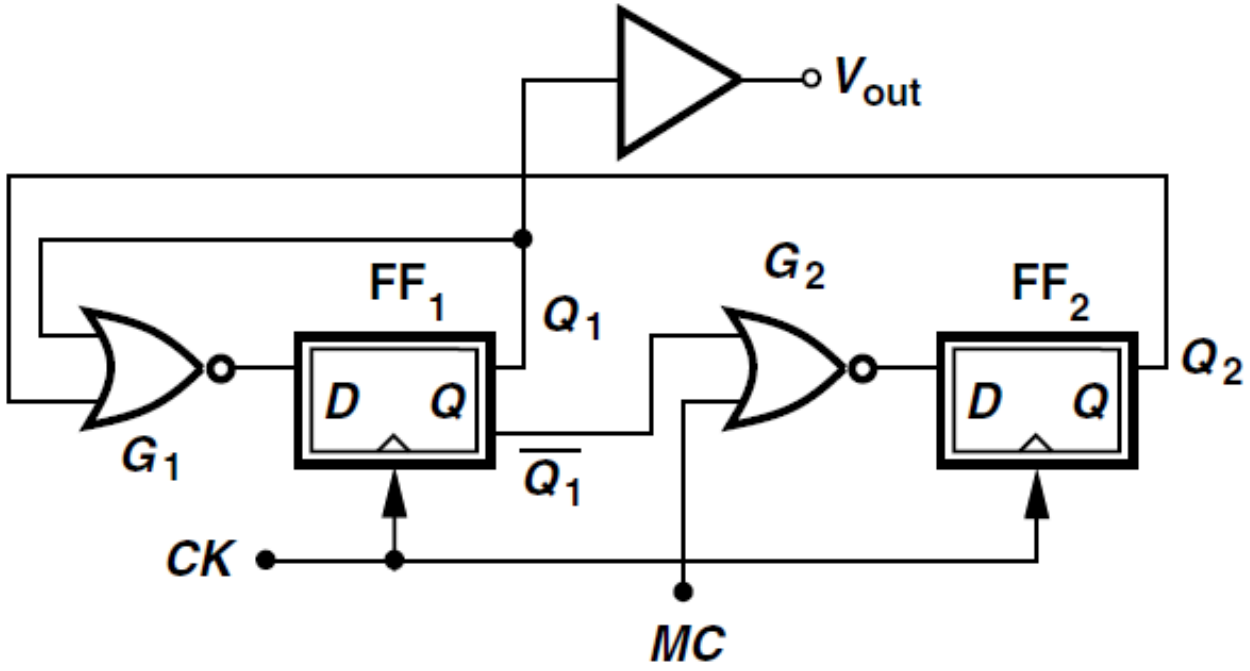


- The ÷2/3 circuit employs an OR gate to permit ÷3 operation if the modulus control MC=0 or ÷2 operation if MC=1
- In the MC=1 case, only FF2 divides the clock by 2 while FF1 plays no role

[B. Razavi, RF Microelectronics]

Divide-by-2/3 Circuit

- It is possible to rearrange the ÷2/3 stage so as to reduce the loading on the second flipflop
- The delay between the two FFs is also reduced

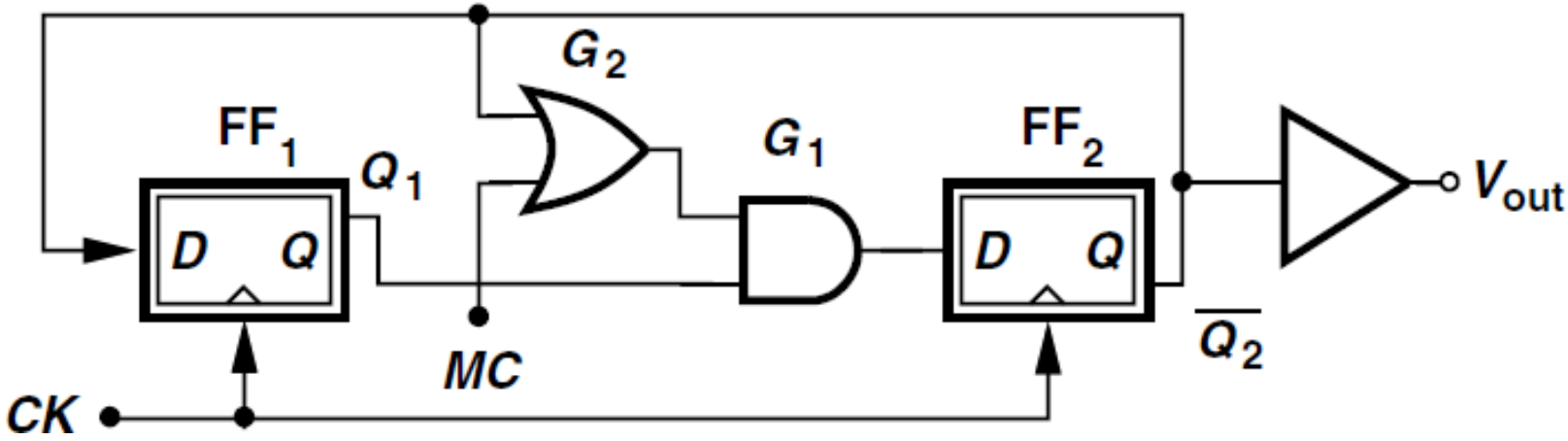


- This circuit has a 40% speed advantage over the previous one

[B. Razavi, RF Microelectronics]

Divide-by-3/4 Circuit

- It is possible to rearrange the ÷2/3 stage so as to reduce the loading on the second flipflop

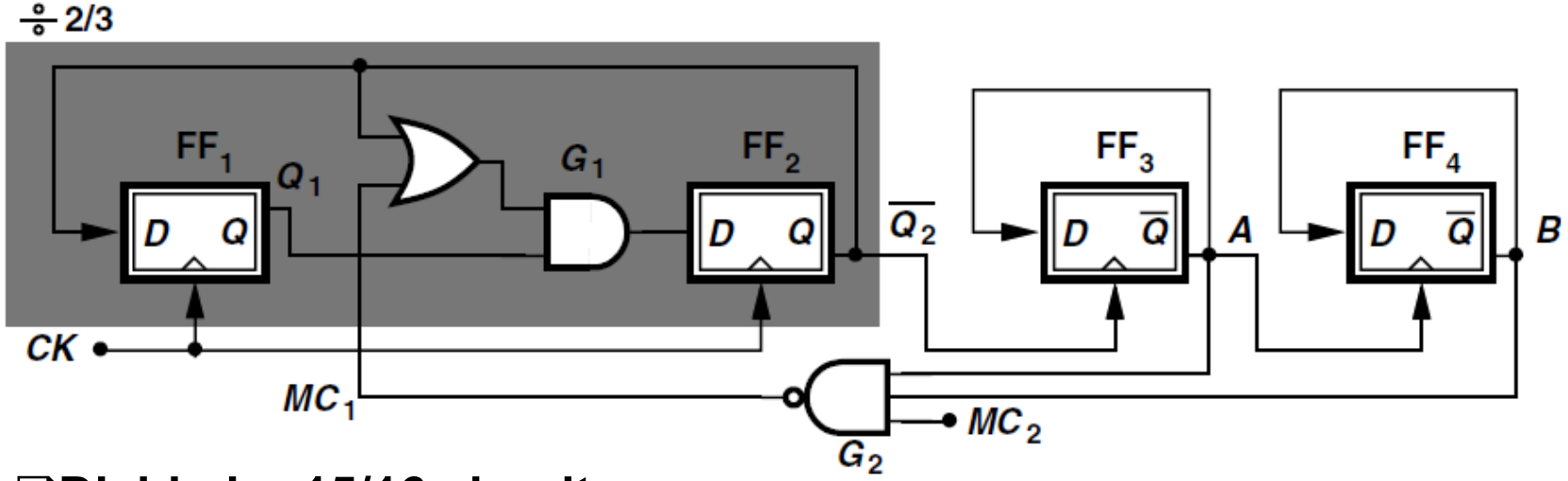


- The critical path (around FF2) contains a greater delay in this circuit than in the ÷3 stage

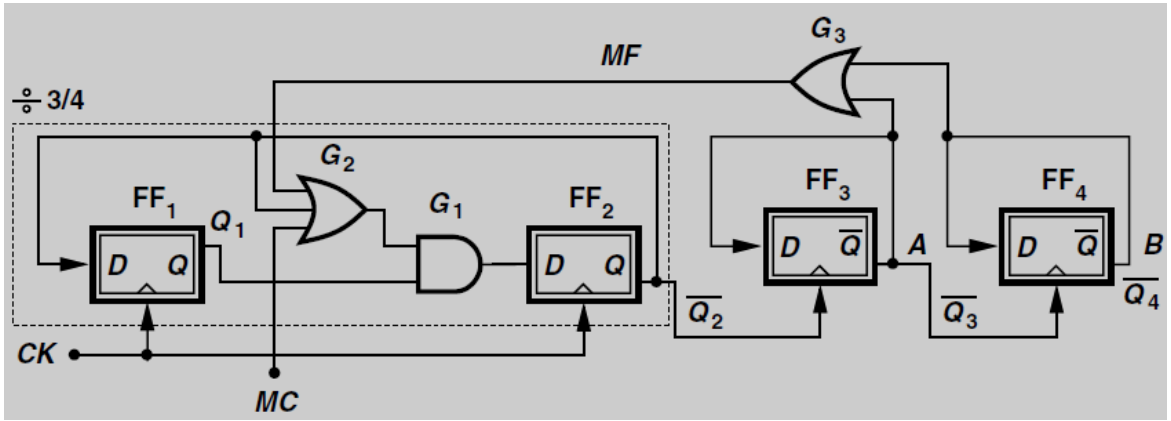
[B. Razavi, RF Microelectronics]

Other Dividers

❑Divide-by-8/9 circuit:



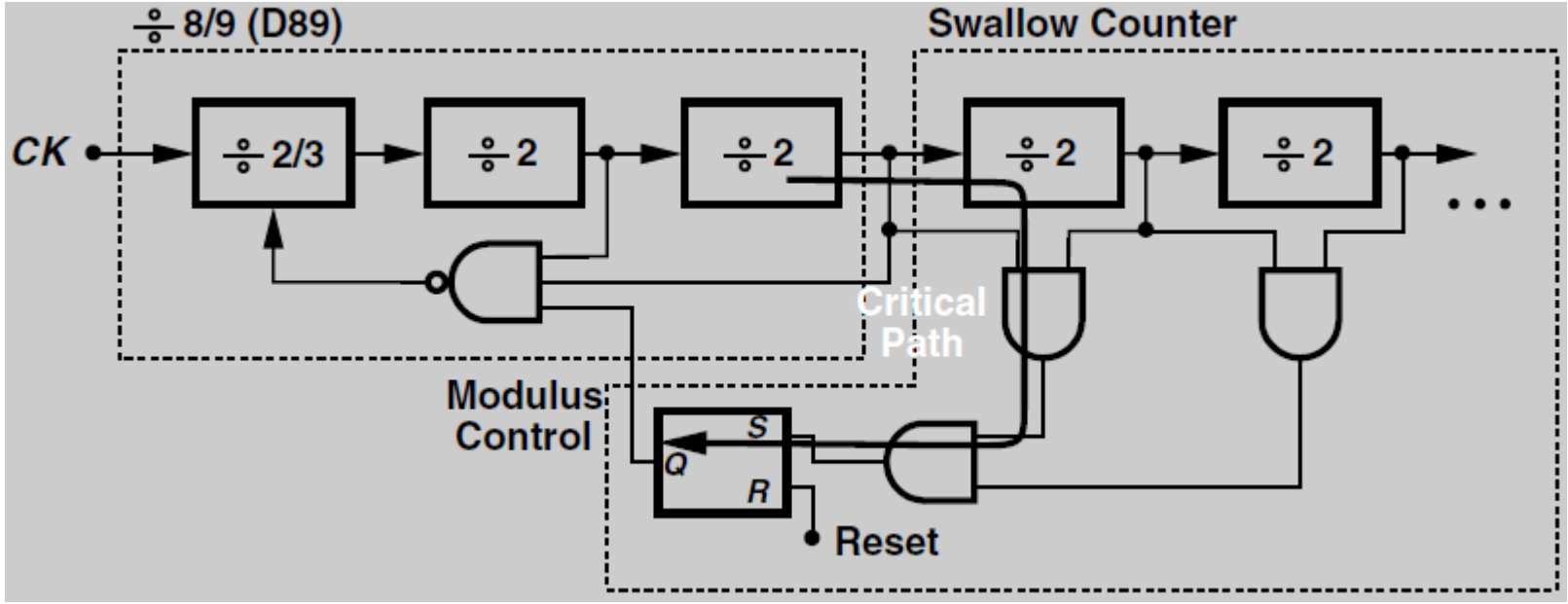
❑Divide-by-15/16 circuit:



[B. Razavi, RF Microelectronics]

Critical Path

- As the prescaler operates at a high frequency, the delay of critical path should be considered

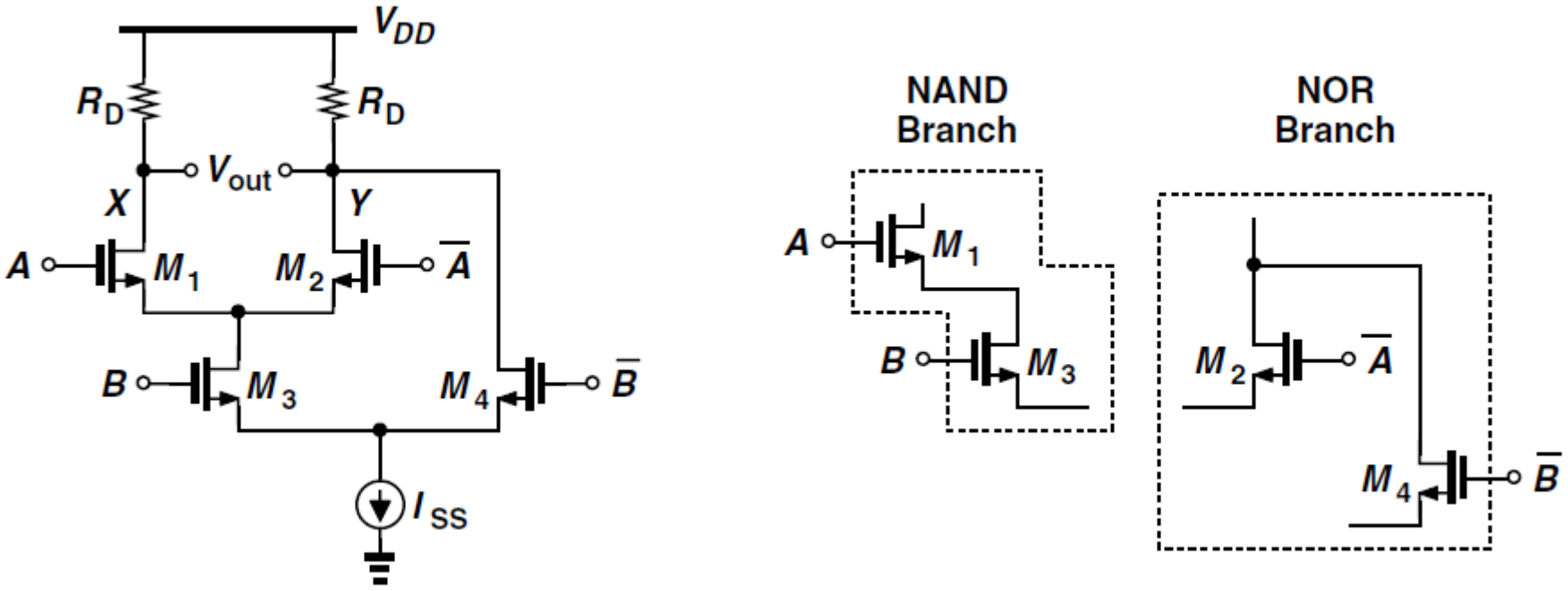


- Nowadays, the digital design tools can help to analyze the delay issue of critical path (Slack>0)

[B. Razavi, RF Microelectronics]

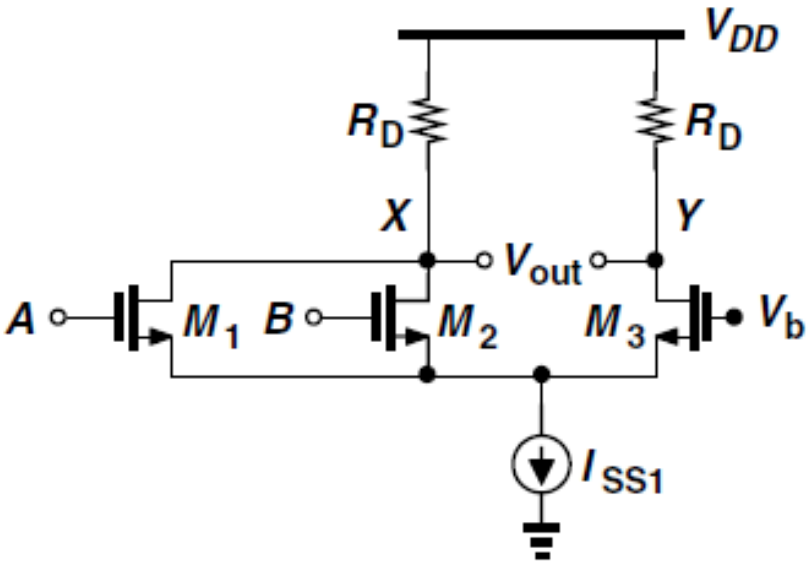
Current Mode Logic (CML)

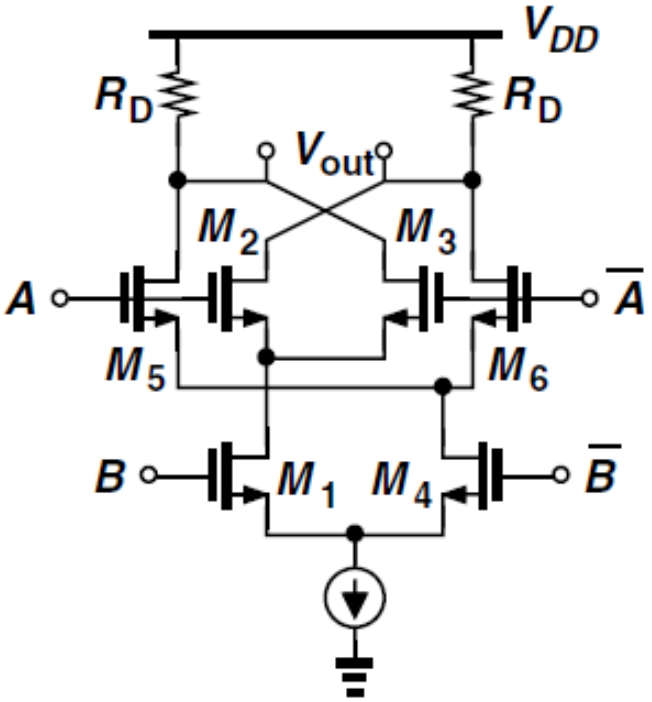
- CML derives its speed from the property that a differential pair can be rapidly enabled and disabled through its tail current source



[B. Razavi, RF Microelectronics]

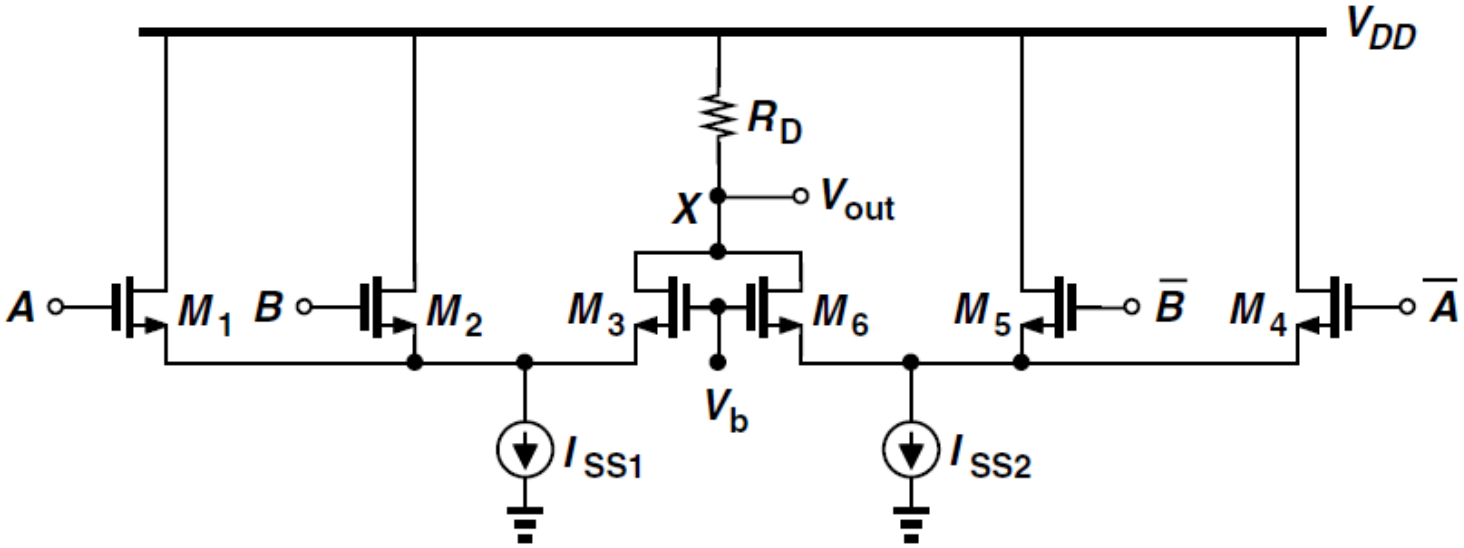
CML NOR & XOR





[B. Razavi, RF Microelectronics]

Low-Voltage XOR



- The XOR gate can avoid stacking to realize low-voltage operation $I_{D3} = \overline{A + B}$ $I_{D6} = \overline{\overline{A} + \overline{B}}$
- The summation of I_{D3} and I_{D6} at node X is equivalent to an OR operation, and the flow of the sum through R_D produces an inversion.

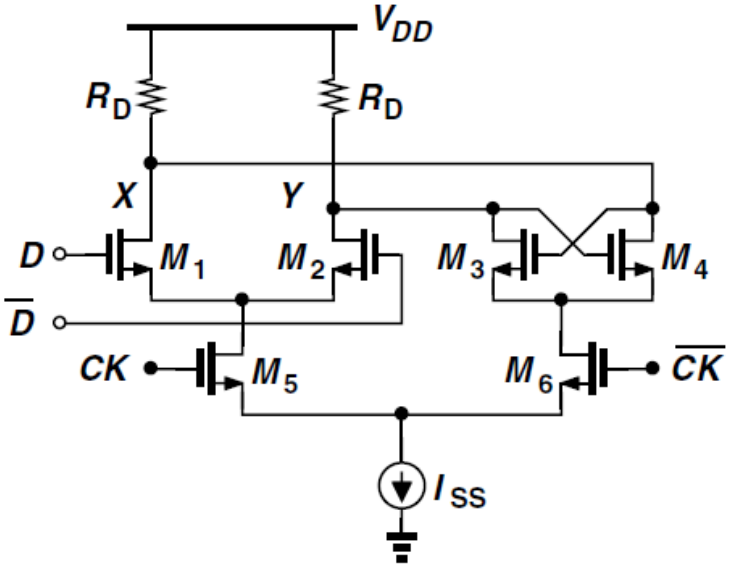
$$V_{out} = \overline{(\overline{A + B} + \overline{\overline{A} + \overline{B}})}$$
$$= \overline{A}B + A\overline{B}$$

[B. Razavi, RF Microelectronics]

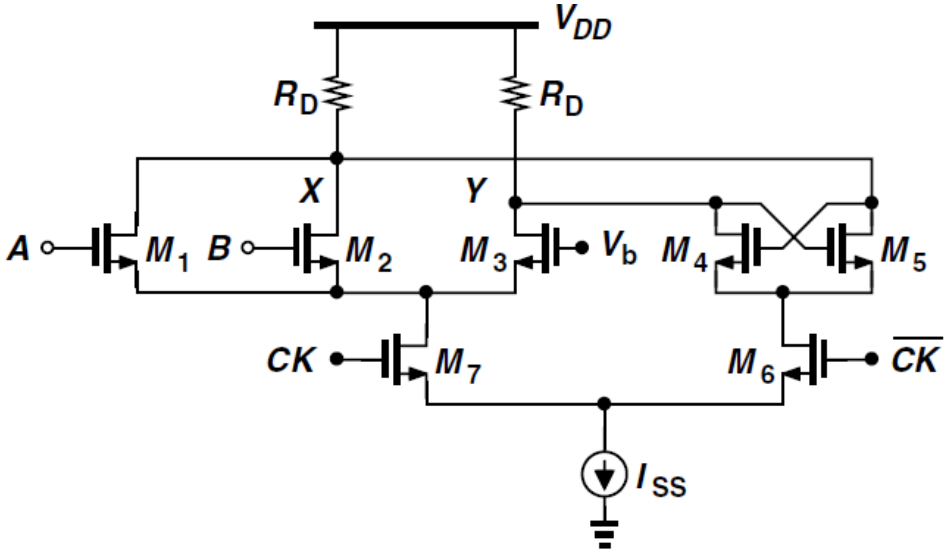
CML Latch

- The speed advantage of CML circuits is especially pronounced in latches

CML Latch



NOR Gate

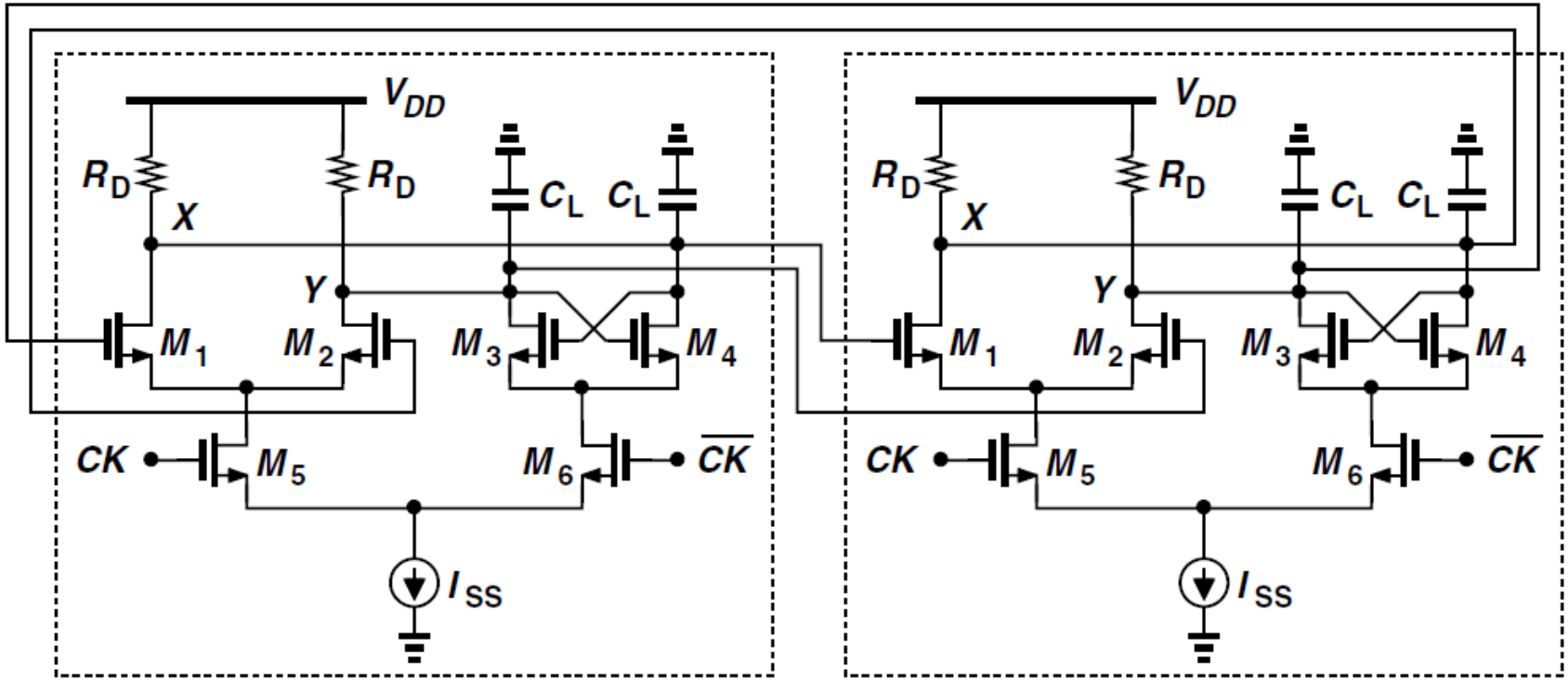


- In the latch mode, the positive feedback of regeneration pair M_3 and M_4 amplifies the difference between V_X and V_Y

[B. Razavi, RF Microelectronics]

CML Divide-by-2 Circuit

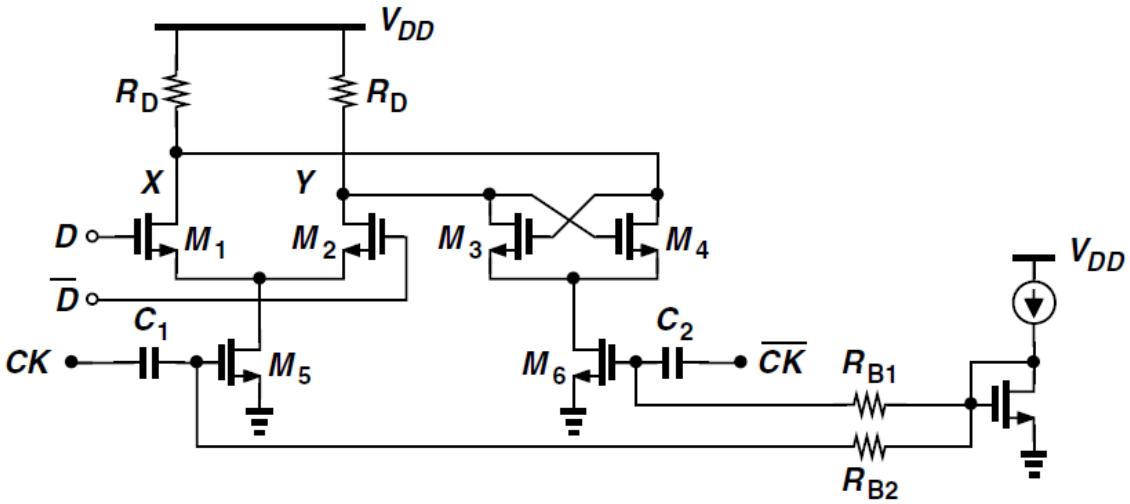
- A ÷2 circuit can be constructed by placing two D latches in a negative feedback loop



[B. Razavi, RF Microelectronics]

Class-AB Latch

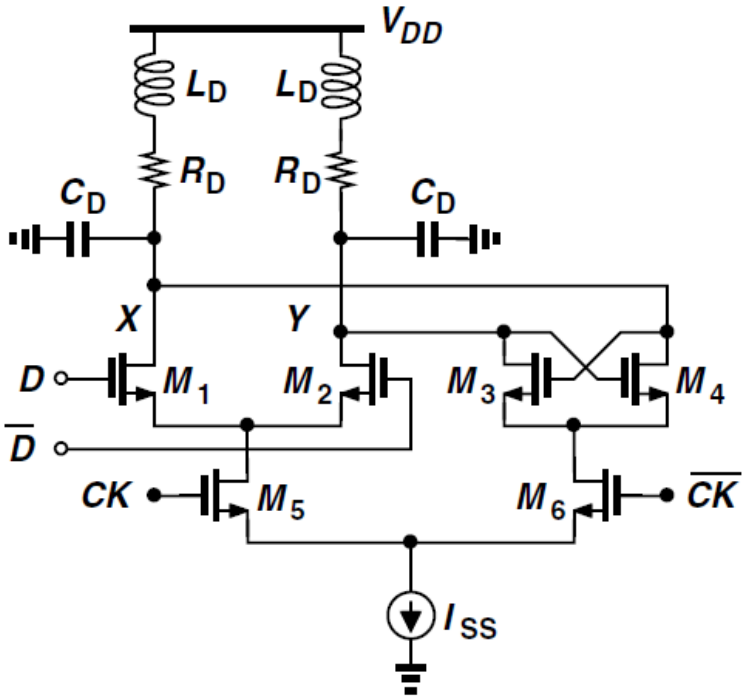
- With low supply voltage, the tail current can be removed

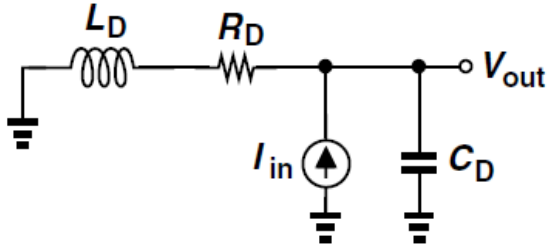


- The bias of the clocked pair is defined by a current mirror and the clock is coupled capacitively
- Large clock swings allow transistors M_5 and M_6 to operate in the class AB mode, i.e., their peak currents well exceed their bias current. This attribute improves the speed of the divider

[B. Razavi, RF Microelectronics]

Inductive Peaking





❑From a small-signal perspective, we observe that the inductors rise in impedance at higher frequencies, allowing more of the currents produced by the transistors to flow through the capacitors and hence generate a larger output voltage.

[B. Razavi, RF Microelectronics]