Low-Noise Amplifiers (2/2)

ZHAO BO

Institute of VLSI Design

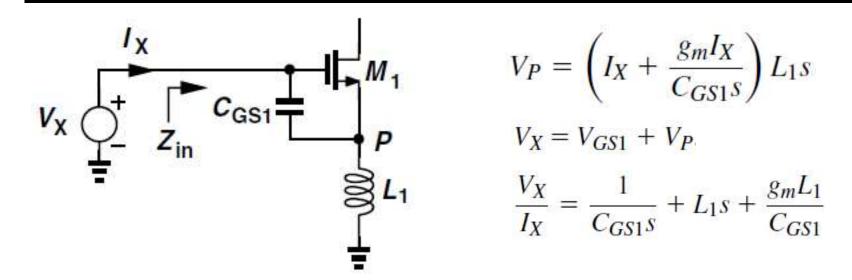
Zhejiang University

Email: zhaobo@zju.edu.cn

Web: person.zju.edu.cn/zhaobo



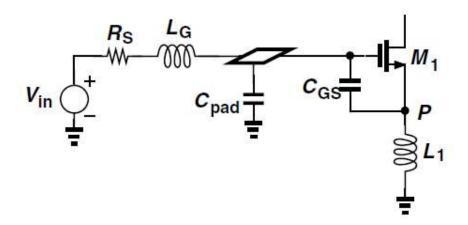
Inductive-Degeneration LNA



- □ The input impedance contains a frequency-independent real part given by $g_m L_1/C_{GS1}$. Thus, the third term can be chosen equal to 500hm.
- □In 65-nm technology, $ω_T ≈ 2π x$ (160 GHz), dictating $L_1 ≈ 50$ pH for 50 Ohm input. But even a bonding wire is higher than 50pH!

Inductive-Degeneration LNA

 \square At operation frequencies far below f_T of the transistor, we can reduce the f_T . This is accomplished by increasing the channel length or simply placing an explicit capacitor in parallel with C_{GS} . \square Another inductor must be placed in series with the gate, where it is assumed L_G is off-chip.



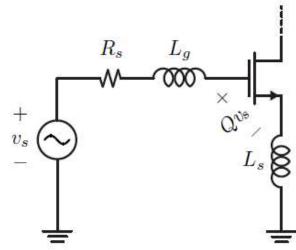
Q Boosting

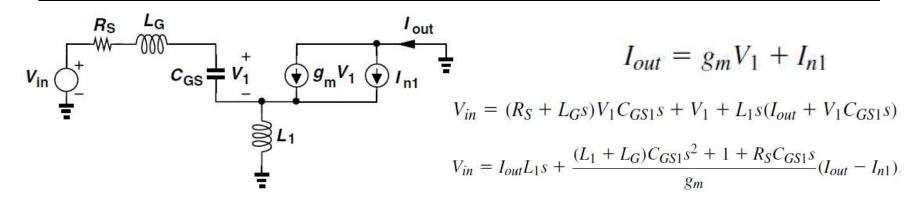
- □Recall that in a resonant circuit, the voltage across the reactive elements is Q times larger than the voltage across the resistor.
- \Box At resonance, the voltage across the resistors is simply V_S, so we have $v_{qs} = Q imes v_s$

$$i_d = g_m v_{gs} = Q \times g_m v_s = G_m v_s$$

$$Q = \frac{1}{\omega_0 C_{gs} 2R_s}$$

$$G_m = Qg_m = \frac{g_m}{\omega_0 C_{gs} 2R_s} = \left(\frac{\omega_T}{\omega_0}\right) \frac{1}{2R_s}$$





 \Box The input network is designed to resonate at the frequency ω_0

$$(L_1 + L_G)C_{GS1}s^2 + 1 = 0$$
 at $s = j\omega_0$

$$V_{in} = I_{out} \left(jL_1 \omega_0 + \frac{jR_S C_{GS1} \omega_0}{g_m} \right) - I_{n1} \frac{jR_S C_{GS1} \omega_0}{g_m} \qquad |\frac{I_{out}}{V_{in}}| = \frac{1}{\omega_0 \left(L_1 + \frac{R_S C_{GS1}}{g_m} \right)}$$

$$\square \text{For input matching: } g_m L_1 / C_{GS1} = R_S \qquad |\frac{I_{out}}{V_{in}}| = \frac{\omega_T}{2\omega_0} \cdot \frac{1}{R_S}$$

$$\left|\frac{I_{out}}{V_{in}}\right| = \frac{\omega_T}{2\omega_0} \cdot \frac{1}{R_S}$$

□Interestingly, the transconductance of the circuit remains independent of L_1 , L_G , and g_m so long as the input is matched.

 \square Setting V_{in} to zero, we compute the output noise due to M_1 :

$$|I_{n,out}|_{M1} = |I_{n1}| \frac{R_S C_{GS1}}{g_m L_1 + R_S C_{GS1}}$$

 \square which, for $g_mL_1/C_{GS}=R_S$, reduces to

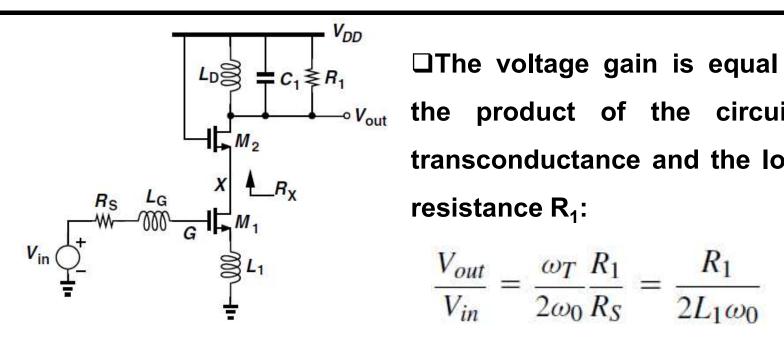
$$|I_{n,out}|_{M1} = \frac{|I_{n1}|}{2} \qquad \overline{I_{n,out}^2}|_{M1} = kT\gamma g_m$$

□Dividing the output noise current by the transconductance of the circuit and by 4kTR_s and adding unity to the result, we arrive at the noise figure:

NF = 1 +
$$\frac{\overline{V_{n,in}^2}}{4kTR_S}$$
 = 1 + $g_m R_S \gamma \left(\frac{\omega_0}{\omega_T}\right)^2$

NF = 1 +
$$g_m R_{SY} \left(\frac{\omega_0}{\omega_T}\right)^2$$
 $g_m = \frac{dI_{DS}}{dV_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)(1 + \lambda V_{DS})$

- \square If the voltage V_{GS} is kept constant and transistor width is scaled down proportionally, then g_m and C_{GS1} decrease while g_m/C_{GS1} =ω_T remains constant.
- □The noise figure decreases while the power dissipation of the circuit also decreases! NF=1 dB (0 value) with an ultra-small W!
- □As C_{GS} approaches zero and L_{G} infinity, the Q of the input network ($\approx L_{G}\omega_{0}/R_{S}$) also goes to infinity, providing an infinite voltage gain
- □In practice, of course, the inductor suffers from a finite Q.



☐ The voltage gain is equal to the product of the circuit's transconductance and the load

$$\frac{V_{out}}{V_{in}} = \frac{\omega_T}{2\omega_0} \frac{R_1}{R_S} = \frac{R_1}{2L_1\omega_0}$$

□Dividing the noise of R₁ by the gain and the noise of R_s and $g_m L_1/C_{GS1} = R_S$ adding the result to the noise figure:

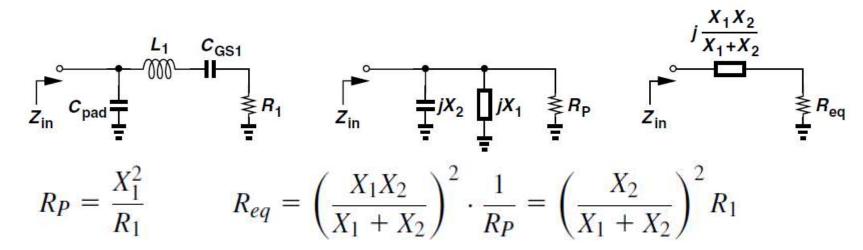
NF = 1 +
$$g_m R_S \gamma \left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{4R_S}{R_1} \left(\frac{\omega_0}{\omega_T}\right)^2$$

Effect of PAD capacitance

 $\Box C_{GS1}$, L₁, and R₁ represent the three terms $\frac{1}{C_{GS1}S} + L_{1}S + \frac{g_m L_1}{C_{GS1}}$

$$\frac{1}{C_{GS1}s} + L_1s + \frac{g_m L_1}{C_{GS1}}$$

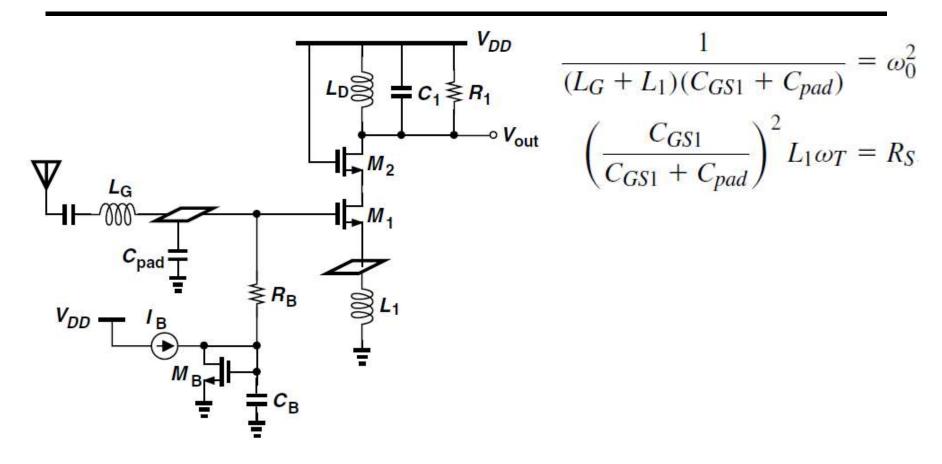
□Denoting the jL₁ω-j/(C_{GS1}ω) by jX₁ and -j/(C_{pad}ω) by jX₂



□In most cases, we can assume $L_1\omega$ <<1/($C_{GS1}\omega$)+1/($C_{Dad}\omega$)

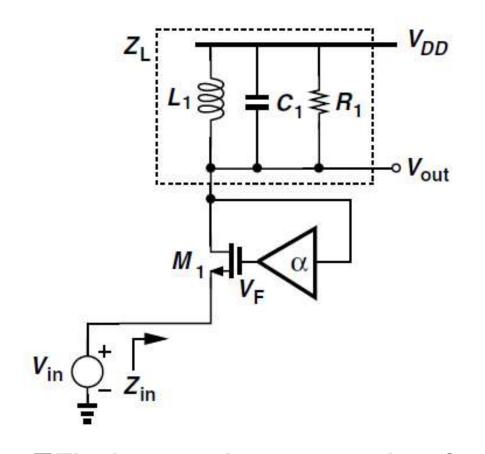
$$R_{eq} pprox \left(\frac{C_{GS1}}{C_{GS1} + C_{pad}}\right)^2 R_1$$

Effect of PAD capacitance



□Parasitic capacitance and bond-wire inductance should be considered in the designs.

CG LNA with Feedback



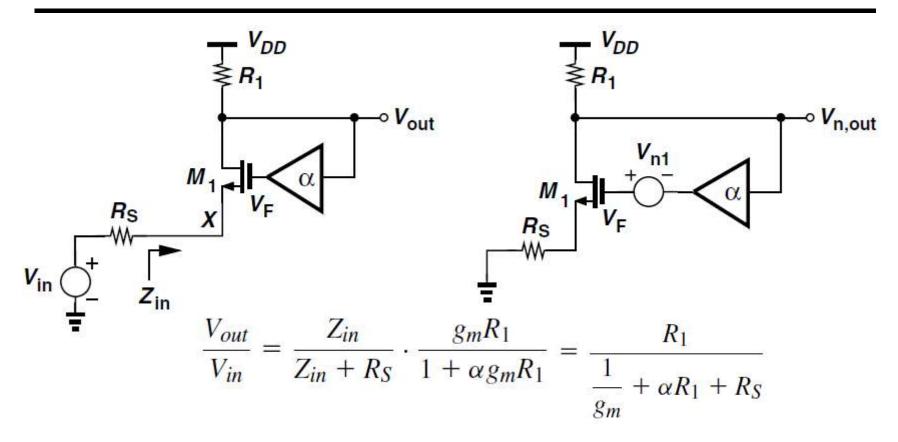
$$Z_{in} = \frac{1}{g_m} + \alpha Z_L$$

□At resonance:

$$Z_{in} = \frac{1}{g_m} + \alpha R_1$$

 \Box The input resistance can therefore be substantially higher than $1/g_m$.

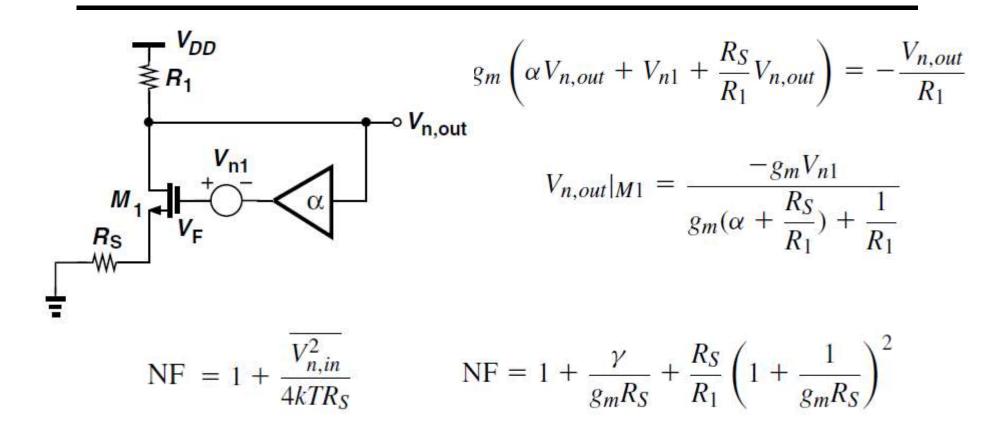
CG LNA with Feedback



\Box At input matching ($Z_{in}=R_s$):

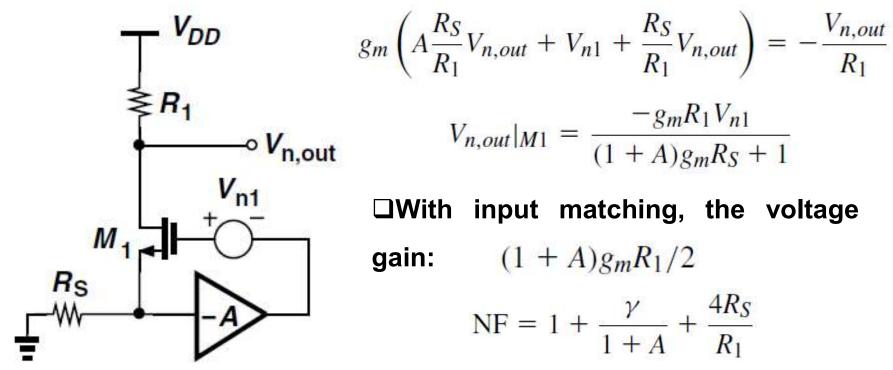
$$\frac{V_{out}}{V_{in}} = R_1/(2R_S)$$

CG LNA with Feedback



 \Box The NF can be lowered by raising g_m. For example, if g_mR_S=4 and γ=1, then the first two terms yield a noise figure of 0.97 dB.

CG LNA with Feedforward

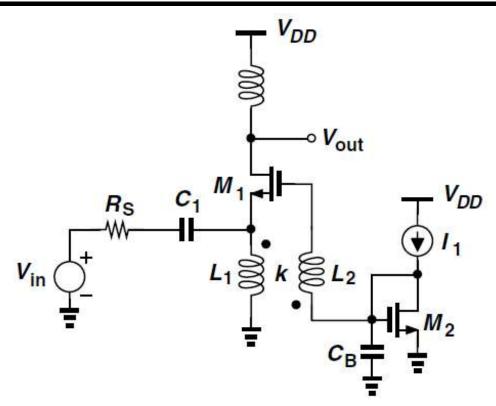


□The above analysis has neglected the noise of the gain stage A.

The input-referred noise leads to an overall noise figure equal to

$$NF = 1 + \frac{\gamma}{1+A} + \frac{4R_S}{R_1} + \frac{A^2}{(1+A)^2} \frac{\overline{V_{nA}^2}}{4kTR_S}$$
[B. Razavi, RF Microelectronics]

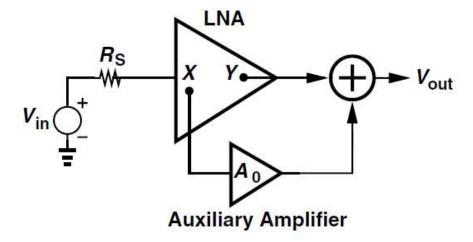
CG LNA with Feedforward



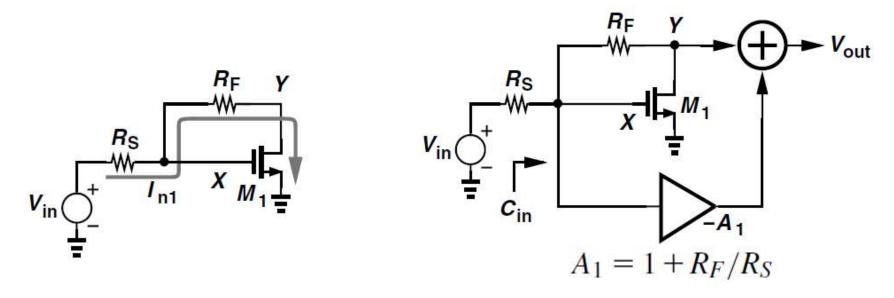
□It is possible to obtain the voltage gain through the use of an on-chip transformer

□The direction of the currents is chosen so as to yield a negative sign. However, on-chip transformer geometries make it difficult to achieve a voltage gain higher than roughly 3

 \Box Three noise terms: a value of unity arising from the noise of R_s itself, a term representing the contribution of the input transistor, and another related to the noise of the load resistor



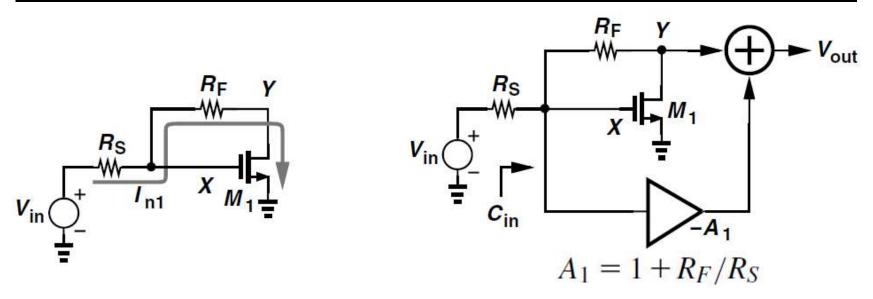
□The signal appears with opposite polarities but the noise of the input transistor appears with the same polarity.



- $\Box \text{Original Gain: } V_Y/V_X = 1 g_m R_F = 1 R_F/R_S$
- **□**Additional Gain:

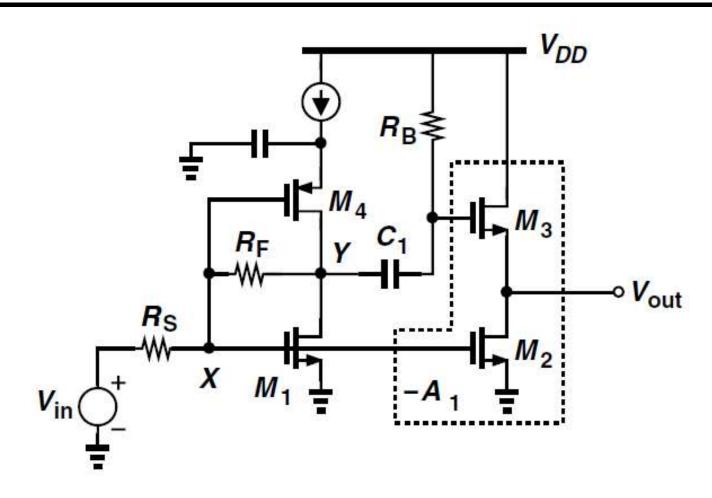
$$\frac{V_{out}}{V_X} = 1 - \frac{R_F}{R_S} - \left(1 + \frac{R_F}{R_S}\right) = -\frac{2R_F}{R_S}$$

 \Box If the input is matched. The gain V_{out}/V_{in} is half of this value.

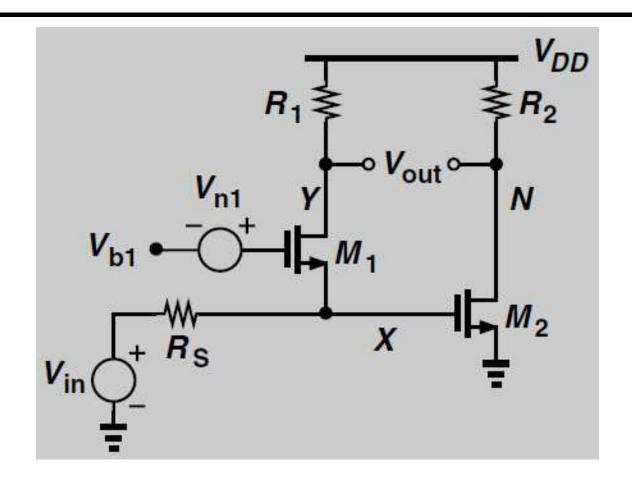


 \square The auxiliary amplifier exhibits an input-referred noise voltage V_{nA1} and the noise voltage of R_F appears directly at the output as

4kTR_F NF =
$$1 + \frac{R_S}{R_F} + A_1^2 \overline{V_{nA1}^2} \frac{R_S}{4kTR_F^2}$$
 $A_1 = 1 + R_F/R_S$
NF = $1 + \frac{R_S}{R_F} + \frac{\overline{V_{nA1}^2}}{4kTR_S} \left(1 + \frac{R_S}{R_F}\right)^2$ NF can be minimized by maximizing R_F [B. Razavi, RF Microelectronics]

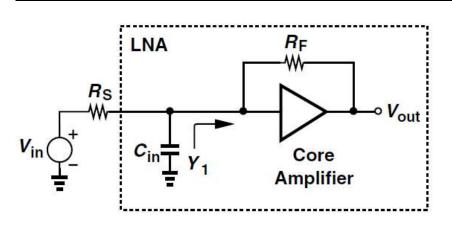


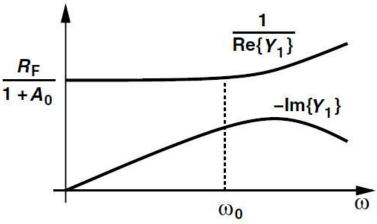
 $\square M_2$ and M_3 act as the $-A_1$ gain stage.



□The noise of M₁ can be cancelled at the differential output.

Reactance-Cancelling LNA





- \Box If the open-loop transfer function of the core amplifier is modeled by a one-pole response: $A_0/(1+s/\omega_0)$
- The input admittance: $Y_1(s) = \frac{s + (A_0 + 1)\omega_0}{R_F(s + \omega_0)}$

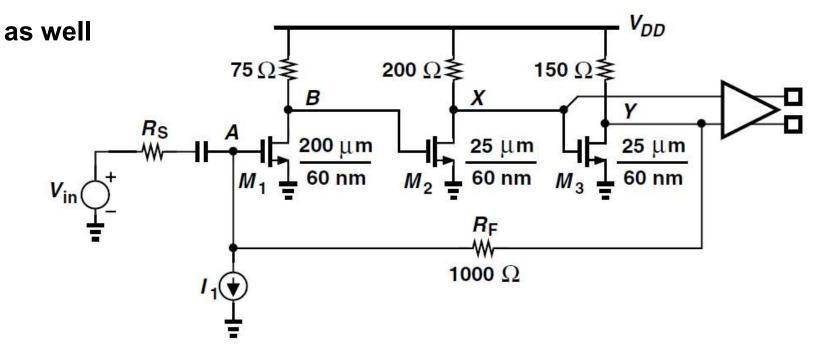
$$\frac{1}{Re\{Y_1\}} = \frac{R_F(\omega^2 + \omega_0^2)}{(1 + A_0)\omega_0^2} \qquad Im\{Y_1\} = \frac{-A_0\omega\omega_0}{R_F(\omega^2 + \omega_0^2)}$$

□The input matching afforded by the above technique holds for

frequencies up to about ω_0

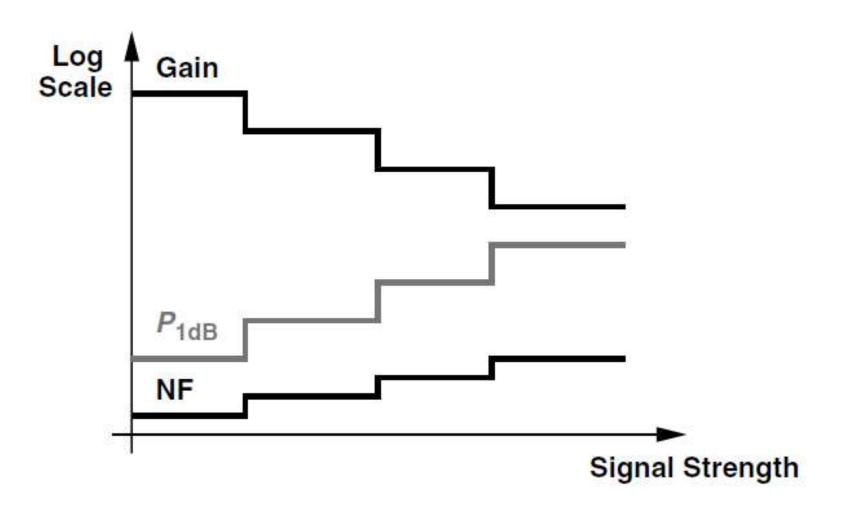
Reactance-Cancelling LNA

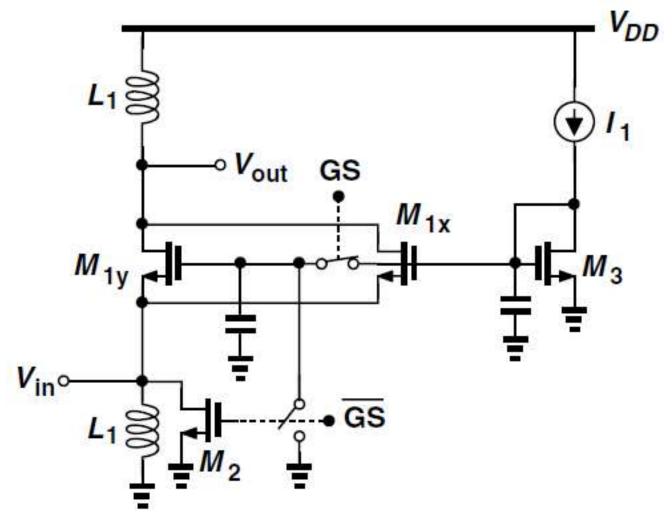
□A one-pole response applies to multistage implementations

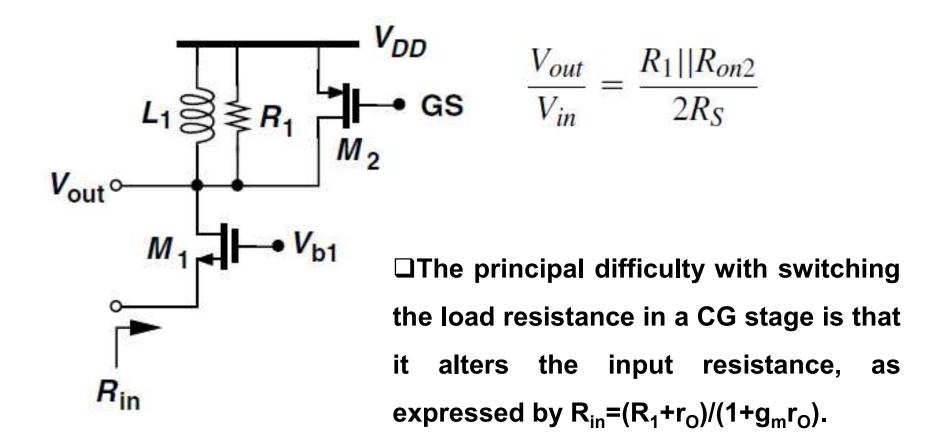


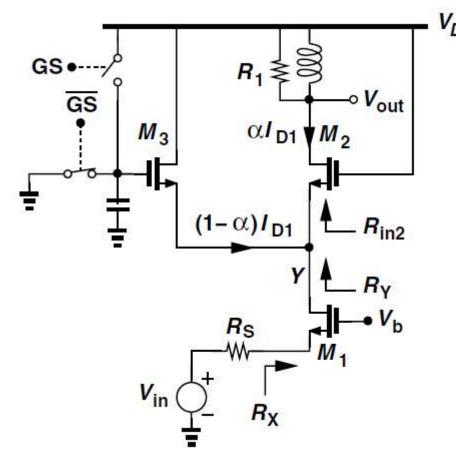
□The open-loop poles at nodes A, B, X, and Y lie at 10 GHz, 24.5 GHz, 22 GHz, and 75 GHz, respectively, collapse to an equivalent value of 9.9 GHz

- □The dynamic range of the signal sensed by a receiver may approach 100 dB.
- □Gain switching in an LNA must deal with several issues:
- √ (1) it must negligibly affect the input matching;
- √ (2) it must provide sufficiently small "gain steps";
- √ (3) The additional devices performing the gain switching must not degrade the speed of the original LNA;
- √ (4) For high input signal levels, gain switching must also make the LNA more linear so that this stage does not limit the receiver linearity.





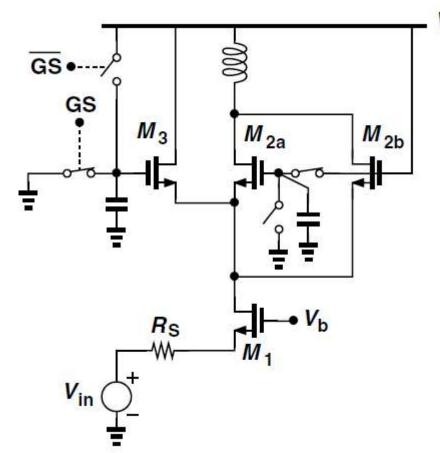




□The advantage of the above technique over the previous two is that the gain step depends only on W_3/W_2 (if M_2 and M₃ have equal lengths) and not the absolute value of the on-resistance of a MOS switch, which can be more accurate.

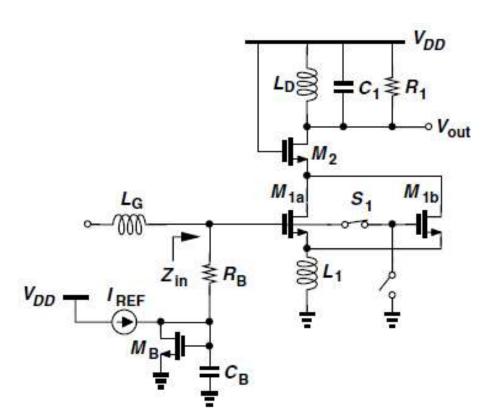
□ However, the capacitance introduced by M₃ at node Y degrades the performance at high frequencies.

| B. Razavi, RF Microelectronics|

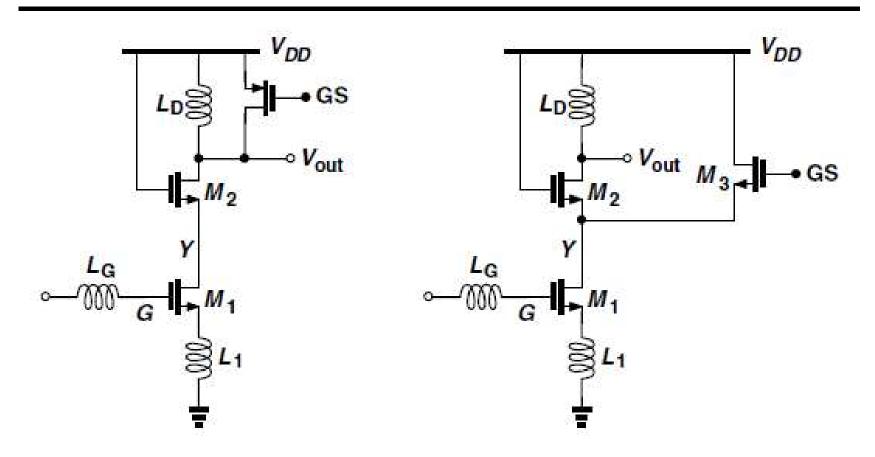


DD

□In order to reduce the capacitance contributed by the gain switching transistor, we can turn off part of the main cascode transistor so as to create a greater imbalance between the two.



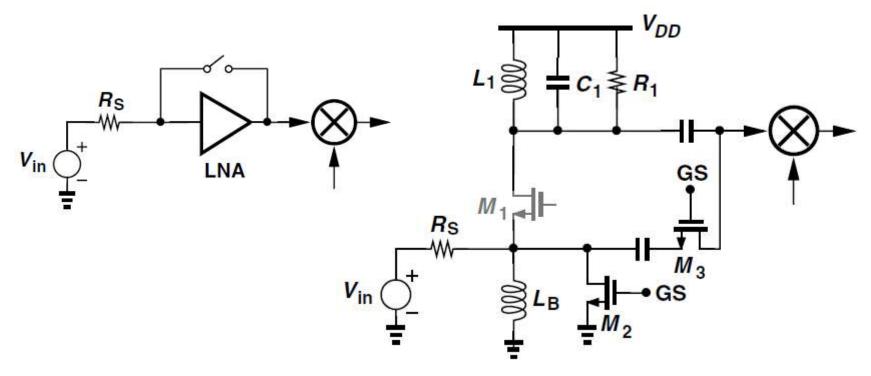
□Turning M_{1b} off does not alter ω_T because the current density remains constant. Thus, Re{Zin}=L_1\omega_T is relatively constant, but Im{Zin} changes, degrading the input match.



□Gain switching in cascode CS stage can be conducted by load switching and additional cascode device.

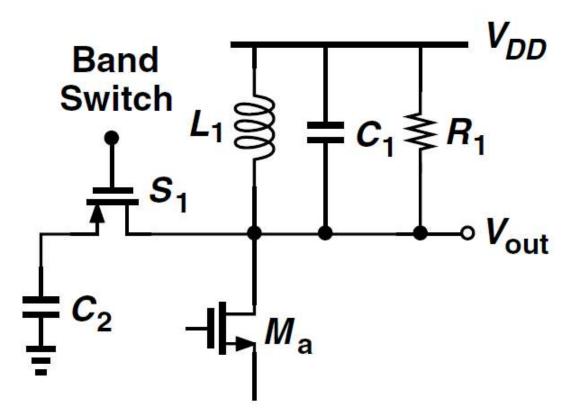
LNA By-Pass

□Receiver designs in which the LNA nonlinearity becomes problematic at high input levels can "bypass" the LNA in very-low-gain modes



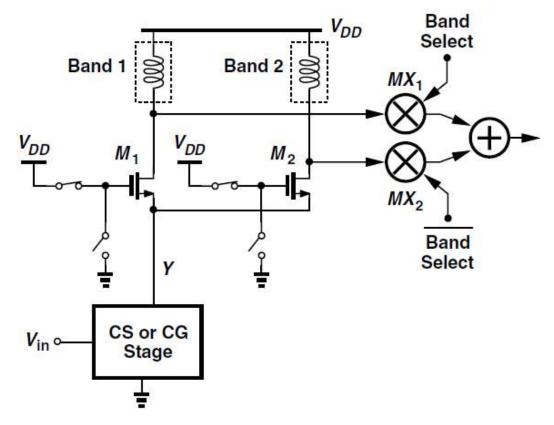
LNA Band Switching

□LNAs usually operate across a wide bandwidth or in different bands can incorporate band switching.

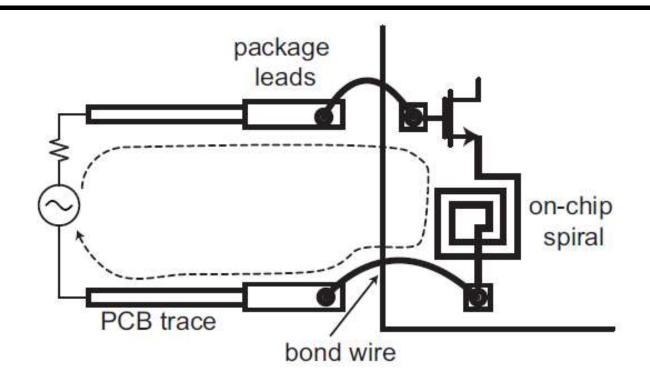


LNA Band Switching

□The LNA operation band can be switched by programmable cascode branches.



LNA Chip/Package/Board Interface

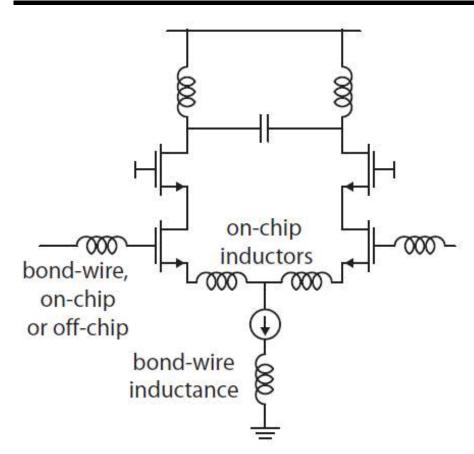


□Since the LNA needs to interface to the external world, its input network must transition from the Si chip to the package and board environment, which involves "macroscopic" structures such as bondwires and package leads.

Bond-Wire Inductance

□One reason inductive degeneration is popular is because we can use package parasitics to our benefit. Some or all of L_s can be absorbed into the loop inductance (or the partial inductance of the bondwire) ☐ These parasitics must be absorbed into the LNA design. □This requires a good model for the package and bondwires. It should be noted that the inductance of the input loop depends on the arrangement of the bondwires, and hence die size and pad locations. ☐ Many designs also require ESD protection, which manifests as increased capacitance on the pads.

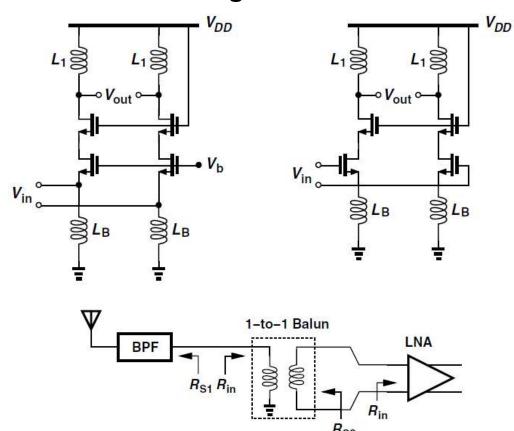
Differential LNA Design



- □One undesired consequence of the package is that the parasitic inductors vary from part to part and require careful modeling and extra care to correctly implement the LNA.
- □The advantage of a differential LNA is that the parasitics are only on the gate side, and not on the source of the transistors. The source inductors are realized with onchip inductors with tight process tolerances.

Differential LNAs

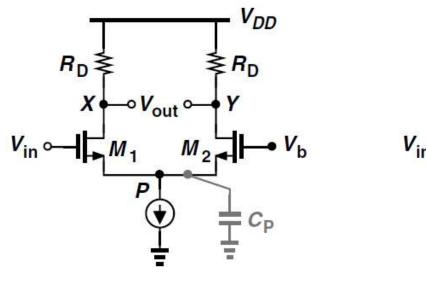
□The impact of even-order distortion can be reduced by differential designs.

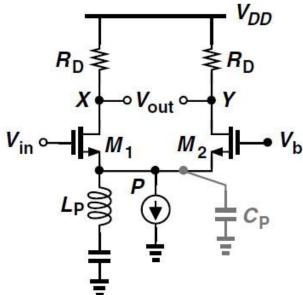


- □Whether the differential version of an LNA exhibits a higher or lower NF depends on the circuit topology.
- □External baluns have a loss as high as 0.5 dB, raising the NF by the same amount.

Single-to-Differential Converter

□As there is loss in a balun, let's consider the circuits:

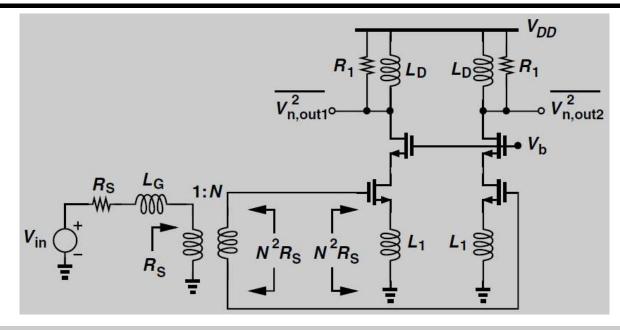




- \Box The parasitic capacitance at node P attenuates and delays the signal propagating from M₁ to M₂
- □The capacitance at P can be nulled through the use of a parallel inductor

 [B. Razavi, RF Microelectronics]

Baluns

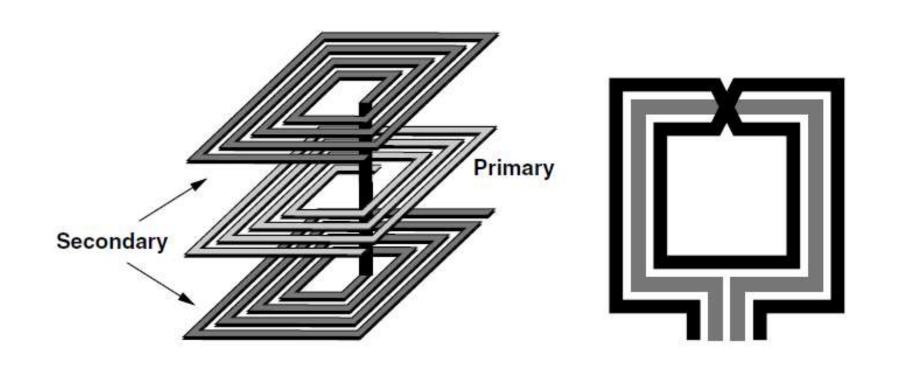


$$NF = N^2 \frac{\gamma}{2} g_{m1} R_S \left(\frac{\omega_0}{\omega_T}\right)^2 + 2N^2 \frac{R_S}{R_1} \left(\frac{\omega_0}{\omega_T}\right)^2 + 1$$

□ The first two terms have risen by a factor of N^2 ! This is because the condition $L_1ω_T=N^2R_S/2$ inevitably leads to an N^2 -fold reduction in the transconductance of the circuit.

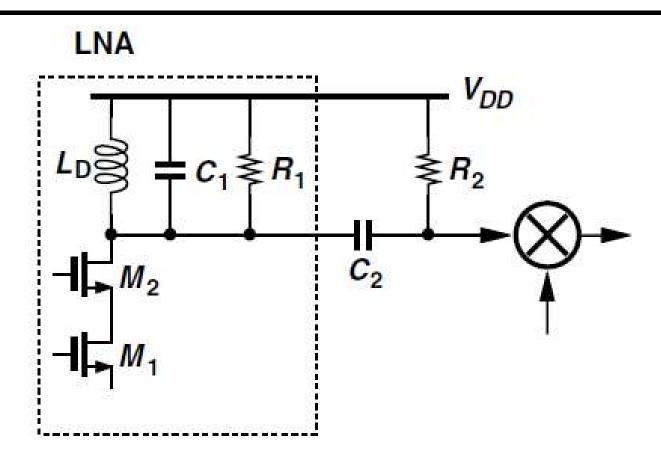
[B. Razavi, RF Microelectronics]

Baluns



□Baluns can be realized by stacked spirals or embedded spirals.

IP2 Improvement



□low-frequency beat can be removed by a high-pass filter.