Frequency Synthesizers (2/2)

ZHAO BO

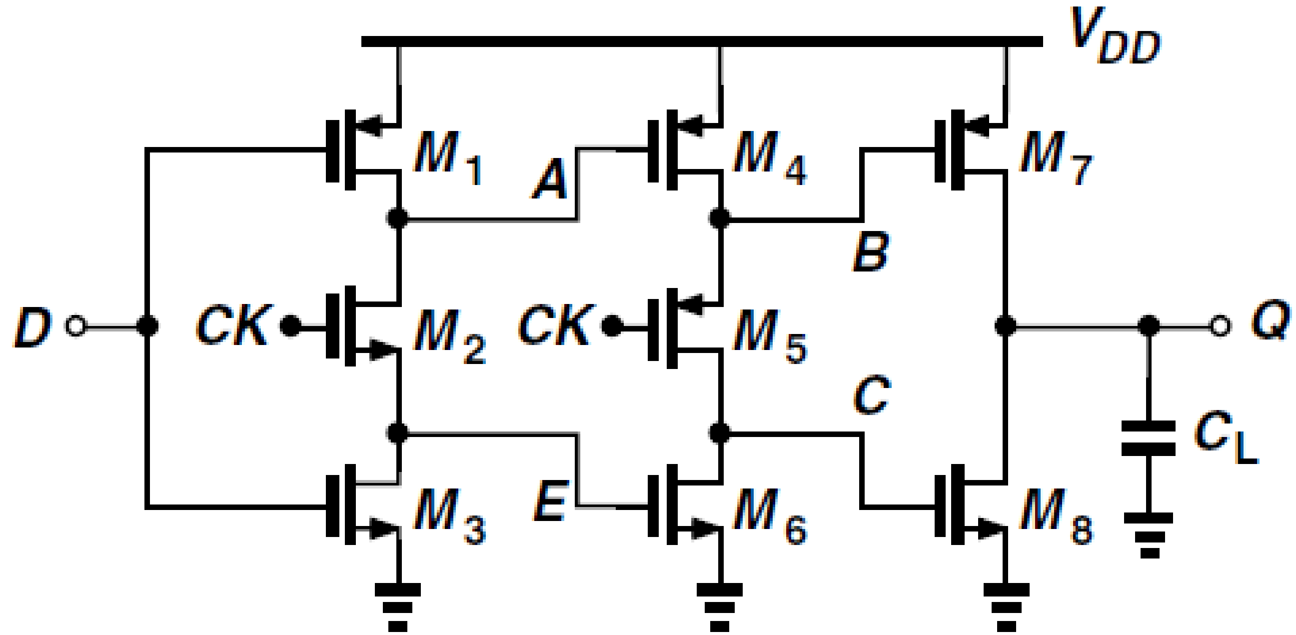
Institute of VLSI Design

Zhejiang University

Email: zhaobo@zju.edu.cn

Web： person.zju.edu.cn/zhaobo

TSPC



❑In comparison to CML, TSPC is a kind of dynamic logic

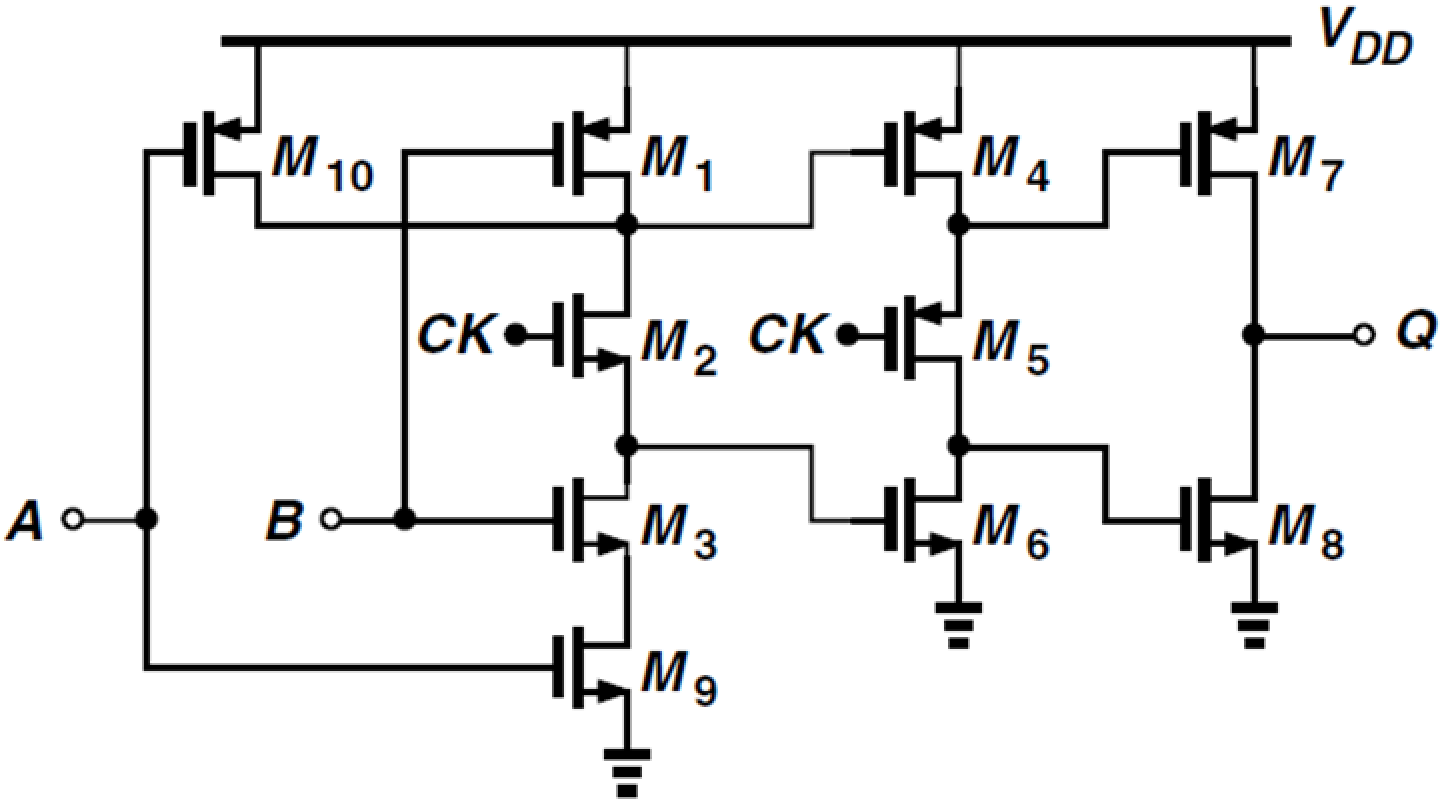
❑TSPC achieves relatively high speeds with low power dissipation (no static power)

❑TSPC divider fails at very low clock frequencies due to the leakage of the transistors

[B. Razavi, RF Microelectronics]

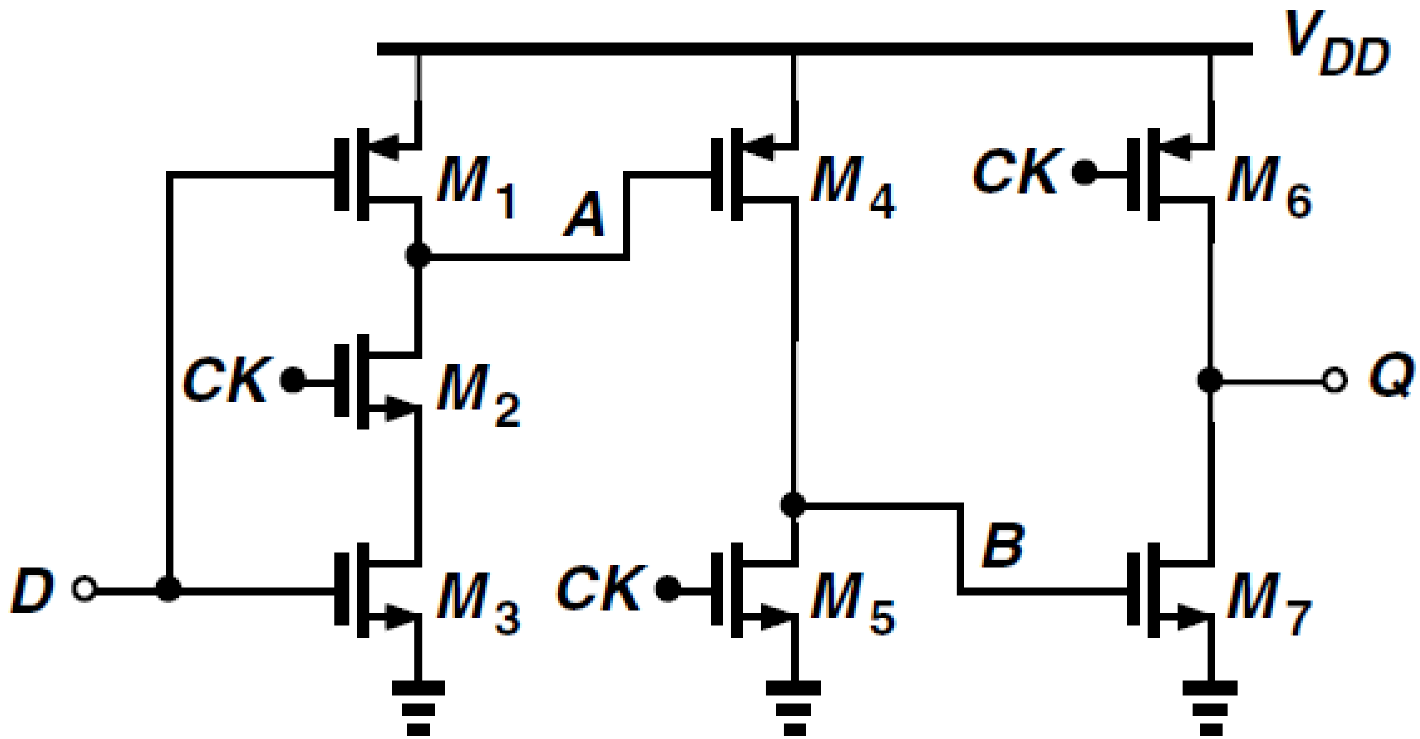
TSPC Logic

❑**The TSPC FF can readily incorporate logic at its input. For example, a NAND gate can be merged with the master latch**



[B. Razavi, RF Microelectronics]

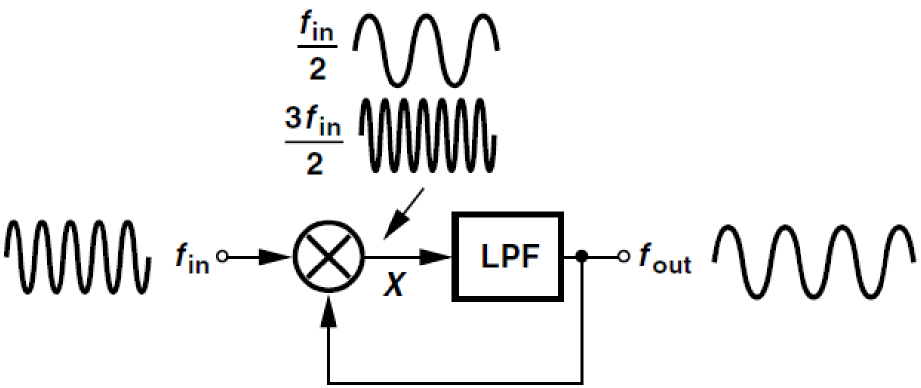
TSPC Ratioed Logic

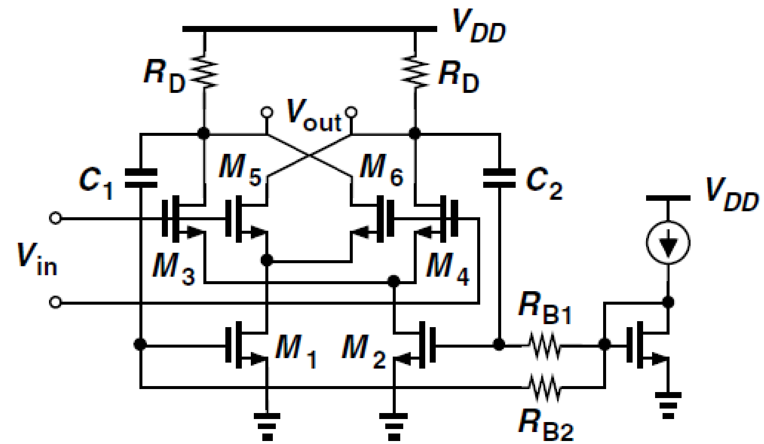


❑The slave latch is designed as “ratioed” logic, i.e., both NMOS devices are strong enough to pull down B and Q even if M_4 or M_6 is on.

[B. Razavi, RF Microelectronics]

Miller Divider

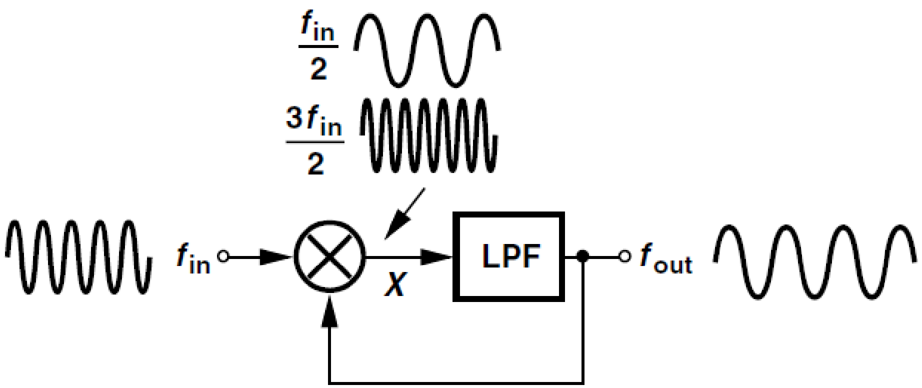


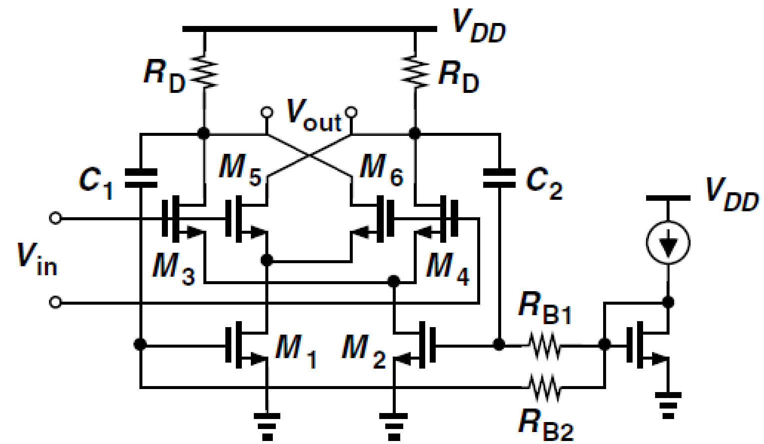


- If the circuit operates properly, $f_{out}=f_{in}/2$, yielding two components, $3f_{in}/2$ and $f_{in}/2$, at node X. The former is attenuated by the LPF, and the latter circulates around the loop
- Correct operation requires that the loop gain for $3f_{in}/2$ be sufficiently small and that for the latter exceed unity

[B. Razavi, RF Microelectronics]

Miller Divider

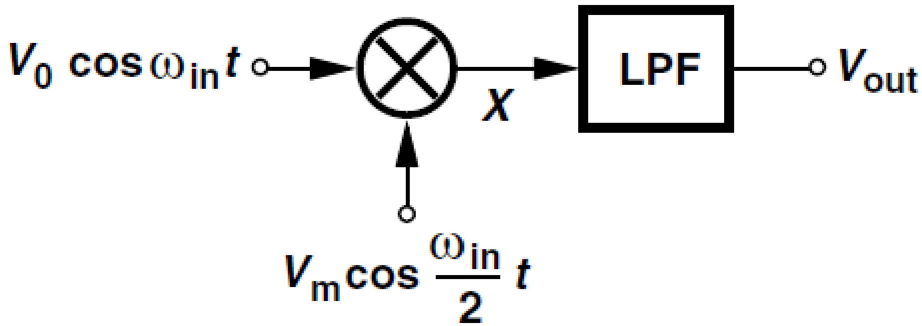


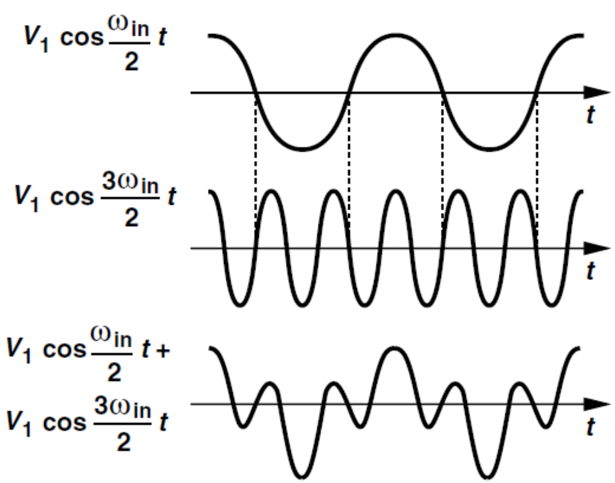


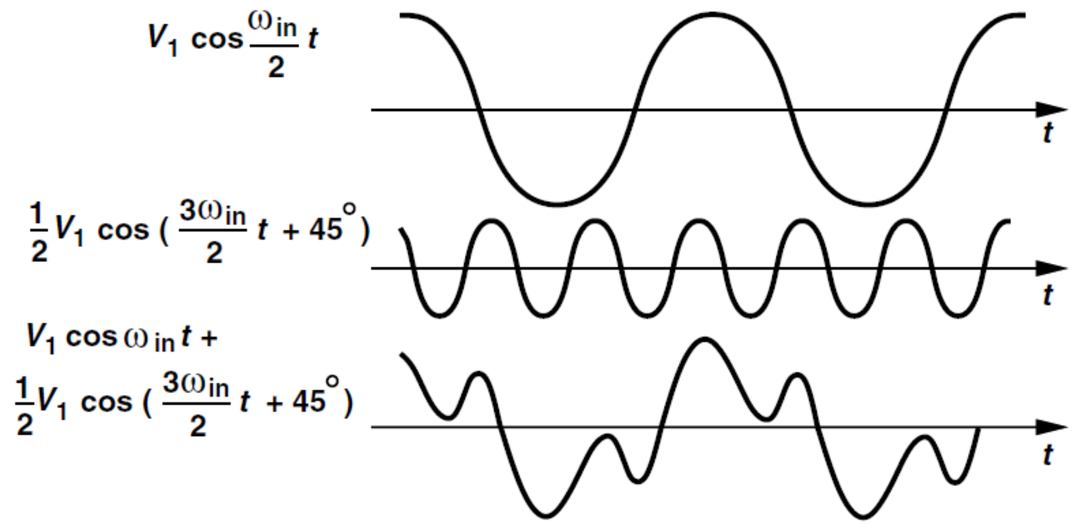
- **With a shorter delay, Miller divider can provide a higher speed than CML logic**
- **However, that the divider loop requires some cycles to reach steady state, i.e., it does not divide correctly instantaneously**

[B. Razavi, RF Microelectronics]

Third Harmonic



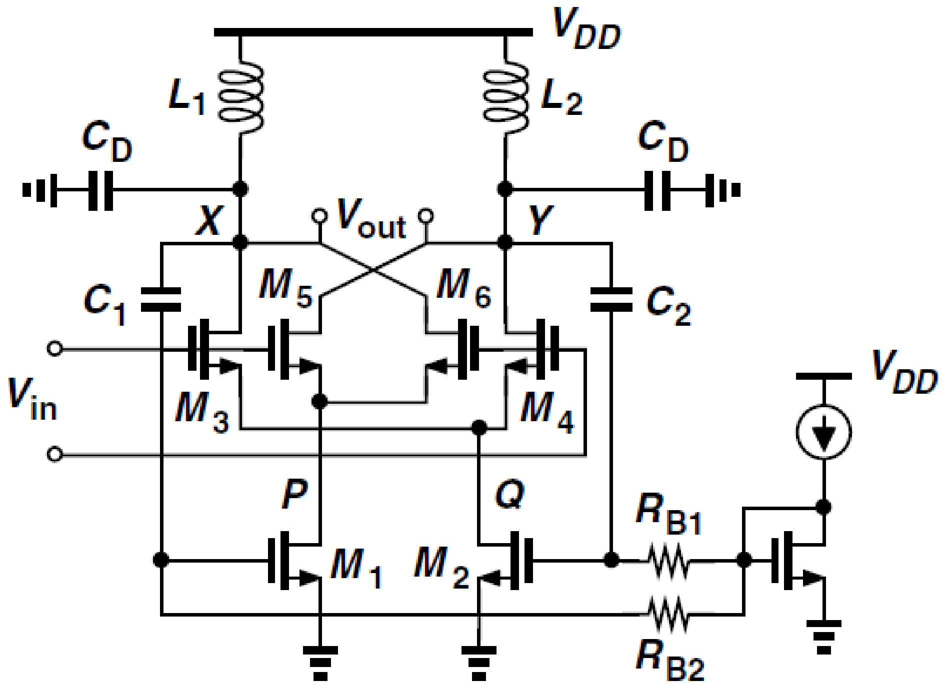




- Miller divider operates properly if the third harmonic is attenuated and shifted to avoid the additional zero crossings

[B. Razavi, RF Microelectronics]

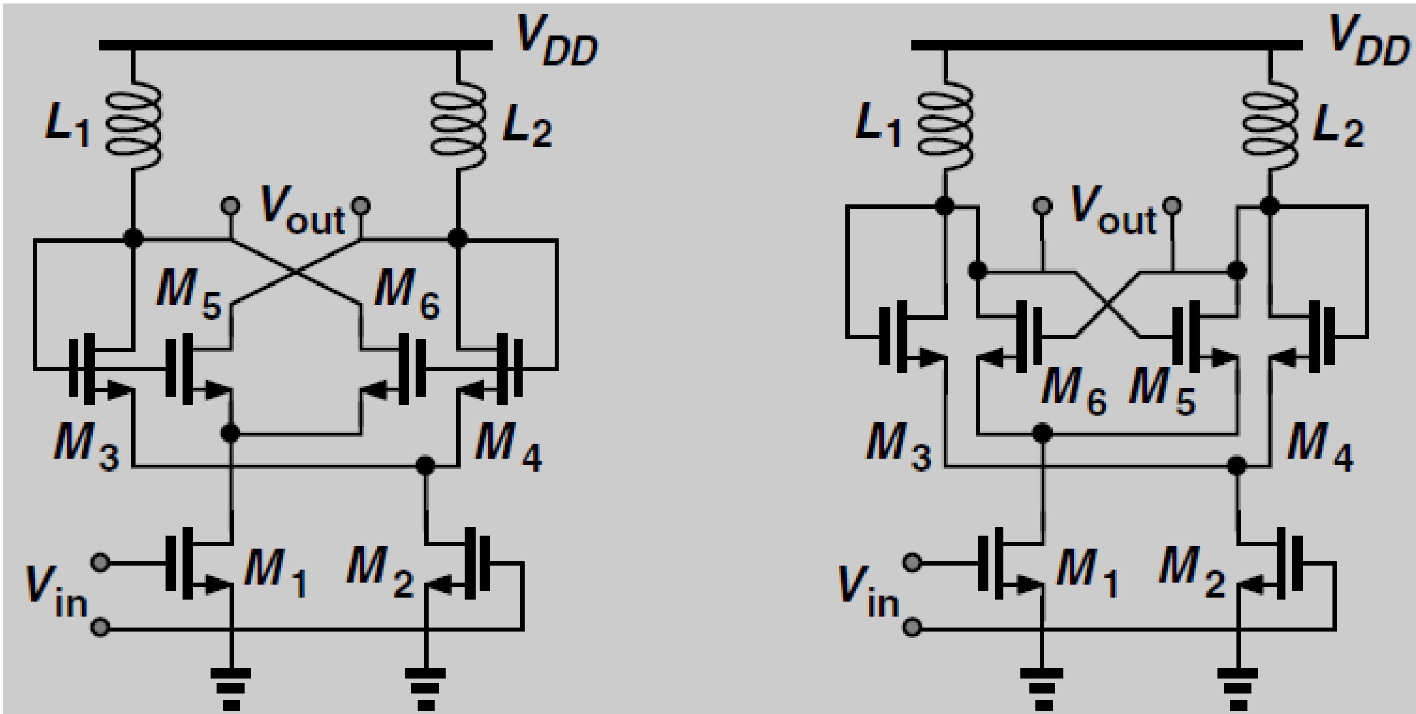
Inductive Load



- ❑Gain-headroom and gain-speed trade-offs are greatly relaxed
- ❑Inductors take more layout area
- ❑Inductors L_1 and L_2 must resonate with the total capacitance at X and Y at the output frequency
- ❑The tanks significantly suppress the third harmonic of the desired output

[B. Razavi, RF Microelectronics]

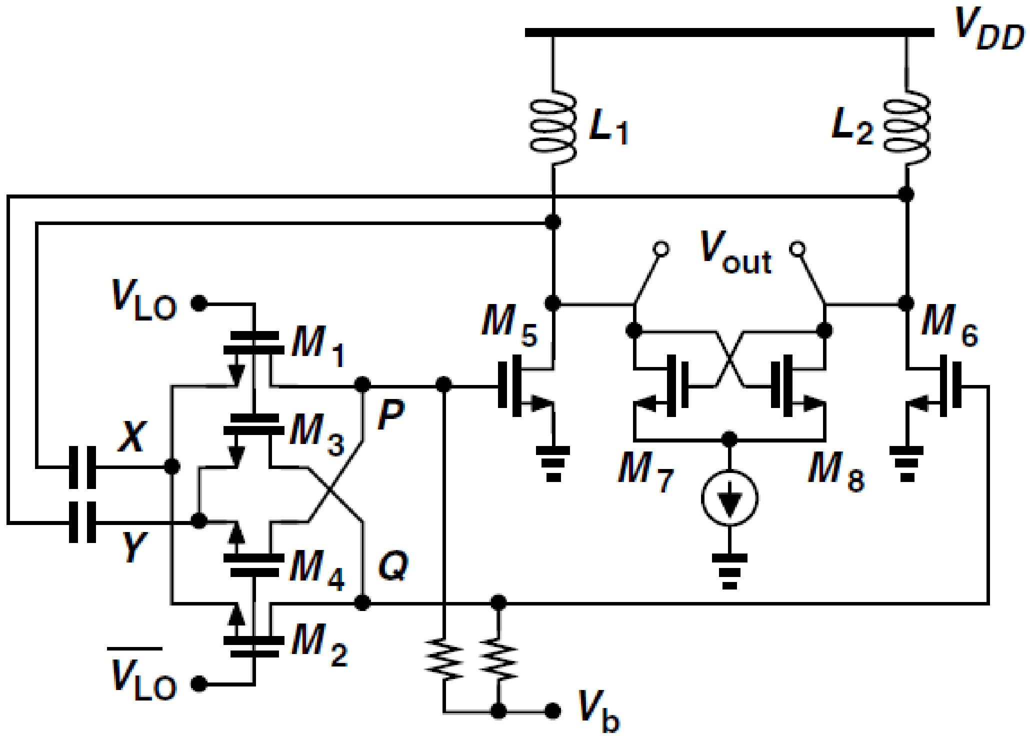
Inductive Load



- ❑Inductively-loaded with feedback to the switching quad, operating as a divider by 2
- ❑An oscillator is formed by M_5-M_6 and L_1-L_2 is heavily loaded by M_3-M_4

[B. Razavi, RF Microelectronics]

Passive Mixer

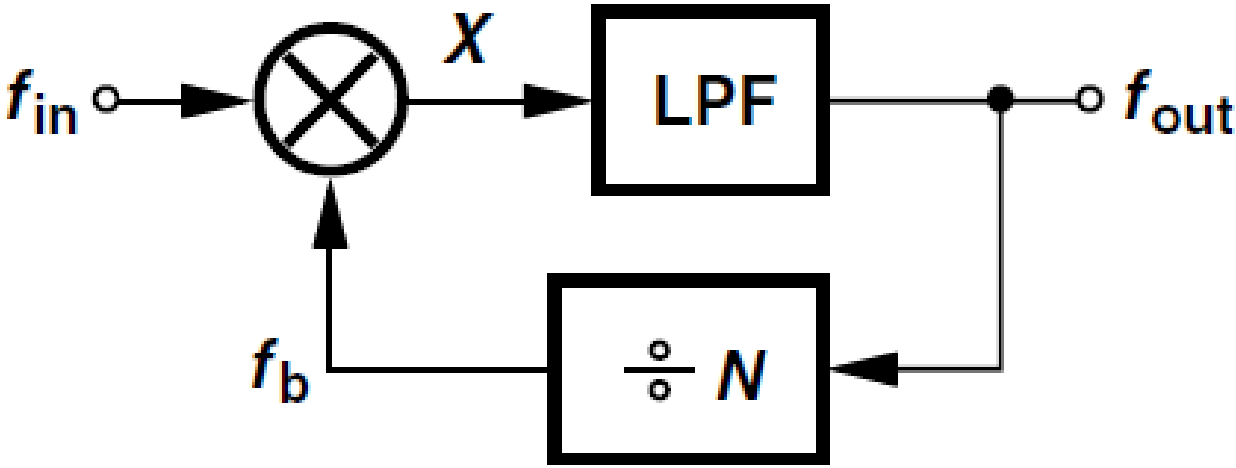


- ❑M_1-M_4 constitute a passive mixer and M_5-M_6 an amplifier
- ❑The cross-coupled pair M_7-M_8 can be added to increase the gain by virtue of its negative resistance.

[B. Razavi, RF Microelectronics]

Feedback Divider

❑A divider within the feedback loop can be used to produce moduli other than 2

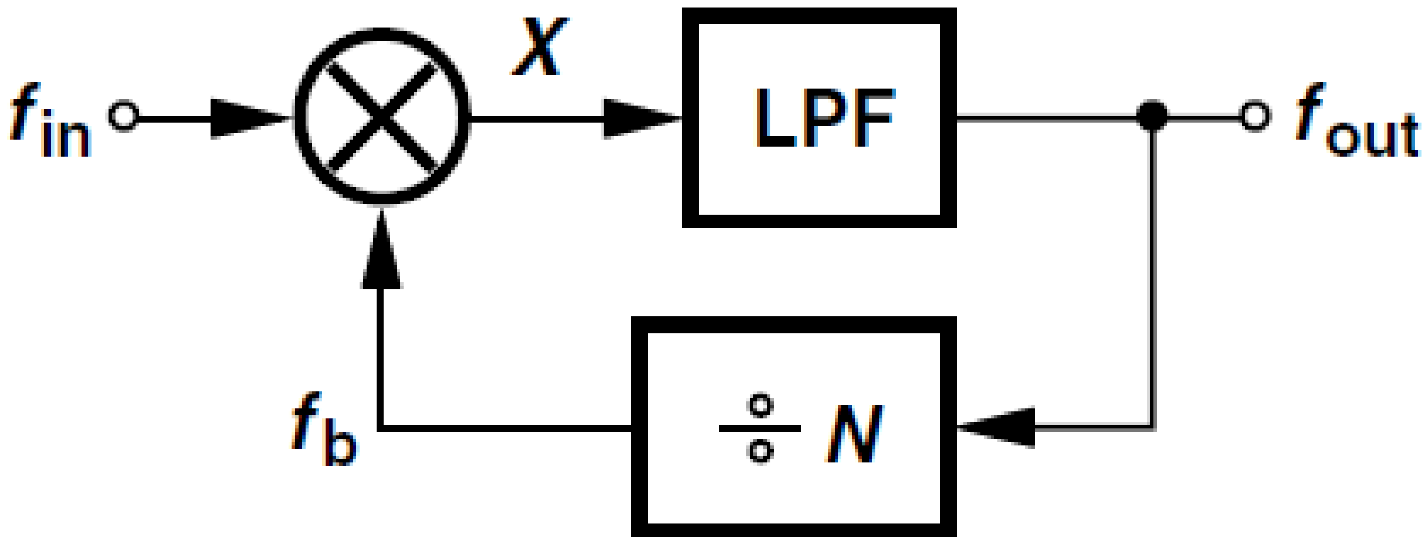


❑If the sum is suppressed by the LPF, then $f_{out}=f_{in}-f_{out}/N$

$$f_{out} = \frac{N}{N+1} f_{in} \qquad f_b = \frac{1}{N+1} f_{in}$$

[B. Razavi, RF Microelectronics]

Feedback Divider

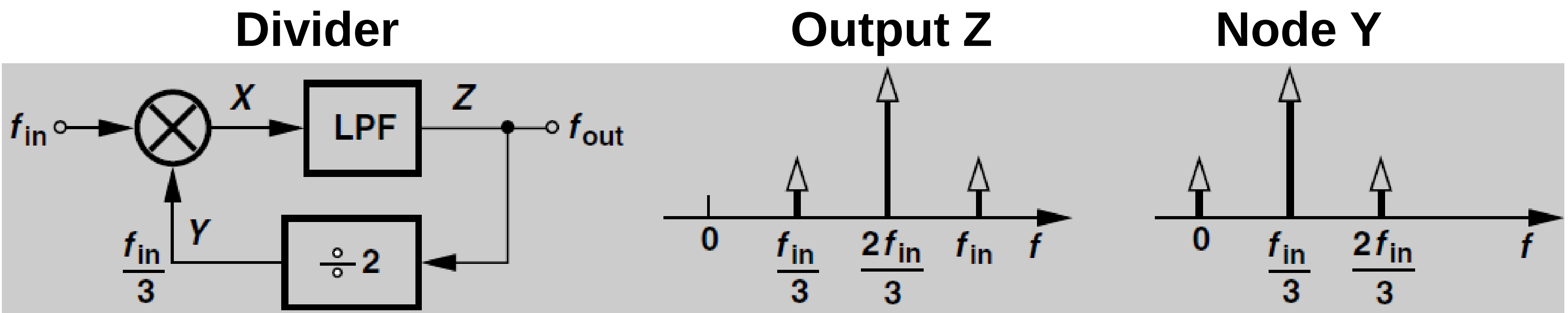


❑The sum component at X comes closer to the difference component as N increases, such as $4f_{in}/3$ and $2f_{in}/3$, dictating a sharper LPF roll-off.

❑The Miller divider suffers from port-to-port feedthroughs of the mixer

[B. Razavi, RF Microelectronics]

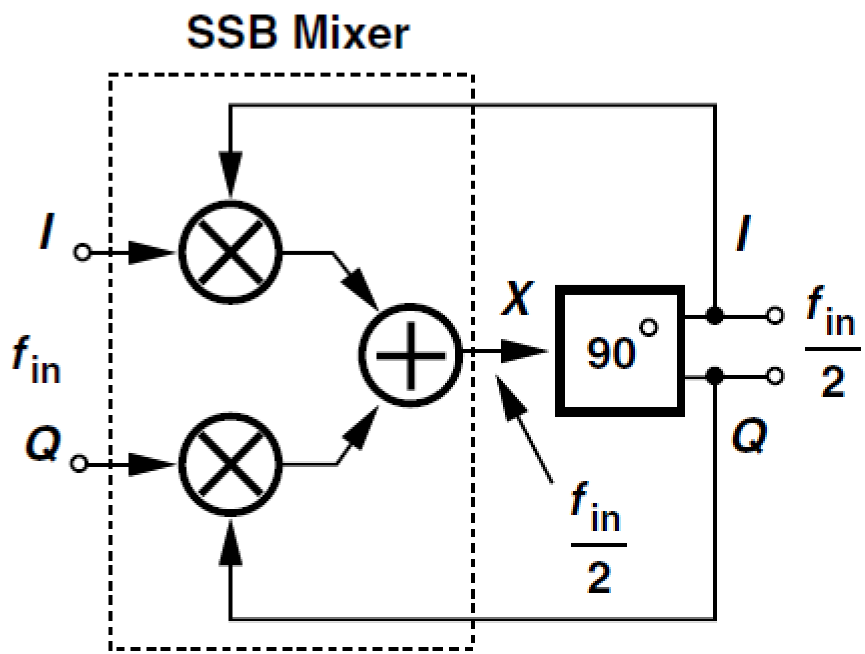
Spurs



- ❑The feedthrough from the main input to node X produces a spur at f_{in}
- ❑The feedthrough from Y to X creates a component at $f_{in}/3$

[B. Razavi, RF Microelectronics]

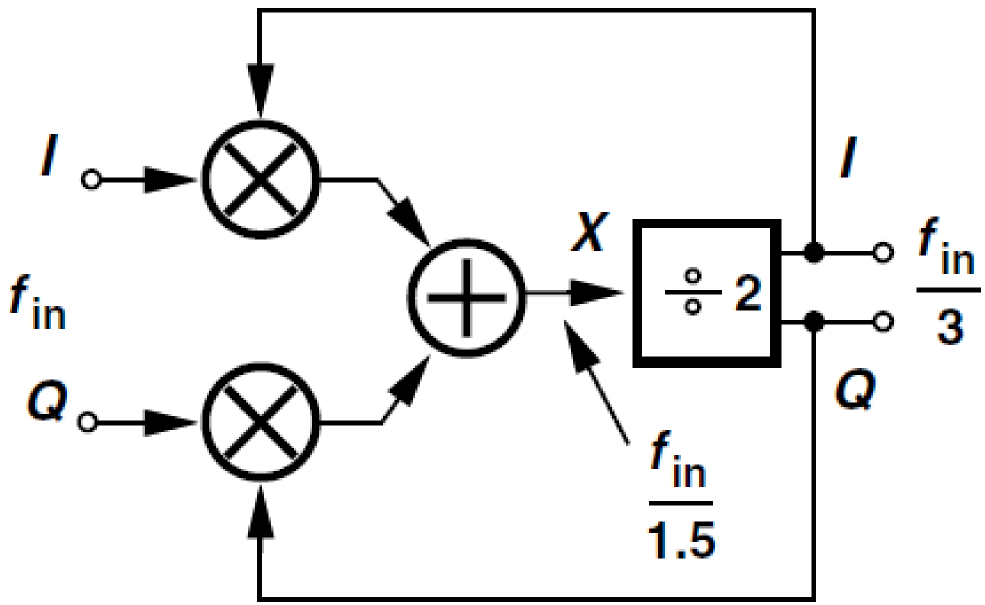
SSB Mixing



- The sum component is suppressed by single-sideband (SSB) mixing rather than filtering, thereby avoiding the problem of additional zero crossings
- however, this approach requires a broadband 90 degree phase shift, a very difficult design.

[B. Razavi, RF Microelectronics]

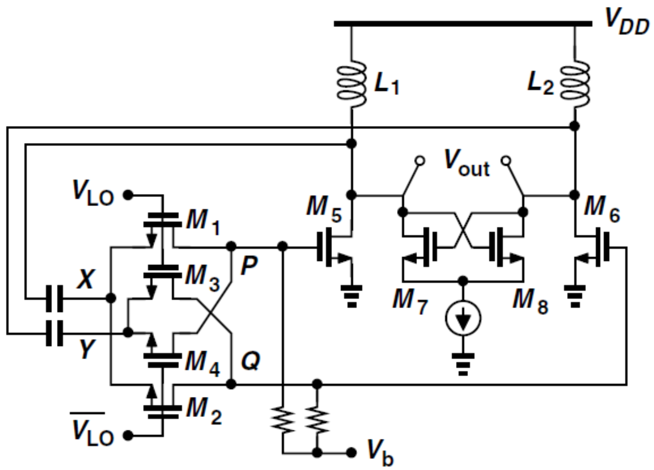
SSB Mixing

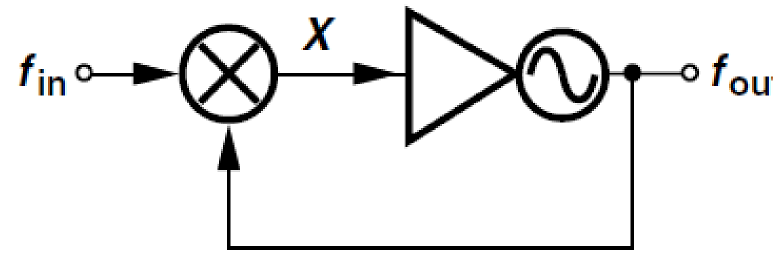


- ❑Employing a ÷2 circuit and generating $f_{in}/3$ at the output generates quadrature outputs
- ❑The principal drawback is that it requires quadrature LO phases as well

[B. Razavi, RF Microelectronics]

Injection-Locked Dividers

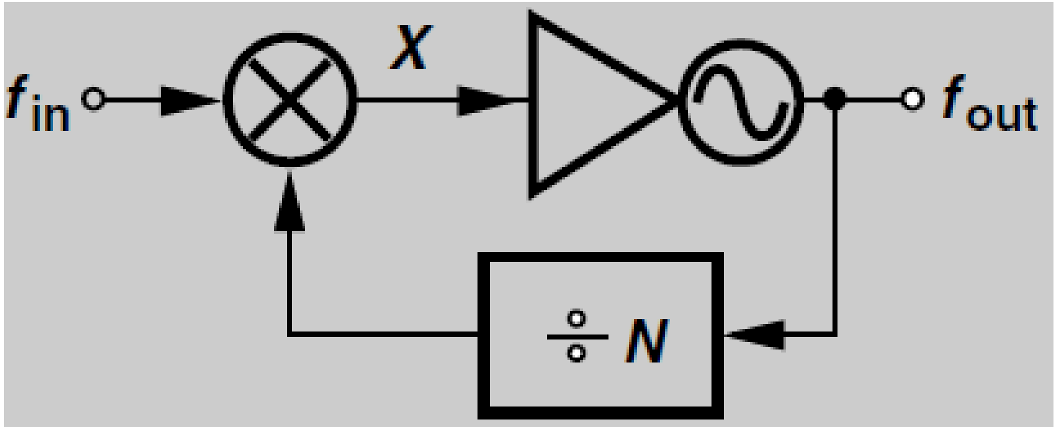




- ❑Assume the cross-coupled pair is strong enough to produce oscillation, transistors M_5 and M_6 can now be viewed as devices that couple the mixer output to the oscillator
- ❑If f_{in} varies across a certain "lock range," the oscillator remains injection locked to the frequency component at node X
- ❑If f_{in} falls outside the lock range, the oscillator is injection-pulled, thus producing a corrupted output

[B. Razavi, RF Microelectronics]

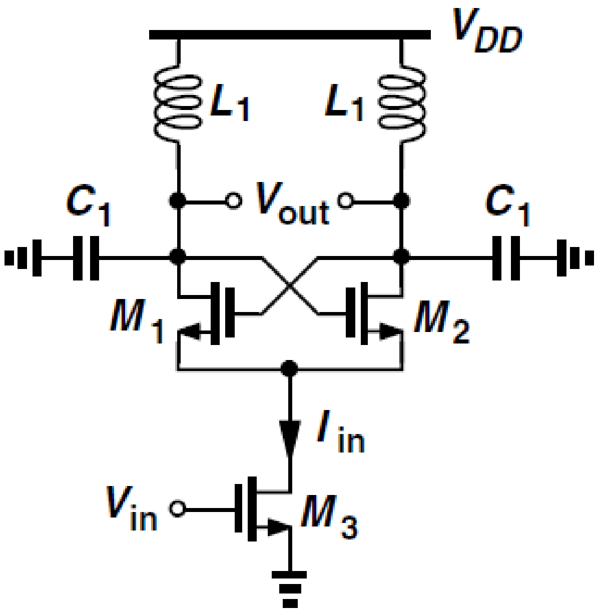
Injection-Locked Dividers

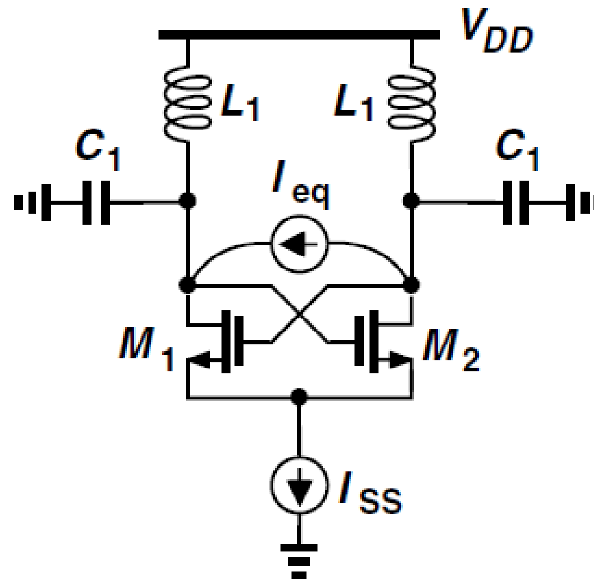


- The mixer yields two components at node X, namely, f_{in}-f_{out}/N and f_{in}+f_{out}/N.
- If the oscillator locks to f_{in}-f_{out}/N, then $f_{out} = \frac{N}{N+1} f_{in}$
- If the oscillator locks to f_{in}+f_{out}/N, then $f_{out} = \frac{N}{N-1} f_{in}$
- The oscillator lock range must therefore be narrow enough to lock to only one of the two components

[B. Razavi, RF Microelectronics]

Injection-Locked Dividers

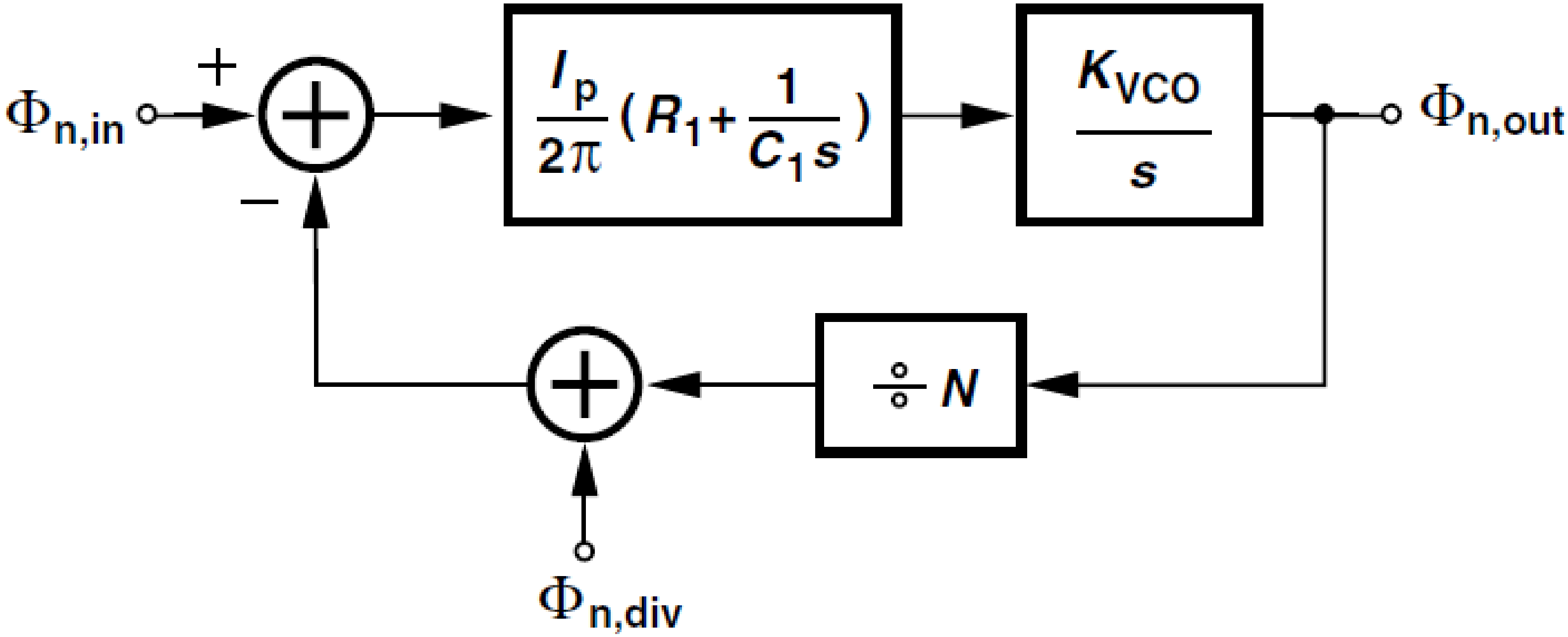




- $I_{in}=g_mV_{in}$ is commutated by M_1 and M_2 and hence translated to $f_{out} \pm f_{in}$ as it emerges at the drains of these transistors.

[B. Razavi, RF Microelectronics]

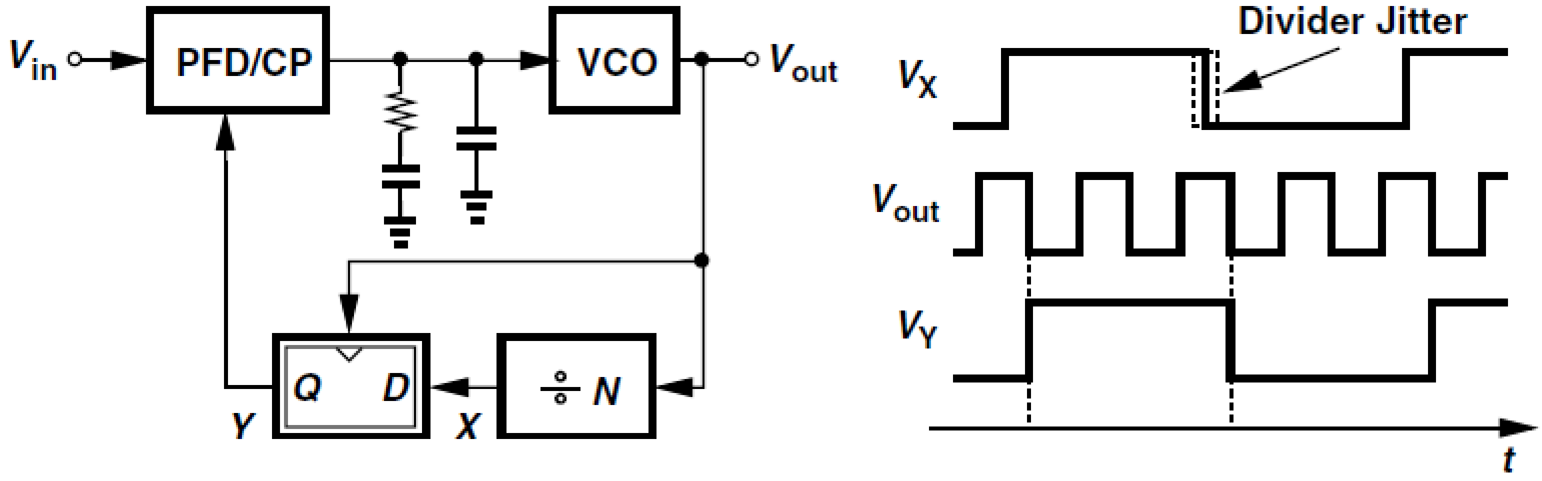
Divider Noise



- **The output phase noise of the divider, $\varphi_{n,div}$, directly adds to the input phase noise, $\varphi_{n,in}$, experiencing the same low-pass response as it propagates to φ_{out}**

[B. Razavi, RF Microelectronics]

Divider Noise



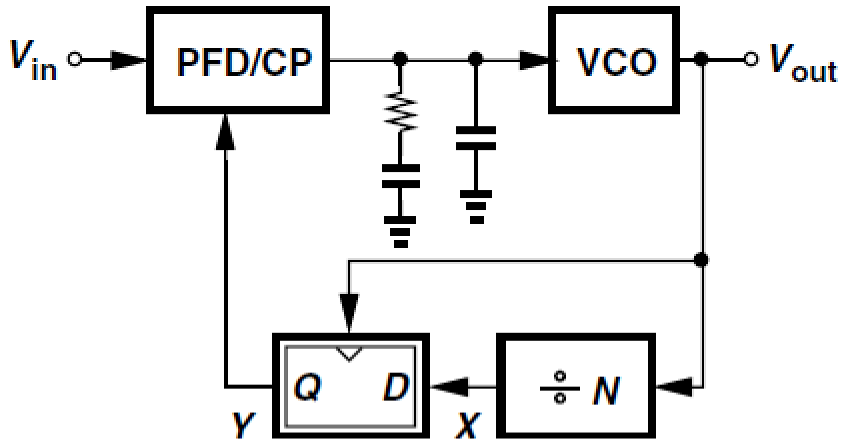
❑A retiming flipflop can be used to suppress the divider noise

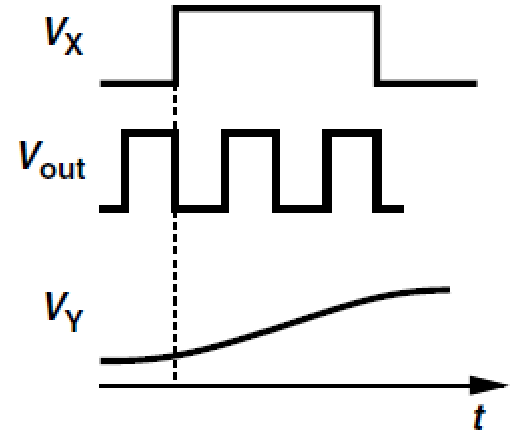
❑The divider output is sampled by the VCO waveform, thus presenting the edges to the PFD only at the VCO transitions

❑In essence, the retiming operation bypasses the phase noise accumulated in the divider chain

[B. Razavi, RF Microelectronics]

Metastability

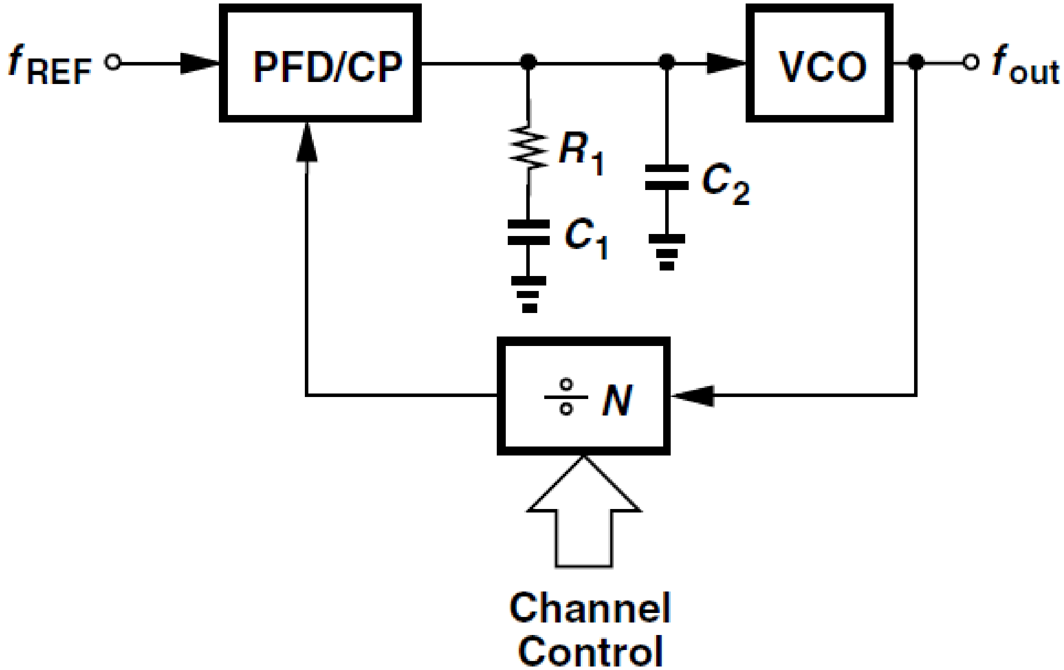




- If the VCO output edge occurs close to the transition at node X, the FF becomes "metastable," i.e., it takes a long time to produce a well-defined logical level
- This effect results in a distorted transition at node Y, confusing the PFD.

[B. Razavi, RF Microelectronics]

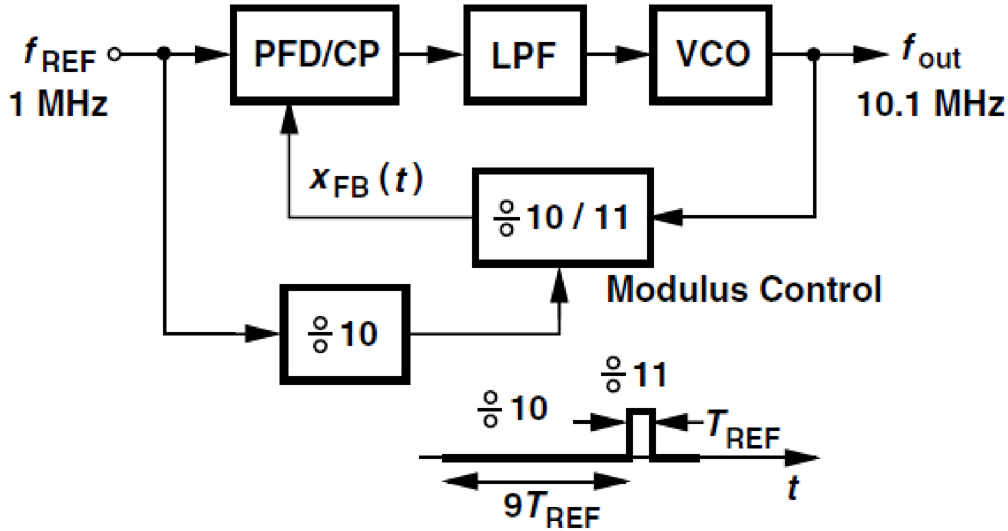
Fractional Multiplication



❑How to realize a fractional multiplication of f_{REF}?

[B. Razavi, RF Microelectronics]

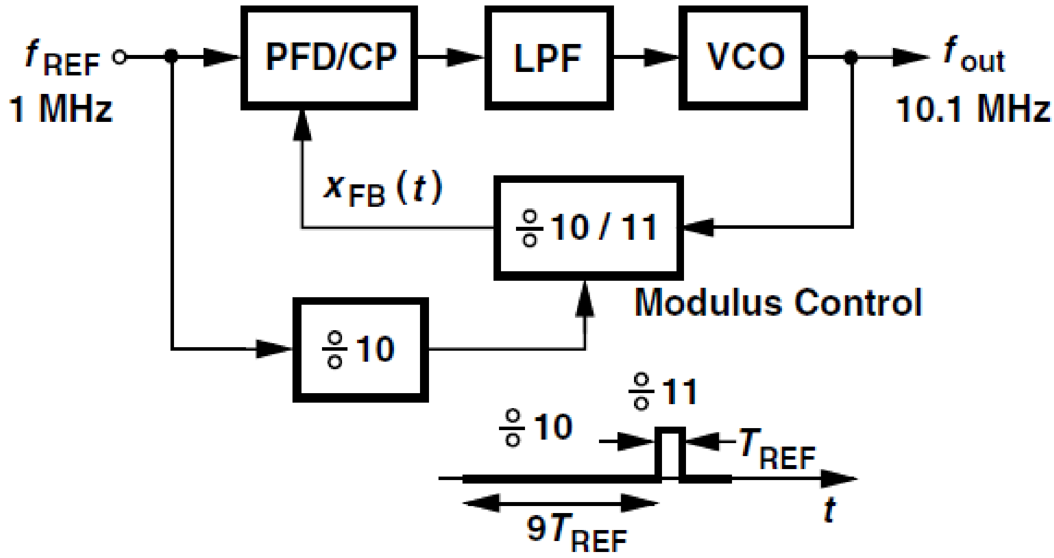
Fractional-N PLL



- ❑Assume the prescaler divides by 10 for 90% of the time (nine reference cycles) and by 11 for 10% of the time,
- ❑For every 10 reference cycles, the output produces 9x10+11=101 pulses, yielding an average divide ratio of 10.1
- ❑If this operation is repeated, the PLL output contains many sidebands at integer multiples of 0.1 MHz (10 reference cycles)

[B. Razavi, RF Microelectronics]

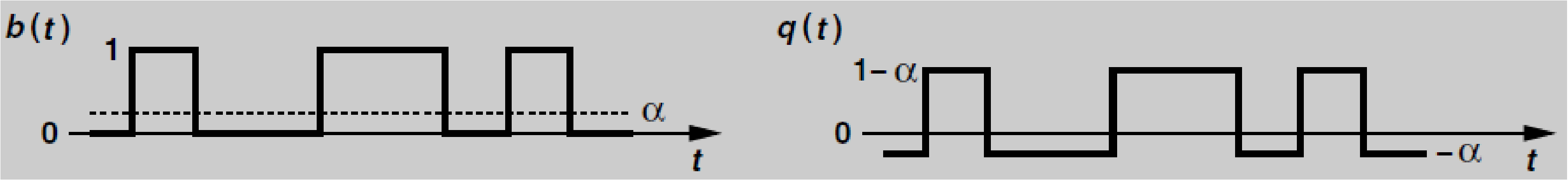
Randomization



- ❑If the divider modulus is randomly set to 10 or 11 but such that its average value is still 10.1
- ❑Randomization of the modulus breaks the periodicity in the loop behavior, converting the spurs to noise

[B. Razavi, RF Microelectronics]

Quantization Noise



❑Suppose the divider has two moduli, N and N+1, and must provide an average modulus of N+α.

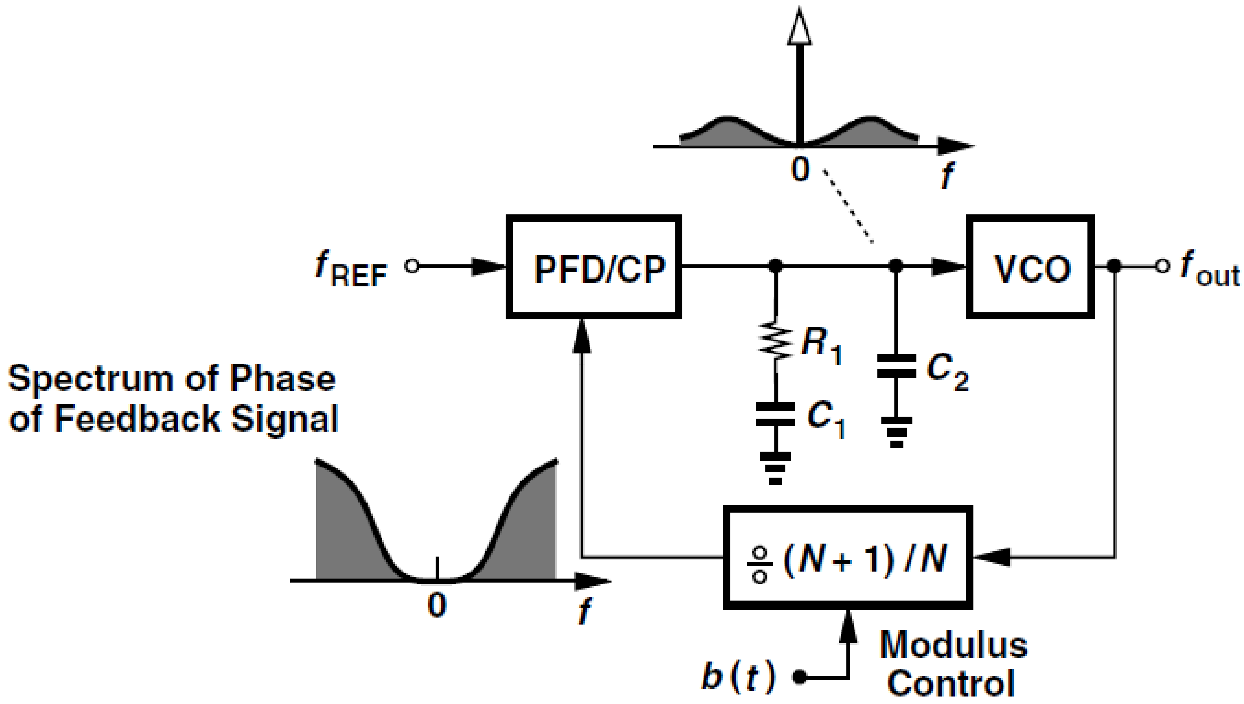
❑We can write the instantaneous modulus as N+b(t), where b(t) randomly assumes a value of 0 or 1 and an average value of α.

$$f_{FB}(t) = \frac{f_{out}}{N + b(t)} \qquad b(t) = \alpha + q(t)$$

❑q(t) the “quantization noise” because it denotes the error incurred by b(t) in approximating the value of α

[B. Razavi, RF Microelectronics]

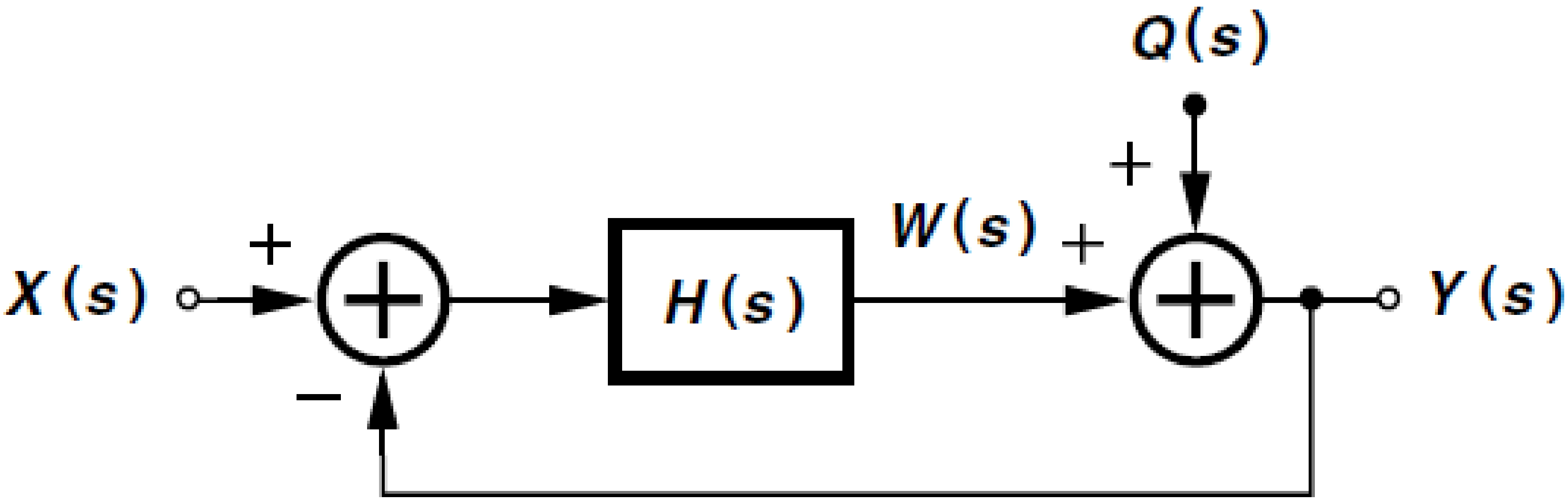
Modulus Randomization



- ❑Randomization can be performed such that the resulting phase noise exhibits a high-pass spectrum
- ❑The generation of the sequence b(t) so as to create a high-pass phase spectrum is called “noise shaping”

[B. Razavi, RF Microelectronics]

Transfer Function



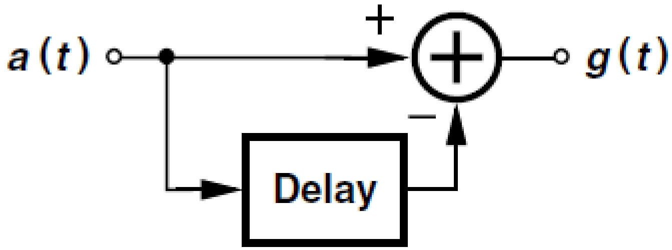
❑if H(s) is an ideal integrator

$$\frac{Y(s)}{Q(s)} = \frac{1}{1 + H(s)} \qquad \frac{Y(s)}{Q(s)} = \frac{s}{s + 1}$$

❑A negative feedback loop containing an integrator acts as a high-pass system on the noise injected "near" the output

[B. Razavi, RF Microelectronics]

Time Domain



- Recall from the definition of the z-transform that $z=\exp(j2\pi fT_{CK})$, where T_{CK} denotes the sampling or clock period
- At a given clock, g(t) shows a high-pass versus the input a(t)

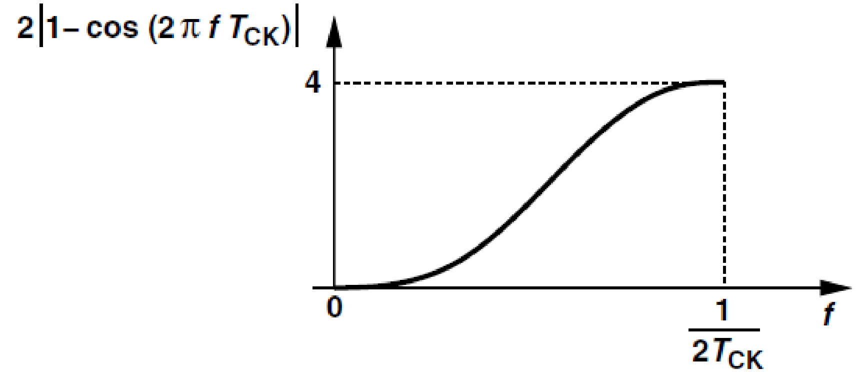
$$\frac{Y}{Q}(z) = 1 - z^{-1}$$

$$= e^{-j\pi f T_{CK}}\left(e^{j\pi f T_{CK}} - e^{-j\pi f T_{CK}}\right)$$

$$= 2je^{-j\pi f T_{CK}}\sin(\pi f T_{CK})$$

$$S_y(f) = S_q(f)|2\sin(\pi f T_{CK})|^2$$

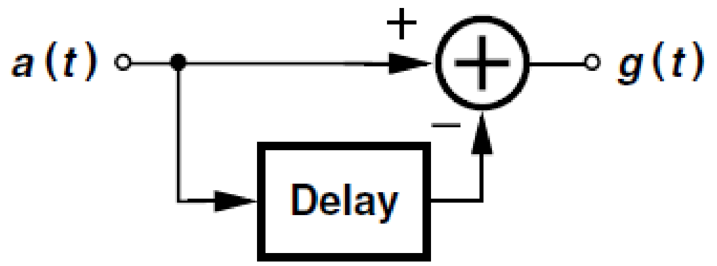
$$= 2S_q(f)|1-\cos(2\pi f T_{CK})|$$

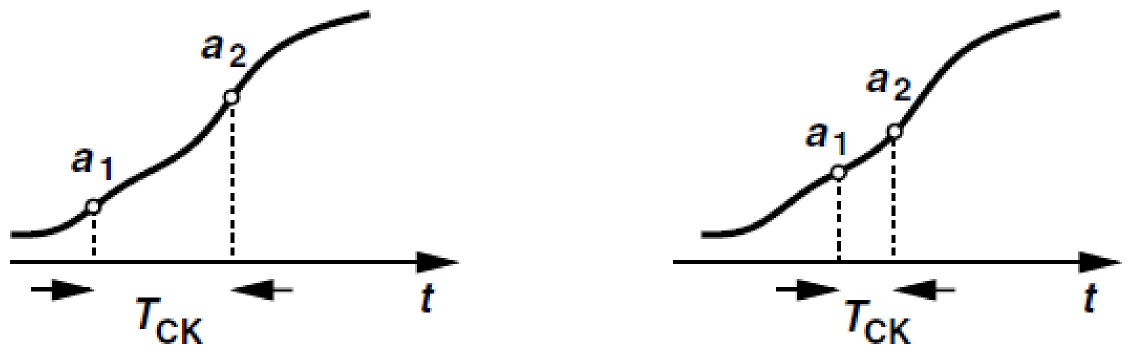


[B. Razavi, RF Microelectronics]

Integrator

- ❑Discrete-time integration can be realized by delaying the signal and adding the result to itself

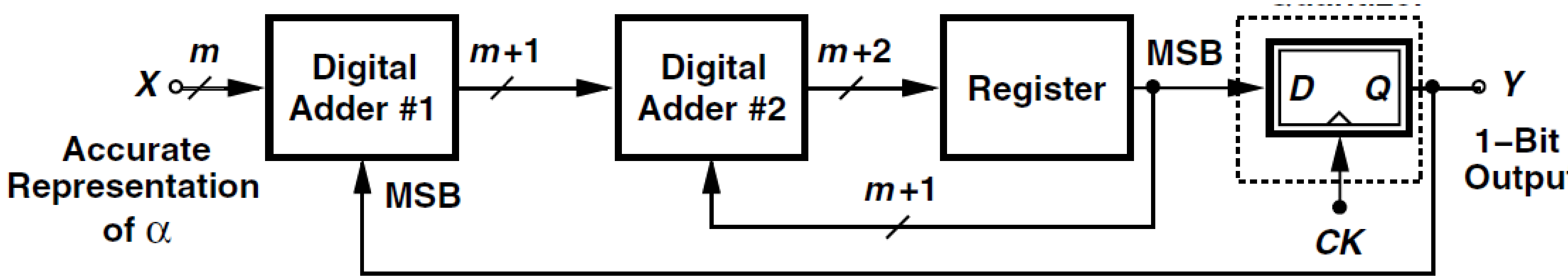




- ❑If the clock frequency increases, a(t) finds less time to change, and a_1 and a_2 exhibit a small difference, so the high-frequency noise of clock can be rejected by a greater amount. *[B. Razavi, RF Microelectronics]*

ΣΔ Modulator

- ΣΔ modulator is constructed to produce a binary output with an average value of α and a shaped noise spectrum

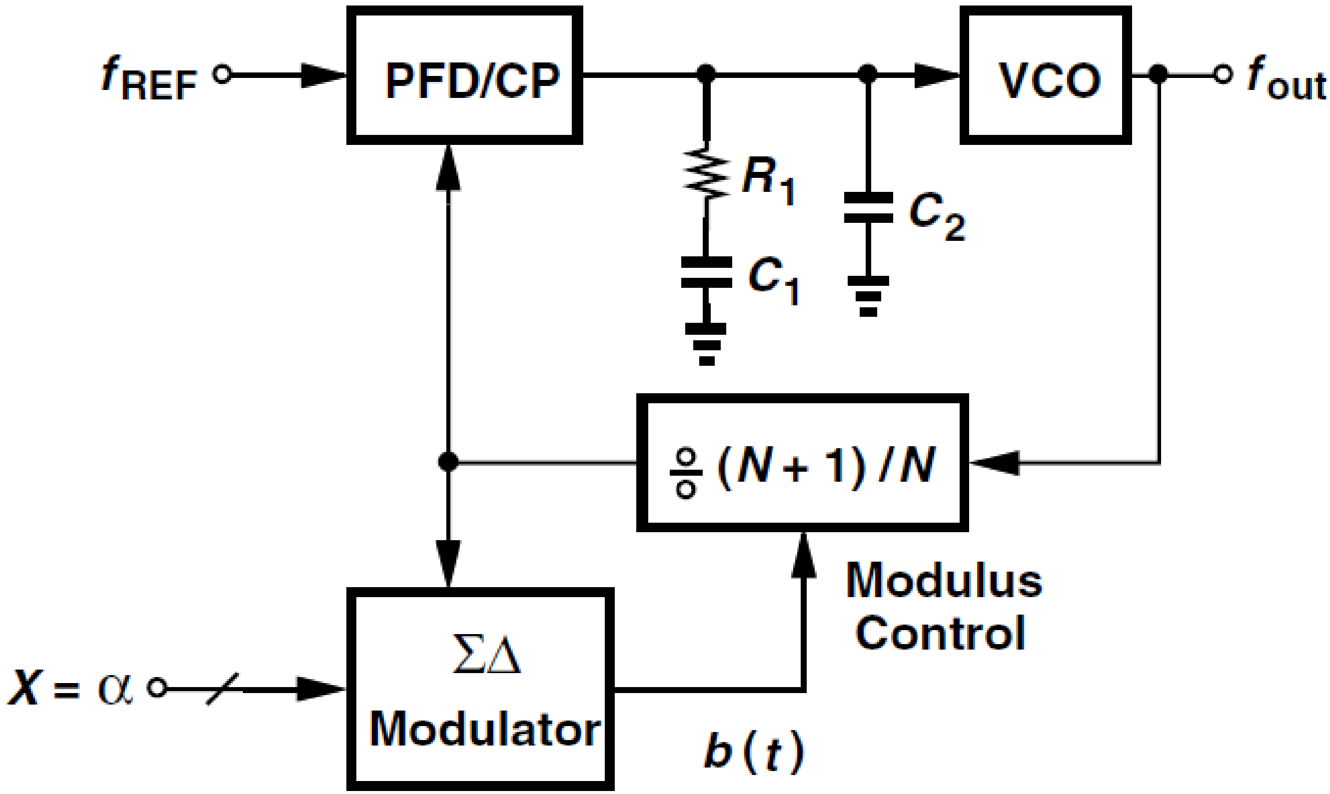


- The high-resolution output of the integrator drives a flipflop (i.e., a one-bit quantizer), thereby generating a single-bit binary stream at the output.

- The quantization from m+2 bits to 1 bit introduces quantization noise, but the feedback loop shapes this noise in proportion to $1\text{-}z^{-1}$

[B. Razavi, RF Microelectronics]

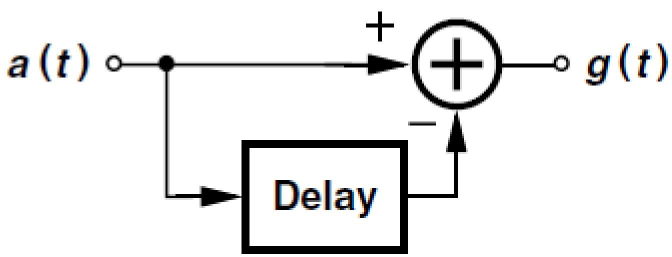
ΣΔ PLL

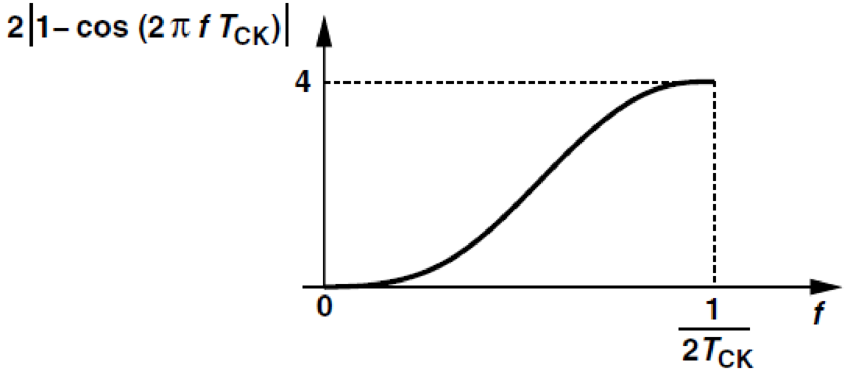


❑Clocked by the feedback signal, the modulator toggles the divide ratio between N and N+1 so that the average is equal to N+α.

[B. Razavi, RF Microelectronics]

Noise Shaping Order





$$S_y(f) = S_q(f)|2\sin(\pi f T_{CK})|^2$$
$$= 2S_q(f)|1 - \cos(2\pi f T_{CK})|$$

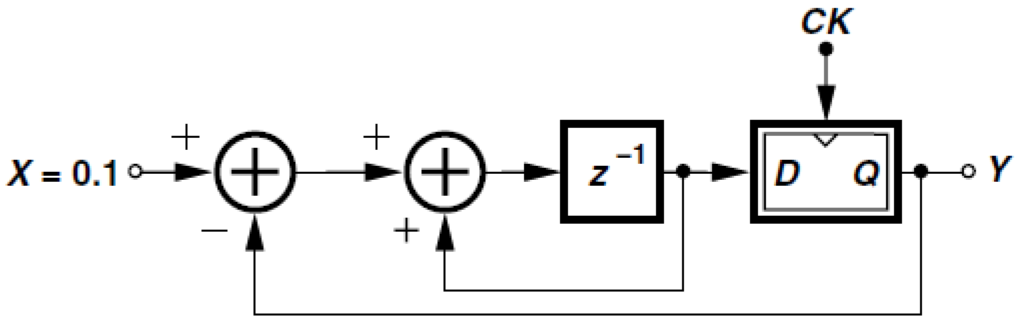
If $f \ll (\pi T_{CK})^{-1}$

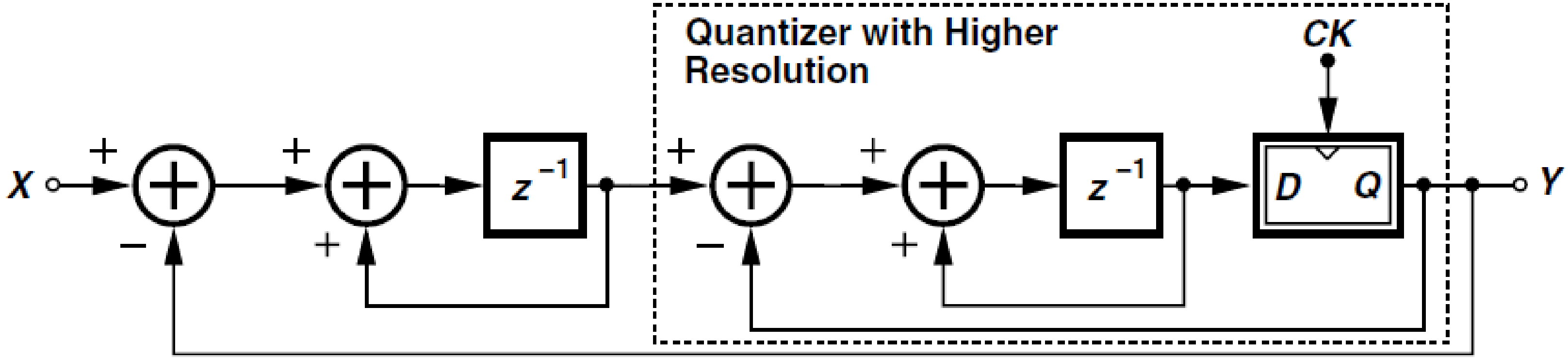
$$S_y(f) = S_q(f)|2\pi f T_{CK}|^2$$

- **An integrator results in a 2^nd^-order roll-off in a PLL**
- **We therefore seek a system that exhibits a sharper roll-off, e.g., an output spectrum in proportion to f^n with n>2**

[B. Razavi, RF Microelectronics]

2^{nd}-Order ΣΔ Modulator

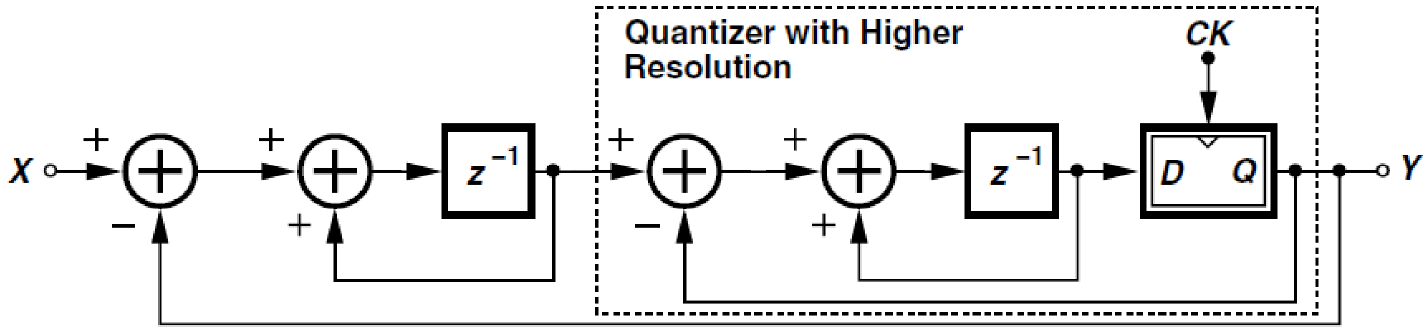


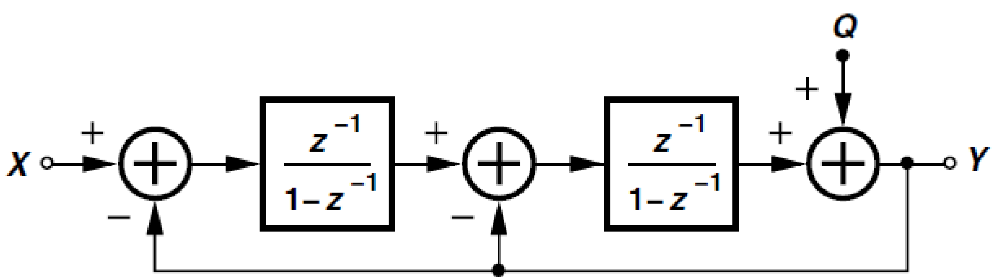


- ❑A ΣΔ modulator can suppress the quantization noise at low frequencies, we therefore replace the 1-bit quantizer with another ΣΔ modulator

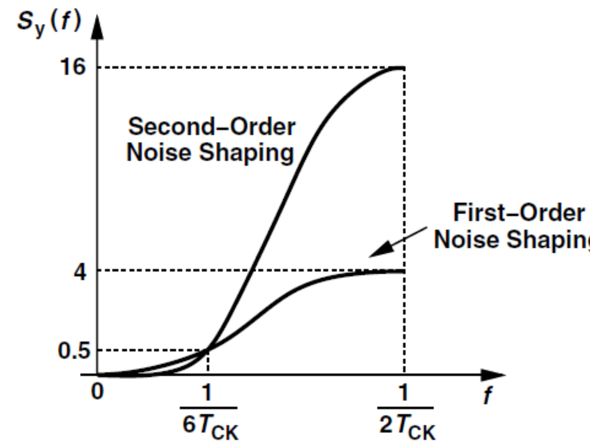
[B. Razavi, RF Microelectronics]

2nd-Order Noise Shaping





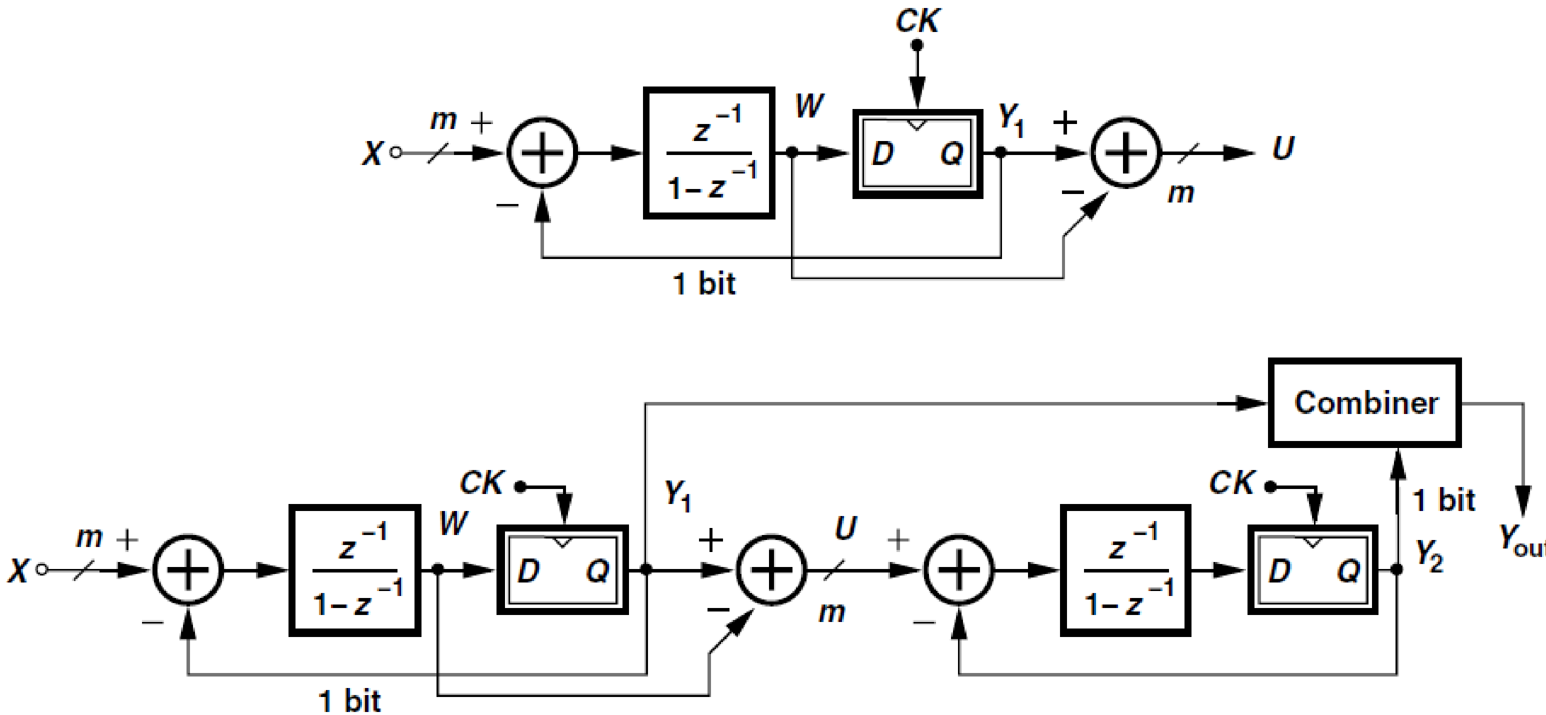
$$\frac{Y}{Q}(z) = (1 - z^{-1})^2 \qquad S_y(f) = S_q(f)|2\sin(\pi f T_{CK})|^4$$



- ❑Noise shaping falls in proportion to f^4
- ❑We can have even higher orders

[B. Razavi, RF Microelectronics]

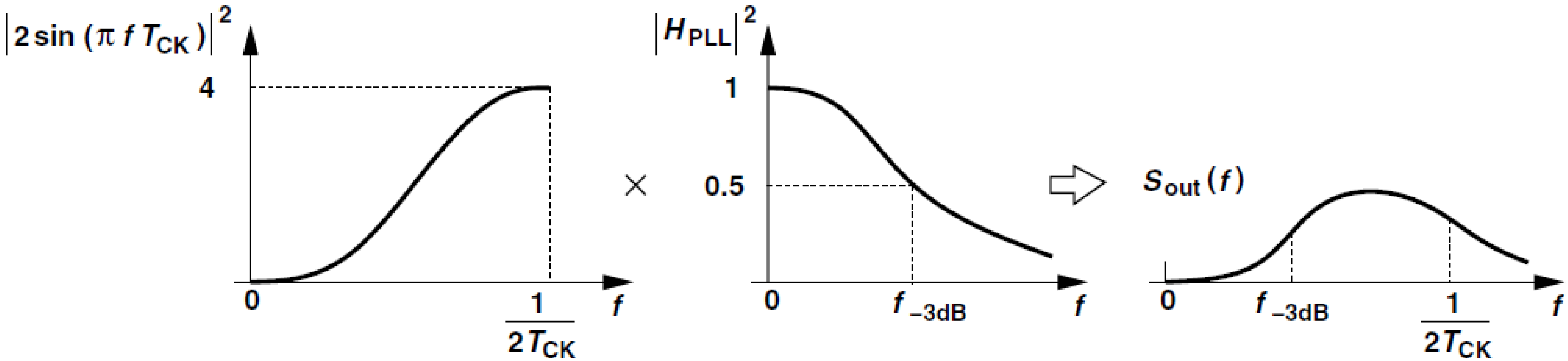
Cascaded Modulator

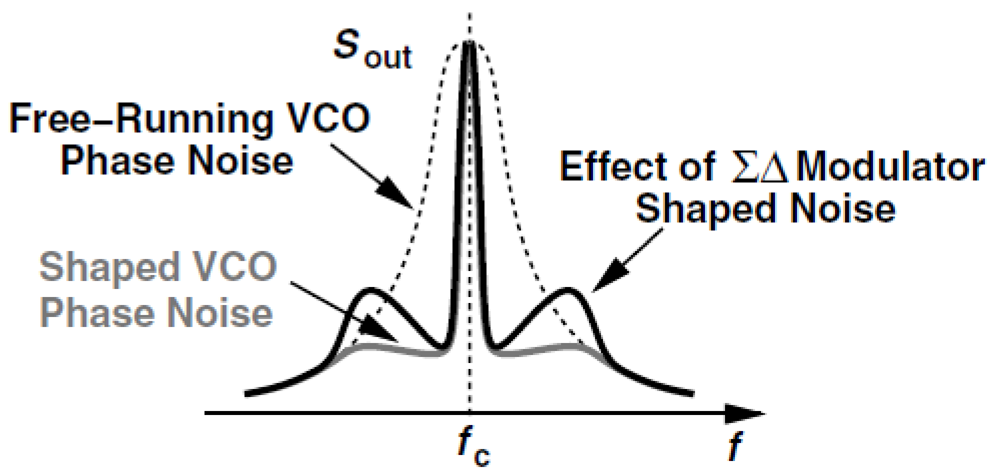


- ❑$U=Y_1-W=Q$ is the quantization error introduced by the first quantizer. Y_2 is a relatively accurate replica of U
- ❑Y_2 is combined with Y_1, yielding Y_{out} as a more accurate representation of X, achieving a 2nd-order modulator

[B. Razavi, RF Microelectronics]

Quantization Noise of PLL





- There is peaking of the phase noise spectrum at a certain frequency.

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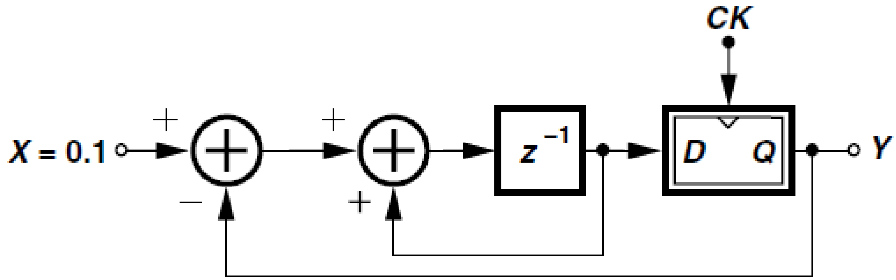
Reconstruct Quantization Noise

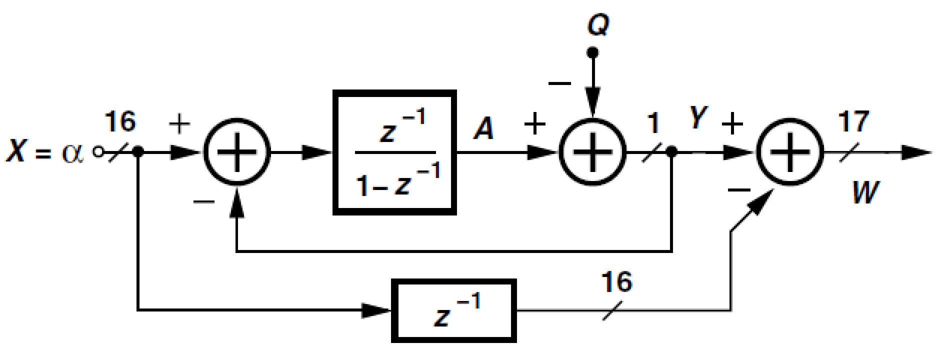


❑A first-order, one-bit modulator produces

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z)$$

❑We delay X(z) by one clock cycle and subtract the result from Y(z) to reconstruct the quantization error:

$$W(z) = Y(z) - z^{-1}X(z) = (1 - z^{-1})Q(z)$$



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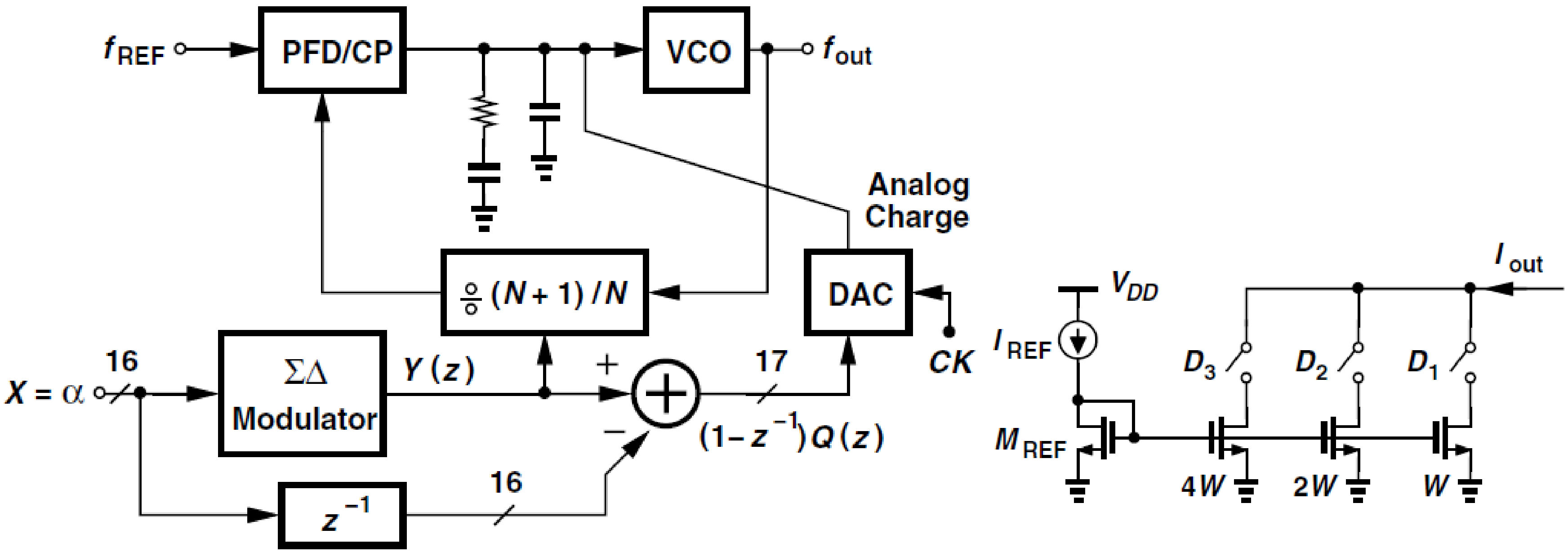
DAC Forward Cancellation

- The output of ΣΔ modulator travels through the divider, the PFD, and the charge pump is met by the output of a DAC, facing perfect cancellation



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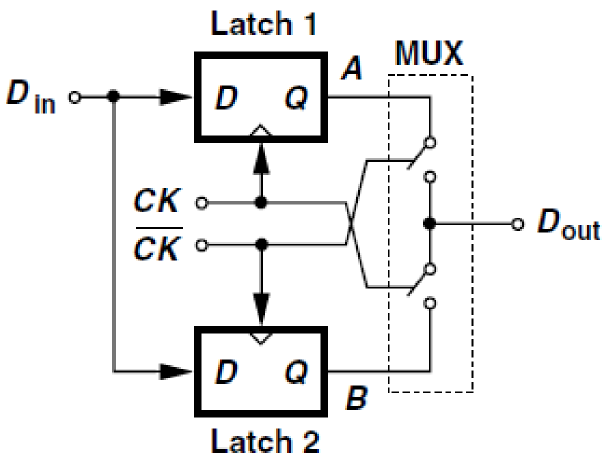
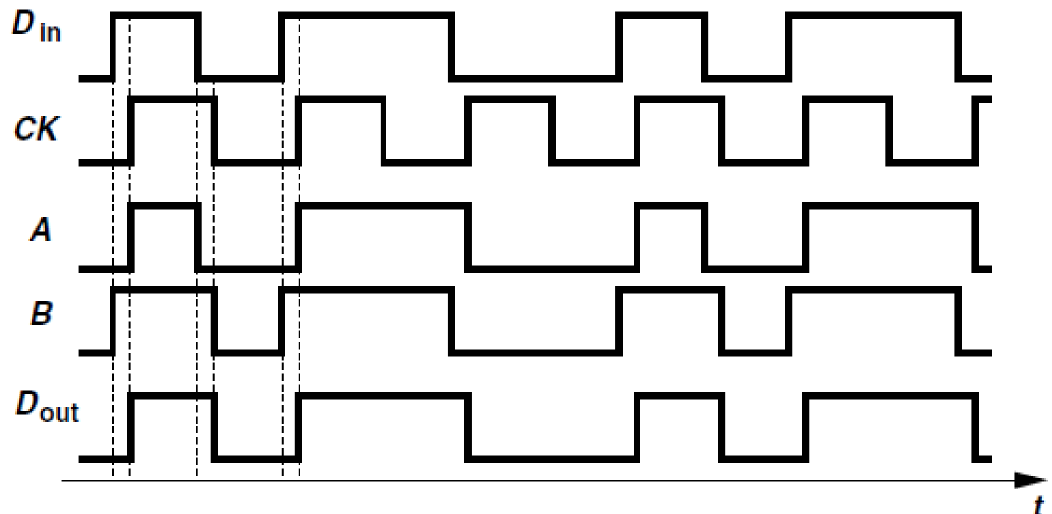
Double-Edge-Triggered Flipflop





- ❑When CK is high, the top latch is in the sense mode and the bottom latch in the hold mode, and vice versa
- ❑For a given clock rate, the input data can be twice as fast as that applied to a single-edge-triggered counterpart

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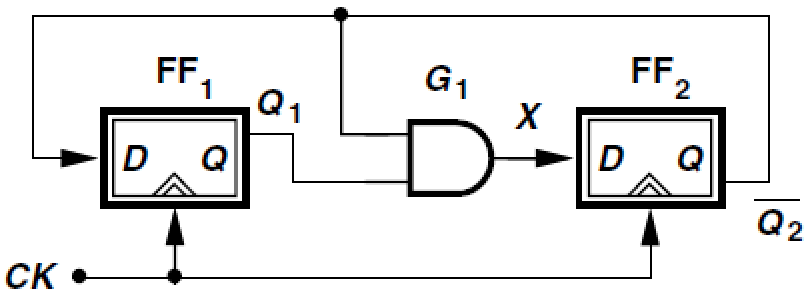
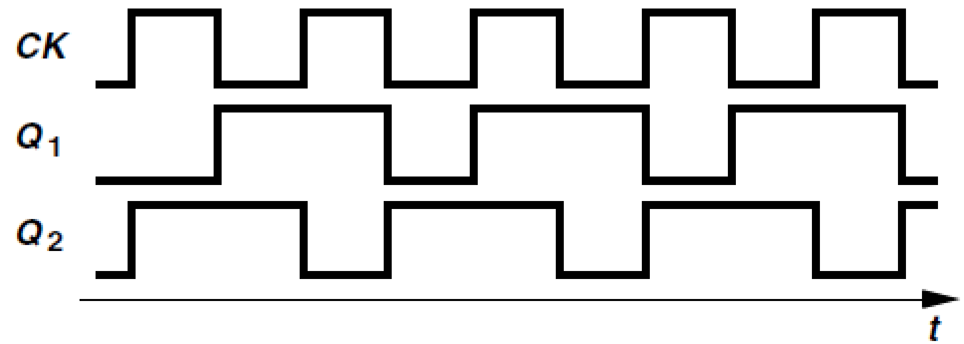
Fractional Divider





- **With the double-edge-triggered flipflops, the ÷3 divider can realize a divide-by-1.5 circuit**
- **The fractional divider can replace the ΣΔ modulator in some case to avoid the quantization noise**

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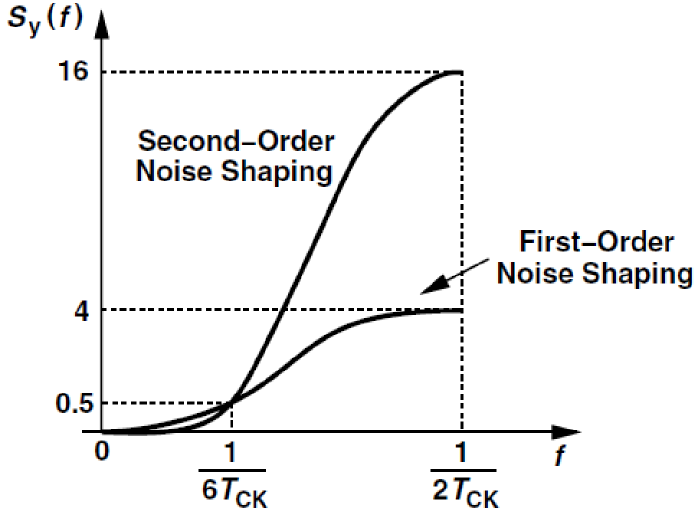
Reference Doubling

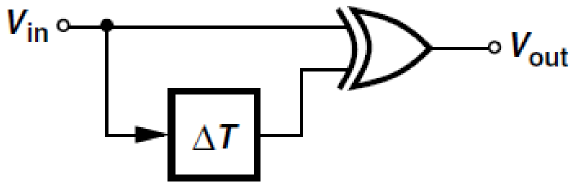


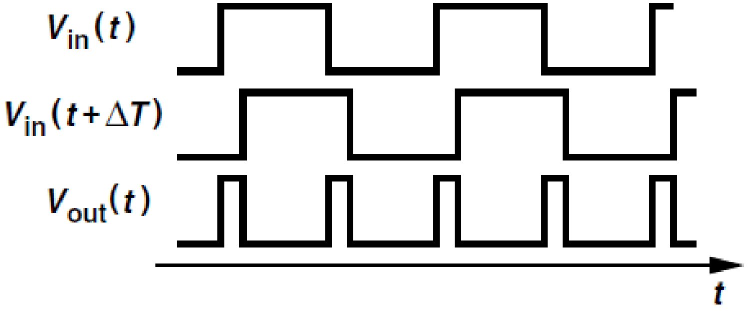
- ❑The noise shaping function indicates a direct dependence on the clock frequency

$$S_y(f) = S_q(f)|2\pi f T_{CK}|^2$$

- ❑If T_{CK} is halved, the noise power falls by 6 dB

- ❑However, a crystal oscillator can only provide a reference frequency less than 100 MHz





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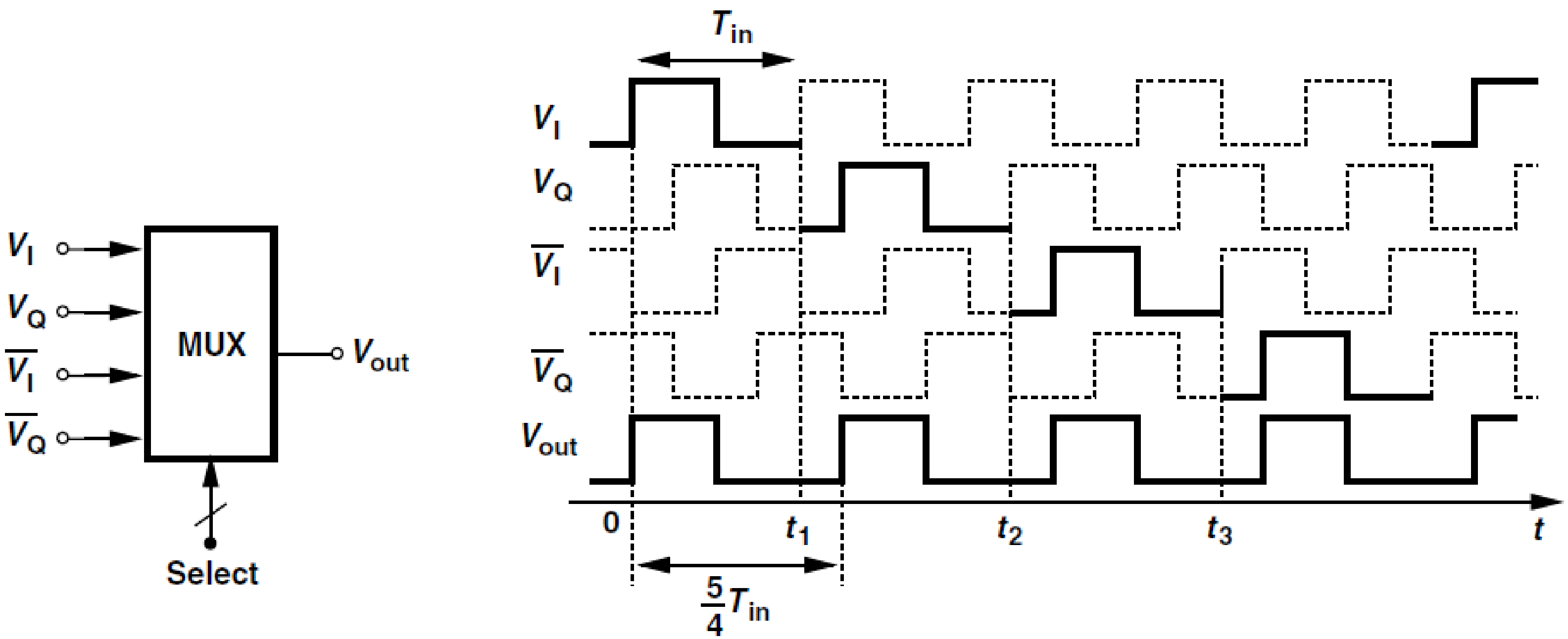
Multiphase Frequency Division



- ❑The VCO is designed to generate multiple phases at the output
- ❑The I and Q are picked out to realize a divide-by-1.25 operation

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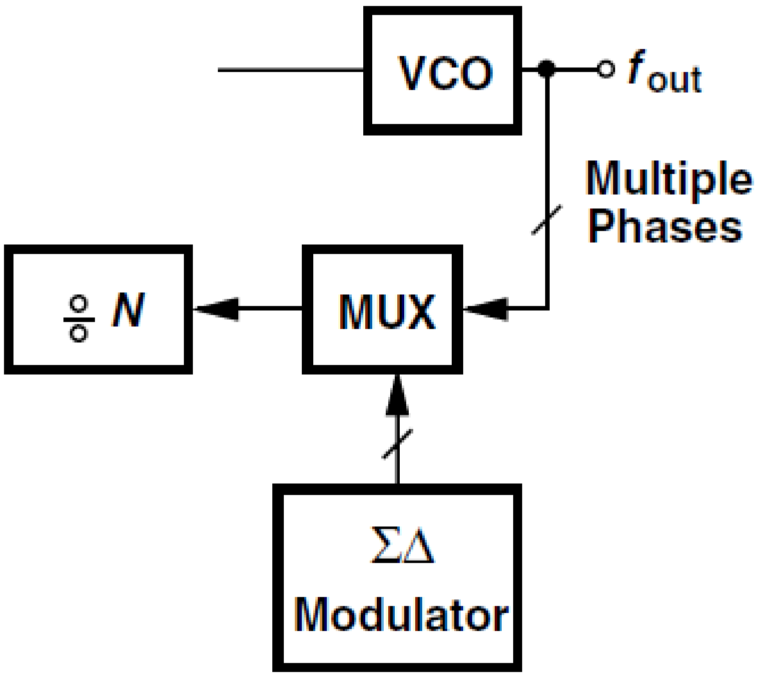
Multiphase Frequency Division



- A ΣΔ modulator is adopted to randomize selection of the VCO phases
- This randomization can also incorporate noise shaping
- The multiplexing of the VCO phases can be placed after the feedback divider to make the MUX easier to design

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