1. **Try to describe the basic principle of the PFD in Fig. 9.1. Analyze its advantage over a XOR gate.**

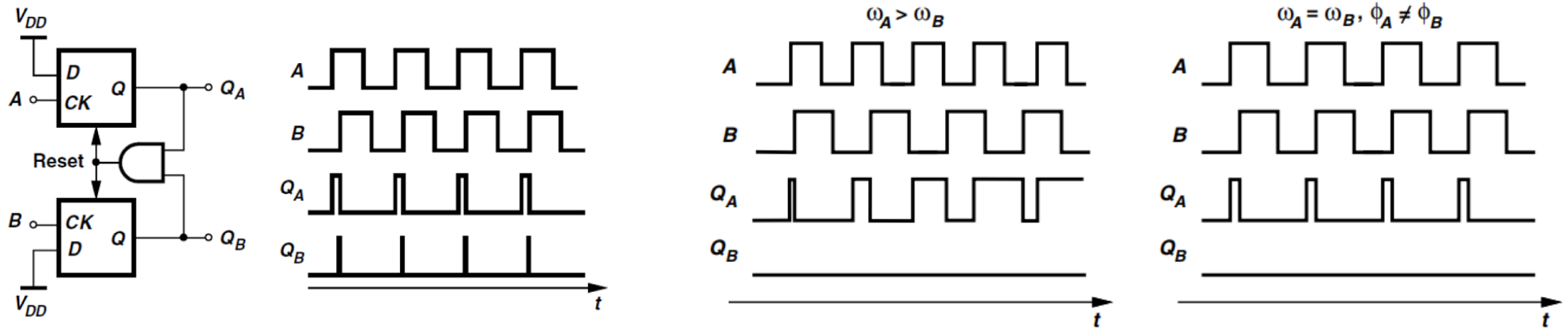


Fig. 9.1

- (1) a rising edge on A yields a rising edge on QA (if QA is low), and (2) a rising edge on B resets QA (if QA is high). The circuit is symmetric with respect to A and B (and QA and QB). We observe from Fig. 9.1 that, if ωA > ωB, then QA produces pulses while QB remains at zero. Conversely, if ωB > ωA, then positive pulses appear at QB and QA=0. On the other hand, as depicted in the figure on the right, if ωA=ωB, the circuit generates pulses at either QA or QB with a width equal to the phase difference between A and B. Thus, the average value of QA-QB represents the frequency or phase difference.
- Signals A and B act as clock inputs of DFFA and DFFB, respectively, and the AND gate resets the flipflops if QA=QB=1. We note that a transition on A forces QA to be equal to D input, i.e., a logical ONE. Subsequent transitions on A have no effect. When B goes high, so does QB, activating the reset of the flipflops. Thus, QA and QB are simultaneously high for a duration given by the total delay through the AND gate and the reset path of the flipflops
- XOR Gate can only detect phase difference, whereas the PFD in Fig. 9.1 can detect frequency difference as well as phase difference.

2. **For the PLL shown in Fig. 9.2. If $\omega_{in}$is a FSK signal with a data rate of 1MHz and a carrier frequency of 10MHz, while the loop bandwidth of PLL is 100KHz. What will happen?**

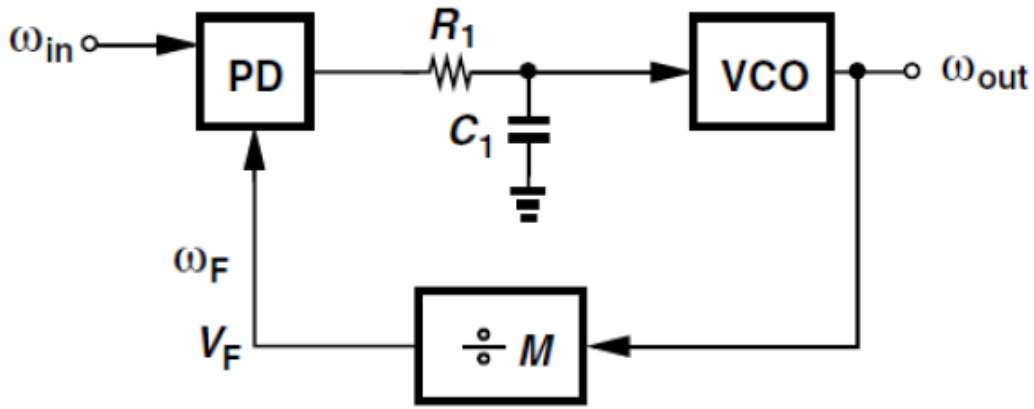
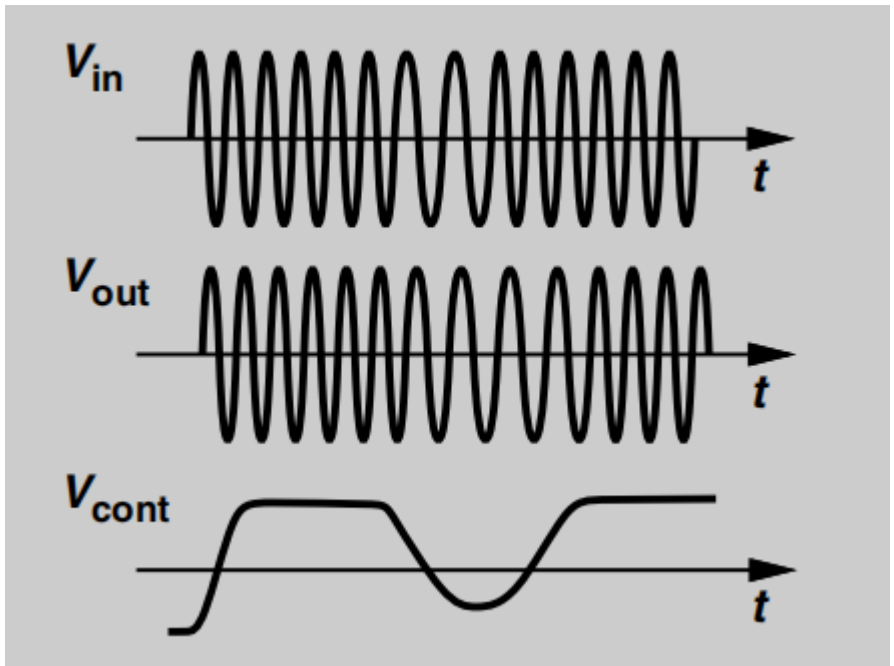
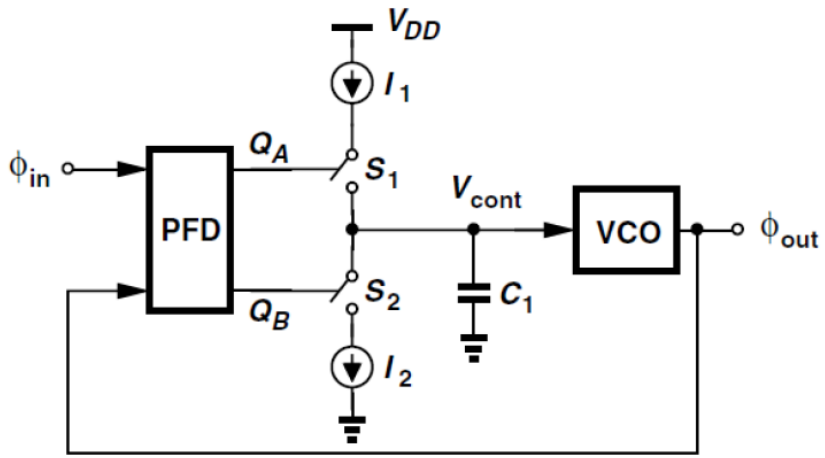


Fig. 9.2



- If the data rate of $\boldsymbol{\omega_{in}}$ is larger than the loop bandwidth of PLL, then the input voltage node of VCO can not follow the changing speed of the data, which would result in the distortion of demodulated FSK signal as shown in the figure on the right.

3. **For the charge pump PLL shown in Fig. 9.3, explain why the gain of PFD and charge pump is infinite. And how about the dead zone?**



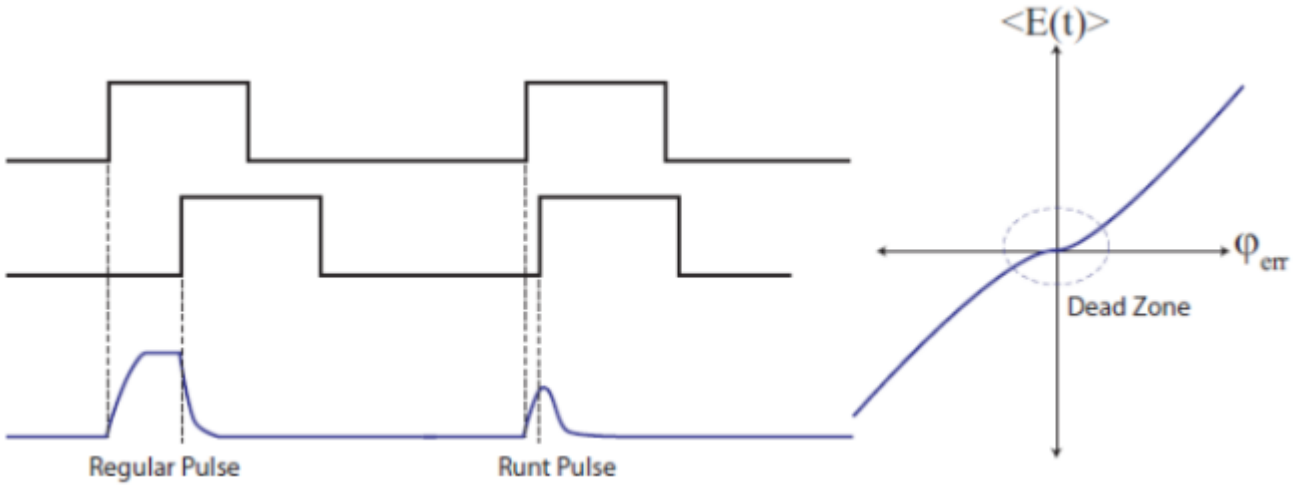


Fig. 9.3

- Because even if the phase difference between A and B is very small, they can continue to open S1 and S2 with A certain time difference, charging and discharging Vcont points continuously, making the voltage of Vcont points rise or fall.

- There is a finite rise/fall time that creates a dead-zone in the PFD response. Assume that the frequency/phase of the divider and reference are nearly matched so that the phase error is small. Ideally a shorter and shorter duty cycle signal would be generated on up or down, but as the duty cycle approaches the rise time of the pulses, the pulse amplitude will begin to decay, thus lowering the gain of the PFD. We see that the gain of the PFD flattens for small inputs.