EEM216A Design of VLSI Circuits and Systems **Fall 2015**
Prof. Dejan Marković Class Project

Due: Thursday, Dec 3 at 4pm

Class Project Submission Guideline

1. Project Sections

Your project contains the following sections, each of which requires a submission of a design:

(A) An unoptimized 32-channel engine with 4 section 10th order polynomial design

Once a one-channel design (as specified in the project specs) is completed, that module is placed 32 times in parallel for this design to accommodate for the 32 incoming ADC channels. Each of the 32 engines placed in parallel contains a 4 section 10th order polynomial design. This design is the same for everybody, i.e. no optimization techniques are employed (except of course for sane design practices). Therefore, a testbench is provided to aid you in the completion of your Verilog design. If you happened to start your design with optimization in mind (i.e. channel interleaved instead of 32 instances of single channel design) you can also submit that design for this part.

This design must also be pushed through logical synthesis and P&R.

(B) An optimized 32-channel engine with 4 section 10th order polynomial design

Because the ADC sample rate is much slower than the system clock, we recognize that the design from part (A) is highly inefficient (lots of unused clock cycles). Therefore, we would like to utilize some of the techniques discussed in class to obtain an energy-optimized design for our correction engine. Here is a list of optimization techniques that you can choose from (you can do both, but not any other techniques listed under extra credit):

- Interleaving (2x, 4x, 8x, 16x, 32x)
  - Have one core take care of multiple channels, using the extra time available between ADC samples.
- Voltage scaling
  - Scale down VDD to lower the power. The delay will increase but can be accommodated for with the extra time available between ADC samples. Note that this delay increase must be taken into account in synthesis.
  - The system clock frequency *cannot* be changed.
  - The delay vs. VDD information can be found here: `/w/class.1/ee/ee216a/ee216ata/setup/vdd_and_tp_curve.mat`

This design will be synthesized but P&R is not necessary. A portion of the grade for this part will be based on the functional design and the rest on the energy efficiency metric (more on that

later). The achieved energy efficiency metric will be compared to the efficiency figures of rest of the class. Note that if you are working on this project alone your energy efficiency score will be compared to the energy efficiency scores of other individual students. If you submit the design from part A you will get credit for the functionality but you will get 0 for the energy efficiency portion.

(C) (Extra Credit) Optional: further optimizations

An energy-optimized 32-channel engine with the following potential techniques employed:

- Power gating
  - Power gating some blocks that are not used can dramatically reduce the energy consumption during the "OFF" phase, especially if the duty cycle is low.
- Different number of sections
  - By changing the number of sections from 4 to something else, the polynomial order required may decrease, leading to additional power savings. Additional MATLAB analysis is necessary to determine the new polynomial order.
- Fixed point arithmetic
  - Replacing floating point with fixed point arithmetic can yield computational energy savings (the bitwidth must be large enough so that the performance is not sacrificed).
- Different polynomial computation method (Not Horner's method)
- Different non-linearity correction algorithm (Not polynomials)

Again, synthesis is required but P&R is not necessary.

5. Files in your Submission

Submit the following by email (ee216a@gmail.com) with "**Project submission: SID1 SID2**" in the subject line:

- **summary-*SID1_SID2*.pdf** Summary report (PPT template provided)
  For each design, create a new slide (don't worry about the chip photo if P&R is not required for that section). So, Part (A) should have one slide, and Part (B) should have one slide (Part (C) should have one slide if you have extra credit).
  Be sure to include your *SID* as part of file name
- **Part (A):**
  - **NLC.v** Your Verilog design (can be several files, be sure to include the wrapper file)
  - **NLC.tcl** The .tcl script you used for logical synthesis

- **NLC.vg** Gate-level Verilog from logical synthesis
- **NLC.sdf** Timing information from logical synthesis
- **NLC.gds** Layout of your design
- **timing-*SID*.txt** Post-synthesis timing report
- **area-*SID*.txt** Post-synthesis area report
- **power-*SID*.txt** Post-synthesis power report
- **timing-*SID*.txt** Post-layout timing report
- **area-*SID*.txt** Post-layout area report
- **power-*SID*.txt** Post-layout power report

- **Part (B):**
  - **NLC_opt.v** Your Verilog design (can be several files, be sure to include the wrapper file)
  - **NLC_opt.tcl** The .tcl script you used for logical synthesis
  - **NLC_opt.vg** Gate-level Verilog from logical synthesis
  - **timing_opt-*SID*.txt** Post-synthesis timing report
  - **area_opt-*SID*.txt** Post-synthesis area report
  - **power_opt-*SID*.txt** Post-synthesis power report
- **Part (C) (optional):**
  - **NLC_optec.v** Your Verilog design
  - **NLC_optec.tcl** The .tcl script you used for logical synthesis
  - **NLC_optec.vg** Gate-level Verilog from logical synthesis
  - **timing_optec-*SID*.txt** Post-synthesis timing report
  - **area_optec-*SID*.txt** Post-synthesis area report
  - **power_optec-*SID*.txt** Post-synthesis power report

7. Grading Metrics

The design objective is to minimize the energy consumed per sample (i.e. pJ/sample). Please minimize the energy while maintaining the system throughput. We use the metric of **Efficiency = Chip Power / ADC Sampling Rate** to evaluate the performance (since the ADC Sampling Rate is constant, this is equivalent to minimization of the chip power).

Your project will be graded based on following criteria (groups of 2 or more):

Functional 4 section 10th order design:	50%
Functional 4 section 10th order design with optimizations:	20%
Efficiency metric (of your most efficient design):	30%

If you don't have a project partner and working on it alone, you will be graded based on the following criteria.

Functional 4 section 10th order design:	60%
Functional 4 section 10th order design with optimizations:	20%
Efficiency metric (of your most efficient design):	20%

Extra credit point scales are as follows. If a technique is employed but does not yield a design that is more energy efficient, you will be given half the points.

Power gating:	5%
Different number of sections:	10%
Fixed-point implementation, wordlength optimization:	10%
A different method for computing the polynomial:	5%
A different algorithm for non-linearity correction:	20%