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High-Performance Organic Field-Effect Transistors and Inverters with Good Flexibility and Low Operating Voltage

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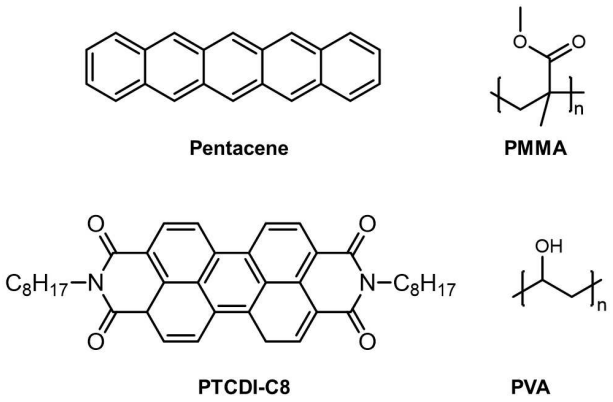
Organic field-effect transistors (OFETs) with good flexibility and low operating voltage, are of great meaning for the low power stretchable and wearable electronic devices. The operating voltage and flexibility are easily affected by the dielectric layers in the OFETs. Bilayer dielectrics comprising both high- and low-permittivity (*k*) insulating polymers, have been reported. The flexible bilayer dielectrics can combine the advantages of both insulating polymers, which are high charge carriers from low-k polymers and low operating voltage from high-*k* polymers. However, the effect of film thicknesses in the bilayer dielectrics on the OFET performance is seldom investigated. Here, bilayer dielectrics comprising high-*k* polyvinyl alcohol (PVA) and low-*k* polymethylmethacrylate (PMMA) were fabricated. And PVA/PMMA bilayers with three different PVA film thicknesses are carefully investigated. The 300 nm PVA/100 nm PMMA bilayer dielectric makes the pentacene OFETs show the highest hole mobility of 1.24 $cm^2V^{-1}s^{-1}$ and the corresponding inverters give a high voltage gain of 40 and a noise margin of 2.3 V (77% of 1/2 V_{DD}) at low operating voltage of 6 V. Both the pentacene transistors and the inverters still work properly under bending radium of 5.85 mm, proving the good prospects of the PVA/PMMA bilayer dielectric in practical applications.

Introduction

The research on flexible organic field-effect transistors (OFETs) is quite important for the development of stretchable and wearable electronic devices.[1–10] Low operating voltage is also of great meaning for the power saving.[11–16] The OFETs usually comprise source/drain electrodes, organic semiconductors (OSCs), dielectric layers, and gate electrodes.[17–22] Especially, the dielectric layers can easily affect the flexibility, operating voltage, and charge carrier mobility.[23–29] Dielectric layers with high-permittivity (*k*) usually correspond to a low operating voltage for the OFETs.[30–31] At present, most of the reported high-*k* dielectric layers with good flexibility are insulating polymers. But a high-*k* insulating polymer usually makes the OFETs show decreased carrier mobility, and increased threshold voltage, due to the existence of OH-group at the interface between the OSC and the insulating polymer.[31,32] To improve the interface, a second low-*k* insulating polymer can be overlapped on the top of the high-*k* insulating polymer.[18,31] Assisted with this bilayer dielectric, flexible OFETs with both high charge carrier mobility and low operating voltage can be realized. However, the effect of film thicknesses in the bilayer dielectrics on the OFET performance has seldom been reported.[33] In this manuscript, we made three bilayer dielectrics comprising high-*k* polyvinyl alcohol (PVA) and low-*k* polymethylmethacrylate (PMMA) as shown in Scheme 1.[34] It is found that the device performance of pentacene OFETs varies with the thicknesses of PVA layer while the thickness of PMMA is unchanged. The bilayer dielectric with 300 nm PVA/100 nm PMMA gives the highest hole mobility (μ_h) of 1.24 $cm^2V^{-2}s^{-1}$, current on/off ratio ($I_{on/off}$) of 2.3×10^4 and the threshold voltage (V_T) of −3.1 V at low operating voltage of 6 V. Organic complementary inverters were successfully fabricated and show good inverter performance. Moreover, both the above transistors and inverters still work properly under the bending radium of 5.85 mm.



Scheme 1. Chemical structures of two OSCs (left) and two insulating polymers (right).

Results and Discussion

Fabrication and Measurement of OFETs

Pentacene transistors with PVA/PMMA bilayer dielectrics were fabricated on flexible PET substrates as shown in Figure 1a & S1. The concentrations of PVA in deionized water were 40 (PVA_{40}), 50 (PVA_{50}) and 60 (PVA_{60}) mg/ml, while the concentration of

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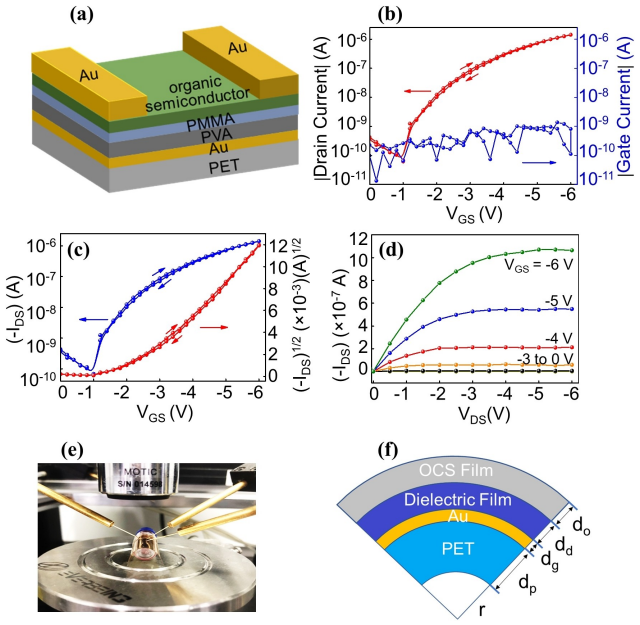

Figure 1. (a) The schematic diagram of a pentacene OFET, and its (b–c) transfer and (d) output curves, (e–f) bending state with a radius of 5.85 mm. The blue curve in (b) represents the gate current. The applied channel W/L is 200 μm/110 μm.

PMMA solution in toluene was kept as 5 mg/ml. Firstly, three PVA solutions were separately spin-coated at 1000 r/min for 30 s on the PET substrates with pre-deposited gate electrodes. The obtained thin films were then annealed at 100 °C for 60 min in a vacuum oven to remove the remaining water. Their film thicknesses are around 300, 420, and 510 nm with increasing concentrations. Secondly, the PMMA solution was coated on the top of the PVA layer at 3000 r/min for 30 s. The resulting PVA/PMMA bilayer dielectrics were also annealed in the vacuum oven at 80 °C for 60 min to remove the residual toluene. The thickness of PMMA is around 100 nm. The measured capacitances are 106.1 (k = 36.6), 77.6 (k = 32.5) and 44.2 (k = 22.7) nF/cm^2 at 1 Hz for three bilayer dielectrics PVA_{40}/PMMA, PVA_{50}/PMMA and PVA_{60}/PMMA (Table S1 & Figure S1). Their surface characterization by contact angle and atomic force microscopy (AFM) are shown in Figures S2–3. In contrast to the PVA films, the PVA/PMMA films have more hydrophobic and smoother surfaces, which is beneficial for the charge transport. Thirdly, 30 nm pentacene films were vacuum deposited onto the PVA/PMMA bilayer dielectrics. Fourthly, 30 nm Au films were vacuum evaporated as source/drain electrodes.

The pentacene transistors were then measured in the air. Among the three bilayer dielectrics, the PVA_{40}/PMMA bilayer shows the best OFET performance (Table 1). As shown in Figure 1b, the gate current (3.7×10^{-10} A) is four orders of magnitude lower than the drain current (1.52×10^{-6} A), implying that the bilayer dielectric has a good insulation property. Both the transfer and the output curves indicate typical p-type transport as shown in Figures 1c-d. And the PVA_{40}/PMMA bilayer makes the pentacene transistors have a low operating voltage of 6 V, the highest μ_h of 1.24 cm^{2}V^{-1}s^{-1} (1.10 cm^{2}V^{-1}s^{-1}), low V_T of −3.1 V, and high $I_{on/off}$ of 2.3×10^4. Relative to the SiO_2/OTS (octadecylsiloxane) dielectric (0.31 cm^{2}V^{-1}s^{-1}), the PVA_{40}/PMMA bilayer improves the μ_h of pentacene transistors by nearly four times (Table S2). The highest μ_h of both PVA_{50}/PMMA (1.04 cm^{2}V^{-1}s^{-1}) and PVA_{60}/PMMA (0.74 cm^{2}V^{-1}s^{-1}) bilayer dielectrics are much lower than that of PVA_{40}/PMMA bilayer dielectric (Table S2). The PVA_{30}/PMMA bilayer dielectric was also studied but it had too large gate current to be used in the OFETs. The N, N′-dioctyl-3,4,9,10-perylene dicarboximide (PTCDI-C8, Scheme 1) OFETs with PVA_{40}/PMMA bilayer dielectric were also fabricated and measured (Figure S4&Table S3). The PTCDI-C8 also works at low operating voltage of 6 V, and displays the highest electron mobility (μ_e) of 0.12 cm^{2}V^{-1}s^{-1} (0.10 cm^{2}V^{-1}s^{-1}), high $I_{on/off}$ of 8.7×10^4 and low V_T of 2.1 V. In comparison to the SiO_2/OTS dielectric (1.61×10^{-3} cm^{2}V^{-1}s^{-1}), the PVA_{40}/PMMA improves the μ_e of PTCDI-C8 by two orders of magnitude. X-ray diffraction (XRD) and AFM characterization indicates that both OSC films have high crystallinity (Figures S5–6), which are consistent with their high charge carrier mobility. In summary, the PVA_{40}/PMMA bilayer dielectric can obviously improve the OSC transistor performance.

Table 1. Performance summary of pentacene OFETs with two W/L ratios of 200 μm/110 μm and 8800 μm /80 μm. The capacitance is measured at 1 Hz.

Dielectric	W/L	Bending State	μ_h (cm^2 V^{-1} s^{-1})	$I_{on/off}$ ($\times10^4$)	V_T (V)
PVA_{40}/PMMA	200/110	Before Bending	1.24 (1.10)[a]	2.3	−3.1
		Bending	1.09 (0.93)[a]	1.4	−3.0
		Removed Bending	1.20 (1.07)[a]	1.5	−3.2
	8800/80	Before Bending	0.029 (0.024)[a]	2.9	−2.4
		Bending	0.028 (0.023)[a]	1.5	−2.4
		Removed Bending	0.030 (0.025)[a]	1.2	−2.3

[a] The brackets indicate the average values among 20 devices.

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We then measured the OFET performance under bending state.[35–37] Owing to the good flexibility of PET substrates, the pentacene OFETs can be easily mounted on a vial with an outer radius (r) of 5.85 mm as shown in Figure 1e. Then, the tensile bending strain of the inverter is analyzed according to the model shown in Figure 1f. The tensile bending strain (ε) appears at the outer surface of the transistors expressed by the following equation:

$$\varepsilon = \frac{d_o + d_d + d_g + d_p}{2r} \quad (1)$$

where d_o (30 nm), d_d (400 nm), d_g (30 nm) and d_p (250 μm) are the thickness of pentacene/PTCDI−C8 film, dielectric film of PVA_{40}/PMMA, gate electrode and the PET substrate, respectively. The ε of bent OFETs on the vial is calculated to be 2.14%. Under the bending state, the pentacene OFETs give the highest μ_h of 1.09 $cm^2V^{-1}s^{-1}$ (0.93 $cm^2V^{-1}s^{-1}$), which is a little lower than that of device before bending (Table 1, Figure S7a). After the bending is removed, the highest μ_h of the pentacene OFETs recovers to 1.20 $cm^2V^{-1}s^{-1}$ (1.07 $cm^2V^{-1}s^{-1}$). The bent PTCDI-C8 transistors were also measured as shown in Table S3 & Figure S7b. The highest μ_e shows a small decrease to 0.094 $cm^2V^{-1}s^{-1}$ (0.072 $cm^2V^{-1}s^{-1}$) under bending state and can restore to 0.117 $cm^2V^{-1}s^{-1}$ (0.094 $cm^2V^{-1}s^{-1}$) after the bending is removed. In short, both the p-type pentacene and n-type PTCDI-C8 transistors can work well at bending state at low operating voltage of 6 V.

Fabrication and Measurement of Organic Inverters

Complementary inverters using pentacene/PTCDI-C8 OFETs with PVA_{40}/PMMA bilayer dielectric were then fabricated (Figures 2a-b & S1).[38–46] In order to balance the OFET performance of two OSCs and to obtain high inverter performance,[32,47–50] we adjusted the W/L ratio of transistors as 8800 μm/80 μm (Tables 1 & S3). The obtained highest μ_h/μ_e, V_T, $I_{on/off}$ are 0.029 $cm^2V^{-1}s^{-1}$, −2.4 V, 2.9×10^4 for pentacene and are 0.022 $cm^2V^{-1}s^{-1}$, 2.6 V, 4.5×10^4 for PTCDI-C8. The voltage transfer curve (VTC) is shown in Figure 2c with a supply voltage (V_{DD}) between 3 and 6 V. The VTC is measured in both sweep direction and ignorable hysteresis can be seen, indicating that the PVA_{40}/PMMA show a good insulation property. One important performance indicator of inverters is the noise margin (NM), which represents the highest noise signal that can't cause the malfunction of inverters.[51–54] Both high-level (NM_H) and low-level (NM_L) NM values should be higher than 10% of the 1/2 V_{DD}, which are calculated by the following equation:

$$NM_H = V_{OH} - V_{IH} \quad (2)$$

$$NM_L = V_{IL} - V_{OL} \quad (3)$$

Where the parameters V_{IH}, V_{IL} represent the highest and lowest input voltages and the parameters V_{OH}, V_{OL} indicate the highest and lowest output voltages. These four parameters can be obtained by the usage of the maximum equal criteria method.[32,55] When V_{DD} is 6 V, the calculated NM_H and NM_L of this inverter are 2.3 and 2.4 V, which reach 77% and 80% of 1/2 V_{DD}, respectively (Table S4).[33] Both NM_H and NM_L values are high enough for noise resistance. The voltage gain is another important parameter and indicates the sensitivity of voltage conversion. The inverters in this manuscript show a high voltage gain of 40 when the V_{DD} is 6 V (Figure 2d).

The switching voltage (V_M) is also an important parameter for the inverter performance.[32] The V_M values are related with the organic transistors in the inverters, which can be calculated according to the following equations:

$$V_M = \frac{\sqrt{\beta_e/\beta_h}V_{Te} + (V_{DD} - V_{Th})}{1 + \sqrt{\beta_e/\beta_h}} \quad (4)$$

$$\beta_e = \mu_e C_i W/L \quad (5)$$

$$\beta_h = \mu_h C_i W/L \quad (6)$$

where V_{Te}, V_{Th} and β_e, β_h are the threshold voltage and transconductance parameters for p- and n-type transistors (Figures S8–9); C_i is the dielectric capacitance. At $V_{DD}=6$ V, the calculated V_M is 3.09 V, which nearly equals the ideal $V_M=1/2$ V_{DD}.[30]

We then measured the inverter performance under bending state ε = 2.14% (Figure 1e).[50,56–58] As shown in Figures 3a-b, there is a small shift of V_M (3.6 V) away from 1/2 V_{DD}, and a small decrease of the voltage gain (26) at $V_{DD}=6$ V. When the bending of inverter is removed, the V_M and voltage gain values recover to 3.4 V and 33. Thus, the inverter can still work properly without severe degradation under bending condition.

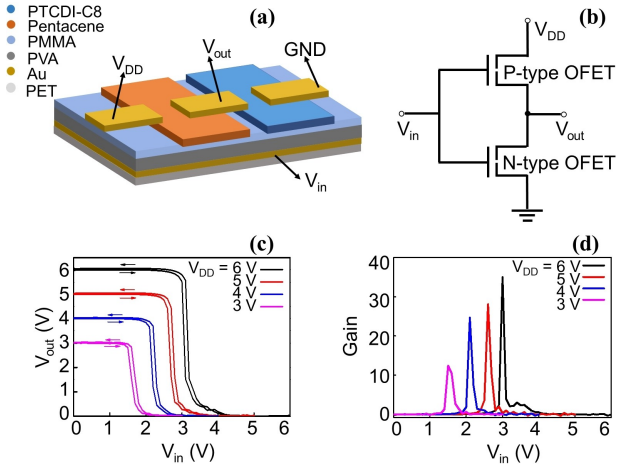

Figure 2. (a) Schematic diagram and (b) schematic circuit of complementary-like inverter. (c) VTC and (d) corresponding voltage gains in the V_{DD} range of 3–6 V. The applied channel W/L is 8800 μm/80 μm.

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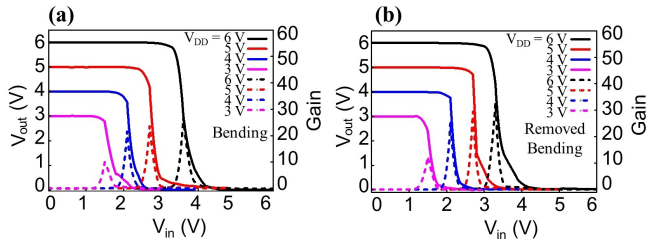

Figure 3. VTC and voltage gains of a CMOS – like inverter with (a) bending and (b) removed bending.

Conclusions

In summary, a bilayer dielectric comprising two insulating polymers PVA and PMMA, is applied in the flexible OFETs and organic inverters. By adjusting the film thickness of this bilayer dielectric, the PVA_{40}/PMMA bilayer dielectric can obviously improve the performance of pentacene transistors. Assisted by this bilayer dielectric, the pentacene transistors show the highest μ_h of 1.24 $cm^2V^{-1}s^{-1}$ (0.31 $cm^2V^{-1}s^{-1}$ for SiO_2/OTS dielectric). The corresponding complementary inverters display good voltage transfer characteristics, with a high voltage gain of 40 and a noise margin of 2.3 V (77% of 1/2 V_{DD}) at V_{DD} = 6 V. Both the transistors and inverters have a low operating voltage of 6 V and can still work properly under the bending strain of 2.14%. The above results indicate the good prospects for the application of the PVA_{40}/PMMA bilayer dielectric in integrated circuits in the future.

Experimental Section

Preparation of PET Substrates

PET (2.5×2.5 cm^2) substrates were ultrasonicated in deionized water, acetone (Greagent, ≥99.5%) and isopropanol (Greagent, ≥99.7%), and then dried with nitrogen blowing. A 30 nm Au film was then vacuum evaporated onto the PET surface at the rates of 0.1 Å/s under a pressure of 10^{-4} Pa.

Fabrication of Pentacene/PTCDI-C8 OFETs

30 nm Pentacene (sublimed) and PTCDI-C8 (≥98.0%) films were thermally evaporated onto the PVA/PMMA bilayer dielectrics at the rates of 0.2 Å/s and 0.3 Å/s, respectively. 30 nm Au films were then thermally evaporated as source/drain electrodes at the rates of 0.1 Å/s at a pressure of 10^{-4} Pa through a shadow mask with channel width (W)/channel length (L) ratio of 200 μm/110 μm. The resulting OFETs were measured with Keithley 4200 SCS.

Fabrication of Organic Inverters

Firstly, 30 nm Au film was vacuum evaporated on the PET substrates as gate electrodes. Secondly, the PVA_{40}/PMMA bilayer was spin-coated on the gold surface and annealed at 80 °C for 60 min. Thirdly, 30 nm Pentacene and 30 nm PTCDI-C8 films were thermally evaporated at deposition rates of 0.2 Å/s and 0.3 Å/s, respectively. Finally, 30 nm Au was deposited as source/drain electrodes through a shadow mask at a pressure of 10^{-4} Pa through a shadow mask with channel W/L ratio of transistors as 8800 μm/80 μm. All the inverters were measured in the air.

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Conflict of Interests

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords: Bilayer dielectric · Electronic devices · Flexibility · Polymers · Semiconductors

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