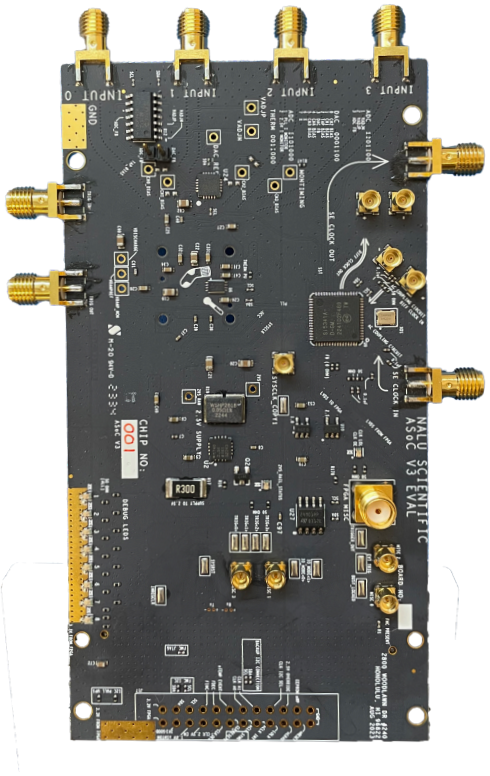
# Product Sheet: ASoCv3 EVBr

**Analog to Digital Converter System on a Chip**

## Features

- Event-based Waveform Digitizer
- Sampling Rate: 3.2 GSa/s / channel
- 4 input channels
- Timing precision < 30ps, (nominal < 100ps)
- ADC input range: 0-2.5 V
- AC-coupled analog inputs
- Input analog bandwidth: 850 MHz
- RMS noise: < 1.89 mV
- Up to 16,256 samples/channel
- Programmable triggering
- Clock/trigger in/out for multi-board sync




## Applications

- Particle and Nuclear Physics
- Radar and LiDAR
- Medical imaging
- Plasma/Fusion Detection
- NP/HEP experiments
- Fast timing detectors using PMT/SiPM
- Quantum sensors and Qubit readout

## 1. Description

The ASoCv3 Eval Board is a low-power, event-based waveform digitizer designed for users who require precise and high-speed data acquisition. The evaluation board supports continuous time-domain sampling across four independent input channels, with a sampling rate of 2.4-3.2 GSa/s per channel (nominal 3.2 GSa/s). Digitization and readout are performed only when an internal or external trigger event is detected. Each channel is also capable of independent triggering for analog self-triggering, as well as coincidence and multi-board triggering options. Connection to the board is available over UART-over-USB or Ethernet. The ASoCv3 board operates with a nominal channel-to-channel timing precision of 100ps, which can be further calibrated to better than 30ps. For high-speed data acquisition and readout applications, the ASoCv3 board

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provides a cost-effective and versatile solution.

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# 2. I/O Specifications

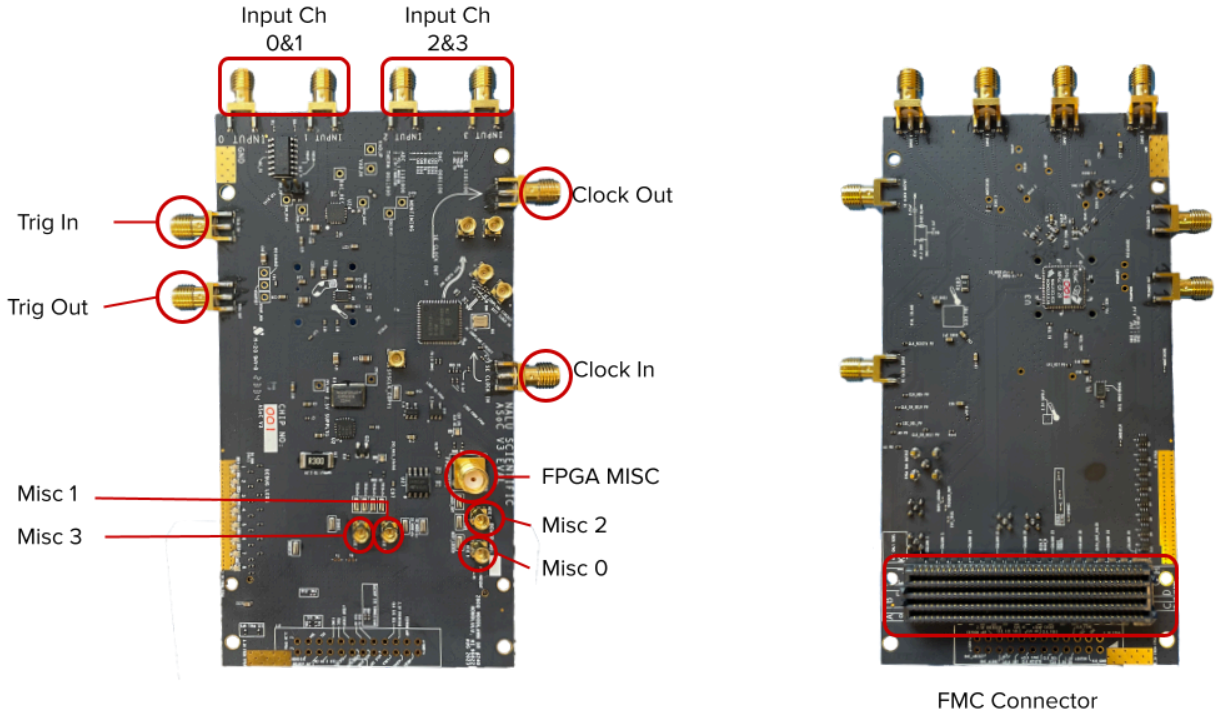


***Figure 1:*** *Available board I/O with and without enclosure.*

| Port | Description | Connector | Rating |
|---|---|---|---|
| **Ch 0–3** | RF Input for Channels 0-3 (AC-Coupled) | SMA | 0–2.5 V |
| **Clock In** | External clock synchronization | SMA | LVCMOS 2.5 |
| **Clock Out** | Configurable clock output for synchronization. | SMA | LVCMOS 2.5 |
| **Trig In** | External Trigger input (Not used) | SMA | LVCMOS 2.5 |
| **Trig Out** | Trigger output | SMA | LVCMOS 2.5 |
| **FPGA Misc** | External Trigger input (Via FPGA) | SMA | LVCMOS 2.5 |
| **Misc 0–3** | FMC debug connectors (Not used) | MMCX | 0-2.5V |
| **FMC** | Specs available on request | FMC | - |

***Table 1:*** *Connection description and rating*

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# 3. General Specifications

## 3.1 Board Specifications

| | |
|---|---|
| **Power Requirement** | 12 VDC ±5% @ 3A |
| **Dimensions** | 140mm x 70mm x 36.5 mm (w/ standoffs) |
| **Weight** | 54g (evaluation board only) |
| **Temperature Range** | 20° to 50° C |
| **Humidity Range** | 5% to 80% RH non-condensing (recommended |
| **Sampling Rate** | 3.2 GSa/s |

***Table 2:*** *General physical specifications for the ASoCv3 EVB*

## 3.2 System Specifications

| | |
|---|---|
| **PC Connectivity** | UART-over-USB up to 1 Mbps<br>Gigabit Ethernet |
| **PC Connector Type** | micro-USB (UART-over-USB)<br>Ethernet RJ45 |
| **Software** | NaluScope (NaluDaq: Python package available on PYPI) |
| **PC Requirement** | RAM: 4 GB<br>Storage: 500 MB (Application only)<br>Processor: Intel Core i3 4370 or Equivalent |

***Table 3:*** *System requirements for the ASoCv3 EVB*

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# 4. Triggering Scheme:

## 4.1. Self-Triggering

Triggering can be performed based on the signal level (self-triggering). Each channel contains an internal discriminator with a programmable threshold, which can be used to generate an internal trigger for all 4 channels of the ASoCv3 chip. Furthermore, taking advantage of a mode called RoI (Region of Interest), the user can opt to acquire only portions of the waveform that cross the programmable threshold, regardless of the state of the other channels.

## 4.2. External Triggering

The ASoCv3 board has an external input connector through which users can supply a pulse trigger signal, instead of relying on the hardware's internal triggering circuitry. Users are able to trigger the board by configuring NaluScope to select the board's trigger mode. When the external trigger pin detects a pulse, the board digitizes the waveform within specified intervals relative to the trigger edge.

| Waveform | $V_{range}$ | Pulse Width (min) | $V_{offset}$ | Maximum Repetition Rate* |
|---|---|---|---|---|
| Pulse | 0 - 2.5V | 10 ns | 0V | Up to 20 KHz |

** Trigger rate is limited by the data transfer rate*

***Table 4:*** *Configuration of External Trigger Signal*

## 4.3. Software Triggering

Users are able to "force trigger" via a software command, which toggles the trigger pin high for a programmable number of clock cycles. Software triggering shares logic with the external trigger input and can be used interchangeably.

## 4.4. Multi-Board Triggering

For users who desire to acquire data from more than 4 channels, a multiboard configuration is possible. The external trigger pin can be split, shared, and used to simultaneously trigger multiple boards. The board also allows cascading trigger signals by using the trigger-out pin, as shown below in Figure 2. Clocks can also be cascaded.

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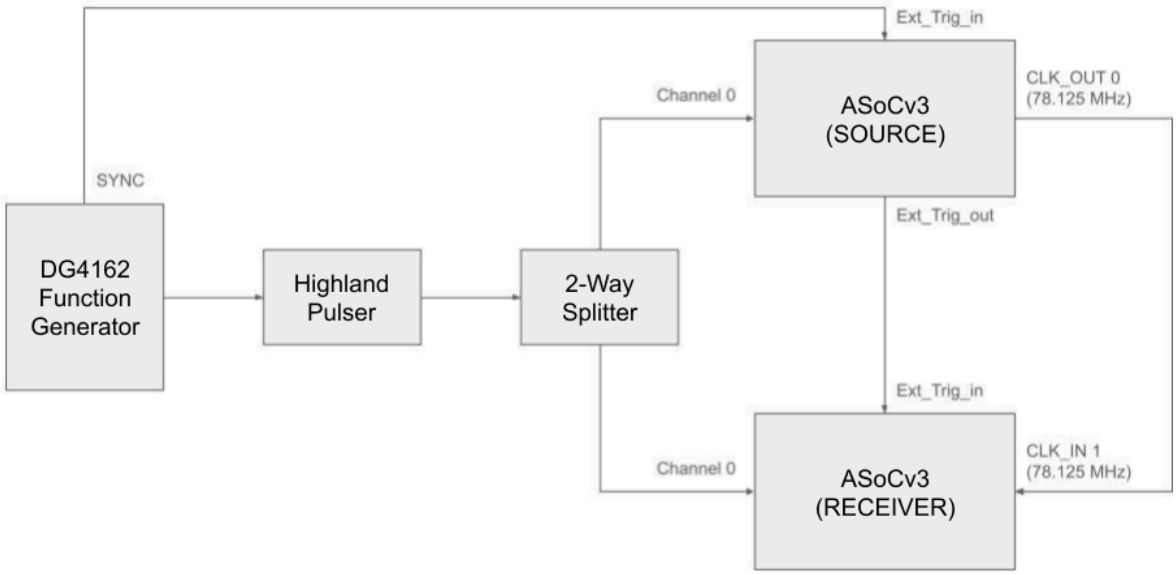


***Figure 2:*** *Example block diagram of multi-board connection with cascaded trigger and clock signals.*

## 4.5. Coincidence Triggering

This is an advanced mode of operation with a combination of software configuration and firmware operation. The ASoCv3 ASIC is capable of coincidence triggering; however, our current ASoCv3 firmware and software do not yet fully support this functionality.

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# 5. Connection Diagram

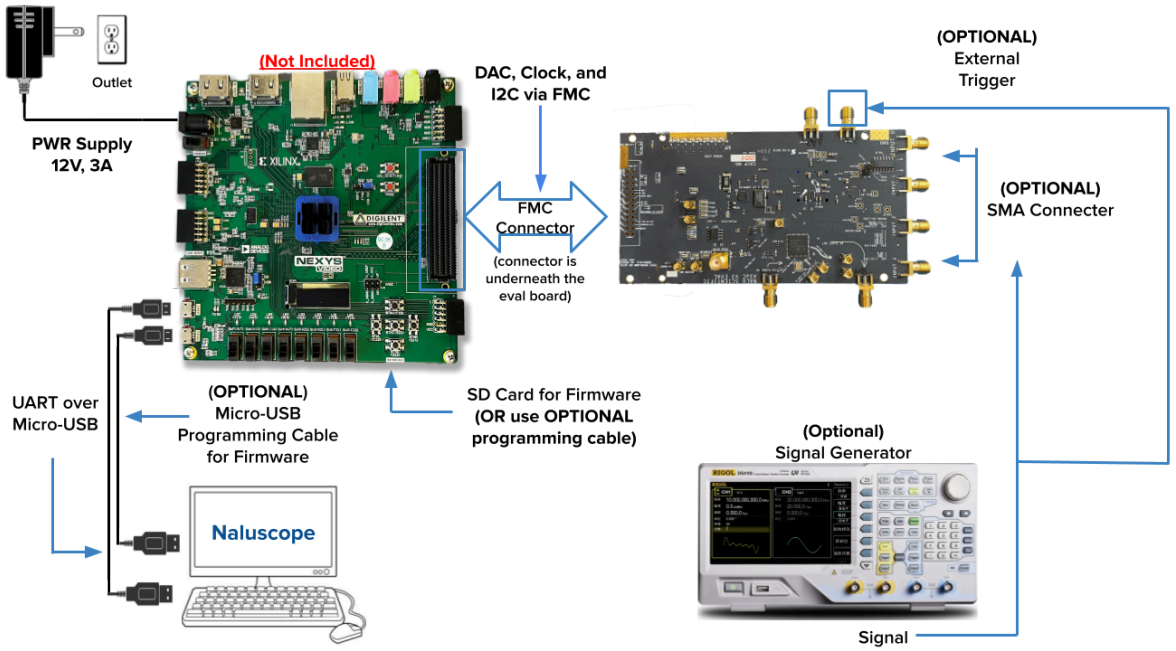


***Figure 3:*** *Example connection diagram*

The diagram above illustrates hardware configurations that can be utilized with the ASoCv3. In this setup, the signal generator, shown in the bottom left, can be substituted with any suitable signal source as per the user's requirements.

There are two options to establish communication between the ASoCv3 and a computer. Option 1 is via USB (UART-over-USB, 115.2 kbaud or 1 Mbps). The USB port also serves as a JTAG interface, but this is only required when re-programming the FPGA firmware. The board ships with the FPGA already flashed, so no re-programming is required for operation. Option 2 is via Ethernet (950 Mbps over UDP), which can be configured either as a direct peer-to-peer connection or through an existing network. For applications demanding high-speed functionality, an Ethernet connection is required.

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# 6. Board Outline and Dimensions

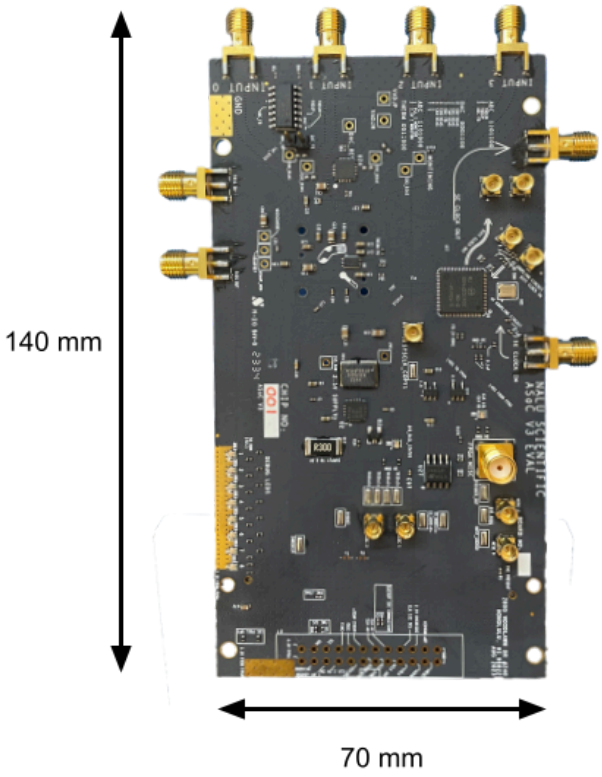


***Figure 4:*** *Dimensions for the ASOCv3*

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## 7. Revision History

**NOTE:** Page numbers for previous revisions may differ from page numbers in the current version.

| Version Number | Date | Author | Remarks |
|---|---|---|---|
| 1.0 | 10/13/2025 | S. Chu & P. Legaspi | First Version |

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