2020 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC) | 978-1-7281-7693-2/20/$31.00 ©2020 IEEE | DOI: 10.1109/NSS/MIC42677.2020.9507893

Measurement results for the ASoC V3: A High Performance Waveform Digitizer System-on-Chip

Isar Mostafanezhad, *Member IEEE*, Luca Macchiarulo, Gary Varner, *Member IEEE*, Benjamin Rotter, *Member IEEE,* Dean Uehara, *Member IEEE,* Christopher Chock

***Abstract*– Based on the requirements for compactness, low power, high timing resolution, and robustness to pile-ups for modern particle imaging based identification detectors, a new multi-channel waveform digitizer, the ASoC (Analog to digital converter System on a Chip), has been designed and fabricated. Measurements of analog and digital performance of the revisions 2 and 3 of the asic will be reported.**

***Keywords*: System-on-chip, data acquisition, front-end electronics, waveform digitization, region of interest, fast timing**

I. Introduction

Data acquisition systems for state of the art imaging based particle identification detectors are expected to handle large numbers of channels, high accuracy timing, and operate under limited spatial and power constraints. In many applications [1][2], full waveform digitization is considered necessary to guarantee the required timing resolution and avoid undesirable degradation due to time walk, pile-up and other sources of noise. Such acquisition systems are problematic in that the data volume and the computational requirements push the power, cost, and space limits even further. With this in mind, the ASoC integrated circuit has been designed to: (i) perform multi-channel waveform sampling, storage, and digitization using switched capacitor arrays, (ii) allow for smart self-triggering and data collection, (iii) perform on-site tuning and initial signal processing, and (iv) communicate properly formatted waveform data in a simple protocol.

The device has been fabricated in a 250 nm process. The results of measurements on the last 2 revisions of the chip will be reported. Figure 1 shows a die photograph with high-level module annotation.

Manuscript received December 20, 2020. This work was partially funded under the U.S. DOE SBIR DE-SC0015231 grant.

I. Mostafanezhad is the founder and CEO of Nalu Scientific, LLC, 2800 Woodlawn Dr. Ste #240, Honolulu, HI 96822 USA.

L. Macchiarulo is with Nalu Scientific, LLC, 2800 Woodlawn Dr. Ste #240, Honolulu, HI 96822 USA.

G. Varner is with the University of Hawaii at Manoa, 2505 Correa Rd., Honolulu, HI 96822 USA.

B. Rotter is with Nalu Scientific, LLC, 2800 Woodlawn Dr. Ste #240, Honolulu, HI 96822 USA.

D. Uehara with Nalu Scientific, LLC, 2800 Woodlawn Dr. Ste #240, Honolulu, HI 96822 USA.

C. Chock with Nalu Scientific, LLC, 2800 Woodlawn Dr. Ste #240, Honolulu, HI 96822 USA.

II. Design Improvements

The **timing generator** derives all required internal signals from a reference clock. The analog values in the **sampling array** are periodically transferred to the **storage array.** This keeps the analog values in analog form to wait for a triggered digitization of selected portions of the array controlled by the **digital control.** Digitization is performed by a Wilkinson **ADC** that operates in parallel on all channels and 64 samples per channel to speed up operation. The **digital control** orchestrates the entire operation of the chip, and simplifies its interaction with the back end electronics. Some of its major functions are:

(i) Controls the portion of the storage array that is written during operation (avoiding overwriting of currently digitized samples).

(ii) Keeps track of internal triggers marking region of interest (ROI) for digitization.

(iii) Allows external access to internal parameters and monitoring data (trigger and timing scalers).

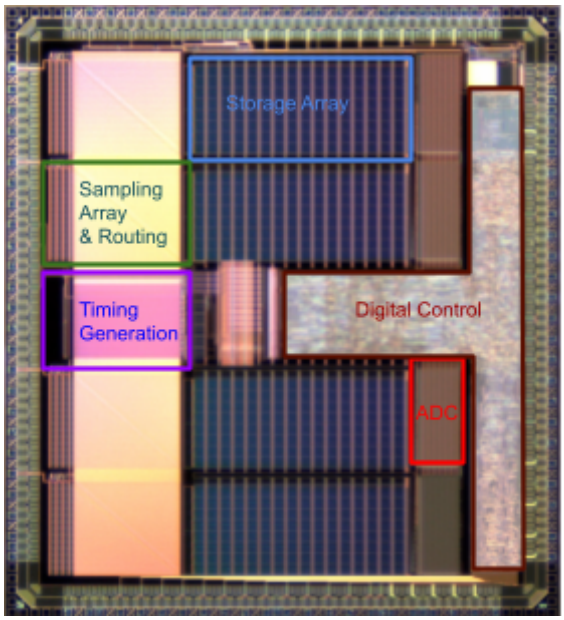

Fig. 1. Die photograph of ASoCv3 asic. Overall dimensions are 4.73mm x 5.27mm=24.9 mm^2.

(iv) Performs signal conditioning to correct for large sample-to-sample fixed offsets ("pedestals").

(v) Allows different operational modes for readout (fixed array position, relative to trigger, region of interest mode), triggering (external, software, autonomous with coincidence or disjunction of trigger signals).

(vi) Packetizes and sends the results in timestamps headers in either parallel or serial interfaces (rev. 3 downlink speed up to 500 Mb/s).

(v) Uses a sophisticated mechanism to allow multi-hit events and avoid deadtime (rev. 3).

Table I below summarizes the measured features of the fabricated chip.

A. Voltage Noise/RMS:

As mentioned previously, the individual samples are subject to large recording offsets ("pedestals") that need to be measured, recorded and corrected. The residual noise errors in voltage conversion after this correction has been measured for each storage sample position. The typical errors are normally distributed with a standard deviation of approximately 1.0 mV (2.5 ADC counts), as shown in Figure 2.

B. Sampling Speed:

ASoC can operate on different sampling frequencies, thanks to the internal generation of all relevant timing strobes. It is sufficient to control the frequency of the reference clock and therefore possible to automatically adjust the sampling frequency. The sampling speed of the ASoC that proved to be functional was measured between 2.4 to 3.6 GSa/s. Preliminary results seem to indicate that higher sampling rates, possibly up to 4GSa/s, are possible, but have not been demonstrated yet.

TABLE I. FONT SIZES AND FORMAT

Parameter	**Spec (measured)**
Sample rate	2.4-3.6GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Resolution	12 bits*
Supply Voltage	2.5V
RMS noise	~1 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps**
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

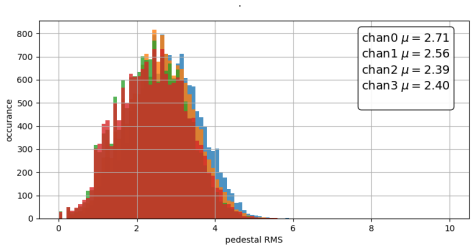

Fig. 2. Noise residuals after pedestal subtraction - typical ~2.5 counts = 1.0mV

III. MEASUREMENT RESULTS

A. Accuracy/Sample jitter:

To measure the achievable timing accuracy of the ASoC, a timing measurement was performed. Two channels received the 2 outputs of a splitter, one of which had been delayed with respect to the other through the use of a longer cable. Repeated event acquisitions result in the pair of waveforms to appear in a random array position (as the input signal is not synchronized with the reference signal to the chip), but their relative position was unchanged. To achieve good timing results, a timing calibration needed to be performed. Using correlation between the waveforms, the delay was estimated for each of the events, and the results were plotted in Figure 3. The standard deviation of the measurement was 22.5ps.

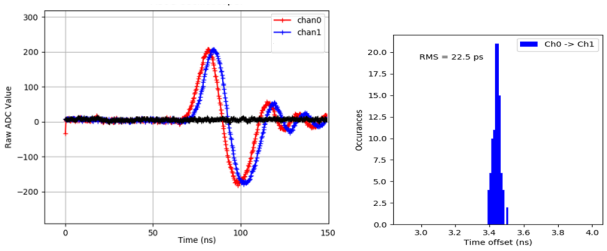

Fig. 3. Timing measurement

B. Other tests:

Among the other chip features that have been tested are the analog bandwidth (850MHz), power dissipation (as low as 120mW/channel with good parameter tuning), and some of the digital operations. Of particular relevance, the ROI mode, which allows for the exploration of a large portion of the storage array but a targeted digitization of signals over threshold, was proven functional, as shown in Figure 4.

IV. SUMMARY

ASoC V3 is expected to be back from fabrication and tested early June 2020.

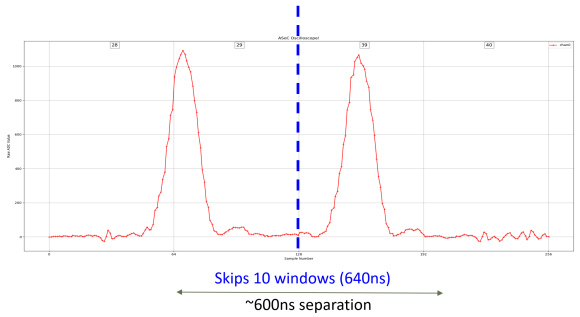

Fig. 4. Region of Interest (RoI) readout mode showing two 10ns pulses separated by ~600ns and are automatically readout while skipping the no-signal in between.

References

[1] G. Varner, M. Andrew, L. Macchiarulo, K. Nishimura, L. Wood The IRSX ASIC for the Belle II Imaging Time of Propagation Detector, IEEE NSS conference 2015, San Diego, CA

[2] "Advanced Waveform Sampling ASICs for the Discovery Frontier", Gary S. Varner, 2016 DPF Instrumentation Prize Symposium, CPAD Instrumentation Frontier Meeting 2016: New Technologies for Discovery II, CalTech, Oct. 8, 2016