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11	OPENSDA

Revisions

Rev	Description	Date	Approved
X1	Original Release	5-17-2013	Eric Zhang
X2	Riew Update	5-23-2013	Eric Zhang
X3	Change Power System	6-4-2013	Eric Zhang
X4	Change HAPSTRAK II	6-13-2013	Eric Zhang
A	Release	7-3-2013	Eric Zhang

X-TWR-FPGA-A7

Microcontroller Solutions Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: X PUBI:

Designer: Qiao Jun	Drawing Title: X-TWR-FPGA-A7		
Drawn by: Qiao Jun	Page Title: TITLE PAGE		
Approved: Eric Zhang	Size D	Document Number SCH-27942 PDF: SPF-27942	Rev A
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1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 10%, 16V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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ICAP Classification: FCP: ___ FIJO: X PUBI: ___

Drawing Title: **X-TWR-FPGA-A7**

Page Title: **NOTES**

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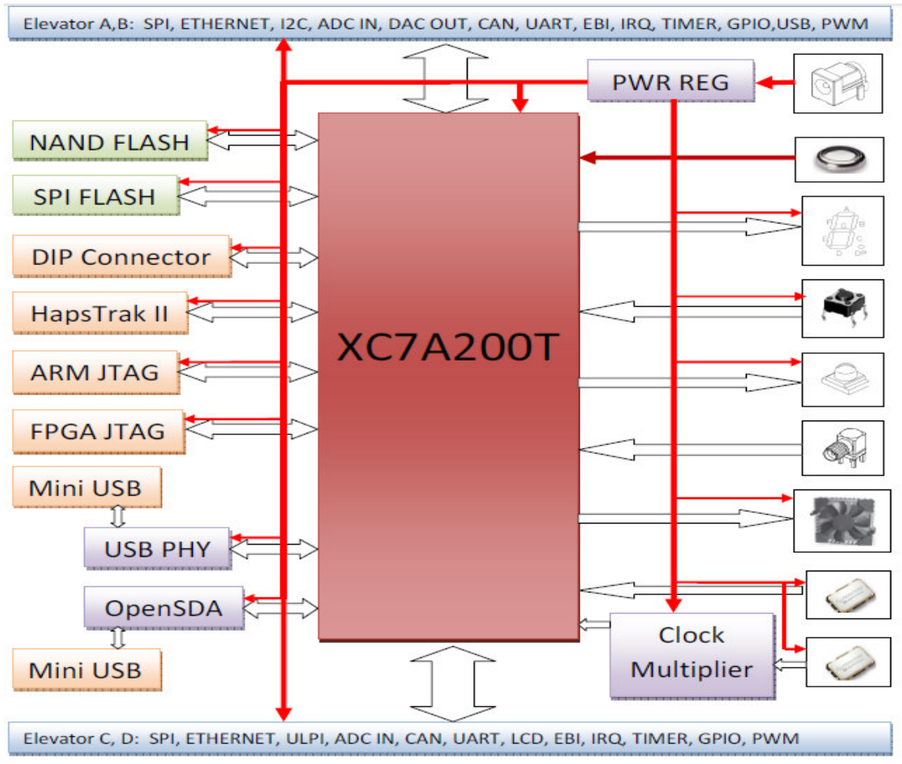

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **X-TWR-FPGA-A7**

Page Title: **BLOCKS**

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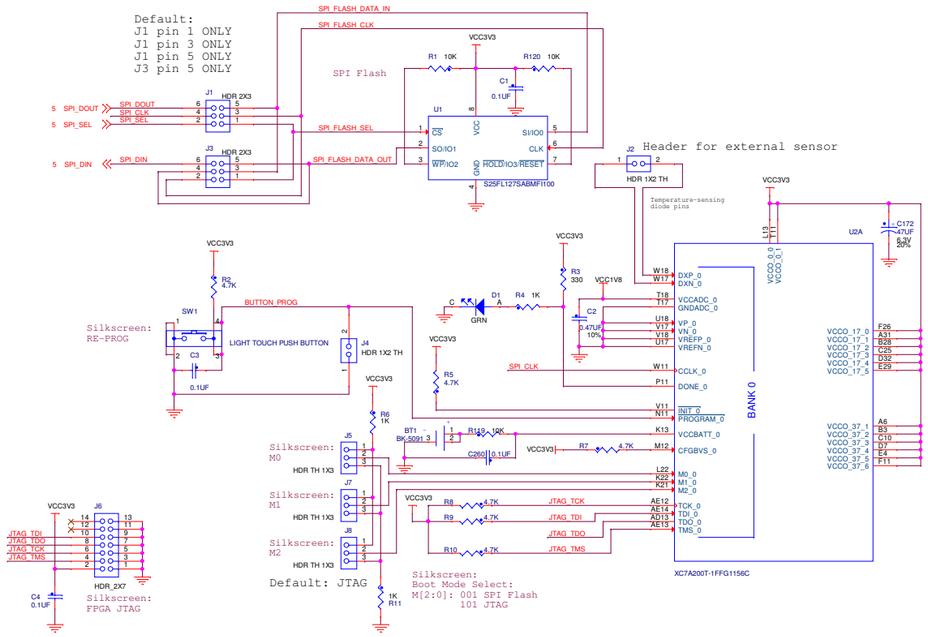
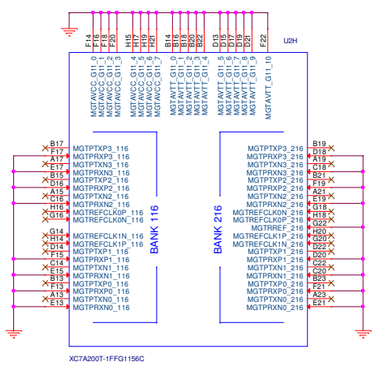
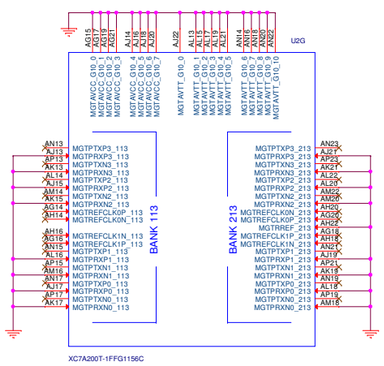
When Burn SPI Flash,
Do Shunt J1:1-2;3-4;5-6 J3:5-6
J3.1:CS J3.2:CLK J3.3:MOSI J3.4:MISO
When Not Burn SPI Flash,
Do Shunt J1:1-2;3-4;5-6 J3:5-6







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ICAP Classification:	FCP: ___	FIJO: X	PUBS: ___
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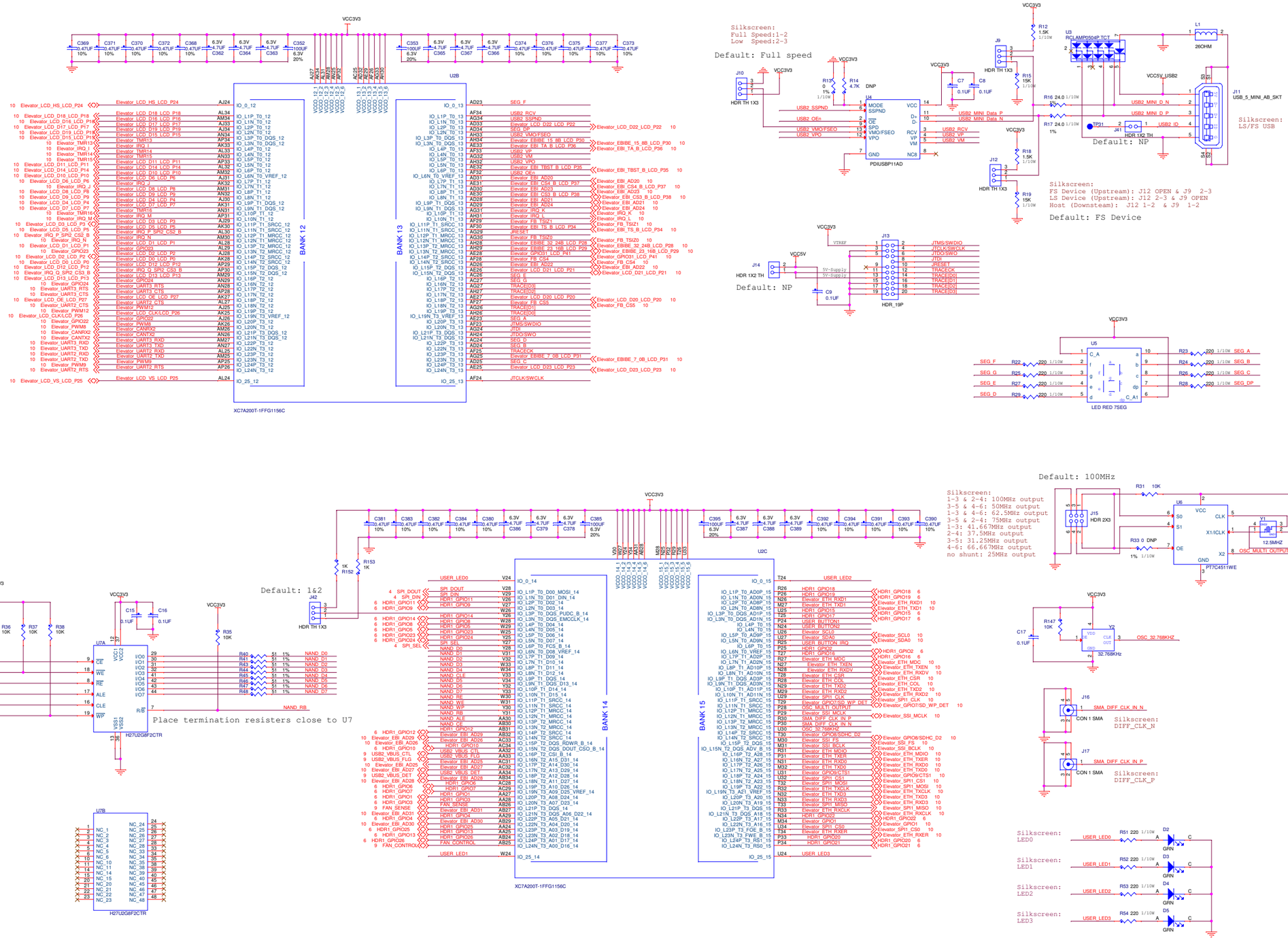

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ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	X-TWR-FPGA-A7		
Page Title:	FPGA BANK12, 13, 14, 15		
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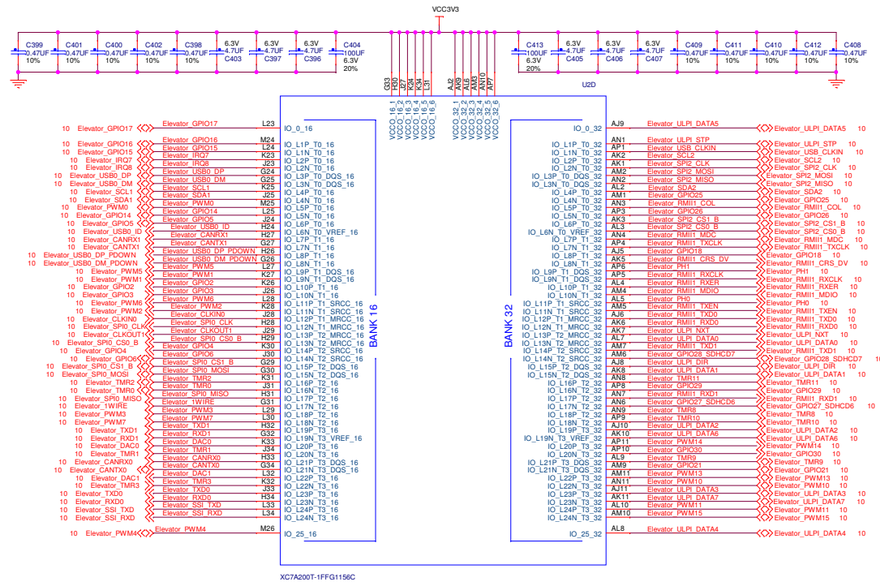

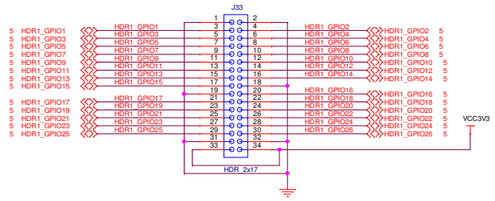

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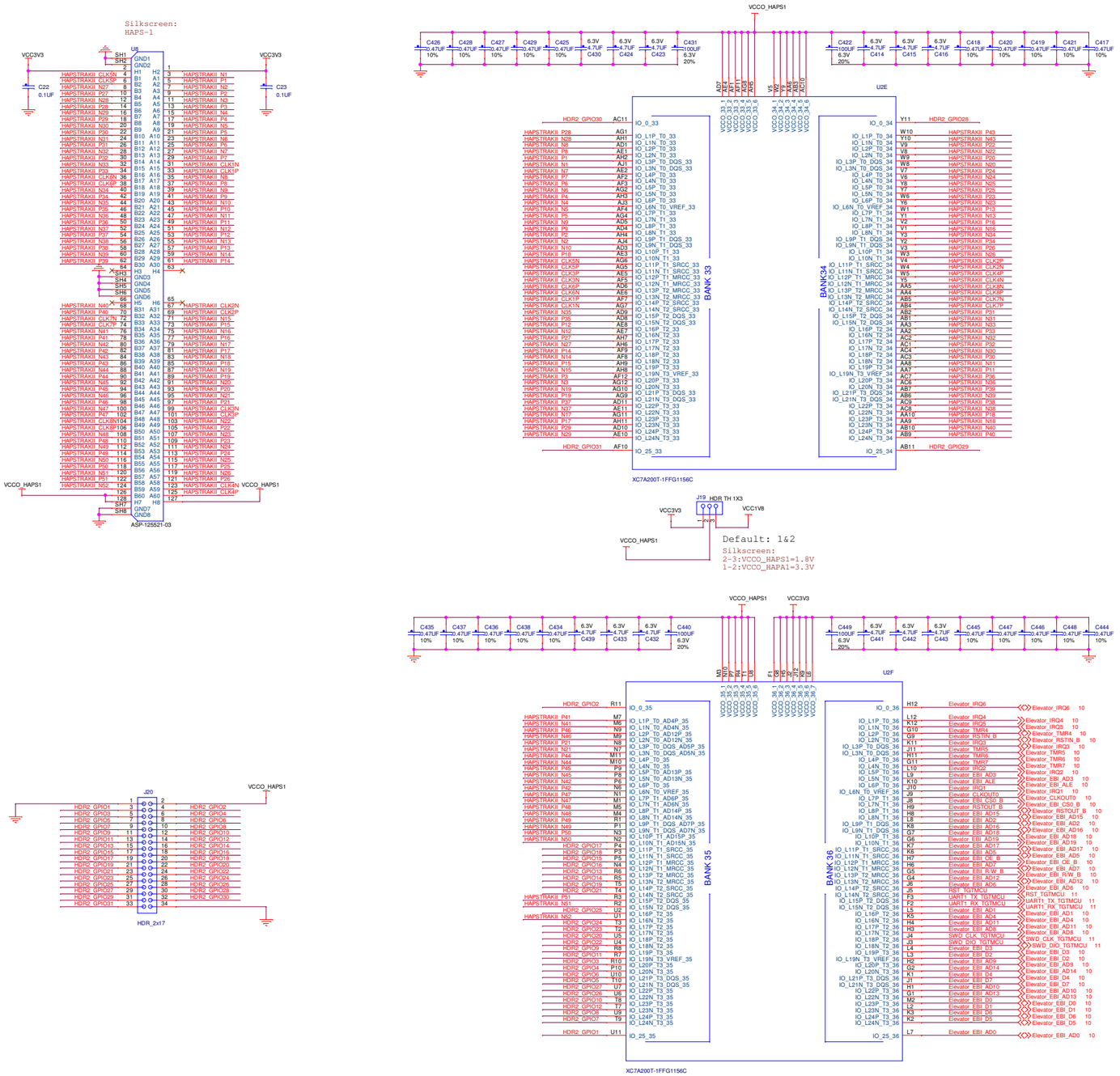
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HAPS-1
U8
ASP-125521-03
VCC3V3
VCCO_HAPS1
C22 0.1UF
C23 0.1UF
HAPSTRAKII CLK5N
HAPSTRAKII CLK5P
HAPSTRAKII CLK6N
HAPSTRAKII CLK6P
HAPSTRAKII P1
HAPSTRAKII P2
HAPSTRAKII P3
HAPSTRAKII P4
HAPSTRAKII P5
HAPSTRAKII P6
HAPSTRAKII P7
HAPSTRAKII P8
HAPSTRAKII P9
HAPSTRAKII P10
HAPSTRAKII P11
HAPSTRAKII P12
HAPSTRAKII P13
HAPSTRAKII P14
HAPSTRAKII CLK2N
HAPSTRAKII CLK2P
HAPSTRAKII P15
HAPSTRAKII P16
HAPSTRAKII P17
HAPSTRAKII P18
HAPSTRAKII P19
HAPSTRAKII P20
HAPSTRAKII P21
HAPSTRAKII CLK3N
HAPSTRAKII CLK3P
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HAPSTRAKII P23
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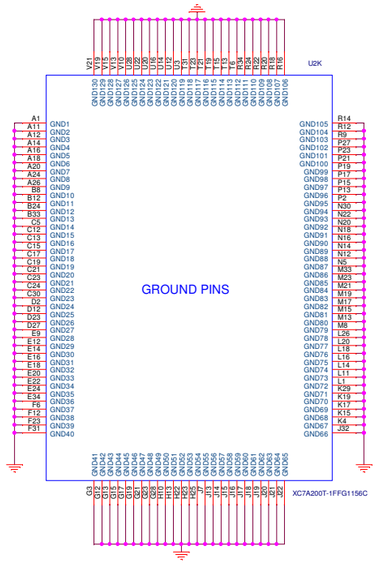
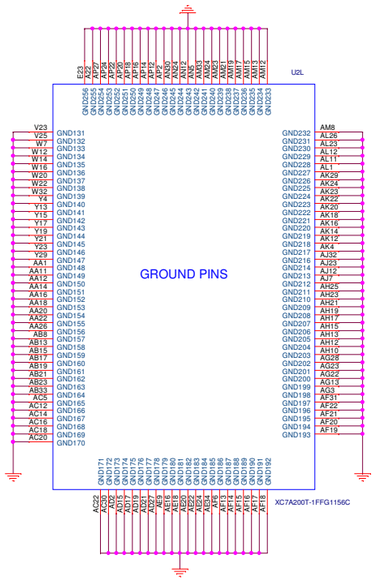
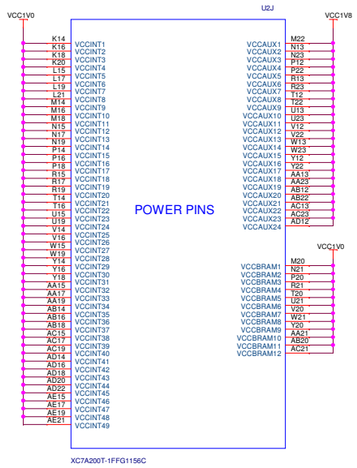
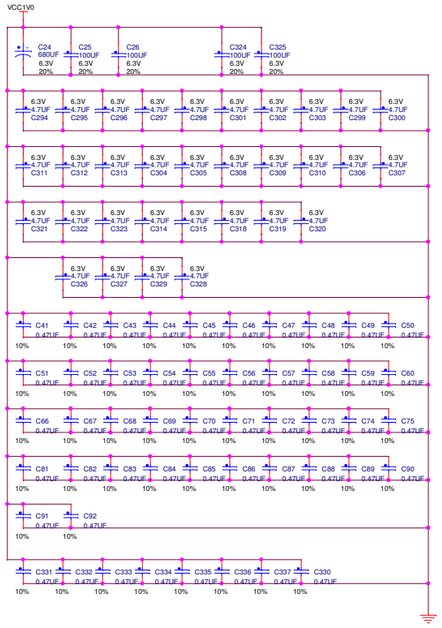
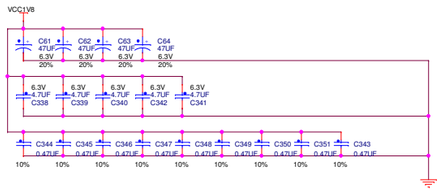
HAPSTRAKII P26
HAPSTRAKII P27
HAPSTRAKII CLK4N
HAPSTRAKII CLK4P
U2E
XC7A200T-1FFG1156C
BANK 33
BANK34
HDR2_GPIO30
HDR2_GPIO31
HDR2_GPIO28
HDR2_GPIO29
J19
HDR TH 1X3
Default: 1&2
Silkscreen:
2-3:VCCO_HAPS1=1.8V
1-2:VCCO_HAPA1=3.3V
J20
HDR_2x17
U2F
XC7A200T-1FFG1156C
BANK 35
BANK 36
HDR2_GPIO2
HDR2_GPIO1











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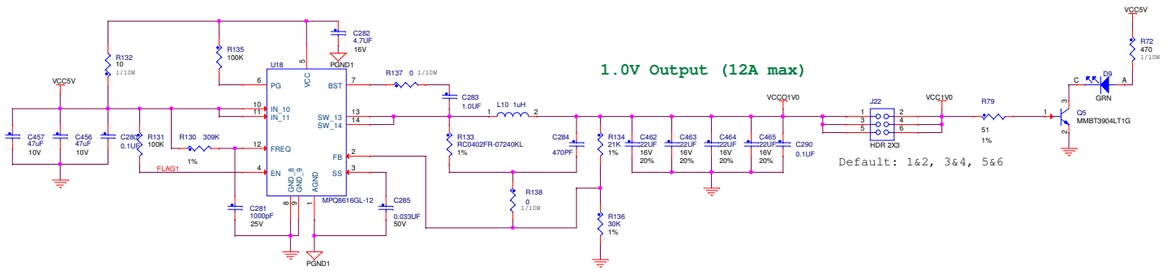
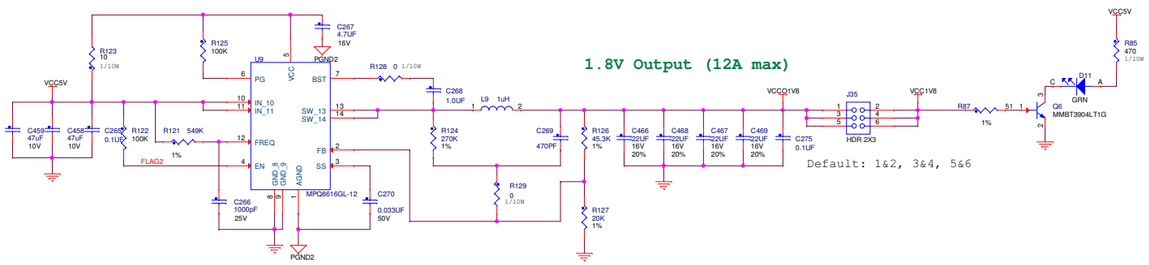
1.0V Output (12A max)



1.8V Output (12A max)



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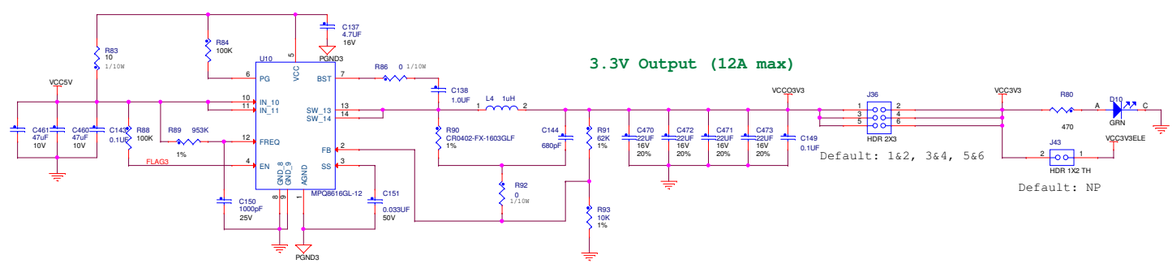

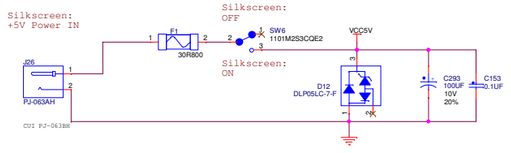

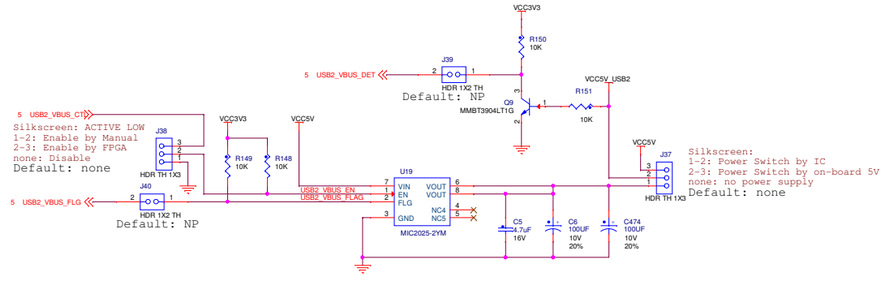

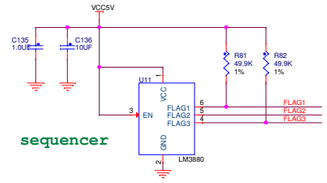

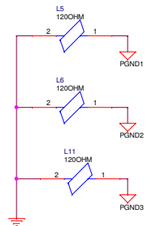

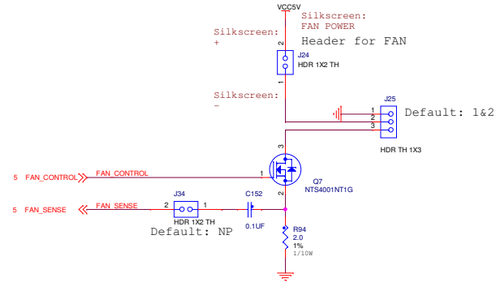

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Page Title:	BOARD POWER DISTRIBUTION		
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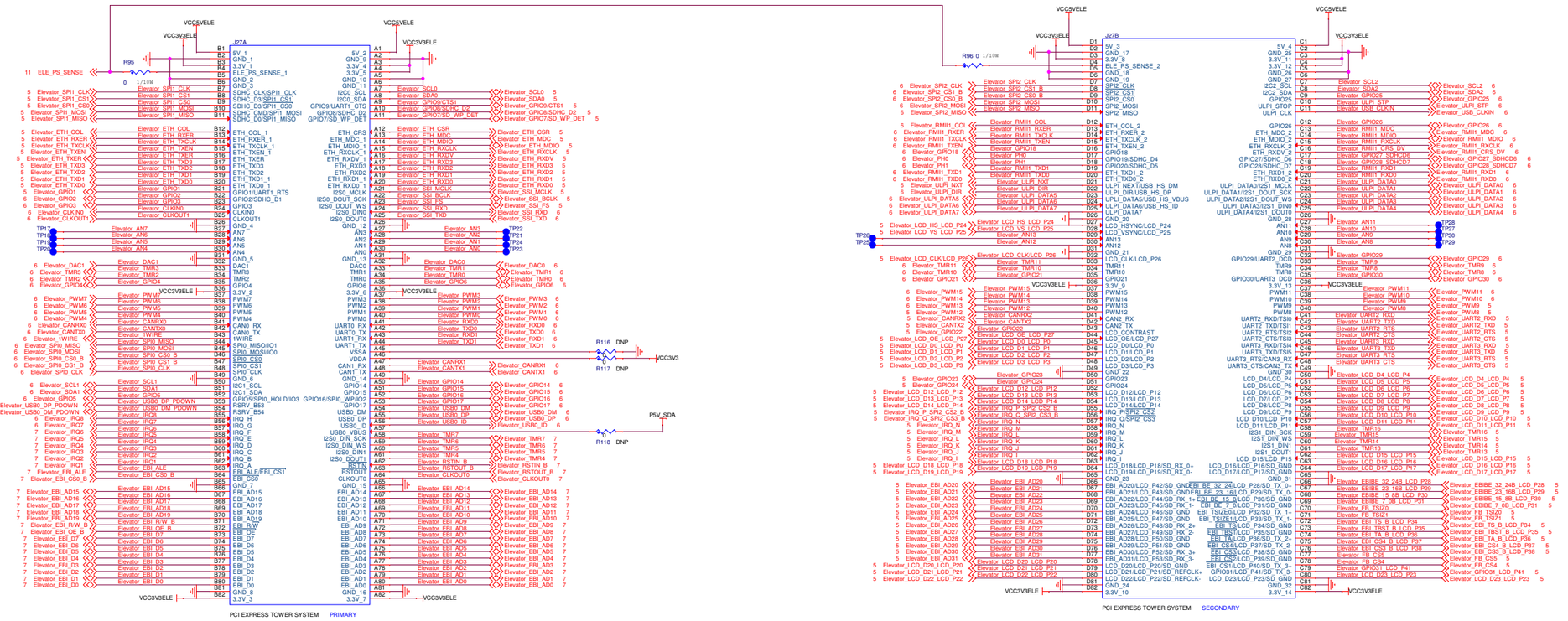

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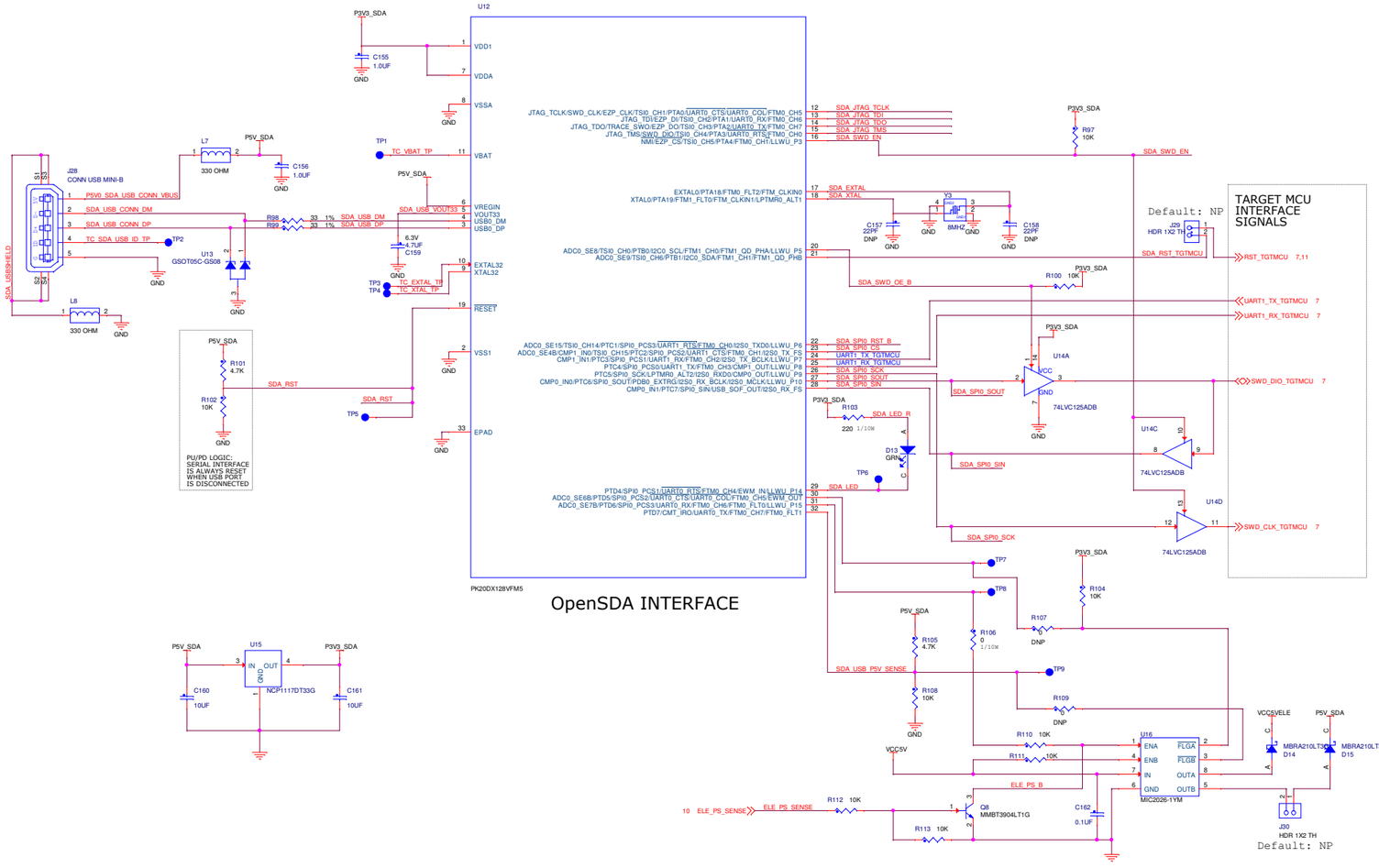

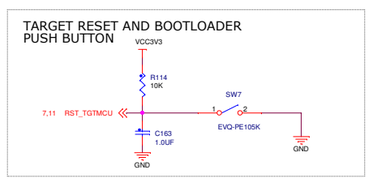

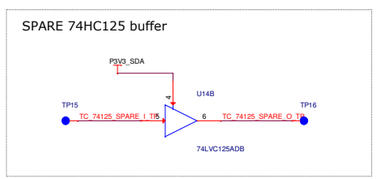

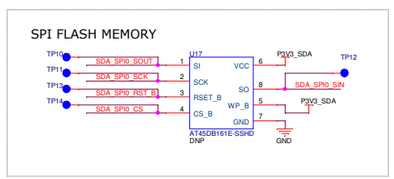

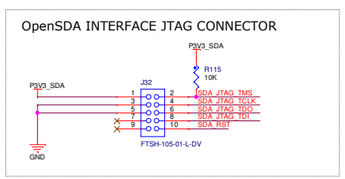

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