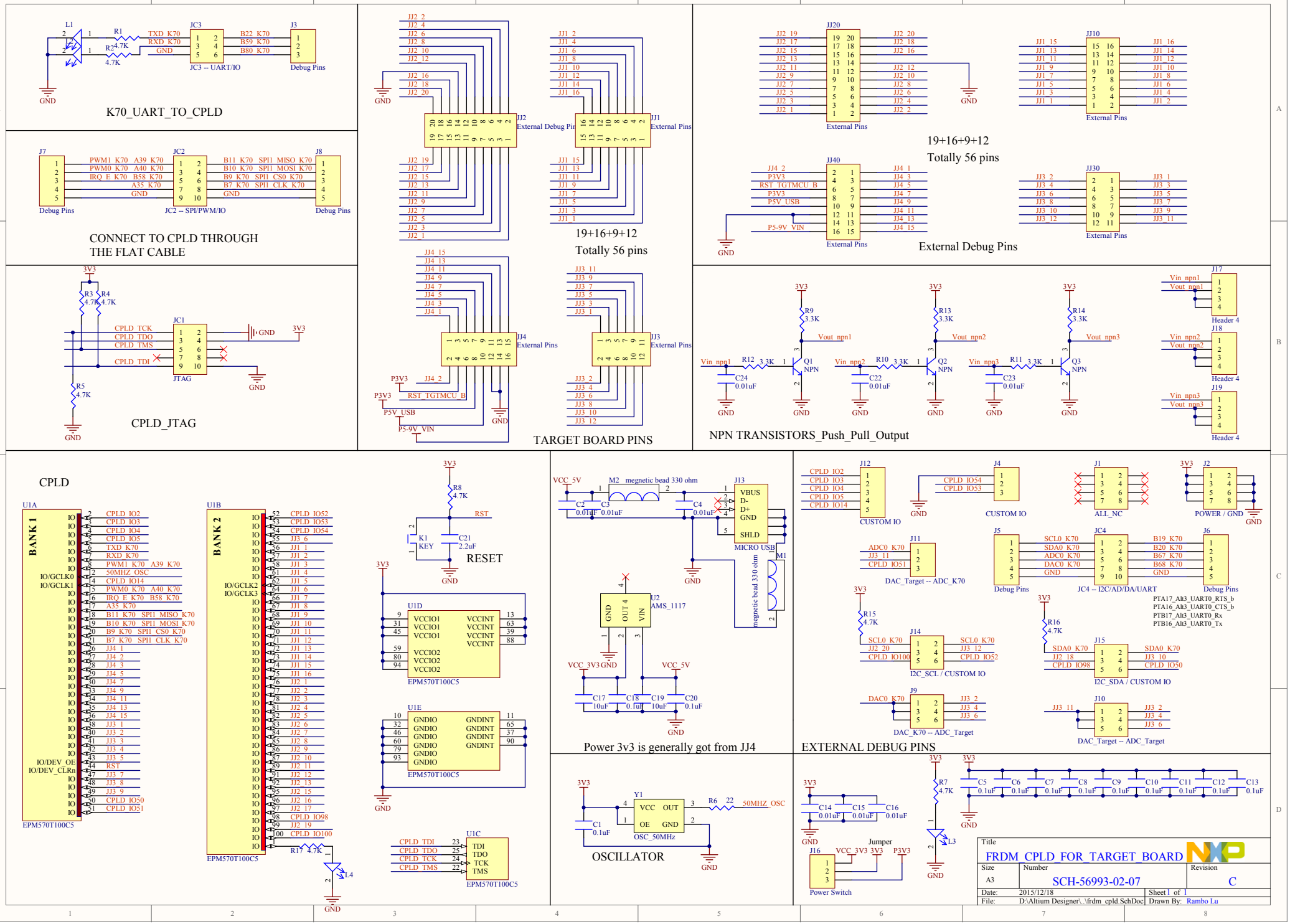
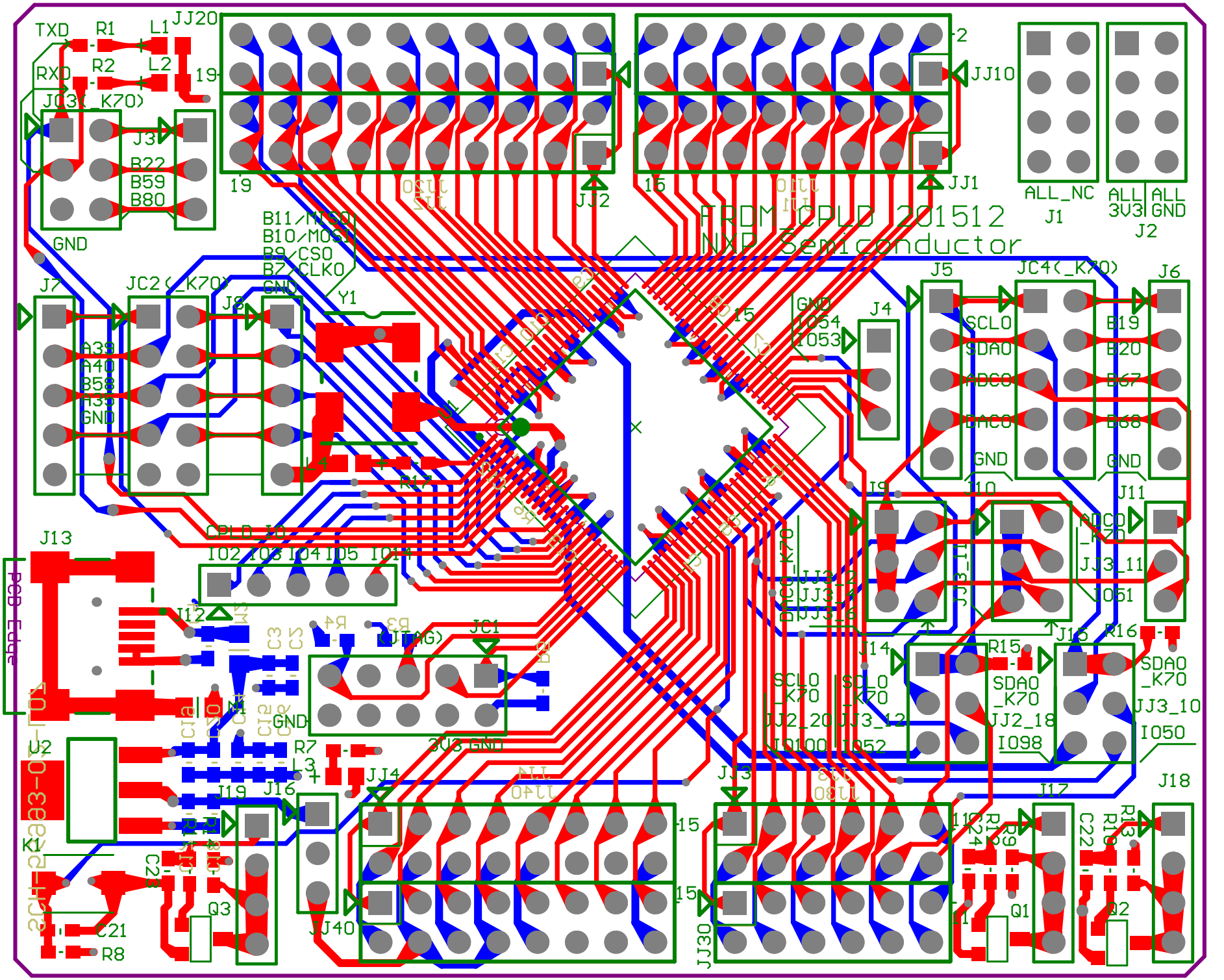

K70_UART_TO_CPLD
CONNECT TO CPLD THROUGH THE FLAT CABLE
CPLD_JTAG
19+16+9+12
Totally 56 pins
TARGET BOARD PINS
External Debug Pins
NPN TRANSISTORS_Push_Pull_Output
CPLD
RESET
Power 3v3 is generally got from JJ4
EXTERNAL DEBUG PINS
OSCILLATOR
Title
FRDM_CPLD_FOR_TARGET_BOARD
Size
A3
Number
SCH-56993-02-07
Revision
C
Date: 2015/12/18
Sheet 1 of 1
File: D:\Altium Designer\..\frdm_cpld.SchDoc
Drawn By: Rambo Lu


FRDM CPLD 201512
NXP Semiconductor
TXD
RXD
R1
R2
L1
L2
JJ20
JC3(_K70)
J3
B22
B59
B80
GND
JJ2
JJ1
JJ10
ALL_NC
J1
ALL
3V3
ALL
GND
J2
B11/MISO
B10/MOSI
B9/CS0
B7/CLKO
GND
J7
JC2(_K70)
J8
Y1
A39
A40
B58
A39
GND
L4
R14
J4
GND
I054
I053
J5
JC4(_K70)
J6
SCLO
SDAO
ADC0
DAC0
B19
B20
B67
B68
GND
GND
J9
J10
J11
ADC0
_K70
JJ3_11
I051
CPLD_IO
I02 I03 I04 I05 I014
J13
J12
JJ3_2
JJ3_4
JJ3_6
JC1
(JTAG)
J14
R15
J15
R16
SCLO
_K70
SDAO
_K70
JJ2_20
JJ3_12
I0100
I052
SDAO
_K70
JJ2_18
I098
JJ3_10
I050
GND
3V3 GND
U2
R7
L3
JJ4
J19
J16
J3
J17
J18
K1
C21
R8
Q3
JJ40
JJ30
Q1
Q2
C22
R13
R10
R26
R24
PCB Edge