Zhuolun (Leon) HE

The Chinese University of Hong Kong
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RESEARCH INTEREST

Efficient physical verification via parallel computing and customized data structures

EDUCATION

The Chinese University of Hong Kong *Hong Kong*
Ph.D. candidate in Computer Scinece and Engineering *Aug. 2019 - Present*
Supervisor: Prof. Bei Yu

Peking University *Beijing*
Ph.D. student in Computer Architecture *Sept. 2017 - Sept. 2018*
Supervisor: Prof. Guojie Luo

Peking University *Beijing*
B.S. in Computer Science and Technology *Sept. 2013 - Jul. 2017*
Thesis: Architecture Support for Monadic Serial Dynamic Programming Algorithm

PUBLICATION

1. **Zhuolun He**, Yihang Zuo, Jiaxi Jiang, Haisheng Zheng, Yuzhe Ma, and Bei Yu. "OpenDRC: An Efficient Open-Source Design Rule Checking Engine with Hierarchical GPU Acceleration". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2023.
2. Wei Zhong, Zhenhua Feng, **Zhuolun He**, Weimin Wang, Yuzhe Ma, and Bei Yu. "Enabling Efficient Design Rule Checking with GPU Acceleration". *IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE)*, Antwerp, 2023. (extended abstract)
3. Yuxuan Zhao, Qi Sun, **Zhuolun He**, Yang Bai, and Bei Yu. "AutoGraph: Optimizing DNN Computation Graph for Parallel GPU Kernel Execution". *AAAI Conference on Artificial Intelligence (AAAI)*, Washington, DC, 2023.
4. Ziyi Wang, **Zhuolun He**, Chen Bai, Haoyu Yang, and Bei Yu. "Efficient Arithmetic Block Identification with Graph Learning and Network-flow". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.
5. **Zhuolun He**, Yuzhe Ma, and Bei Yu. "X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweepline Algorithms". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Diego, CA, 2022.
6. Ziyi Wang, Chen Bai, **Zhuolun He**, Guangliang Zhang, Qiang Xu, Tsung-Yi Ho, Bei Yu, and Yu Huang. "Functionality Matters in Netlist Representation Learning". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2022.
7. **Zhuolun He**, Ziyi Wang, Chen Bai, Haoyu Yang, and Bei Yu. "Graph Learning-Based Arithmetic Block Identification". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, Munich, 2021.
8. **Zhuolun He**, Peiyu Liao, Siting Liu, Yuzhe Ma, and Bei Yu. "Physical Synthesis for Advanced Neural Network Processors". *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, 2021. (Invited Paper)

9. **Zhuolun He**, Lu Zhang, Peiyu Liao, Yuzhe Ma, and Bei Yu. "Reinforcement Learning Driven Physical Synthesis". *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Kunming, 2020. (Invited Paper)
10. Rui Lin, Ching-Yun Ko, **Zhuolun He**, Cong Chen, Yuan Cheng, Hao Yu, Graziano Chesi, and Ngai Wong. "Hotcake: Higher order tucker articulated kernels for deeper CNN compression". *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Kunming, 2020. (Invited Paper)
11. **Zhuolun He**, Yuzhe Ma, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, and Martin D.F. Wong. "Learn to Floorplan through Acquisition of Effective Local Search Heuristics". *IEEE International Conference on Computer Design (ICCD)*, Hartford, CT, 2020.
12. Yuzhe Ma, **Zhuolun He**, Wei Li, Tinghuan Chen, Lu Zhang, and Bei Yu. "Understanding Graphs in EDA: From Shallow to Deep Learning". *ACM International Symposium on Physical Design (ISPD)*, Taipei, 2020. (Invited Paper)
13. Ching-Yun Ko, Cong Chen, **Zhuolun He**, Yuke Zhang, Kim Batselier, and Ngai Wong. "Deep Model Compression and Inference Speedup of Sum-Product Networks on Tensor Trains". *IEEE Transactions on Neural Networks and Learning Systems (TNNLS)*, 2019.
14. **Zhuolun He**, Hanxian Huang, Ming Jiang, Yuanchao Bai, and Guojie Luo. "FPGA-based Real-time Super-resolution System for Ultra High Definition Videos". *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Boulder, CO, 2018.
15. **Zhuolun He** and Guojie Luo. "FPGA Acceleration for Computational Glass-Free Displays". *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, 2017.

WORK EXPERIENCE

Shanghai AI Lab — *Shanghai*
Research Intern — *Sept. 2022 - Present*

SmartMore — *Hong Kong*
Research Intern — *Jun. 2020 - Apr. 2022*

The University of Hong Kong — *Hong Kong*
Research Assistant — *Nov. 2018 - Jul. 2019*

AWARDS

- 3rd Place in ISPD Contest *2020*
- Champion of EDAthon 2018 *2018*
- Outstanding Dissertation Award at EECS, Peking University *2017*

SKILL SET

Programming	Proficient in C/C++, Python Experienced with CUDA, HLS-C, Javascript/Typescript, MATLAB, Rust
Framework/Tool	Bash, Bootstrap, LaTeX, PyTorch, Taskflow