

Zhuolun (Leon) HE

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RESEARCH INTERESTS

LLM empowered EDA, efficient physical verification, netlist representation learning

WORK EXPERIENCE

The Chinese University of Hong Kong
Postdoctoral Fellow

Hong Kong
Nov. 2023 - Present

Shanghai AI Lab
Research Intern

Shanghai
Sept. 2022 - Oct. 2023

SmartMore
Research Intern

Hong Kong
Jun. 2020 - Apr. 2022

The University of Hong Kong
Research Assistant

Hong Kong
Nov. 2018 - Jul. 2019

EDUCATION

The Chinese University of Hong Kong
Ph.D. in Computer Science and Engineering
Supervisor: Prof. Bei Yu
Thesis: The Trio of Learning, Optimization, and Acceleration for Efficient Electronic Design Automation

Hong Kong
Aug. 2019 - Aug. 2023

Peking University
Ph.D. student in Computer Architecture
Supervisor: Prof. Guojie Luo

Beijing
Sept. 2017 - Sept. 2018

Peking University
B.S. in Computer Science and Technology
Thesis: Architecture Support for Monadic Serial Dynamic Programming Algorithm

Beijing
Sept. 2013 - Jul. 2017

PUBLICATION

42. Yuan Pu, **Zhuolun He**, Yuqi Jiang, Tairu Qiu, Haoyuan Wu, Qi Sun, Cheng Zhuo, and Bei Yu. "Customized Retrieval Augmented Generation and Benchmarking for EDA Tool Documentation QA". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2025.
41. **Zhuolun He**, Yuan Pu, Haoyuan Wu, Tairu Qiu, and Bei Yu. "Large Language Models for EDA: Future or Mirage?" *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2025.
40. Jiahao Xu, **Zhuolun He**, Shuo Yin, Yuan Pu, Wenjian Yu, and Bei Yu. "EasyMRC: Efficient Mask Rule Checking via Representative Edge Sampling". *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2025.
39. Siting Liu, Jieya Zhou, Jiaxi Jiang, **Zhuolun He**, Ziyi Wang, Yibo Lin, Bei Yu, and Martin Wong. "Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs". *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2025.

38. Haisheng Zheng, Haoyuan Wu, and **Zhuolun He**. "ChatLS: Multimodal Retrieval-Augmented Generation and Chain-of-Thought for Logic Synthesis Script Customization". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, June 22–25, 2025.
37. Hang Liu, Hao Geng, **Zhuolun He**, Qi Sun, and Cheng Zhuo. "Swift or Exact? Boosting Efficient Microarchitecture DSE via Multi-fidelity Partial Order Prediction". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, June 22–25, 2025.
36. Haoyuan Wu, Haisheng Zheng, **Zhuolun He**, and Bei Yu. "Divergent Thoughts toward One Goal: LLM-based Multi-Agent Collaboration System for Electronic Design Automation". *Nations of the Americas Chapter of the Association for Computational Linguistics (NAACL)*, Albuquerque, NM, USA, Apr. 29–May 2, 2025.
35. Yuan Pu, Tinghuan Chen, **Zhuolun He**, Jiajun Qin, Chen Bai, Haisheng Zheng, Yibo Lin, and Bei Yu. "IncreMacro: Incremental Macro Placement Refinement". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2025.
34. **Zhuolun He**, Yuan Pu, Haoyuan Wu, Tairu Qiu, and Bei Yu. "Large Language Models for EDA: Future or Mirage?" *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2025.
33. Haisheng Zheng, Haoyuan Wu, **Zhuolun He**, Yuzhe Ma, and Bei Yu. "iRw: An Intelligent Rewriting". *IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE)*, Lyon, France, Mar. 31–Apr. 2, 2025.
32. Yuan Pu, Fangzhou Liu, **Zhuolun He**, Keren Zhu, Rongliang Fu, Ziyi Wang, Tsung-Yi Ho, and Bei Yu. "HeLO: A Heterogeneous Logic Optimization Framework by Hierarchical Clustering and Graph Learning". *ACM International Symposium on Physical Design (ISPD)*, Austin, IL, USA, Mar. 16–19, 2025. (Best Paper Award Nomination)
31. Ziyi Wang, Chen Bai, **Zhuolun He**, Guangliang Zhang, Qiang Xu, Tsung-Yi Ho, Yu Huang, and Bei Yu. "FGNN2: A Powerful Pre-training Framework for Learning the Logic Functionality of Circuits". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2025.
30. Haoyuan Wu, Haisheng Zheng, **Zhuolun He**, and Bei Yu. "Parameter-Efficient Sparsity Crafting from Dense to Mixture-of-Experts for Instruction Tuning on General Tasks". *Empirical Methods in Natural Language Processing (EMNLP)*, Miami, FL, USA, Dec. 12–16, 2024.
29. Yuan Pu, **Zhuolun He**, Tairu Qiu, Haoyuan Wu, and Bei Yu. "Customized Retrieval Augmented Generation and Benchmarking for EDA Tool Documentation QA". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, Newark, NJ, USA, Oct. 27–31, 2024.
28. Haoyuan Wu, **Zhuolun He**, Xinyun Zhang, Xufeng Yao, Su Zheng, Haisheng Zheng, and Bei Yu. "ChatEDA: A Large Language Model Powered Autonomous Agent for EDA". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2023.
27. Yuan Pu, Fangzhou Liu, Yu Zhang, **Zhuolun He**, Kai-Yuan Chao, Yibo Lin, and Bei Yu. "Lesyn: Placement-aware Logic Resynthesis for Non-Integer Multiple-Cell-Height Designs". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, June 23–27, 2024.
26. Jiayi Jiang, Lancheng Zou, Wenqian Zhao, **Zhuolun He**, Tinghuan Chen, and Bei Yu. "PDR: Package Design Rule Checking via GPU-Accelerated Geometric Intersection Algorithms for Non-Manhattan Geometry". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, June 23–27, 2024.
25. Fangzhou Liu, Zehua Pei, Ziyang Yu, Haisheng Zheng, **Zhuolun He**, Tinghuan Chen, and Bei Yu. "CBTune: Contextual Bandit Tuning for Logic Synthesis". *IEEE/ACM Design, Automation*

and Test in Europe Conference (DATE), Valencia, Spain, Mar. 25–27, 2024.

24. **Zhuolun He** and Bei Yu. “Large Language Models for EDA: Future or Mirage?” *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 12–15, 2024.
23. Yuan Pu, Tinghuan Chen, **Zhuolun He**, Chen Bai, Haisheng Zheng, Yibo Lin, and Bei Yu. “IncreMacro: Incremental Macro Placement Refinement”. *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 12–15, 2024. (Best Paper Award Nomination)
22. Siting Liu, Jiayi Jiang, **Zhuolun He**, Ziyi Wang, Yibo Lin, and Bei Yu. “Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs”. *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 12–15, 2024.
21. Haisheng Zheng, **Zhuolun He**, Fangzhou Liu, Zehua Pei, and Bei Yu. “LSTP: A Logic Synthesis Timing Predictor”. *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Incheon, South Korea, Jan. 22–25, 2024.
20. **Zhuolun He** and Bei Yu. “Heterogenous Acceleration for Design Rule Checking”. *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Francisco, CA, USA, Oct. 29–Nov. 2, 2023. (Invited Paper)
19. Zehua Pei, Fangzhou Liu, **Zhuolun He**, Guojin Chen, Haisheng Zheng, Keren Zhu, and Bei Yu. “AlphaSyn: Logic Synthesis Optimization with Efficient Monte Carlo Tree Search”. *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Francisco, CA, USA, Oct. 29–Nov. 2, 2023.
18. **Zhuolun He**, Haoyuan Wu, Xinyun Zhang, Xufeng Yao, Su Zheng, Haisheng Zheng, and Bei Yu. “ChatEDA: A Large Language Model Powered Autonomous Agent for EDA”. *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Snowbird, UT, USA, Oct. 29–Nov. 2, 2023.
17. **Zhuolun He**, Yihang Zuo, Jiayi Jiang, Haisheng Zheng, Yuzhe Ma, and Bei Yu. “OpenDRC: An Efficient Open-Source Design Rule Checking Engine with Hierarchical GPU Acceleration”. *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, July 9–13, 2023.
16. Zehua Pei, Wenqian Zhao, **Zhuolun He**, and Bei Yu. “Bit-Level Quantization for Efficient Layout Hotspot Detection”. *International Symposium of Electronics Design Automation (ISED)*, Nanjing, China, May 9–11, 2023.
15. Bizhao Shi, Jiayi Zhang, **Zhuolun He**, Xuechao Wei, Sicheng Li, Guojie Luo, Hongzhong Zheng, and Yuan Xie. “Efficient Super-Resolution System with Block-wise Hybridization and Quantized Winograd on FPGA”. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2023.
14. Wei Zhong, Zhenhua Feng, **Zhuolun He**, Weimin Wang, Yuzhe Ma, and Bei Yu. “Enabling Efficient Design Rule Checking with GPU Acceleration”. *Design, Automation and Test in Europe Conference (DATE)*, Antwerp, Belgium, Apr. 17–19, 2023. (extended abstract)
13. Yuxuan Zhao, Qi Sun, **Zhuolun He**, Yang Bai, and Bei Yu. “AutoGraph: Optimizing DNN Computation Graph for Parallel GPU Kernel Execution”. *AAAI Conference on Artificial Intelligence (AAAI)*, Washington, DC, USA, Feb. 7–14, 2023.
12. Ziyi Wang, **Zhuolun He**, Chen Bai, Haoyu Yang, and Bei Yu. “Efficient Arithmetic Block Identification with Graph Learning and Network-flow”. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.
11. **Zhuolun He**, Yuzhe Ma, and Bei Yu. “X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweep Algorithms”. *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Diego, CA, USA, Oct. 30–Nov. 3, 2022.

10. Ziyi Wang, Chen Bai, **Zhuolun He**, Guangliang Zhang, Qiang Xu, Tsung-Yi Ho, Bei Yu, and Yu Huang. "Functionality Matters in Netlist Representation Learning". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, July 10–14, 2022.
9. **Zhuolun He**, Ziyi Wang, Chen Bai, Haoyu Yang, and Bei Yu. "Graph Learning-Based Arithmetic Block Identification". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, Munich, Germany, Nov. 1–4, 2021.
8. **Zhuolun He**, Peiyu Liao, Siting Liu, Yuzhe Ma, and Bei Yu. "Physical Synthesis for Advanced Neural Network Processors". *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, Jan. 18–21, 2021. (Invited Paper)
7. **Zhuolun He**, Lu Zhang, Peiyu Liao, Yuzhe Ma, and Bei Yu. "Reinforcement Learning Driven Physical Synthesis". *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Kunming, China, Nov. 3–6, 2020. (Invited Paper)
6. Rui Lin, Ching-Yun Ko, **Zhuolun He**, Cong Chen, Yuan Cheng, Hao Yu, Graziano Chesi, and Ngai Wong. "Hotcake: Higher order tucker articulated kernels for deeper CNN compression". *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Kunming, China, Nov. 3–6, 2020. (Invited Paper)
5. **Zhuolun He**, Yuzhe Ma, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, and Martin D.F. Wong. "Learn to Floorplan through Acquisition of Effective Local Search Heuristics". *IEEE International Conference on Computer Design (ICCD)*, Hartford, CT, USA, Oct. 18–21, 2020.
4. Yuzhe Ma, **Zhuolun He**, Wei Li, Tinghuan Chen, Lu Zhang, and Bei Yu. "Understanding Graphs in EDA: From Shallow to Deep Learning". *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 25–Apr. 1, 2020. (Invited Paper)
3. Ching-Yun Ko, Cong Chen, **Zhuolun He**, Yuke Zhang, Kim Batselier, and Ngai Wong. "Deep Model Compression and Inference Speedup of Sum-Product Networks on Tensor Trains". *IEEE Transactions on Neural Networks and Learning Systems (TNNLS)*, 2019.
2. **Zhuolun He**, Hanxian Huang, Ming Jiang, Yuanchao Bai, and Guojie Luo. "FPGA-based Real-time Super-resolution System for Ultra High Definition Videos". *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Boulder, CO, USA, Apr. 29–May 1, 2018.
1. **Zhuolun He** and Guojie Luo. "FPGA Acceleration for Computational Glass-Free Displays". *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, USA, Feb. 22–24, 2017.

AWARDS

• Best Paper Award Nomination in ISPD	2025
• Best Paper Award Nomination in ICCAD	2024
• Best Paper Award Nomination in ISPD	2024
• 3rd Place in ISPD Contest	2020
• Champion of EDathon 2018	2018
• Outstanding Dissertation Award at EECS, Peking University	2017

SKILL SET

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Programming

Proficient in C/C++, Python

Framework/Tool

Experienced with CUDA, HLS-C, Javascript/Typescript, MATLAB, Rust
Bash, Bootstrap, \LaTeX , PyTorch, Taskflow