Zhuolun (Leon) HE

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RESEARCH INTERESTS

LLM empowered EDA, efficient physical verification, netlist representation learning

WORK EXPERIENCE

The Chinese University of Hong Kong *Hong Kong*
Postdoctoral Fellow *Nov. 2023 - Present*

Shanghai AI Lab *Shanghai*
Research Intern *Sept. 2022 - Oct. 2023*

SmartMore *Hong Kong*
Research Intern *Jun. 2020 - Apr. 2022*

The University of Hong Kong *Hong Kong*
Research Assistant *Nov. 2018 - Jul. 2019*

EDUCATION

The Chinese University of Hong Kong *Hong Kong*
Ph.D. in Computer Scinece and Engineering *Aug. 2019 - Aug. 2023*
Supervisor: Prof. Bei Yu
Thesis: The Trio of Learning, Optimization, and Acceleration for Efficient Electronic Design Automation

Peking University *Beijing*
Ph.D. student in Computer Architecture *Sept. 2017 - Sept. 2018*
Supervisor: Prof. Guojie Luo

Peking University *Beijing*
B.S. in Computer Science and Technology *Sept. 2013 - Jul. 2017*
Thesis: Architecture Support for Monadic Serial Dynamic Programming Algorithm

PUBLICATION

25. Fangzhou Liu, Zehua Pei, Ziyang Yu, Haisheng Zheng, **Zhuolun He**, Tinghuan Chen, and Bei Yu. "CBTune: Contextual Bandit Tuning for Logic Synthesis". *IEEE/ACM Design, Automation and Test in Europe Conference (DATE)*, Valencia, Spain, Mar. 25–27, 2024.
24. **Zhuolun He** and Bei Yu. "Large Language Models for EDA: Future or Mirage?" *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 12–15, 2024.
23. Yuan Pu, Tinghuan Chen, **Zhuolun He**, Chen Bai, Haisheng Zheng, Yibo Lin, and Bei Yu. "IncreMacro: Incremental Macro Placement Refinement". *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 12–15, 2024. (Best Paper Award Nomination)
22. Siting Liu, Jiaxi Jiang, **Zhuolun He**, Ziyi Wang, Yibo Lin, and Bei Yu. "Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs". *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 12–15, 2024.
21. Haisheng Zheng, **Zhuolun He**, Fangzhou Liu, Zehua Pei, and Bei Yu. "LSTP: A Logic Synthesis Timing Predictor". *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Incheon, South Korea, Jan. 22–25, 2024.

20. **Zhuolun He** and Bei Yu. "Heterogenous Acceleration for Design Rule Checking". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Francisco, CA, USA, Oct. 29–Nov. 2, 2023. (Invited Paper)
19. Zehua Pei, Fangzhou Liu, **Zhuolun He**, Guojin Chen, Haisheng Zheng, Keren Zhu, and Bei Yu. "AlphaSyn: Logic Synthesis Optimization with Efficient Monte Carlo Tree Search". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Francisco, CA, USA, Oct. 29–Nov. 2, 2023.
18. **Zhuolun He**, Haoyuan Wu, Xinyun Zhang, Xufeng Yao, Su Zheng, Haisheng Zheng, and Bei Yu. "ChatEDA: A Large Language Model Powered Autonomous Agent for EDA". *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Snowbird, UT, USA, Oct. 29–Nov. 2, 2023.
17. **Zhuolun He**, Yihang Zuo, Jiaxi Jiang, Haisheng Zheng, Yuzhe Ma, and Bei Yu. "OpenDRC: An Efficient Open-Source Design Rule Checking Engine with Hierarchical GPU Acceleration". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, July 9–13, 2023.
16. Zehua Pei, Wenqian Zhao, **Zhuolun He**, and Bei Yu. "Bit-Level Quantization for Efficient Layout Hotspot Detection". *International Symposium of Electronics Design Automation (ISEDA)*, Nanjing, China, May 9–11, 2023.
15. Bizhao Shi, Jiaxi Zhang, **Zhuolun He**, Xuechao Wei, Sicheng Li, Guojie Luo, Hongzhong Zheng, and Yuan Xie. "Efficient Super-Resolution System with Block-wise Hybridization and Quantized Winograd on FPGA". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2023.
14. Wei Zhong, Zhenhua Feng, **Zhuolun He**, Weimin Wang, Yuzhe Ma, and Bei Yu. "Enabling Efficient Design Rule Checking with GPU Acceleration". *Design, Automation and Test in Europe Conference (DATE)*, Antwerp, Belgium, Apr. 17–19, 2023. (extended abstract)
13. Yuxuan Zhao, Qi Sun, **Zhuolun He**, Yang Bai, and Bei Yu. "AutoGraph: Optimizing DNN Computation Graph for Parallel GPU Kernel Execution". *AAAI Conference on Artificial Intelligence (AAAI)*, Washington, DC, USA, Feb. 7–14, 2023.
12. Ziyi Wang, **Zhuolun He**, Chen Bai, Haoyu Yang, and Bei Yu. "Efficient Arithmetic Block Identification with Graph Learning and Network-flow". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2022.
11. **Zhuolun He**, Yuzhe Ma, and Bei Yu. "X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweepline Algorithms". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Diego, CA, USA, Oct. 30–Nov. 3, 2022.
10. Ziyi Wang, Chen Bai, **Zhuolun He**, Guangliang Zhang, Qiang Xu, Tsung-Yi Ho, Bei Yu, and Yu Huang. "Functionality Matters in Netlist Representation Learning". *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, July 10–14, 2022.
9. **Zhuolun He**, Ziyi Wang, Chen Bai, Haoyu Yang, and Bei Yu. "Graph Learning-Based Arithmetic Block Identification". *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, Munich, Germany, Nov. 1–4, 2021.
8. **Zhuolun He**, Peiyu Liao, Siting Liu, Yuzhe Ma, and Bei Yu. "Physical Synthesis for Advanced Neural Network Processors". *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, Jan. 18–21, 2021. (Invited Paper)
7. **Zhuolun He**, Lu Zhang, Peiyu Liao, Yuzhe Ma, and Bei Yu. "Reinforcement Learning Driven Physical Synthesis". *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Kunming, China, Nov. 3–6, 2020. (Invited Paper)

6. Rui Lin, Ching-Yun Ko, **Zhuolun He**, Cong Chen, Yuan Cheng, Hao Yu, Graziano Chesi, and Ngai Wong. "Hotcake: Higher order tucker articulated kernels for deeper CNN compression". *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Kunming, China, Nov. 3–6, 2020. (Invited Paper)
5. **Zhuolun He**, Yuzhe Ma, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, and Martin D.F. Wong. "Learn to Floorplan through Acquisition of Effective Local Search Heuristics". *IEEE International Conference on Computer Design (ICCD)*, Hartford, CT, USA, Oct. 18–21, 2020.
4. Yuzhe Ma, **Zhuolun He**, Wei Li, Tinghuan Chen, Lu Zhang, and Bei Yu. "Understanding Graphs in EDA: From Shallow to Deep Learning". *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 25–Apr. 1, 2020. (Invited Paper)
3. Ching-Yun Ko, Cong Chen, **Zhuolun He**, Yuke Zhang, Kim Batselier, and Ngai Wong. "Deep Model Compression and Inference Speedup of Sum-Product Networks on Tensor Trains". *IEEE Transactions on Neural Networks and Learning Systems (TNNLS)*, 2019.
2. **Zhuolun He**, Hanxian Huang, Ming Jiang, Yuanchao Bai, and Guojie Luo. "FPGA-based Real-time Super-resolution System for Ultra High Definition Videos". *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Boulder, CO, USA, Apr. 29–May 1, 2018.
1. **Zhuolun He** and Guojie Luo. "FPGA Acceleration for Computational Glass-Free Displays". *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, USA, Feb. 22–24, 2017.

AWARDS

- Best Paper Award Nomination in ISPD *2024*
- 3rd Place in ISPD Contest *2020*
- Champion of EDAthon 2018 *2018*
- Outstanding Dissertation Award at EECS, Peking University *2017*

SKILL SET

Programming	Proficient in C/C++, Python Experienced with CUDA, HLS-C, Javascript/Typescript, MATLAB, Rust
Framework/Tool	Bash, Bootstrap, LaTeX, PyTorch, Taskflow