

JL32xx – I2C Host Interface

The logo of JEILIN Technology Co., Ltd. is a large, stylized blue 'E' that is partially enclosed by a blue circular ring. A blue vertical bar is positioned to the right of the 'E', and a blue horizontal bar is positioned below the 'E'.

Revision: 0.1

Date: Mar/08/2018

JEILIN Technology Co., Ltd.

8F, No.179, Jian Yi Rd., Chung Ho Dist.,
New Taipei City, Taiwan
www.jeilin.com.tw

TEL : 886-2-82215466 FAX : 886-2-82215456



Table of Contents

REVISION HISTORY	3
INTRODUCTION	4
I2C WIRE CONNECTION	4
I2C READ/WRITE TIMING CHART	5
REGISTER DESCRIPTIONS	6



Revision History

Revision	Description of Changes	Date
0.1	Preliminary release	Mar/08/2018

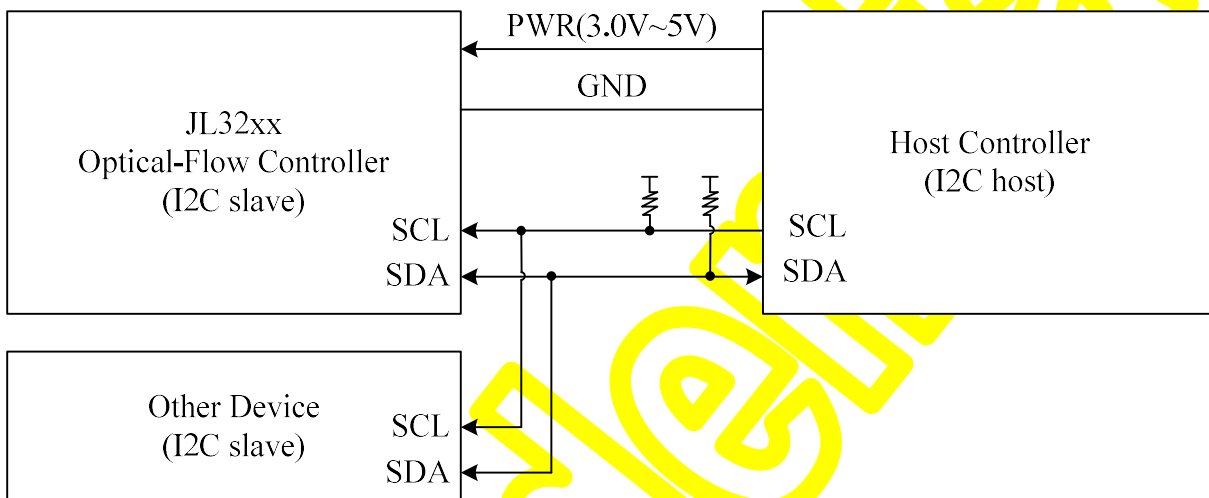


Introduction

This document describes slave mode I2C host interface of JL32xx. The “JL32xx” represents JL3283, JL3285 and JL3287.

The binary code of 7-bits I2C slave address is “0001001” and the maximum I2C clock rate is 400 KHz.

I2C Wire Connection





I2C Read/Write timing chart

Legend:

S	Start bit
P	Stop bit
A	Acknowledge bit from host CPU
A	Acknowledge bit form JL32xx
nW	Data write bit
R	Data read bit
	Delay Time

Register write sequence

S	7 bit SLAVE_ADDR	nW	A	Reg_Addr	A	Reg_Data	A	P
---	------------------	----	---	----------	---	----------	---	---

Register read sequence

S	7 bit SLAVE_ADDR	nW	A	Reg_Addr	A	P	Delay >80us	S	7 bit SLAVE_ADDR	R	A	DATA	A	P
---	------------------	----	---	----------	---	---	----------------	---	------------------	---	---	------	---	---

*Please insert 80us delay between Stop-bit and Start-Bit for JL32xx to prepare read data.



Register Descriptions

● Info Registers (Read only)

Address	Name	Descriptions
0x02	ROM ID	The revision number of internal mask ROM
0x03	Chip ID	The Chip ID of JL32xx: <ul style="list-style-type: none">● JL3283A: 0x0F● JL3285A: 0x0E● JL3287A: 0x0D

● Light Frequency (Read/Write)

Address	Name	Descriptions
0x11	Light Frequency	Set light frequency: 0: 50Hz (Default) 1: 60Hz

● Motion Data Ready flag (Read only)

Address	Name	Descriptions
0x08	Motion Data Ready	This register indicates whether motion data is ready or not. Before reading motion data, host CPU should wait until motion data ready. 0: Motion data not ready 1: Motion data ready

● Motion data (Read only)

There are 2 types of motion data format, i.e. short motion data and long motion data. Short motion data is a 6-byte burst data which provides surface quality information and X-Y motion value. Long motion data is a 16-byte burst data which provides full optical flow motion information.

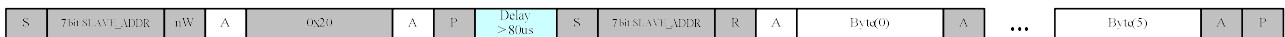
Motion data register accumulate motion value from previous reading to current reading, the register will be cleared after reading. If host CPU miss the reading time, motion value will be accumulated to next frame. Host CPU should read motion data in burst sequence, describes as follows:

Short Motion data:

Address	Name	Descriptions
0x20	Short Motion data	The read address of short motion burst



Timing chart:



Motion burst description:

B[0]	Quality	<p>This value tells the positioning quality of surface feature, the bigger the better.</p> <ul style="list-style-type: none">Quality between 128~255 indicates surface feature is strongQuality between 64~127 indicates surface feature is normalQuality between 32~63 indicates surface feature is weak, it is not suggest for high speed motion over these surfaces.Quality between 0~31 indicates surface feature is poor or ambient light is very low. Motion over these surfaces may with accumulated errors. <p>Value range: 0~255</p>
B[1]	Delta-XL	The accumulated X-axis motion value. Value rang: -32768 ~32767 pixel
B[2]	Delta-XH	
B[3]	Delta-YL	The accumulated Y-axis motion value. Value rang: -32768 ~32767 pixel
B[4]	Delta-YH	
B[5]	Checksum	<p>The checksum value of byte 0~4.</p> <p>Host CPU detects check sum error if the check sum from B[0] to B[5] is not 0.</p>

Long Motion data:

Address	Name	Descriptions
0x21	Long Motion data	The read address of long motion burst

Timing chart:



Motion burst description:

B[0]	Quality	<p>This value tells the positioning quality of surface feature, the bigger the better.</p> <ul style="list-style-type: none">Quality between 128~255 indicates surface feature is strongQuality between 64~127 indicates surface feature is normal
------	---------	---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------



		<ul style="list-style-type: none">Quality between 32~63 indicates surface feature is weak, it is not suggest for high speed motion over these surfaces.Quality between 0~31 indicates surface feature is poor or ambient light is very low. Motion over these surfaces may with accumulated errors. <p>Value range: 0~255</p>
B[1]	Delta-XL	The accumulated X-axis motion value. Value rang: -32768 ~32767 pixel
B[2]	Delta-XH	
B[3]	Delta-YL	The accumulated Y-axis motion value. Value rang: -32768 ~32767 pixel
B[4]	Delta-YH	
B[5]	Delta-ZL	The accumulated Z-axis motion value. Value rang: -32768 ~32767
B[6]	Delta-ZH	
B [7]	Reference number	Reference search images update counter. This value will auto wrap to 0 after reaching 255. Value range: 0~255
B[8]	Lightness	This value indicates the lightness of ambient. Low light environment will cause poor positioning outcomes. Value rang: 0~255
B[9]	Sub_XL	The sub-view X-axis motion value. Value rang: -32768 ~32767 pixel
B[10]	Sub_XH	
B[11]	Sub_YL	The sub-view Y-axis motion value. Value rang: -32768 ~32767 pixel
B[12]	Sub_YH	
B[13]	Interval_L	The time interval (ms) from previous reading to current reading. Value rang: 0~65535
B[14]	Interval_H	
B[15]	Checksum	The checksum value of byte 0~14. Host CPU detects check sum error if the check sum from B[0] to B[15] is not 0.



- **Special Function Register (Read/Write)**

The Special Function Register, i.e. SFR, is for host CPU to update initial code or poll hardware status. Since I2C is 8bit addressing, SFR registers are extended by adding Bank addressing. Host CPU should specify Bank + Address to access SFR registers.

Address	Name	Descriptions
0x80	Reg_Bank	SFR bank
0x81	Reg_Addr	SFR address
0x82	Reg_Data	SFR data

Write data to SFR:

Timing Chart:

S	7 bit SLAVE_ADDR	nW	A	0x80	A	Reg_Bank	A	Reg_Addr	A	Reg_Data	A	P
---	------------------	----	---	------	---	----------	---	----------	---	----------	---	---

Read data from SFR:

Step 1: Specify the Reg_Bank + Reg_Addr of SFR to be read

S	7 bit SLAVE_ADDR	nW	A	0x80	A	Reg_Bank	A	Reg_Addr	A	P
---	------------------	----	---	------	---	----------	---	----------	---	---

Step 2: Read specified SFR data

S	7 bit SLAVE_ADDR	nW	A	0x82	A	P	Delay > 80us	S	7 bit SLAVE_ADDR	R	A	DATA	A	P
---	------------------	----	---	------	---	---	-----------------	---	------------------	---	---	------	---	---



JEILIN Technology Co., Ltd.

8F, No. 179, Jian Yi Rd., Chung Ho Dist.,

New Taipei City, Taiwan

Tel: 886-2-8221-5466

Fax: 886-2-8221-5456

Website: www.jeilin.com.tw

Email: jeilin@jeilin.com.tw

©2018 JEILIN Technology Corp., Ltd. All rights reserved.

The information in this document has been carefully checked and is believed to be reliable; however no responsibility can be assumed for inaccuracies that may not have been caught. All information in this document is subject to change without prior notice. The information contained in this document is presented only as a guide for applications of our products. No responsibility is assumed by JEILIN Technology for any infringements of intellectual property or other rights of the third parties, which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of JEILIN Technology or others. No part of this document may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of JEILIN Technology.