City College of New York

Take Home Test # 4

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Objective:

The objective of this Take-Home Test is to create static random-access memory chips (SRAM) using d-latches. Our goal is to learn how to create a memory device that can hold 4, 16, 32-bit wide values as well as understanding how address inputs work as well as the functionalities of the inputs and outputs of the SRAM. This includes the Data in input, Write Enable input, Output Enable input, Chip Select Input, and output of the SRAM works.

Functionality, Specifications, and Simulation:

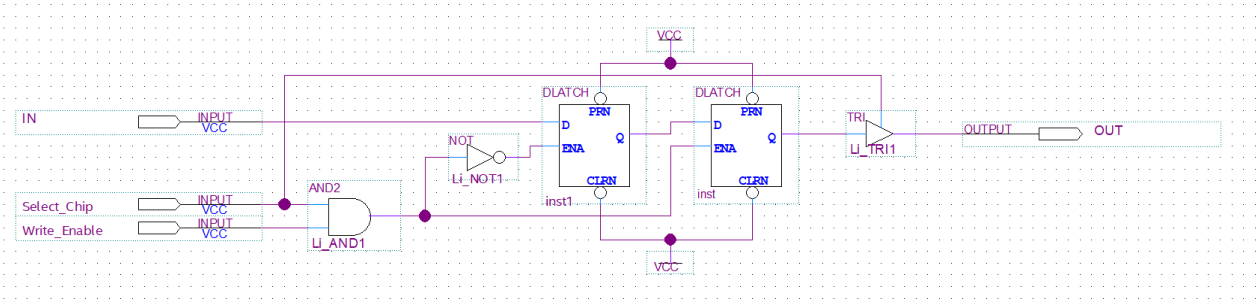

Figure 1: Above is the circuit diagram for a 1-bit Static RAM cell made using a Master Slave D-Flipflop.

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.all;
3
4   entity Decoder2to4 is
5
6    port(
7    Bin : in std_logic_vector(1 downto 0);
8    Quat : out std_logic_vector(3 downto 0));
9   end Decoder2to4;
10
11  architecture arch of Decoder2to4 is
12  begin
13
14  with Bin select
15   Quat <= "0001" when "00",
16   "0010" when "01",
17   "0100" when "10",
18   "1000" when "11",
19   "0000" when others;
20
21  end arch;
22
```

Figure 2: Above is the VHDL code of my Adapted 2 to 4 Decoder code derived from the 4 to 16 Decoder code provided in the instructions.

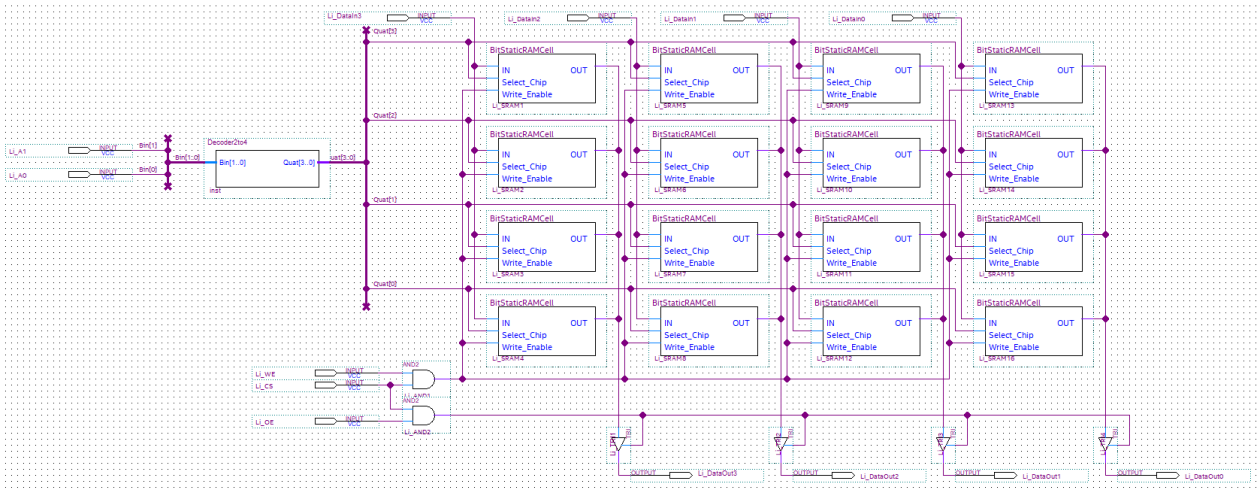

Figure 3: Above is the circuit diagram for the 4x4 SRAM built similarly to figure 16 as instructed.

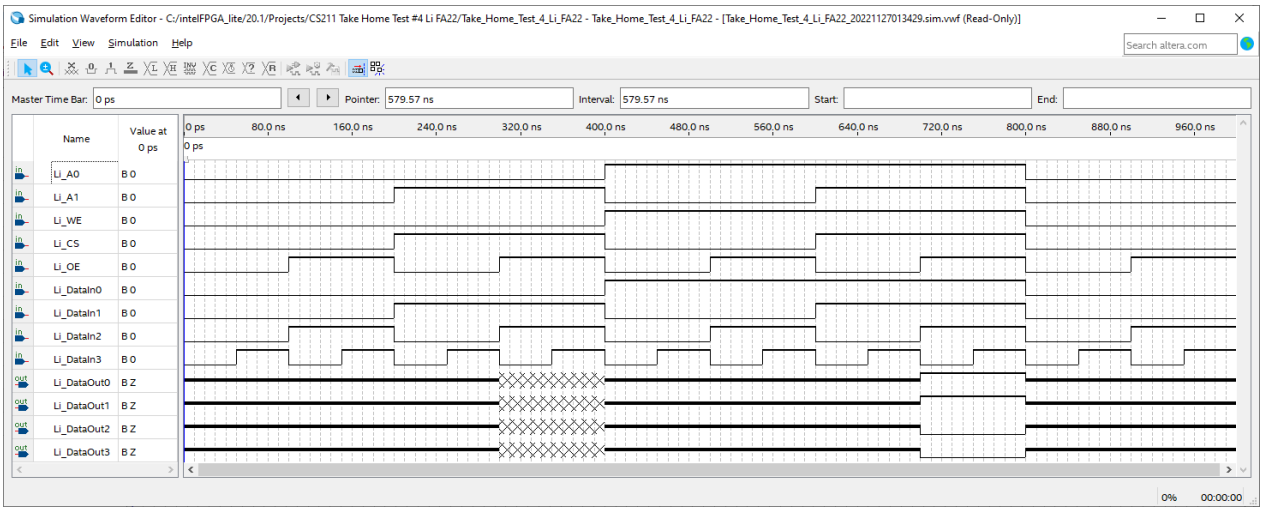

Figure 4: Above is the VWF output of the circuit diagram in Figure 3.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Decoder4to16 is

 port(
 Quat : in std_logic_vector(3 downto 0);
 Hexa : out std_logic_vector(15 downto 0));
end Decoder4to16;

architecture arch of Decoder4to16 is
begin

with Quat select
 Hexa <= "0000000000000001" when "0000",
 "0000000000000010" when "0001",
 "0000000000000100" when "0010",
 "0000000000001000" when "0011",
 "0000000000010000" when "0100",
 "0000000000100000" when "0101",
 "0000000001000000" when "0110",
 "0000000010000000" when "0111",
 "0000000100000000" when "1000",
 "0000001000000000" when "1001",
 "0000010000000000" when "1010",
 "0000100000000000" when "1011",
 "0001000000000000" when "1100",
 "0010000000000000" when "1101",
 "0100000000000000" when "1110",
 "1000000000000000" when "1111",
 "0000000000000000" when others;

end arch;
```

Figure 5: Above is the VHDL code of the 4 to 16 Decoder provided in the instructions that will be used in the 16 x 4 SRAM & 16 x 32 SRAM circuit diagram.

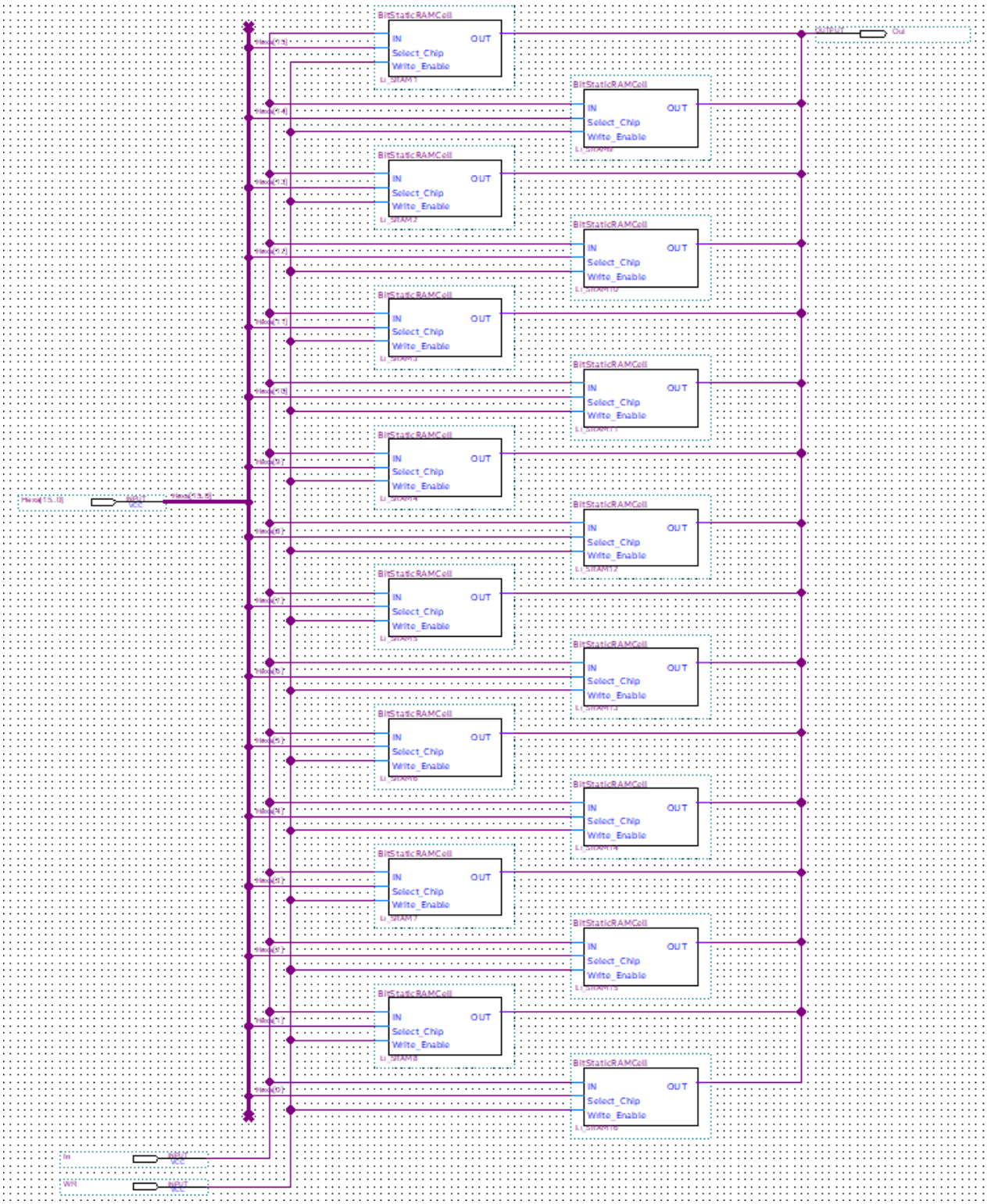

Figure 6: Above is the circuit diagram of a 16 stack of SRAM i.e., 16 x 1 SRAM built following the instructions of 19a in the lab.

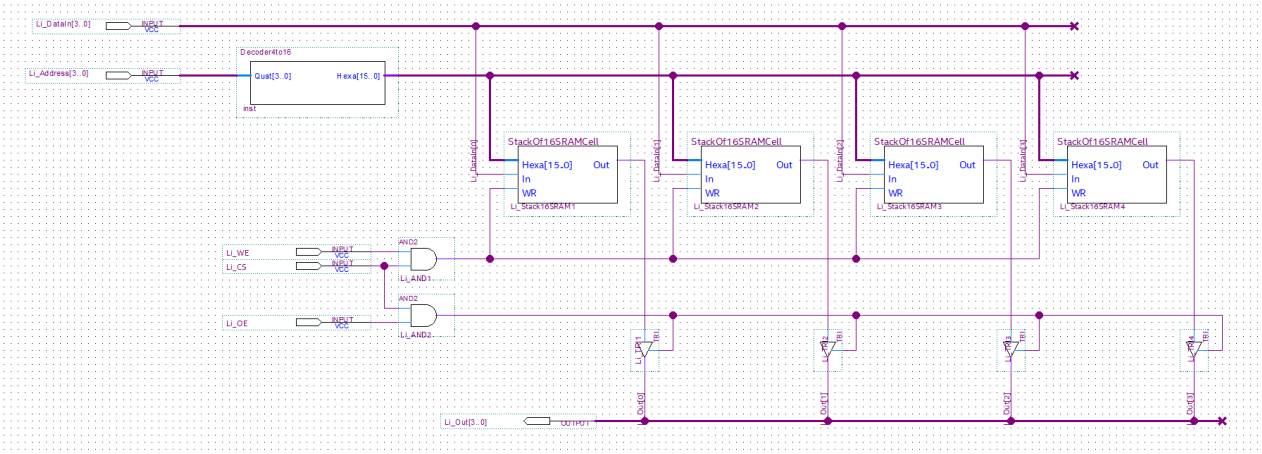

Figure 7: Above is the circuit diagram for a 16 x 4 SRAM using a stack of 16 SRAM cells.

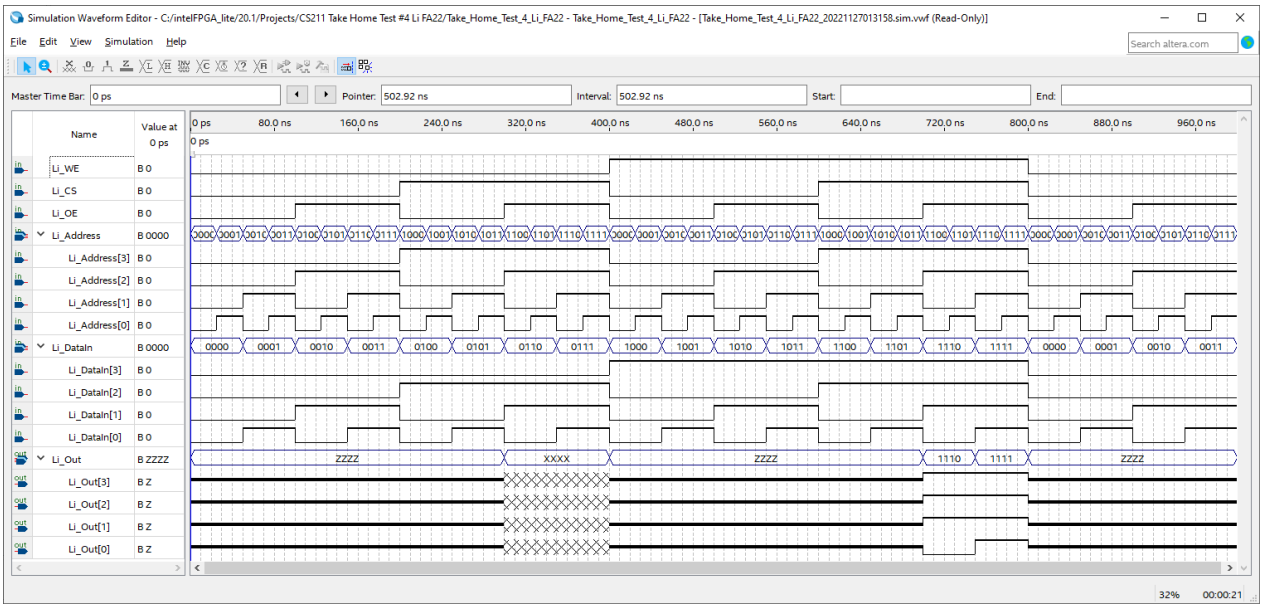

Figure 8: Above is the VWF output of the circuit diagram in Figure 7.

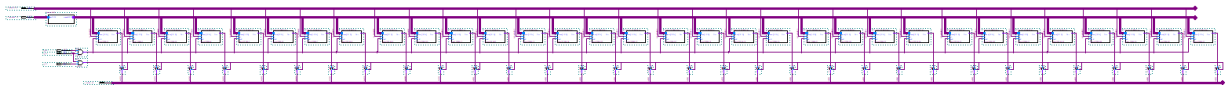

Figure 9: Expanded view of 16 x 32 SRAM circuit diagram.

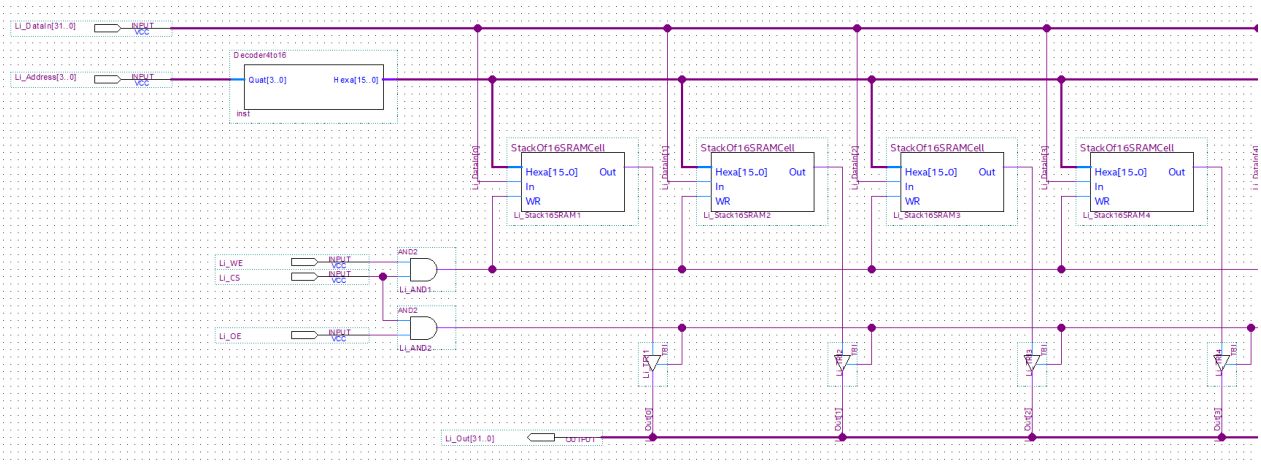

Figure 10: Front 4 16 x 1 SRAM symbols used in the 16 x 32 SRAM circuit diagram. (This pattern repeats from 0 to 31 to represent the 32 different bits)

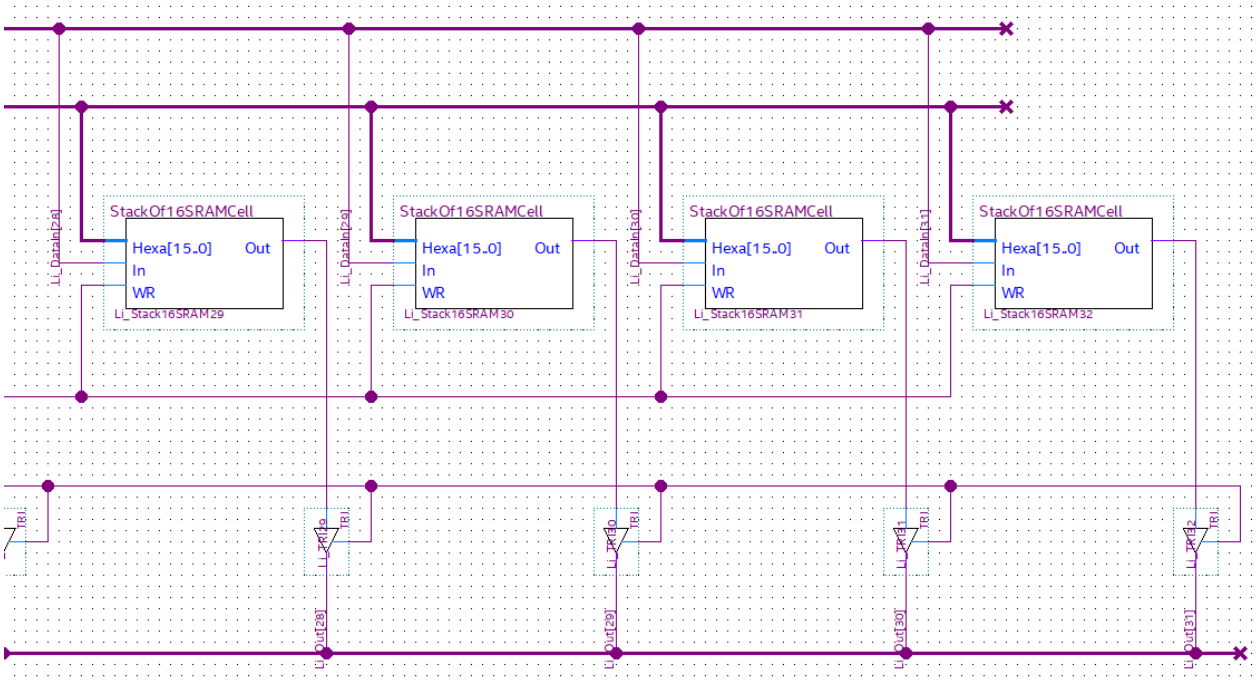

Figure 11: Last 4 16 x 1 SRAM symbols used in the 16 x 32 SRAM circuit diagram. (This pattern repeats from 0 to 31 to represent the 32 different bits)

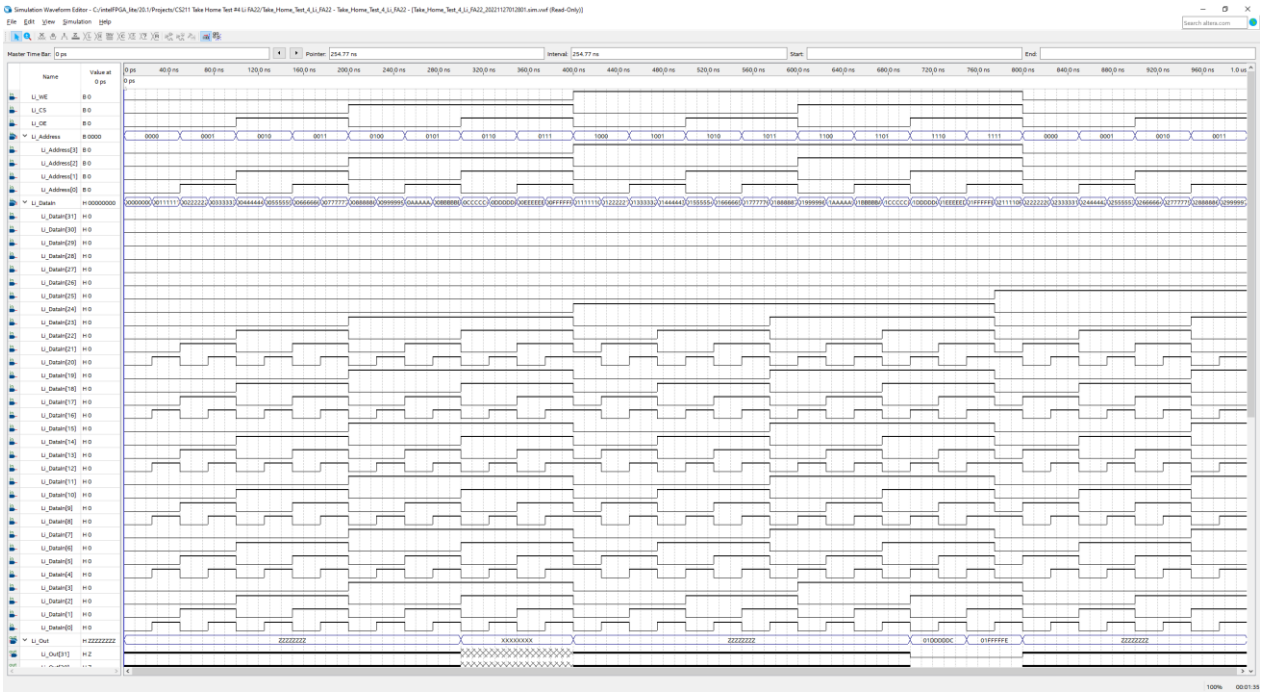

Figure 12: Above is the VWF output of the circuit diagram in Figure 9.

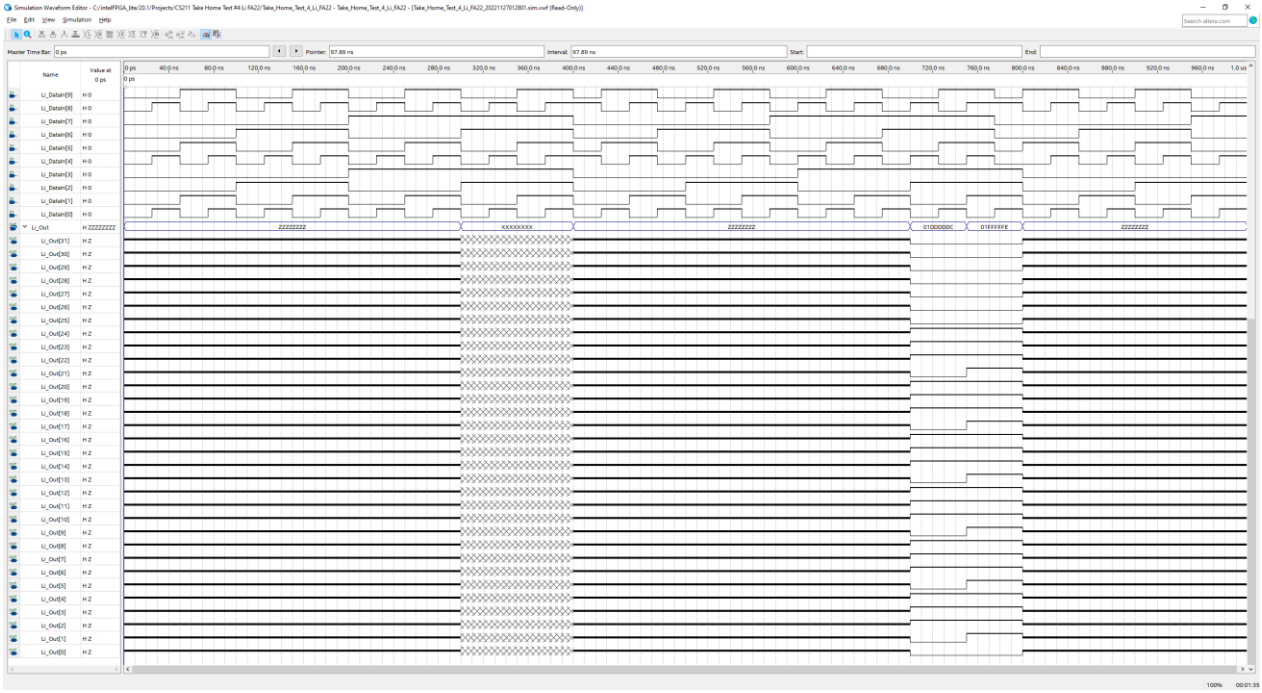

Figure 13: Above is the VWF output of the circuit diagram in Figure 9 continued.

Questions to be answered:

- What is the difference between a latch and a flip-flop?

The latch and flip-flop are both sequential devices that watch their inputs and change their outputs. The main difference between a latch and a flip-flop is that a latch can change their output at ANY given time whereas the flip-flop can ONLY change their output when the clock signal is changing (rising edge or falling edge).

- Explain the behavior of a SR Latch.

The behavior of the SR-latch is simply a storage device used to store a singular binary bit. The SR-latch has two functions that are controlled by its input signals, S and R, respectively. When input S is 1 and input R is 0, the latch is in the "set" state and its output, Q, will always be one. When input S is 0 and input R is 1, the latch is in the "reset" state and its output, Q, will always be zero. When both inputs S and R are 0, the latch is in the "latch" state and will hold the state of the previous output. When both inputs S and R are 1, the latch is in the "undefined" state, thus it will not be possible to predict its next state.

- Explain how the gated (control) SR-Latch is a modified SR-Latch.

The gated SR-latch is a modified SR-latch because they serve the same purpose, to store a binary bit, but the gated SR-latch has an extra input to determine state changes. Furthermore, the circuit of the gated SR-latch is a regular SR-latch with the extra input C that determines state changes.

- Explain how the D-Latch is a modified gated SR-Latch.

The D-Latch is a modified gated SR-latch because the circuit of the gated SR-latch and D-latch are the same with the exception that their inputs are different and D-latch has an extra NOT gate. The D-latch and gated SR-latch both use the clock signal in the same manner as to control the signal and their equations are similar.

- Explain how to build a Master-Slave flip flop.

To build a Master-Slave flip-flop, two d-latches are connected in a series. The output of the first D-latch, Q, is tied to the input of the second d-latch, D, and both d-latches must use the same clock signal, but the first latch inverts said clock signal.

- Explain how to build SRAM cells from flip flops.

To build a SRAM cell from flip-flops, a master slave flip-flop must be created, and a tristate logic buffer must be used. Using the Master-Slave flip-flop circuit diagram, we have 3 inputs: IN, SelectChip, WriteEnable and 1 output: Out. The SelectChip and WriteEnable act as the clock input for the d-latches and the tristate logic buffer takes the output of the slave latch, Q, as 1 and the SelectChip as 2, with the output 3 going to Out. The IN input signal will act as the input D.

- Why do we want to avoid the scenario when S=1 and R=1 in an SR-Latch? Could this scenario happen in a D-Latch? Why or why not?

We avoid the scenario where both inputs are 1 in the SR-latch because it violates the fact that both outputs are complements of each other since each of them tries to go to 0, which is not a stable configuration. It is impossible to predict which output will go to 1 or 0. This scenario does not happen to

the D-latch because the D-latch does not have 2 inputs S and R, only input D. Without the two inputs S and R, the latch has no invalid or illegal states.

- What is the difference between edge-triggered and level triggered devices? Is the flipflop used for the SRAM cell in this lab level or edge triggered?

The difference between edge-triggered and level-triggered devices are that edge-triggered devices become active at the negative or positive edge of the clock signal and level-triggered devices become active when the clock pulse is at a particular level. If a circuit is positive edge triggered, it will take an input at exactly the time the clock signal goes from low to high. Similarly, the input is taken at exactly the time in which the clock goes from high to low in negative edge triggering. On the other hand, level triggering circuits become active when the clock pulse is on a particular level, usually high or low. Negative level triggering circuits are active when the clock pulse is low and positive level triggering circuits are active when the clock pulse is high. The flip-flop used in the SRAM cell in this lab is edge triggered, more specifically positive edge triggered.

- Please explain how a SRAM works.

A singular bit SRAM has 3 inputs. The IN input, the SelectChip input, and the WriteEnable input. The IN input is used to latch data input. The SelectChip input is used to store data when the signal is high and not store data when the signal is low. The WriteEnable input allows the latch to store data from the IN input.

Conclusions:

In this lab, I reviewed and gained a better understanding of digital circuits that I made previously in the class such as the SR-latch, D-latch, and D-flip-flop. Through this lab, I have solidified my understanding of edge triggering circuits vs level triggering circuits. But most importantly, I learned and understood how to create a static random-access memory cell and its functionality and applications.