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Professor Gertner

CS 211

October 11th, 2022

Objective:

- What is the goal of this lab?

  The goal of this lab was to allow us to apply everything we learned from the Master Tutorial to build and simulate multiplexors to better understand concepts such as AND, OR, NOT, and NAND gates that we learned in class.

Functionality and Specifications:

- What is the combinational logic function of the circuit?

  Part 1: Simple digital 2:1 Mux from AND/OR/NOT gates

  xs’ + ys = m

  Part 2: 2:1 Mux from NAND gates

  xs’ + ys = m

  Part 3: 4:1 Mux from NAND gates

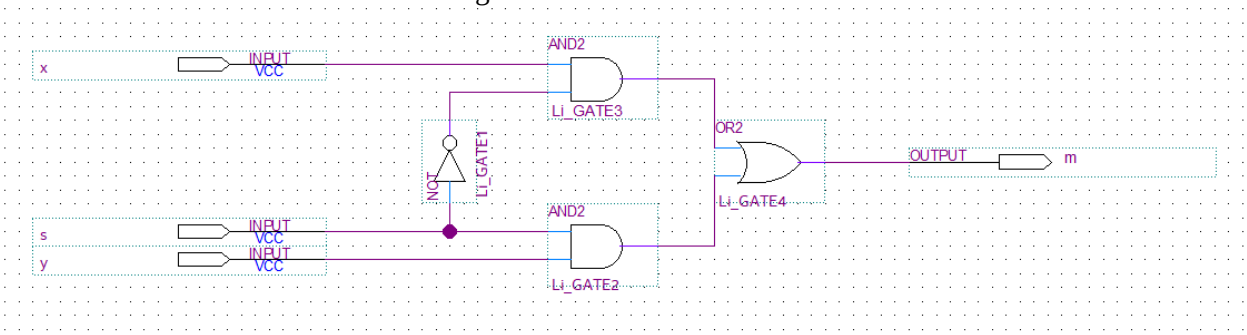
  s0’s1’i1 + s0’s1i1 + s0s1’i2 + s0s1i3 = Y

  Part 4: 4 to 1 Mux using 2 to 1 Mux as components

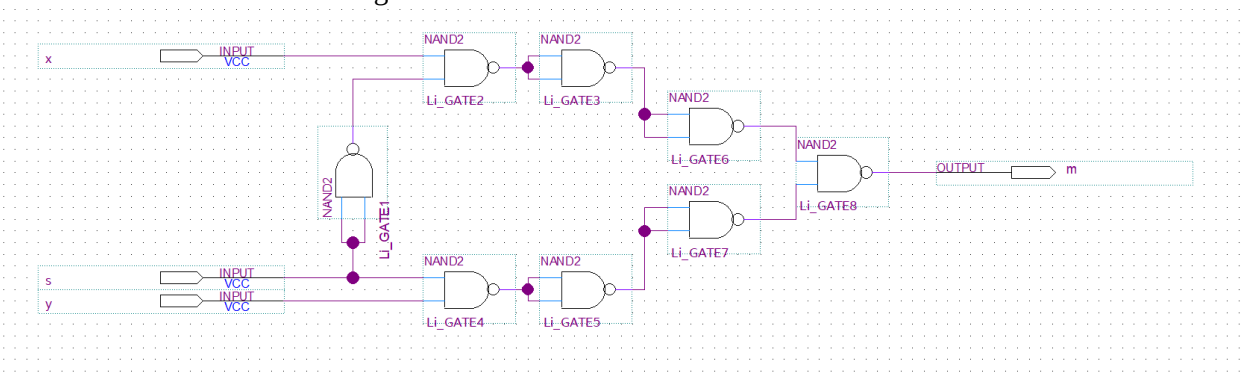
  s0’s1’i1 + s0’s1i1 + s0s1’i2 + s0s1i3 = Y

- Include a screenshot of the circuit

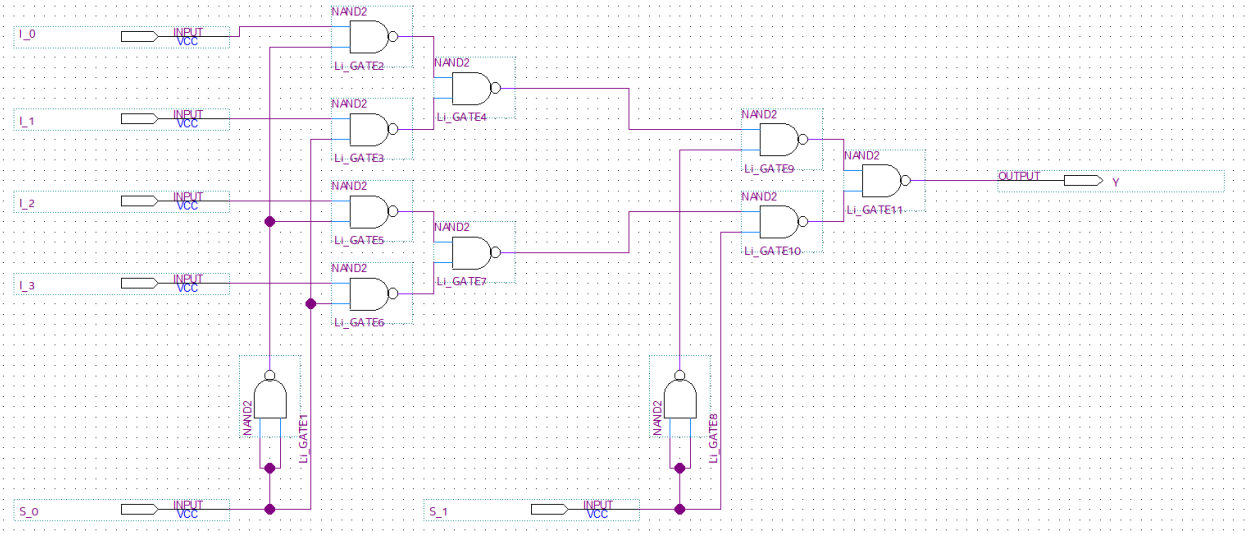
  Part 1: 2 to 1 Mux from AND/OR/NOT gates



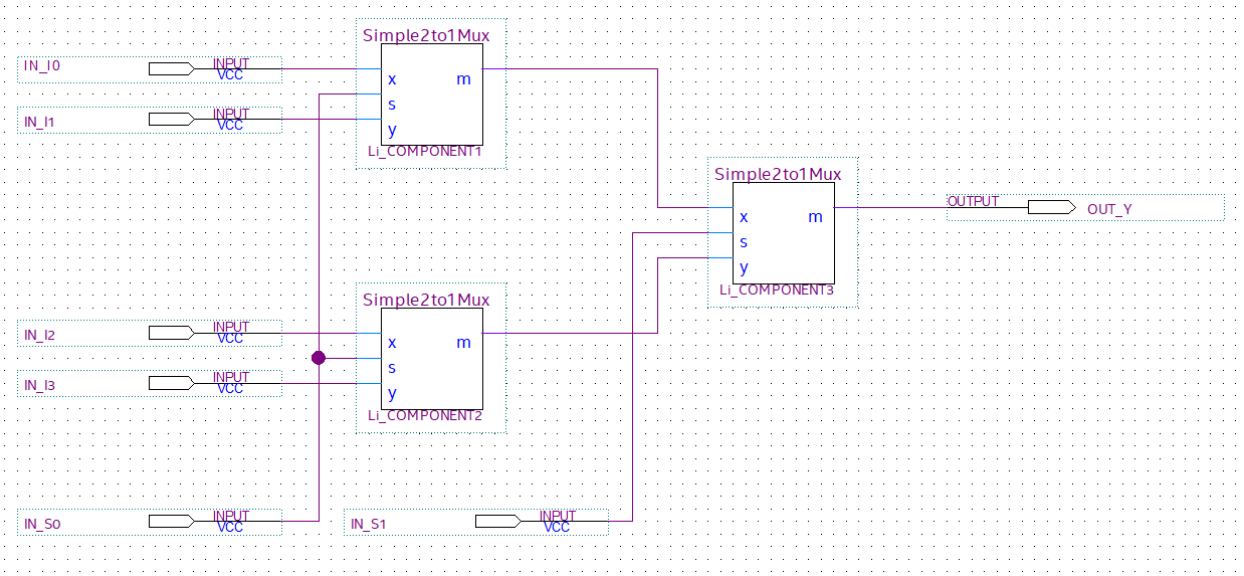
Part 2: 2 to 1 Mux from NAND gates



Part 3: 4 to 1 Mux from NAND gates



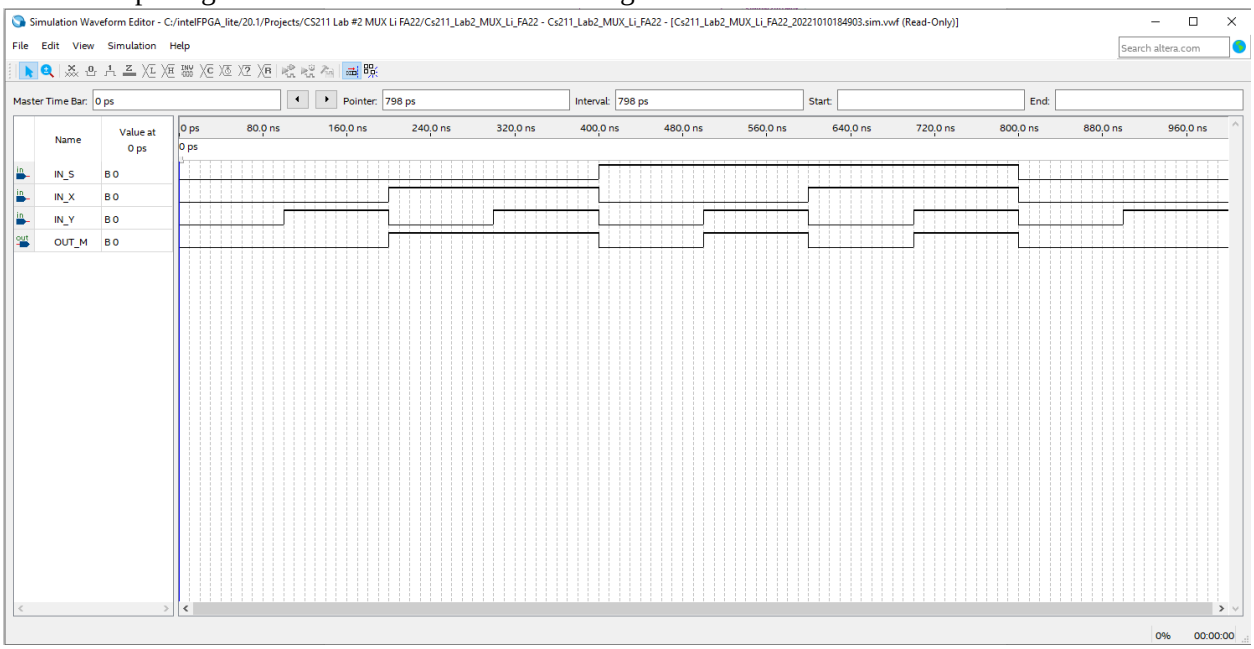
Part 4: 4 to 1 Mux using 2 to 1 Mux as components



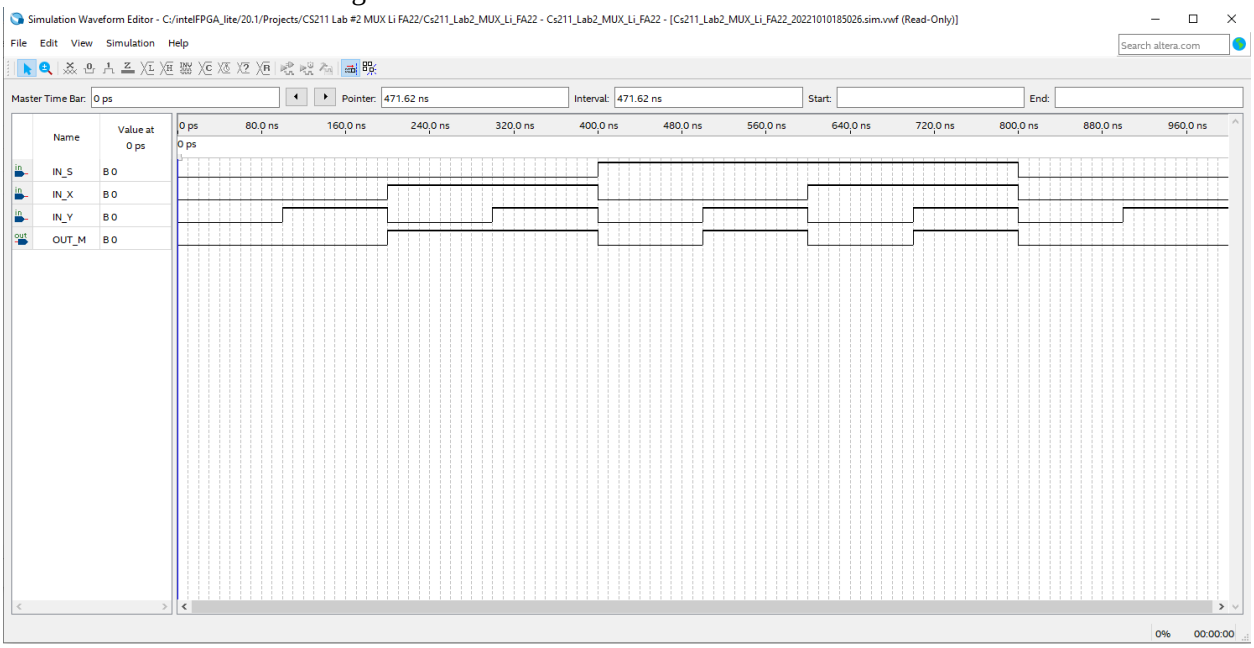
Simulation:

- Include a screenshot of the vector waveform output file.

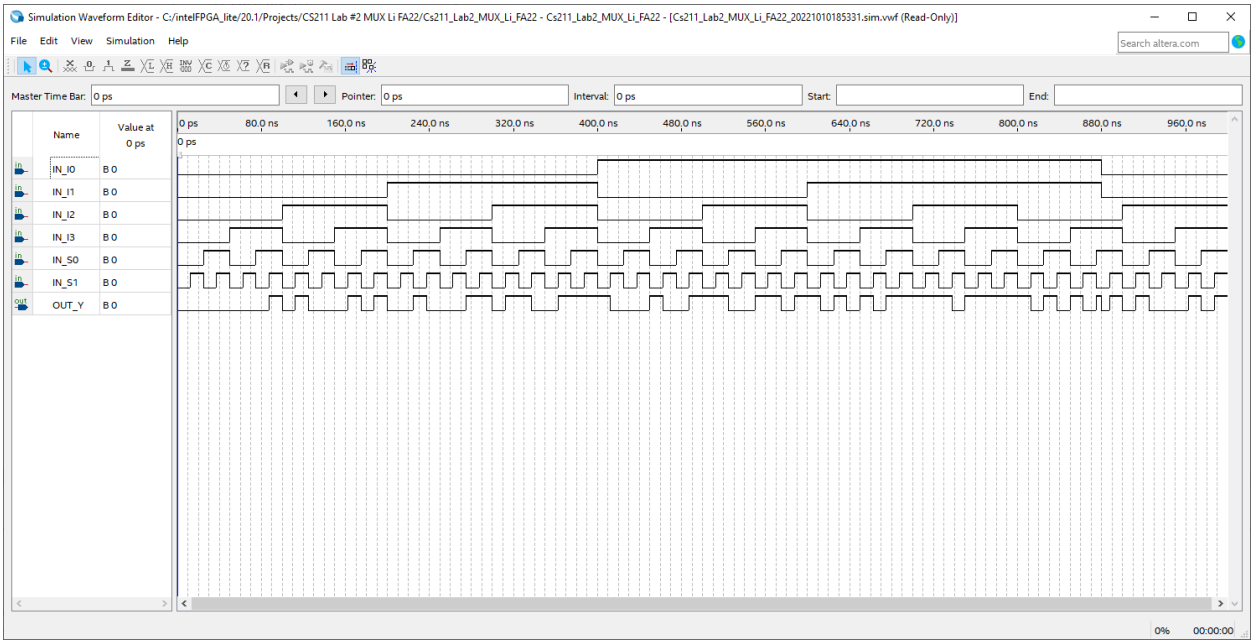
Part 1: Simple digital 2:1 Mux from AND/OR/NOT gates



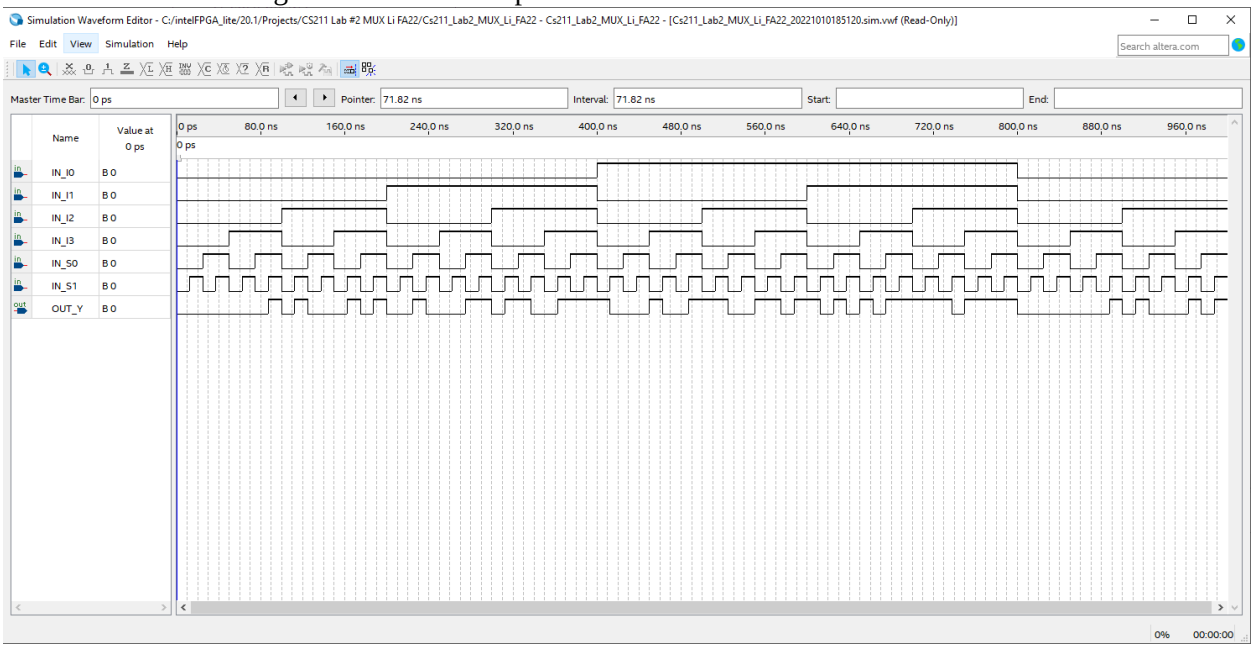
Part 2: 2:1 Mux from NAND gates



Part 3: 4:1 Mux from NAND gates (idk why the interval is between 400 to 880 here even when I set it as 400 to 800ns.)



Part 4: 4 to 1 Mux using 2 to 1 Mux as components



- Draw a truth table and explain how you used the waveform data to derive it.

  X in the tables denote the don't care condition which implies that the value on that input does not affect the outcome of the logic circuit.

Part 1: Simple digital 2:1 Mux from AND/OR/NOT gates

s	x	y	m

0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Part 2: 2:1 Mux from NAND gates

s	x	y	m
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Part 3: 4:1 Mux from NAND gates

S0	S1	I0	I1	I2	I3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

Part 4: 4 to 1 Mux using 2 to 1 Mux as components

S0	S1	I0	I1	I2	I3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

- Write a Boolean function for each exercise.

  Part 1: Simple digital 2:1 Mux from AND/OR/NOT gates

  xs’ + ys = m

  Part 2: 2:1 Mux from NAND gates

  xs’ + ys = m

  Part 3: 4:1 Mux from NAND gates

s0’s1’i1 + s0’s1i1 + s0s1’i2 + s0s1i3 = Y

Part 4: 4 to 1 Mux using 2 to 1 Mux as components

s0’s1’i1 + s0’s1i1 + s0s1’i2 + s0s1i3 = Y

Conclusions:

- What did you learn?

  I learned how to use the Quartus application to design and simulate 2 to 1 and 4 to 1 multiplexors using AND, OR, NOT, and NAND gates as well as designing a 4 to 1 multiplexor using a 2 to 1 multiplexor as a component. Additionally, I learned how to derive Boolean expressions from logic circuits and create truth tables for logic circuits.