City College of New York

Laboratory Exercise Report: D – Latch Functionality

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CSC 211 Fall 2022

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November 2nd, 2022

Objective:

The goal of this laboratory exercise is to find and use the built-in D–Latch component in Quartus and verify the component's functionality for all inputs of D, PRN, CLRN, ENA, and Q using the verification and debugging tool, "University Program VWF".

Functionality and Specifications:

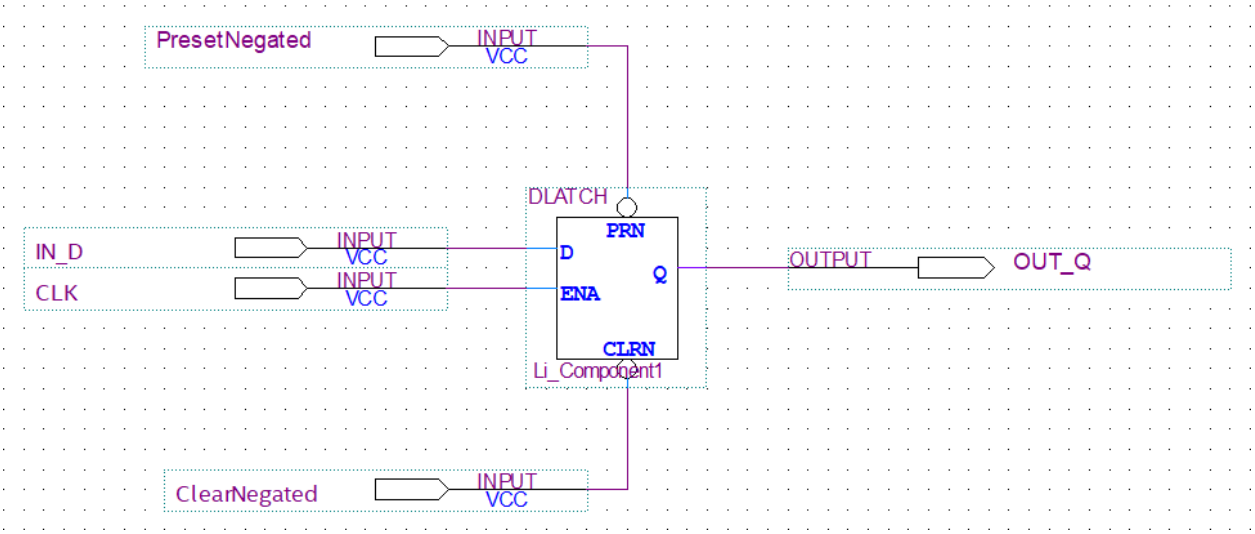

Figure 1: The image above is a screenshot of the D-Latch circuit with its inputs and outputs named accordingly.

Simulation:

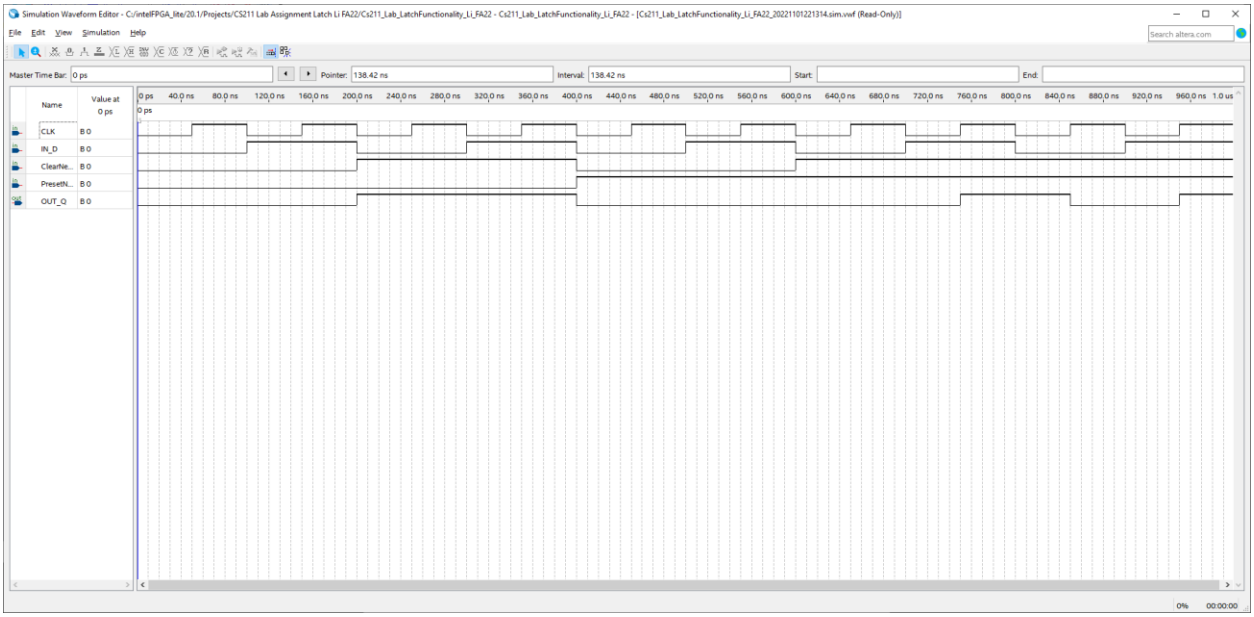

Figure 2: The image above is a screenshot of the vector waveform output of the D-Latch.

Enable (Clock)	D (IN D)	Q (OUT Q)
0	0	latch
0	1	latch
1	0	0
1	1	1

Figure 3: This is the truth table of the D-Latch.

Ignoring the OUT_Q when inputs “PresetNegated” and “ClearNegated” is at 00, 01, and 10 respectively we can map the OUT_Q to IN_D and CLK. This is because by ignoring these inputs at 00, 01, and 10 we are only looking at the functionality of the D-Latch when both PRN and CLRN is tied to 1. Looking at the waveform output we can map that when CLK and IN_D are both high (1) at 750ns to 800ns that OUT_Q is 1. When CLK is high and IN_D is low at 850ns to 900ns that OUT_Q is 0. Otherwise, we can notice by the pattern of the waveform that until CLK is at a rising edge that OUT_Q outputs the same value from before.

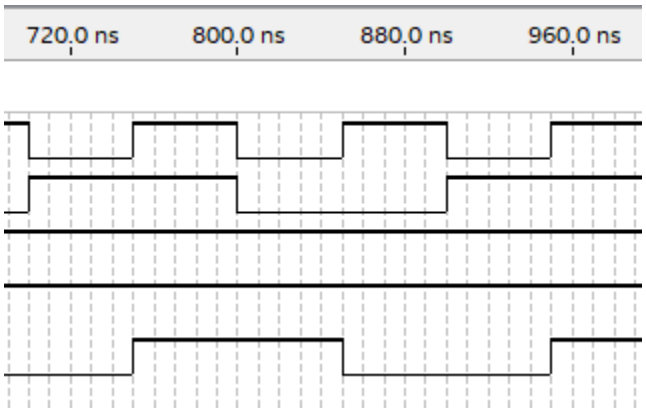

Figure 4: The image above is a close up of the VWF at 750ns to 900ns with input signals being CLK, IN_D, CLEARNEGATED, PRESETNEGATED, OUT_Q ordered from top to bottom respectively.

Conclusions:

In this laboratory exercise I learned how the D-Latch component functions which is that, when the enable input is high (1) you can store a bit (1 or 0) in the latch by setting D to whatever stored bit is desired. When the enable input is low (0), the latch ignores the input of D and holds onto the stored bit previously and outputting that stored value at Q.